DATA CONVERTER REFERENCE MANUAL VOLUME II



A/D CONVERTERS • V/F & F/V CONVERTERS •
SAMPLE/TRACK-HOLD AMPLIFIERS •
SWITCHES & MULTIPLEXERS • VOLTAGE REFERENCES •
DATA ACQUISITION SUBSYSTEMS •
ANALOG I/O PORTS • ASICs • POWER SUPPLIES

ANALOG DEVICES

How to Find Product Data in This Reference Manual

THIS IS VOLUME II OF THE DATA CONVERTER REFERENCE MANUAL

It and its companion volume contain Data Sheets, Selection Guides and a wealth of background information on signal conversion and a wide variety of components for mixed signal processing.

It is one member of a four-volume set of reference manuals describing and specifying Linear, Converter and Audio/Video products from Analog Devices, Inc., in IC, hybrid and assembled form for measurement, control and real-world signal processing.

IF YOU KNOW THE MODEL NUMBER

Turn to the product index at the back of the book and look up the model number. You will find the Volume-Section-Page location of any data sheet in this volume or Volume I. You will find additional references for product categories not included in the *Data Converter Reference Manual*.

If you're looking for a form-and-function-compatible version of a product originally brought to market by some other manufacturer (second source), you may find it by adding our "AD" prefix and looking it up in the index. Or call our nearest sales office.

IF YOU DON'T KNOW THE MODEL NUMBER

Find your functional group in the list on the opposite page, or in the listing for Volume I below. Turn directly to the appropriate Section. You will find a functional Selection Guide at the beginning of the Section. The Selection Guide (and the "Orientation" that usually accompanies it) will help you find the products that are the closest to satisfying your need. Use them to compare all products in the category by salient criteria. A comprehensive Table of Contents (of this volume) is provided for your convenience on pages 1–5 through 1–10.

IF YOU CAN'T FIND IT HERE OR IN VOLUME I . . . ASK!

If it's not a signal conversion product, it's probably in one of the two companion volumes, the *Linear Products Reference Manual* or the *Audio/Video Products Reference Manual*. If you don't already own these volumes, you can have them FREE by getting in touch with Analog Devices or the nearest sales office, or phoning 1-800-262-5643.

See the Worldwide Sales Directory on pages 12–12 and 12–13 at the back of this volume for our sales office phone numbers.

Contents of Other Reference Manuals

AUDIO/VIDEO PRODUCTS

- Operational Amplifiers
- Audio A/D Converters
- Video A/D Converters
- Audio D/A Converters
- Video D/A Converters
- Special Function Audio Products
- Special Function Video Products
- Digital Signal Processing Products
- Application Notes

DATA CONVERTER PRODUCTS (VOLUME I)

- D/A Converters
- S/D Converters
- Communications Products
- Digital Panel Meters
- Digital Signal Processing Products
- Bus Interface & Serial I/O Products
- Application Specific ICs
- Power Supplies

LINEAR PRODUCTS

- Operational Amplifiers
- Comparators
- Instrumentation Amplifiers
- Isolation Amplifiers
- Analog Multipliers/Dividers
- Log/Antilog Amplifiers
- RMS-to-DC Converters
- Mass Storage Components
- ATE Components
- Special Function Components
- Temperature Transducers
- Signal Conditioning Components & Subsystems
- Digital Panel Instruments
- Bus Interface & Serial I/O Products
- Automotive Components
- Application Specific ICs
- Power Supplies
- Component Test Systems

1992 DATA CONVERTER REFERENCE MANUAL

VOLUME II

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1

Introduction

Analog Devices designs, manufactures and sells worldwide sophisticated electronic components and subsystems for use in real-world signal processing. More than six hundred standard products are produced in manufacturing facilities located throughout the world. These facilities encompass all relevant technologies, including several embodiments of CMOS, BiMOS, bipolar and hybrid integrated circuits, each optimized for specific attributes—and assembled products in the form of potted modules, printed-circuit boards and instrument packages.

State-of-the-art technologies (including surface micromachining) have been utilized (and in many cases invented) to provide timely, reliable, easy-to-use advanced designs at realistic prices. Our popular IC products are available in both conventional and surface-mount packages (SOIC, LCC, PLCC), and many of our assembled products employ surface-mount technology to reduce manufacturing costs and overall size. A quarter-century of successful applications experience and continuing vertical integration insure that these products are oriented to user needs. The ongoing application of today's state-of-the-art and the invention of tomorrow's state-of-the-art processes strengthen the leadership position of Analog Devices in standard data-acquisition and signal-processing products and make us a strong contender in high performance mixed-signal ASICs.

MAJOR PROGRESS

Since publication of the selection guides in the *1990 Databook Series*, more than 120 significant new products have been introduced by Analog Devices; they run the gamut from brand new product categories and technologies to new standard products (with improvements in price, performance or design) to augmented second-source products. In addition, the Analog Devices line of IC products now includes the products of Precision Monolithics, Inc., which was acquired by Analog Devices in 1990. The new products are all classified and summarized in these volumes, along with existing products that are desirable for use in new designs.

Examples of the variety and innovation content of outstanding new ICs to be found in these two volumes include:

- the ADV7141/46/48 Edsun CEG/DAC™ family of monolithic RAM-DACs, designed to eliminate "jaggies" and improve color resolution in VGA displays (Vol. I)
- the AD28msp02 16-bit codec, a complete analog front end for high-performance voiceband DSP applications (Vol. I)
- the DAC-8800 and -8840 TrimDACs™, which eliminate pots and permit automatic trimming of offsets and gains in electronic circuits and systems (Vol. I)
- the AD7710/11/12 family of 21-bit sigma-delta a/d converters with complete on-chip signal conditioning (Vol. II)
- the AD9100 wideband low-distortion monolithic track-hold amplifier with 13 ns acquisition time to 0.1% (Vol. II)
- the AD1674 12-bit sampling a/d converter, a "faster, better, cheaper" upgrade for AD574/674/774 a/d converter sockets (Vol. II)
- the AD9020/9060 10-bit TTL/ECL flash a/d converters with sampling rates to 75 MSPS (Vol. II)
- the AD671 12-bit, 500 ns a/d converter (Vol. II).

Many more could have been added to this list.

CEG/DAC, TrimDAC and DSPatch are trademarks of Analog Devices, Inc.

2-VOLUME DATA CONVERTER REFERENCE MANUAL

This two-volume set provides comprehensive technical data on Analog Devices data-conversion products, which are involved in spanning the interface between analog and digital worlds. It is a companion to the *Linear Products Databook*, which provides similar data for analog-to-analog products. Both volumes contain:

- comprehensive data sheets and package information on a total of more than 350 significant product families
- orientation material and selection guides for finding products rapidly
- a representative list of available Analog Devices technical publications on real-world analog and digital signal processing
- our Worldwide Sales Directory
- the complete Product Index to all data-conversion and DSP products listed in these two volumes and all products listed in the Linear Products Databook.

Division of Product Groups between the Two Books

Volume I contains information on
- Digital-to-analog converters
- Synchro/resolver-to-digital converters
- Communications products
- Digital panel meters
- Digital signal processing products
- Bus interface and serial I/O products
- Application specific ICs
- Power supplies.

Volume II contains information on:
- Analog-to-digital converters
- Voltage-to-frequency and frequency-to-voltage converters
- Sample/track-hold amplifiers
- Switches and multiplexers
- Voltage references
- Data acquisition subsystems
- Analog I/O ports
- Application-specific ICs
- Power supplies.

The product data in this book are intended primarily for the majority of users who are concerned with new designs. For this reason, existing and available products that offer little if any unique advantage over newer products in future designs are listed in the Index, and data sheets may be available separately—but they are not published in this book.

TECHNICAL SUPPORT

Our extensive technical literature discusses the technology and applications of products for real-world signal processing. Besides tutorial material and comprehensive data sheets, including a large number in our Databooks, we offer Application Notes, Application Guides, Technical Handbooks (at reasonable prices), and several free serial publications; for example, *Analog Productlog* provides brief information on new products being introduced, and *Analog Dialogue*, our technical magazine, provides in-depth discussions of new developments in analog and digital circuit technology as applied to data acquisition, signal processing, control, and test. *DSPatch*™ is a quarterly newsletter that brings its readers up-to-date applications information on

our DSP products and the general field of digital signal processing. We maintain a mailing list of engineers, scientists, and technicians with a serious interest in our products. In addition to Databook catalogs—and general short-form selection guides—we also publish several short-form catalogs on specific product families. You will find typical publications described on pages 12–8 to 12–11 at the back of the book.

SALES AND SERVICE

Backing up our design and manufacturing capabilities and our extensive array of publications, is a network of distributors, plus sales offices and representatives throughout the United States and most of the world, staffed by experienced sales and applications engineers. Our Worldwide Sales Directory, as of the publication date, appears on pages 12–12 and 12–13 at the back of the book.

RELIABILITY

The manufacture of reliable products is a key objective at Analog Devices. The primary focus is the companywide Quality Improvement Process (QIP). In addition, we maintain facilities that have been qualified under such standards as MIL-M-38510 (Class B and Class S) for ICs in the U.S. and MIL-STD-1772 for hybrids. Many of our product —both proprietary and second-source—have qualified for JAN part numbers; others are in the process. A larger number of products—including many of the newer ones just starting the JAN qualification process—are specifically characterized on Standard Military Drawings (SMDs). Most of our ICs are available in versions that comply with MIL-STD-883C Class B, and many also comply with Class S. We publish a *Military Products Databook* for designers who specify ICs and hybrids for military contracts. The 1990 issue consists of two volumes with data on 343 product families; the 120 entries in the second of those volumes describe qualified products manufactured by our PMI Division. A newsletter, *Analog Briefings®*, provides current information about the status of reliability at ADI.

Our PLUS program makes available standard devices (commercial and industrial grades, plastic or ceramic packaging) for *any* user with demanding application environments, at a small premium. Subjected to stringent screening, similar to MIL-STD-883 test methods, these devices are suffixed "/+" and are available from stock.

PRODUCTS NOT FOUND IN THE SELECTION GUIDES

For maximum usefulness to designers of new equipment, we have limited the contents of selection guides to standard products most likely to be used for the design of new circuits and systems. If the model number of a product you are interested in is not in the Index, turn to page 12–4 at the back of this volume where you will find a list of older products for which data sheets are available upon request. On page 12–5 you will find a guide to substitutions (where possible) for products no longer available.

ICs embodying combinations of functions that you need but cannot find among our standard offerings may be available to meet your specific requirements as custom designs. Consult the section in this book on Application Specific ICs—and/or get in touch with Analog Devices.

PRICES

Accurate, up-to-date prices are an important consideration in making a choice among the many available product families. Since prices are subject to change, current price lists and/or quotations are available upon request from our sales offices and distributors .

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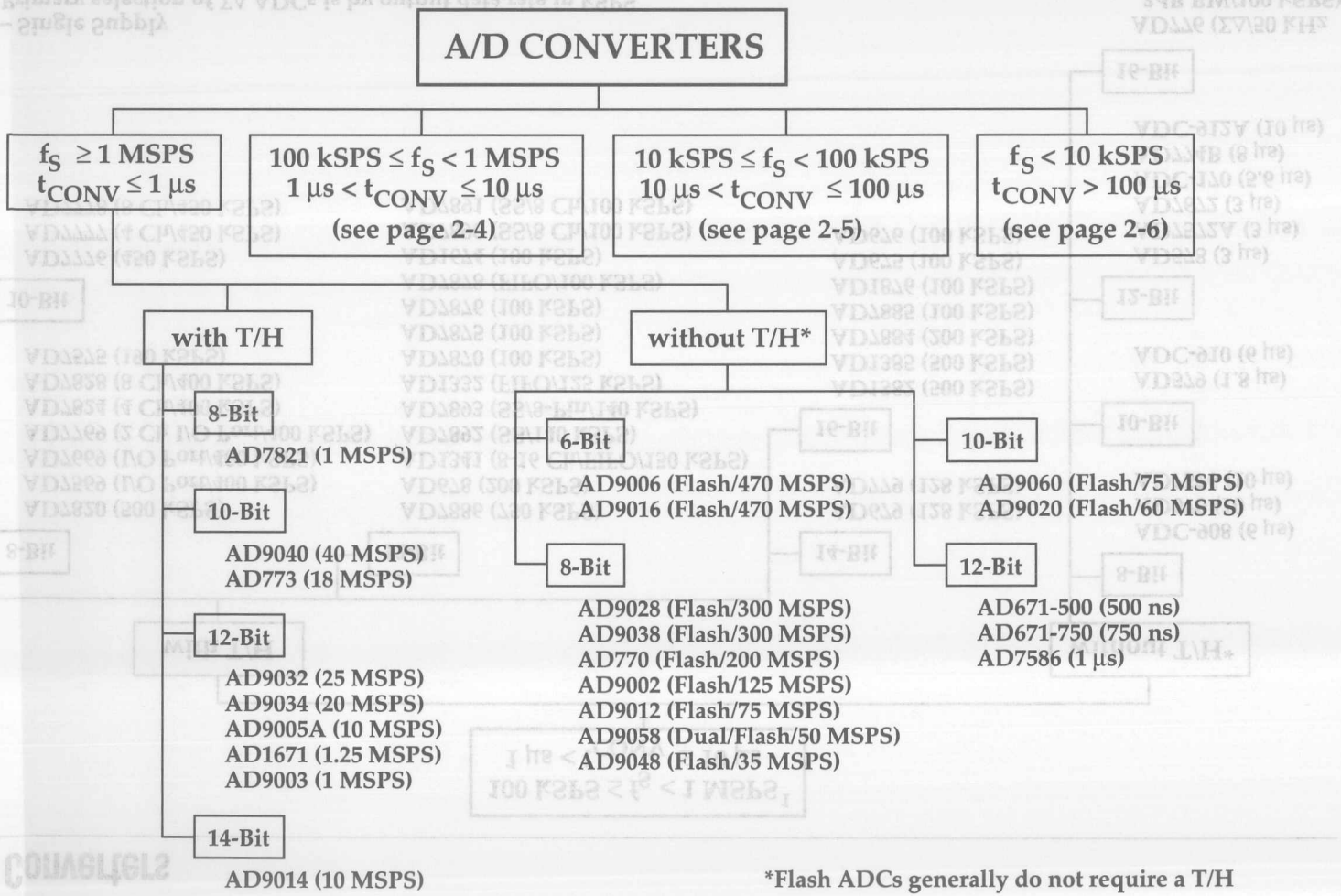
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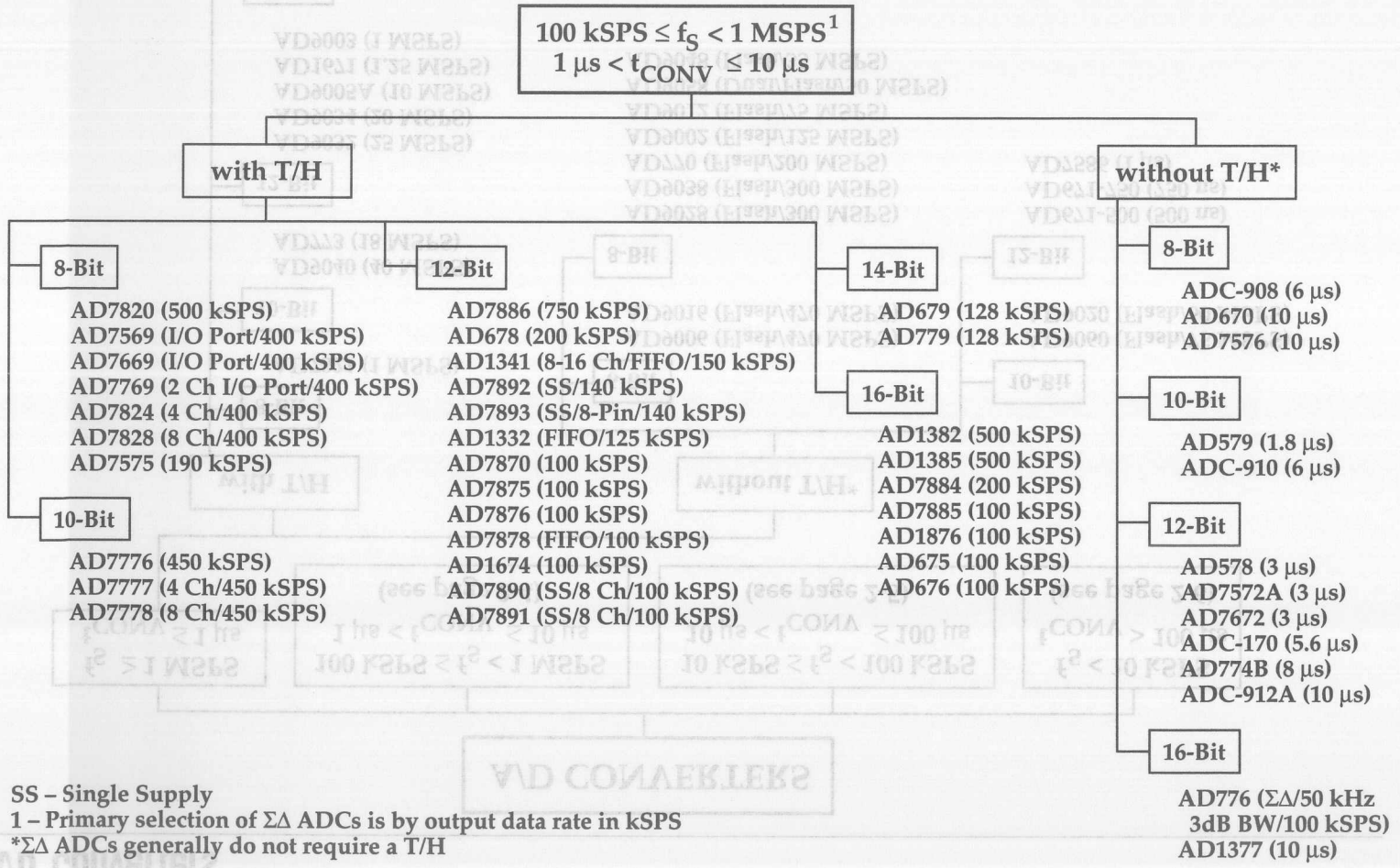
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Selection Tree
A/D Converters

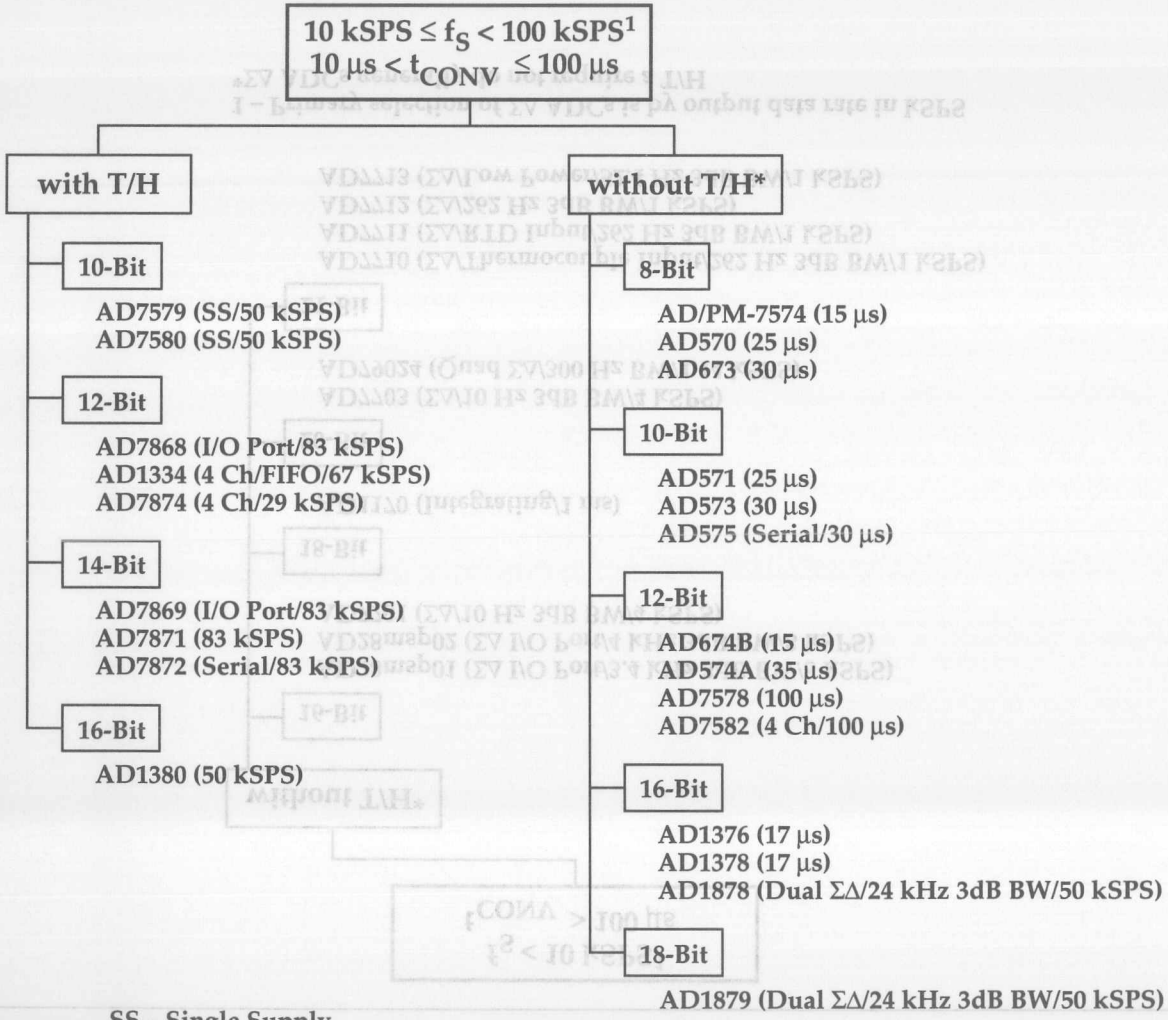


*Flash ADCs generally do not require a T/H

Selection Tree
A/D Converters

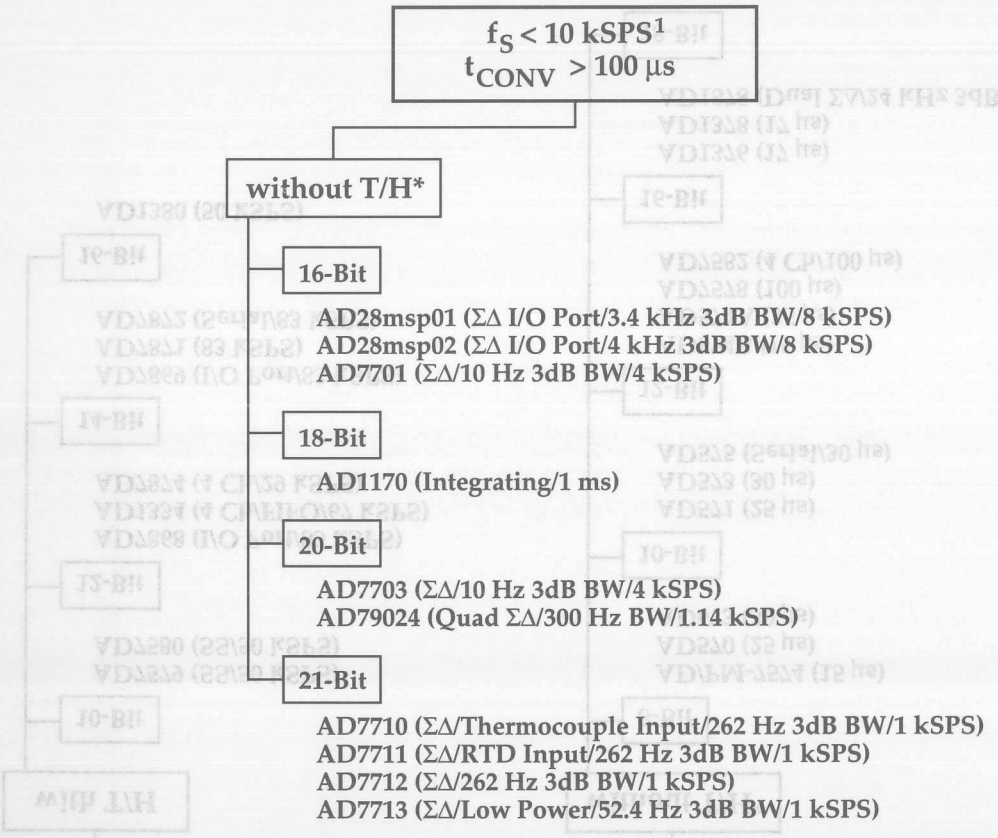


SS – Single Supply
1 – Primary selection of ΣΔ ADCs is by output data rate in kSPS
*ΣΔ ADCs generally do not require a T/H



SS – Single Supply
1 – Primary selection of ΣΔ ADCs is by output data rate in kSPS
*ΣΔ ADCs generally do not require a T/H

Selection Tree
A/D Converters



1 – Primary selection of ΣΔ ADCs is by output data rate in kSPS
*ΣΔ ADCs generally do not require a T/H

Selection Guide
Analog-to-Digital Converters

Sampling Converters

Model	Res Bits	Through-put Rate kSPS max	SHA BW kHz typ[1]	Reference Volt Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Range[5]	Page	Comments
AD7821	**8**	**1000**	**100**	**0–5 V, Ext**	**8, µP**	**2, 3, 4, 5, 6**	**I, M**	**C II 2–521**	**CMOS, Bipolar or Unipolar Operation**
AD7820	8	500	14	0-5 V, Ext	8, µP	2, 3, 4, 5, 6	I, M	C II 2–511	CMOS, 8-Bit Sampling ADC
AD7569	**8**	**400**	**200**	**Int**	**8, µP**	**2, 3, 4, 5, 6**	**C, I, M**	**C II 8–7**	**CMOS, Complete I/O Port with DAC, ADC, SHA, Amps and Reference**
AD7669	**8**	**400**	**200**	**Int**	**8, µP**	**2, 5, 6**	**C, I, M**	**C II 8–7**	**CMOS, Complete I/O Port with 2 DACs, ADC, SHA, Amps and Reference**
AD7769	**8**	**400**	**200**	**Ext**	**8, µP**	**2, 5**	**C**	**C II 8–27**	**CMOS, Complete 2-Channel I/O Port with Input/Output Signal Conditioning**
AD7824	**8**	**400**	**10**	**0–5 V, Ext**	**8, µP**	**2, 3, 6**	**C, I, M**	**C II 2–533**	**CMOS, 4-Channel, 8-Bit Sampling ADC**
AD7828	**8**	**400**	**10**	**0–5 V, Ext**	**8, µP**	**2, 3, 4, 5**	**C, I, M**	**C II 2–533**	**CMOS, 8-Channel, 8-Bit Sampling ADC**
AD7575	8	190	50	1.23 V, Ext	8, µP	2, 3, 4, 5	C, I, M	C II 2–323	CMOS, Low Cost
***AD7776**	**10**	**500**	**50**	**2.0 V, Int/Ext**	**10, µP**	**2, 6**	**C, I**	**C II 2–509**	**CMOS, Single Channel Complete Sampling ADC, Single Supply, Twos Complement Output Code**
***AD7777**	**10**	**500**	**50**	**2.0 V, Int/Ext**	**10, µP**	**2, 6**	**C, I**	**C II 2–509**	**CMOS, 4-Channel Complete ADC for Single or Simultaneous Dual Channel Sampling, Single Supply**
***AD7778**	**10**	**500**	**50**	**2.0 V, Int/Ext**	**10, µP**	**10**	**C, I**	**C II 2–509**	**CMOS, 8-Channel Complete ADC for Single or Simultaneous Dual Channel Sampling, Single Supply**
AD7579	**10**	**50**	**25**	**2.5 V, Ext**	**8, µP**	**2, 3, 4, 5**	**C, I, M**	**C II 2–347**	**CMOS, Low Cost 10-Bit Sampling ADC**
AD7580	**10**	**50**	**25**	**2.5 V, Ext**	**10, µP**	**2, 3, 4, 5**	**C, I, M**	**C II 2–347**	**CMOS, Low Cost 10-Bit Sampling ADC**
AD9003	**12**	**1000**	**10000**	**Int**	**12**	**8**	**C**	**C II 2–689**	**12-Bit, 1 MSPS ADC, Single 40-Pin DIP**
***AD1671**	**12**	**1250**	**2000**	**2.5 V, Int**	**12**	**1, 2, 4, 5**	**C, I, M**	**C II 2–259**	**Complete, Monolithic 12-Bit, 1.25 MSPS ADC**
***AD7886**	**12**	**750**	**1000**	**5 V, Ext**	**12, µP**	**2, 3, 5**	**C, I**	**C II 2–637**	**CMOS, 12-Bit 750 kSPS Sampling ADC**
AD678	**12**	**200**	**1000**	**5 V, Int**	**8/12, µP**	**1, 2, 14**	**C, I, M**	**C II 2–137**	**BiMOS, High Impedance High Bandwidth Sampling Input, 10 V Range, AC/DC Tested**
***AD1341**	**12**	**150**	**150**	**10 V, Int**	**16, µP**	**12**	**C, M**	**C II 7–25**	**High Speed 8/16 Channel DAS**
***AD7893**	**12**	**140**	**70**	**2.5 V, Ext**	**Serial**	**2, 3, 6**	**I, M**	**C II 2–669**	**CMOS, Single Supply Sampling ADC in 8-Pin Package**
***AD7892**	**12**	**140**	**70**	**2.5 V, Ext**	**8/12/Serial, µP**	**2, 3, 6**	**I, M**	**C II 2–663**	**±10 V Input, Single Supply Sampling ADC**
AD1332	**12**	**125**	**125**	**−5 V, Int**	**12, µP**	**1**	**I, M**	**C II 7–17**	**Complete 12-Bit 125 kHz Sampling ADC for Digital Signal Processing, On-Chip FIFO**

[1]X indicates that the internal SHA bandwidth is not specified in kHz.
[2]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.
[3]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 13-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.
[4]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-In-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92.
[5]Temperature Ranges: C = Commercial, 0 to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.
*New product since the publication of the most recent Databooks.

Selection Guide
Analog-to-Digital Converters

Sampling Converters

Model	Res Bits	Through-put Rate kSPS max	SHA BW kHz typ[1]	Reference Volt Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Range[5]	Page	Comments
*AD7874	12	29	500	Int (+3 V), Ext	12, µP	2, 3, 4, 6	C, I, M	C II 2–579	CMOS, Simultaneous Sampling 4-Channel ADC for ±10 V Input Signals
AD7870	12	100	500	3 V, Int	8/12/Serial, µP	2, 3, 4, 5	C, I, M	C II 2–545	CMOS, 100 kHz Throughput, ±3 V Input
*AD7875	12	100	500	3 V, Int	8/12/Serial, µP	2, 3, 5	C, I, M	C II 2–545	CMOS 100 kHz Throughput, 0–5 V Input
*AD7876	12	100	500	3 V, Int	8/12/Serial, µP	2, 3, 6	I, M	C II 2–545	CMOS, 100 kHz Throughput, ±10 V Input
AD7878	12	100	500	3 V, Int	12, µP	2, 3, 4, 5	C, I, M	C II 2–595	CMOS, 100 kHz Throughput, ±3 V Input, On-Chip FIFO
*AD1674	12	100	500	10 V, Int	8/12, µP	1, 2, 6	C, I, M	C II 2–269	Complete AD574A Pinout Compatible, Sampling Input, AC/DC Tested
*AD7890	12	100	50	2.5 V, Ext	Serial	2, 3, 6	I, M	C II 2–653	±10 V Input 8-Channel Single Supply Sampling ADC
*AD7891	12	100	50	2.5 V, Ext	12, µP	10	I, M	C II 2–659	±10 V Input 8-Channel Single Supply Sampling ADC
*AD7868	12	83	500	3 V, Int	Serial, µP	2, 3, 6	I, M	C II 8–79	CMOS, Complete I/O Port with 12-Bit ADC and 12-Bit DAC
AD1334	12	67	235	−5 V, Int	12, µP	1	I, M	C II 7–21	Four- Channel 67 kHz 12-Bit Sampling ADC, On-Chip FIFO
*AD7880	12	66	33	5 V, Ext	12, µP	2, 3, 6	I	C II 2–611	Single +5 V Supply, Low Power Shutdown
AD368	12	50	40–1000	6.3 V, Int	12	1	I, M	C II 12–4	Complete 12-Bit ADC, PGA with Gains of 1, 8, 64, 512
AD369	12	50	40–1000	6.3 V, Int	12	1	I, M	C II 12–4	Complete 12-Bit ADC, PGA with Gains of 1, 10, 100, 500
AD363R	12	25		10 V, Int	12, µP	1	C, M	C II 7–5	16-Channel, 12-Bit DAS
AD364R	12	20		10 V, Int	12, µP	1	C, M	C II 7–5	High Speed, 16-Channel, 12-Bit DAS with Three-State Buffered Output
AD679	14	128	1000	5 V, Int	8, µP	1, 2, 14	C, I, M	C II 2–149	BiMOS, High Impedance, High Bandwidth Sampling Input, 10 V Input Range, AC/DC Tested
AD779	14	128	1000	5 V, Int	14, µP	1, 2, 14	C, I, M	C II 2–191	BiMOS, High Impedance, High Bandwidth Sampling Input, 10 V Input Range, AC/DC Tested
*AD7869	14	83	500	3 V, Int	Serial	2, 3, 6	C, I	C II 8–95	CMOS, Complete I/O Port with 14-Bit DAC and 14-Bit ADC
AD7871	14	83	500	3 V, Int	8/14/Serial, µP	2, 3, 5	C, I, M	C II 2–563	CMOS, Complete Sampling ADC, ±3 V Input
AD7872	14	83	500	3 V, Int	Serial, µP	2, 3, 6	C, I, M	C II 2–563	CMOS, Complete, Serial Interface, 16-Pin DIP/SOIC
DAS1152	14	25	X	10 V, Int	14	Module	I	C II 7–65	14-Bit High Accuracy Sampling ADC
DAS1157	14	18	X	10 V, Int	14	Module	I	C II 7–69	Low Power Sampling ADC
DAS1153	15	20	X	10 V, Int	15	Module	I	C II 7–65	15-Bit High Accuracy Sampling ADC
DAS1158	15	18	X	10 V, Int	15	Module	I	C II 7–69	Low Power, 15-Bit Sampling ADC
*AD1382	16	500	2200	10 V, Int	8, µP	1	C	C II 2–239	High Speed, Guaranteed Dynamic Performance
*AD1385	16	500	2200	10 V, Int	8, µP	1	C, M	C II 2–255	Similar to AD1382 with Autocalibration Ability, Guaranteed Dynamic Performance
*AD7884	16	166	83	3 V, Ext	16, µP	2, 3, 5	I, M	C II 2–625	CMOS, Low Power (250 mW), 5.3 µs Conversion
*AD7885	16	166	83	3 V, Ext	8, µP	2, 3, 5	I, M	C II 2–625	Similar to AD7884, 28-Pin Package, Byte Output
*AD1876	16	100	1000	3–7 V, Ext	Serial	2	C	C II 2–283	Autocalibrating, 16-Pin DIP ADC, AC Tested

Model	Res Bits	Throughput Rate kSPS max	SHA BW kHz typ[1]	Reference Volt Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Range[5]	Page	Comments
***AD675**	**16**	**100**	**1000**	**3–10 V, Ext**	**8/Serial, µP**	**1, 2**	**C, I, M**	**C II 2–121**	**Autocalibrating, 24-Pin DIP ADC, AC/DC Tested**
***AD676**	**16**	**100**	**1000**	**3–10 V, Ext**	**16, µP**	**1, 2**	**C, I, M**	**C II 2–123**	**Similar to AD675 but in 28-Pin DIP, Parallel Output**
AD1380	**16**	**50**	**900**	**Int**	**16/Serial**	**1**	**C**	**C II 2–231**	**Low Cost, 16-Bit Sampling ADC**
DAS1159	16	18	X	10 V, Int	16	Module	I	C II 7–69	Low Power, 16-Bit Sampling ADC

Nonsampling Converters

Model	Res Bits	Conv Rate µs max	Reference Voltage Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Range[5]	Page	Comments
ADC-908	8	6.0	−10 V, Ext	8, µP	2, 3, 4, 6	C, I, M	C II 12–4	CMOS, +5 V Operation, Fast
AD670	8	10	Int	8, µP	1, 2, 4, 5	C, I, M	C II 2–69	Single +5 V Supply, Including In-Amp and Reference
AD7576	8	10	1.23 V, Ext	8, µP	2, 3, 4, 5	C, I, M	C II 12–4	CMOS, Low Cost, Single Supply
PM-7574	8	15.0	−10 V, Ext	8, µP	2, 3, 4, 6	C, I, M	C II 12–4	CMOS, +5 V Operation
AD7574	**8**	**15**	**−10 V, Ext**	**8, µP**	**2, 3, 4**	**C, I, M**	**C II 2–315**	**CMOS, +5 V Operation**
AD570	8	25	Int	8	1	C, M	C II 2–25	
AD673	8	30	Int	8, µP	1, 2, 5	C, M	C II 2–97	
AD7581	8	66.7	−5 V to (−15 V), Ext	8, µP	2, 3, 5	C, I	C II 2–363	CMOS 8-Bit ADC
AD579	10	1.8	10 V, Int	10/Serial	1	C, M	C II 2–61	High Speed with Low Power
ADC-910	**10**	**6.0**	**2.5 V, Int**	**8, 10, µP**	**3**	**C, I, M**	**C II 2–819**	**Bipolar, Fast with Byte Output**
AD571	10	25	Int	10	1	C, M	C II 2–25	Complete 10-Bit ADC
AD573	**10**	**30**	**Int**	**8/10, µP**	**1, 2, 5**	**C, M**	**C II 2–33**	**Complete 10-Bit ADC, Byte or Parallel Interface**
AD575	10	30	Int	Serial	1, 2	C, M	C II 2–53	Complete 10-Bit ADC with Serial Interface
AD671-500	**12**	**0.5**	**5 V, Ext**	**12**	**1, 2**	**C, M**	**C II 2–81**	**12-Bit 500 ns Monolithic ADC**
AD671-750	**12**	**0.75**	**5 V, Ext**	**12**	**1, 2**	**C, M**	**C II 2–81**	**12-Bit 750 ns Monolithic ADC**
***AD7586**	**12**	**1**	**−4 V, Ext**	**12, µP**	**1, 2, 5**	**C, I**	**C II 2–383**	**CMOS 12-Bit, 1 MHz ADC**
AD578	12	3	10 V, Int	12	1	C, M	C II 2–61	Complete, 3 µs, 12-Bit ADC
***AD7572A**	**12**	**3**	**Int**	**8/12, µP**	**2, 3, 4, 6**	**C, I, M**	**C II 2–303**	**Improved Version of Industry Standard**
AD7672	12	3	−5 V, Ext	12, µP	2, 3, 4, 5	C, I, M	C II 2–391	CMOS, Unipolar or Bipolar, −12 V, +5 V Supply
AD5240	12	5	6.3 V, Int	12	1	C, M	C II 2–809	Industry Standard
AD7572	12	5	−5.25 V, Int	8/12, µP	2, 3, 4, 5	C, I, M	C II 2–299	CMOS 12-Bit ADC
***ADC-170**	**12**	**5.6**	**−5.25 V, Ext**	**Serial**	**2, 3, 6**	**I, M**	**C II 2–817**	**Complete, 3 µs, 12-Bit ADC in 8-Pin Mini-DIP**
***AD774B**	**12**	**8**	**10 V, Int**	**8/12, µP**	**1, 2, 6**	**C, I, M**	**C II 2–109**	**Faster Version of AD674B with 8 µs Conversion**

[1]X indicates that the internal SHA bandwidth is not specified in kHz.

[2]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.

[3]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 13-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.

[4]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-in-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92.

[5]Temperature Ranges: C = Commercial, 0 to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.

Boldface Type: Product recommended for new design.

*New product since the publication of the most recent Databooks.

Selection Guide
Analog-to-Digital Converters

Nonsampling Converters

Model	Res Bits	Conv Rate µs max	Reference Voltage Int/Ext[1]	Bus Interface Bits[2]	Package Options[3]	Temp Range[4]	Page	Comments
AD ADC84/85	12	10	6.3 V, Int	12	1	C, I, M	C II 2–809	Industry Standard
***ADC-912A**	**12**	**10**	**−5 V, Ext**	**12, µP**	**2, 3, 6**	**I, M**	**C II 2–831**	**CMOS, Improved Version of ADC-912**
ADC-912	12	12.5	−5 V, Ext	12, µP	2, 3, 6	C	C II 12–4	CMOS, Low Transition Noise
AD5210	12	13	−10 V, Int/Ext	12	1	I, M	C II 12–4	Industry Standard (AD5211/12/14/15)
AD674A	12	15	10 V, Int	8/12, µP	1	C, M	C II 2–105	Complete 12-Bit ADC, Industry Standard Pinout
***AD674B**	**12**	**15**	**10 V, Int**	**8/12, µP**	**1, 2, 6**	**C, I, M**	**C II 2–109**	**Improved Monolithic Version of AD674A and AD574A**
AD572	12	25	10 V, Int	12	1	I, M	C II 2–31	12-Bit Successive Approximation ADC
AD ADC80	12	30	6.3 V, Int	12	1	I	C II 2–803	Industry Standard
AD574A	**12**	**35**	**10 V, Int**	**8/12, µP**	**1, 2, 4, 5**	**C, M**	**C II 2–41**	**Complete ADC with Reference and Clock**
AD5200	12	50	−10 V, Int/Ext	12	1	I, M	C II 12–4	Industry Standard (AD5201/02/04/05)
AD7578	**12**	**100**	**5 V, Ext**	**8, µP**	**1, 2**	**C, I, M**	**C II 2–335**	**CMOS, 1 LSB Total Unadjusted Error**
AD7582	**12**	**100**	**5 V, Ext**	**8, µP**	**1, 2, 5**	**C, I, M**	**C II 2–371**	**CMOS, 4 Channel, 1 LSB Total Unadjusted Error**
AD1377	16	10	Int	16, Serial	1	C	C II 2–215	Complete, High Speed 16-Bit ADC Operation over −25°C to +85°C
AD1376	16	17	Int	16, Serial	1	C	C II 2–215	Complete 16-Bit Converter; Industry Standard Pinout
***AD1378**	**16**	**17**	**Int**	**16, Serial**	**1**	**M**	**C II 2–223**	**Complete 16-Bit Converter; MIL Temp Range; Industry Standard Pinout**
ADC1140	16	35	10 V, Int	16	Module	C	C II 2–843	16-Bit ADC, Operates over −25°C to +85°C Temperature Range
AD ADC71	16	50	6.3 V, Int	16	1	C	C II 2–801	Industry Standard
AD ADC72	16	50	6.3 V, Int	16	1	C, I	C II 2–801	Industry Standard
AD1170	**18**	**1000**	**5 V, Int**	**8**	**2**	**C**	**C II 2–203**	**7 to 22-Bit Programmable Integrating ADC**

High Speed ADCs

Model	Res Bits	Through-put Rate MSPS min	Full Power BW MHz typ	Reference Voltage Int/Ext[1]	Bus Interface Bits[2]	Package Options[3]	Temp Range[4]	Page	Comments
AD9006	6	470	550	±1 V, Ext	6, µP	4, 12	C, M	C II 2–705	470 MSPS, 6-Bit ADC; 8.0 pF Input Capacitance
AD9016	6	550		±1 V, Ext	Dual 6, µP	4, 12	C, M	C II 2–705	AD9006 with 1:2 Demultiplexed Data Output Demultiplexing Circuitry
AD9000	6	50	20	0.5–2 V, Ext	6	1, 3	C, M	C II 2–673	MIL-STD-883, Rev. C, Devices Available; Low Error Rate
AD9028	8	300	250	–2 V, Ext	8	4	C, M	C II 2–753	300 MSPS, 8-Bit ADC, Guaranteed Dynamic Performance
AD9038	8	300	250	–2 V, Ext	Dual 8	4	C, M	C II 2–753	AD9028 with On-Board 1:2 Demultiplexed Data Outputs
AD770	8	200	250	±2 V, Ext	8	1	C, M	C II 2–161	High Bandwidth, Error Correction
AD9002	8	125	160	0.1–(−2.1) Ext	8	1, 4	I, M	C II 2–681	Single Supply, Low Power, Low Input Capacitance, MIL-STD-883, Rev. C Device Available
AD9012	8	75	160	−2 V, Ext	8	3, 4	I, M	C II 2–721	TTL Outputs, Low Power, Low Input Cap
*AD9058	8	50	175	+2 V, Int	8	1, 5, 14	C, M	C II 2–781	Dual 8-Bit, TTL Output
AD9048	8	35	15	−2 V, Ext	8, µP	2, 3, 5, 12	C, M	C II 2–773	35 MSPS, 8-Bit Video ADC, 16 pF Input Capacitance
*AD9020	10	60	175	±1.75 V, Ext	10	4, 12	C, M	C II 2–741	Fastest 10-Bit TTL Monolithic ADC
*AD9060	10	75	175	±1.75 V, Ext	10	4, 12	C, M	C II 2–789	Fastest 10-Bit ECL Monolithic ADC
*AD9040	10	40	50	+1.2 V	10	3, 4, 5	C, M	C II 2–769	Low Cost, High Performance 10-Bit TTL Monolithic
*AD773	10	18	75	+2.5, Ext	10	1, 2	C, M	C II 2–173	Low Power, 10-Bit 18 MSPS with On-Chip T/H
*AD9032	12	25	150	Int	12	8	C, M	C II 2–765	World's Fastest Complete 12-Bit ADC
*AD9034	12	20	150	Int	12	8	C, M	C II 2–765	20 Ms
*AD9005A	12	10	38	Int	12	8	C, M	C II 2–697	Complete 12-Bit ADC with T/H, Reference and Timing Circuitry
*AD1671	12	1.25	2	2.5 V, Int	12	1, 2, 4, 5	C, I, M	C II 2–259	Complete, Monolithic 12-Bit, 1.25 MSPS ADC
AD9003	12	1	10	Int	12	8	C	C II 2–689	12-Bit, 1 MSPS ADC, Single 40-Pin DIP
*AD7886	12	.75	1	+5 V, Ext	12, µP	1, 2, 5	C, I, M	C II 2–637	CMOS, 12-Bit 750 kSPS Sampling ADC
*AD9014	14	10	60	Int	14	Board	C	C II 2–729	Wide Spurious Free Dynamic Range

[1]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.

[2]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.

[3]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-In-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92.

[4]Temperature Ranges: C = Commercial, 0 to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.

Boldface Type: Product recommended for new design.

*New product since the publication of the most recent Databooks.

Selection Guide
Analog-to-Digital Converters

Sigma-Delta ADCs

Model	Res Bits	Input BW kHz	Through-put Rate kHz	Reference Voltage Int/Ext[1]	Bus Interface Bits[2]	Package Options[3]	Temp Range[4]	Page	Comments
*AD776	16	50	100 to 400	2 V, Int	Serial	1, 2	C, I, M	C II 2–189	16-Bit 100 kSPS Oversampling ADC, Single Supply
*AD1878	16	24	2.5 to 50	3 V, Int	Serial	2	C	C II 2–295	Similar to AD1879 with 16-Bit Resolution
*AD7701	16	10 Hz	4	2.5 V, Ext	Serial, µP	2, 3, 6	I, M	C II 2–403	16-Bit Sigma-Delta ADC, 0.1–10 Hz Input Bandwidth
*AD28msp02	16	4	8	2.5, Ext	Serial, µP	6	C	C I 4–25	Complete Voice Band Linear Codec with On-Chip Filtering, Single Supply
*AD28msp01	16	3.4	7.2/8.0/9.6	2.5, Ext	Serial, µP	6	C	C I 4–9	Complete Analog Front End for High Performance, DSP-Based Modems, Single Supply
*AD1879	18	24	2.5 to 50	3 V, Int	Serial	2	C	C II 2–297	Dual Channel, High Performance Stereo 18-Bit Oversampled ADC
*AD79024	20	18.5 to 300 Hz	0.075 to 1.145	2.5 V, Int	Serial	2, 6	C	C II 7–57	Quad 20-Bit Sigma Delta ADC, Low Power with BW up to 300 Hz
*AD7703	20	10 Hz	4	2.5 V, Ext	Serial, µP	2, 3, 6	I, M	C II 2–419	20-Bit Sigma-Delta ADC, 0.1–10 Hz Input Bandwidth
*AD7710	21	DC to 262 Hz	0.01 to 1.0	2.5 V, Int	Serial, µP	2, 3, 6	I, M	C II 2–435	21-Bit Sigma-Delta Signal Conditioning ADC for Thermocouple or mV Input
*AD7711	21	DC to 262 Hz	0.01 to 1.0	2.5 V, Int	Serial, µP	2, 3, 6	I, M	C II 2–457	Similar to AD7710 but for RTD or mV Input
*AD7712	21	DC to 262 Hz	0.01 to 1.0	2.5 V, Int	Serial, µP	2, 3, 6	I, M	C II 2–479	Similar to AD7710 with Higher Input Voltage Range, More General Purpose
*AD7713	21	DC to 52.4 Hz	2.0 to 200 Hz	2.5 V, Ext	Serial, µP	2, 3, 6	I, M	C II 2–501	Loop Powered 21-Bit Sigma-Delta Signal Conditioning ADC

Multiplexed ADCs

Model	Res Bits	# Chan	Conv Time µs	SHA BW kHz	Reference Volt Int/Ext[1]	Bus Interface Bits[2]	Package Options[3]	Temp Range[4]	Page	Comments
AD7769	**8**	**2**	**2.5**	**200**	**Ext**	**8, µP**	**2, 5**	**C**	**C II 8–27**	**CMOS, Complete 2-Channel I/O Port with Input/Output Signal Conditioning**
AD7824	**8**	**4**	**2.5**	**10**	**0–5 V, Ext**	**8, µP**	**2, 3, 6**	**C, I, M**	**C II 2–533**	**CMOS, On-Chip Track-Hold**
AD7828	**8**	**8**	**2.5**	**10**	**0–5 V, Ext**	**8, µP**	**2, 3, 4, 5**	**C, I, M**	**C II 2–533**	**CMOS, On-Chip Track-Hold**
AD7581	8	8	66.7		−10 V, Ext	8, µP	2, 3, 5	C, I	C II 2–363	CMOS, 8-Channel DAS
***AD1341**	**12**	**8/16**	**6.67**		**10 V, Int**	**16, µP**	**12**	**C, M**	**C II 7–25**	**High Speed, 16-Channel Programmable 12-Bit DAS with 25 ns Bus Interface**
AD1334	**12**	**4**	**15**	**235**	**−5 V, Int**	**12, µP**	**1**	**I, M**	**C II 7–21**	**Four-Channel 65 kHz 12-Bit Sampling ADC for Digital Signal Processing, On-Chip FIFO**
***AD7874**	**12**	**4**	**32.5 (for 4 Channels)**	**500**	**3 V Int**	**12, µP**	**2, 3, 6**	**C, I, M**	**C II 2–579**	**CMOS, Simultaneous Sampling Four-Channel 29 kHz ADC for ±10 V Input Signals**
AD363R	12	8/16	40		10 V, Int	12, µP	1	C, M	C II 7–5	High Speed, 16-Channel, 12-Bit DAS
AD364R	12	8/16	50		10 V, Int	12, µP	1	C, M	C II 7–5	16-Channel, 12-Bit DAS with Three-State Buffers
AD7582	**12**	**4**	**100**		**4 V–6 V, Ext**	**12, µP**	**1, 2, 5**	**C, I, M**	**C II 2–371**	**CMOS, 1 LSB Total Unadjusted Error**
***AD7890**	**12**	**8**	**10**	**500**	**2.5 V, Ext**	**Serial, µP**	**2, 3, 6**	**I, M**	**C II 2–653**	**CMOS, 8-Channel Multiplexed ADC for ±10 V Input Signals**
***AD7891**	**12**	**8**	**10**	**500**	**2.5 V, Ext**	**12, µP**	**10**	**I, M**	**C II 2–659**	**CMOS, 8-Channel Multiplexed ADC for ±10 V Input Signals**

[1]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.

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Boldface Type: Product recommended for new design.

*New product since the publication of the most recent Databooks.

Orientation
Analog-to-Digital Converters

FACTORS IN CHOOSING AN A/D CONVERTER

This section contains technical data and selection guides for *stand-alone general- and special-purpose analog-to-digital converters* (ADCs), including many *sampling* types. Devices and subsystems that perform analog-to-digital conversion functions are also to be found in many other sections of this reference manual; they include ICs (general purpose and application specific), multichip modules, and larger packages:

- V/F and F/V Converters (for low noise, high resolution conversion applications)
- Synchro- and Resolver-to-Digital Converters (for position- and motion-control applications)
- Data Acquisition Subsystems (for applications requiring signal conditioning combined with conversion)
- I/O Ports (for applications requiring both A/D & D/A conversion)
- Bus Interface and Serial I/O Products (subsystems)
- Digital Panel Meters
- ASICs (systems-on-a-chip for custom applications)
- Communications Products (codecs for modems, DSP peripherals, etc.)

The devices in this section include approximately 80 different families of analog-to-digital converters (ADCs) constructed using elements of a few basic architectures. If one were to consider all the variations, there would be hundreds of different types among which to choose. Why so many?

The answer is found in the diversity of real-world applications. Besides the key parameters, *resolution* and *speed*, many other considerations influence the choice of converter for a given application. Among the degrees of freedom are static and dynamic accuracy, digital data interface, control interface and timing, sample-and-hold capability, the analog signal, reference requirements, calibration capability, number of channels, power consumption, environmental requirements, package constraints, and software-related issues.

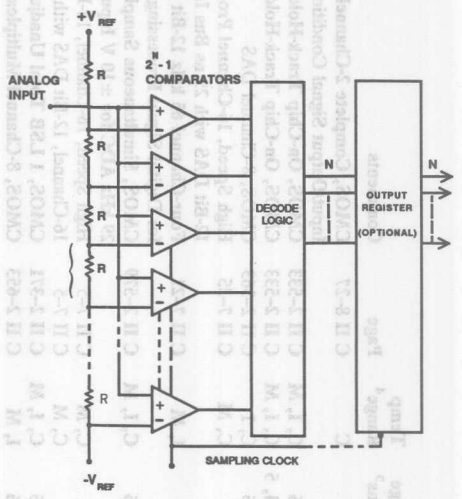
In this section, we discuss the various types of converter architectures that have evolved to deal with these considerations, followed by a glossary that includes definitions of the most-important specifications and many additional terms. Much additional information can be found in books listed in the Technical Publications section, starting on page 12–8, particularly the Analog Devices *High-Speed Design Seminar* (1990) and *Mixed-Signal Design Seminar* (1991) and the classic *Analog-Digital Conversion Handbook* from Prentice Hall (1986); all of these can be purchased from Analog Devices at reasonable cost.

FUNCTIONAL CHARACTERISTICS

Direct Conversion

In concept, the simplest—and fastest—A/D converter is one that performs a conversion directly. The basic architectural element of all A/D converters is a 1-bit converter, the comparator. If the input signal, applied to the + input (for example), is greater than a reference, applied to the − input, the output goes high ("1"); if the input signal is less, the output goes low ("0").

A "*flash*"—or direct—converter provides the fastest multibit conversion. The basic n-bit flash converter typically consists of $2^n - 1$ comparators* connected in parallel, with references spaced $V_{FS}/2^n$ (i.e., 1 LSB) apart; if the input signal increases, more comparators go high. The latched comparator outputs are combined by a priority encoder to form parallel n-bit digital words. An example of flash converter is the 10-bit AD9060, which can convert at a rate of 75 megasamples per second.



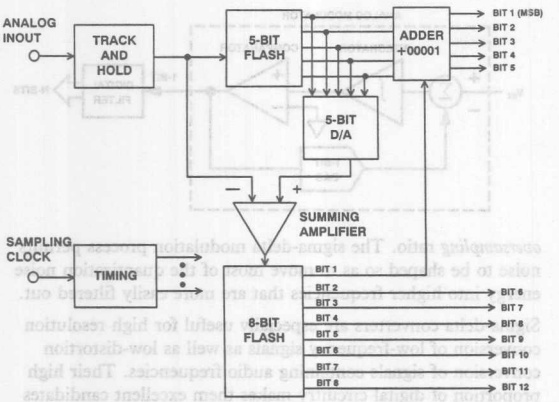
The space, input capacitance, and power required by large numbers of comparators have historically limited the resolution available with direct conversion. For this reason, most of the converters in use today perform a sequence of partial direct conversions and/or rely on an indirect method involving time integrations.

Partial Conversions in Sequence

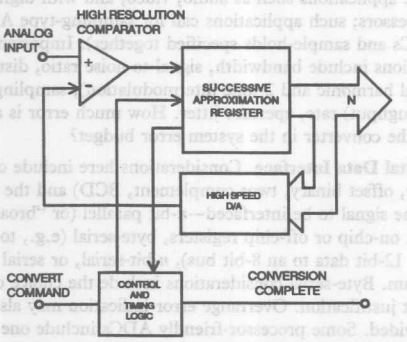
Converters in this class perform several conversions involving one or more bits to arrive at the complete n-bit conversion.

- *Subranging Converters* use two or more steps of lower-resolution flash conversion to convert an analog signal at high speeds with resolutions of up to 14 bits (e.g., the 14-bit, 10 MSPS hybrid AD9014, and the 12-bit, 500 ns monolithic AD671). For example, in performing an n-bit conversion using two steps of subranging, first a coarse m-bit conversion is performed, then the result is converted back to one of 2^m levels—using a D/A converter with at least n-bit accuracy—and compared with the input. The difference is then converted with a k-bit converter (where $k + m \geq n$) and the two outputs are combined. If $k + m > n$, digital correction may be used to eliminate overlap errors.

*An efficient variation of the flash converter, invented at Analog Devices (U.S. Patent 4,928,103) uses one-half as many input comparators.



- *Successive Approximations*. In this popular technique, a single comparator is used to compare the input with the output of an n-bit DAC as a reference, and n single-bit conversions are performed—in a manner similar to weighing an object on a chemist's balance with binary weights. Using a successive-approximations (shift) register (SAR), the MSB of the DAC is asserted and the input is compared with the MSB alone (one-half the DAC's span). The choice (1 or 0) is latched in and—applied to the DAC—fixes the DAC output (at 0 or 1/2).

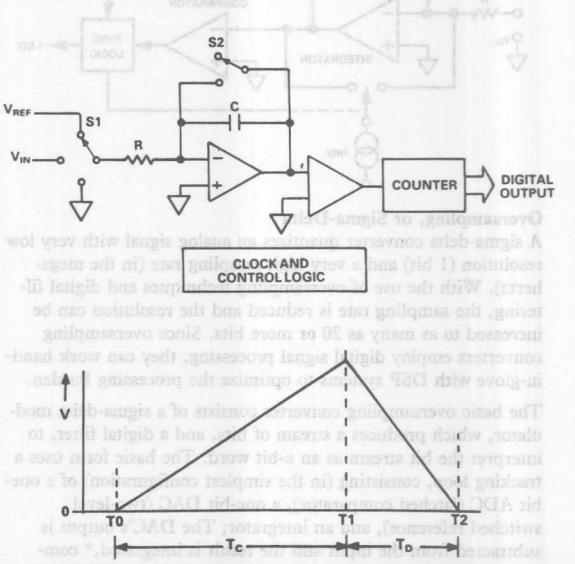


The register is clocked, the second bit is asserted, and the input is now compared with the first result plus the second bit, (0 + 1/4) or (1/2 + 1/4). The result of the second-bit test (1 or 0) is latched in; the DAC's output is either 0, 1/4, 1/2, or 3/4; the third bit is asserted; and the process continues until the LSB has been tried, the DAC output is within 1/2 LSB of the input, and all n bits have been latched into the corresponding states. Successive-approximation converters are widely used because they are capable of speeds approaching 1 MHz and resolutions up to 16 bits and more. A typical example is the industry-standard 12-bit AD574A, plus its variants and successors.

Integrating Converters

Integrating converters have two main sections, a measuring section—that converts the analog information to a time interval or a train of pulses—and a counter or filter to quantify the result as a digital number.

- *Dual-Slope*. Typically, a dual-slope converter consists of an analog integrator with switched inputs, a comparator, and a counter. Starting from an initial value and computing for a fixed interval (number of counts), $N\Delta t$, with the analog input signal applied, the output of the integrator traverses a range proportional to the average value of the analog signal, V_{IN}. At the end of the N counts, a fixed reference voltage of opposite sense to the signal is applied, and the integrator ramps linearly in the opposite direction until the comparator detects that the integrator output has reached the original starting point—after n counts. Since n is proportional to the voltage range traversed (which in turn is proportional to the average value of the input signal), $n = N\,(V_{IN}/V_{REF})$. Between conversions, a calibration cycle can be used to zero out offsets.



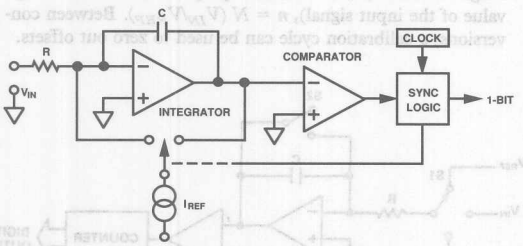
THE INTEGRATOR CHARGES FOR FIXED TIME T_C WITH V_{IN}. THE DISCHARGE TIME WITH A FIXED REFERENCE (= V_{REF}) INPUT IS THEN MEASURED (T_D).

$$\text{RATIO}\,\frac{|V_{IN}|}{|V_{REF}|} = \frac{T_D}{T_C}$$

The inherent −6-dB-per-octave low-pass characteristic of the integrator in dual-slope converters tends to reject high frequency noise; in addition, noise components having periods that are submultiples of the signal-integration interval (N) will integrate to zero. Δt may therefore be chosen to reject noise at power frequency (e.g., 50 or 60 Hz) and its harmonics. Because of the

time required for integration, these types of converters tend to be used for signals having relatively low bandwidths (compared to the types discussed above). They are especially useful where noisy signals are to be converted and relatively infrequent updating is necessary, for example in numeric display of voltage (e.g., digital panel meters).

Charge-Balance. This architecture is used by voltage-to-frequency converters and is similar to architectures used for Σ-Δ types. Employing a free-running integrator in a feedback loop, it continually seeks to null its input by subtracting precisely determined packets of charge when the accumulated charge exceeds a reference value. The number of charge packets per second (or frequency) required to balance a given input is proportional to the input. A counter may be used to convert the serial pulse train to a digital word. The figure shows a synchronous charge-balance voltage-to-frequency converter.

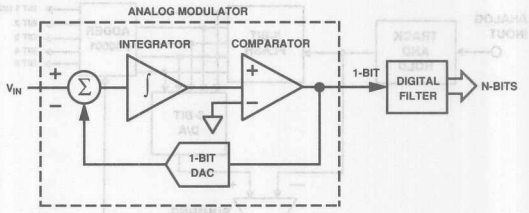


Oversampling, or Sigma-Delta

A sigma-delta converter quantizes an analog signal with very low resolution (1 bit) and a very high sampling rate (in the megahertz). With the use of oversampling techniques and digital filtering, the sampling rate is reduced and the resolution can be increased to as many as 20 or more bits. Since oversampling converters employ digital signal processing, they can work hand-in-glove with DSP systems to optimize the processing burden.

The basic oversampling converter consists of a sigma-delta modulator, which produces a stream of bits, and a digital filter, to interpret the bit stream as an *n*-bit word. The basic form uses a tracking loop, consisting (in the simplest configuration) of a one-bit ADC (latched comparator), a one-bit DAC (two-level switched reference), and an integrator; The DAC's output is subtracted from the input and the result is integrated,* compared to zero, and latched at a megahertz rate; the DAC feeds back a one-bit analog representation of the ADC's output, a serial stream of bits—1s and 0s. The bit stream is filtered digitally to trade speed for resolution.

Because sigma-delta converters latch on a high speed clock pulse, they do not require sample-holds. Since the bit stream is a train of 1s and zeros, there are no missing codes. The digital filtering is essentially another sampling operation; it produces data at a rate less than one-half the fast clock rate but substantially higher than twice the maximum signal bandwidth. The ratio of the output data rate to the input's Nyquist rate is the



oversampling ratio. The sigma-delta modulation process permits noise to be shaped so as to move most of the quantization noise energy into higher frequencies that are more easily filtered out.

Sigma-delta converters are especially useful for high resolution conversion of low-frequency signals as well as low-distortion conversion of signals containing audio frequencies. Their high proportion of digital circuitry makes them excellent candidates for high yield manufacture in IC form.

APPLICATION CONSTRAINTS

The many factors that call for large numbers of different devices are summarized briefly here. Definitions and discussions of terms used will be found in the glossary.

- **Static and Dynamic Accuracy.** Examples of static accuracy specifications, required in many precision low-frequency applications, include differential and integral nonlinearity, missing-code specs, gain error, offset error and drift, as well as conversion time (or rate). Dynamic accuracy is important in ac applications such as audio, video, and with digital signal processors; such applications call for sampling-type ADCs (or ADCs and sample-holds specified together). Important specifications include bandwidth, signal-to-noise ratio, distortion (total harmonic and 2-tone intermodulation), sampling (or throughput) rate, aperture jitter. How much error is allowed for the converter in the system error budget?
- **Digital Data Interface.** Considerations here include code (binary, offset binary, twos complement, BCD) and the format of the signal to be interfaced—*n*-bit parallel (or "broadside"), with on-chip or off-chip registers, byte-serial (e.g., to interface 12-bit data to an 8-bit bus), *n*-bit-serial, or serial bit stream. Byte-serial considerations include the choice of left or right justification. Overrange error indication may also be provided. Some processor-friendly ADCs include one or more words (FIFO) of buffer memory; less-friendly ADCs may rely on interrupts to indicate when conversions have been completed. What logic compatibility is required (TTL, low-voltage CMOS, high voltage CMOS, ECL)?
- **Control Interface and Timing.** These specify modes of chip selection and enabling, starting conversions, status indication (busy, data ready, end of conversion), data format, short cycle, conversion clocking, repetitive (continuous) conversions, sample-hold control, serial clock, synchronization, reset, and "sleep" mode (to minimize dissipation). They may also control analog functions, such as bipolar offset, gain, self-calibration modes, and selection of multiplexer channel.

*The name, sigma-delta, is a consequence of the integral, or summation over time (Σ), applied to the difference (Δ).

- **Sampling Capability**. An ADC requires a low-jitter sample/hold (or track/hold) function to maintain a constant input value during conversion, to establish precisely the instant of time associated with the converted data, and—in consequence—to obtain a train of regularly spaced conversions for digital signal-processing applications. For applications where a sample-hold function is needed, sampling ADCs (SADCs) eliminate the need for an external sample-hold function. Where all other considerations are met, this has the key advantages of compactness, combined tested specifications (usually better than for separate devices), and lower cost. Some sampling converters are ready for another sample well before a multiple-step conversion has been completed; this *pipelining* makes it possible to speed up the conversion rate for multiple conversions; but for an isolated data point one must consider *latency*, the time required for a complete single conversion.
- **The Analog Signal**. Elements of choice include range, whether unipolar or bipolar, and bandwidth. What resolution is desired? Is it single-ended or differential? Is signal conditioning needed (isolation, fixed or programmable gain or attenuation, I-to-V conversion, offsetting, noise filtering, multiplexing)? Is it already sampled? Is the output low enough in dynamic impedance to drive a proposed ADC's input? (If not, a buffer amplifier may be needed.) Is impedance matching necessary to avoid reflections? What sort of ground management will be necessary?
- **Reference Requirements**. What reference range and polarity are needed? Is an internal reference desired, or will a system reference be used? (Or will the converter's internal reference provide the system reference?) Is the converter to be used ratiometrically (because the variable actually converted is the ratio of signal to reference, accuracy can be gained by using for the converter the same reference that provides excitation for an input source, e.g., bridge excitation voltage). What current load must it supply? Is one end grounded, or must its output be differential? Are Kelvin connections necessary? desirable? available? Are the gains and/or the bipolar offset jumpered externally or switched by software.
- **Calibration Capability**. How are the offset and gain trimmed? Are zeroing and/or gain adjustment terminals available? Are trim DACs provided on chip for digital adjustment? Is calibration performed automatically on the device? Periodically or on request?
- **Number of Channels**. Does the application call for more than one input? Is multiplexing to be provided on- or off-chip? Is more than one A/D conversion at a time needed simultaneously in the same device? Is a multiple sample-hold needed for simultaneous sampling of input channels? Can conversion of a single channel be speeded up by "ping-ponging" pairs of sampling converters? Does a fast converter have a pair of alternately updated output registers so that its output can be distributed to two slow memory channels?
- **Clock**. Considerations include: speed range, drive required, edge rate, allowable overshoot, internal/external system clock, duty cycle, rising/falling-edge reference.
- **Power Supply**. What supply voltage levels are available? Is the supply a switching or a linear type? What are the power supply's regulation and noise characteristics? What sort of bypassing will be needed? Is there a limitation on available current drain or power dissipation? What are the supply's power-up characteristics? Is operation continuous or intermittent? Is a reference voltage to be derived from the power supply? Where is the supply located physically in relation to the converter and analog signals? Are electrical or magnetic fields associated with the supply likely to cause problems? Are remote devices powered centrally or locally? What is the best grounding scheme? Is isolation desirable?
- **Environmental Requirements**. What is the specified operating temperature range: 0°C to +70°C (commercial), −25°C to +85°C (industrial), −40°C to +85°C (extended industrial), or −55°C to +125°C (military)? What other environmental aspects are of importance (humidity, barometric pressure, dust, moisture, shock, vibration, ionizing radiation)? What behavior is expected in worst-case environmental conditions (survival, reliable operation, performance within specifications)? Is the environment electrically noisy? What is the character of the noise (amplitude, frequency, waveshape)?
- **Package Constraints**. What level of physical protection is required (chip, multichip reel, plastic package, hermetic package)? What kind of package and interconnections does your customer specify? What is the assembly method (automated, surface-mount, chip-and-wire, manually board-mounted)? How much space is available? Is a completely self-contained device desirable? What terminals or functions must be accessible?
- **Software- and Control-Related Issues**. Is conversion to occur at a regular rate or on the occurrence of an event? How much latency is permissible? How much time is available for conversion? For bus access? Must the conversion results be used immediately? If not, must buffer capacity be available to store more than one result? Must a new conversion start as soon as the last one ended? Is glue logic undesirable?

SPECIFICATIONS AND TERMS

Definitions of performance specifications and other frequently used terms will be found below in alphabetical order. Since they tend to be broad and generally applicable, specific data sheets and application notes should be consulted for details as they apply to specific products and applications.

Accuracy, Absolute

The error of an A/D converter at a given output code is the difference between the theoretical and the actual analog input voltages required to produce that code. Since the code can be produced by any analog voltage in a finite band (*see* Quantizing uncertainty), the "input required to produce that code" is defined as the midpoint of the band of inputs that will produce the code. For example, if 5 volts (±1.2 mV) will theoretically produce a 12-bit half-scale code of 100000000000, then a converter for which any voltage from 4.997 V to 4.999 V will produce that code will have an absolute error of (4.997 + 4.999)/2 − 5 volts = −2 mV.

Absolute error comprises gain error, zero error and nonlinearity, together with noise. Absolute-accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.

Accuracy, Relative
Relative accuracy error, expressed in percent, parts per million, or fractions of an LSB (full-scale range/2^n), is the deviation of the analog value at any code, (relative to the full analog range of the device transfer characteristic) from its theoretical value (relative to the same range) after the full-scale range (FSR) has been calibrated.

Since the discrete points on the theoretical transfer characteristic lie on a straight line, this deviation can also be interpreted as a measure of *nonlinearity*.

The "discrete points" of an A/D transfer characteristic are the midpoints of the quantization bands at each code (*see* Accuracy, absolute). However, since transitions between codes are easier to find than the midpoints, this characteristic is often defined in terms of an adjacent transition, usually the low-side transition.

Aliasing
A signal within a bandwidth, f_A, must be sampled at a rate, $f_S > 2\,f_A$ in order to avoid loss of information. If the number of samples of a signal, f, is inadequate, i.e., $f_S < 2\,f$, a phenomenon called aliasing, inherent in the spectrum of the sampled signal, will cause a frequency equal to $f_S - f$, called an "alias" to appear in the signal band (of frequencies below $f_S/2$). For example, if f_S = 4 kHz and f = 3 kHz, a 1 kHz alias will appear. Note also that, for a 1 kHz signal (which is *within* the band, $f_S/2$), the alias will be at 3 kHz, *outside* the band. Since noise is also aliased, it is essential to provide low-pass filtering prior to the sampling stage to prevent high frequency noise on the signal line from being aliased into the signal range.

Analog-to-Digital Converter (ADC)
An analog-to-digital converter quantizes an analog input voltage (i.e., measures and assigns it to one of 2^n equal ranges, or *quanta*, within the expected span) and interprets the quantum as a digital number.

Aperture Jitter
Aperture jitter is the sample-to-sample variation in the space in time between the effective points at which the samples are actually taken. It is often due to phase jitter on the input sine wave or unwanted phase-modulation of the sampling clock by sources such as random noise, power line noise, or digital noise stemming from poor layout, bypassing, or grounding. The resulting error can be expressed in terms of an rms time jitter, which produces a corresponding rms voltage error, decreasing the overall ADC signal-to-noise ratio.

When a sample-hold is used ahead of a nonsampling A/D converter (typically successive-approximation and flash), the timing uncertainty of the conversion process is reduced by the ratio of aperture jitter to the conversion time. Expressed another way, the maximum frequency that can be handled with less than 1 LSB error due to timing is $2^{-n}/(\pi\tau_a)$, instead of $2^{-n}/(\pi\tau_c)$, where τ_a is the aperture uncertainty and τ_c is the conversion time.

Aperture Time (Delay)
Aperture time (sometimes called aperture *delay* time—although it may be either a delay or an advance) is a measure of the interval between the leading edge of the sampling clock and the instant at which the sample-hold or sampling ADC actually takes the sample. The variation or tolerance placed on this parameter from part to part is important in simultaneous sampling applications or other applications where ADCs are required to track each other when processing dynamic signals. Timing can be advanced or delayed to improve accuracy, but precision is ultimately limited by *aperture jitter*.

Bandwidth, Full-Linear
The full-linear bandwidth is the input frequency at which the slew-rate limit of the sample-hold amplifier (SHA) is reached. Up to this point, the amplitude of the reconstructed fundamental will have been attenuated by less than 0.1 dB. Beyond this frequency, distortion of the sampled input signal increases significantly.

Bandwidth, Full-Power (FPBW)
The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental (using FFTs) is reduced by 3 dB for a full-scale input. In order to be meaningful, the FPBW must be examined in conjunction with the signal-to-noise ratio (SNR), effective number of bits (ENOB), and harmonic distortion in order to ascertain the true dynamic performance of the ADC at the FPBW frequency.

Binary Coding
The digital output of an ADC is considered binary-coded when outputs start at all-zeros for a zero-scale (unipolar) analog input, increasing to all-ones for FSR ($1 - 2^{-n}$), in binary sequence. For a bipolar analog range, all-zeros starts at negative full-scale, increasing in binary sequence to FSR ($1 - 2^{-n+1}$) for all ones; this coding is called *offset binary*, which is easy for converters but not useful for computers; however, it is easily converted to *twos complement* by complementing the MSB.

Bipolar Mode
A configuration that an A/D converter uses to handle signal spans containing both positive and negative signals. Usually it means offsetting half-scale to become analog zero, and either accepting the resulting offset binary code or changing it to twos complement by complementing the most-significant bit (*see* Binary Coding).

Bipolar Negative Full-Scale Error
In bipolar converters, for the first step of code (from 0000 . . . 00 to 0000 . . . 01 in offset binary, or 1000 . . . 00 to 1000 . . . 01 in twos complement), the ideal transition occurs at 1/2 LSB above $-V_{REF}$. Bipolar negative-full-scale error is the deviation of the first code transition from the ideal when operating in the bipolar mode.

Bipolar Zero Error (Offset) and Drift
In the bipolar mode, this is the deviation of the midscale transition (011 . . . 111 to 100 . . . 000 in offset binary, 111 . . . 111 to 000 . . . 000 in twos complement) from the ideal (A_{GND} – 0.5 LSB).

Bus
A parallel path of binary information signals—usually 8, 16, or 32 bits wide. Three common types of information usually found on buses are data, addresses, and control signals. 3-state output switches (inactive, high, and low) permit many sources—such as ADCs—to be connected to a bus, while only one is active at any time.

Byte
A byte is a binary digital word, usually 8 bits wide. A byte is often part of a longer word that must be placed on an 8-bit bus in two stages. The byte containing the MSB is called the *high byte*; that containing the LSB is called the *low byte*. A four-bit byte is called a *nybble*.

Byte, High
When a 12- or 16-bit word is placed on an 8-bit bus in two stages, the high byte contains the 4- or 8 most-significant bits. If 8, a 12-bit word is said to be left-justified; if 4 (plus filled-in leading sign bits), the word is said to be right justified.

Byte, Low
When a 12- or 16-bit word is placed on an 8-bit bus in two stages, the low byte contains the 4- or 8 least-significant bits. If 8, a 12-bit word is said to be right justified; if 4 (plus trailing zeros), the word is said to be left-justified.

Capacitance, Input (C_{IN})
The capacitance measured between the analog input and all supply pins (including grounds) of an A/D converter. Input capacitance often varies with input voltage, so it should be measured at worst-case input voltage. This parameter is important at high input frequencies because an amplifier or track-and-hold must drive it without introducing unacceptable levels of distortion.

Chip Select ($\overline{CS}$)
A logic input signal activating data or control information transfer between the ADC and the digital circuitry. This signal is usually active-low, as designated by the overbar. $\overline{CS}$ is used in conjunction with additional qualifying logic signals to determine the exact activities to take place.

Clock (CLK)
The operation of many common A/D conversion processes requires a clock to order events in the process. A system clock is also present to time the interfacing between the converter and the system. Operations may depend on clock levels or clock edges, either ascending or descending.

Code, Missing
In practice, the 2^n–2 inner codes (excluding zero and full scale) are always wider or narrower than the ideal 1 LSB, especially in flash, subranging, and successive-approximation converters. If code-width errors (*see* Nonlinearity, Differential) exceed 1 LSB, one or more codes may have zero width; as the input increases, the output will jump between the adjacent codes, e.g., from 11 . . . 011 to 11 . . . 101, skipping 11 . . . 010. A specification that guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input level is increased.

Code Repetition
The ability of the ADC to continuously provide the same digital output for a stable analog input voltage in the middle of a code.

Code Width and Uncertainty
Code width is the amount of input voltage change between output code transitions, expressed in LSBs of full scale ($FSR/2^n$). The ideal code width is 1 LSB. Since transition voltage is sensitive to noise and jitter, there is always a degree of uncertainty associated with code-width measurements.

Coding
This term refers to the code and format employed to express an ADC's digital output data. Codes include binary, binary-coded decimal (BCD), offset binary, twos complement, and complementary (*negative-true*) versions of these codes. The codes may be expressed in parallel, byte-serial, and bit-serial formats. Some converters, (e.g., V/Fs) have *uncoded* (i.e., bit-stream) outputs.

Command Register
An internal register of the ADC that can be programmed by the user to select various modes of operation; examples of selection choices include unipolar or bipolar conversion, range, data output format.

Common-Mode Rejection
The ability of a device to reject the effect of voltage applied to both input terminals simultaneously—often through variation of a ground level—is specified as a *common-mode rejection ratio* (CMRR, or in logarithmic form, CMR = 20 log CMRR). CMRR is the ratio of gain for the differential, or *normal-mode*, signal to the gain for the common-mode signal.

Conformance, Straight Line
This term describes how closely the ADC transfer characteristic conforms to a reference straight line. Nonconformance can be described in terms of integral nonlinearity (the difference between the actual code centers and a straight line), or dynamically in terms of waveform distortion. For many applications, this property is far more important than calibration errors and drifts.

Control Lines
Digital input/output pins that activate or monitor and control ADC operation. Examples include chip select, low byte, high byte, start convert, end of conversion, conversion complete, busy, read, etc.

Conversion Complete (CC)
This digital output signal indicates the end of conversions. When this signal is in the opposite state, the ADC is considered to be "busy." Also called end of conversion, or EOC.

Conversion Time (t_C) and Conversion Rate
The time required for a complete measurement by an ADC is called *conversion time*. For most converters (assuming no significant additional delays), this is the same as the inverse of *conversion rate*. For simple sampling ADCs, however, the conversion rate is the inverse of the conversion-time-plus-the-sample-hold's acquisition-time. However, in some high speed sampling converters, because of pipelining, new conversions are initiated before a prior conversion has been completed. Once a train of conversions has been initiated, as in signal-processing applications, the conversion rate can be much faster than the conversion time would imply.

Cycle Time
The time required for the converter clock to finish a complete conversion cycle and be ready to start the next cycle. This can be longer than the conversion time because of a cycle required to reset the successive-approximation register or several cycles longer to perform a calibration. Sometimes known as *latency*.

Delta-Sigma, *see* Sigma-Delta

Differential Nonlinearity (DNL), *see* Nonlinearity

Distortion, (Total) Harmonic
THD is usually measured as the ratio of the rms sum of the next five harmonic components to the rms value of a full-scale fundamental input signal and is expressed as a percentage or in decibels:

$$THD = 10 \log [(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)/V_1^2].$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonic. The THD can be derived from the measured FFT plot of the device's output spectrum. For input signals or harmonics that are above the Nyquist frequency, the aliased component is used.

Distortion, Intermodulation (IMD)
With inputs consisting of sine waves at two frequencies, f_A and f_B, any device with nonlinearities will create distortion products, of order $(m+n)$, at sum and difference frequencies of $mf_A \pm nf_B$, where $m,n = 0, 1, 2, 3 \ldots$. Intermodulation terms are those for which m or n is not equal to zero. For example, the second-order terms are $(f_A + f_B)$ and $(f_A - f_B)$, and the third-order terms are $(2f_A + f_B)$, $(2f_A - f_B)$, $(f_A + 2f_B)$, and $(f_A - 2f_B)$.

The IMD products are expressed as the decibel ratio of the rms sum of the distortion terms to the rms sum of the measured input signals.

Drift, Temperature
The temperature drifts for full-scale (or *gain*) error, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

Dual-Slope Conversion
A form of integrating conversion. See the FUNCTIONAL CHARACTERISTICS section.

Effective Number of Bits
For a sine wave, *signal-to-noise ratio* (SNR) can be expressed in terms of the number of bits. Rewriting the SNR formula, it is possible to get a measure of performance expressed as N, the *effective number of bits* (ENOB).

$$N = (\text{SNR} - 1.76)/6.02$$

Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SNR.

End of Conversion (EOC)
This digital output signal flags the conversion complete and data-ready condition of an A/D converter.

Feedthrough
Undesirable signal coupling around switches of other devices that are supposed to be turned off or provide isolation, e.g., *feedthrough error* in a multiplexer. It is variously specified in percent, ppm, fractions of 1 LSB, or fractions of 1 volt, with a given set of inputs at a specified frequency.

FIFO (First-In, First-Out Memory)
This is best defined by an example. The AD7878 12-bit sampling ADC, designed to interface with signal processors, has eight words of first-in, first-out (FIFO) memory on-chip. This permits up to 8 data samples to be acquired and stored before the processor is required to read; the benefit is that the software overhead associated with servicing processor interrupts is greatly reduced. The 8 words that were stored can then be read out of the FIFO at maximum processor speed.

"Flash" Converter
A converter providing direct (hence the most rapid) conversion. See the FUNCTIONAL CHARACTERISTICS section.

Frequency-Domain Testing
In one approach, a device is tested dynamically using a sine-wave input and a 2,048-point fast Fourier transform (FFT) to analyze the resulting output. Coherent sampling is used, wherein the ADC sampling frequency and the analog input frequency are related to each other by a ratio of integers. This ensures that an integral multiple of input cycles is captured, allowing direct FFT processing without windowing or digital filtering, which could mask some of the dynamic characteristics of the device. In addition, the frequencies are chosen to be "relatively prime" (no common factors) to maximize the number of different ADC codes that are present in a sample sequence. The result, called prime coherent sampling, is a highly accurate and repeatable measure of the actual frequency-domain response of the converter.

Full-Scale Calibration Range
For self-calibrating Σ-Δ converters in the system calibration mode, the range of voltages the device can accept and still calibrate full-scale accurately.

Full-Scale Error, *see also* Gain Error
The last transition (from 111 . . . 10 to 111 . . . 11) should occur for an analog magnitude 1 1/2 LSB (i.e., 1.5 FSR/2^n) below the nominal full scale. The full-scale error is the deviation of the actual level of the last transition from the ideal level at 25°C without adjusting the offset. The full-scale error can be adjusted to zero.

Full-Scale Range (Span)
The difference between the maximum and minimum analog values for input to an A/D converter.

Gain Drift, *see* Drift

Gain Error
The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. The first transition is 1/2 LSB above the low end of the scale (zero in unipolar converters, −FS in bipolar converters). The gain error is the deviation of the actual difference between the first and last code transitions from the ideal difference between the first and last code transitions. This error can be adjusted.

Half-Step Offset (Low-Side Transition)
In designing an ADC, since comparisons establish transition points, a half-step offset is necessary to center the analog input voltages halfway between the output code transition points. For example, the successive-approximation converter architecture inherently has a 1 LSB transition voltage (instead of 1/2 LSB) for the first code change if a half-step offset is not inserted.

Impedance, Input
The dynamic load presented by a converter to its input source. In unbuffered successive-approximation converters employing current-summing at the comparator input, the presence of current pulses at the converter's clock frequency mandates that the converter be driven from a low impedance (at the clock frequency) in order to maintain an accurate voltage input.

Input Range (Span)
See Full-Scale Range. See also individual data sheets, especially for devices that provide self-calibration.

Integral Nonlinearity, *see* Nonlinearity

Least-Significant Bit (LSB)
In a digital word, the binary digit with the smallest numerical weighting—or its voltage equivalent. Normally, one LSB is equal to the full-scale range divided by 2^n, where n is the number of bits provided by the converter.

Left-Justified Data
When a 12-bit word is placed on an 8-bit bus in two stages, the high byte contains the 4- or 8 most-significant bits. If 8, the word is said to be left justified; if 4 (plus filled-in leading sign bits), the word is said to be right justified.

Linearity Error, *see* Nonlinearity

Major Transition
The digital output code change at one-half the full span, from 011 . . . 111 to 100 . . . 000.

Missing Codes, *see* Code

Most-Significant Bit
The binary digit with the largest numerical weighting. Normally, the MSB of a digital word has a weighting of 1/2 the full-scale range. In bipolar-input converters, the MSB is also used as a sign bit (representing the upper or lower half of the full-scale range). If placed on a right justified bus wider than the data word, all bits to the left of the MSB should be filled with the same bit.

Noise, Quantization
As the input to an A/D converter increases smoothly, the output moves up in a series of steps. When the analog input is summed with an ideal DAC reconstruction, these steps produce an error waveform shaped like an irregular sawtooth as each bit transition is crossed. This waveform can be considered as a type of white noise. In sigma-delta converter design, the quantization-noise spectrum is shaped so as to move most of its energy out of the baseband, a key to the low noise and high resolution available in these converters.

Noise, Transition
As repeated conversions are made in the vicinity of a transition, the transition will be found to occur at somewhat differing values of input. Transition noise is the rms value of the variation in the transition region.

Nonlinearity, AC (Histogram Method)
A full-scale sine wave is applied to the ADC and a large number of samples are taken (several million for a 12-bit converter, to achieve statistically satisfactory results). The number of occurrences of each code is recorded on a histogram plot. The data is normalized by comparison with the U-shaped ideal probability density distribution of a sine wave. From it, DNL can be plotted, and integral nonlinearity can be determined by compiling a cumulative histogram, in which the bin widths are the transition levels. (An example of the results can be found in the AD7870 technical data.)

Nonlinearity, Differential (DNL)
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation, expressed in LSBs, from this ideal value. It is often specified in terms of the maximum number of bits for which no missing codes (NMC) are guaranteed.

Nonlinearity, Integral (INL)
The ideal transfer function for an ADC is a straight line drawn between "zero" and "full scale." The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition. Integral nonlinearity is the worst-case deviation of a code from the straight line. The deviation of each code is measured from the middle of that code. In some cases, integral nonlinearity is defined with respect to a best-fit straight line, which is typically calculated using the least-squares method.

Nyquist Frequency, Sampling Rate
According to the sampling theorem, a signal within a bandwidth, f_A, must be sampled at a rate, $f_S > 2\,f_A$ in order to avoid loss of information (*see* Aliasing). The "Nyquist (input) frequency" of a converter sampling at f_S is $f_S/2$; alternatively, the "Nyquist (sampling) rate" is $2\,f_A$.

Offset Binary Code
A digital binary code used to represent bipolar analog voltages. Negative full-scale voltage is assigned all-zeros (000 . . . 00), zero voltage is at MSB high—all other bits zero (100 . . . 00), and positive "full-scale" (from a transition 1 1/2 LSB below full-scale) is assigned all-ones (111 . . . 11). The more useful twos-complement code is similar to offset binary, except that the MSB is complemented.

Offset, Bipolar (also Bipolar Zero Error)
In the bipolar mode the major carry transition (011111111111 to 100000000000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error specifies the maximum deviation of the actual transition point at 25°C. This offset is usually adjustable. The bipolar offset error and temperature coefficient respectively specify the initial deviation and maximum change in the error over temperature.

Offset Calibration Range
For self-calibrating Σ-Δ converters in the system calibration mode, this is the range of voltages the device can accept and still calibrate offset accurately.

Offset, Unipolar
The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point at 25°C. This offset can be adjusted.

The *unipolar offset temperature coefficient* specifies the maximum change of the transition point over temperature, with or without external adjustments.

Overrange
When analog input voltages exceed the input range, an overrange condition is in effect. Normally, the digital output code stays at all-ones for positive overrange and all-zeros for negative overrange, with binary coding. Some converters have a digital output flag to signal overrange.

Overrange, Negative Full-Scale
In Σ-Δ converters, negative full-scale overrange is the amount of overhead available to handle input voltages below $-V_{REF}$ (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator of Σ-Δ converters or overflowing the digital filter. Note that the analog input will accept negative voltage peaks, even in the unipolar mode.

Overrange, Positive Full-Scale
In Σ-Δ converters, positive full-scale overrange is the amount of overhead available to handle input voltages greater than $+V_{REF}$ (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or overflowing the digital filter of Σ-Δ converters.

Oversampling
Sampling at a rate greater than Nyquist is *oversampling*. If the degree of oversampling is substantial, the noise-filtering problem is ameliorated. Oversampling is the key to the advantages of sigma-delta conversion.

Overvoltage Recovery
Overvoltage recovery time is defined as that amount of time required for the ADC to achieve a specified accuracy after an overvoltage (usually 50% greater than full-scale range), measured from the time the overvoltage signal reenters the converter's range. The ADC should act as an ideal limiter for out-of-range signals, producing a positive or negative full-scale code during the overvoltage condition. Some converters provide over- and underrange flags to allow gain-adjustment circuits to be activated.

Peak Spurious (Peak Harmonic Component)
In the FFT spectrum of a converter output for a given sinusoidal input signal, the peak "spur" is the largest individual spectral component, excluding the input signal and dc. Its magnitude is expressed in dB relative to the rms value of a full-scale input signal. The dB difference in amplitude between it and the signal is the *spurious-free dynamic range* (SFDR).

Pipelining
A pipelined converter is a multistage converter which is capable of accepting a new signal before it has completed the conversion of one or more previous ones. A new signal arrives while others are still "in the pipeline." This is a technique used where a fast conversion rate is highly desirable and the latency of individual conversions is relatively unimportant.

Power Supply Rejection, Sensitivity
For many converters, variations in power supply will affect the scale factor, but not the converter's linearity. Power supply rejection is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

Quantizing Uncertainty (Error)
The analog continuum is partitioned into 2^n discrete ranges for n-bit conversion. All analog values within a given range are represented by the same digital code, which is assigned to the nominal midrange value. There is, therefore, an inherent quantization uncertainty of ±1/2 LSB, in addition to the actual conversion errors. In integrating converters, this "error" is often expressed as "±1 count."

R-2R Ladder
A resistor network providing the basic binary-current division used in many successive-approximation A/D converters.

Ratiometric Converter
The output of an A/D converter is a digital number proportional to the ratio of (some measure of) the input to a reference. Many requirements for conversions call for an absolute measurement, i.e., against a fixed reference. In some cases, where the measurement is affected by a changing reference voltage (e.g., the voltage applied to a bridge), it is advantageous to use that same reference as the reference for the conversion, to eliminate the effect of variation.

Reference
The reference voltage establishes an A/D conversion system's accuracy at full scale. At other voltages, the integral nonlinearity and reference determine absolute accuracy. References may be furnished either externally or internally.

Resolution
Resolution of an ADC is the number of states (2^n) that the analog input voltage is resolved—or divided—into, where n is equal to the number of bits.

Right Justified Data
When a 12-bit word is placed on an 8-bit bus in two stages, the high byte contains the 4- or 8 most-significant bits. If 8, the word is said to be left-justified; if 4 (plus filled-in leading sign bits), the word is said to be right justified.

Sampling A/D Converter
A sampling A/D converter includes a sample-hold which acquires the input value at a given instant and holds it throughout the conversion (or until the converter is ready for the next data point). (*See* Aperture Time.)

Sampling Frequency
The rate at which an ADC can continuously convert analog inputs into digital outputs. In successive-approximation converters, clock frequency and data-transfer overhead determine the sampling frequency.

Serial Output
A bit-serial output consists of a series of bits clocked out on a single line. There must be a means of identifying the beginning and end of words; this can be furnished via an additional clock line, by using synchronized clocks, and/or by providing a consistent identifying signature for the beginning of a word. *Byte serial* consists of a series of bytes transmitted in sequence on a bus (*see* Byte).

Settling Time, *see also* Transient Response
Settling time is a function of the sample-hold's (SHA) ability to track fast-slewing signals. This is specified as the maximum time required in track mode after a full-scale step input to guarantee rated conversion accuracy.

Short Cycling
An n-bit successive-approximation converter takes at least n clock cycles to complete a conversion. Some converters have the capability of stopping the conversion at an arbitrary point, thus shortening the cycle. Speeding up the conversion by such an approach is useful for maximizing information transfer when the full n bit accuracy or resolution is not needed for a given conversion.

Sigma-Delta Converter
An A/D converter that uses a one-bit or other low-resolution quantizer and very high oversampling rate, combined with a one-bit or low-resolution DAC in a feedback loop. The digital quantizer output is then followed by a low-pass digital filter to remove the noise and output an n-bit digital representation of the input signal.

Signal-to-Noise and Distortion (S/N+D) Ratio
S/(N+D) is the logarithmic expression (decibels) of the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. This is actually the generally accepted definition for signal-to-noise ratio (SNR); in this case, the "+D" is intended to emphasize the inclusion of harmonic distortion for audio applications.

Signal-to-Noise Ratio (SNR)
SNR is the measured signal-to-noise ratio at the output of an ADC. The signal is the rms magnitude of the fundamental. Noise is the RMS sum of all the nonfundamental signals up to half the sampling frequency ($f_{SAMPLE}/2$) excluding DC. SNR is dependent on the number of levels used in the quantization process; the more levels, the smaller the quantization noise. The theoretical signal-to-noise ratio for a sine wave input is given by:

$$\text{SNR} = (6.02\ N + 1.76)\ \text{dB}$$

where N is the number of bits. Thus, for an ideal 14-bit converter, SNR $\approx$ 86 dB.

Slew Rate
Slew rate is the maximum rate of change allowed at the input such that the a digitized recreation of the output will track the input without increased error.

Span
The full-scale analog input range. Some ADCs have resistor- or software-selectable analog input ranges.

Spurious-Free Dynamic Range (SFDR)
The difference, in dB (log scale) between the rms amplitude of the input signal and the peak spurious signal (*see* Peak Spurious).

Status Register
A register indicating current status of the analog-to-digital conversion by means of a Busy or Conversion Complete signal.

Subranging
High-resolution fast conversion using flash converters to perform partial conversions. See the FUNCTIONAL CHARACTERISTICS section.

Successive Approximation Conversion
A popular conversion method in which an n-bit conversion is performed by n successively finer approximations. See the FUNCTIONAL CHARACTERISTICS section.

Successive Approximation Register (SAR)
A digital circuit that controls the operation of a successive-approximation ADC and accumulates the digital output word in its register.

Temperature Coefficients
The temperature coefficients for unipolar offset, bipolar zero, and gain error specify the maximum change from the initial (+25°C) value to the value at T_{MIN} or T_{MAX}.

Three-State (Output Buffer), *see* Bus

Transient Response
The transient response (or settling time) of an ADC is the time required for the ADC to settle to rated accuracy after the application of a full-scale step input.

Transition, *see* Accuracy, Relative

Transition, Major; *see* Major Transition

Undersampling
Sampling at a rate below Nyquist. Ordinarily this results in loss of information. However, the aliasing it produces can be used to translate the sidebands of a high frequency carrier down to a lower frequency for detection and demodulation, provided that the ADC has sufficient analog bandwidth.

Unipolar Mode
Operation of an ADC with zero-to-full-scale voltage inputs of one polarity only.

Zero- and Gain Adjustment Principles
The zero adjustment of a unipolar ADC is set so that the transition from all-bits-off to LSB-on occurs at $1/2 \times 2^{-n}$ of nominal full scale. The gain is set for the final transition to all-bits-on to occur at FS $(1 - [3/2 \times 2^{-n}])$.

The "zero" of an offset-binary bipolar ADC is set so that the first transition occurs at $-\text{FS}\ (1 - 2^{-n})$ and the last transition at FS $(1 - [3 \times 2^{-n}])$. The data sheet instructions should be followed.

Zero-Code Error
The difference between the ideal 1/2-LSB offset at zero of an ADC and the actual value of input required to produce the first transition.

Zero Drift
The change with temperature of analog zero for an ADC operating in the unipolar mode. It is generally expressed in ppm of FS/°C, or LSBs.

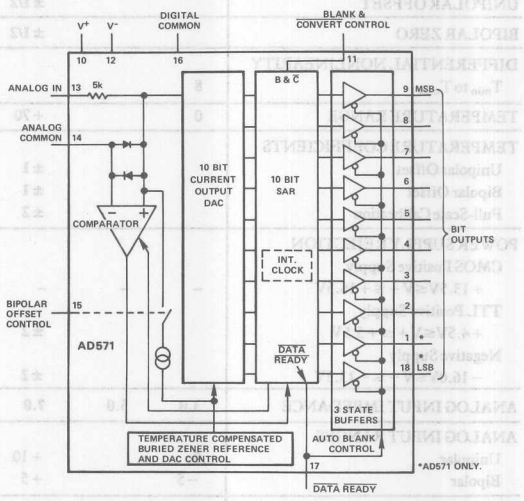
8- and 10-Bit Analog-to-Digital Converters

AD570/AD571*

FEATURES

Complete A/D Converters with Reference and Clock
AD570: 8 Bit
AD571: 10 Bit
Fast Successive Approximation Conversion – 25μs
No Missing Codes Over Temperature
Digital Multiplexing – 3 State Outputs
18-Pin Ceramic DIP
Low Cost Monolithic Construction
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTIONS

The AD570/AD571 are successive approximation A/D converters consisting of a DAC, voltage reference, clock, comparator, successive approximation register and output buffers – all fabricated on a single chip. No external components are required to perform full accuracy conversions in 25μs.

The AD570/AD571 incorporate advanced integrated circuit design and processing technologies. They employ I^2L (integrated logic) processing in the fabrication of the SAR function. Laser trimming of the high stability SiCr thin-film resistor ladder network insures high accuracy, which is maintained with a temperature compensated, subsurface Zener reference.

Operating on supplies of +5V to +15V and −15V, the AD570/AD571 will accept analog inputs of 0 to +10V, unipolar or ±5V bipolar, externally selectable. As the BLANK and $\overline{\text{CONVERT}}$ input is driven low, the three-state outputs will be open and a conversion will commence. Upon completion of the conversion, the $\overline{\text{DATA READY}}$ line will go low and the data will appear at the output. Pulling the BLANK and $\overline{\text{CONVERT}}$ high blanks the outputs and readies the device for the next conversion.

The devices are available in two versions: the "J" and "K" specified for the 0 to +70°C temperature range. The "S" guarantees the specified accuracy and no missing codes from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD571 is a complete 10-bit A/D converter. The AD570 is an 8-bit version which employs the same architecture. No external components are required to perform a conversion.
2. The AD570/AD571 are single chip devices employing advanced IC processing techniques. Thus, the user has at his disposal a truly precision component with the reliability and low cost inherent in monolithic construction.
3. The converters accept either unipolar (0 to +10V) or bipolar (−5V to +5V) analog inputs by simply grounding or opening a single pin.
4. Each device offers the specified accuracy with no missing codes over its entire operating temperature range.
5. Operation is guaranteed with −15V and +5V to +15V supplies. The devices will also operate with a −12V supply.
6. The AD570 and AD571 are available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current /883B data sheet for detailed specifications.

*Covered by Patent Nos. 3,940,760; 4,213,806; 4,136,349.

AD570/AD571—SPECIFICATIONS

(T_A = +25°C, V+ = +5V, V− = −12V or −15V, all voltages measured with respect to digital common, unless otherwise indicated)

Model	AD570J Min	AD570J Typ	AD570J Max	AD570S Min	AD570S Typ	AD570S Max	Units
RESOLUTION[1]			8			8	Bits
RELATIVE ACCURACY							
T_{min} to T_{max}			±1/2			±1/2	LSB
FULL-SCALE CALIBRATION		±2			±2		LSB
UNIPOLAR OFFSET			±1/2			±1/2	LSB
BIPOLAR ZERO			±1/2			±1/2	LSB
DIFFERENTIAL NONLINEARITY							
T_{min} to T_{max}	8			8			Bits
TEMPERATURE RANGE	0		+70	−55		+125	°C
TEMPERATURE COEFFICIENTS							
Unipolar Offset			±1			±1	LSB
Bipolar Offset			±1			±1	LSB
Full-Scale Calibration			±2			±2	LSB
POWER SUPPLY REJECTION							
CMOS Positive Supply							
+13.5V≤V+≤+16.5V	–	–	–	–	–	–	LSB
TTL Positive Supply							
+4.5V≤V+≤+5.5V			±2			±2	LSB
Negative Supply							
−16.0V≤V−≤−13.5V			±2			±2	LSB
ANALOG INPUT IMPEDANCE	3.0	5.0	7.0	3.0	5.0	7.0	kΩ
ANALOG INPUT RANGES							
Unipolar	0		+10	0		+10	V
Bipolar	−5		+5	−5		+5	V
OUTPUT CODING							
Unipolar	Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT							
Output Sink Current							
(V_{OUT} = 0.4V max, T_{min} to T_{max})	3.2			3.2			mA
Output Source Current							
(V_{OUT} = 2.4V max, T_{min} to T_{max})	0.5			0.5			mA
Output Leakage			±40			±40	µA
LOGIC INPUTS							
Input Current			±100			±100	µA
Logic "1"	2.0			2.0			V
Logic "0"			0.8			0.8	V
CONVERSION TIME							
T_{min} to T_{max}	15	25	40	15	25	40	µs
POWER SUPPLY							
V+	+4.5	+5.0	+7.0	+4.5	+5.0	+7.0	V
V−	−12.0	−15	−16.5	−12.0	−15	−16.5	V
OPERATING CURRENT							
V+		7	10		7	10	mA
V−		9	15		9	15	mA
PACKAGE OPTION[2,3]							
Ceramic (D-18)	AD570JD			AD570SD			

NOTES

[1]The AD570 is a selected version of the AD571 10-bit A-to-D converter. Only TTL logic inputs should be connected to Pins 1 and 18 (or no connection made) or damage may result.

[2]D = Ceramic DIP. For outline information see Package Information section.

[3]For details on grade and package offerings for SD-grade in accordance with MIL-STD-883, refer to Analog Devices Military Products databook or current /883B data sheet.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD571J Min	AD571J Typ	AD571J Max	AD571K Min	AD571K Typ	AD571K Max	AD571S Min	AD571S Typ	AD571S Max	Units
RESOLUTION			10			10			10	Bits
RELATIVE ACCURACY, T_A			±1			±1/2			±1	LSB
T_{min} to T_{max}			±1			±1/2			±1	LSB
FULL-SCALE CALIBRATION		±2			±2			±2		LSB
UNIPOLAR OFFSET			±1			±1/2			±1	LSB
BIPOLAR ZERO			±1			±1/2			±1	LSB
DIFFERENTIAL NONLINEARITY, T_A	10			10			10			Bits
T_{min} to T_{max}	9			10			10			Bits
TEMPERATURE RANGE	0		+70	0		+70	−55		+125	°C
TEMPERATURE COEFFICIENTS										
Unipolar Offset			±2			±1			±2	LSB
Bipolar Offset			±2			±1			±2	LSB
Full-Scale Calibration			±4			±2			±5	LSB
POWER SUPPLY REJECTION										
CMOS Positive Supply										
+13.5V≤V+≤+16.5V	–	–	–			±1	–	–	–	LSB
TTL Positive Supply										
+4.5V≤V+≤+5.5V			±2			±1			±2	LSB
Negative Supply										
−16.0V≤V−≤−13.5V			±2			±1			±2	LSB
ANALOG INPUT IMPEDANCE	3.0	5.0	7.0	3.0	5.0	7.0	3.0	5.0	7.0	kΩ
ANALOG INPUT RANGES										
Unipolar	0		+10	0		+10	0		+10	V
Bipolar	−5		+5	−5		+5	−5		+5	V
OUTPUT CODING										
Unipolar	Positive True Binary			Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT										
Output Sink Current										
(V_{OUT} = 0.4V max, T_{min} to T_{max})	3.2			3.2			3.2			mA
Output Source Current[1]										
(V_{OUT} = 2.4V max, T_{min} to T_{max})	0.5			0.5			0.5			mA
Output Leakage			±40			±40			±40	μA
LOGIC INPUTS										
Input Current			±100			±100			±100	μA
Logic "1"	2.0			2.0			2.0			V
Logic "0"			0.8			0.8			0.8	V
CONVERSION TIME										
T_{min} to T_{max}	15	25	40	15	25	40	15	25	40	μs
POWER SUPPLY										
V+	+4.5	+5.0	+7.0	+4.5	+5.0	+16.5	+4.5	+5.0	+7.0	V
V−	−12.0	−15	−16.5	−12.0	−15	−16.5	−12.0	−15	−16.5	V
OPERATING CURRENT										
V+		7	10		7	10		7	10	mA
V−		9	15		9	15		9	15	mA
PACKAGE OPTION[2,3]										
Ceramic (D-18)		AD571JD			AD571KD			AD571SD		

NOTES

[1]The data output lines have active pull-ups to source 0.5mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6kΩ internal pull-up resistor.

[2]D = Ceramic DIP. For outline information see Package Information section.

[3]For details on grade and package offerings for SD-grade in accordance with MIL-STD-883, refer to Analog Devices Military Products databook or current /883B data sheet.

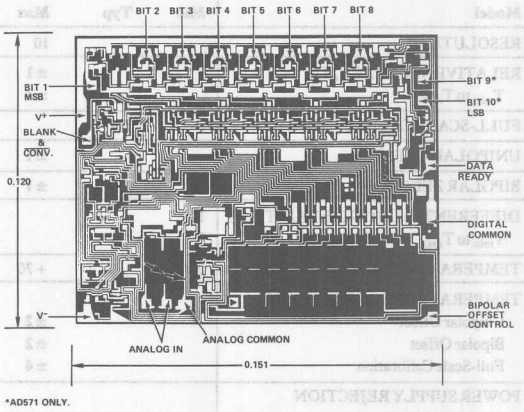
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common AD570J, S/AD571J, S	0 to +7V
AD571K	0 to +16.5V
V− to Digital Common	0 to −16.0V
Analog Common to Digital Common	±1V
Analog Input to Analog Common	±15V
Control Inputs	0 to V+
Digital Outputs (Blank Mode)	0 to V+
Power Dissipation	800mW

CHIP BONDING DIAGRAM



CIRCUIT DESCRIPTION

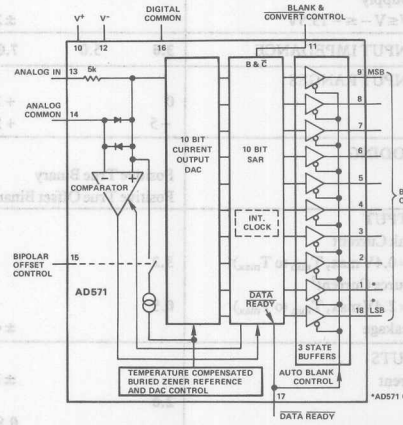
The AD571 is a complete 10-bit A/D converter which requires no external components to provide the complete successive approximation analog-to-digital conversion function. The AD570 is an 8-bit version. A functional block diagram of the AD570/AD571 is shown below. Upon receipt of the CONVERT command, the internal 10-bit (AD571) current output DAC is sequenced by the I^2L successive approximation register (SAR) from its most-significant bit (MSB) to least-significiant bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ input resistor. The comparator determines whether the addition of each successively weighted bit current causes the DAC current sum to be greater or less than the input current. If the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 10-bit binary code which accurately represents the input signal to within ±1/2LSB (0.05%).

Upon completion of the sequences, the SAR sends out a $\overline{\text{DATA READY}}$ signal (active low), which also brings the three-state buffers out of their "open" state, making the bit output lines become active high or low, depending on the code in the SAR. When the BLANK and $\overline{\text{CONVERT}}$ line is brought high, the output buffers again go "open", and the SAR is prepared for another conversion cycle. Details of the timing are given further on.

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The bipolar offset input controls a switch which allows a positive bipolar offset current to be injected into the summing (+) node of the comparator to offset the DAC output. The nominal 0 to +10V unipolar input range now becomes a −5V to +5V range. The 5kΩ thin-film input resistor is trimmed so that with a full-scale input signal, an input current will be generated which exactly matches the DAC output with all bits on. (The input resistor is trimmed slightly low to facilitate user trimming, as discussed on the next page.)

POWER SUPPLY SELECTION

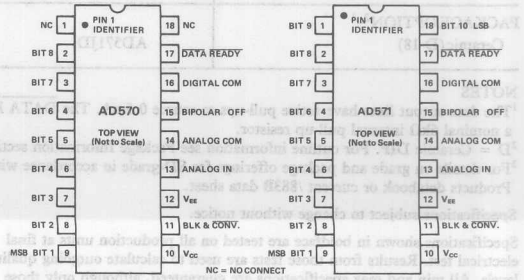
The AD570/AD571 are designed for optimum performance using a +5V and −15V supply, for which the J and S grades are specified. AD571K will also operate with up to a +15V supply, which allows direct interface to CMOS logic.



AD570/AD571 Functional Block Diagram

CONNECTING THE AD570/AD571 FOR STANDARD OPERATION

The AD570/AD571 contain all the active components required to perform a complete A/D conversion. Thus, for most situations, all that is necessary is connection of the power supply (+5 and −15), the analog input, and the conversion start pulse. The functional pin outs are shown below.



AD570 Pin Connections *AD571 Pin Connections*

FULL-SCALE CALIBRATION

The 5kΩ thin-film input resistor is laser trimmed to produce a current which matches the full-scale current of the internal DAC when a full-scale analog input voltage of 10 volts – 1LSB is applied at the input. The input resistor is trimmed in this way so that if a fine-trimming potentiometer is inserted in series with the input signal, the input current at the full-scale input voltage can be trimmed down to match the DAC full-scale current as precisely as desired. However, for many applications the nominal 9.990 (9.961 for the AD570) volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to Pin 13. Typical full-scale calibration error will then be about ±2LSB. If the more precise calibration is desired, a trimmer should be used instead. A 50Ω potentiometer should be used with the AD571 and a 200Ω with the AD570. Set the analog input at full scale and set the trimmer so that the output code is just at the transition between 1111111110 and 1111111111. Each LSB will then have a weight of $10V/2^N$ (where N = number of bits).

BIPOLAR OPERATION

The standard unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin to digital common. If the pin is left open, the bipolar offset current will be switched into the comparator summing node, giving a −5V to +5V range with an offset binary code. The bipolar offset control input is not directly TTL compatible, but a TTL interface for logic control can be constructed as shown in Figure 1.

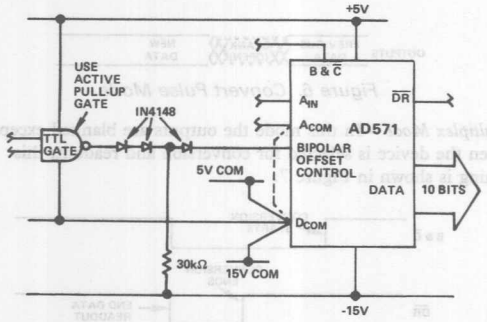


Figure 1. Bipolar Offset Controlled by Logic Gate
Gate Output = 1 Unipolar 0 – 10V Input Range
Gate Output = 0 Bipolar ±5V Input Range

COMMON-MODE RANGE

The AD570/AD571 provide separate analog and digital common connections. The circuit will operate properly with as much as ±200mV of common-mode range between the two commons. This permits more flexible control of system common bussing and digital and analog return.

In normal operation the analog common terminal may generate transient currents of up to 2mA during a conversion. In addition, a static current of about 2mA will flow into analog common in the unipolar mode after a conversion is complete. An additional 1mA will flow in during a blank interval with zero analog input. The analog common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 volt. We recommend the connection of a parallel pair of back-to-back protection diodes between the commons if they are not connected locally.

ZERO OFFSET

The apparent zero point of the AD570/AD571 can be adjusted by inserting an offset voltage between the analog common of the device and the actual signal return or signal common. Figure 2 illustrates two methods of providing this offset for the AD571. Figure 2a shows how the converter zero may be offset by up to ±3 bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode. In bipolar mode R2 should be omitted to obtain a symmetrical range.

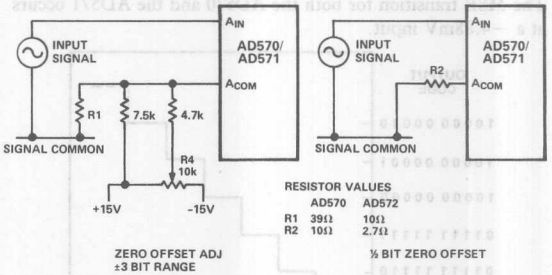


Figure 2a. *Figure 2b.*

Figure 3 shows the nominal transfer curve near zero for an AD571 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics. This offset can easily be accomplished as shown in Figure 2b. At balance

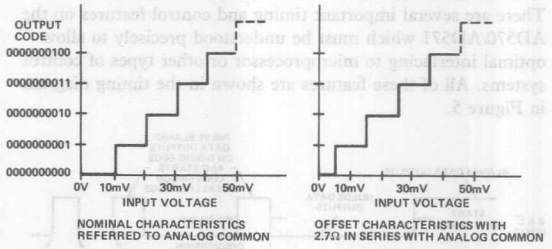


Figure 3. AD571 Transfer Curve – Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights~9.755mV)

(after a conversion) approximately 2mA flows into the analog common terminal. A 2.7Ω resistor in series with this terminal will result in approximately the desired 1/2 bit offset of the transfer characteristics. The nominal 2mA analog common current is not closely controlled in manufacture. If high accuracy is required, a 5Ω potentiometer (connected as a rheostat) can be used as R1. Additional negative offset range may be obtained by using larger values of R1. Of course, if the zero transition point is changed, the full-scale transition point will also move. Thus, if an offset of 1/2LSB is introduced, full-scale trimming as previously described should be done with an analog input of 9.985 volts.

NOTE: During a conversion transient currents from the analog common terminal will disturb the offset voltage. Capacitive

decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling, which returns to analog signal common, should go to the signal input side of the resistive offset network.

BIPOLAR CONNECTION

To obtain the bipolar −5V to +5V range with an offset binary output code the bipolar offset control pin is left open.

A −5.0 volt signal will give a 10-bit code of 00000000 00; an input of 0.00 volts results in an output code of 10000000 00 and +4.99 volts at the input yields the 11111111 11 code. The nominal transfer curve for the AD571 is shown in Figure 4. The MSB transition for both the AD570 and the AD571 occurs at a −4.88mV input.

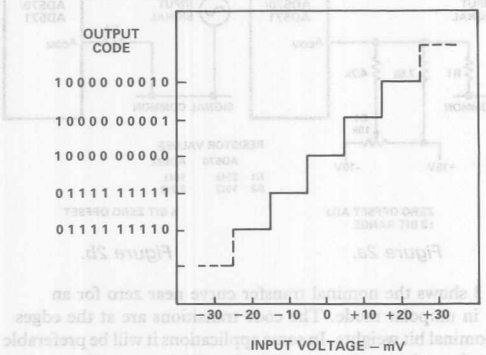


Figure 4. AD571 Transfer Curve – Bipolar Operation

CONTROL AND TIMING OF THE AD570/AD571

There are several important timing and control features on the AD570/AD571 which must be understood precisely to allow optimal interfacing to microprocessor or other types of control systems. All of these features are shown in the timing diagram in Figure 5.

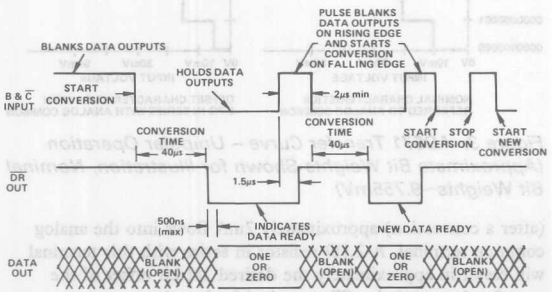


Figure 5. AD570/AD571 Timing and Control Sequences

The normal standby situation is shown at the left end of the drawing. The BLANK and $\overline{\text{CONVERT}}$ (B & $\overline{\text{C}}$) line is held high, the output lines will be "open", and the $\overline{\text{DATA READY}}$ ($\overline{\text{DR}}$) line will be high. This mode is the lowest power state of the device (typically 150mW). When the (B & $\overline{\text{C}}$) line is brought low, the conversion cycle is initiated; but the $\overline{\text{DR}}$ and data lines do not change state. When the conversion cycle is complete (typically 25μs), the $\overline{\text{DR}}$ line goes low, and within 500ns, the

About 1.5μs after the B & $\overline{\text{C}}$ line is again brought high, the $\overline{\text{DR}}$ will go high and the data lines will go open. When the B & $\overline{\text{C}}$ line is again brought low, a new conversion will begin. The minimum pulse width for the B & $\overline{\text{C}}$ line to blank previous data and start a new conversion is 2μs. If the the B & $\overline{\text{C}}$ line is brought high during a conversion, the conversion will stop, and the $\overline{\text{DR}}$ and data lines will not change. If a 2μs or longer pulse is applied to the B & $\overline{\text{C}}$ line during a conversion, the converter will clear and start a new conversion cycle.

CONTROL MODES WITH BLANK AND $\overline{\text{CONVERT}}$

The timing sequence of the AD570/AD571 discussed above allows the devices to be easily operated in a variety of systems with differing control modes. The two most common control modes, the convert pulse mode and the multiplex mode, are illustrated here.

Convert Pulse Mode – In this mode, data is present at the output of the converter at all times except when conversion is taking place. Figure 6 illustrates the timing of this mode. The BLANK and $\overline{\text{CONVERT}}$ line is normally low and conversions are triggered by a positive pulse.

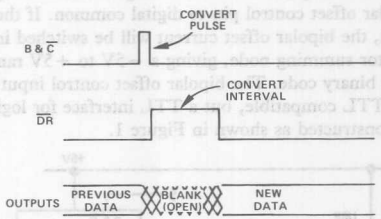


Figure 6. Convert Pulse Mode

Multiplex Mode – In this mode the outputs are blanked except when the device is selected for conversion and readout; this timing is shown in Figure 7.

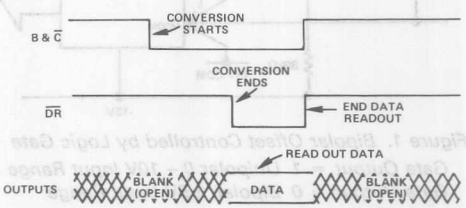


Figure 7. Multiplex Mode

This operating mode allows multiple converters to drive common data lines. All BLANK and $\overline{\text{CONVERT}}$ lines are held high to keep the outputs blanked. A single AD571 is selected, its BLANK and $\overline{\text{CONVERT}}$ line is driven low and at the end of conversion, which is indicated by $\overline{\text{DATA READY}}$ going low, the conversion result will be present at the outputs. When this data has been read from the 10-bit bus, BLANK and $\overline{\text{CONVERT}}$ is restored to the blank mode to clear the data bus for other converters. When several converters are multiplexed in sequence, a new conversion may be started in one AD570/AD571 while data is being read from another. As long as the data is read and the first AD570/AD571 is cleared within 15μs after the start of conversion of the second AD570/AD571, no data overlap will occur.

12-Bit Successive Approximation Integrated Circuit A/D Converter

AD572*

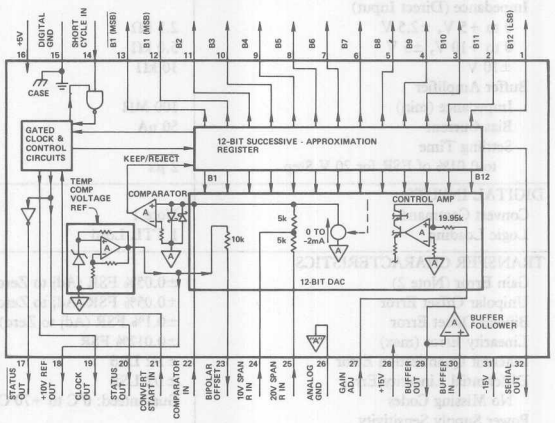
FEATURES

PERFORMANCE
- True 12-Bit Operation: Max Nonlinearity <±0.012%
- Low Gain T.C.: < ±15 ppm/°C (AD572B)
- Low Power: 900 mW
- Fast Conversion Time: < 25 μs
- Monotonic Feedback DAC Guarantees No Missing Codes

VERSATILITY
- Aerospace Temperature Range: −55°C to +125°C (AD572S)
- Positive-True Serial or Parallel Logic Outputs
- Short-Cycle Capability

VALUE
- Precision +10 V Reference for External Application
- Internal Buffer Amplifier
- High Reliability Package

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD572 is a complete 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference, comparator, and buffer amplifier. Its hybrid IC design utilizes MSI digital and linear monolithic chips and active laser trimming of high-stability thin-film resistors to provide superior performance, flexibility and ease of use, combined with IC size, price, and reliability.

Important performance characteristics of the AD572 include a maximum linearity error at 25°C of ±0.012%, gain T.C. below 15 ppm/°C, typical power dissipation of 900 mW, and conversion time of less than 25 μs. Of considerable significance in aerospace applications is the guaranteed performance from −55°C to +125°C of the AD572S. Monotonic operation of the feedback D/A converter guarantees no missing output codes over temperature ranges of 0°C to +70°C, −25°C to +85°C, and −55°C to +125°C.

The design of the AD572 includes scaling resistors that provide analog input signal ranges of ±2.5, ±5.0, ±10, 0 to +5, or 0 to +10 volts. Adding flexibility and value are the +10 V precision reference, which also can be used for external applications, and the input buffer amplifier. All digital signals are fully TTL compatible, and the data output is positive-true and available in either serial or parallel form.

The AD572 is available in three versions with differing guaranteed performance characteristics and operating temperature ranges; the "A" and "B" are specified from −25°C to +85°C, and the "S" from −55°C to +125°C.

PRODUCT DESCRIPTION

The AD572 functional diagram and pinout are shown above. The device consists of the following monolithic bipolar circuit elements:

1. Twelve-bit successive-approximation register
2. Twelve-bit DAC
3. Low-drift comparator
4. Temperature-compensated precision +10 V reference
5. High-impedance buffer follower
6. Gated clock and digital control circuits

ORDERING GUIDE

Model	Specification Temp Range	Max Gain TC	Max Reference TC	Guaranteed Temp Range No Missing Codes	Package Option*
AD572AD	−25°C to +85°C	±30 ppm/°C	±20 ppm/°C	0°C to +70°C	DH-32C
AD572BD	−25°C to +85°C	±15 ppm/°C	±10 ppm/°C	−25°C to +85°C	DH-32C
AD572SD	−55°C to +125°C	±15 ppm/°C (−25°C to +85°C) ±25 ppm/°C (−55°C to +125°C)	±20 ppm/°C	−55°C to +125°C	DH-32C
AD572SD/883B	Meets all specifications after processing to the requirements of MIL-STD-883, Method 5008, Class B. Refer to Analog Devices Military Databook for details.				

*DH-32C = Size Brazed Ceramic Dip for Hybrid (Medium Cavity). For outline information see Package Information section.

*Protected by U.S. Patent Nos. 3,961.326; 3,803,590; and 3,747,088.

This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

AD572—SPECIFICATIONS (typical @ +25°C, ±15 V and +5 V unless otherwise noted)

Model	AD572AD	AD572BD	AD572SD
RESOLUTION	12 Bits	*	*
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±2.5, ±5.0, ±10.0 V	*	*
Unipolar	0 to +5, 0 to +10 V	*	*
Impedance (Direct Input)			
0 to +5 V, ±2.5 V	2.5 kΩ	*	*
0 to +10 V, ±5 V	5.0 kΩ	*	*
±10 V	10 kΩ	*	*
Buffer Amplifier			
Impedance (min)	100 MΩ	*	*
Bias Current	50 nA	*	*
Settling Time			
to 0.01% of FSR for 20 V Step	2 µs	*	*
DIGITAL INPUTS			
Convert Command	Note 1	*	*
Logic Loading	1 TTL Load	*	*
TRANSFER CHARACTERISTICS			
Gain Error (Note 2)	±0.05% FSR (Adj to Zero)	*	*
Unipolar Offset Error	±0.05% FSR (Adj to Zero)	*	*
Bipolar Offset Error	±0.1% FSR (Adj to Zero)	*	*
Linearity Error (max)	±0.012% FSR	*	*
Inherent Quantization Error	±1/2 LSB	*	*
Differential Linearity Error	±1/2 LSB	*	*
No Missing Codes	Guaranteed: 0°C to +70°C	Guaranteed: −25°C to +85°C	Guaranteed: −55°C to +125°C
Power Supply Sensitivity			
±15 V	±0.002% FSR/%ΔV_S	*	*
±5 V	±0.001% FSR/%ΔV_S	*	*
TEMPERATURE COEFFICIENTS			
Gain (max)	±30 ppm/°C (−25°C to +85°C)	±15 ppm/°C (−25°C to +85°C)	±15 ppm/°C (−25°C to +85°C) ±25 ppm/°C (−55°C to +125°C)
Unipolar Offset	±3 ppm FSR/°C	±5 ppm FSR/°C (max)	**
Bipolar Offset (max)	±15 ppm FSR/°C	±7 ppm FSR/°C	**
Linearity	±3 ppm FSR/°C	±2 ppm FSR/°C	**
CONVERSION TIME (max)	25 µs	*	*
DIGITAL OUTPUTS (All Codes Positive-True)			
Parallel Data			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary/Twos Complement	*	*
Output Drive	2 TTL Loads	*	*
Serial Data (NRZ format)			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary	*	*
Output Drive	2 TTL Loads	*	*
Status	Logic "1" during Conversion	*	*
Status	Logic "0" during Conversion	*	*
Output Drive	2 TTL Loads	*	*
Internal Clock			
Output Drive	2 TTL Loads	*	*
Frequency	500 kHz	*	*
INTERNAL REFERENCE VOLTAGE	+10.00 V, ±10 mV typ	*	*
Max External Current	±1 mA	*	*
Voltage Temperature Coefficient (max)	±20 ppm/°C	±10 ppm/°C	*
POWER REQUIREMENTS			
Supply Voltages/Currents	+15 V, ±5% @ +25 mA (40 max)	*	*
	−15 V, ±5% @ −20 mA (35 max)	*	*
	+5 V, ±5% @ +80 mA (150 max)	*	*
Total Power Dissipation	925 mW	*	*
TEMPERATURE RANGE			
Specification	−25°C to +85°C	*	−55°C to +125°C
Operating	−55°C to +125°C	*	*
Storage	−55°C to +150°C	*	*

NOTES
*Same specification as AD572AD.
**Same specifications as AD572BD.
Note 1 Positive pulse 200 ns wide (min). Leading edge ("0" to "1") resets registers. Trailing edge ("1" to "0") initiates conversion.
Note 2 With 50 Ω. 1% fixed resistor in place of Gain Adjust pot.
Specifications subject to change without notice.

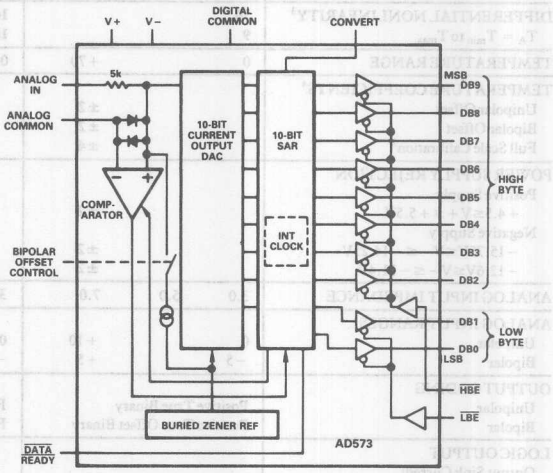
10-Bit A/D Converter

AD573*

FEATURES

- **Complete 10-Bit A/D Converter with Reference, Clock and Comparator**
- **Full 8- or 16-Bit Microprocessor Bus Interface**
- **Fast Successive Approximation Conversion – 20μs typ**
- **No Missing Codes Over Temperature**
- **Operates on +5V and −12V to −15V Supplies**
- **Low Cost Monolithic Construction**

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD573 is a complete 10-bit successive approximation analog to digital converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register (SAR) and 3 state output buffers–all fabricated on a single chip. No external components are required to perform a full accuracy 10-bit conversion in 20μs.

The AD573 incorporates advanced integrated circuit design and processing technologies. The successive approximation function is implemented with I^2L (integrated injection logic). Laser trimming of the high stability SiCr thin film resistor ladder network insures high accuracy, which is maintained with a temperature compensated sub-surface Zener reference.

Operating on supplies of +5V and −12V to −15V, the AD573 will accept analog inputs of 0 to +10V or −5V to +5V. The trailing edge of a positive pulse on the CONVERT line initiates the 20μs conversion cycle. DATA READY indicates completion of the conversion. HIGH BYTE ENABLE (HBE) and LOW BYTE ENABLE (LBE) control the 8-bit and 2-bit three state output buffers.

The AD573 is available in two versions for the 0 to +70°C temperature range, the AD573J and AD573K. The AD573S guarantees ±1LSB relative accuracy and no missing codes from −55°C to +125°C.

Three package configurations are offered. All versions are offered in a 20-pin hermetically sealed ceramic DIP. The AD573J and AD573K are also available in a 20-pin plastic DIP or 20-pin leaded chip carrier.

PRODUCT HIGHLIGHTS

1. The AD573 is a complete 10-bit A/D converter. No external components are required to perform a conversion.
2. The AD573 interfaces to many popular microprocessors without external buffers or peripheral interface adapters. The 10 bits of output data can be read as a 10-bit word or as 8- and 2-bit words.
3. The device offers true 10-bit accuracy and exhibits no missing codes over its entire operating temperature range.
4. The AD573 adapts to either unipolar (0 to +10V) or bipolar (−5V to +5V) analog inputs by simply grounding or opening a single pin.
5. Performance is guaranteed with +5V and −12V or −15V supplies.
6. The AD573 is available in a version compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current /883B datasheet for detailed specifications.

***Protected by U.S. Patent Nos. 3,940,760; 4,213,806; 4,136,349; 4,400,689; and 4,400,690**

AD573—SPECIFICATIONS (T_A = 25V, V+ = +5V, V− = −12V or −15V, all voltages measured with respect to digital common, unless otherwise indicated.)

Model	AD573J Min	AD573J Typ	AD573J Max	AD573K Min	AD573K Typ	AD573K Max	AD573S Min	AD573S Typ	AD573S Max	Units
RESOLUTION		10			10			10		Bits
RELATIVE ACCURACY[1]			±1			±1/2			±1	LSB
$T_A = T_{min}$ to T_{max}			±1			±1/2			±1	LSB
FULL SCALE CALIBRATION[2]		±2			±2				±2	LSB
UNIPOLAR OFFSET			±1			±1/2			±1	LSB
BIPOLAR OFFSET			±1			±1/2			±1	LSB
DIFFERENTIAL NONLINEARITY[3]	**10**			**10**			**10**			Bits
$T_A = T_{min}$ to T_{max}	**9**			**10**			**10**			Bits
TEMPERATURE RANGE	0		+70	0		+70	−55		+125	°C
TEMPERATURE COEFFICIENTS[4]										
Unipolar Offset			±2			±1			±2	LSB
Bipolar Offset			±2			±1			±2	LSB
Full Scale Calibration[2]			±4			±2			±5	LSB
POWER SUPPLY REJECTION										
Positive Supply										
+4.5≤V+≤+5.5V			±2			±1			±2	LSB
Negative Supply										
−15.75V≤V−≤−14.25V			±2			±1			±2	LSB
−12.6V≤V−≤−11.4V			±2			±1			±2	LSB
ANALOG INPUT IMPEDANCE	3.0	5.0	7.0	3.0	5.0	7.0	3.0	5.0	7.0	kΩ
ANALOG INPUT RANGES										
Unipolar	0		+10	0		+10	0		+10	V
Bipolar	−5		+5	−5		+5	−5		+5	V
OUTPUT CODING										
Unipolar	Positive True Binary			Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT										
Output Sink Current										
(V_{OUT} = 0.4V max, T_{min} to T_{max})	**3.2**			**3.2**			**3.2**			mA
Output Source Current[5]										
(V_{OUT} = 2.4V min, T_{min} to T_{max})	**0.5**			**0.5**			**0.5**			mA
Output Leakage			±40			±40			±40	μA
LOGIC INPUTS										
Input Current			±100			±100			±100	μA
Logic "1"	**2.0**			**2.0**			**2.0**			V
Logic "0"			**0.8**			**0.8**			**0.8**	V
CONVERSION TIME										
$T_A = T_{min}$ to T_{max}	**10**	20	**30**	**10**	20	**30**	**10**	20	**30**	μs
POWER SUPPLY										
V+	**+4.5**	+5.0	**+7.0**	**+4.5**	+5.0	**+7.0**	**+4.5**	+5.0	**+7.0**	V
V−	**−11.4**	−15	**−16.5**	**+11.4**	−15	**−16.5**	**−11.4**	−15	**−16.5**	V
OPERATING CURRENT										
V+		15	**20**		15	**20**		15	**20**	mA
V−		9	**15**		9	**15**		9	**15**	mA

NOTES

[1]Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[2]Full-scale calibration is guaranteed trimmable to zero with an external 50Ω potentiometer in place of the 15Ω fixed resistor. Full scale is defined as 10 volts minus 1LSB, or 9.990 volts.

[3]Defined as the resolution for which no missing codes will occur.

[4]Change from +25°C value from +25°C to T_{min} or T_{max}.

[5]The data output lines have active pull-ups to source 0.5mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6kΩ internal pull-up resistor.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

V+ to Digital Common	0 to +7V
V− to Digital Common	0 to −16.5V
Analog Common to Digital Common	±1V
Analog Input to Analog Common	±15V
Control Inputs	0 to V+
Digital Outputs (High Impedance State)	0 to V+
Power Dissipation	800mW

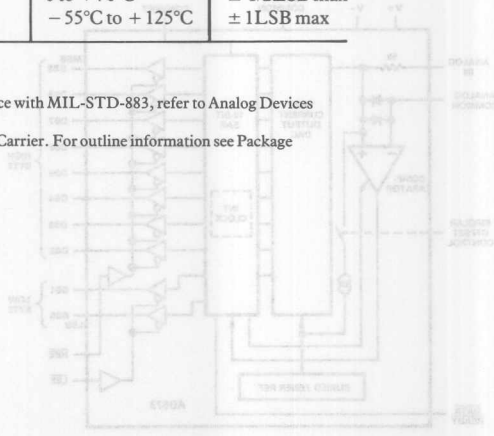
ORDERING GUIDE[1]

Model	Package Option[2]	Temperature Range	Relative Accuracy
AD573JN	20-Pin Plastic DIP (N-20)	0 to +70°C	±1LSB max
AD573KN	20-Pin Plastic DIP (N-20)	0 to +70°C	±1/2LSB max
AD573JP	20-Pin Leaded Chip Carrier (P-20A)	0 to +70°C	±1LSB max
AD573KP	20-Pin Leaded Chip Carrier (P-20A)	0 to +70°C	±1/2LSB max
AD573JD	20-Pin Ceramic DIP (D-20)	0 to +70°C	±1LSB max
AD573KD	20-Pin Ceramic DIP (D-20)	0 to +70°C	±1/2LSB max
AD573SD	20-Pin Ceramic DIP (D-20)	−55°C to +125°C	±1LSB max

NOTES

[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to Analog Devices Military Products Databook.

[2]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.



FUNCTIONAL DESCRIPTION

A block diagram of the AD573 is shown in Figure 1. The positive CONVERT pulse must be at least 500ns wide. $\overline{DR}$ goes high within 1.5μs after the leading edge of the convert pulse indicating that the internal logic has been reset. The negative edge of the CONVERT pulse initiates the conversion. The internal 10-bit current output DAC is sequenced by the integrated injection logic (I^2L) successive approximation register (SAR) from its most significant bit to least significant bit to provide an output current which accurately balances the input signal current through the 5kΩ resistor. The comparator determines whether the addition of each successively weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is more, the bit is turned off. After testing all bits, the SAR contains a 10-bit binary code which accurately represents the input signal to within ½LSB (0.05% of full scale).

The SAR drives $\overline{DR}$ low to indicate that the conversion is complete and that the data is available to the output buffers. $\overline{HBE}$ and $\overline{LBE}$ can then be activated to enable the upper 8-bit and lower 2-bit buffers as desired. $\overline{HBE}$ and $\overline{LBE}$ should be brought high prior to the next conversion to place the output buffers in the high impedance state.

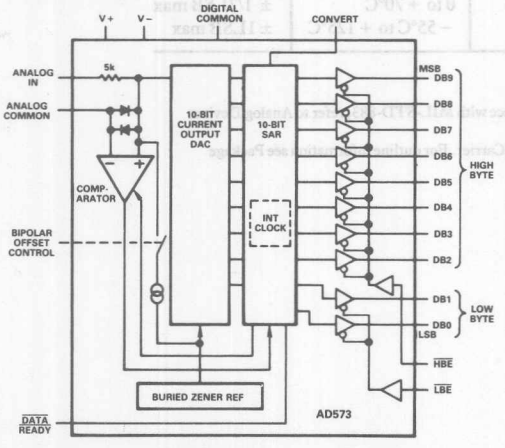


Figure 1. AD573 Functional Block Diagram

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and ensures excellent stability with both time and temperature. The bipolar offset input controls a switch which allows the positive bipolar offset current (exactly equal to the value of the MSB less ½LSB) to be injected into the summing (+) node of the comparator to offset the DAC output. Thus the nominal 0 to +10V unipolar input range becomes a −5V to +5V range. The 5kΩ thin film input resistor is trimmed so that with a full scale input signal, an input current will be generated which exactly matches the DAC output with all bits on.

UNIPOLAR CONNECTION

The AD573 contains all the active components required to perform a complete A/D conversion. Thus, for many applications, all that is necessary is connection of the power supplies (+5V and −12V to −15V), the analog input and the convert pulse. However, there are some features and special connections which should be considered for achieving optimum performance. The functional pin-out is shown in Figure 2.

The standard unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin (pin 16) to digital common (pin 17).

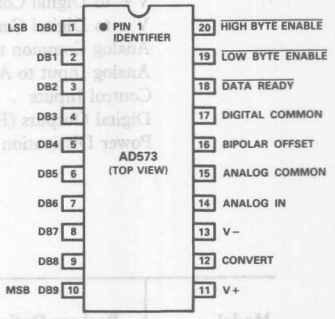


Figure 2. AD573 Pin Connections

Full Scale Calibration

The 5kΩ thin film input resistor is laser trimmed to produce a current which matches the full scale current of the internal DAC–plus about 0.3%–when an analog input voltage of 9.990 volts (10 volts – 1LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 9.99 volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to pin 14. Typical full scale calibration error will then be within ±2LSB or ±0.2%. If more precise calibration is desired, a 50Ω trimmer should be used instead. Set the analog input at 9.990 volts, and set the trimmer so that the output code is just at the transition between 11111111 10 and 11111111 11. Each LSB will then have a weight of 9.766mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have a weight of exactly 10.00mV), a 100Ω resistor and a 100Ω trimmer (or a 200Ω trimmer with good resolution) should be used. Of course, larger full scale ranges can be arranged by using a larger input resistor, but linearity and full scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5kΩ. Figure 3 illustrates the connections required for full scale calibration.

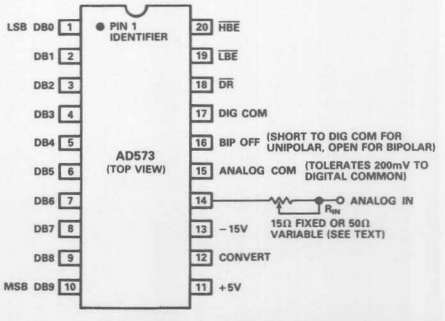


Figure 3. Standard AD573 Connections

Unipolar Offset Calibration

Since the Unipolar Offset is less than ±1LSB for all versions of the AD573, most applications will not require trimming. Figure 4 illustrates two trimming methods which can be used if greater accuracy is necessary.

Figure 4a shows how the converter zero may be offset by up to ±3 bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode.

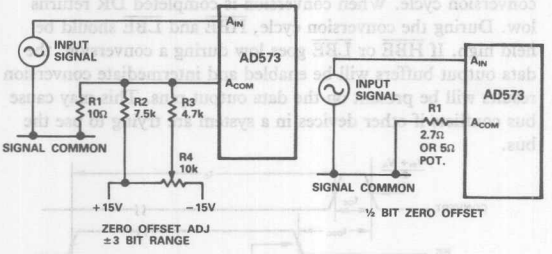


Figure 4a. *Figure 4b.*

Figure 4. Offset Trims

Figure 5 shows the nominal transfer curve near zero for an AD573 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics.

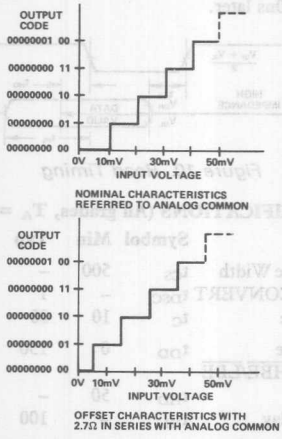


Figure 5. AD573 Transfer Curve – Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights ~ 9.766mV)

This offset can easily be accomplished as shown in Figure 4b. At balance (after a conversion) approximately 2mA flows into the Analog Common terminal. A 2.7Ω resistor in series with this terminal will result in approximately the desired ½ bit offset of the transfer characteristics. The nominal 2mA Analog Common current is not closely controlled in manufacture. If high accuracy is required, a 5Ω potentiometer (connected as a rheostat) can be used as R1. Additional negative offset range may be obtained by using larger values of R1. Of course, if the zero transition point is changed, the full scale transition point will also move. Thus, if an offset of ½LSB is introduced, full scale trimming as described on the previous page should be done with an analog input of 9.985 volts.

NOTE: During a conversion, transient currents from the Analog Common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle appropriately during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling, which returns to analog signal common, should go to the signal input side of the resistive offset network.

BIPOLAR CONNECTION

To obtain the bipolar −5V to +5V range with an offset binary output code, the bipolar offset control pin is left open.

A −5.000 volt signal will give a 10-bit code of 00000000 00; an input of 0.000 volts results in an output code of 10000000 00 and +4.99 volts at the input yields the 11111111 11 code. The nominal transfer curve is shown in Figure 6.

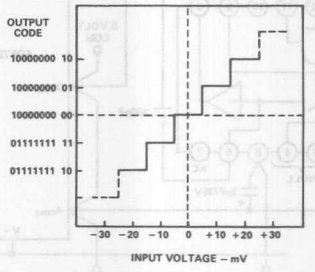


Figure 6. AD573 Transfer Curve – Bipolar Operation

Note that in the bipolar mode, the code transitions are offset ½LSB such that an input voltage of 0 volts ±5mV yields the code representing zero (10000000 00). Each output code is then *centered* on its nominal input voltage.

Full Scale Calibration

Full Scale Calibration is accomplished in the same manner as in Unipolar operation except the full scale input voltage is +4.985 volts.

Negative Full Scale Calibration

The circuit in Figure 4a can also be used in Bipolar operation to offset the input voltage (nominally −5V) which results in the 00000000 00 code. R2 should be omitted to obtain a symmetrical range.

The bipolar offset control input is not directly TTL compatible but a TTL interface for logic control can be constructed as shown in Figure 7.

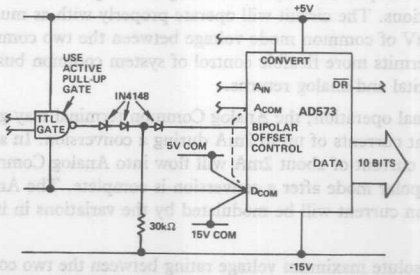


Figure 7. Bipolar Offset Controlled by Logic Gate
Gate Output = 1 Unipolar 0 – 10V Input Range
Gate Output = 0 Bipolar ±5V Input Range

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD573

Many situations in high-speed acquisition systems or digitizing rapidly changing signals require a sample-hold amplifier (SHA) in front of the A-D converter. The SHA can acquire and hold a

signal faster than the converter can perform a conversion. A SHA can also be used to accurately define the exact point in time at which the signal is sampled. For the AD573, a SHA can also serve as a high input impedance buffer.

Figure 8 shows the AD573 connected to the AD582 monolithic SHA for high speed signal acquisition. In this configuration, the AD582 will acquire a 10 volt signal in less than 10μs with a droop rate less than 100μV/ms.

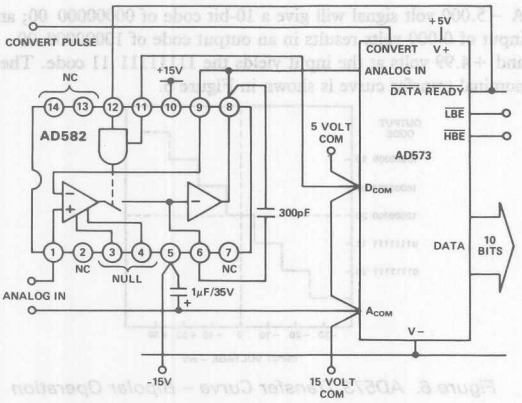


Figure 8. Sample-Hold Interface to the AD573

$\overline{DR}$ goes high after the conversion is initiated to indicate that reset of the SAR is complete. In Figure 8 it is also used to put the AD582 into the hold mode while the AD573 begins its conversion cycle. (The AD582 settles to final value well in advance of the first comparator decision inside the AD573).

$\overline{DR}$ goes low when the conversion is complete placing the AD582 back in the sample mode. Configured as shown in Figure 8, the next conversion can be initiated after a 10μs delay to allow for signal acquisition by the AD582.

Observe carefully the ground, supply, and bypass capacitor connections between the two devices. This will minimize ground noise and interference during the conversion cycle.

GROUNDING CONSIDERATIONS

The AD573 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200mV of common mode voltage between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation, the Analog Common terminal may generate transient currents of up to 2mA during a conversion. In addition a static current of about 2mA will flow into Analog Common in the unipolar mode after a conversion is complete. The Analog Common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 volt. It is recommended that a parallel pair of back-to-back protection diodes be connected between the commons if they are not connected locally.

CONTROL AND TIMING OF THE AD573

The operation of the AD573 is controlled by three inputs: CONVERT, $\overline{HBE}$ and $\overline{LBE}$.

Starting a Conversion

The conversion cycle is initiated by a positive-going CONVERT pulse at least 500ns wide. The rising edge of this pulse resets the internal logic, clears the result of the previous conversion, and sets $\overline{DR}$ high. The falling edge of CONVERT begins the conversion cycle. When conversion is completed $\overline{DR}$ returns low. During the conversion cycle, $\overline{HBE}$ and $\overline{LBE}$ should be held high. If $\overline{HBE}$ or $\overline{LBE}$ goes low during a conversion, the data output buffers will be enabled and intermediate conversion results will be present on the data output pins. This may cause bus conflicts if other devices in a system are trying to use the bus.

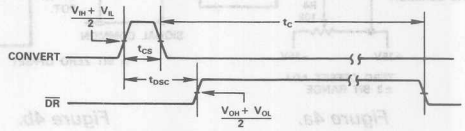


Figure 9. Convert Timing

Reading the Data

The three-state data output buffers are enabled by $\overline{HBE}$ and $\overline{LBE}$. Access time of these buffers is typically 150ns (250 maximum). The Data outputs remain valid until 50ns after the enable signal returns high, and are completely into the high-impedance state 100ns later.

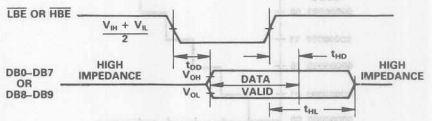


Figure 10. Read Timing

TIMING SPECIFICATIONS (All grades, $T_A = T_{min} - T_{max}$)

Parameter	Symbol	Min	Typ	Max	Units
CONVERT Pulse Width	t_{CS}	500	–	–	ns
$\overline{DR}$ Delay from CONVERT	t_{DSC}	–	1	1.5	μs
Conversion Time	t_C	10	20	30	μs
Data Access Time	t_{DD}	0	150	250	ns
Data Valid after $\overline{HBE}$/$\overline{LBE}$ High	t_{HD}	50	–	–	ns
Output Float Delay	t_{HL}	–	100	200	ns

MICROPROCESSOR INTERFACE CONSIDERATIONS – GENERAL

When an analog-to-digital converter like the AD573 is interfaced to a microprocessor, several details of the interface must be considered. First, a signal to start the converter must be generated; then an appropriate delay period must be allowed to pass before valid conversion data may be read. In most applications, the AD573 can interface to a microprocessor system with little or no external logic.

The most popular control signal configuration consists of decoding the address assigned to the AD573, then gating this signal with the system's WR signal to generate the CONVERT pulse, and gating it with RD to enable the output buffers. The use of a memory address and memory WR and RD signals denotes "memory-mapped" I/O interfacing, while the use of a separate I/O address space denotes "isolated I/O" interfacing. In 8-bit bus systems, the 10-bit AD573 will occupy two locations when data is to be read; therefore, two (usually consecutive) addresses must be decoded. One of the addresses can also be used as

the address which produces the CONVERT signal during WR operations.

Figure 11 shows a generalized diagram of the control logic for an AD573 interfaced to an 8-bit data bus, where two addresses (ADC ADDR and ADC ADDR + 1) have been decoded. ADC ADDR starts the converter when written to (the actual data being written to the converter does not matter) and contains the high byte data during read operations. ADC ADDR + 1 performs no function during write operations, but contains the low byte data during read operations.

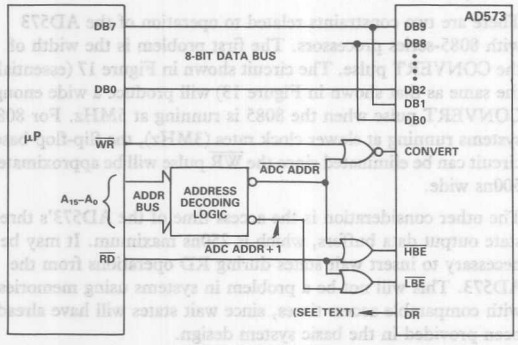


Figure 11. General AD573 Interface to 8-Bit Microprocessor

In systems where this read-write interface is used, at least 30 microseconds (the maximum conversion time) must be allowed to pass between starting a conversion and reading the results. This delay or "timeout" period can be implemented in a short software routine such as a countdown loop, enough dummy instructions to consume 30 microseconds, or enough actual useful instructions to consume the required time. In tightly-timed systems, the $\overline{DR}$ line may be read through an external three-state buffer to determine precisely when a conversion is complete. Higher-speed systems may choose to use $\overline{DR}$ to signal an interrupt to the processor at the end of a conversion.

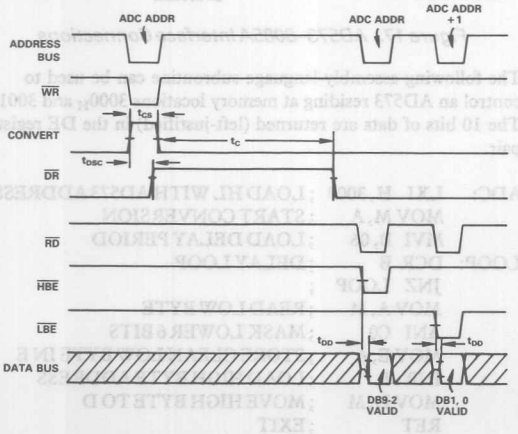


Figure 12. Typical AD573 Interface Timing Diagram

CONVERT Pulse Generation

The AD573 is tested with a CONVERT pulse width of 500ns and will typically operate with a pulse as short as 300ns. However, some microprocessors produce active WR pulses which are shorter than this. Either of the circuits shown in Figure 13 can be used to generate an adequate CONVERT pulse for the AD573.

In both circuits, the short low-going WR pulse sets the CONVERT line high through a flip-flop. The rising edge of $\overline{DR}$ (which signifies that the internal logic has been reset) resets the flip-flop and brings CONVERT low, which starts the conversion.

Note that t_{DSC} is slightly longer when the result of the previous conversion contains a logic 1 on the LSB. This means that the actual CONVERT pulse generated by the circuits in Figure 13 will vary slightly in width.

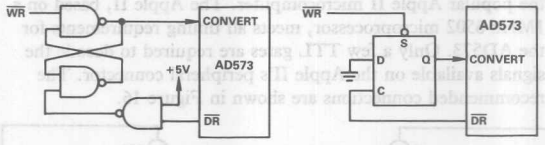


Figure 13a. Using 74LS00 *Figure 13b. Using 1/2 74LS74*

Output Data Format

The AD573 output data is presented in a left-justified format. The 8 MSBs (DB9–DB2, pins 10 through 3) are enabled by $\overline{HBE}$ (pin 20) and the 2 LSBs (DB1, DB0 – pins 2 and 1) are enabled by $\overline{LBE}$ (pin 19). This allows simple interface to 8-bit system buses by overlapping the 2 MSBs and the 2 LSBs. The organization of the data is shown in Figure 14.

When the least significant bits are read ($\overline{LBE}$ brought low), the six remaining bits of the byte will contain meaningless data. These unwanted bits can be masked by logically ANDing the byte with 11000000 (C0 hex), which forces the 6 lower bits to logic 0 while preserving the two most significant bits of the byte.

Note that it is not possible to reconfigure the AD573 for right justified data.

$\overline{HBE}$	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2
$\overline{LBE}$	DB1	DB0	X	X	X	X	X	X

Figure 14. AD573 Output Data Format

In systems where all 10 bits are desired at the same time, $\overline{HBE}$ and $\overline{LBE}$ may be tied together. This is useful in interfacing to 16-bit bus systems. The resulting 10-bit word can then be placed at the high end of the 16-bit bus for left justification or at the low end for right justification.

It is also possible to use the AD573 in a "stand-alone" mode, where the output data buffers are automatically enabled at the end of a conversion cycle. In this mode, the $\overline{DR}$ output is wired to the $\overline{HBE}$ and $\overline{LBE}$ inputs. The outputs thus are forced into the high-impedance state during the conversion period, and valid data becomes available approximately 500ns after the $\overline{DR}$ signal goes low at the end of the conversion. The 500ns delay allows propagation of the least significant bit through the internal logic.

This mode is particularly useful for bench-testing of the AD573, and in applications where dedicated I/O ports of peripheral interface adapter chips are available.

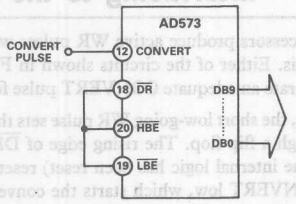


Figure 15. AD573 in "Stand-Alone" Mode (Output Data Valid 500ns After DR Goes Low)

Apple II Microcomputer Interface

The AD573 can provide a flexible, low-cost analog interface for the popular Apple II microcomputer. The Apple II, based on a 1MHz 6502 microprocessor, meets all timing requirements for the AD573. Only a few TTL gates are required to decode the signals available on the Apple II's peripheral connector. The recommended connections are shown in Figure 16.

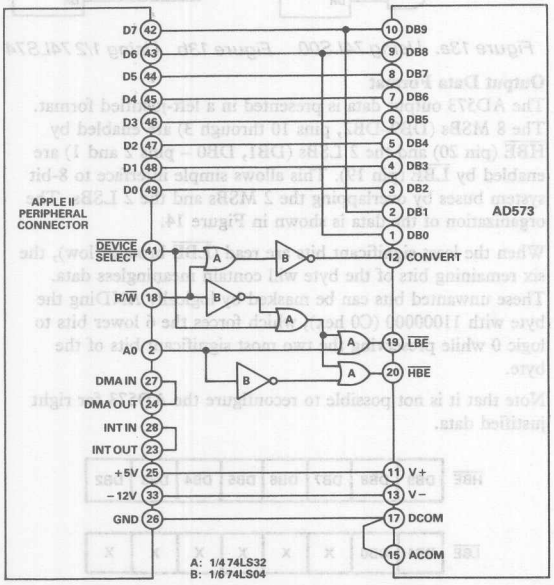


Figure 16. AD573 Interface to Apple II

The BASIC routine listed here will operate the AD573 circuit shown in Figure 16. The conversion is started by POKEing to the location which contains the AD573. The relatively slow execution speed of BASIC eliminates the need for a delay routine between starting and reading the converter. This routine assumes that the AD573 is connected for a ±5 volt input range. Variable I represents the integer value (from 0 to 1023) read from the AD573. Variable V represents the actual value of the input signal (in volts).

```
100 PRINT "WHICH SLOT IS THE A/D IN";:INPUT S
110 A= 49280+16*S
120 POKE A,0
130 L=PEEK(A) :H=PEEK(A+1)
140 I=(4*H)+INT(L/64)
150 V=(I/1024)*10-5
160 PRINT "THE INPUT SIGNAL IS ";V;"VOLTS."
```

It is also possible to write a faster-executing assembly-language routine to control the AD573. Such a routine will require a delay between starting and reading the converter. This can be easily implemented by calling the Apple's WAIT subroutine (which resides at location $FCA8) after loading the accumulator with a number greater than or equal to two.

8085-Series Microprocessor Interface

The AD573 can also be used with 8085-series microprocessors. These processors use separate control signals for RD and WR, as opposed to the single R/$\overline{W}$ control signal used in the 6800/6500 series processors.

There are two constraints related to operation of the AD573 with 8085-series processors. The first problem is the width of the CONVERT pulse. The circuit shown in Figure 17 (essentially the same as that shown in Figure 13) will produce a wide enough CONVERT pulse when the 8085 is running at 5MHz. For 8085 systems running at slower clock rates (3MHz), the flip-flop-based circuit can be eliminated since the $\overline{WR}$ pulse will be approximately 500ns wide.

The other consideration is the access time of the AD573's three-state output data buffers, which is 250ns maximum. It may be necessary to insert wait states during RD operations from the AD573. This will not be a problem in systems using memories with comparable access times, since wait states will have already been provided in the basic system design.

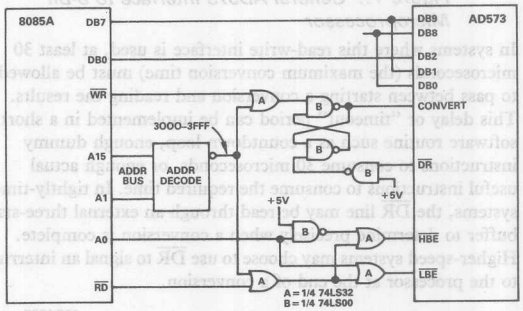


Figure 17. AD573–8085A Interface Connections

The following assembly-language subroutine can be used to control an AD573 residing at memory locations 3000_H and 3001_H. The 10 bits of data are returned (left-justified) in the DE register pair.

```
ADC:   LXI  H,3000  ;LOAD HL WITH AD573 ADDRESS
       MOV  M,A     ;START CONVERSION
       MVI  B,06    ;LOAD DELAY PERIOD
LOOP:  DCR  B       ;DELAY LOOP
       JNZ  LOOP    ;
       MOV  A,M     ;READ LOW BYTE
       ANI  C0      ;MASK LOWER 6 BITS
       MOV  E,A     ;STORE CLEAN LOW BYTE IN E
       INR  L       ;LOAD HIGH BYTE ADDRESS
       MOV  D,M     ;MOVE HIGH BYTE TO D
       RET          ;EXIT
```

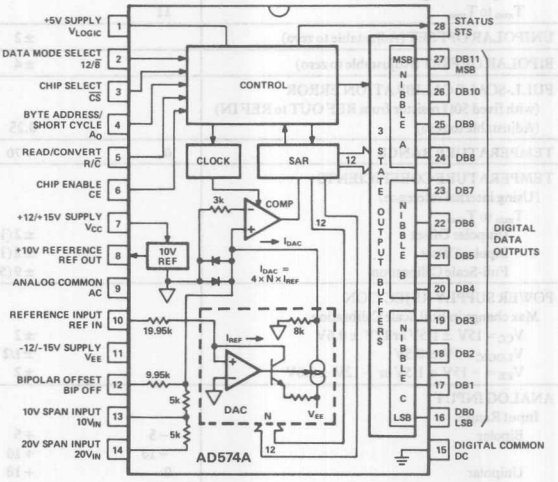
Complete 12-Bit A/D Converter

AD574A*

FEATURES

Complete 12-Bit A/D Converter with Reference and Clock
8- and 16-Bit Microprocessor Bus Interface
Guaranteed Linearity Over Temperature
0 to +70°C – AD574AJ, K, L
−55°C to +125°C – AD574AS, T, U
No Missing Codes Over Temperature
35µs Maximum Conversion Time
Buried Zener Reference for Long-Term Stability and Low Gain T.C. 10ppm/°C max AD574AL
12.5ppm/°C max AD574AU
Ceramic DIP, Plastic DIP or PLCC Package
Available in Higher Speed, Pinout-Compatible Versions (15µs AD674B, 8µs AD774B; 10µs (with SHA) AD1674)
Available in Versions Compliant with MIL-STD-883 and JAN QPL.

BLOCK DIAGRAM AND PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD574A is a complete 12-bit successive-approximation analog-to-digital converter with 3-state output buffer circuitry for direct interface to an 8- or 16-bit microprocessor bus. A high-precision voltage reference and clock are included on-chip, and the circuit guarantees full-rated performance without external circuitry or clock signals.

The AD574A design is implemented using Analog Devices' Bipolar/I^2L process, and integrates all analog and digital functions on one chip. Offset, linearity and scaling errors are minimized by active laser-trimming of thin-film resistors at the wafer stage. The voltage reference uses an implanted buried Zener for low noise and low drift. On the digital side, I^2L logic is used for the successive-approximation register, control circuitry and 3-state output buffers.

The AD574A is available in six different grades. The AD574AJ, K, and L grades are specified for operation over the 0 to +70°C temperature range. The AD574AS, T, and U are specified for the −55°C to +125°C range. All grades are available in a 28-pin hermetically-sealed ceramic DIP. Also, the J, K, and L grades are available in a 28-pin plastic DIP and PLCC, and the J and K grades are available in ceramic LCC.

The S, T, and U grades in ceramic DIP or LCC are available with optional processing to MIL-STD-883C Class B; the T and U grades are available as JAN QPL. The Analog Devices' Military Products Databook should be consulted for details on /883B testing of the AD574A.

***Protected by U.S. Patent Nos. 3,803,590; 4,213,806; 4,511,413; RE 28,633.**

PRODUCT HIGHLIGHTS

1. The AD574A interfaces to most 8- or 16-bit microprocessors. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12 bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).
2. The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges: 0 to +10 and 0 to +20 volts unipolar, −5 to +5 and −10 to +10 volts bipolar. Typical bipolar offset and full-scale calibration errors of ±0.1% can be trimmed to zero with one external component each.
3. The internal buried Zener reference is trimmed to 10.00 volts with 0.2% maximum error and 15ppm/°C typical T.C. The reference is available externally and can drive up to 1.5mA beyond the requirements of the reference and bipolar offset resistors.
4. AD674B (15µs) and AD774B (8µs) provide higher speed, pin compatibility; AD1674 (10µs) includes on-chip Sample-Hold Amplifier (SHA).

AD574A — SPECIFICATIONS (@ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise indicated)

Model	AD574AJ Min	AD574AJ Typ	AD574AJ Max	AD574AK Min	AD574AK Typ	AD574AK Max	AD574AL Min	AD574AL Typ	AD574AL Max	Units
RESOLUTION			12			12			12	Bits
LINEARITY ERROR @ +25°C			±1			±1/2			±1/2	LSB
T_{min} to T_{max}			±1			±1/2			±1/2	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed) T_{min} to T_{max}	11			12			12			Bits
UNIPOLAR OFFSET (Adjustable to zero)			±2			±1			±1	LSB
BIPOLAR OFFSET (Adjustable to zero)			±4			±4			±2	LSB
FULL-SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF OUT to REF IN) (Adjustable to zero)			0.25			0.25			0.125	% of F.S.
TEMPERATURE RANGE	0		+70	0		+70	0		+70	°C
TEMPERATURE COEFFICIENTS (Using internal reference) T_{min} to T_{max}										
Unipolar Offset			±2 (10)			±1 (5)			±1 (5)	LSB (ppm/°C)
Bipolar Offset			±2 (10)			±1 (5)			±1 (5)	LSB (ppm/°C)
Full-Scale Calibration			±9 (50)			±5 (27)			±2 (10)	LSB (ppm/°C)
POWER SUPPLY REJECTION Max change in Full Scale Calibration										
V_{CC} = 15V ±1.5V or 12V ±0.6V			±2			±1			±1	LSB
V_{LOGIC} = 5V ±0.5V			±1/2			±1/2			±1/2	LSB
V_{EE} = −15V ±1.5V or −12V ±0.6V			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar	−5		+5	−5		+5	−5		+5	Volts
	−10		+10	−10		+10	−10		+10	Volts
Unipolar	0		+10	0		+10	0		+10	Volts
	0		+20	0		+20	0		+20	Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
DIGITAL CHARACTERISTICS[1] (T_{min}–T_{max})										
Inputs[2] (CE, $\overline{CS}$, R/$\overline{C}$, A_0)										
Logic "1" Voltage	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	Volts
Logic "0" Voltage	−0.5		+0.8	−0.5		+0.8	−0.5		+0.8	Volts
Current	−20		+20	−20		+20	−20		+20	μA
Capacitance		5			5			5		pF
Outputs (DB11–DB0, STS)										
Logic "1" Voltage (I_{SOURCE}≤500μA)	+2.4			+2.4			+2.4			Volts
Logic "0" Voltage (I_{SINK}≤1.6mA)			+0.4			+0.4			+0.4	Volts
Leakage (DB11–DB0, High-Z State)	−20		+20	−20		+20	−20		+20	μA
Capacitance		5			5			5		pF
POWER SUPPLIES										
Operating Range										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−11.4		−16.5	−11.4		−16.5	−11.4		−16.5	Volts
Operating Current										
I_{LOGIC}		30	40		30	40		30	40	mA
I_{CC}		2	5		2	5		2	5	mA
I_{EE}		18	30		18	30		18	30	mA
POWER DISSIPATION		390	725		390	725		390	725	mW
INTERNAL REFERENCE VOLTAGE	9.98	10.0	10.02	9.98	10.0	10.02	9.99	10.0	10.01	Volts
Output current (available for external loads)[3] (External load should not change during conversion)			1.5			1.5			1.5	mA
PACKAGE OPTIONS[4]										
Ceramic (D-28)		AD574ASD			AD574AKD			AD574ALD		
Plastic (N-28)		AD574AJN			AD574AKN			AD574ALN		
PLCC (P-28A)		AD574AJP			AD574AKP			AD574ALP		
LCC (E-28A)		AD574AJE			AD574AKE					

NOTES

[1]Detailed Timing Specifications appear in the Timing Section.

[2]12/$\overline{8}$ Input is not TTL-compatible and must be hard wired to V_{LOGIC} or Digital Common.

[3]The reference should be buffered for operation on ±12V supplies.

[4]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

Model	AD574AS Min	AD574AS Typ	AD574AS Max	AD574AT Min	AD574AT Typ	AD574AT Max	AD574AU Min	AD574AU Typ	AD574AU Max	Units
RESOLUTION			12			12			12	Bits
LINEARITY ERROR @ +25°C			±1			±1/2			±1/2	LSB
T_{min} to T_{max}			±1			±1			±1	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed) T_{min} to T_{max}	11			12			12			Bits
UNIPOLAR OFFSET (Adjustable to zero)			±2			±1			±1	LSB
BIPOLAR OFFSET (Adjustable to zero)			±4			±4			±2	LSB
FULL-SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF OUT to REF IN) (Adjustable to zero)			0.25			0.25			0.125	% of F.S.
TEMPERATURE RANGE	−55		+125	−55		+125	−55		+125	°C
TEMPERATURE COEFFICIENTS (Using internal reference) T_{min} to T_{max}										
Unipolar Offset			±2 (5)			±1 (2.5)			±1 (2.5)	LSB (ppm/°C)
Bipolar Offset			±4 (10)			±2 (5)			±1 (2.5)	LSB (ppm/°C)
Full-Scale Calibration			±20 (50)			±10 (25)			±5 (12.5)	LSB (ppm/°C)
POWER SUPPLY REJECTION Max change in Full Scale Calibration										
V_{CC} = 15V ±1.5V or 12V ±0.6V			±2			±1			±1	LSB
V_{LOGIC} = 5V ±0.5V			±1/2			±1/2			±1/2	LSB
V_{EE} = −15V ±1.5V or −12V ±0.6V			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar	−5		+5	−5		+5	−5		+5	Volts
	−10		+10	−10		+10	−10		+10	Volts
Unipolar	0		+10	0		+10	0		+10	Volts
	0		+20	0		+20	0		+20	Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
DIGITAL CHARACTERISTICS[1] (T_{min}–T_{max})										
Inputs[2] (CE, $\overline{CS}$, R/$\overline{C}$, A_0)										
Logic "1" Voltage	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	Volts
Logic "0" Voltage	−0.5		+0.8	−0.5		+0.8	−0.5		+0.8	Volts
Current	−20		+20	−20		+20	−20		+20	μA
Capacitance		5			5			5		pF
Outputs (DB11–DB0, STS)										
Logic "1" Voltage (I_{SOURCE}≤500μA)	+2.4			+2.4			+2.4			Volts
Logic "0" Voltage (I_{SINK}≤1.6mA)			+0.4			+0.4			+0.4	Volts
Leakage (DB11–DB0, High-Z State)	−20		+20	−20		+20	−20		+20	μA
Capacitance		5			5			5		pF
POWER SUPPLIES										
Operating Range										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−11.4		−16.5	−11.4		−16.5	−11.4		−16.5	Volts
Operating Current										
I_{LOGIC}		30	40		30	40		30	40	mA
I_{CC}		2	5		2	5		2	5	mA
I_{EE}		18	30		18	30		18	30	mA
POWER DISSIPATION		390	725		390	725		390	725	mW
INTERNAL REFERENCE VOLTAGE	9.98	10.0	10.02	9.98	10.0	10.02	9.99	10.0	10.01	Volts
Output current (available for external loads)[3] (External load should not change during conversion)			1.5			1.5			1.5	mA
PACKAGE OPTIONS[4]										
Ceramic (D-28)		AD574ASD			AD574ATD			AD574AUD		

NOTES

[1]Detailed Timing Specifications appear in the Timing Section.

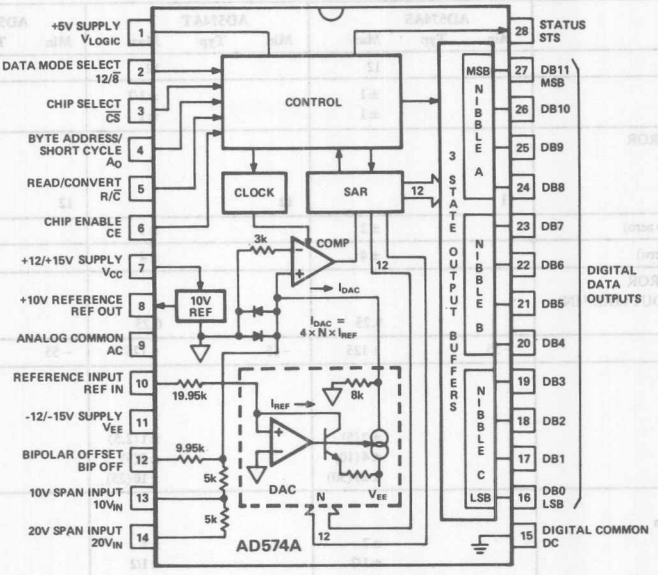
[2]12/$\overline{8}$ Input is *not* TTL-compatible and must be hard wired to V_{LOGIC} or Digital Common.

[3]The reference should be buffered for operation on ±12V supplies.

[4]D = Ceramic DIP. For outline information see Package Information section.

Specifications subject to change without notice.

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AD574A Block Diagram and Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

(Specifications apply to all grades, except where noted)

V_{CC} to Digital Common . . . . . 0 to +16.5V
V_{EE} to Digital Common . . . . . 0 to −16.5V
V_{LOGIC} to Digital Common . . . . . 0 to +7V
Analog Common to Digital Common . . . . . ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to
Digital Common . . . −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to
Analog Common . . . . . V_{EE} to V_{CC}
$20V_{IN}$ to Analog Common . . . . . ±24V
REF OUT . . . . . Indefinite short to common
Momentary short to V_{CC}

Chip Temperature . . . . . 175°C
Power Dissipation 825mW
Lead Temperature, Soldering . . . . . +300°C, 10 sec.
Storage Temperature (Ceramic) . . . . . −65°C to +150°C
(Plastic) . . . . . −25°C to +100°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model[1]	Temperature Range	Linearity Error Max (T_{min} to T_{max})	Resolution No Missing Codes (T_{min} to T_{max})	Max Full Scale T.C. (ppm/°C)
AD574AJ(X)	0 to +70°C	±1LSB	11 Bits	50.0
AD574AK(X)	0 to +70°C	±1/2LSB	12 Bits	27.0
AD574AL(X)	0 to +70°C	±1/2LSB	12 Bits	10.0
AD574AS(X)[2]	−55°C to +125°C	±1LSB	11 Bits	50.0
AD574AT(X)[2]	−55°C to +125°C	±1LSB	12 Bits	25.0
AD574AU(X)[2]	−55°C to +125°C	±1LSB	12 Bits	12.5

NOTES
[1]X = Package designator. Available packages are:
D (D-28) for all grades.
E (E-28A) for J and K grades and /883B processed S, T and U grades.
N (N-28) for J, K, and L grades.
P (P-28A)for PLCC in J, K grades.
Example: AD574AKN is K grade in plastic DIP.
[2]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to Analog Devices Military Products Databook.

THE AD574A OFFERS GUARANTEED MAXIMUM LINEARITY ERROR OVER THE FULL OPERATING TEMPERATURE RANGE

DEFINITIONS OF SPECIFICATIONS

LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs 1/2LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1 1/2LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The AD574AK, L, T, and U grades are guaranteed for maximum nonlinearity of ±1/2LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The AD574AJ and S grades are guaranteed to ±1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the AD574AK, L, T, and U grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The AD574AJ and S grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following two pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET

In the bipolar mode the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±1/2LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

LEFT-JUSTIFIED DATA

The data format used in the AD574A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

FULL-SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1 1/2LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full-scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 3 and 4.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

POWER SUPPLY REJECTION

The standard specifications for the AD574A assume use of +5.00 and ±15.00 or ±12.00V supplies. The only effect of power supply error on the performance of the device will be a small change in the full-scale calibration. This will result in a linear change in all lower-order codes. The specifications show the maximum full-scale change from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full-scale range or 2.44mV out of 10 volts for a 12-bit ADC.

CIRCUIT OPERATION

The AD574A is a complete 12-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD574A is shown in Figure 1.

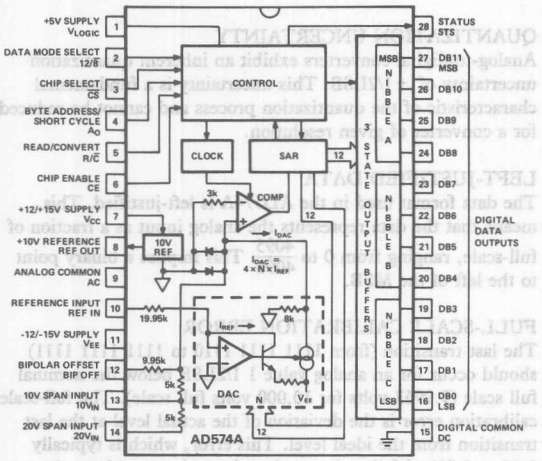


Figure 1. Block Diagram of AD574A 12-Bit A-to-D Converter

When the control section is commanded to initiate a conversion (as described later), it enables the clock and resets the successive-approximation register (SAR) to all zeros. Once a conversion cycle has begun, it cannot be stopped or re-started and data is not available from the output buffers. The SAR, timed by the clock, will sequence through the conversion cycle and return an end-of-convert flag to the control section. The control section will then disable the clock, bring the output status flag low, and enable control functions to allow data read functions by external command.

During the conversion cycle, the internal 12-bit current output DAC is sequenced by the SAR from the most significant bit (MSB) to least significant bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ (or 10kΩ) input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2LSB.

The temperature-compensated buried zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ±0.2%; it can supply up to 1.5mA to an external load in addition to the requirements of the reference input resistor (0.5mA) and bipolar offset resistor (1mA) when the AD574A is powered from ±15V supplies. If the AD574A is used with ±12V supplies, or if external current must be supplied over the full temperature range, an external buffer amplifier is recommended. Any external load on the AD574A reference must remain constant during conversion. The thin-film application resistors are trimmed to match the full-scale output current of the DAC. There are two 5kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10kΩ bipolar offset resistor is grounded for unipolar operation and connected to the 10 volt reference for bipolar operation.

DRIVING THE AD574 ANALOG INPUT

The internal circuitry of the AD574 dictates that its analog input be driven by a low source impedance. Voltage changes at the current summing node of the internal comparator result in abrupt modulations of the current at the analog input. For accurate 12-bit conversions the driving source must be capable of holding a constant output voltage under these dynamically changing load conditions.

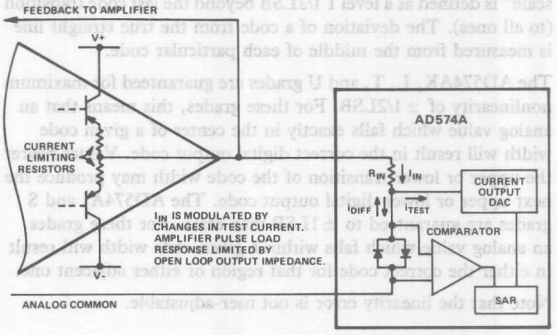


Figure 2. Op Amp – AD574A Interface

The output impedance of an op amp has an open-loop value which, in a closed loop, is divided by the loop gain available at the frequency of interest. The amplifier should have acceptable loop gain at 500kHz for use with the AD574A. To check whether the output properties of a signal source are suitable, monitor the AD574's input with an oscilloscope while a conversion is in progress. Each of the 12 disturbances should subside in 1μs or less.

For applications involving the use of a sample-and-hold amplifier, the AD585 is recommended. The AD711 or AD544 op amps are recommended for dc applications.

SAMPLE-AND-HOLD AMPLIFIERS

Although the conversion time of the AD574A is a maximum of 35μs, to achieve accurate 12-bit conversions of frequencies greater than a few Hz requires the use of a sample-and-hold amplifier (SHA). If the voltage of the analog input signal driving the AD574A changes by more than 1/2LSB over the time interval needed to make a conversion, then the input requires a SHA.

The AD585 is a high-linearity SHA capable of directly driving the analog input of the AD574A. The AD585's fast acquisition time, low aperture and low aperture jitter are ideally suited for high-speed data acquisition systems. Consider the AD574A converter with a 35μs conversion time and an input signal of 10V p-p: the maximum frequency which may be applied to achieve rated accuracy is 1.5Hz. However, with the addition of an AD585, as shown in Figure 3, the maximum frequency increases to 26kHz.

The AD585's low output impedance, fast-loop response, and low droop maintain 12-bits of accuracy under the changing load conditions that occur during a conversion, making it suitable for use in high-accuracy conversion systems. Many other SHAs cannot achieve 12-bits of accuracy and can thus compromise a

system. The AD585 is recommended for AD574A applications requiring a sample and hold.

An alternate approach is to use the AD1674, which combines the ADC and SHA on one chip, with a total throughput time of 10μs.

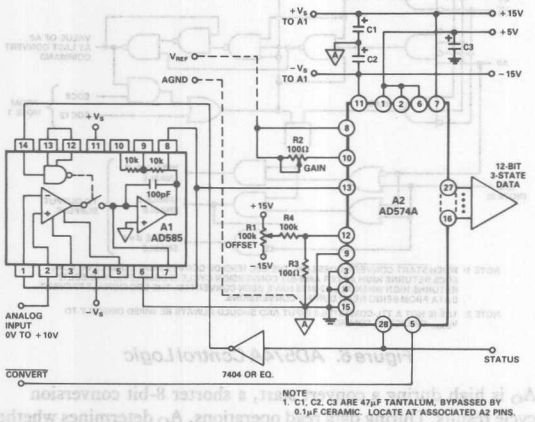


Figure 3. AD574A with AD585 Sample and Hold

SUPPLY DECOUPLING AND LAYOUT CONSIDERATIONS

It is critically important that the AD574A power supplies be filtered, well regulated, and free from high-frequency noise. Use of noisy supplies will cause unstable output codes. Switching power supplies are not recommended for circuits attempting to achieve 12-bit accuracy unless great care is used in filtering any switching spikes present in the output. Remember that a few millivolts of noise represents several counts of error in a 12-bit ADC.

Decoupling capacitors should be used on all power supply pins; the +5V supply decoupling capacitor should be connected directly from pin 1 to pin 15 (digital common) and the $+V_{CC}$ and $-V_{EE}$ pins should be decoupled directly to analog common (pin 9). A suitable decoupling capacitor is a 4.7μF tantalum type in parallel with a 0.1μF disc ceramic type.

Circuit layout should attempt to locate the AD574A, associated analog input circuitry, and interconnections as far as possible from logic circuitry. For this reason, the use of wire-wrap circuit construction is not recommended. Careful printed-circuit construction is preferred.

GROUNDING CONSIDERATIONS

The analog common at pin 9 is the ground reference point for the internal reference and is thus the "high quality" ground for the AD574A; it should be connected directly to the analog reference point of the system. In order to achieve all of the high-accuracy performance available from the AD574A in an environment of high digital noise content, the analog and digital commons should be connected together at the package. In some situations, the digital common at pin 15 can be connected to the most convenient ground reference point; analog power return is preferred.

UNIPOLAR RANGE CONNECTIONS FOR THE AD574A

The AD574A contains all the active components required to perform a complete 12-bit A/D conversion. Thus, for most situations, all that is necessary is connection of the power supplies (+5, +12/+15 and −12/−15 volts), the analog input, and the conversion initiation command, as discussed on the next page. Analog input connections and calibration are easily accomplished; the unipolar operating mode is shown in Figure 4.

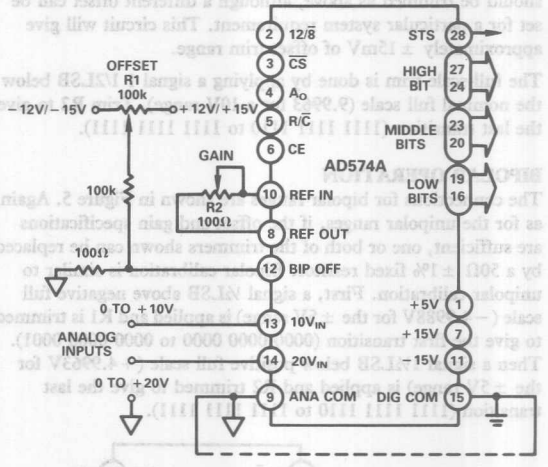


Figure 4. Unipolar Input Connections

All of the thin-film application resistors of the AD574A are trimmed for absolute calibration. Therefore, in many applications, no calibration trimming will be required. The absolute accuracy for each grade is given in the specification tables. For example, if no trims are used, the AD574AK guarantees ±1LSB max zero offset error and ±0.25% (10LSB) max full-scale error. (Typical full-scale error is ±2LSB.) If the offset trim is not required, pin 12 can be connected directly to pin 9; the two resistors and trimmer for pin 12 are then not needed. If the full-scale trim is not needed, a 50Ω ±1% metal film resistor should be connected between pin 8 and pin 10.

The analog input is connected between pin 13 and pin 9 for a 0 to +10V input range, between 14 and pin 9 for a 0 to +20V input range. The AD574A easily accommodates an input signal beyond the supplies. For the 10 volt span input, the LSB has a nominal value of 2.44mV; for the 20 volt span, 4.88mV. If a 10.24V range is desired (nominal 2.5mV/bit), the gain trimmer (R2) should be replaced by a 50Ω resistor, and a 200Ω trimmer inserted in series with the analog input to pin 13 for a full-scale range of 20.48V (5mV/bit), use a 500Ω trimmer into pin 14. The gain trim described below is now done with these trimmers. The nominal input impedance into pin 13 is 5kΩ, and 10kΩ into pin 14.

The AD574A is intended to have a nominal 1/2LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2LSB (1.22mV for 10V range).

If pin 12 is connected to pin 9, the unit will behave in this manner, within specifications. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±15mV of offset trim range.

The full-scale trim is done by applying a signal 1 1/2LSB below the nominal full scale (9.9963 for a 10V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 5. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient, one or both of the trimmers shown can be replaced by a 50Ω ±1% fixed resistor. Bipolar calibration is similar to unipolar calibration. First, a signal ½LSB above negative full scale (−4.9988V for the ±5V range) is applied and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1½LSB below positive full scale (+4.9963V for the ±5V range) is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

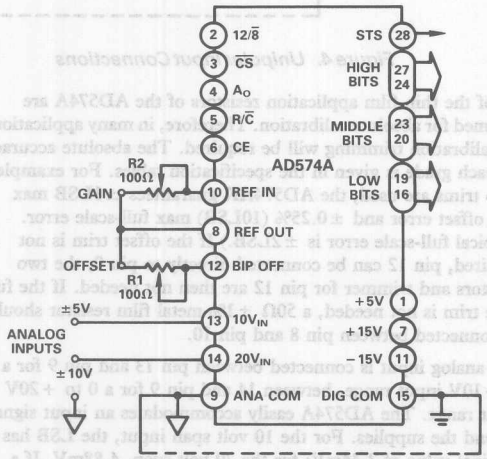
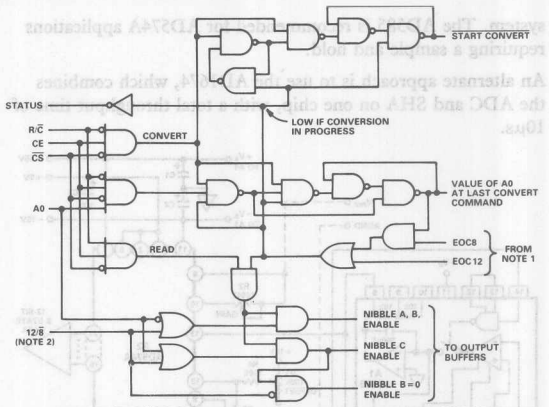


Figure 5. Bipolar Input Connections

CONTROL LOGIC

The AD574A contains on-chip logic to provide conversion initiation and data read operations from signals commonly available in microprocessor systems. Figure 6 shows the internal logic circuitry of the AD574A.

The control signals CE, $\overline{CS}$, and R/$\overline{C}$ control the operation of the converter. The state of R/$\overline{C}$ when CE and $\overline{CS}$ are both asserted determines whether a data read (R/$\overline{C}$ = 1) or a convert (R/$\overline{C}$ = 0) is in progress. The register control inputs A_0 and 12/$\overline{8}$ control conversion length and data format. The A_0 line is usually tied to the least significant bit of the address bus. If a conversion is started with A_0 low, a full 12-bit conversion cycle is initiated. If



NOTE 1: WHEN START CONVERT GOES LOW, THE EOC (END OF CONVERSION) SIGNALS GO LOW. EOC8 RETURNS HIGH AFTER AN 8-BIT CONVERSION CYCLE IS COMPLETE, AND EOC12 RETURNS HIGH WHEN ALL 12 BITS HAVE BEEN CONVERTED. THE EOC SIGNALS PREVENT DATA FROM BEING READ DURING CONVERSIONS.

NOTE 2: 12/$\overline{8}$ IS NOT A TTL-COMPATIBLE INPUT AND SHOULD ALWAYS BE WIRED DIRECTLY TO V_{LOGIC} OR DIGITAL COMMON.

Figure 6. AD574A Control Logic

A_0 is high during a convert start, a shorter 8-bit conversion cycle results. During data read operations, A_0 determines whether the three-state buffers containing the 8 MSBs of the conversion result (A_0 = 0) or the 4 LSBs (A_0 = 1) are enabled. The 12/$\overline{8}$ pin determines whether the output data is to be organized as two 8-bit words (12/$\overline{8}$ tied to DIGITAL COMMON) or a single 12-bit word (12/$\overline{8}$ tied to V_{LOGIC}). The 12/$\overline{8}$ pin is not TTL-compatible and must be hard-wired to either V_{LOGIC} or DIGITAL COMMON. In the 8-bit mode, the byte addressed when A_0 is high contains the 4 LSBs from the conversion followed by four trailing zeroes. This organization allows the data lines to be overlapped for direct interface to 8-bit buses without the need for external three-state buffers.

It is not recommended that A_0 change state during a data read operation. Asymmetrical enable and disable times of the three-state buffers could cause internal bus contention resulting in potential damage to the AD574A.

An output signal, STS, indicates the status of the converter. STS goes high at the beginning of a conversion and returns low when the conversion cycle is complete.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-Bit Conversion
1	0	0	X	1	Initiate 8-Bit Conversion
1	0	1	Pin 1	X	Enable 12-Bit Parallel Output
1	0	1	Pin 15	0	Enable 8 Most Significant Bits
1	0	1	Pin 15	1	Enable 4LSBs +4 Trailing Zeroes

Table I. AD574A Truth Table

TIMING

The AD574A is easily interfaced to a wide variety of microprocessors and other digital systems. The following discussion of the timing requirements of the AD574A control signals should provide the system designer with useful insight into the operation of the device.

CONVERT START TIMING – FULL CONTROL MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DSC}	STS Delay from CE			400	ns
t_{HEC}	CE Pulse Width	300			ns
t_{SSC}	$\overline{CS}$ to CE Setup	300			ns
t_{HSC}	$\overline{CS}$ Low During CE High	200			ns
t_{SRC}	R/$\overline{C}$ to CE Setup	250			ns
t_{HRC}	R/$\overline{C}$ Low During CE High	200			ns
t_{SAC}	A_O to CE Setup	0			ns
t_{HAC}	A_O Valid During CE High	300			ns
t_C	Conversion Time				
	8-Bit Cycle	10		24	µs
	12-Bit Cycle	15		35	µs

Figure 7 shows a complete timing diagram for the AD574A convert start operation. R/$\overline{C}$ should be low before both CE and $\overline{CS}$ are asserted; if R/$\overline{C}$ is high, a read operation will momentarily occur, possibly resulting in system bus contention. Either CE or $\overline{CS}$ may be used to initiate a conversion; however, use of CE is recommended since it includes one less propagation delay than $\overline{CS}$ and is the faster input. In Figure 7, CE is used to initiate the conversion.

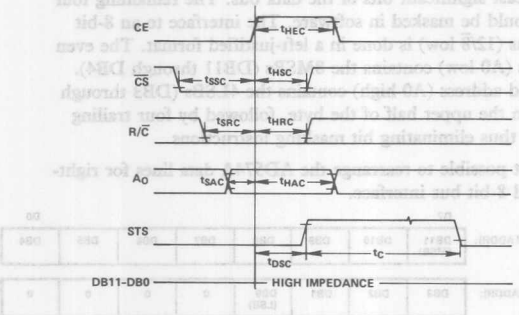


Figure 7. Convert Start Timing

Once a conversion is started and the STS line goes high, convert start commands will be ignored until the conversion cycle is complete. The output data buffers cannot be enabled during conversion.

Figure 8 shows the timing for data read operations. During data read operations, access time is measured from the point where CE and R/$\overline{C}$ both are high (assuming $\overline{CS}$ is already low). If $\overline{CS}$ is used to enable the device, access time is extended by 100ns.

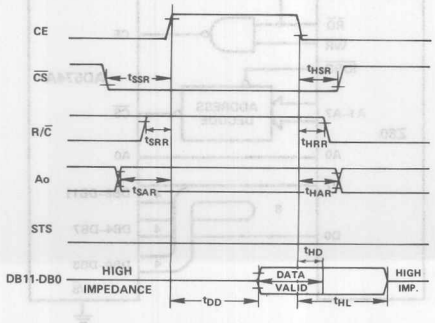


Figure 8. Read Cycle Timing

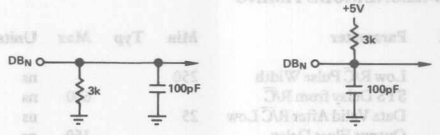
In the 8-bit bus interface mode (12/$\overline{8}$ input wired to DIGITAL COMMON), the address bit, A_O, must be stable at least 150ns prior to $\overline{CE}$ going high and must remain stable during the entire read cycle. If A_O is allowed to change, damage to the AD574A output buffers may result.

READ TIMING – FULL CONTROL MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DD}[1]	Access Time (from CE)			200	ns
t_{HD}	Data Valid after CE Low	25			ns
t_{HL}[2]	Output Float Delay			100	ns
t_{SSR}	$\overline{CS}$ to CE Setup	150			ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0			ns
t_{SAR}	A_O to CE Setup	150			ns
t_{HSR}	$\overline{CS}$ Valid After CE Low	50			ns
t_{HRR}	R/$\overline{C}$ High After CE Low	0			ns
t_{HAR}	A_O Valid After CE low	50			ns

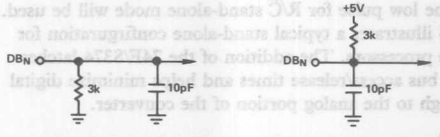
[1] t_{DD} is measured with the load circuit of Figure 9 and defined as the time required for an output to cross 0.4V or 2.4V.

[2] t_{HL} is defined as the time required for the data lines to change 0.5V when loaded with the circuit of Figure 10.



a. High-Z to Logic 1 *b. High-Z to Logic 0*

Figure 9. Load Circuit for Access Time Test



a. Logic 1 to High-Z *b. Logic 0 to High-Z*

Figure 10. Load Circuit for Output Float Delay Test

"STAND-ALONE" OPERATION

The AD574A can be used in a "stand-alone" mode, which is useful in systems with dedicated input ports available and thus not requiring full bus interface capability.

In this mode, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_O are wired low, and conversion is controlled by R/$\overline{C}$. The three-state buffers are enabled when R/$\overline{C}$ is high and a conversion starts when R/$\overline{C}$ goes low. This allows two possible control signals – a high pulse or a low pulse. Operation with a low pulse is shown in Figure 11. In this case, the outputs are forced into the high-impedance state in response to the falling edge of R/$\overline{C}$ and return

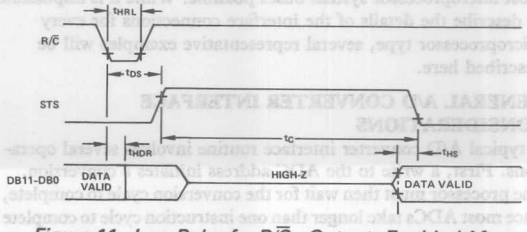


Figure 11. Low Pulse for R/$\overline{C}$ – Outputs Enabled After Conversion

to valid logic levels after the conversion cycle is completed. The STS line goes high 600ns after R/$\overline{C}$ goes low and returns low 300ns after data is valid.

If conversion is initiated by a high pulse as shown in Figure 12, the data lines are enabled during the time when R/$\overline{C}$ is high. The falling edge of R/$\overline{C}$ starts the next conversion, and the data lines return to three-state (and remain three-state) until the next high pulse of R/$\overline{C}$.

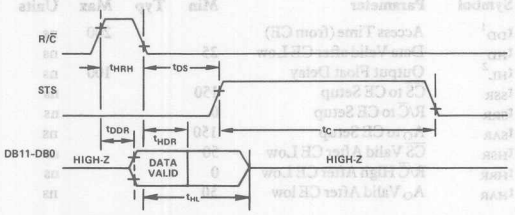


Figure 12. High Pulse for R/$\overline{C}$ – Outputs Enabled While R/$\overline{C}$ High, Otherwise High-Z

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	250			ns
t_{DS}	STS Delay from R/$\overline{C}$			600	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HL}	Output Float Delay			150	ns
t_{HS}	STS Delay After Data Valid	300		1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	300			ns
t_{DDR}	Data Access Time			250	ns

Usually the low pulse for R/$\overline{C}$ stand-alone mode will be used. Figure 13 illustrates a typical stand-alone confirguration for 8086 type processors. The addition of the 74F/S374 latches improves bus access/release times and helps minimize digital feedthrough to the analog portion of the converter.

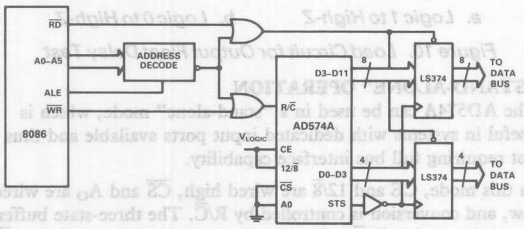


Figure 13. 8086 Stand-Alone Configuration

INTERFACING THE AD574A TO MICROPROCESSORS

The control logic of the AD574A makes direct connection to most microprocessor system buses possible. While it is impossible to describe the details of the interface connections for every microprocessor type, several representative examples will be described here.

GENERAL A/D CONVERTER INTERFACE CONSIDERATIONS

A typical A/D converter interface routine involves several operations. First, a write to the ADC address initiates a conversion. The processor must then wait for the conversion cycle to complete, since most ADCs take longer than one instruction cycle to complete a conversion. Valid data can, of course, only be read after the conversion is complete. The AD574A provides an output signal (STS) which indicates when a conversion is in progress. This signal can be polled by the processor by reading it through an external three-state buffer (or other input port). The STS signal can also be used to generate an interrupt upon completion of conversion, if the system timing requirements are critical (bear in mind that the maximum conversion time of the AD574A is only 35 microseconds) and the processor has other tasks to perform during the ADC conversion cycle. Another possible time-out method is to assume that the ADC will take 35 microseconds to convert, and insert a sufficient number of "do-nothing" instructions to ensure that 35 microseconds of processor time is consumed.

Once it is established that the conversion is finished, the data can be read. In the case of an ADC of 8-bit resolution (or less), a single data read operation is sufficient. In the case of converters with more data bits than are available on the bus, a choice of data formats is required, and multiple read operations are needed. The AD574A includes internal logic to permit direct interface to 8-bit or 16-bit data buses, selected by connection of the 12/$\overline{8}$ input. In 16-bit bus applications (12/$\overline{8}$ high) the data lines (DB11 through DB0) may be connected to either the 12 most significant or 12 least significant bits of the data bus. The remaining four bits should be masked in software. The interface to an 8-bit data bus (12/$\overline{8}$ low) is done in a left-justified format. The even address (A0 low) contains the 8MSBs (DB11 through DB4). The odd address (A0 high) contains the 4LSBs (DB3 through DB0) in the upper half of the byte, followed by four trailing zeroes, thus eliminating bit masking instructions.

It is not possible to rearrange the AD574A data lines for right-justified 8-bit bus interface.

	D7							D0
XXX0 (EVEN ADDR):	DB11 (MSB)	DB10	DB9	DB8	DB7	DB6	DB5	DB4
XXX1 (ODD ADDR):	DB3	DB2	DB1	DB0 (LSB)	0	0	0	0

Figure 14. AD574A Data Format for 8-Bit Bus

SPECIFIC PROCESSOR INTERFACE EXAMPLES

Z-80 System Interface

The AD574A may be interfaced to the Z-80 processor in an I/O or memory mapped configuration. Figure 15 illustrates an I/O mapped configuration. The Z-80 uses address lines A0-A7 to decode the I/O port address.

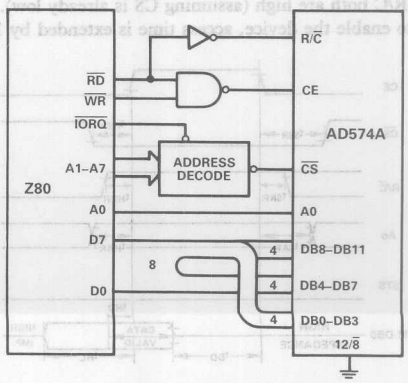


Figure 15. Z80–AD574A Interface

An interesting feature of the Z-80 is that during I/O operations a single wait state is automatically inserted, allowing the AD574A to be used with Z-80 processors having clock speeds up to 4MHz. For applications faster than 4MHz use the wait state generator in Figure 16. In a memory mapped configuration the AD574A may be interfaced to Z-80 processors with clock speeds of up to 2.5MHz.

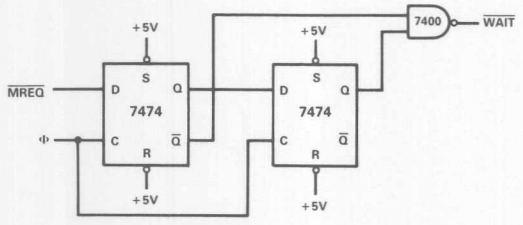


Figure 16. Wait State Generator

IBM PC Interface

The AD574A appears in Figure 17 interfaced to the 4MHz 8088 processor of an IBM PC. Since the device resides in I/O space, its address is decoded from only the lower ten address lines and must be gated with AEN (active low) to mask out internal DMA cycles which use the same I/O address space. This active low signal is applied to $\overline{CS}$. $\overline{IOR}$ and $\overline{IOW}$ are used to initiate the conversion and read, and are gated together to drive the chip enable, CE. Because the data bus width is limited to 8 bits, the AD574A data resides in two adjacent addresses selected by A0.

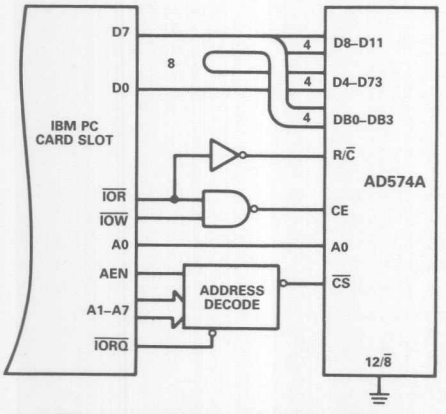


Figure 17. IBM PC – AD574A Interface

Note: Due to the large number of of options that may be installed in the PC, the I/O bus loading should be limited to one Schottky TTL load. Therefore, a buffer/driver should be used when interfacing more than two AD574As to the I/O bus.

8086 Interface

The data mode select pin (12/$\overline{8}$) of the AD574A should be connected to V_{LOGIC} to provide a 12-bit data output. To prevent possible bus contention, a demultiplexed and buffered address/data bus is recommended. In the cases where the 8-bit short conversion cycle is not used, A0 should be tied to digital common. Figure 18 shows a typical 8086 configuration.

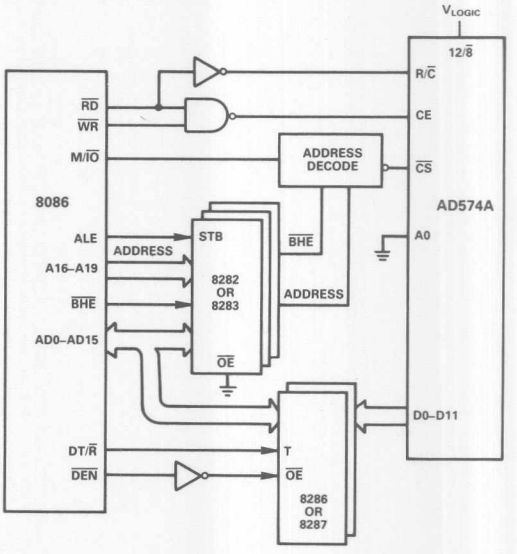


Figure 18. 8086 – AD574A with Buffered Bus Interface

For clock speeds greater than 4MHz wait state insertion similar to Figure 16 is recommended to ensure sufficient CE and R/$\overline{C}$ pulse duration.

The AD574A can also be interfaced in a stand-alone mode (see Figure 13). A low-going pulse derived from the 8086's $\overline{WR}$ signal logically ORed with a low address decode starts the conversion. At the end of the conversion, STS clocks the data into the three-state latches.

68000 Interface

The AD574, when configured in the stand-alone mode, will easily interface to the 4MHz version of the 68000 microprocessor. The 68000 R/$\overline{W}$ signal combined with a low address decode initiates conversion. The $\overline{UDS}$ or $\overline{LDS}$ signal, with the decoded address, generates the $\overline{DTACK}$ input to the processor, latching in the AD574A's data. Figure 19 illustrates this configuration.

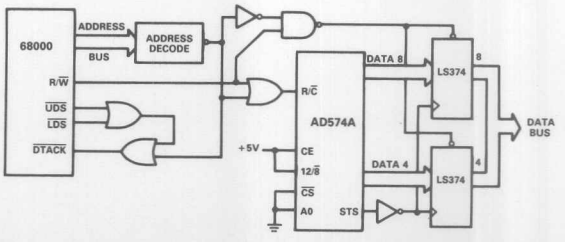
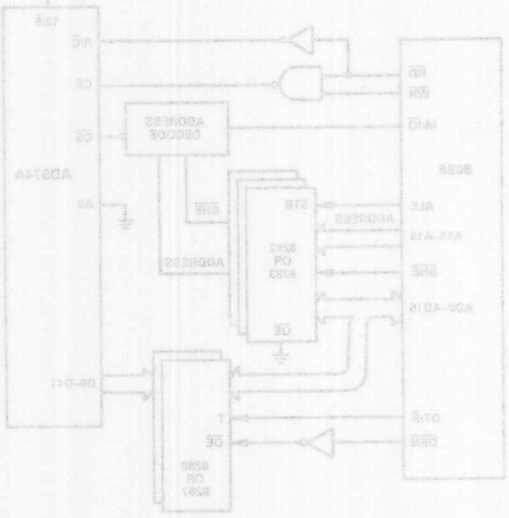
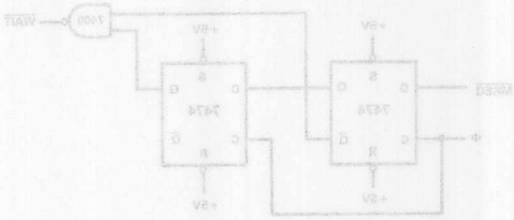
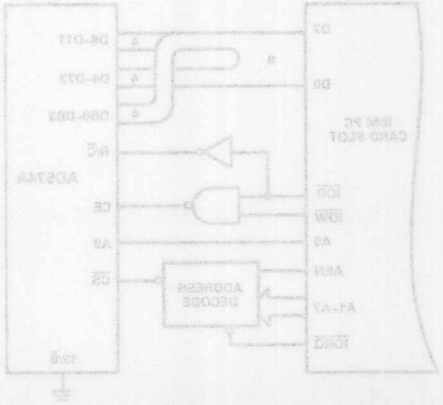
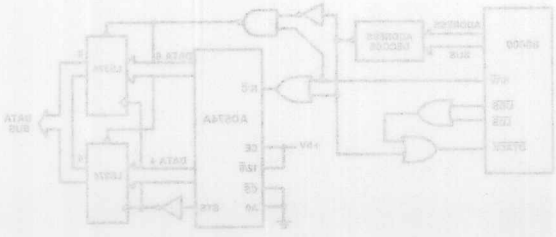


Figure 19. 68000 – AD574A Interface









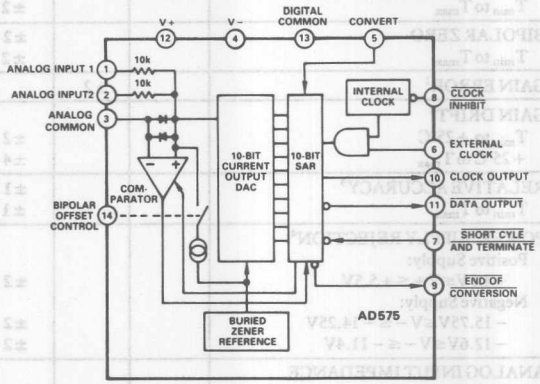
with Serial Output

AD575*

FEATURES

Complete Serial Output 10-Bit A/D Converter with Reference, Clock and Comparator
30μs Conversion
No Missing Codes Over Temperature
Operates on +5V and −12V to −15V Supplies
Low Cost Monolithic Construction
Internal or External Clock
Triggered or Continuous Conversions
Short Cycle Capability

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD575 is a complete 10-bit successive-approximation analog-to-digital converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register (SAR) and serial interface on a single chip. No additional components are required to perform a full-accuracy 10-bit conversion in 30μs.

The AD575 incorporates the most advanced integrated circuit design and processing technology available. The successive approximation function is implemented with I^2L (integrated injection logic). Laser trimming of the SiCr thin-film resistor ladder network at the wafer stage insures high accuracy, which is maintained with a temperature-compensated sub-surface zener reference.

Operating on supplies of +5V and −12V to −15V, the AD575 will accept full scale analog inputs of 0V to +10V, 0V to +20V, −5V to +5V or −10V to +10V. The rising edge of a positive pulse on the CONVERT line initiates the conversion cycle. Eleven pulses will appear at the CLOCK OUTPUT pin with data valid on the falling edges of the clock waveform. The data is presented serially beginning with the MSB which is valid on the falling edge of the second clock pulse. The part may be programmed to perform 8-bit conversions or short cycled to 2-, 4-, 6- or 8-bit word lengths. $\overline{EOC}$ indicates that conversion is complete. The AD575 may be synchronized to an external clock if desired.

The AD575 is available in two versions for the 0 to +70°C temperature range, the AD575J and AD575K; packaging is a 14-pin plstic DIP.

PRODUCT HIGHLIGHTS

1. The AD575 is a complete 10-bit A/D converter. No external active components or control signals are required to perform a conversion.
2. The serial output of the AD575 allows a wide range of microprocessor interfacing and data transmission possibilities.
3. The device offers true 10-bit relative accuracy and exhibits no missing codes over its entire operating temperature range.
4. The AD575 adapts to unipolar or bipolar analog inputs by grounding or opening a single pin.
5. Performance is guaranteed with +5V and −12V or −15V supplies.
6. The AD575 can be synchronized to an external clock.
7. Conversions can be initiated externally or internally.
8. The AD575 can be short-cycled to 8 bits by pin programming.
9. The Short Cycle and Terminate feature allows the user to program conversions of 2, 4, 6 or 8 bits.

***Protected by U.S. Patent Nos. 3,940,760; 4,400,689; and 4,400,690.**

AD575—SPECIFICATIONS (@ +25°C, V+ = +5V, V− = −12V or −15V, unless otherwise noted.)

	AD575J			AD575K			
	Min	Typ	Max	Min	Typ	Max	Units
RESOLUTION							
For Which No Missing Codes is Guaranteed	10			10			Bits
T_{min} to T_{max}	9			10			Bits
UNIPOLAR OFFSET			±2			±1	LSB
T_{min} to T_{max}			±2			±1	LSB
BIPOLAR ZERO			±2			±1	LSB
T_{min} to T_{max}			±2			±1	LSB
GAIN ERROR[1]		±2				±2	LSB
GAIN DRIFT[2]							
T_{min} to +25°C			±2			±1	LSB
+25°C to T_{max}			±4			±2	LSB
RELATIVE ACCURACY[3]			±1			±1/2	LSB
T_{min} to T_{max}			±1			±1/2	LSB
POWER SUPPLY REJECTION[4]							
Positive Supply:							
+4.5V≤V+≤+5.5V			±2			±1	LSB
Negative Supply:							
−15.75V≤V−≤−14.25V			±2			±1	LSB
−12.6V≤V−≤−11.4V			±2			±1	LSB
ANALOG INPUT IMPEDANCE							
Pin 1, Pin 2	6	10	14	6	10	14	kΩ
ANALOG INPUT RANGES							
Unipolar	0 to 10			0 to 10			V
	0 to 20			0 to 20			V
Bipolar	−5 to +5			−5 to +5			V
	−10 to +10			−10 to +10			V
OUTPUT CODING							
Unipolar	NEGATIVE TRUE BINARY			NEGATIVE TRUE BINARY			
Bipolar	NEGATIVE TRUE OFFSET BINARY			NEGATIVE TRUE OFFSET BINARY			
LOGIC OUTPUTS (T_{min} to T_{max})							
V_{OL} @ I_{SINK} = 3.2mA	0		0.4	0		0.4	V
V_{OH} @ I_{SOURCE} = 0.5mA	2.4		5.0	2.4		5.0	V
LOGIC INPUTS (T_{min} to T_{max})							
I_{INH} @ V_{IN} = 5V[5]			+50			+50	μA
I_{INL} @ V_{IN} = 0V[5]	−800			−800			μA
V_{INH}	2.0		5.5	2.0		5.5	V
V_{INL}	0		0.8	0		0.8	V
CONVERSION TIME (T_{min} to T_{max})							
Internal Clock	10	20	30	10	20	30	μs
External Clock	25			25			μs
POWER SUPPLY							
V+	+4.5		+5.5	+4.5		+5.5	V
V−	−11.4		−15.75	−11.4		−15.75	V
OPERATING CURRENT							
V+		15	25		15	25	mA
V−		9	15		9	15	mA

NOTES

[1]Gain Error is specified with a 15Ω resistor in series with the 10V input (Pins 1 and 2 tied together) or a 30Ω resistor in series with the 20V input (Pin 1 with Pin 2 tied to analog common). Gain Error is guaranteed trimmable to zero (see text).

[2]The gain drift is calculated from gain measurements at the extremes of the temperature range under consideration.

[3]Relative Accuracy, also referred to as Integral Linearity, is defined as the deviation of the code transition points from the ideal transfer points on a straight line from zero to full-scale. It is also a measure of the error which remains when offset and full scale errors are trimmed to zero in an application.

[4]Measured at full scale.

[5]These specifications apply to the CONV, XCL, and $\overline{SCAT}$ inputs. $\overline{CLI}$ is hardwired to DGND or $+V_S$ in most applications. Typically I_{INH} = +350μA and I_{INL} = 120μA for the $\overline{CLI}$ input.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common . . . . . 0 to +7V
V− to Digital Common . . . . . 0 to −16.5V
Analog Common to Digital Common . . . . . ±1V
Analog Inputs . . . . . (V−) −0.3V to +22V
Control Inputs . . . . . 0 to V+
Power Dissipation 800mW

NOTE
All pins must be kept more positive than (V−) −0.3V.

ORDERING GUIDE

Model	Package Option*	Temperature Range−°C	Relative Accuracy
AD575JN	N-14	0 to +70	±1LSB max
AD575KN	N-14	0 to +70	±1/2LSB max

*N = Plastic DIP. For outline information see Package Information section.

2

FUNCTIONAL DESCRIPTION

A block diagram of the AD575 is shown in Figure 1. A conversion is initiated by a positive pulse on the CONVERT line. $\overline{EOC}$ goes high within 150ns indicating that a conversion has started. The internal 10-bit current-output DAC is sequenced by the successive approximation register (SAR) from most significant bit to least significant bit to provide an output current which accurately balances the input signal current through the 10kΩ input resistor(s). The comparator determines whether the addition of each successively-weighted bit current causes the DAC current to be higher or lower than the input current. If the sum is less the bit is left on ($\overline{DO}$ set low). If the sum is more, the bit is turned off ($\overline{DO}$ set high). The result of each bit decision is passed to $\overline{DO}$ on the rising edge of CO.

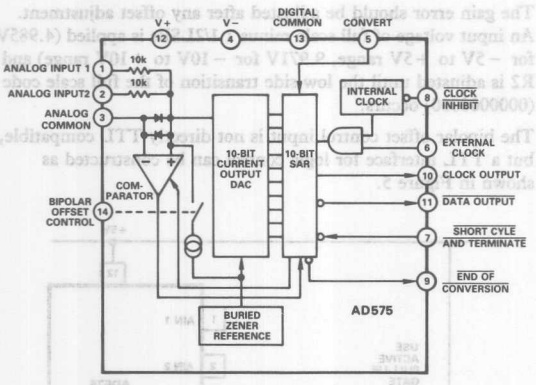


Figure 1. AD575 Functional Block Diagram

After all bits have been tested, the DAC output current will match the input signal current to within 0.05% (1/2LSB). $\overline{EOC}$ returns low after the final bit decision to indicate that the AD575 has been reset and is ready to perform a new conversion. The output data stream can be synchronized to an external clock using the XCL input and short cycled to any desired word length using the $\overline{SCAT}$ line.

The AD575 contains all the active components required to perform a complete A/D conversion. Thus, for many applications, all that is necessary is to connect the power supplies (+5V and −12V or −15V), and the analog input. The pinout is shown in Figure 2.

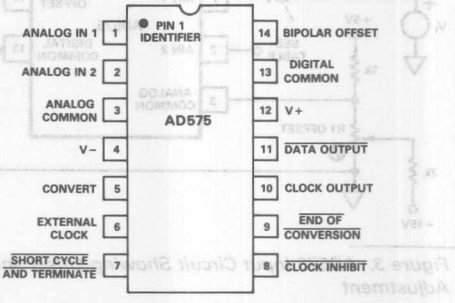


Figure 2. AD575 Pin Connections

ANALOG INPUT CONNECTIONS

The AD575 can be configured for unipolar or bipolar operation on 10V span or 20V span input signals. The appropriate input range is selected by connecting pins 2 and 14 according to the table of Figure 3.

The AD575's low offset and gain errors (shown in the Specifications) are adequate for most applications. For these cases, a fixed gain resistor (R2 in Figure 3) is the only external component, in addition to any power supply decoupling that may be required. Pins 3 and 13 should be connected directly together.

Figure 3 shows a trimming circuit that can be used to adjust the offset to zero, using the appropriate value of the R1 potentiometer as shown in the table. If gain trim is required, R2 should also be replaced by the appropriate potentiometer as shown in the table.

ANALOG INPUT RANGE	CONNECTIONS PIN 2	CONNECTIONS PIN 14	COMPONENTS R1 (OFFSET)	COMPONENTS R2 (GAIN)
0V TO +10V	PIN 1	PIN 13	10Ω	15Ω FIXED OR 50Ω POT
0V TO +20V	PIN 3	PIN 13	20Ω	30Ω FIXED OR 100Ω POT
−5V TO +5V	PIN 1	OPEN	10Ω	15Ω FIXED OR 50Ω POT
−10V TO +10V	PIN 3	OPEN	20Ω	30Ω FIXED OR 100Ω POT

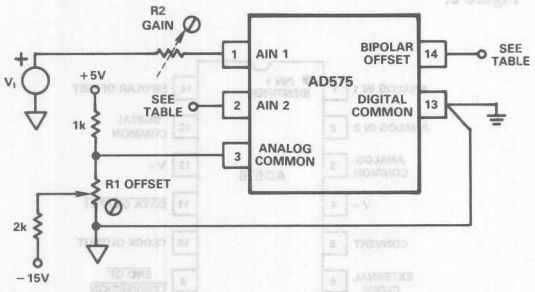


Figure 3. AD575 Input Circuit Showing Offset and Gain Adjustment

UNIPOLAR MODE OPERATION

In unipolar mode, the nominal location of the low side transition of the first code (1111111110) occurs at an input voltage of +1LSB (10mV for the 10V span, 20mV for the 20V span). The offset error of the AD575 can be trimmed out, if required, by applying an input voltage of +1LSB to the analog input and adjusting R1 until the low side transition of the first code occurs.

If the Gain Error needs to be trimmed, the gain resistor should be replaced with a potentiometer according to Figure 3. The nominal location of the low side transition of the full scale code (0000000000) in unipolar mode is full scale minus 1LSB (9.99V for 10V span, 19.98V for 20V span). Once the offset has been adjusted, the full scale range can be set by adjusting the gain potentiometer.

BIPOLAR CONNECTION

If the bipolar offset control (pin 14) is left open, the AD575 will accept bipolar input voltages with 0V as the nominal bipolar zero point. The input voltage corresponding to the low side transition of the mid-scale code (0111111111) is −1/2LSB (−5mV for 10V spans and −10mV for 20V spans). The nominal location of the code transitions are therefore offset by 1/2LSB as shown in Figure 4. This offset may be adjusted using the trim scheme shown in Figure 3 with a 1.2kΩ resistor in place of the 1kΩ resistor shown.

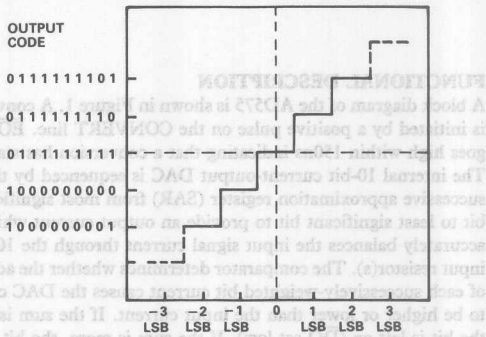


Figure 4. AD575 Transfer Characteristic (Bipolar Operation)

The gain error should be adjusted after any offset adjustment. An input voltage of full scale minus 1 1/2LSBs is applied (4.985V for −5V to +5V range, 9.971V for −10V to +10V range) and R2 is adjusted until the low-side transition of the full scale code (0000000000) occurs.

The bipolar offset control input is not directly TTL compatible, but a TTL interface for logic control can be constructed as shown in Figure 5.

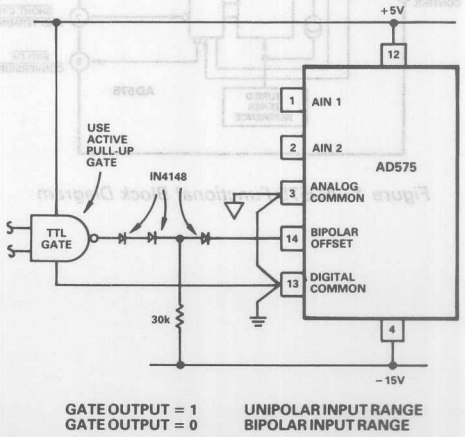


Figure 5. Bipolar Offset Controlled by Logic Gate

CONTROL AND TIMING OF THE AD575

The AD575 has a flexible control architecture which supports several operating modes. It can provide its own clock or it can be synchronized to an external clock. Conversions can be initiated externally, or the part can perform continuous conversions yielding a stream of output data. In addition, the AD575 can be short-cycled to any of several convenient data word lengths to tailor the output to the specific input requirements of the system. Figure 6 shows the control logic diagram of the AD575. The four inputs which control the operation of the AD575 are CONV (convert), $\overline{CLI}$ (clock inhibit), XCL (external clock), and $\overline{SCAT}$ (short cycle and terminate). Three outputs are provided: $\overline{DO}$ (Data Out), CO (Clock Out), and $\overline{EOC}$ (End of Conversion).

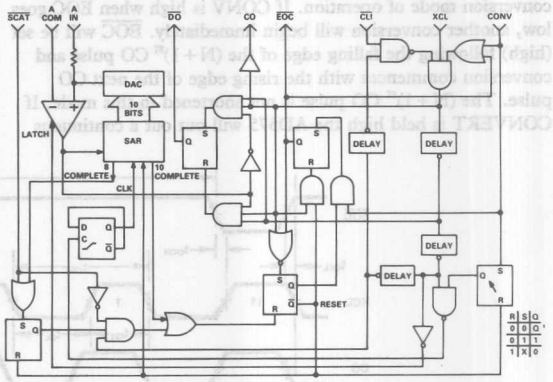


Figure 6. AD575 Control Logic Diagram

EXTERNALLY INITIATED CONVERSIONS

Figure 7 is the timing diagram which illustrates the operation of the AD575 with an externally applied convert signal. Conversions are initiated by a positive-going pulse applied to the CONV (convert) input. This pulse should be at least 250ns wide and should return low before $\overline{EOC}$ returns low to prevent the initiation of a second conversion. If the internal clock is used, the clock will start on the rising edge of the convert start pulse. If an external clock is used, the falling edge of the clock must occur no earlier than 900ns following the rising edge of the convert command.

INTERNAL CLOCK MODE

The AD575 can be configured for internal clock operation by tying $\overline{CLI}$ and XCL to +5V. CO (clock output) provides the necessary synchronizing information in this mode. Data is transferred to $\overline{DO}$ on the rising clock edge and is stable on the falling edge. The duty cycle of the CO waveform in this mode will be in the range of 30% to 70%.

EXTERNAL CLOCK MODE

When $\overline{CLI}$ is connected to digital common, an external clock can be applied to XCL. The external clock should have a maximum frequency of 450kHz with a minimum of 900ns in the high or low phase. Arbitrarily slow clocks may be used as long as these minimum high and low periods are observed. Conversion time will increase as clock frequency decreases. Each data bit will be stable within 150ns of the rising edge of the associated external clock pulse and will remain stable until the rising edge of the subsequent clock pulse. Data is guaranteed to be stable on the falling edge of the clock pulse.

The state of the $\overline{DO}$ output during the first clock period is undefined but it is stable until the rising edge of the second clock period. The MSB appears at $\overline{DO}$ during the second clock period. The subsequent data bits are then clocked out until the Nth bit or LSB is clocked out on the $(N+1)^{th}$ clock pulse. $\overline{EOC}$ returns low within 150ns of the rising edge of this final clock pulse. In internal clock mode, the output clock pulse associated with the LSB is shorter than the others but the LSB is guaranteed to be stable on the falling edge of this pulse. The LSB will remain stable until a new conversion is initiated. The value of N will be 10 unless the conversion has been short cycled (see "short cycle and terminate" text).

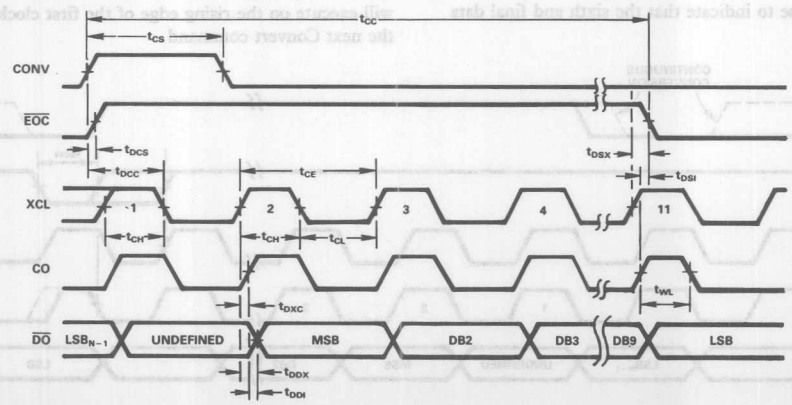


Figure 7. Externally Initiated Conversions

CONTINUOUS CONVERSIONS

Figure 8 is the timing diagram associated with the continuous conversion mode of operation. If CONV is high when $\overline{EOC}$ goes low, another conversion will begin immediately. $\overline{EOC}$ will be set (high) following the falling edge of the $(N+1)^{st}$ CO pulse and conversion commences with the rising edge of the next CO pulse. The $(N+1)^{st}$ CO pulse is not shortened in this mode. If CONVERT is held high the AD575 will put out a continuous stream of conversions, punctuated by $\overline{EOC}$ which will mark the last clock pulse of a conversion. $\overline{EOC}$ will remain low until the falling edge of CO, the output clock, in this mode. Therefore, the rising edge of $\overline{EOC}$ may be used to signal that conversion is complete and that data is transferred. This sequence is useful for initiating parallel dumps from a serially loaded shift register.

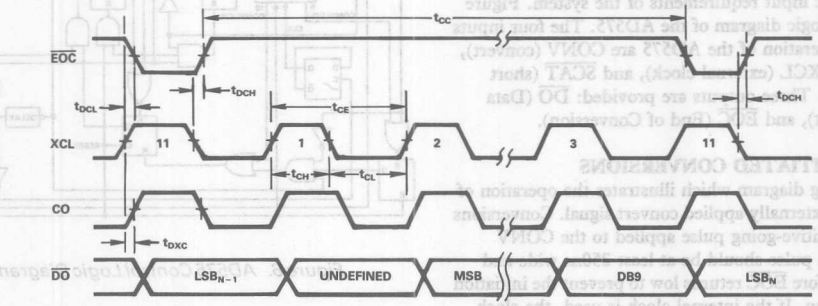


Figure 8. Continuous Conversion Mode (CONV. Held High)

SHORT CYCLE AND TERMINATE

For normal 10-bit operation, the Short Cycle and Terminate ($\overline{SCAT}$) line should be tied high. If 8-bit conversions are required, $\overline{SCAT}$ should be tied low. In this mode, $\overline{EOC}$ will go low after the rising edge of the ninth clock pulse to indicate that the eighth and final data bit is valid. This mode is useful when parallel loads to 8-bit data buses are desired since it avoids the complication of suppressing the 9th and 10th data bits.

Conversions of 2, 4, 6 or 8 bits can be performed by pulling $\overline{SCAT}$ low during the negative clock phase prior to the positive clock associated with the desired LSB. Figure 9 illustrates the timing associated with this mode of operation. For example, to terminate the conversion after six data bits, $\overline{SCAT}$ should be driven low during the negative clock phase following the sixth clock pulse. $\overline{EOC}$ will then go low following the rising edge of the seventh clock pulse to indicate that the sixth and final data bit is valid.

This terminate feature can also be used to program conversions of 1, 3, 5, 7 or 9 bits. However, the conversion immediately following a conversion of an odd number of data bits will be spurious. All subsequent conversions will be normal until the conversion following another odd data word length conversion.

The negative edge of the $\overline{SCAT}$ signal should always occur during the negative phase of a clock cycle and it should be held low for a minimum of 900ns. $\overline{SCAT}$ may be held low into the next conversion but it must be restored high at least one clock cycle prior to being used to terminate a conversion. If $\overline{SCAT}$ is not restored high prior to the eighth clock pulse, $\overline{EOC}$ will go low and an 8-bit short cycle will occur. Care should be taken not to pulse $\overline{SCAT}$ from high to low between conversions (when $\overline{EOC}$ is low). This would initiate a terminate sequence which will execute on the rising edge of the first clock pulse following the next Convert command.

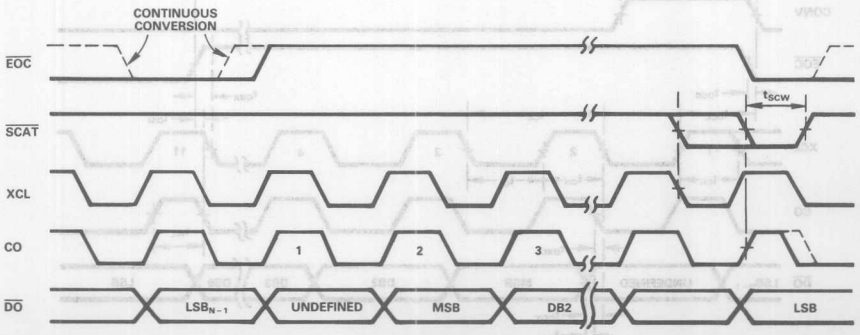


Figure 9. Short Cycle and Terminate Operation

Parameter	Symbol	Min	Typ	Max	Units
EXTERNALLY-INITIATED CONVERSIONS					
Convert Pulse Width	t_{CS}	300			ns
Convert to $\overline{EOC}$ Delay	t_{DCS}			150	ns
CO LSB Clock Pulse Width	t_{WL}	400			ns
XCL to $\overline{EOC}$ Reset	t_{DSX}	50		150	ns
↑ CO to ↓ $\overline{EOC}$ Reset Delay	t_{DSI}	20		150	ns
CONTINUOUS CONVERSIONS					
↑ XCL to ↓ $\overline{EOC}$ Reset Delay	t_{DCL}	50		150	ns
↓ XCL to ↑ $\overline{EOC}$ Delay	t_{DCH}	50		1000	ns
INTERNAL CLOCK TIMING					
Conversion Time	t_{CC}	10	20	30	µs
CO to $\overline{DO}$ Output Delay	t_{DDI}	−100		+100	ns
EXTERNAL CLOCK TIMING					
Conversion Time	t_{CC}	25			µs
↑ XCL to $\overline{DO}$ Output	t_{DDX}	30		150	ns
XCL to CO Output	t_{DXC}	30		160	ns
↑ Convert to ↓ XCL Set-Up Time	t_{DCC}	900			ns
XCL Period	t_{CE}	2.2			µs
XCL High	t_{CH}	900			ns
XCL Low	t_{CL}	900			ns
SHORT CYCLE TIMING					
$\overline{SCAT}$ Pulse Width	t_{SCW}	900			ns

Table I. AD575 Timing Specifications

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD575

Many data acquisition systems for digitizing rapidly changing signals require a sample-hold amplifier (SHA) in front of the A/D converter. A SHA can be used to accurately define the exact point in time at which the signal is sampled. A SHA can also serve as a high input-impedance buffer for the AD575.

Figure 10 shows the AD575 connected to the AD585 monolithic SHA. In this configuration, the AD585 will acquire a 10V signal in less than 2µs and droop less than 1mV/ms using the on-chip hold capacitor.

$\overline{EOC}$ goes high after the conversion is initiated to indicate that a conversion is underway. In Figure 10 it is also used to put the AD585 into the hold mode while the AD575 begins its conversion cycle. (The AD585 output settles to final value well in advance of the first comparator decision within the AD575.) $\overline{EOC}$ goes low when the conversion is complete placing the AD585 back in the sample mode.

Configured as shown in Figure 10, the next conversion can be initiated after a 2µs delay to allow for signal acquisition by the AD585.

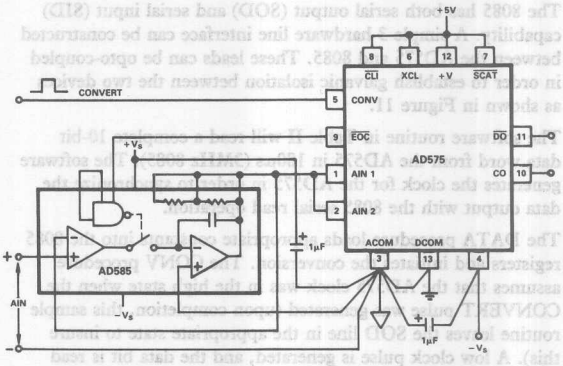


Figure 10. AD575 to AD585 Sample and Hold Interface

SUPPLY DECOUPLING AND LAYOUT

For proper operation, the AD575's power supplies should be free from high-frequency noise. The stability of the transfer function is especially sensitive to noise on the V− supply. Noise on the V+ supply can also propagate to the digital outputs.

If decoupling is required, tantalum capacitors are suggested. Best results will be obtained if the capacitors are connected directly to the appropriate pins of the AD575. Decoupling capacitors for V− should be connected between pin 4 and Analog Common (pin 3). Decoupling capacitors for V+ should be connected between pin 12 and Digital Common (pin 13).

Good circuit layout practice suggests that the AD575 and its associated analog input circuitry be kept separate from system logic circuitry to avoid unwanted interactions.

GROUNDING CONSIDERATIONS

The AD575 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200mV of common-mode voltage between the two commons. The absolute maximum voltage rating between the two commons is ±1V. A parallel pair of back-to-back protection diodes should be connected between the commons if they are not connected locally.

In normal operation, the Analog Common terminal may generate transient currents of up to 2mA during a conversion. In addition, a static current of about 2mA will flow into Analog Common in the unipolar mode after a conversion is complete. The Analog Common current will be modulated by the variations in input signal.

AD575 TO 8085 INTERFACE

The 8085 has both serial output (SOD) and serial input (SID) capability. A simple 3 hardware line interface can be constructed between the AD575 and 8085. These leads can be opto-coupled in order to establish galvanic isolation between the two devices as shown in Figure 11.

The software routine in Table II will read a complete 10-bit data word from the AD575 in 180μs (3MHz 8085). The software generates the clock for the AD575 in order to synchronize the data output with the 8085 serial read operation.

The DATA procedure loads appropriate constants into the 8085 registers and initiates the conversion. The CONV procedure assumes that the AD575 clock was in the high state when the CONVERT pulse was generated (upon completion, this sample routine leaves the SOD line in the appropriate state to insure this). A low clock pulse is generated, and the data bit is read into the MSB of the accumulator. The data bit is then shifted into the LSB of the temporary register (L), the clock is set high, and the procedure is repeated.

After the loop has executed three times, a logical AND is performed to set the first bit (the undefined bit) to zero, and the result is placed into the high byte (H) register. The loop counter is then reset, and the CONV procedure is executed 8 more times. Upon completion of the sample routine, 10 bits of right-justified data will reside in the HL register pair.

Note that the opto-isolators invert the clock and data lines. If these are not used (no inversion present), the constants in the D and E registers should be swapped, a CMA instruction should be inserted after the RIM instruction, and an inverter should be connected between the address decoder and the CONVERT pin. Also, the results of the first pass through the routine should be ignored following power up and reset cycles to insure that the AD575 has been reset.

LABEL	MNEMONIC	OPERAND	COMMENT
DATA	MVI	B,03	Set inner loop counter to 3
	MVI	C,02	Set outer loop counter to 2
	MVI	D,CO	Setup register D for clock low
	MVI	E,40	Setup register E for clock high
	MVI	H,10	AD575 address location
	MVI	L,00	Clear temp register
	MOV	M,B	Generate CONVERT pulse
CONV	MOV	A,D	Setup ACC for clock low
	SIM		Output clock low
	RIM		Read AD575 data bit into ACC
	RAL		Shift data bit into Carry
	MOV	A,L	Move temp to ACC
	RAL		Shift data bit from Carry to ACC
	MOV	L,A	Replace temp
	MOV	A,E	Setup ACC for clock high
	SIM		Output clock high
	DCR	B	Decrement inner loop counter
	JNZ	CONV	Repeat CONV until done
	DCR	C	Decrement outer loop counter
	JZ	DONE	Skip to DONE on 2nd pass
	MOV	A,L	Move temp to ACC
	ANI	03	Mask undefined bit
	MOV	H,A	Store temp in H register
	MVI	B,OB	Set inner loop counter to 8
	JMP	CONV	Repeat CONV for 8 LSBs
DONE	RET		10 bits of right-justified data now reside in HL; return

Table II. Sample Assembly Code for AD575 to 8085 Isolated Interface

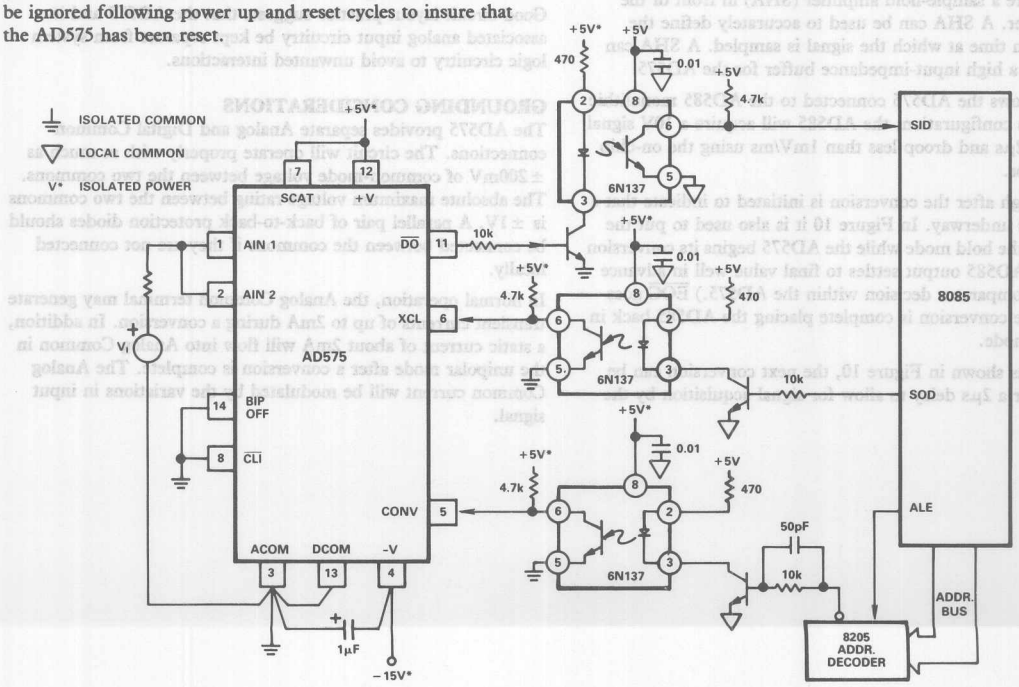


Figure 11. AD575 to 8085 Isolated Interface

Very Fast, Complete 10- or 12-Bit A/D Converters

AD578/AD579

FEATURES

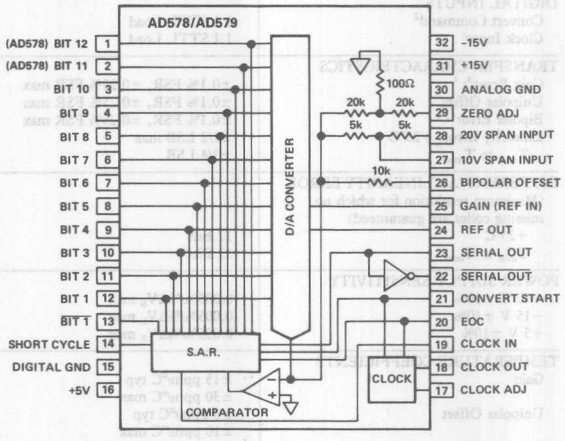
Performance

- Complete 12-Bit A/D Converter with Reference and Clock
- Fast Conversion: 3 μs (max)
- Buried Zener Reference for Long Term Stability and Low Gain T.C.: ±30 ppm/°C max (AD578)
  ±40 ppm/°C max (AD579)
- Max Nonlinearity: <±0.012%
- No Missing Codes Over Temperature
- Low Power: 555 mW (AD578); 775 mW (AD579)
- Available to MIL-STD-883

Versatility

- Positive-True Parallel or Serial Logic Outputs
- Short Cycle Capability
- Precision +10 V Reference for External Applications
- Adjustable Internal Clock
- "Z" Models for ±12 V Supplies

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD578 and AD579 are high speed 12-bit and 10-bit successive approximation analog-to-digital converters that include internal clock, reference, and comparator. Their hybrid design utilizes MSI digital and linear ICs in conjunction with a 12-bit or 10-bit monolithic, monotonic DAC to provide superior performance and versatility with IC size, price, and reliability.

Important performance characteristics of the AD578 include ±1/2 LSB_{12} linearity error maximum at +25°C, maximum gain tempco of ±30 ppm/°C, and maximum conversion time of 3 μs at a typical power dissipation of 555 mW. The 10-bit AD579 provides ±1/2 LSB_{10} maximum linearity error at 1.8 μs maximum, and 775 mW typical P_D.

Both the AD578 and AD579 include scaling resistors that provide analog input signal ranges of ±5 V, ±10 V, and 0 to +10 V. Both are contained in 32-pin ceramic side-brazed DIP packages, and are available with MIL-STD-883 Class B processing.

PRODUCT HIGHLIGHTS

1. Both are complete analog-to-digital converters. No external components are required to perform a conversion.
2. The fast conversion rates—3 μs for the AD578, and 1.8 μs for the AD579—make them ideal candidates for high speed data acquisition systems requiring high throughput.
3. The internal buried Zener reference is laser trimmed to high initial accuracy and low T.C. and is available externally.
4. Precision thin film scaling resistors on the DAC provide for excellent thermal tracking.
5. Short cycle and external clock capabilities are provided for applications requiring faster conversion speeds and/or lower resolution.

AD578/AD579—SPECIFICATIONS (typical @ +25°C, ±15 V and +5 V unless otherwise noted)

Model	AD578J	AD578K	AD578L	AD578SD[1]	AD578TD[1]
RESOLUTION	12 Bits	*	*	*	*
ANALOG INPUTS					
Voltage Ranges					
Bipolar	±5.0 V, ±10 V	*	*	*	*
Unipolar	0 to +10 V, 0 to +20 V	*	*	*	*
Input Impedance					
0 to +10 V, ±5 V	5 kΩ	*	*	*	*
±10 V, 0 to +20 V	10 kΩ	*	*	*	*
DIGITAL INPUTS					
Convert Command[2]	1 LSTTL Load	*	*	*	*
Clock Input	1 LSTTL Load	*	*	*	*
TRANSFER CHARACTERISTICS					
Gain Error[3, 4]	±0.1% FSR, ±0.25% FSR max	*	*	*	*
Unipolar Offset[4]	±0.1% FSR, ±0.25% FSR max	*	*	*	*
Bipolar Error[4, 5]	±0.1% FSR, ±0.25% FSR max	*	*	*	*
Linearity Error, +25°C	±1/2 LSB max	*	*	*	*
T_{min} to T_{max}	±3/4 LSB	*	*	±3/4 LSB max	±3/4 LSB max
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)					
+25°C	12 Bits	*	*	*	*
T_{min} to T_{max}	12 Bits	*	*	*	*
POWER SUPPLY SENSITIVITY					
+15 V ±10%	0.005%/%ΔV_S max	*	*	*	*
−15 V ±10%	0.005%/%ΔV_S max	*	*	*	*
+5 V ±10%	0.005%/%ΔV_S max	*	*	*	*
TEMPERATURE COEFFICIENTS					
Gain	±15 ppm/°C typ	*	*	*	*
	±30 ppm/°C max	*	*	±50 ppm/°C max	±30 ppm/°C max
Unipolar Offset	±3 ppm/°C typ	*	*	*	*
	±10 ppm/°C max	*	*	±15 ppm/°C max	±10 ppm/°C max
Bipolar Offset	±8 ppm/°C typ	*	*	*	*
	±20 ppm/°C max	*	*	±25 ppm/°C max	±20 ppm/°C max
Differential Linearity	±2 ppm/°C typ	*	*	*	*
CONVERSION TIME[6, 7, 8] (max)	6.0 µs	4.5 µs	3 µs	6.0 µs	4.5 µs
PARALLEL OUTPUTS					
Unipolar Code	Binary	*	*	*	*
Bipolar Code	Offset Binary/Twos Complement	*	*	*	*
Output Drive	2 LSTTL Loads	*	*	*	*
SERIAL OUTPUTS (NRZ FORMAT)					
Unipolar Code	Binary/Complementary Binary	*	*	*	*
Bipolar Code	Offset Binary/Comp. Offset Binary	*	*	*	*
Output Drive	2 LSTTL Loads	*	*	*	*
END OF CONVERSION (EOC)	Logic "1" During Conversion	*	*	*	*
Output Drive	8 LSTTL Loads	*	*	*	*
INTERNAL CLOCK[8]					
Output Drive	2 LSTTL Loads	*	*	*	*
INTERNAL REFERENCE					
Voltage	10.000 ±100 mV	*	*	*	*
Drift	±12 ppm/°C, ±20 ppm/°C max	*	*	*	*
External Current	±1 mA max	*	*	*	*
POWER SUPPLY REQUIREMENTS[9]					
Range for Rated Accuracy	4.75 to 5.25 and ±13.5 to ±16.5	*	*	*	*
Supply Current +15 V	5 mA typ, 8 mA max	*	*	*	*
−15 V	22 mA typ, 35 mA max	*	*	*	*
+5 V	30 mA typ, 40 mA max	*	*	*	*
Power Dissipation	555 mW typ	*	*	*	*
TEMPERATURE RANGE					
Operating	0 to +70°C	*	*	−55°C to +125°C	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*	*

NOTES
[1]Available to MIL-STD-883, Level B. See ADI Military Products Databook for detail specifications.
[2]Positive pulse 200 ns wide (min) leading edge (0 to 1) resets outputs. Trailing edge initiates conversion.
[3]With 50 Ω, 1% fixed resistor in place of gain adjust potentiometer.
[4]Adjustable to zero.
[5]With 50 Ω, 1% resistor between Ref Out and Bipolar Offset (Pins 24 & 26).
[6]Conversion time is defined as the time between the falling edge of convert start and the falling edge of the EOC.
[7]Each grade is specified at the conversion speed shown.
[8]Externally adjustable by a resistor or capacitor (see Figure 6).
[9]For "Z" models order AD578ZJ, ZK, ZL (±11.6 V to ±16.5 V).

*Specifications same as AD578J.
Specifications subject to change without notice.

Model	AD579JN	AD579KN	AD579TD[1]
RESOLUTION	10 Bits	*	*
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±5.0 V, ±10 V	*	*
Unipolar	0 to +10 V, 0 to +20 V	*	*
Input Impedance			
0 to +10 V, ±5 V	5 kΩ (±20%)	*	*
±10 V, 0 to +20 V	10 kΩ (±20%)	*	*
DIGITAL INPUTS			
Convert Command[2]	1 LSTTL Load	*	*
Clock Input	1 LSTTL Load	*	*
TRANSFER CHARACTERISTICS			
Gain Error[3, 4]	±0.1% FSR (±0.25% FSR max)	*	*
Unipolar Offset[3]	±0.1% FSR (±0.25% FSR max)	*	*
Bipolar Error[3, 4]	±0.1% FSR (±0.25% FSR max)	*	*
Linearity Error, +25°C	±1/2 LSB max	*	*
T_{min} to T_{max}	±3/4 LSB	*	*
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)			
+25°C	10 Bits	*	*
T_{min} to T_{max}	10 Bits	*	*
POWER SUPPLY SENSITIVITY			
+15 V ±10%	0.005%/%ΔV_S max	*	*
−15 V ±10%	0.005%/%ΔV_S max	*	*
+5 V ±10%	0.001%/%ΔV_S max	*	*
"Z" Versions			
+12 V ±5%	0.007%/%ΔV_S max	*	*
−12 V ±5%	0.007%/%ΔV_S max	*	*
TEMPERATURE COEFFICIENTS			
Gain	±25 ppm/°C typ	*	*
	±40 ppm/°C max	*	*
Unipolar Offset	±5 ppm/°C typ	*	*
	±15 ppm/°C max	*	*
Bipolar Offset	±8 ppm/°C typ	*	*
	±20 ppm/°C max	*	*
Differential Linearity	±2 ppm/°C typ	*	*
CONVERSION TIME[5, 6] (max)	2.2 µs	1.8 µs	**
Conversion Time T_{min} to T_{max}	2.4 µs	2.0 µs	**
PARALLEL OUTPUTS			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary/Twos Complement	*	*
Output Drive	2 LSTTL Loads	*	*
SERIAL OUTPUTS (NRZ FORMAT)			
Unipolar Code	Binary/Complementary Binary	*	*
Bipolar Code	Offset Binary/Comp. Offset Binary	*	*
Output Drive	2 LSTTL Loads	*	*
END OF CONVERSION (EOC)	Logic "1" During Conversion	*	*
Output Drive	8 LSTTL Loads	*	*
INTERNAL CLOCK[7]			
Output Drive	2 LSTTL Loads	*	*
INTERNAL REFERENCE			
Voltage	10.000 ±10 mV typ	*	*
Temperature Coefficient	15 ppm/°C	*	*
External Current	±1 mA max	*	*
POWER SUPPLY REQUIREMENTS			
Range for Rated Accuracy	4.75 to 5.25 and ±13.5 to ±16.5	*	*
Z Models[8]	4.75 to 5.25 and ±11.4 to ±16.5	*	*
Supply Current +15 V	5 mA typ, 8 mA max	*	*
−15 V	22 mA typ, 35 mA max	*	*
+5 V	100 mA typ, 150 mA max	*	*
Power Dissipation	775 mW typ	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*

NOTES
[1]Available to MIL-STD-883, Level B. See ADI Military Products Databook for detail specifications.
[2]Positive pulse 200 ns wide (min) leading edge (0 to 1) resets outputs. Trailing edge initiates conversion.
[3]With 50 Ω, 1% fixed resistor in place of gain adjust potentiometer.
[4]Adjustable to zero.
[5]With 50 Ω, 1% resistor between Ref Out and Bipolar Offset (Pins 24 & 26).
[6]Conversion time is defined as the time between the falling edge of convert start and the falling edge of the EOC.
[7]Each grade is specified at the conversion speed shown. See Figure 7 for appropriate connections.
[8]Externally adjustable by a resistor or capacitor.
[9]For "Z" models order AD579ZJN, AD579ZKN or AD579ZTD.
*Specifications same as AD579JN.
**Specifications same as AD579KN.

Specifications subject to change without notice.

ORDERING GUIDE[1]

Model	Resolution	Conversion Speed	Temperature Range	Package Option[2]
AD578JN (JD)	12 Bits	6.0 µs	0°C to +70°C	DH-32B
AD578KN (KD)	12 Bits	4.5 µs	0°C to +70°C	DH-32B
AD578LN (LD)	12 Bits	3.0 µs	0°C to +70°C	DH-32B
AD578SD	12 Bits	6.0 µs	−55°C to +125°C	DH-32B
AD578TD	12 Bits	4.5 µs	−55°C to +125°C	DH-32B
AD578SD/883B	12 Bits	6.0 µs	−55°C to +125°C	DH-32B
AD578TD/883B	12 Bits	4.5 µs	−55°C to +125°C	DH-32B
AD579JN	10 Bits	2.2 µs	0°C to +70°C	DH-32B
AD579KN	10 Bits	1.8 µs	0°C to +70°C	DH-32B
AD579TD	10 Bits	1.8 µs	−55°C to +125°C	DH-32B
AD579TD/883B	10 Bits	1.8 µs	−55°C to +125°C	DH-32B

NOTES
[1]For ±12 V operation "Z" Version, order AD578ZTD
[2]For outline information see Package Information section.

THEORY OF OPERATION

The AD578 is a complete pretrimmed 12-bit A/D converter which requires no external components to provide the successive-approximation analog-to-digital conversion function. A block diagram of the AD578 is shown in Figure 1.

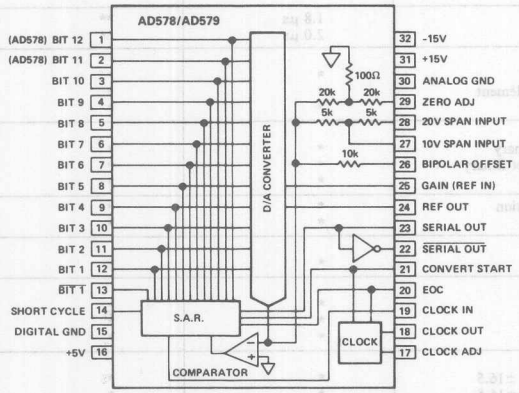
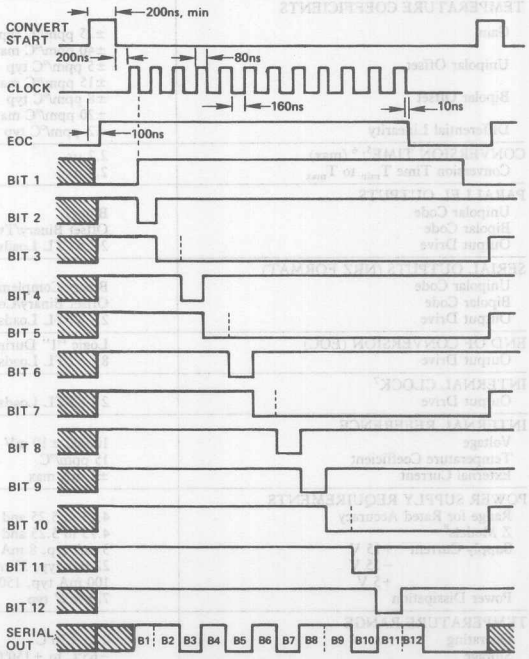


Figure 1. AD578/AD579 Functional Block Diagram and Pinout

When the control section is commanded to initiate a conversion it enables the clock and resets the successive-approximation register (SAR). The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section. The control section disables the clock and brings the output status flag low. The data bits are valid on the falling edge of the clock pulse starting with t_1 and ending with t_{12} (Figure 2), and accurately represent the input signal to within ±1/2 LSB.



CLOCK
INTERNAL: CONNECT CLOCK OUT (18) TO CLOCK IN (19)
EXTERNAL: CONNECT EXTERNAL CLOCK TO CLOCK IN (19)
CLOCK SHOULD BE AT LEAST 30% DUTY CYCLE WITH MINIMUM PERIOD, T_{MIN} OF 100ns.

NOTE
[1]THE RISING EDGE OF CONVERT START PULSE RESETS THE MSB TO ZERO, AND THE LSBs TO ONE. THE TRAILING EDGE INITIATES CONVERSION.

Figure 2a. AD578 3 µs Timing Diagram

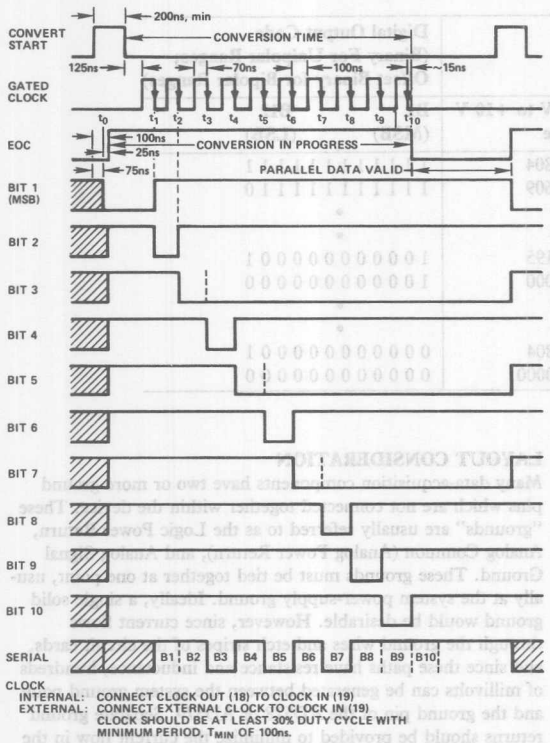


Figure 2b. AD579 Timing Diagram

The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ±1.0%, it is buffered and can supply up to 1.0 mA to an external load in addition to the current required to drive the reference input resistor (0.5 mA) and bipolar offset resistor (1 mA). The thin-film application resistors are trimmed to match the full scale output current of the DAC. There are two 5 kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10 kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation.

UNIPOLAR CALIBRATION

The AD578/AD579 is intended to have a nominal 1/2 LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2 LSB.

If Pin 26 is connected to Pin 30, the unit will behave in this manner, within specifications. Refer to Table I, Table II, and Figure 3 for further clarification. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±25 mV of offset trim range.

The full scale trim is done by applying a signal 1 1/2 LSB below the nominal full scale. Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).

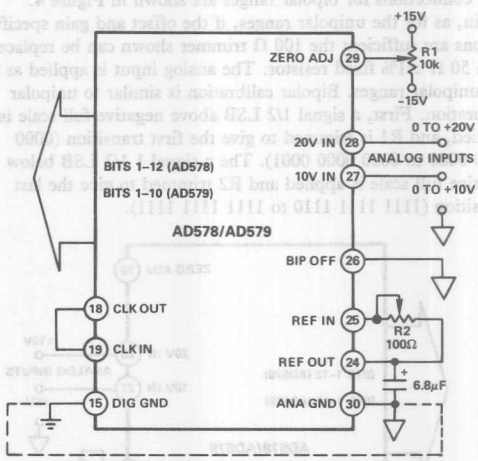


Figure 3. Unipolar Input Connections

Table I. AD578 Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

Analog Input–Volts (Center of Quantization Interval)				Digital Output Code (Binary For Unipolar Ranges; Offset Binary for Bipolar Ranges)
0 to +10 V Range	0 to +20 V Range	−5 V to +5 V Range	−10 V to +10 V Range	B1 (MSB) B12 (LSB)
+9.9976	+19.9951	+4.9976	+9.9951	1 1 1 1 1 1 1 1 1 1 1 1
+9.9952	+19.9902	+4.9952	+9.9902	1 1 1 1 1 1 1 1 1 1 1 0
•	•	•	•	•
•	•	•	•	•
+5.0024	+10.0049	+0.0024	+0.0049	1 0 0 0 0 0 0 0 0 0 0 1
+5.0000	+10.0000	+0.0000	+0.0000	1 0 0 0 0 0 0 0 0 0 0 0
•	•	•	•	•
•	•	•	•	•
+0.0024	+0.0051	−4.9976	−9.9951	0 0 0 0 0 0 0 0 0 0 0 1
+0.0000	+0.0000	−5.0000	−10.0000	0 0 0 0 0 0 0 0 0 0 0 0

Table II. AD579 Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

Analog Input–Volts (Center of Quantization Interval)				Digital Output Code (Binary For Unipolar Ranges; Offset Binary for Bipolar Ranges)
0 to +10 V Range	0 to +20 V Range	−5 V to +5 V Range	−10 V to +10 V Range	B1 (MSB) B12 (LSB)
+9.9902	+19.9804	+4.9902	+9.9804	1 1 1 1 1 1 1 1 1 1 1 1
+9.9804	+19.9609	+4.9804	+9.9609	1 1 1 1 1 1 1 1 1 1 1 0
•	•	•	•	•
•	•	•	•	•
+5.0097	+10.0195	+0.0097	+0.0195	1 0 0 0 0 0 0 0 0 0 0 1
+5.0000	+10.0000	+0.0000	+0.0000	1 0 0 0 0 0 0 0 0 0 0 0
•	•	•	•	•
•	•	•	•	•
+0.0097	+0.0195	−4.9902	−9.9804	0 0 0 0 0 0 0 0 0 0 0 1
+0.0000	+0.0000	−5.0000	−10.0000	0 0 0 0 0 0 0 0 0 0 0 0

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 4. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient the 100 Ω trimmer shown can be replaced by a 50 Ω ±1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal 1/2 LSB above negative full scale is applied, and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). The a signal 1 1/2 LSB below positive full scale is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

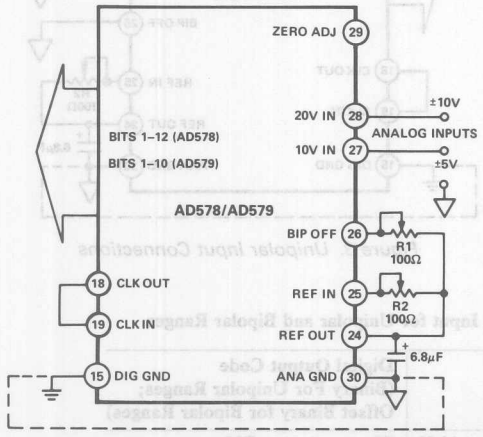


Figure 4. Bipolar Input Connections

LAYOUT CONSIDERATION

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD578 or AD579. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

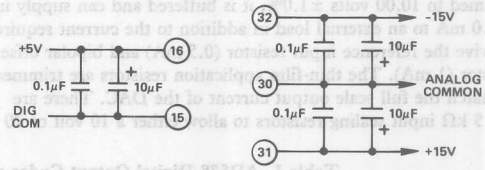


Figure 5. Basic Bypassing Practice

Each of the AD578 or AD579 supply terminals should be capacitively decoupled as close to the ADC as possible. A large value capacitor such as 10 μF in parallel with a 0.1 μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Digital GND pin.

To minimize noise the reference output (Pin 24) should be decoupled by a 6.8 μF capacitor to Pin 30.

CLOCK RATE CONTROL

The internal clock is preset to a nominal conversion time of 5.6 μs (AD578) or 4.8 μs (AD579). It can be adjusted for either faster or slower conversion rates. For faster conversions connect the appropriate 1% resistor between Pins 17 and 18, and short Pin 18 to Pin 19. See Figure 6 or 7.

For slower conversions (AD578 only) connect a capacitor between Pins 15 and 17.

NOTE: No-Missing-Code operation is not guaranteed when operating in this mode if a particular grade's conversion speed specification is exceeded.

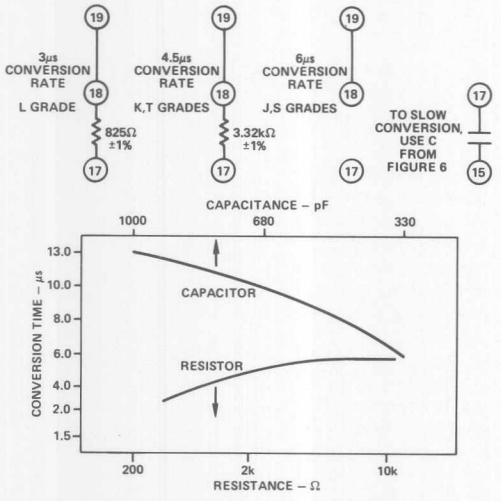


Figure 6. AD578 Conversion Times vs. R or C Values

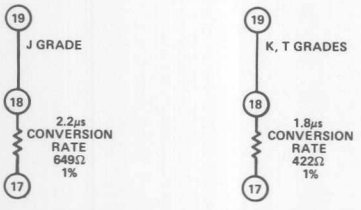


Figure 7. AD579 Clock Rate Control Connection

Short Cycle Input—A short cycle input, Pin 14, permits the timing cycle to be terminated after any number of desired bits has been converted, allowing shorter conversion times in applications not requiring the full 10-bit (AD579) or 12-bit (AD578) resolution. Short cycle pin connections and associated conversion times are summarized in Tables III and IV.

Table III. AD578 Short Cycle Connections

Resolution (Bits)	12	10	8
Connect Pin 14 to Pin	16	2	4
Conversion Speed (μs)	3	2.5	2

Table IV. AD579 Short Cycle Connections

Resolution (Bits)	10	8
Connect Pin 14 to Pin	2	4
Conversion Speed (μs)	1.8	1.5

External Clock—An external clock may be connected directly to the clock input, Pin 19. When operating in this mode, the convert start should be held high for a minimum of one clock period in order to reset the SAR and synchronize the conversion cycle. A positive going pulse width of 100 to 200 nanoseconds will provide a continuous string of conversions that start on the first rising edge of the external clock after the EOC output has gone low.

External Buffer Amplifier—In applications where the AD578 is to be driven from high impedance sources or directly from an analog multiplexer a fast slewing, wideband op amp like the AD711 should be used.

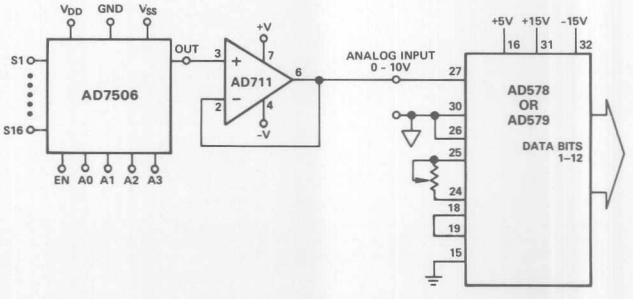
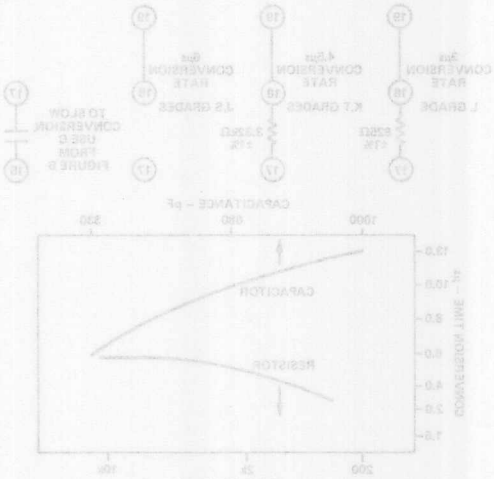


Figure 8. Input Buffer


CAPACITANCE – pF
RESISTANCE – Ω
CAPACITOR
RESISTOR
CONVERSION TIME – µs

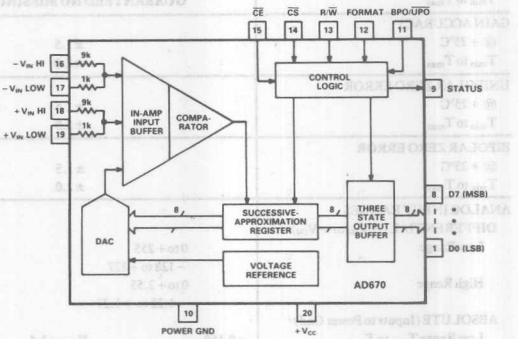
ANALOG INPUT
0 – 10V
ADS78
OR
ADS79
DATA BITS
ADJ711
ADS78B

Low Cost Signal Conditioning 8-Bit ADC

AD670

FEATURES

- **Complete 8-Bit Signal Conditioning A/D Converter Including Instrumentation Amp and Reference**
- **Microprocessor Bus Interface**
- **10μs Conversion Speed**
- **Flexible Input Stage: Instrumentation Amp Front End Provides Differential Inputs and High Common-Mode Rejection**
- **No User Trims Required**
- **No Missing Codes Over Temperature**
- **Single +5V Supply Operation**
- **Convenient Input Ranges**
- **20-Pin DIP or Surface-Mount Package**
- **Low Cost Monolithic Construction**
- **MIL-STD-883B Compliant Versions Available**



GENERAL DESCRIPTION

The AD670 is a complete 8-bit signal conditioning analog-to-digital converter. It consists of an instrumentation amplifier front end along with a DAC, comparator, successive approximation register (SAR), precision voltage reference, and a three-state output buffer on a single monolithic chip. No external components or user trims are required to interface, with full accuracy, an analog system to an 8-bit data bus. The AD670 will operate on the +5V system supply. The input stage provides differential inputs with excellent common-mode rejection and allows direct interface to a variety of transducers.

The device is configured with input scaling resistors to permit two input ranges: 0 to 255mV (1mV/LSB) and 0 to 2.55V (10mV/LSB). The AD670 can be configured for both unipolar and bipolar inputs over these ranges. The differential inputs and common-mode rejection of this front end are useful in applications such as conversion of transducer signals superimposed on common-mode voltages.

The AD670 incorporates advanced circuit design and proven processing technology. The successive approximation function is implemented with I^2L (integrated injection logic). Thin-film SiCr resistors provide the stability required to prevent missing codes over the entire operating temperature range while laser wafer trimming of the resistor ladder permits calibration of the device to within ±1LSB. Thus, no user trims for gain or offset are required. Conversion time of the device is 10μs.

The AD670 is available in four package types and five grades. The J and K grades are specified over 0 to +70°C and come in 20-pin plastic DIP packages or 20-terminal PLCC packages. The A and B grades (−40°C to +85°C) and the S grade (−55°C to +125°C) come in 20-pin ceramic DIP packages.

The S grade is also available with optional processing to MIL-STD-883 in 20-pin ceramic DIP or 20-terminal LCC packages. The Analog Devices Military Products Databook should be consulted for detailed specifications.

PRODUCT HIGHLIGHTS

1. The AD670 is a complete 8-bit A/D including three-state outputs and microprocessor control for direct connection to 8-bit data buses. No external components are required to perform a conversion.
2. The flexible input stage features a differential instrumentation amp input with excellent common-mode rejection. This allows direct interface to a variety of transducers without preamplification.
3. No user trims are required for 8-bit accurate performance.
4. Operation from a single +5V supply allows the AD670 to run off of the microprocessor's supply.
5. Four convenient input ranges (two unipolar and two bipolar) are available through internal scaling resistors: 0 to 255mV (1mV/LSB) and 0 to 2.55V (10mV/LSB).
6. Software control of the output mode is provided. The user can easily select unipolar or bipolar inputs and binary or 2's complement output codes.

AD670—SPECIFICATIONS (@ V_{CC} = +5V and +25°C unless otherwise noted)

Model	AD670J			AD670K			Units
	Min	Typ	Max	Min	Typ	Max	
OPERATING TEMPERATURE RANGE	0		+70	0		+70	°C
RESOLUTION	8			8			Bit
CONVERSION TIME			**10**			**10**	µs
RELATIVE ACCURACY			±1/2			±1/4	LSB
T_{min} to T_{max}			±1/2			±1/2	LSB
DIFFERENTIAL LINEARITY ERROR[1]							
T_{min} to T_{max}	**GUARANTEED NO MISSING CODES ALL GRADES**						
GAIN ACCURACY							
@ +25°C			**±1.5**			**±0.75**	LSB
T_{min} to T_{max}			**±2.0**			**±1.0**	LSB
UNIPOLAR ZERO ERROR							
@ +25°C			**±1.5**			**±0.75**	LSB
T_{min} to T_{max}			**±2.0**			**±1.0**	LSB
BIPOLAR ZERO ERROR							
@ +25°C			**±1.5**			**±0.75**	LSB
T_{min} to T_{max}			**±2.0**			**±1.0**	LSB
ANALOG INPUT RANGES							
DIFFERENTIAL ($-V_{IN}$ to $+V_{IN}$)							
Low Range		0 to +255			0 to +255		mV
		−128 to +127			−128 to +127		mV
High Range		0 to +2.55			0 to +2.55		V
		−1.28 to +1.27			−1.28 to +1.27		V
ABSOLUTE (Inputs to Power Gnd)							
Low Range T_{min} to T_{max}	**−0.150**		**V_{CC} −3.4**	**−0.150**		**V_{CC} −3.4**	V
High Range T_{min} to T_{max}	−1.50		V_{CC}	−1.50		V_{CC}	V
BIAS CURRENT (255mV RANGE)							
T_{min} to T_{max}		200	**500**		200	**500**	nA
OFFSET CURRENT (255mV RANGE)							
T_{min} to T_{max}		40	**200**		40	**200**	nA
2.55V RANGE INPUT RESISTANCE	**8.0**		**12.0**	**8.0**		**12.0**	kΩ
2.55V RANGE FULL SCALE MATCH							
+ AND − INPUT		±1/2			±1/2		LSB
COMMON-MODE REJECTION							
RATIO (255mV RANGE)		**1**			**1**		LSB
COMMON-MODE REJECTION							
RATIO (2.55V RANGE)		**1**			1		LSB
POWER SUPPLY							
Operating Range	**4.5**		**5.5**	**4.5**		**5.5**	V
Current I_{CC}		30	**45**		30	**45**	mA
Rejection Ratio T_{min} to T_{max}			**0.015**			**0.015**	% of FS/%
DIGITAL OUTPUTS							
SINK CURRENT (V_{OUT} = 0.4V)							
T_{min} to T_{max}	**1.6**			**1.6**			mA
SOURCE CURRENT (V_{OUT} = 2.4V)							
T_{min} to T_{max}	**0.5**			**0.5**			mA
THREE-STATE LEAKAGE CURRENT			**±40**			**±40**	µA
OUTPUT CAPACITANCE		5			5		pF
DIGITAL INPUT VOLTAGE							
V_{INL}			**0.8**			**0.8**	V
V_{INH}	**2.0**			**2.0**			V
DIGITAL INPUT CURRENT							
(0≤V_{IN}≤ +5V)							
I_{INL}	**−100**			**−100**			µA
I_{INH}			**+100**			**+100**	µA
INPUT CAPACITANCE		10			10		pF

NOTES

[1]Tested at V_{CC} = 4.5V, 5.0V and 5.5V.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

Model	AD670A			AD670B			AD670S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPERATING TEMPERATURE RANGE	−40		+85	−40		+85	−55		+125	°C
RESOLUTION	8			8			8			Bit
CONVERSION TIME			10			10			10	µs
RELATIVE ACCURACY			±1/2			±1/4			±1/2	LSB
T_{min} to T_{max}			±1/2			±1/2			±1	LSB
DIFFERENTIAL LINEARITY ERROR[1]										
T_{min} to T_{max}	GUARANTEED NO MISSING CODES ALL GRADES									
GAIN ACCURACY										
@ +25°C			±1.5			±0.75			±1.5	LSB
T_{min} to T_{max}			±2.5			±1.5			±2.5	LSB
UNIPOLAR ZERO ERROR										
@ +25°C			±1.0			±0.5			±1.0	LSB
T_{min} to T_{max}			±2.0			±1.0			±2.0	LSB
BIPOLAR ZERO ERROR										
@ +25°C			±1.0			±0.5			±1.0	LSB
T_{min} to T_{max}			±2.0			±1.0			±2.0	LSB
ANALOG INPUT RANGES										
DIFFERENTIAL ($-V_{IN}$ to $+V_{IN}$)										
Low Range		0 to +255			0 to +255			0 to +255		mV
		−128 to +127			−128 to +127			−128 to +127		mV
High Range		0 to +2.55			0 to +2.55			0 to +2.55		V
		−1.28 to +1.27			−1.28 to +1.27			−1.28 to +1.27		V
ABSOLUTE (Inputs to Power Gnd)										
Low Range T_{min} to T_{max}	−0.150		V_{CC} −3.5	−0.150		V_{CC} −3.5	−0.150		V_{CC} −3.5	V
High Range T_{min} to T_{max}	−1.50		V_{CC}	−1.50		V_{CC}	−1.50		V_{CC}	V
BIAS CURRENT (255mV RANGE)										
T_{min} to T_{max}		200	500		200	500		200	750	nA
OFFSET CURRENT (255mV RANGE)										
T_{min} to T_{max}		40	200		40	200		40	200	nA
2.55V RANGE INPUT RESISTANCE	8.0		12.0	8.0		12.0	8.0		12.0	kΩ
2.55V RANGE FULL SCALE MATCH										
+ AND − INPUT		±1/2			±1/2			±1/2		LSB
COMMON-MODE REJECTION										
RATIO (255mV RANGE)			1			1			1	LSB
COMMON-MODE REJECTION										
RATIO (2.55V RANGE)			1			1			1	LSB
POWER SUPPLY										
Operating Range	4.5		5.5	4.5		5.5	4.75		5.5	V
Current I_{CC}		30	45		30	45		30	45	mA
Rejection Ratio T_{min} to T_{max}			0.015			0.015			0.015	% of FS/%
DIGITAL OUTPUTS										
SINK CURRENT (V_{OUT} = 0.4V)										
T_{min} to T_{max}	1.6			1.6			1.6			mA
SOURCE CURRENT (V_{OUT} = 2.4V)										
T_{min} to T_{max}	0.5			0.5			0.5			mA
THREE-STATE LEAKAGE CURRENT			±40			±40			±40	µA
OUTPUT CAPACITANCE		5			5			5		pF
DIGITAL INPUT VOLTAGE										
V_{INL}			0.8			0.8			0.7	V
V_{INH}	2.0			2.0			2.0			V
DIGITAL INPUT CURRENT										
($0 \le V_{IN} \le +5V$)										
I_{INL}	−100			−100			−100			µA
I_{INH}			+100			+100			+100	µA
INPUT CAPACITANCE		10			10			10		pF

NOTES

[1]Tested at V_{CC} = 4.5V, 5.0V and 5.5V for A, B grades; 4.75V, 5.0V and 5.5V for S grade.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

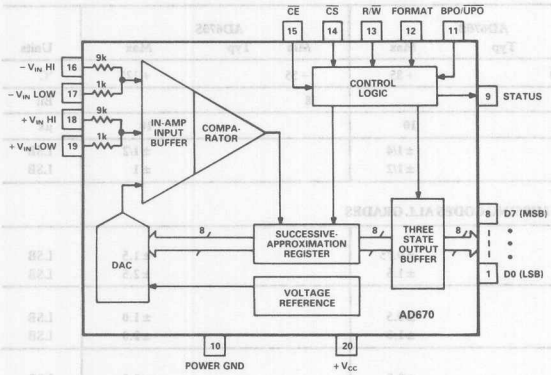


Figure 1. AD670 Block Diagram and Terminal Configuration (All Packages)

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Ground	0V to +7.5V
Digital Inputs (Pins 11-15)	−0.5V to V_{CC} +0.5V
Digital Outputs (Pins 1-9)	Momentary Short to V_{CC} or Ground
Analog Inputs (Pins 16-19)	−30V to +30V
Power Dissipation	450mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy @ +25°C	Gain Accuracy @ +25°C	Package Option[2]
AD670JN	0 to +70°C	±1/2LSB	±1.5LSB	Plastic DIP (N-20)
AD670JP	0 to +70°C	±1/2LSB	±1.5LSB	PLCC (P-20A)
AD670KN	0 to +70°C	±1/4LSB	±0.75LSB	Plastic DIP (N-20)
AD670KP	0 to +70°C	±1/4LSB	±0.75LSB	PLCC (P-20A)
AD670AD	−40°C to +85°C	±1/2LSB	±1.5LSB	Ceramic DIP (D-20)
AD670BD	−40°C to +85°C	±1/4LSB	±0.75LSB	Ceramic DIP (D-20)
AD670SD	−55°C to +125°C	±1/2LSB	±1.5LSB	Ceramic DIP (D-20)

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook.
[2]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

CIRCUIT OPERATION/FUNCTIONAL DESCRIPTION

The AD670 is a functionally complete 8-bit signal conditioning A/D converter with microprocessor compatibility. The input section uses an instrumentation amplifier to accomplish the voltage to current conversion. This front end provides a high impedance, low bias current differential amplifier. The common-mode range allows the user to directly interface the device to a variety of transducers.

The A/D conversions are controlled by R/$\overline{W}$, $\overline{CS}$, and $\overline{CE}$. The R/$\overline{W}$ line directs the converter to read or start a conversion. A minimum write/start pulse of 300ns is required on either $\overline{CE}$ or $\overline{CS}$. The STATUS line goes high, indicating that a conversion is in process. The conversion thus begun, the internal 8-bit DAC is sequenced from MSB to LSB using a novel successive approximation technique. In conventional designs, the DAC is stepped through the bits by a clock. This can be thought of as a static design since the speed at which the DAC is sequenced is determined solely by the clock. No clock is used in the AD670. Instead, a "dynamic SAR" is created consisting of a string of inverters with taps along the delay line. Sections of the delay line between taps act as one shots. The pulses are used to set and reset the DAC's bits and strobe the comparator. When strobed, the comparator then determines whether the addition of each successively weighted bit current causes the DAC current sum to be greater or less than the input current. If the sum is less, the bit is turned off. After all bits are tested, the SAR holds an 8-bit code representing the input signal to within 1/2LSB accuracy. Ease of implementation and reduced dependence on process related variables make this an attractive approach to a successive approximation design.

The SAR provides an end-of-conversion signal to the control logic which then brings the STATUS line low. Data outputs remain in a high impedance state until R/$\overline{W}$ is brought high with $\overline{CE}$ and $\overline{CS}$ low and allows the converter to be read. Bringing $\overline{CE}$ or $\overline{CS}$ high during the valid data period ends the read cycle. The output buffers cannot be enabled during a conversion. Any convert start commands will be ignored until the conversion cycle is completed; once a conversion cycle has been started it cannot be stopped or restarted.

The AD670 provides the user with a great deal of flexibility by offering two input spans and formats and a choice of output codes. Input format and input range can each be selected. The BPO/$\overline{UPO}$ pin controls a switch which injects a bipolar offset current of a value equal to the MSB less 1/2LSB into the summing node of the comparator to offset the DAC output. Two precision 10 to 1 attenuators are included on board to provide input range selection of 0 to 2.55V or 0 to 255mV. Additional ranges of

– 1.28 to 1.27V and – 128 to 127mV are possible if the BPO/$\overline{\text{UPO}}$ switch is high when the conversion is started. Finally, output coding can be chosen using the FORMAT pin when the conversion is started. In the bipolar mode and with a logic 1 on FORMAT, the output is in two's complement; with a logic 0, the output is offset binary.

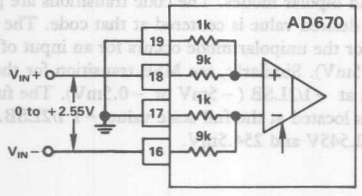
CONNECTING THE AD670

The AD670 has been designed for ease of use. All active components required to perform a complete A/D conversion are on board and are connected internally. In addition, all calibration trims are performed at the factory, assuring specified accuracy without user trims. There are, however, a number of options and connections that should be considered to obtain maximum flexibility from the part.

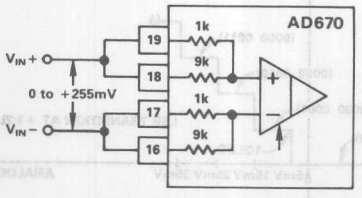
INPUT CONNECTIONS

Standard connections are shown in the figures that follow. An input range of 0 to 2.55V may be configured as shown in Figure 2a. This will provide a one LSB change for each 10mV of input change. The input range of 0 to 255mV is configured as shown in Figure 2b. In this case, each LSB represents 1mV of input change. When unipolar input signals are used, Pin 11, BPO/$\overline{\text{UPO}}$, should be grounded. Pin 11 selects the input format for either unipolar or bipolar signals. Figures 3a and 3b show the input connections for bipolar signals. Pin 11 should be tied to $+V_{CC}$ for bipolar inputs.

Although the instrumentation amplifier has a differential input, there must be a return path to ground for the bias currents. If it is not provided, these currents will charge stray capacitances and cause internal circuit nodes to drift uncontrollably causing the digital output to change. Such a return path is provided in Figures 2a and 3a (larger input ranges) since the 1k resistor leg



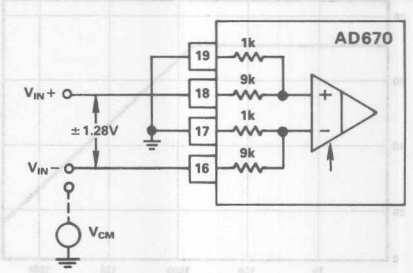
2a. 0 to 2.55V (10mV/LSB)



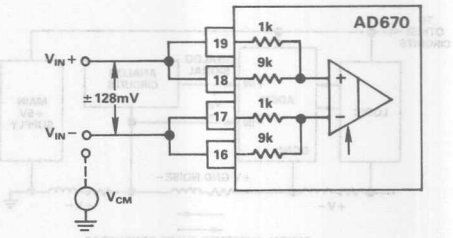
2b. 0 to 255mV (1mV/LSB)

NOTE: PIN 11, BPO/$\overline{\text{UPO}}$ SHOULD BE LOW WHEN CONVERSION IS STARTED.

Figure 2. Unipolar Input Connections



3a. ± 1.28V Range



3b. ± 128mV Range

NOTE: PIN 11, BPO/$\overline{\text{UPO}}$ SHOULD BE HIGH WHEN CONVERSION IS STARTED.

Figure 3. Bipolar Input Connections

is tied to ground. This is not the case for Figures 2b and 3b (the lower input ranges). When connecting the AD670 inputs to floating sources, such as transformers and ac-coupled sources, there must still be a dc path from each input to common. This can be accomplished by connecting a 10kΩ resistor from each input to ground.

Bipolar Operation

Through special design of the instrumentation amplifier, the AD670 accommodates input signal excursions below ground, even though it operates from a single 5V supply. To the user, this means that true bipolar input signals can be used without the need for any additional external components. Bipolar signals can be applied differentially across both inputs, or one of the inputs can be grounded and a bipolar signal applied to the other.

Common-Mode Performance

The AD670 is designed to reject dc and ac common-mode voltages. In some applications it is useful to apply a differential input signal V_{IN} in the presence of a dc common-mode voltage V_{CM}. The user must observe the absolute input signal limits listed in the specifications, which represent the maximum voltage V_{IN} + V_{CM} that can be applied to either input without affecting proper operation. Exceeding these limits (within the range of absolute maximum ratings), however, will not cause permanent damage.

The excellent common-mode rejection of the AD670 is due to the instrumentation amplifier front end, which maintains the differential signal until it reaches the output of the comparator. In contrast to a standard operational amplifier, the instrumentation amplifier front end provides significantly improved CMRR over a wide frequency range (Figure 4a).

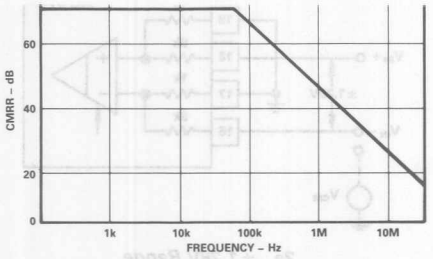


Figure 4a. CMRR over Frequency

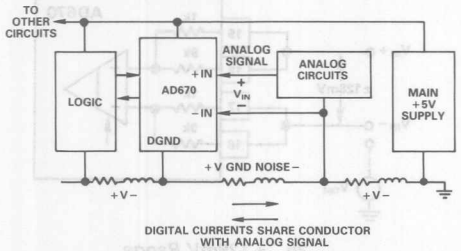


Figure 4b. AD670 Input Rejects Common-Mode Ground Noise

Good common-mode performance is useful in a number of situations. In bridge-type transducer applications, such performance facilitates the recovery of differential analog signals in the presence of a dc common-mode or a noisy electrical environment. High-frequency CMRR also becomes important when the analog signal is referred to a noisy, remote digital ground. In each case, the CMRR specification of the AD670 allows the integrity of the input signal to be preserved.

The AD670's common-mode voltage tolerance allows great flexibility in circuit layout. Most other A/D converters require the establishment of one point as the analog reference point. This is necessary in order to minimize the effects of parasitic voltages. The AD670, however, eliminates the need to make the analog ground reference point and A/D analog ground one and the same. Instead, a system such as that shown in Figure 4b is possible as a result of the AD670's common-mode performance. The resistors and inductors in the ground return represent unavoidable system parasitic impedances.

Input/Output Options

Data output coding (2's complement vs. straight binary) is selected using Pin 12, the FORMAT pin. The selection of input format (bipolar vs. unipolar) is controlled using Pin 11, BPO/$\overline{\text{UPO}}$. Prior to a write/convert, the state of FORMAT and BPO/$\overline{\text{UPO}}$ should be available to the converter. These lines may be tied to the data bus and may be changed with each conversion if desired. The configurations are shown in Table I. Output coding for representative signals in each of these configurations is shown in Figure 5.

An output signal, STATUS, indicates the status of the conversion. STATUS goes high at the beginning of the conversion and returns low when the conversion cycle has been completed.

0	0	Unipolar/Straight Binary
1	0	Bipolar/Offset Binary
0	1	Unipolar/2's Complement
1	1	Bipolar/2's Complement

Table I. AD670 Input Selection/Output Format Truth Table

$+V_{IN}$	$-V_{IN}$	DIFF V_{IN}	STRAIGHT BINARY (FORMAT = 0, BPO/$\overline{\text{UPO}}$ = 0)
0	0	0	0000 0000
128mV	0	128mV	1000 0000
255mV	0	255mV	1111 1111
255mV	255mV	0	0000 0000
128mV	127mV	1mV	0000 0001
128mV	–127mV	255mV	1111 1111

Figure 5a. Unipolar Output Codes (Low Range)

$+V_{IN}$	$-V_{IN}$	DIFF V_{IN}	OFFSET BINARY (FORMAT = 0, BPO/$\overline{\text{UPO}}$ = 1)	2's COMPLEMENT (FORMAT = 1, BPO/$\overline{\text{UPO}}$ = 1)
0	0	0	1000 0000	0000 0000
127mV	0	127mV	1111 1111	0111 1111
1.127V	1.000V	127mV	1111 1111	0111 1111
255mV	255mV	0	1000 0000	0000 0000
128mV	127mV	1mV	1000 0001	0000 0001
127mV	128mV	–1mV	0111 1111	1111 1111
127mV	255mV	–128mV	0000 0000	1000 0000
–128mV	0	–128mV	0000 0000	1000 0000

Figure 5b. Bipolar Output Codes (Low Range)

Calibration

Because of its precise factory calibration, the AD670 is intended to be operated without user trims for gain and offset; therefore, no provisions have been made for such user trims. Figures 6a, 6b, and 6c show the transfer curves at zero and full scale for the unipolar and bipolar modes. The code transitions are positioned so that the desired value is centered at that code. The first LSB transition for the unipolar mode occurs for an input of +1/2LSB (5mV or 0.5mV). Similarly, the MSB transition for the bipolar mode is set at –1/2LSB (–5mV or –0.5mV). The full scale transition is located at the full scale value –1 1/2LSB. These values are 2.545V and 254.5mV.

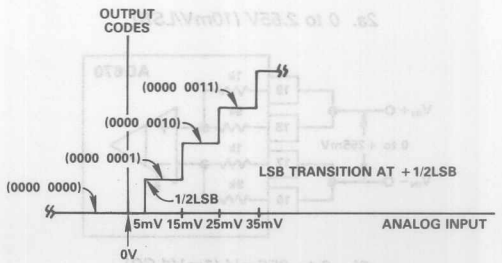


Figure 6a. Unipolar Transfer Curve

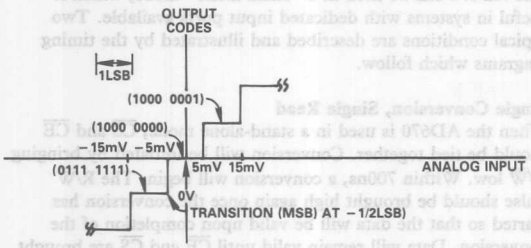


Figure 6b. Bipolar

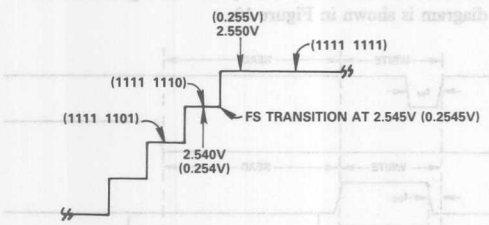


Figure 6c. Full Scale (Unipolar)

Figure 6. Transfer Curves

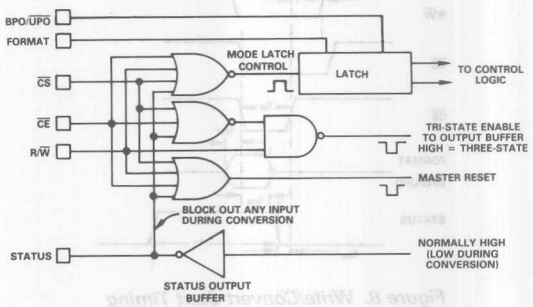


Figure 7. Control Logic Block Diagram

R/$\overline{W}$	$\overline{CS}$	$\overline{CE}$	OPERATION
0	0	0	WRITE/CONVERT
1	0	0	READ
X	X	1	NONE
X	1	X	NONE

Table II. AD670 Control Signal Truth Table

CONTROL AND TIMING OF THE AD670

Control Logic

The AD670 contains on-chip logic to provide conversion and data read operations from signals commonly available in microprocessor systems. Figure 7 shows the internal logic circuitry of the AD670. The control signals, $\overline{CE}$, $\overline{CS}$, and R/$\overline{W}$ control the operation of the converter. The read or write function is determined by R/$\overline{W}$ when both $\overline{CS}$ and $\overline{CE}$ are low as shown in Table II. If all three control inputs are held low longer than the conversion time, the device will continuously convert until one input, $\overline{CE}$, $\overline{CS}$, or R/$\overline{W}$ is brought high. The relative timing of these signals is discussed later in this section.

Timing

The AD670 is easily interfaced to a variety of microprocessors and other digital systems. The following discussion of the timing requirements of the AD670 control signals will provide the designer with useful insight into the operation of the device.

Write/Convert Start Cycle

Figure 8 shows a complete timing diagram for the write/convert start cycle. $\overline{CS}$ (chip select) and $\overline{CE}$ (chip enable) are active low and are interchangeable signals. Both $\overline{CS}$ and $\overline{CE}$ must be low for the converter to read or start a conversion. The minimum pulse width, t_W, on either $\overline{CS}$ or $\overline{CE}$ is 300ns to start a conversion.

Table III. AD670 TIMING SPECIFICATIONS

Boldface indicates parameters tested 100% unless otherwise noted. See Specifications page for explanation.

		@ +25°C			
Symbol	Parameter	Min	Typ	Max	Units
WRITE/CONVERT START MODE					
t_W	Write/Start Pulse Width	300			ns
t_{DS}	Input Data Setup Time	200			ns
t_{DH}	Input Data Hold	10			ns
t_{RWC}	Read/Write Setup Before Control	0			ns
t_{DC}	Delay to Convert Start			700	ns
t_C	**Conversion Time**			**10**	µs
READ MODE					
t_R	Read Time	250			ns
t_{SD}	Delay from Status Low to Data Read			250	ns
t_{TD}	**Bus Access Time**		200	**250**	ns
t_{DH}	Data Hold Time	25			ns
t_{DT}	**Output Float Delay**			**150**	ns
t_{RT}	R/$\overline{W}$ before $\overline{CE}$ or $\overline{CS}$ low	0			ns

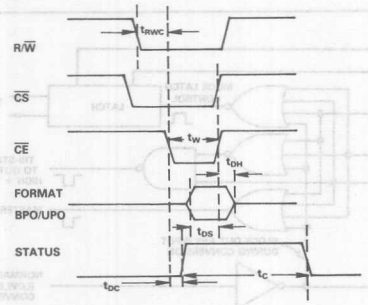


Figure 8. Write/Convert Start Timing

The R/$\overline{W}$ line is used to direct the converter to start a conversion (R/$\overline{W}$ low) or read data (R/$\overline{W}$ high). The relative sequencing of the three control signals (R/$\overline{W}$, $\overline{CE}$, $\overline{CS}$) is unimportant. However, when all three signals remain low for at least 300ns (t_W), STATUS will go high to signal that a conversion is taking place.

Once a conversion is started and the STATUS line goes high, convert start commands will be ignored until the conversion cycle is complete. The output data buffer cannot be enabled during a conversion.

Read Cycle

Figure 9 shows the timing for the data read operation. The data outputs are in a high impedance state until a read cycle is initiated. To begin the read cycle, R/$\overline{W}$ is brought high. During a read cycle, the minimum pulse length for $\overline{CE}$ and $\overline{CS}$ is a function of the length of time required for the output data to be valid. The data becomes valid and is available to the data bus in a maximum of 250ns. This delay between the high impedance state and valid data is the maximum bus access time or t_{TD}. Bringing $\overline{CE}$ or $\overline{CS}$ high during valid data ends the read cycle. The outputs remain valid for a minimum of 25ns (t_{DH}) and return to the high impedance state after a delay, t_{DT}, of 150ns maximum.

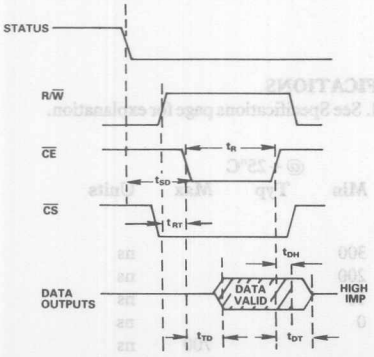


Figure 9. Read Cycle Timing

STAND-ALONE OPERATION

The AD670 can be used in a "stand-alone" mode, which is useful in systems with dedicated input ports available. Two typical conditions are described and illustrated by the timing diagrams which follow.

Single Conversion, Single Read

When the AD670 is used in a stand-alone mode, $\overline{CS}$ and $\overline{CE}$ should be tied together. Conversion will be initiated by bringing R/$\overline{W}$ low. Within 700ns, a conversion will begin. The R/$\overline{W}$ pulse should be brought high again once the conversion has started so that the data will be valid upon completion of the conversion. Data will remain valid until $\overline{CE}$ and $\overline{CS}$ are brought high to indicate the end of the read cycle or R/$\overline{W}$goes low. The timing diagram is shown in Figure 10.

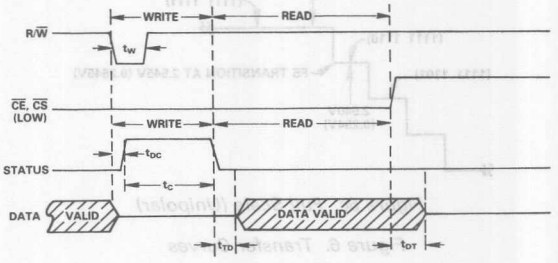


Figure 10. Stand-Alone Mode Single Conversion/ Single Read

Continuous Conversion, Single Read

A variety of applications may call for the A/D to be read after several conversions. In process control systems, this is often the case since a reading from a sensor may only need to be updated every few conversions. Figure 11 shows the timing relationships.

Once again, $\overline{CE}$ and $\overline{CS}$ should be tied together. Conversion will begin when the R/$\overline{W}$ signal is brought low. The device will convert repeatedly as indicated by the status line. A final conversion will take place once the R/$\overline{W}$ line has been brought high. The rising edge of R/$\overline{W}$ must occur while STATUS is high. R/$\overline{W}$ should not return high while STATUS is low since the circuit is in a reset state prior to the next conversion. Since the rising edge of R/$\overline{W}$ must occur while STATUS is high, R/$\overline{W}$'s length must be a minimum of 10.25µs (t_C + t_{TD}). Data becomes valid upon completion of the conversion and will remain so until the $\overline{CE}$ and $\overline{CS}$ lines are brought high indicating the end of the read cycle or R/$\overline{W}$ goes low initiating a new series of conversions.

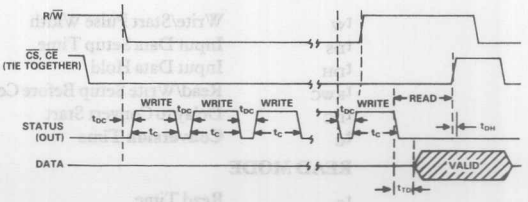


Figure 11. Stand-Alone Mode Continuous Conversion/ Single Read

APPLYING THE AD670

The AD670 has been designed for ease of use, system compatibility, and minimization of external components. Transducer interfaces generally require signal conditioning and preamplification before the signal can be converted. The AD670 will reduce and even eliminate this excess circuitry in many cases. To illustrate the flexibility and superior solution that the AD670 can bring to a transducer interface problem, the following discussions are offered.

Temperature Measurements

Temperature transducers are one of the most common sources of analog signals in data acquisition systems. These sensors require circuitry for excitation and preamplification/buffering. The instrumentation amplifier input of the AD670 eliminates the need for this signal conditioning. The output signals from temperature transducers are generally sufficiently slow that a sample/hold amplifier is not required. Figure 12 shows the AD590 IC temperature transducer interfaced to the AD670. The AD580 voltage reference is used to offset the input for 0°C calibration. The current output of the AD590 is converted into a voltage by R1. The high impedance unbuffered voltage is applied directly to the AD670 configured in the −128mV to 127mV bipolar range. The digital output will have a resolution of 1°C.

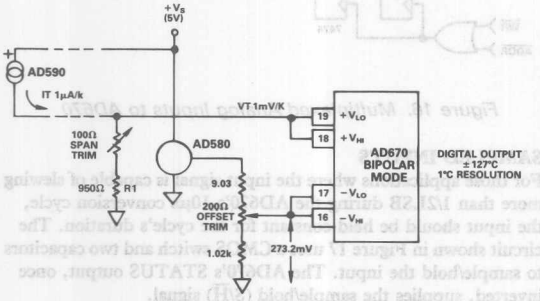


Figure 12. AD670 Temperature Transducer Interface

Platinum RTDs are also a popular, temperature transducer. Typical RTDs have a resistance of 100Ω at 0°C and change resistance 0.4Ω per °C. If a constant excitation current is caused to flow in the RTD, the change in voltage drop will be a measure of the change in temperature. Figure 13 shows such a method and the required connections to the AD670. The AD580 2.5V reference provides the accurate voltage for the excitation current and range offsetting for the RTD. The op-amp is configured to force a constant 2.5mA current through the RTD. The differential inputs of the AD670 measure the difference between a fixed offset voltage and the temperature dependent output of the op-amp which varies with the resistance of the RTD. The RTD change of approximately 0.4Ω/°C results in a 1mV/°C voltage change. With the AD670 in the 1mV/LSB range, temperatures from 0 to 255°C can be measured.

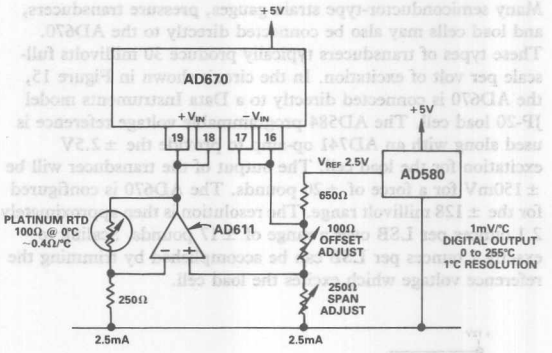


Figure 13. Low Cost RTD Interface

Differential temperature measurements can be made using an AD590 connected to each of the inputs as shown in Figure 14. This configuration will allow the user to measure the relative temperature difference between two points with a 1°C resolution. Although the internal 1k and 9k resistors on the inputs have ±20% tolerance, trimming the AD590 is unnecessary as most differential temperature applications are concerned with the relative differences between the two. However, the user may see up to a 20% scale factor error in the differential temperature to digital output transfer curve.

This scale factor error can be eliminated through a software correction. Offset corrections can be made by adjusting for any difference that results when both sensors are held at the same temperature. A span adjustment can then be made by immersing one AD590 in an ice bath and one in boiling water and eliminating any deviation from 100°C. For a low cost version of this setup, the plastic AD592 can be substituted for the AD590.

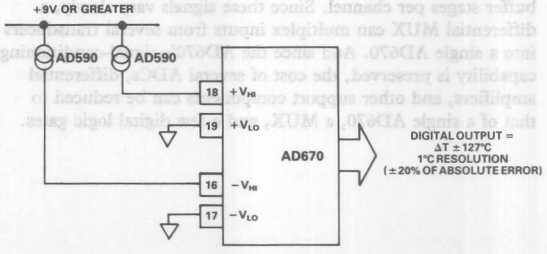


Figure 14. Differential Temperature Measurement Using the AD590

STRAIN GAUGE MEASUREMENTS

Many semiconductor-type strain gauges, pressure transducers, and load cells may also be connected directly to the AD670. These types of transducers typically produce 30 millivolts full-scale per volt of excitation. In the circuit shown in Figure 15, the AD670 is connected directly to a Data Instruments model JP-20 load cell. The AD584 programmable voltage reference is used along with an AD741 op-amp to provide the ±2.5V excitation for the load cell. The output of the transducer will be ±150mV for a force of ±20 pounds. The AD670 is configured for the ±128 millivolt range. The resolution is then approximately 2.1 ounces per LSB over a range of ±17 pounds. Scaling to exactly 2 ounces per LSB can be accomplished by trimming the reference voltage which excites the load cell.

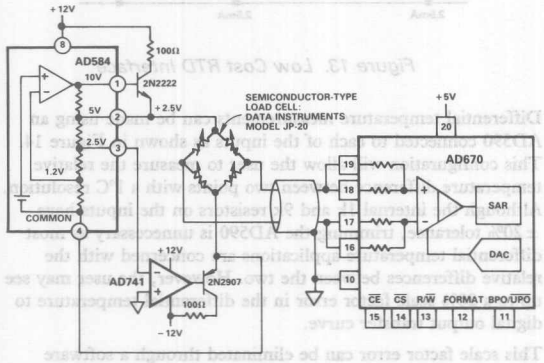


Figure 15. AD670 Load Cell Interface

MULTIPLEXED INPUTS

Most data acquisition systems require the measurement of several analog signals. Multiple A/D converters are often used to digitize these inputs, requiring additional preamplification and buffer stages per channel. Since these signals vary slowly, a differential MUX can multiplex inputs from several transducers into a single AD670. And since the AD670's signal-conditioning capability is preserved, the cost of several ADCs, differential amplifiers, and other support components can be reduced to that of a single AD670, a MUX, and a few digital logic gates.

An AD7502 dual 4-channel MUX appears in Figure 16 multiplexing four differential signals to the AD670. The AD7502's decoded address is gated with the microprocessor's write signal to provice a latching strobe at the flip-flops. A write cycle to the AD7502's address then latches the two LSBs of the data word thereby selecting the input channel for subsequent conversions.

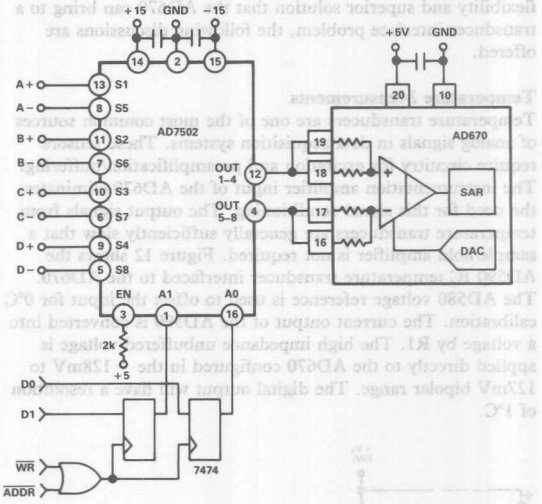


Figure 16. Multiplexed Analog Inputs to AD670

SAMPLED INPUTS

For those applications where the input signal is capable of slewing more than 1/2LSB during the AD670's 10μs conversion cycle, the input should be held constant for the cycle's duration. The circuit shown in Figure 17 uses a CMOS switch and two capacitors to sample/hold the input. The AD670's STATUS output, once inverted, supplies the sample/hold ($S/\overline{H}$) signal.

A convert command applied on the $\overline{CE}$, $\overline{CS}$ OR $R/\overline{W}$ lines will initiate the conversion. The AD670's STATUS output, once inverted, supplies the sample/hold signal to the CD4066. The CD4066 CMOS switch shown in Figure 17 was chosen for its fast transition times, low on-resistance and low cost. The control input's propagation delay for switch-closed to switch-open should remain less than 150ns to ensure that the sample-to-hold transition occurs before the first bit decision in the AD670.

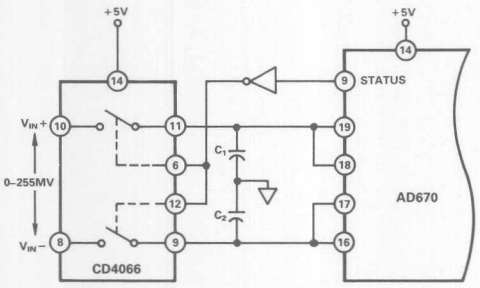


Figure 17. Low Cost Sample-and-Hold Circuit for AD670

Since settling to 1/2LSB at 8-bits of resolution requires 6.2 RC time constants, the 500pF hold capacitors and CD4066's 300Ω on-resistance yield an acquisition time of under 1μs, assuming a low impedance source.

This sample/hold approach makes use of the differential capabilities of the AD670. Because 500pF hold capacitors are used on both V_{IN}+ and V_{IN}− inputs, the droop rate depends only on the offset current of the AD670, typically 20nA. With the matched 500pF capacitors, the droop rate is 40μV/μs. The input will then droop only 0.4mV (0.4LSB) during the AD670's 10μs conversion time. The differential approach also minimizes pedestal error since only the difference in charge injection between the two switches results in errors at the A/D.

The fast conversion time and differential and common-mode capabilities of the AD670 permit this simple sample-hold design to perform well with low sample-to-hold offset, droop rate of about 40μV/μs and acquisition time under 1μs. The effective aperture time of the AD670 is reduced by about 2 orders of magnitude with this circuit, allowing frequencies to be converted up to several kilohertz.

While no input anti-aliasing filter is shown, filtering will be necessary to prevent output errors if higher frequencies are present in the input signal. Many practical variations are possible with this circuit, including input MUX control, for digitizing a number of AC channels.

IBM PC INTERFACE

The AD670 appears in Figure 18 interfaced to the IBM PC. Since the device resides in I/O space, its address is decoded from only the lower ten address lines and must be gated with AEN (active low) to mask out internal (DMA) cycles which use the same I/O address space. This active low signal is applied to $\overline{CS}$. AO, meanwhile, is reserved for the R/$\overline{W}$ input. This places

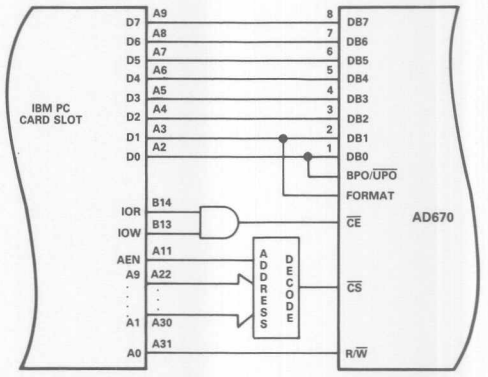


Figure 18. IBM PC Interface to AD670

the AD670 in two adjacent addresses; one for starting the conversion and the other for reading the result. The $\overline{IOR}$ and $\overline{IOW}$ signals are then gated and applied to $\overline{CE}$, while the lower two data lines are applied to FORMAT and BPO/$\overline{UPO}$ inputs to provide software programmable input formats and output coding.

In BASIC, a simple OUT ADDR, WORD command initiates a conversion. While the upper six bits of the data WORD are meaningless, the lower two bits define the analog input format and digital output coding according to Table IV. The data is available ten microseconds later (which is negligible in BASIC) and can be read using INP (ADDR + 1). The 3-line subroutine in Figure 19, used in conjunction with the interface of Figure 18, converts an analog input within a bipolar range to an offset binary coded digital word.

NOTE: Due to the large number of options that may be installed in the PC, the I/O bus loading should be limited to one Schottky TTL load. Therefore, a buffer/driver should be used when interfacing more than two AD670's to the I/O bus.

DATA	INPUT FORMAT	OUTPUT CODING
0	Unipolar	Straight Binary
1	Bipolar	Offset Binary
2	Unipolar	2's Complement
3	Bipolar	2's Complement

Table IV.

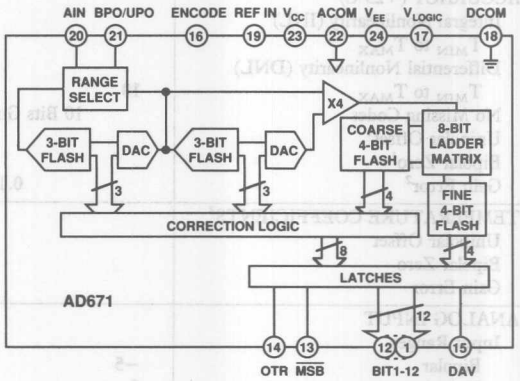
```
10 OUT &H310,1                    'INITIATE CONVERSION
20 ANALOGIN = INP (&H311)         'READ ANALOG INPUT
30 RETURN
```

Figure 19. Conversion Subroutine

FEATURES

12-Bit Resolution
24-Pin "Skinny DIP" Package
Conversion Time: 500 ns max – AD671J/K/S-500
750 ns max – AD671J/K/S-750
Low Power: 475 mW
Unipolar (0 to +5 V, 0 to +10 V) and Bipolar Input Ranges (±5 V)
Twos Complement or Offset Binary Output Data
Out of Range Indicator
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD671 is a high speed monolithic 12-bit A/D converter offering conversion rates of up to 2 MHz (500 ns conversion time). The combination of a merged high speed bipolar/CMOS process and a novel architecture results in a combination of speed and power consumption far superior to previously available hybrid implementations. Additionally, the greater reliability of monolithic construction offers improved system reliability and lower costs than hybrid designs.

The AD671 uses a subranging flash conversion technique, with digital error correction for possible errors introduced in the first part of the conversion cycle. An on-chip timing generator provides strobe pulses for each of the four internal flash cycles and assures adequate settling time for the interflash residue amplifier. A single ENCODE pulse is used to control the converter.

The performance of the AD671 is made possible by using high speed, low noise bipolar circuitry in the linear sections and low power CMOS for the logic sections. Analog Devices' ABCMOS-1 process provides both high speed bipolar and 2-micron CMOS devices on a single chip. Laser trimmed thin-film resistors are used to provide accuracy and temperature stability.

The AD671 is available in two conversion speeds and performance grades. The AD671J and K grades are specified for operation over the 0 to +70°C temperature range. The AD671S grades are specified for operation over the −55°C to +125°C temperature range. All grades are available in a 0.300 inch wide 24-pin ceramic DIP. The J and K grades are also available in a 24-pin plastic DIP.

PRODUCT HIGHLIGHTS

1. The AD671 offers a single chip 2 MHz analog-to-digital conversion function in a space saving 24-pin DIP.
2. Input signal ranges are 0 to +5 V and 0 to +10 V unipolar, and −5 V to +5 V bipolar, selected by pin strapping. Input resistance is 1.5 kΩ. Power supplies are +5 V and −5 V, and typical power consumption is less than 500 mW.
3. The external +5 V reference can be chosen to suit the dc accuracy and temperature drift requirements of the application.
4. Output data is available in unipolar, bipolar offset or bipolar twos complement binary format.
5. An OUT OF RANGE output bit indicates when the input signal is beyond the AD671's input range.
6. The AD671 is available in versions compliant with the MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD671/883B data sheet for detailed specifications.

AD671—SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −5 V ± 5%, V_{REF} = +5.000 V, unless otherwise indicated)

Parameter	AD671J/S-500 Min	AD671J/S-500 Typ	AD671J/S-500 Max	AD671K-500 Min	AD671K-500 Typ	AD671K-500 Max	Units
RESOLUTION	12			12			Bits
ACCURACY (+25°C)							
Integral Nonlinearity (INL)							
T_{MIN} to T_{MAX}			±4			±2	LSB
Differential Nonlinearity (DNL)							
T_{MIN} to T_{MAX}	**10**			**11**			Bits
No Missing Codes		10 Bits Guaranteed			11 Bits Guaranteed		
Unipolar Offset[1]			±4			±4	LSB
Bipolar Zero[1]			±10			±10	LSB
Gain Error[2]		0.1	0.25		0.1	0.25	% FSR
TEMPERATURE COEFFICIENTS[3]							
Unipolar Offset			±10			±10	ppm/°C
Bipolar Zero			±15			±15	ppm/°C
Gain Error			±20			±20	ppm/°C
ANALOG INPUT							
Input Ranges							
Bipolar	−5		+5	−5		+5	Volts
Unipolar	**0**		+5	**0**		+5	Volts
	0		+10	**0**		+10	Volts
Input Resistance							
10 Volt Range	1.0	1.5	2.0	1.0	1.5	2.0	kΩ
5 Volt Range	0.5	0.75	1.0	0.5	0.75	1.0	kΩ
Input Capacitance		10			10		pF
Reference Input Resistance	2.4	3.5	4.7	2.4	3.5	4.7	kΩ
POWER SUPPLIES							
Power Supply Rejection[4]							
V_{CC} (+5 V ± 0.25 V)			±1			±1	LSB
V_{LOGIC} (+5 V ± 0.5 V)			±1			±1	LSB
V_{EE} (−5 V ± 0.25 V)			±1			±1	LSB
Operating Voltages							
V_{CC}	+4.75		+5.25	+4.75		+5.25	Volts
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	Volts
V_{EE}	−5.25		−4.75	−5.25		−4.75	Volts
Operating Current							
I_{CC}		46	56		46	56	mA
I_{LOGIC}[5]		3	6		3	6	mA
I_{EE}		46	56		46	56	mA
POWER CONSUMPTION		475	621		475	621	mW
TEMPERATURE RANGE							
Specified (J/K)	0		+70	0		+70	°C
(S)	−55		+125				°C

NOTES

[1]Adjustable to zero with external potentiometers. See Offset/Gain Calibration section for additional information.

[2]Full-scale range (FSR) is 5 V for the 0 to 5 V range and 10 V for the 0 to 10 V and −5 V to +5 V ranges.

[3]25°C to T_{MIN} and 25°C to T_{MAX}.

[4]Change in gain error as a function of the dc supply voltage.

[5]Tested under static conditions. See Figure 12 for typical curves of I_{LOGIC} vs. Conversion Rate and Output Loading.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at 0, +25°C and +70°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

DC SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −5 V ± 5%, V_{REF} = +5.000 V, unless otherwise indicated)

Parameter	AD671J/S-750 Min	AD671J/S-750 Typ	AD671J/S-750 Max	AD671K-750 Min	AD671K-750 Typ	AD671K-750 Max	Units
RESOLUTION	12			12			Bits
ACCURACY (+25°C)							
Integral Nonlinearity (INL)							
T_{MIN} to T_{MAX} (J)			±2			±1.5	LSB
T_{MIN} to T_{MAX} (S)			±2.5				LSB
Differential Nonlinearity (DNL)							
T_{MIN} to T_{MAX}	11			12			Bits
No Missing Codes	11 Bits Guaranteed			12 Bits Guaranteed			
Unipolar Offset[1]			±4			±4	LSB
Bipolar Zero[1]			±10			±10	LSB
Gain Error[2]		0.1	0.25		0.1	0.25	% FSR
TEMPERATURE COEFFICIENTS[3]							
Unipolar Offset			±10			±10	ppm/°C
Bipolar Zero			±15			±15	ppm/°C
Gain Error			±20			±20	ppm/°C
ANALOG INPUT							
Input Ranges							
Bipolar	−5		+5	−5		+5	Volts
Unipolar	0		+5	0		+5	Volts
	0		+10	0		+10	Volts
Input Resistance							
10 Volt Range	1.0	1.5	2.0	1.0	1.5	2.0	kΩ
5 Volt Range	0.5	0.75	1.0	0.5	0.75	1.0	kΩ
Input Capacitance		10			10		pF
Reference Input Resistance	2.4	3.5	4.7	2.4	3.5	4.7	kΩ
POWER SUPPLIES							
Power Supply Rejection[4]							
V_{CC} (+5 V ± 0.25 V)			±1			±1	LSB
V_{LOGIC} (+5 V ± 0.5 V)			±1			±1	LSB
V_{EE} (−5 V ± 0.25 V)			±1			±1	LSB
Operating Voltages							
V_{CC}	+4.75		+5.25	+4.75		+5.25	Volts
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	Volts
V_{EE}	−5.25		−4.75	−5.25		−4.75	Volts
Operating Current							
I_{CC}		46	56		46	56	mA
I_{LOGIC}[5]		3	6		3	6	mA
I_{EE}		46	56		46	56	mA
POWER CONSUMPTION		475	621		475	621	mW
TEMPERATURE RANGE							
Specified (J/K)	0		+70	0		+70	°C
(S)	−55		+125				°C

NOTES
[1]Adjustable to zero with external potentiometers. See Offset/Gain Calibration section for further information.
[2]Full-scale range (FSR) is 5 V for the 0 to 5 V range and 10 V for the 0 to 10 V and −5 V to +5 V ranges.
[3]25°C to T_{MIN} and 25°C to T_{MAX}.
[4]Change in gain error as a function of the dc supply voltage.
[5]Tested under static conditions. See Figure 12 for typical curve of I_{LOGIC} vs. Conversion Rate and Output Loading.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at 0, +25°C and +70°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested.

DIGITAL SPECIFICATIONS (For all grades I_{MIN} to I_{MAX}, with V_{CC} = +5 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −5 V ± 5%, V_{REF} = +5.000 V, unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units
LOGIC INPUT					
High Level Input Voltage	V_{IH}	+2.0			V
Low Level Input Voltage	V_{IL}			+0.8	V
High Level Input Current (V_{IN} = V_{LOGIC})	I_{IH}	−10		+10	μA
Low Level Input Current (V_{IN} = 0 V)	I_{IL}	−10		+10	μA
Input Capacitance	C_{IN}		5		pF
LOGIC OUTPUTS					
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}	+2.4			V
Low Level Output Voltage (I_{OL} = 1.6 mA)	V_{OL}			+0.4	V
Output Capacitance	C_{OUT}		5		pF

Specifications shown in **boldface** are tested on all devices at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

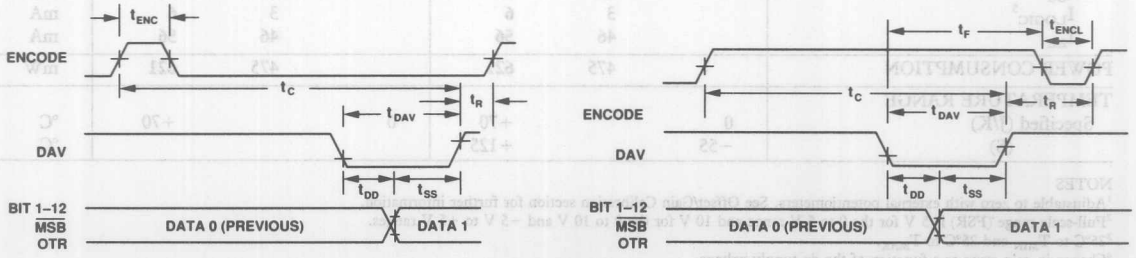
SWITCHING SPECIFICATIONS (For all grades T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −5 V ± 5%; V_{IL} = 0.8 V, V_{IH} = 2.0 V, V_{OL} = 0.4 V and V_{OH} = 2.4 V)

Parameter	Symbol	Min	Typ	Max	Units
Conversion Time					
(AD671-500)	t_C		475	500	ns
(AD671-750)	t_C		725	750	ns
ENCODE Pulse Width High					
(AD671-500)	t_{ENC}	20		30	ns
(AD671-750)	t_{ENC}	20		50	ns
ENCODE Pulse Width Low	t_{ENCL}	20			ns
DAV Pulse Width					
(AD671-500)	t_{DAV}	75		200	ns
(AD671-750)	t_{DAV}	75		300	ns
ENCODE Falling Edge Delay	t_F	0			ns
Start New Conversion Delay	t_R	0			ns
Data and OTR Delay from DAV Falling Edge	t_{DD} [1]	20	75		ns
Data and OTR Valid before DAV Rising Edge	t_{SS} [2]	20	75		ns

NOTES

[1] t_{DD} is measured from when the falling edge of DAV crosses 0.8 V to when the output crosses 0.4 V or 2.4 V with a 25 pF load capacitor on each output pin.

[2] t_{SS} is measured from when the outputs cross 0.4 V or 2.4 V to when the rising edge of DAV crosses 2.4 V with a 25 pF load capacitor on each output pin.



a. Encode Pulse HIGH *b. Encode Pulse LOW*

Figure 1. AD671 Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
V_{CC}	ACOM	−0.5	+6.5	Volts
V_{EE}	ACOM	−6.5	+0.5	Volts
V_{LOGIC}	DCOM	−0.5	+6.5	Volts
ACOM	DCOM	−1.0	+1.0	Volts
V_{CC}	V_{LOGIC}	−6.5	+6.5	Volts
ENCODE	DCOM	−0.5	V_{LOGIC}+0.5	Volts
REF IN	ACOM	−0.5	V_{CC}+0.5	Volts
AIN, BPO/UPO	ACOM	−6.5	11.0	Volts
Junction Temperature			+175	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)		+300		°C
Power Dissipation			1000	mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



ORDERING GUIDE

Model[1]	Linearity	Temperature Range	Package Options[2]
AD671JN-500	±4 LSB	0 to +70°C	N-24
AD671KN-500	±2 LSB	0 to +70°C	N-24
AD671JD-500	±4 LSB	0 to +70°C	D-24
AD671KD-500	±2 LSB	0 to +70°C	D-24
AD671JN-750	±2 LSB	0 to +70°C	N-24
AD671KN-750	±1.5 LSB	0 to +70°C	N-24
AD671JD-750	±2 LSB	0 to +70°C	D-24
AD671KD-750	±1.5 LSB	0 to +70°C	D-24
AD671SD-500	±4 LSB	−55°C to +125°C	D-24
AD671SD-750	±2.5 LSB	−55°C to +125°C	D-24

NOTES

[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD671/883 data sheet.

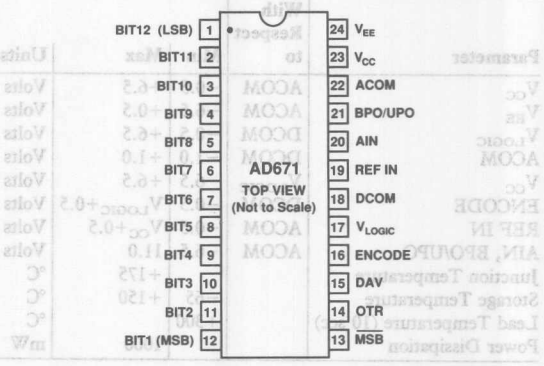
[2]D = Ceramic DIP; N = Plastic DIP. For outline information see Package Information section.

AD671 PIN DESCRIPTION

Symbol	Pin	Type	Name and Function
ACOM	22	P	Analog Ground.
AIN	20	AI	Analog Input Signal.
BIT1 (MSB)	12	DO	Most Significant Bit.
BIT2–BIT11	11–2	DO	Data Bits 2–11.
BIT12 (LSB)	1	DO	Least Significant Bit.
BPO/UPO	21	AI	Bipolar or Unipolar Configuration Pin. Connect to AIN for 0 to +5 V Span, to ACOM for 0 to +10 V Span and to REF IN for −5 V to +5 V Span.
DAV	15	DO	Data Available Output. The Rising Edge of DAV Indicates an End of Conversion and Can Be Used to Latch Current Data into an External Register. The Falling Edge of DAV Can Be Used to Latch Previous Data into an External Register.
DCOM	18	P	Digital Ground.
ENCODE	16	DI	The AD671 Starts a Conversion on the Rising Edge of the ENCODE Pulse.
$\overline{\text{MSB}}$	13	DO	Inverted Most Significant Bit. Provides Twos Complement Output Data Format.
OTR	14	DO	Out of Range Is Active HIGH when the analog input is beyond the input range of the converter.
REF IN	19	AI	+5 V Reference Input.
V_{CC}	23	P	+5 V Analog Power.
V_{EE}	24	P	−5 V Analog Power.
V_{LOGIC}	17	P	+5 V Digital Power.

TYPE:
AI = Analog Input
DI = Digital Input
DO = Digital Output
P = Power

CONNECTION DIAGRAM
PINOUT



Integral nonlinearity refers to the deviation of each individual code from a line drawn from "zero" through "full scale." The point used as "zero" occurs 1/2 LSB (1.22 mV for a 10 V span) before the first code transition (all zeros to only the LSB on). "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition (to all ones). The deviation is measured from the low side transition of each particular code to the true straight line.

DIFFERENTIAL NONLINEARITY (DNL, NO MISSING CODES)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Thus every code must have a finite width. Guaranteed no missing codes to 10-bit resolution indicates that all 1024 codes represented by Bits 1–10 must be present over all operating ranges. Guaranteed no missing codes to 11- or 12-bit resolution indicates that all 2048 and 4096 codes, respectively, must be present over all operating ranges.

UNIPOLAR OFFSET
The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual from that point. This offset can be adjusted as discussed later. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustments.

BIPOLAR ZERO
In the bipolar mode the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

should occur for an analog value 1 1/2 LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The gain error is the deviation of the actual level at the last transition from the ideal level. The gain error can be adjusted to zero as shown in Figures 7, 8 and 9.

TEMPERATURE COEFFICIENTS
The temperature coefficients for unipolar offset, bipolar zero and gain error specify the maximum change from the initial (+25°C) value to the value at T_{MIN} or T_{MAX}.

POWER SUPPLY REJECTION
The only effect of power supply error on the performance of the device will be a small change in gain. The specifications show the maximum full-scale change from the initial value with the supplies at the various limits.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

EFFECTIVE NUMBER OF BITS (ENOB)
ENOB is calculated from the expression SNR = 6.02N + 1.8 dB, where N is equal to the effective number of bits.

TOTAL HARMONIC DISTORTION (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

PEAK SPURIOUS OR PEAK HARMONIC COMPONENT
The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in decibels relative to the rms value of a full-scale input signal.

Theory of Operation

The AD671 uses a successive subranging architecture. The analog to digital conversion takes place in four independent steps or flashes. The analog input signal is subranged to an intermediate residue voltage for the final 12-bit result by utilizing multiple flashes with subtraction DACs (see the AD671 functional block diagram).

The AD671 can be configured to operate with unipolar (0 to +5 V, 0 to +10 V) or bipolar (±5 V) inputs by connecting AIN (Pin 20), REFIN (Pin 19) and BPO/UPO (Pin 21) as shown in Figure 2.

The AD671 conversion cycle begins by simply providing an active HIGH pulse on the ENCODE pin (Pin 16). The rising edge of the ENCODE pulse starts the conversion. The falling edge of the ENCODE pulse is specified to operate within a window of time: less than 30 ns after the rising edge of ENCODE (AD671-500) and less than 50 ns after the falling edge of ENCODE (AD671-750) or after the falling edge of DAV. The time window prevents digitally coupled noise from being introduced during the final stages of conversion. An internal timing generator circuit accurately controls all internal timing.

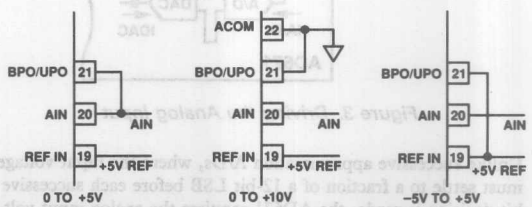


Figure 2. Input Range Connections

Upon receipt of an ENCODE command, the first 3-bit flash converts the analog input voltage. The 3-bit result is passed to a correction logic register and a segmented current output DAC. The DAC output is connected through a resistor (within the Range/Span Select Block) to AIN. A residue voltage is created by subtracting the DAC output from AIN, which is less than one eighth of the full-scale analog input. The second flash has an input range that is configured with one bit of overlap with the previous DAC. The overlap allows for errors during the flash conversion. The first residue voltage is connected to the second 3-bit flash and to the noninverting input of a high speed, differential, gain-of-four amplifier. The second flash result is passed to the correction logic register and to the second segmented current output DAC. The output of the second DAC is connected to the inverting input of the differential amplifier. The differential amplifier output is connected to a two step backend 8-bit flash. This 8-bit flash consists of coarse and fine flash converters. The result of the coarse 4-bit flash converter, also configured to overlap one bit of DAC 2, is connected to the correction logic register and selects one of 16 resistors from which the fine 4-bit flash will establish its span voltage. The fine 4-bit flash is connected directly to the output latches.

The AD671 will flag an out-of-range condition when the input voltage exceeds the analog input range. OTR (Pin 14) is active HIGH when an out of range high or low condition exists. Bits 1–12 are HIGH when the analog input voltage is greater than the selected input range and LOW when the analog input is less than the selected input range.

APPLYING THE AD671

DRIVING THE AD671 ANALOG INPUT

The AD671 uses a very high speed current output DAC to subtract a known voltage from the analog input. This results in very fast steps of current at the analog input. It is important to recognize that the signal source driving the analog input of the AD671 must be capable of maintaining the input voltage under dynamically-changing load conditions. When the AD671 starts its conversion cycle, the subtraction DAC will sink up to 5 mA (see Figure 3) from the source driving the analog input. The source must respond to this current step by settling the input voltage back to a fraction of an LSB before the AD671 makes its final 12-bit decision.

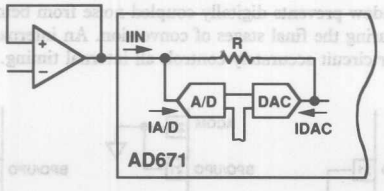


Figure 3. Driving the Analog Input

Unlike successive approximation A/Ds, where the input voltage must settle to a fraction of a 12-bit LSB before each successive bit decision is made, the AD671 requires the analog input voltage settle to within 12-bits before the third flash conversion, approximately 200 ns. This "free" 200 ns is useful in applications requiring a sample-and-hold amplifier (SHA), overlapping the SHA's hold mode settling time within the 200 ns window will increase total system throughput. See the "Discrete Sample-and-Hold" section for a high speed SHA application.

INPUT BUFFER AMPLIFIER

The closed-loop output impedance of an op amp is equal to the open loop output impedance (usually a few hundred ohms) divided by the loop gain at the frequency of interest. It is often assumed that loop gain of a follower-connected op amp is sufficiently high to reduce the closed-loop output impedance to a negligibly small value, particularly if the input signal is low frequency. At higher frequencies the open-loop gain is lower, increasing the output impedance which decreases the instantaneous analog input voltage and produces an error.

The recommended wideband, fast settling input amplifiers for use with the AD671 are the AD841, AD843, AD845 or the AD847. The AD841 is unity gain stable and recommended as a follower connected op amp. The AD843 and AD845 FET inputs make them ideal for high speed sample-and-hold amplifiers and the AD847 can be used as a low power, high speed buffer. Figure 4 shows the AD841 driving the AD671. As shown in the figure the analog input voltage should be produced with respect to the ACOM pin.

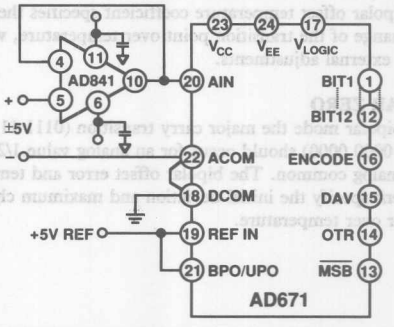


Figure 4. Input Buffer Amplifier

REFERENCE INPUT

The AD671 uses a standard +5 volt reference. The initial accuracy and temperature stability of the reference can be selected to meet specific system requirements. Like the analog input, fast switching input-dependent currents are modulated at the reference input pin (REF IN–Pin 19). However, unlike the analog input the reference input is held at a constant +5 volts with the use of capacitor. The recommended reference is the AD586, a +5 V precision reference with an output buffer amplifier. Figure 5 shows the AD671 configured in the ±5 V input range. The 6.8 μF capacitor maintains a constant +5 volts under the dynamically changing load conditions. An optional 1 μF noise reduction capacitor can be connected to the AD586, further reducing broadband output noise. To minimize ground voltage drops the AD586's ground pin should be tied as close as possible to the AD671's ACOM pin. See Figures 20, 21 and 22 for PCB layout recommendations.

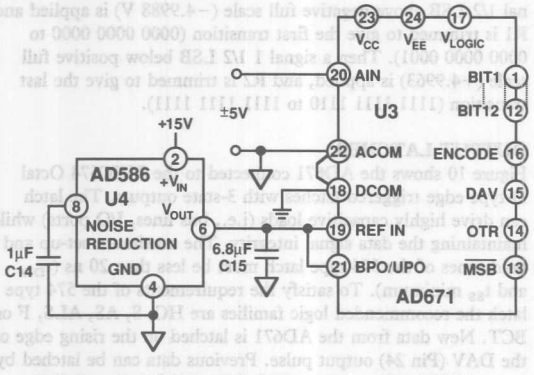


Figure 5. AD586 as Reference Input for AD671

GROUNDING AND DECOUPLING RULES

Proper grounding and decoupling should be a primary design objective in any high speed, high resolution system. The AD671 separates analog and digital grounds to optimize the management of analog and digital ground currents in a system. The AD671 is designed to minimize the current flowing from ACOM (Pin 22) by directing the majority of the current from V_{CC} (+5 V–Pin 23) to V_{EE} (−5 V–Pin 24). Minimizing analog ground currents hence reduces the potential for large ground voltage drops. This can be especially true in systems that do not utilize ground planes or wide ground runs. ACOM is also configured to be code independent, therefore reducing input dependent analog ground voltage drops and errors. The input current supplied by the external reference (REFIN–Pin 19) and the majority of the full-scale input signal (AIN–Pin 20) are also directed to V_{EE}. Also critical in any high speed digital design are the use of proper digital grounding techniques to avoid potential CMOS "ground bounce." Figure 6 is provided to assist in the proper layout, grounding and decoupling techniques.

Table I is a list of grounding and decoupling guidelines that should be reviewed before laying out a printed circuit board.

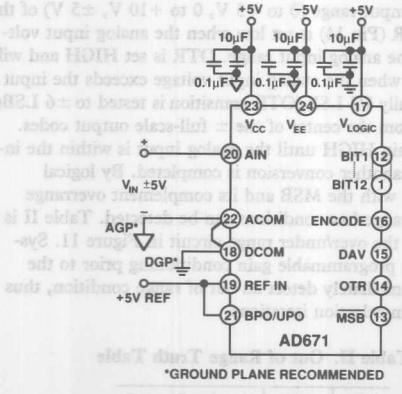


Figure 6. AD671 Grounding and Decoupling

Table I. Grounding and Decoupling Guidelines

Power Supply Decoupling	Comment
Capacitor Values	0.1 µF (Ceramic) and 10 µF (Tantalum). (Surface Mount Chip Capacitors Recommended to Reduce Lead Inductance)
Capacitor Locations	Directly at Positive and Negative Supply Pins to Respective Ground Plane.
Grounding	
Analog Ground	Ground Plane or Wide Ground Return Connected to the Analog Power Supply.
Digital Ground	Ground Plane or Wide Ground Return Connected to the Digital Power Supply.
Analog and Digital Ground	Connected Together Once at the AD671

UNIPOLAR (0 TO +10 V) CALIBRATION

The AD671 is factory trimmed to minimize offset, gain and linearity errors. In some applications the offset and gain errors of the AD671 need to be externally adjusted to zero. This is accomplished by trimming the voltage at BPO/UPO (Pin 21) and REFIN (Pin 19). In those applications the AD588, a high precision pin programmable voltage reference, is an ideal choice. The AD588 includes a reference cell and three additional amplifiers which can be configured to provide offset and gain trims for the AD671. The circuit in Figure 7 is recommended for calibrating offset and gain errors of the AD671 when configured in the 0 to +10 V input range.

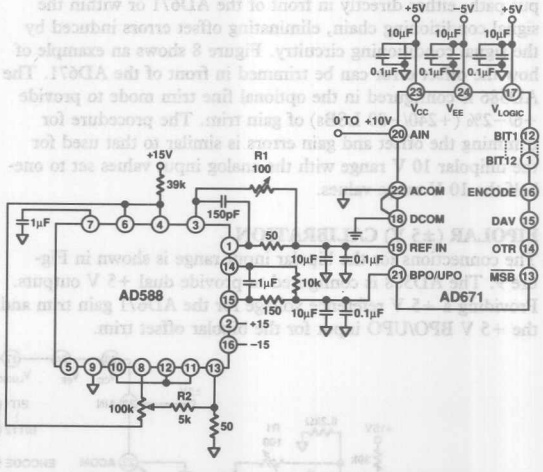


Figure 7. Unipolar (0 to +10 V) Calibration

The AD671 is intended to have a nominal 1/2 LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above it and below it). Thus, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2 LSB (1.22 mV for 10 V range). If the offset trim resistor R2 is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±50 mV of offset trim range.

The gain trim is done by applying a signal 1 1/2 LSBs below the nominal full scale (9.9963 for a 10 V range). Trim R1 to give the last transition (1111 1111 1110 to 1111 1111 1111).

UNIPOLAR (0 TO +5 V) CALIBRATION

The connections for the 0 to +5 V input range calibration is shown in Figure 8. The AD586, a +5 V precision voltage reference, is an excellent choice for this mode of operation because of its performance, stability and optional fine trim. The AD845 (16 MHz, low power, low cost op amp) is used to maintain the +5 volts under the dynamically changing load conditions of the reference input.

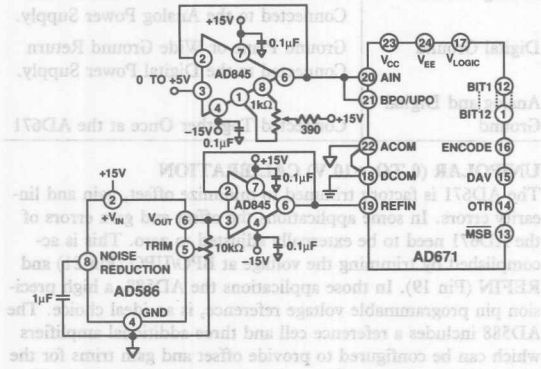


Figure 8. Unipolar (0 to +5 V) Calibration

The AD671 offset error must be trimmed within the analog input path, either directly in front of the AD671 or within the signal conditioning chain, eliminating offset errors induced by the signal conditioning circuitry. Figure 8 shows an example of how the offset error can be trimmed in front of the AD671. The AD586 is configured in the optional fine trim mode to provide +6/−2% (+240/−80 LSBs) of gain trim. The procedure for trimming the offset and gain errors is similar to that used for the unipolar 10 V range with the analog input values set to one-half the 10 V range values.

BIPOLAR (±5 V) CALIBRATION

The connections for the bipolar input range is shown in Figure 9. The AD588 is configured to provide dual +5 V outputs. Providing a +5 V reference voltage for the AD671 gain trim and the +5 V BPO/UPO input for the bipolar offset trim.

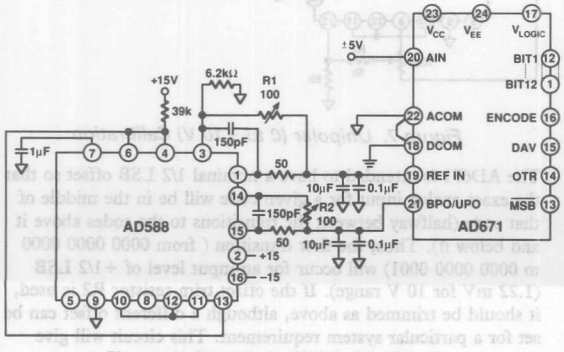


Figure 9. Bipolar (±5 V) Calibration

Bipolar calibration is similar to unipolar calibration. First, a signal 1/2 LSB above negative full scale (−4.9988 V) is applied and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1 1/2 LSB below positive full scale (+4.9963) is applied, and R2 is trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

OUTPUT LATCHES

Figure 10 shows the AD671 connected to the 74HC574 Octal D-type edge triggered latches with 3-state outputs. The latch can drive highly capacitive loads (i.e., bus lines, I/O ports) while maintaining the data signal integrity. The maximum set-up and hold times of the 574 type latch must be less than 20 ns (t_{DD} and t_{SS} minimum). To satisfy the requirements of the 574 type latch the recommended logic families are HC, S, AS, ALS, F or BCT. New data from the AD671 is latched on the rising edge of the DAV (Pin 24) output pulse. Previous data can be latched by inverting the DAV output with a 7404 type inverter. See Figures 20, 21 and 22 for PCB layout recommendations.

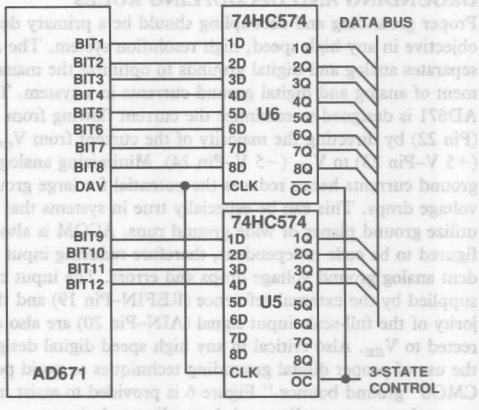


Figure 10. AD671 to Output Latches

OUT OF RANGE

An Out of Range condition exists when the analog input voltage is beyond the input range (0 to +5 V, 0 to +10 V, ±5 V) of the converter. OTR (Pin 14) is set low when the analog input voltage is within the analog input range. OTR is set HIGH and will remain HIGH when the analog input voltage exceeds the input range by typically 1/2 LSB (OTR transition is tested to ±6 LSBs of accuracy) from the center of the ± full-scale output codes. OTR will remain HIGH until the analog input is within the input range and another conversion is completed. By logical ANDing OTR with the MSB and its complement overrange high or underrange low conditions can be detected. Table II is a truth table for the over/under range circuit in Figure 11. Systems requiring programmable gain conditioning prior to the AD671 can immediately detect an out of range condition, thus eliminating gain selection iterations.

Table II. Out of Range Truth Table

OTR	MSB	Analog Input Is
0	0	In Range
0	1	In Range
1	0	Underrange
1	1	Overrange

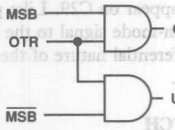


Figure 11. Overrange or Underrange Logic

OUTPUT DATA FORMAT

The AD671 provides both MSB and $\overline{MSB}$ outputs, delivering data in positive true straight binary for unipolar input ranges and positive true offset binary or twos complement for bipolar input ranges. Straight binary coding is used for systems that accept positive-only signals. If straight binary coding is used with bipolar input signals a 0 V input would result in a binary output of 2048. The application software would have to subtract 2048 to determine the true input voltage. Most processors typically perform math on signed integers and assume data is in that format. Twos complement format minimizes software overhead which is especially important in high speed data transfers, such as a DMA operation. The CPU is not bogged down performing data conversion steps, hence increasing the total system throughput.

2

Table III. Output Data Format

Input Range	Coding	Analog Input[1]	Digital Output	OTR[2]
0 to +5 V	Straight Binary	≤−0.00061 V	0000 0000 0000	1
		0 V	0000 0000 0000	0
		+5 V	1111 1111 1111	0
		≥+5.00061 V	1111 1111 1111	1
0 to +10 V	Straight Binary	≤−0.00122 V	0000 0000 0000	1
		0 V	0000 0000 0000	0
		+10 V	1111 1111 1111	0
		≥+10.00122 V	1111 1111 1111	1
−5 V to +5 V	Offset Binary	≤−5.00122 V	0000 0000 0000	1
		−5 V	0000 0000 0000	0
		0 V	1000 0000 0000	0
		+4.99756 V	1111 1111 1111	0
		≥ +4.99878 V	1111 1111 1111	1
−5 V to +5 V	2s Complement (Using $\overline{MSB}$)	≤−5.00122 V	1000 0000 0000	1
		−5 V	1000 0000 0000	0
		0 V	0000 0000 0000	0
		+4.99756 V	0111 1111 1111	0
		≥ +4.99878 V	0111 1111 1111	1

NOTES
[1]Voltages listed are with offset and gain errors adjusted to zero.
[2]Typical performance.

I_{LOGIC} vs. CONVERSION RATE

Figure 12 shows the typical logic supply current vs. conversion rate for various capacitive loads on the digital outputs.

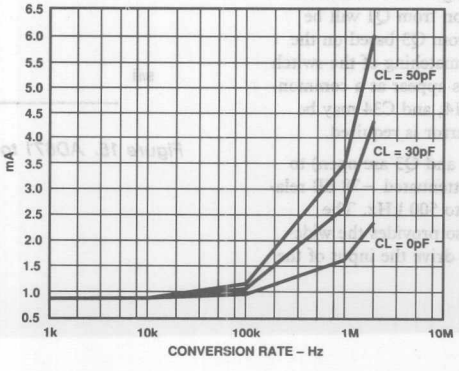


Figure 12. I_{LOGIC} vs. Conversion Rate for Various Capacitive Loads on the Digital Outputs

HIGH PERFORMANCE SAMPLE-AND-HOLD AMPLIFIER (SHA)

In order to take full advantage of the AD671's high speed capabilities, a sample-and-hold amplifier (SHA) with fast acquisition capabilities and rigid accuracy requirements is essential. One possibility is a hybrid SHA such as the HTC-0300A, but often a cost effective alternative like the one shown in Figure 13 may be a better solution. This discrete SHA requires very few components and is able to acquire signals to 0.01% accuracy in less than 350 nanoseconds. Combined with the AD671, signals with bandwidths up to 500 kHz can be converted with 12-bit accuracy.

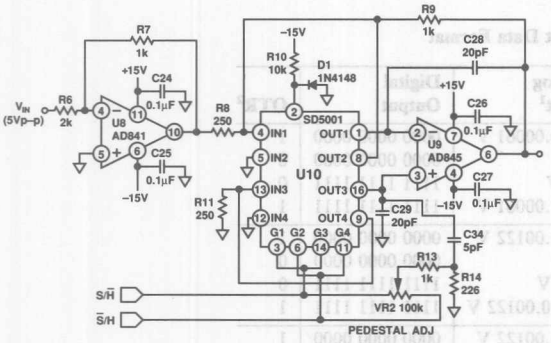


Figure 13. Discrete High Speed Sample-and-Hold Amplifier

CIRCUIT DESCRIPTION

The discrete SHA shown in Figure 13 is a closed-loop, noninverting architecture which accepts 5 V p–p inputs. The overall gain of the SHA is +2 in order to accommodate the 10 V input span of the AD671. The AD841, with a 0.01% settling time of 110 ns, is the suggested input buffer to the SHA. The circuit also employs a SD5001 which contains four ultrahigh speed DMOS switches (Q1–Q4). The high CMRR, low input offset current, and fast settling time of the AD845 op amp are all critical features necessary for optimal performance of the discrete SHA.

In sample mode, Q1 and Q3 of the SD5001 are closed (Q2 and Q4 are open). C28 is charged to the input voltage level at a rate primarily determined by the time constant, R9 · C28. Simultaneously, C29 is connected to ground through a 250 ohm resistor. If C28 is equal to C29, charge injection from Q1 will be approximately equal to charge injection from Q3 based on the symmetry of the circuit and the inherent matching of the switch capacitances. The resultant pedestal errors appear as a common-mode signal to the AD845. VR2, R13, R14, and C34 may be included if further reduction of pedestal error is required.

In hold mode, Q2 and Q4 are closed (Q1 and Q3 are open) to reduce feedthrough. The input signal is attenuated −78 dB relative to the input signal at frequencies up to 500 kHz. The AD845 buffers the voltage on C28 and also provides the wideband, low-impedance output necessary to drive the input of the AD671.

Droop, which occurs as a result of leakage currents, will appear on C28 and will similarly appear on C29. Like pedestal errors, droop appears as a common-mode signal to the AD845 and is greatly reduced by the differential nature of the circuit. Voltage droop is typically 5 µV/µs.

CROSS COUPLED LATCH

As noted in the Theory of Operation, the ENCODE pulse is specified to operate within a window of time. The circuit in Figure 14 can be used to generate a valid ENCODE pulse if a clock pulse width of greater than 30 ns is available.

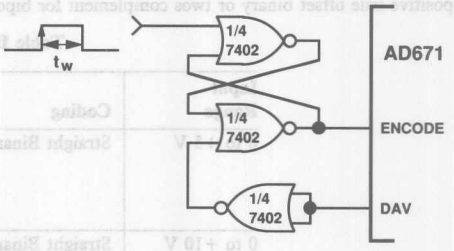


Figure 14. Cross Coupled Latch

TIMING DESCRIPTION

Figure 15 shows the timing requirements for the discrete SHA.

The complementary S/H inputs are HCMOS-compatible although larger gate voltages will improve performance by lowering the on resistances of the DMOS switches. It should be noted that a conversion is started before the SHA has settled to 0.01% accuracy. The discrete SHA takes advantage of the fact that the AD671 does not require a 12-bit accurate input until it is 150 ns into its conversion cycle. See Figures 21, 22 and 23 for PCB layout recommendations.

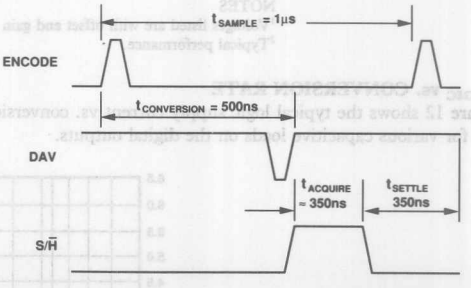


Figure 15. AD671 to Discrete SHA Timing Diagram

DYNAMIC PERFORMANCE

In most sampling applications the dynamic performance of the system is limited by the performance of the SHA. The SHA's dynamic performance can be selected to meet the system sampling requirements. Figures 16 and 17 are typical FFT plots using the discrete SHA in Figure 13.

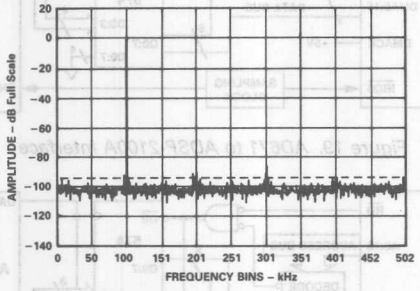


Figure 16. Typical FFT Plot of AD671 and Discrete SHA F_{IN} = 100 kHz

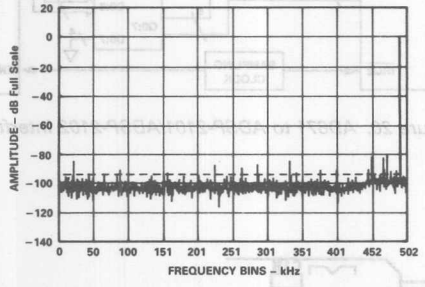


Figure 17. Typical FFT Plot of AD671 and Discrete SHA F_{IN} = 500 kHz

DYNAMIC CHARACTERISTICS

(@ +25°C, tested using the discrete SHA in Figure 15 with V_{CC} = +5 V, V_{LOGIC} = +5 V, V_{EE} = −5 V, f_{SAMPLE} = 1 MSPS)[1]

Model	AD671JD-500 Typ	Units
Effective Number of Bits (ENOB)		
F_{IN} = 100 kHz	11.3	Bits
F_{IN} = 490 kHz	11.2	Bits
Signal-to-Noise and Distortion (S/N+D) Ratio		
F_{IN} = 100 kHz	70	dB
F_{IN} = 490 kHz	68	dB
Total Harmonic Distortion (THD)		
F_{IN} = 100 kHz	−80	dB
F_{IN} = 490 kHz	−75	dB
Peak Spurious (dc to 490 kHz)	−79	dB
Peak Harmonic Component (dc to 490 kHz)	−76	dB

NOTE

[1]f_{IN} amplitude = −0.2 dB @100 kHz and −0.9 dB @ 490 kHz, bipolar mode unless otherwise indicated. See Definition of Specifications for additional information.

MULTICHANNNEL DATA ACQUISITION SYSTEM

The AD684, a quad high speed sample-and-hold amplifier is ideally suited for multichannel data acquisition applications. Figure 18 shows a typical data acquisition circuit using the AD684 (SHA), ADG201HS (Multiplexer), AD588 (Reference) and the AD671. The AD684 is configured to simultaneously sample four analog inputs. Each held analog input voltage can be selected by the multiplexer and buffered by the AD841. The AD671 is connected in the bipolar input range (±5 V).

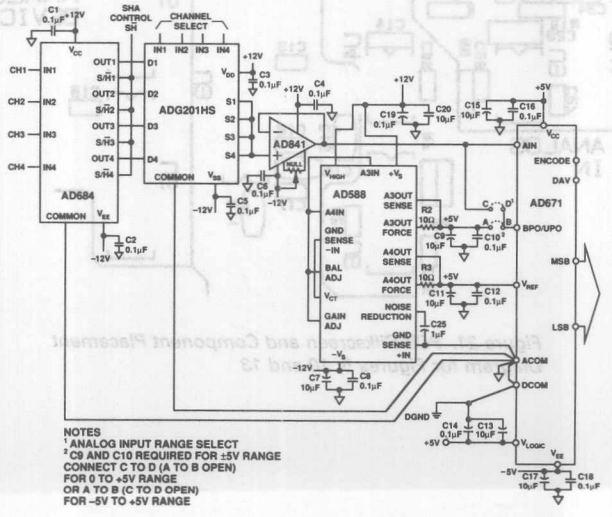


Figure 18. Data Acquisition System Using the AD684 and the AD671

AD671 TO ADSP-2100A INTERFACE

Figure 19 demonstrates the AD671 to ADSP-2100A interface. The 2100A with a clock frequency of 12.5 MHz can execute an instruction in one 80 ns cycle. The AD671 is configured to perform continuous time sampling. The DAV output of the AD671 is asserted at the end of each conversion. DAV can be used to latch the conversion result into the two 574 octal D-latches. The falling edge of the sampling clock is used to generate an interrupt (IRQ3) for the processor. Upon interrupt, the ADSP-2100A starts a data memory read by providing an address on the DMA bus. The decoded address generates OE for the latches and the processor reads their output over the DMA bus. The conversion result is read within a single processor cycle.

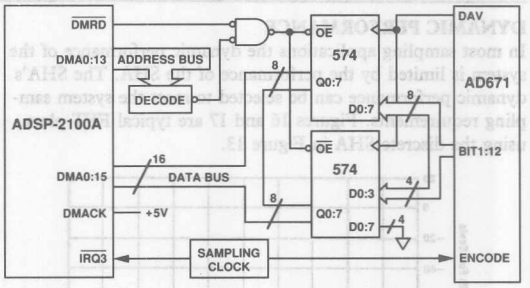


Figure 19. AD671 to ADSP-2100A Interface

AD671 TO ADSP-2101/ADSP-2102 INTERFACE

Figure 20 is identical to the 2100A interface except the sampling clock is used to generate an interrupt (IRQ2) for the processor. Upon interrupt the ADSP-2101A starts a data memory read by providing an address on the Address (A) bus. The decode address generates $\overline{OE}$ for the D-latches and the processor reads their output over the Data (D) bus. Reading the conversion result is thus completed within a single processor cycle.

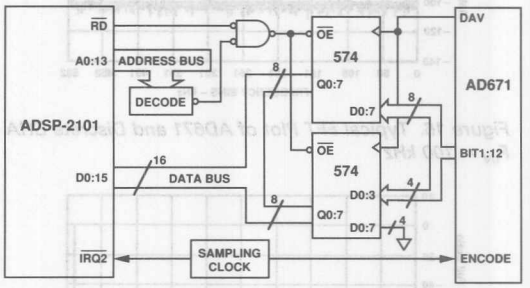


Figure 20. AD671 to ADSP-2101/ADSP-2102 Interface

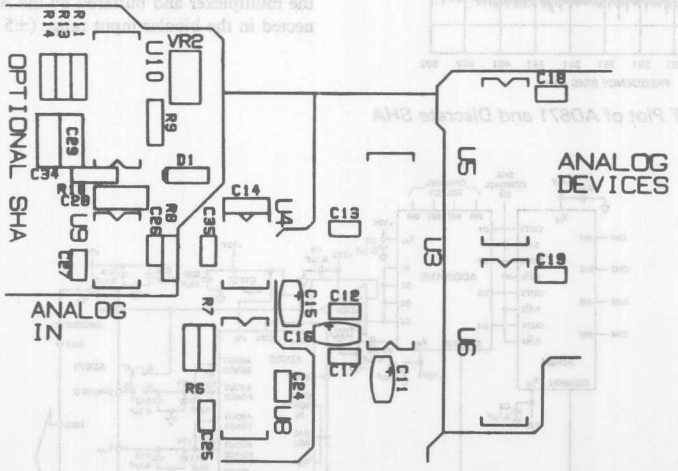


Figure 21. PCB Silkscreen and Component Placement Diagram for Figures 5, 10 and 13

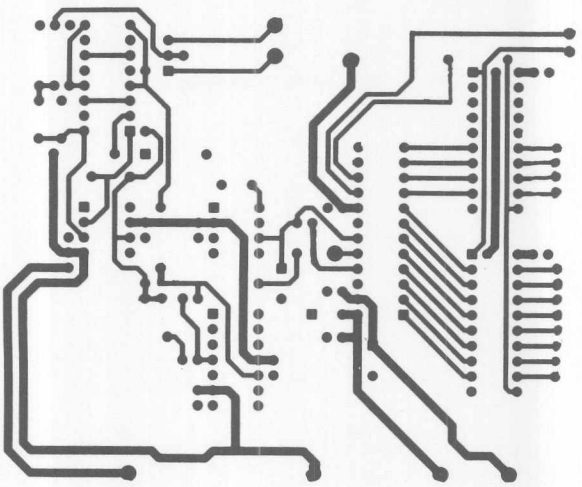


Figure 22. PCB Solder Side Layout for Figures 5, 10 and 13

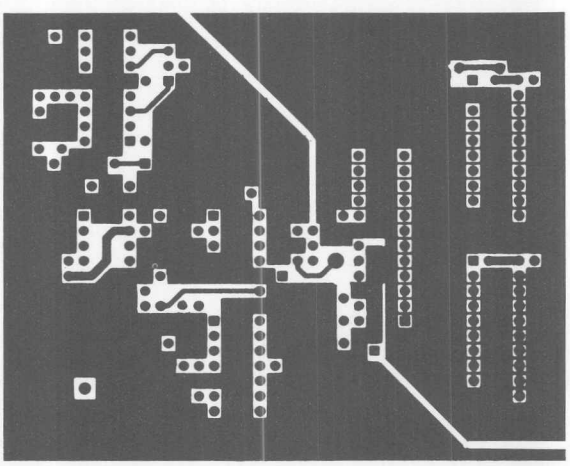
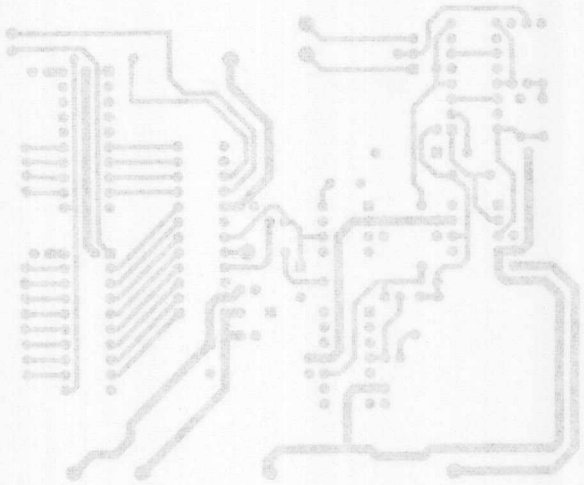
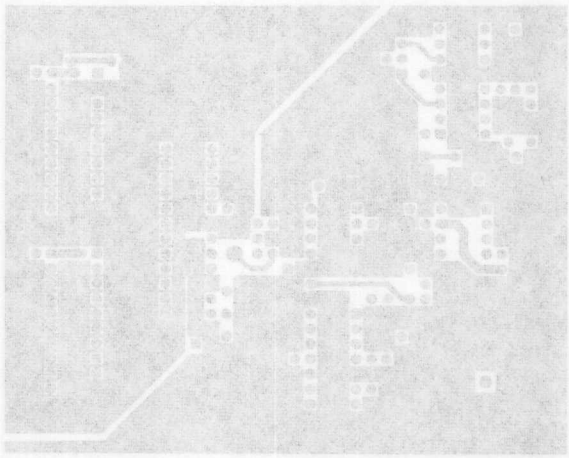


Figure 23. PCB Component Side Layout for Figures 5, 10 and 13





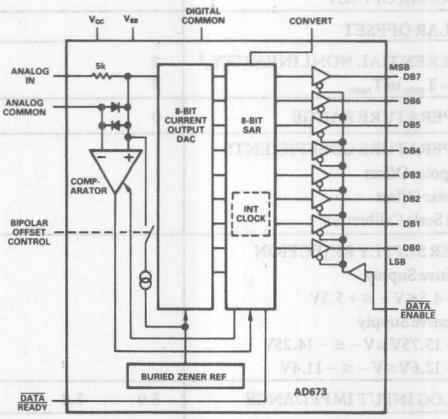
8-Bit A/D Converter

AD673*

FEATURES

- Complete 8-Bit A/D Converter with Reference, Clock and Comparator
- 30μs Maximum Conversion Time
- Full 8- or 16-Bit Microprocessor Bus Interface
- Unipolar and Bipolar Inputs
- No Missing Codes Over Temperature
- Operates on +5V and −12V to −15V Supplies
- MIL-STD-883 Compliant Version Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD673 is a complete 8-bit successive approximation analog-to-digital converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register (SAR) and 3 state output buffers–all fabricated on a single chip. No external components are required to perform a full accuracy 8-bit conversion in 20μs.

The AD673 incorporates advanced integrated circuit design and processing technologies. The successive approximation function is implemented with I^2L (integrated injection logic). Laser trimming of the high stability SiCr thin film resistor ladder network insures high accuracy, which is maintained with a temperature compensated sub-surface Zener reference.

Operating on supplies of +5V and −12V to −15V, the AD673 will accept analog inputs of 0 to +10V or −5V to +5V. The trailing edge of a positive pulse on the CONVERT line initiates the 20μs conversion cycle. $\overline{\text{DATA READY}}$ indicates completion of the conversion.

The AD673 is available in two versions. The AD673J as specified over the 0 to +70°C temperature range and the AD673S guarantees ±½LSB relative accuracy and no missing codes from −55°C to +125°C.

Two package configurations are offered. All versions are also offered in a 20-pin hermetically sealed ceramic DIP. The AD673J is also available in a 20-pin plastic DIP.

PRODUCT HIGHLIGHTS

1. The AD673 is a complete 8-bit A/D converter. No external components are required to perform a conversion.
2. The AD673 interfaces to many popular microprocessors without external buffers or peripheral interface adapters.
3. The device offers true 8-bit accuracy and exhibits no missing codes over its entire operating temperature range.
4. The AD673 adapts to either unipolar (0 to +10V) or bipolar (−5V to +5V) analog inputs by simply grounding or opening a single pin.
5. Performance is guaranteed with +5V and −12V or −15V supplies.
6. The AD673 is available in a version compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD673/883B data sheet for detailed specifications.

***Protected by U.S. Patent Nos. 3,940,760; 4,213,806; 4,136,349; 4,400,689; and 4,400,690**

AD673—SPECIFICATIONS (T_A = 25°C, V+ = +5V, V− = −12V or −15V, all voltages measured with respect to digital common, unless otherwise indicated.)

Model	AD673J Min	AD673J Typ	AD673J Max	AD673S Min	AD673S Typ	AD673S Max	Units
RESOLUTION		8			8		Bits
RELATIVE ACCURACY,[1]			±1/2			±1/2	LSB
$T_A = T_{min}$ to T_{max}			±1/2			±1/2	LSB
FULL SCALE CALIBRATION[2]		±2			±2		LSB
UNIPOLAR OFFSET			±1/2			±1/2	LSB
BIPOLAR OFFSET			±1/2			±1/2	LSB
DIFFERENTIAL NONLINEARITY,[3]	8			8			Bits
$T_A = T_{min}$ to T_{max}	8			8			Bits
TEMPERATURE RANGE	0		+70	−55		+125	°C
TEMPERATURE COEFFICIENTS							
Unipolar Offset			±1			±1	LSB
Bipolar Offset			±1			±1	LSB
Full Scale Calibration[2]			±2			±2	LSB
POWER SUPPLY REJECTION							
Positive Supply							
+4.5≤V+≤+5.5V			±2			±2	LSB
Negative Supply							
−15.75V≤V−≤−14.25V			±2			±2	LSB
−12.6V≤V−≤−11.4V			±2			±2	LSB
ANALOG INPUT IMPEDANCE	3.0	5.0	7.0	3.0	5.0	7.0	kΩ
ANALOG INPUT RANGES							
Unipolar	0		+10	0		+10	V
Bipolar	−5		+5	−5		+5	V
OUTPUT CODING							
Unipolar	Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT							
Output Sink Current							
(V_{OUT} = 0.4V max, T_{min} to T_{max})	3.2			3.2			mA
Output Source Current[4]							
(V_{OUT} = 2.4V min, T_{min} to T_{max})	0.5			0.5			mA
Output Leakage			±40			±40	μA
LOGIC INPUTS							
Input Current			±100			±100	μA
Logic "1"	2.0			2.0			V
Logic "0"			0.8			0.8	V
CONVERSION TIME, T_A and T_{min} to T_{max}	10	20	30	10	20	30	μs
POWER SUPPLY							
V+	+4.5	+5.0	+7.0	+4.5	+5.0	+7.0	V
V−	−11.4	−15	−16.5	−11.4	−15	−16.5	V
OPERATING CURRENT							
V+		15	20		15	20	mA
V−		9	15		9	15	mA

NOTES

[1]Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[2]Full scale calibration is guaranteed trimmable to zero with an external 200Ω potentiometer in place of the 15Ω fixed resistor.
Full scale is defined as 10 volts minus 1LSB, or 9.961 volts.

[3]Defined as the resolution for which no missing codes will occur.

[4]The data output lines have active pull-ups to source 0.5mA. The DATA READY line is open collector with a nominal 6kΩ internal pull-up resistor.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common	0 to +7V
V− to Digital Common	0 to −16.5V
Analog Common to Digital Common	±1V
Analog Input to Analog Common	±15V
Control Inputs	0 to V+
Digital Outputs (High Impedance State)	0 to V+
Power Dissipation	800mW

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Package Option[1]
AD673JN	0 to +70°C	±1/2LSB max	Plastic DIP (N-20)
AD673JD	0 to +70°C	±1/2LSB max	Ceramic DIP (D-20)
AD673SD[2]	−55°C to +125°C	±1/2LSB max	Ceramic DIP (D-20)
AD673JP	0 to +70°C	±1/2LSB max	PLCC (P-20A)

NOTES
[1]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.
[2]For details on grade and package offering screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook.

2

FUNCTIONAL DESCRIPTION

A block diagram of the AD673 is shown in Figure 1. The positive CONVERT pulse must be at least 500ns wide. $\overline{DR}$ goes high within 1.5μs after the leading edge of the convert pulse indicating that the internal logic has been reset. The negative edge of the CONVERT pulse initiates the conversion. The internal 8-bit current output DAC is sequenced by the integrated injection logic (I^2L) successive approximation register (SAR) from its most significant bit to least significant bit to provide an output current which accurately balances the input signal current through the 5kΩ resistor. The comparator determines whether the addition of each successively weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is more, the bit is turned off. After testing all bits, the SAR contains a 8-bit binary code which accurately represents the input signal to within (0.05% of full scale).

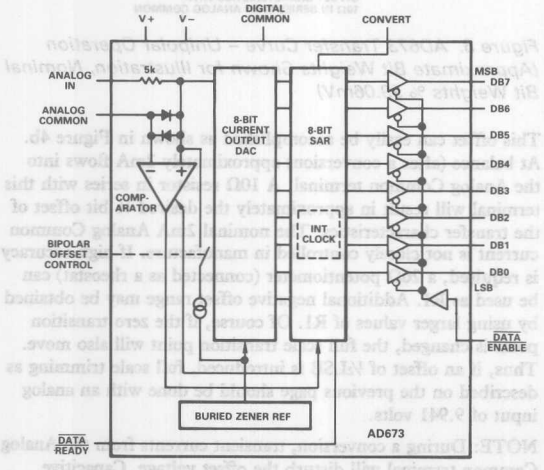


Figure 1. AD673 Functional Block Diagram

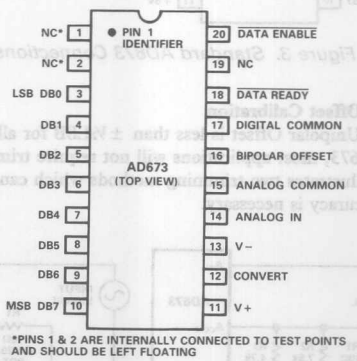
The SAR drives $\overline{DR}$ low to indicate that the conversion is complete and that the data is available to the output buffers. $\overline{DATA\ ENABLE}$ can then be activated to enable the 8-bits of data desired. $\overline{DATA\ ENABLE}$ should be brought high prior to the next conversion to place the output buffers in the high impedance state.

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and ensures excellent stability with both time and temperature. The bipolar offset input controls a switch which allows the positive bipolar offset current (exactly equal to the value of the MSB less ½LSB) to be injected into the summing (+) node of the comparator to offset the DAC output. Thus the nominal 0 to +10V unipolar input range becomes a −5V to +5V range. The 5kΩ thin film input resistor is trimmed so that with a full scale input signal, an input current will be generated which exactly matches the DAC output with all bits on.

UNIPOLAR CONNECTION

The AD673 contains all the active components required to perform a complete A/D conversion. Thus, for many applications, all that is necessary is connection of the power supplies (+5V and −12V to −15V), the analog input and the convert pulse. However, there are some features and special connections which should be considered for achieving optimum performance. The functional pin-out is shown in Figure 2.

The standard unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin (pin 16) to digital common (pin 17).



*PINS 1 & 2 ARE INTERNALLY CONNECTED TO TEST POINTS AND SHOULD BE LEFT FLOATING

Figure 2. AD673 Pin Connections

Full Scale Calibration

The 5kΩ thin film input resistor is laser trimmed to produce a current which matches the full scale current of the internal DAC–plus about 0.3%–when an analog input voltage of 9.961 volts (10 volts – 1LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 9.961 volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to pin 14. Typical full scale calibration error will then be within ±2LSB or ±0.8%. If more precise calibration is desired, a 200Ω trimmer should be used instead. Set the analog input at 9.961 volts, and set the trimmer so that the output code is just at the transition between 111111 10 and 11111111. Each LSB will then have a weight of 39.06mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have a weight of exactly 40.0mV), a 100Ω resistor and a 100Ω trimmer (or a 200Ω trimmer with good resolution) should be used. Of course, larger full scale ranges can be arranged by using a larger input resistor, but linearity and full scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5kΩ. Figure 3 illustrates the connections required for full scale calibration.

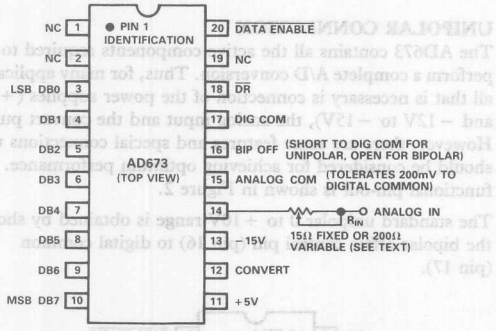


Figure 3. Standard AD673 Connections

Unipolar Offset Calibration

Since the Unipolar Offset is less than ±½LSB for all versions of the AD673, most applications will not require trimming. Figure 4 illustrates two trimming methods which can be used if greater accuracy is necessary.

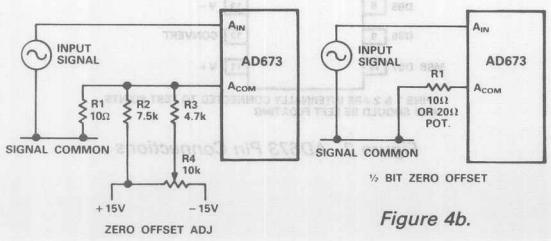


Figure 4a.

Figure 4b.

Figure 4. Unipolar Offset Trimming

Figure 4a shows how the converter zero may be offset to correct for initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode.

Figure 5 shows the nominal transfer curve near zero for an AD673 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics.

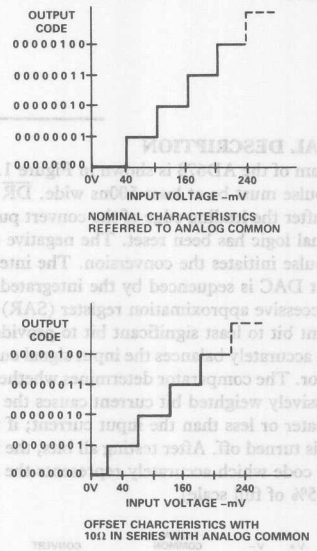


Figure 5. AD673 Transfer Curve – Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights % 39.06mV)

This offset can easily be accomplished as shown in Figure 4b. At balance (after a conversion) approximately 2mA flows into the Analog Common terminal. A 10Ω resistor in series with this terminal will result in approximately the desired ½ bit offset of the transfer characteristics. The nominal 2mA Analog Common current is not closely controlled in manufacture. If high accuracy is required, a 20Ω potentiometer (connected as a rheostat) can be used as R1. Additional negative offset range may be obtained by using larger values of R1. Of course, if the zero transition point is changed, the full scale transition point will also move. Thus, if an offset of ½LSB is introduced, full scale trimming as described on the previous page should be done with an analog input of 9.941 volts.

NOTE: During a conversion, transient currents from the Analog Common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle appropriately during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling, which returns to analog signal common, should go to the signal input side of the resistive offset network.

BIPOLAR CONNECTION

To obtain the bipolar −5V to +5V range with an offset binary output code, the bipolar offset control pin is left open.

A −5.00 volt signal will give a 8-bit code of 00000000; an input of 0.00 volts results in an output code of 10000000 and +4.961 volts at the input yields the 11111111 code. The nominal transfer curve is shown in Figure 6.

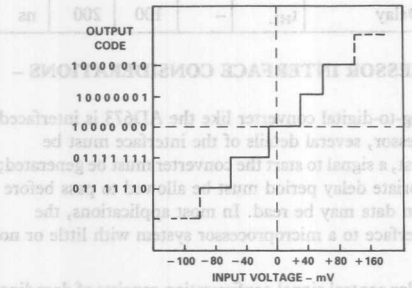


Figure 6. AD673 Transfer Curve–Bipolar Operation

Note that in the bipolar mode, the code transitions are offset ¼LSB such that an input voltage of 0 volts −5mV to +35mV yields the code representing zero (10000000). Each output code is then *centered* on its nominal input voltage.

Full Scale Calibration

Full Scale Calibration is accomplished in the same manner as in Unipolar operation except the full scale input voltage is +4.61 volts.

Negative Full Scale Calibration

The circuit in Figure 4a can also be used in Bipolar operation to offset the input voltage (nominally −5V) which results in the 000000 00 code. R2 should be omitted to obtain a symmetrical range.

The bipolar offset control input is not directly TTL compatible but a TTL interface for logic control can be constructed as shown in Figure 7.

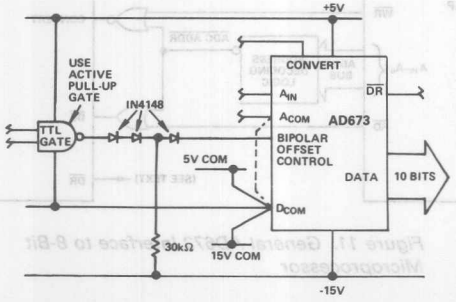


Figure 7. Bipolar Offset Controlled by Logic Gate
Gate Output = 1 Unipolar 0–10V Input Range
Gate Output = 0 Bipolar ±5V Input Range

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD673

Many situations in high-speed acquisition systems or digitizing rapidly changing signals require a sample-hold amplifier (SHA) in front of the A-D converter. The SHA can acquire and hold a signal faster than the converter can perform a conversion. A SHA can also be used to accurately define the exact point in time at which the signal is sampled. For the AD673, a SHA can also serve as a high input impedance buffer.

Figure 8 shows the AD673 connected to the AD582 monolithic SHA for high speed signal acquisition. In this configuration, the AD582 will acquire a 10 volt signal in less than 10μs with a droop rate less than 100μV/ms.

$\overline{DR}$ goes high after the conversion is initiated to indicate that reset of the SAR is complete. In Figure 8 it is also used to put the AD582 into the hold mode while the AD673 begins its conversion cycle. (The AD582 settles to final value well in advance of the first comparator decision inside the AD673).

$\overline{DR}$ goes low when the conversion is complete placing the AD582 back in the sample mode. Configured as shown in Figure 8, the next conversion can be initiated after a 10μs delay to allow for signal acquisition by the AD582.

Observe carefully the ground, supply, and bypass capacitor connections between the two devices. This will minimize ground noise and interference during the conversion cycle.

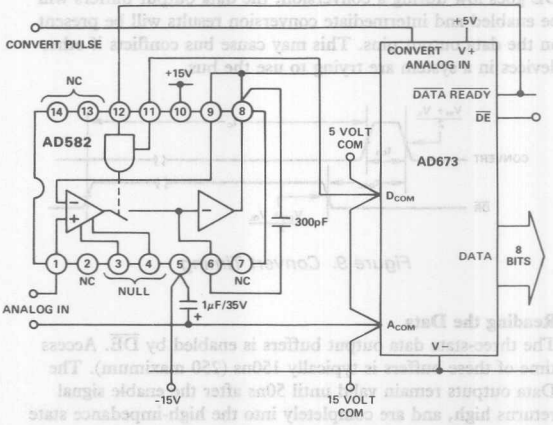


Figure 8. Sample-Hold Interface to the AD673

GROUNDING CONSIDERATIONS

The AD673 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200mV of common mode voltage between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation, the Analog Common terminal may generate transient currents of up to 2mA during a conversion. In addition a static current of about 2mA will flow into Analog Common in the unipolar mode after a conversion is complete. The Analog Common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 volt. It is recommended that a parallel pair of back-to-back protection diodes be connected between the commons if they are not connected locally.

CONTROL AND TIMING OF THE AD673

The operation of the AD673 is controlled by two inputs: CONVERT and $\overline{\text{DATA ENABLE}}$.

Starting a Conversion

The conversion cycle is initiated by a positive-going CONVERT pulse at least 500ns wide. The rising edge of this pulse resets the internal logic, clears the result of the previous conversion, and sets $\overline{\text{DR}}$ high. The falling edge of CONVERT begins the conversion cycle. When conversion is completed $\overline{\text{DR}}$ returns low. During the conversion cycle, $\overline{\text{DE}}$ should be held high. If $\overline{\text{DE}}$ goes low during a conversion, the data output buffers will be enabled and intermediate conversion results will be present on the data output pins. This may cause bus conflicts if other devices in a system are trying to use the bus.

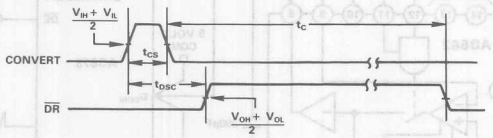


Figure 9. Convert Timing

Reading the Data

The three-state data output buffers is enabled by $\overline{\text{DE}}$. Access time of these buffers is typically 150ns (250 maximum). The Data outputs remain valid until 50ns after the enable signal returns high, and are completely into the high-impedance state 100ns later.

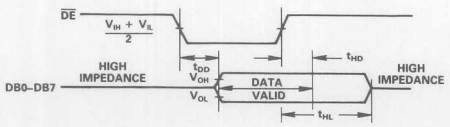


Figure 10. Read Timing

TIMING SPECIFICATIONS

Parameter	Symbol	Min	Typ	Max	Units
CONVERT Pulse Width	t_{CS}	500	–	–	ns
$\overline{\text{DR}}$ Delay from CONVERT	t_{DSC}	–	1	1.5	µs
Conversion Time	t_C	10	20	30	µs
Data Access Time	t_{DD}	0	150	250	ns
Data Valid after $\overline{\text{DE}}$ High	t_{HD}	50	–	–	ns
Output Float Delay	t_{HL}	–	100	200	ns

MICROPROCESSOR INTERFACE CONSIDERATIONS – GENERAL

When an analog-to-digital converter like the AD673 is interfaced to a microprocessor, several details of the interface must be considered. First, a signal to start the converter must be generated; then an appropriate delay period must be allowed to pass before valid conversion data may be read. In most applications, the AD673 can interface to a microprocessor system with little or no external logic.

The most popular control signal configuration consists of decoding the address assigned to the AD673, then gating this signal with the system's WR signal to generate the CONVERT pulse, and gating it with RD to enable the output buffers. The use of a memory address and memory WR and RD signals denotes "memory-mapped" I/O interfacing, while the use of a separate I/O address space denotes "isolated I/O" interfacing.

Figure 11 shows a generalized diagram of the control logic for an AD673 interfaced to an 8-bit data bus, where an address ADC ADDR has been decoded. ADC ADDR starts the converter when written to (the actual data being written to the converter does not matter) and contains the high byte data during read operations.

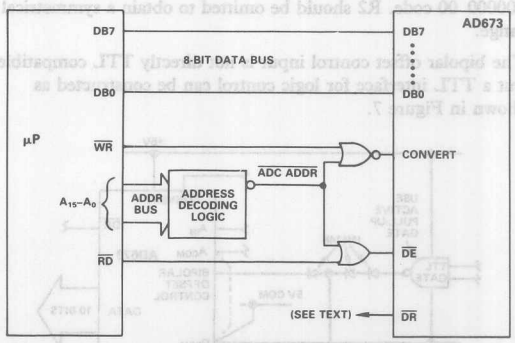


Figure 11. General AD673 Interface to 8-Bit Microprocessor

In systems where this read-write interface is used, at least 30 microseconds (the maximum conversion time) must be allowed to pass between starting a conversion and reading the results. This delay or "timeout" period can be implemented in a short software routine such as a countdown loop, enough dummy instructions to consume 30 microseconds, or enough actual useful instructions to consume the required time. In tightly-timed systems, the $\overline{DR}$ line may be read through an external three-state buffer to determine precisely when a conversion is complete. Higher-speed systems may choose to use $\overline{DR}$ to signal an interrupt to the processor at the end of a conversion.

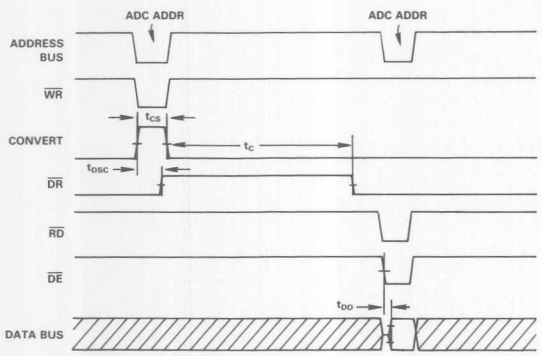


Figure 12. Typical AD673 Timing Diagram

CONVERT Pulse Generation

The AD673 is tested with a CONVERT pulse width of 500ns and will typically operate with a pulse as short as 300ns. However, some microprocessors produce active WR pulses which are shorter than this. Either of the circuits shown in Figure 13 can be used to generate an adequate CONVERT pulse for the AD673. In both circuits, the short low-going WR pulse sets the CONVERT line high through a flip-flop. The rising edge of $\overline{DR}$ (which signifies that the internal logic has been reset) resets the flip-flop and brings CONVERT low, which starts the conversion.

Note that t_{DSC} is slightly longer when the result of the previous conversion contains a logic 1 on the LSB. This means that the actual CONVERT pulse generated by the circuits in Figure 13 will vary slightly in width.

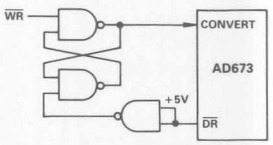


Figure 13a. Using 74LS00

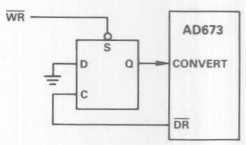


Figure 13b. Using 1/2 74LS74

12-Bit A/D Converter

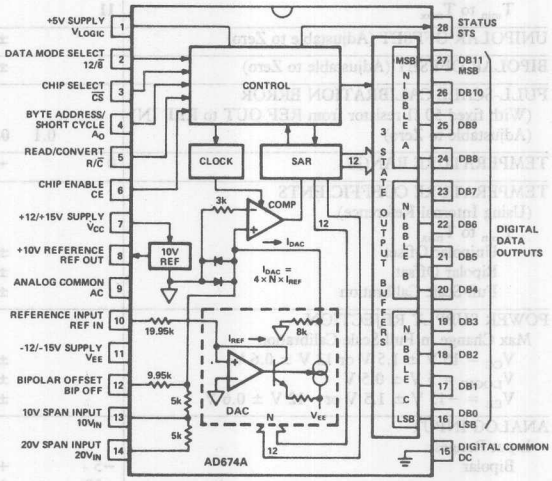
AD674A*

FEATURES

Complete 12-Bit A/D Converter with Reference and Clock
Faster Version of AD574A
8- and 16-Bit Bus Interface
No Missing Codes Over Temperature
15 μs max Conversion Time
±12 V and ±15 V Operation
Unipolar and Bipolar Inputs

NOT RECOMMENDED FOR NEW DESIGNS, REPLACE WITH AD674B (SEE PAGE 2–109)

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD674A is a complete 12-bit successive-approximation analog-to-digital converter with three-state output buffer circuitry for direct interface to an 8- and 16-bit microprocessor bus. A high-precision voltage reference and clock are included on-chip, and the circuit requires only power supplies and control signals for operation.

The AD674A is pin compatible with the industry-standard AD574A but offers faster conversion time and bus-access speed.

The AD674A design is implemented with two LSI chips each containing both analog and digital circuitry, resulting in the maximum performance and flexibility at the lowest cost. The chips are laser trimmed at the wafer stage to obtain full rated performance without external trims.

The AD674A is available in six different grades. The AD674AJ, K, and L grades are specified for operation over the 0 to +70°C temperature range. The AD674AS, T, and U are specified for the −55°C to +125°C range. All grades are available in a 28-pin hermetically sealed ceramic DIP.

The S, T, and U grades are also available with optional processing to MIL-STD-883C, Class B in a 28-pin DIP or 28-pin LCC package. The Analog Devices Military Products Databook should be consulted for details on /883B testing of the AD674A.

***Protected by U.S. Patent Nos. 3,803,590; 4,213,806; 4,511,413; RE 28,633.**

This an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

PRODUCT HIGHLIGHTS

1. The AD674A interfaces to most 8- or 16-bit microprocessors. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12 bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeroes).
2. The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges: 0 to +10 and 0 to +20 volts unipolar, −5 to +5 and −10 to +10 volts bipolar. Typical bipolar offset and full-scale calibration errors of ±0.1% can be trimmed to zero with one external component each.
3. The internal buried Zener reference is trimmed to 10.00 volts with 1% maximum error and 15 ppm/°C typical T.C. The reference is available externally and can drive up to 2.0 mA beyond the requirements of the reference and bipolar offset resistors.

AD674A—SPECIFICATIONS (@ +25°C with V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, V_{EE} = −15 V or −12 V unless otherwise indicated)

Model	AD674AJ Min	AD674AJ Typ	AD674AJ Max	AD674AK Min	AD674AK Typ	AD674AK Max	AD674AL Min	AD674AL Typ	AD674AL Max	Units
RESOLUTION			12			12			12	Bits
LINEARITY ERROR			±1			±1/2			±1/2	LSB
T_{min} to T_{max}			±1			±1/2			±1/2	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)										
T_{min} to T_{max}	**11**			12			12			Bits
UNIPOLAR OFFSET (Adjustable to Zero)			±2			±2			±2	LSB
BIPOLAR OFFSET (Adjustable to Zero)			±10			±4			±4	LSB
FULL-SCALE CALIBRATION ERROR (With fixed 50 Ω resistor from REF OUT to REF IN) (Adjustable to Zero)		0.1	0.25		0.1	0.25		0.1	0.25	% of FS
TEMPERATURE RANGE	0		+70	0		+70	0		+70	°C
TEMPERATURE COEFFICIENTS (Using Internal Reference)										
T_{min} to T_{max}										
Unipolar Offset			±2 (10)			±1 (5)			±1 (5)	LSB (ppm/°C)
Bipolar Offset			±2 (10)			±1 (5)			±1 (5)	LSB (ppm/°C)
Full-Scale Calibration			±9 (50)			±5 (27)			±2 (10)	LSB (ppm/°C)
POWER SUPPLY REJECTION										
Max Change in Full-Scale Calibration										
V_{CC} = 15 V ± 1.5 V or 12 V ± 0.6 V			±2			±1			±1	LSB
V_{LOGIC} = 5 V ± 0.5 V			±1/2			±1/2			±1/2	LSB
V_{EE} = −15 V ± 1.5 V or −12 V ± 0.6 V			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar	−5		+5	−5		+5	−5		+5	Volts
	−10		+10	−10		+10	−10		+10	Volts
Unipolar	0		+10	0		+10	0		+10	Volts
	0		+20	0		+20	0		+20	Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
DIGITAL CHARACTERISTICS (T_{min} to T_{max})										
Inputs										
Logic "1" Voltage	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	Volts
Logic "0" Voltage	−0.5		+0.8	−0.5		+0.8	−0.5		+0.8	Volts
Current	−100		+100	−100		+100	−100		+100	µA
Capacitance		5			5			5		pF
Outputs (DB11–DB0, STS)										
Logic "1" Voltage (I_{SOURCE} ≤500 µA)	+2.4			+2.4			+2.4			Volts
Logic "0" Voltage (I_{SINK} ≤1.6 mA)			+0.4			+0.4			+0.4	Volts
Leakage (DB11–DB0, High-Z State)	−20		+20	−20		+20	−20		+20	µA
Capacitance		5			5			5		pF
POWER SUPPLIES										
Operating Range										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−11.4		−16.5	−11.4		−16.5	−11.4		−16.5	Volts
Operating Current										
I_{LOGIC}		30	40		30	40		30	40	mA
I_{CC}		2	5		2	5		2	5	mA
I_{EE}		18	29		18	29		18	29	mA
POWER DISSIPATION		390	720		390	720		390	720	mW
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1	9.9	10.0	10.1	Volts
Output current (available for external loads)[1] (External load should not change during conversion)			2.0			2.0			2.0	mA

NOTES

[1]The reference should be buffered for operation on ±12 V supplies.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD674AS Min	Typ	Max	AD674AT Min	Typ	Max	AD674AU Min	Typ	Max	Units
RESOLUTION			12			12			12	Bits
LINEARITY ERROR			±1			±1/2			±1/2	LSB
T_{min} to T_{max}			±1			±1			±1	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)										
T_{min} to T_{max}	11			12			12			Bits
UNIPOLAR OFFSET (Adjustable to Zero)			±2			±2			±2	LSB
BIPOLAR OFFSET (Adjustable to Zero)			±10			±4			±4	LSB
FULL-SCALE CALIBRATION ERROR (With fixed 50 Ω resistor from REF OUT to REF IN) (Adjustable to Zero)		0.1	0.25		0.1	0.25		0.1	0.25	% of FS
TEMPERATURE RANGE	−55		+125	−55		+125	−55		+125	°C
TEMPERATURE COEFFICIENTS (Using Internal Reference)										
T_{min} to T_{max}										
Unipolar Offset			±2 (5)			±1 (2.5)			±1 (2.5)	LSB (ppm/°C)
Bipolar Offset			±4 (10)			±2 (5)			±1 (2.5)	LSB (ppm/°C)
Full-Scale Calibration			±20 (50)			±10 (25)			±5 (12.5)	LSB (ppm/°C)
POWER SUPPLY REJECTION										
Max Change in Full-Scale Calibration										
V_{CC} = 15 V ± 1.5 V or 12 V ± 0.6 V			±2			±1			±1	LSB
V_{LOGIC} = 5 V ± 0.5 V			±1/2			±1/2			±1/2	LSB
V_{EE} = −15 V ± 1.5 V or −12 V ± 0.6 V			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar	−5		+5	−5		+5	−5		+5	Volts
	−10		+10	−10		+10	−10		+10	Volts
Unipolar	0		+10	0		+10	0		+10	Volts
	0		+20	0		+20	0		+20	Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
DIGITAL CHARACTERISTICS (T_{min} to T_{max})										
Inputs										
Logic "1" Voltage	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	Volts
Logic "0" Voltage	−0.5		+0.8	−0.5		+0.8	−0.5		+0.8	Volts
Current	−100		+100	−100		+100	−100		+100	μA
Capacitance		5			5			5		pF
Outputs (DB11–DB0, STS)										
Logic "1" Voltage (I_{SOURCE} ≤500 μA)	+2.4			+2.4			+2.4			Volts
Logic "0" Voltage (I_{SINK} ≤1.6 mA)			+0.4			+0.4			+0.4	Volts
Leakage (DB11–DB0, High-Z State)	−20		+20	−20		+20	−20		+20	μA
Capacitance		5			5			5		pF
POWER SUPPLIES										
Operating Range										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−11.4		−16.5	−11.4		−16.5	−11.4		−16.5	Volts
Operating Current										
I_{LOGIC}		30	40		30	40		30	40	mA
I_{CC}		2	5		2	5		2	5	mA
I_{EE}		18	29		18	29		18	29	mA
POWER DISSIPATION		390	720		390	720		390	720	mW
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1	9.9	10.0	10.1	Volts
Output current (available for external loads)[1] (External load should not change during conversion)			2.0			2.0			2.0	mA

NOTES

[1]The reference should be buffered for operation on ±12 V supplies.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Digital Common . . . . . 0 to +16.5 V
V_{EE} to Digital Common . . . . . 0 to −16.5 V
V_{LOGIC} to Digital Common . . . . . 0 to +7 V
Analog Common to Digital Common . . . . . ±1 V
Digital Inputs to Digital Common . . −0.5 V to V_{LOGIC} +0.5 V
Analog Inputs to Analog Common . . . . . V_{EE} to V_{CC}
20 V_{IN} to Analog Common . . . . . ±24 V
REF OUT . . . . . Indefinite Short to Common
Momentary Short to V_{CC}
Chip Temperature . . . . . 175°C
Power Dissipation . . . . . 825 mW
Lead Temperature, Soldering . . . . . 300°C, 10 sec
Storage Temperature . . . . . −65°C to +150°C

NOTE
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONVERT START TIMING - FULL CONTROL MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DSC}	STS Delay from CE			200	ns
t_{HEC}	CE Pulse Width	50			ns
t_{SSC}	$\overline{CS}$ to CE Setup	50			ns
t_{HSC}	$\overline{CS}$ Low During CE High	50			ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50			ns
t_{HRC}	R/$\overline{C}$ Low During CE High	50			ns
t_{SAC}	A_O to CE Setup	0			ns
t_{HAC}	A_O Valid During CE High	50			ns
t_C	Conversion Time				
	8-Bit Cycle	6	8	10	µs
	12-Bit Cycle	9	12	15	µs

READ TIMING - FULL CONTROL MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DD}	Access Time (from CE)		75	150	ns
t_{HD}	Data Valid after CE Low	25			ns
t_{HL}	Output Float Delay			150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50			ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0			ns
t_{SAR}	A_O to CE Setup	50			ns
t_{HSR}	$\overline{CS}$ Valid After CE Low	0			ns
t_{HRR}	R/$\overline{C}$ High After CE Low	0			ns
t_{HAR}	A_O Valid After CE low	50			ns

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	30	55	600	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

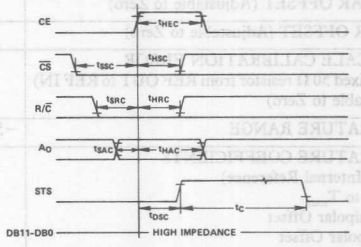


Figure 1. Convert Start Timing

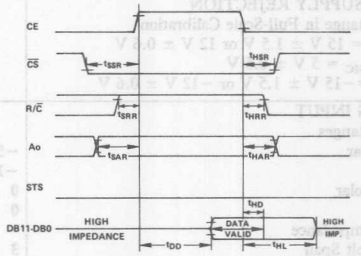


Figure 2. Read Cycle Timing

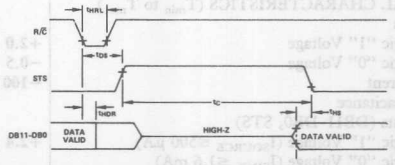


Figure 3. Low Pulse for R/C-Outputs Enabled After Conversion

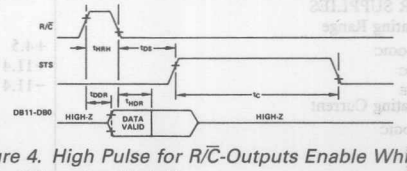


Figure 4. High Pulse for R/C-Outputs Enable While R/C High, Otherwise High-Z

ORDERING GUIDE

Model	Temperature Range	Linearity Error (T_{min} to T_{max})	No Missing Codes (T_{min} to T_{max})	Full Scale T.C. (ppm/°C)	Package Option*
AD674AJD	0 to +70°C	±1 LSB	11 Bits	50.0	D-28
AD674AKD	0 to +70°C	±1/2 LSB	12 Bits	27.0	D-28
AD674ALD	0 to +70°C	±1/2 LSB	12 Bits	10.0	D-28
AD674ASD	−55°C to +125°C	±1 LSB	11 Bits	50.0	D-28
AD674ATD	−55°C to +125°C	±1 LSB	12 Bits	25.0	D-28
AD674AUD	−55°C to +125°C	±1 LSB	12 Bits	12.5	D-28

*D = Ceramic DIP. For outline information see Package Information section.

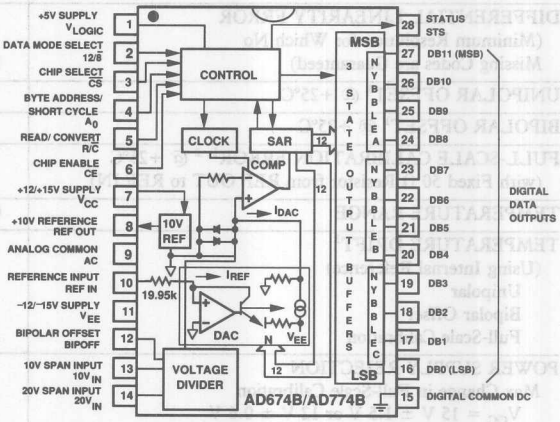
Complete 12-Bit A/D Converters

AD674B*/AD774B*

FEATURES

Complete Monolithic 12-Bit A/D Converters with Reference, Clock, and Three-State Output Buffers
Industry Standard Pinout
High Speed Upgrades for AD574A
8- and 16-Bit Microprocessor Interface
8 μs (max) Conversion Time (AD774B)
15 μs (max) Conversion Time (AD674B)
±5 V, ±10 V, 0–10 V, 0–20 V Input Ranges
Commercial, Industrial and Military Temperature Range Grades
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD674B and AD774B are complete 12-bit successive-approximation analog-to-digital converters with three-state output buffer circuitry for direct interface to 8- and 16-bit microprocessor busses. A high precision voltage reference and clock are included on chip, and the circuit requires only power supplies and control signals for operation.

The AD674B and AD774B are pin compatible with the industry-standard AD574A, but offer faster conversion time and bus-access speed than the AD574A and lower power consumption. The AD674B converts in 15 μs (maximum) and the AD774B converts in 8 μs (maximum).

The monolithic design is implemented using Analog Devices' BiMOS II process allowing high performance bipolar analog circuitry to be combined on the same die with digital CMOS logic. Offset, linearity and scaling errors are minimized by active laser-trimming of thin-film resistors.

Five different grades are available. The J and K grades are specified for operation over the 0°C to +70°C temperature range. The A and B grades are specified from −40°C to +85°C, the T grade is specified from −55°C to +125°C. The J and K grades are available in a 28-pin plastic DIP or 28-lead SOIC. All other grades are available in a 28-pin hermetically sealed ceramic DIP.

PRODUCT HIGHLIGHTS

1. Industry Standard Pinout: The AD674B and AD774B utilize the pinout established by the industry standard AD574A.
2. Analog Operation: The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges: 0 to +10 V and 0 to +20 V unipolar; −5 V to +5 V and −10 V to +10 V bipolar. The AD674B and AD774B operate on +5 V and ±12 V or ±15 V power supplies.
3. Flexible Digital Interface: On-chip multiple-mode three-state output buffers and interface logic allow direct connection to most microprocessors. The 12 bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).
4. The internal reference is trimmed to 10.00 volts with 1% maximum error and 10 ppm/°C typical temperature coefficient. The reference is available externally and can drive up to 2.0 mA beyond the requirements of the converter and bipolar offset resistors.
5. The AD674B and AD774B are available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD674B/AD774B/883B data sheet for detailed specifications.

*Protected by U.S. Patent Nos. 4,250,445; 4,808,908; RE30586.

AD674B/AD774B—SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −15 V ± 10% or −12 V ± 5% unless otherwise indicated)

Model (AD674B or AD774B)	J Grade			K Grade		
	Min	Typ	Max	Min	Typ	Max
RESOLUTION			12			12
LINEARITY ERROR @ +25°C			±1			±1/2
T_{MIN} to T_{MAX}			±1			±1/2
DIFFERENTIAL LINEARITY ERROR (Minimum Resolution for Which No Missing Codes are Guaranteed)	12			12		
UNIPOLAR OFFSET[1] @ +25°C			±2			±2
BIPOLAR OFFSET[1] @ +25°C			±6			±3
FULL-SCALE CALIBRATION ERROR[1, 2] @ +25°C (with Fixed 50 Ω Resistor from REF OUT to REF IN)		0.1	0.25		0.1	0.125
TEMPERATURE RANGE	0		+70	0		+70
TEMPERATURE DRIFT[3] (Using Internal Reference)						
Unipolar			±2			±1
Bipolar Offset			±2			±1
Full-Scale Calibration			±6			±2
POWER SUPPLY REJECTION						
Max Change in Full-Scale Calibration						
V_{CC} = 15 V ± 1.5 V or 12 V ± 0.6 V			±2			±1
V_{LOGIC} = 5 V ± 0.5 V			±1/2			±1/2
V_{EE} = −15 V ± 1.5 V or −12 V ± 0.6 V			±2			±1
ANALOG INPUT						
Input Ranges						
Bipolar	−5		+5	−5		+5
	−10		+10	−10		+10
Unipolar	0		+10	0		+10
	0		+20	0		+20
Input Impedance						
10 Volt Span	3	5	7	3	5	7
20 Volt Span	6	10	14	6	10	14
POWER SUPPLIES						
Operating Range						
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5
V_{CC}	+11.4		+16.5	+11.4		+16.5
V_{EE}	−16.5		−11.4	−16.5		−11.4
Operating Current						
I_{LOGIC}		3.5	7		3.5	7
I_{CC}		3.5	7		3.5	7
I_{EE}		10	14		10	14
POWER CONSUMPTION		220	375		220	375
		175			175	
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1
Output Current (Available for External Loads) (External Load Should Not Change During the Conversion)			2.0			2.0

NOTES
[1]Adjustable to zero.
[2]Includes internal voltage reference error.
[3]Maximum change from +25°C value to the value at T_{MIN} or T_{MAX}.
[4]Tested with REF OUT tied to REF IN through 50 Ω resistor, V_{CC} = +16.5 V, V_{EE} = −16.5 V, V_{LOGIC} = +5.5 V, and outputs in high-Z mode.
[5]Tested with REF OUT tied to REF IN through 50 Ω resistor, V_{CC} = +12 V, V_{EE} = −12 V, V_{LOGIC} = +5 V, and outputs in high-Z mode.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all devices at final electrical test at T_{MIN}, +25°C, and T_{MAX}, and results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

A Grade			B Grade			T Grade			
Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
		12			12			12	Bits
		±1			±1/2			±1/2	LSB
		±1			±1/2			±1	LSB
12			12			12			Bits
		±2			±2			±2	LSB
		±6			±3			±3	LSB
	0.1	0.25		0.1	0.125		0.1	0.125	% of FS
−40		+85	−40		+85	−55		+125	°C
		±2			±1			±1	LSB
		±2			±1			±2	LSB
		±8			±5			±7	LSB
		±2			±1			±1	LSB
		±1/2			±1/2			±1/2	LSB
		±2			±1			±1	LSB
−5		+5	−5		+5	−5		+5	Volts
−10		+10	−10		+10	−10		+10	Volts
0		+10	0		+10	0		+10	Volts
0		+20	0		+20	0		+20	Volts
3	5	7	3	5	7	3	5	7	kΩ
6	10	14	6	10	14	6	10	14	kΩ
+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
−16.5		−11.4	−16.5		−11.4	−16.5		−11.4	Volts
	3.5	7		3.5	7		3.5	7	mA
	3.5	7		3.5	7		3.5	7	mA
	10	14		10	14		10	14	mA
	220	375		220	375		220	375	mW[4]
	175			175			175		mW[5]
9.9	10.0	10.1	9.9	10.0	10.1	9.9	10.0	10.1	Volts
		2.0			2.0			2.0	mA

DIGITAL SPECIFICATIONS (for all grades T_{MIN} to T_{MAX}, with V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −15 V ± 10% or −12 V ± 5%)

Parameter		Test Conditions	Min	Max	Units
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		+2.0	V_{LOGIC} +0.5 V	V
V_{IL}	Low Level Input Voltage		−0.5	+0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{LOGIC}$	−10	+10	μA
I_{IL}	Low Level Input Current	V_{IN} = 0 V	−10	+10	μA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.5 mA	+2.4		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		+0.4	V
I_{OZ}	High-Z Leakage Current	V_{IN} = 0 to V_{LOGIC}	−10	+10	μA
C_{OZ}	High-Z Output Capacitance			10	pF

SWITCHING SPECIFICATIONS (for all grades T_{MIN} to T_{MAX} with V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −15 V ± 10% or −12 V ± 5%; unless otherwise noted)

CONVERTER START TIMING (Figure 1)

Parameter	Symbol	J, K, A, B Grades Min	Typ	Max	T Grade Min	Typ	Max	Units
Conversion Time								
8-Bit Cycle (AD674B)	t_C	6	8	10	6	8	10	μs
12-Bit Cycle (AD674B	t_C	9	12	15	9	12	15	μs
8-Bit Cycle (AD774B)	t_C	4	5	6	4	5	6	μs
12-Bit Cycle (AD774B)	t_C	6	7.3	8	6	7.3	8	μs
STS Delay from CE	t_{DSC}			200			225	ns
CE Pulse Width	t_{HEC}	50			50			ns
$\overline{CS}$ to CE Setup	t_{SSC}	50			50			ns
$\overline{CS}$ Low During CE High	t_{HSC}	50			50			ns
R/$\overline{C}$ to CE Setup	t_{SRC}	50			50			ns
R/$\overline{C}$ Low During CE High	t_{HRC}	50			50			ns
A_0 to CE Setup	t_{SAC}	0			0			ns
A_0 Valid During CE High	t_{HAC}	50			50			ns

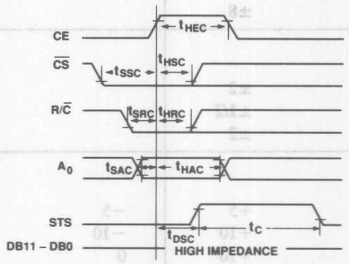


Figure 1. Convert Start Timing

READ TIMING—FULL CONTROL MODE (Figure 2)

Parameter	Symbol	J, K, A, B Grades Min	Typ	Max	T Grade Min	Typ	Max	Units
Access Time								
C_L = 100 pF	t_{DD}[1]		75	150		75	150	ns
Data Valid After CE Low	t_{HD}	25[2]			25[2]			ns
		20[3]			15[4]			ns
Output Float Delay	t_{HL}[5]			150			150	ns
$\overline{CS}$ to CE Setup	t_{SSR}	50			50			ns
R/$\overline{C}$ to CE Setup	t_{SRR}	0			0			ns
$\overline{A_0}$ to CE Setup	t_{SAR}	50			50			ns
$\overline{CS}$ Valid After CE Low	t_{HSR}	0			0			ns
R/$\overline{C}$ High After CE Low	t_{HRR}	0			0			ns
A_0 Valid After CE Low	t_{HAR}	50			50			ns

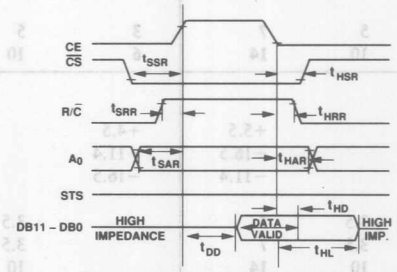
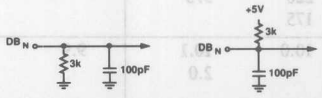
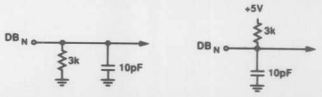


Figure 2. Read Cycle Timing



High-Z to Logic 1 High-Z to Logic 0

Figure 3a. Load Circuit for Access Time Test



Logic 1 to High-Z Logic 0 to High-Z

Figure 3b. Load Circuit for Output Float Delay Test

NOTES

[1] t_{DD} is measured with the load circuit of Figure 3a and is defined as the time required for an output to cross 0.4 V or 2.4 V.

[2] 0°C to T_{MAX}.

[3] At −40°C.

[4] At −55°C.

[5] t_{HL} is defined as the time required for the data lines to change 0.5 V when loaded with the circuit of Figure 3b.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at T_{MIN}, +25°C, and T_{MAX}. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

TIMING—STAND-ALONE MODE (Figures 4a and 4b)

Parameter	Symbol	J, K, A, B Grades Min	Typ	Max	T Grade Min	Typ	Max	Units
Data Access Time	t_{DDR}			150			150	ns
Low R/$\overline{C}$ Pulse Width	t_{HRL}	50			50			ns
STS Delay from R/$\overline{C}$	t_{DS}			200			225	ns
Data Valid After R/$\overline{C}$ Low	t_{HDR}	25			25			ns
STS Delay After Data Valid	t_{HS}	30	200	600	30	200	600	ns
High R/$\overline{C}$ Pulse Width	t_{HRH}	150			150			ns

Specifications subject to change without notice.

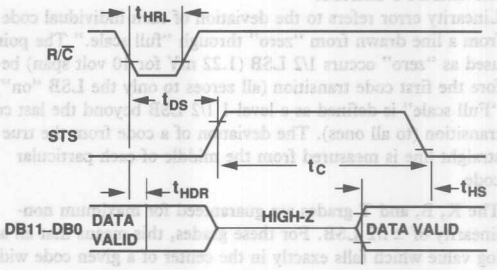


Figure 4a. Stand-Alone Mode Timing Low Pulse for R/$\overline{C}$

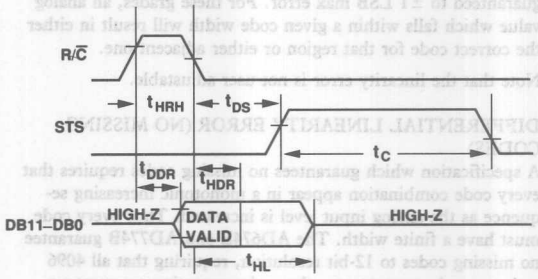


Figure 4b. Stand-Alone Mode Timing High Pulse for R/$\overline{C}$

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Digital Common . . . . . 0 to +16.5 V
V_{EE} to Digital Common . . . . . 0 to −16.5 V
V_{LOGIC} to Digital Common . . . . . 0 to +7 V
Analog Common to Digital Common . . . . . ±1 V
Digital Inputs to Digital Common . −0.5 V to V_{LOGIC} +0.5 V
Analog Inputs to Analog Common . . . . . V_{EE} to V_{CC}
20 V_{IN} to Analog Common . . . . . ±24 V
REF OUT . . . . . Indefinite Short to Common
. . . . . Momentary Short to V_{CC}
Junction Temperature . . . . . +175°C
Power Dissipation . . . . . 825 mW
Lead Temperature, Soldering . . . . . 300°C, 10 sec
Storage Temperature . . . . . −65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



ORDERING GUIDE

Model[1]	Temperature	Conversion Time (max)	INL (T_{MIN} to T_{MAX})	Package Description	Package Option[2]
AD674BJN	0°C to +70°C	15 µs	±1 LSB	Plastic DIP	N-28A
AD674BKN	0°C to +70°C	15 µs	±1/2 LSB	Plastic DIP	N-28A
AD674BJR	0°C to +70°C	15 µs	±1 LSB	Plastic SOIC	R-28
AD674BKR	0°C to +70°C	15 µs	±1/2 LSB	Plastic SOIC	R-28
AD674BAD	−40°C to +85°C	15 µs	±1 LSB	Ceramic DIP	D-28A
AD674BBD	−40°C to +85°C	15 µs	±1/2 LSB	Ceramic DIP	D-28A
AD674BTD	−55°C to +125°C	15 µs	±1 LSB	Ceramic DIP	D-28A
AD774BJN	0°C to +70°C	8 µs	±1 LSB	Plastic DIP	N-28A
AD774BKN	0°C to +70°C	8 µs	±1/2 LSB	Plastic DIP	N-28A
AD774BJR	0°C to +70°C	15 µs	±1 LSB	Plastic SOIC	R-28
AD774BKR	0°C to +70°C	15 µs	±1/2 LSB	Plastic SOIC	R-28
AD774BAD	−40°C to +85°C	8 µs	±1 LSB	Ceramic DIP	D-28A
AD774BBD	−40°C to +85°C	8 µs	±1/2 LSB	Ceramic DIP	D-28A
AD774BTD	−55°C to +125°C	8 µs	±1 LSB	Ceramic DIP	D-28A

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD674B/AD774B/883B data sheet.
[2]N = Plastic DIP; D = Hermetic DIP; R = Plastic SOIC. For outline information see Package Information section.

DEFINITION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale." The point used as "zero" occurs 1/2 LSB (1.22 mV for 10 volt span) before the first code transition (all zeroes to only the LSB "on"). "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The K, B, and T grades are guaranteed for maximum nonlinearity of ±1/2 LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The J and A grades are guaranteed to ±1 LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. The AD674B and AD774B guarantee no missing codes to 12-bit resolution, requiring that all 4096 codes must be present over the entire operating temperature ranges.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed later. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET

In the bipolar mode the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±1/2 LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

LEFT-JUSTIFIED DATA

The output data format is left-justified. This means that the data represents the analog input as a fraction of full scale, ranging from 0 to 4095/4096. This implies a binary point 4095 to the left of the MSB.

FULL-SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1 1/2 LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full-scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 7 and 8. The full-scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full-scale gain from the initial value using the internal 10 V reference.

TEMPERATURE DRIFT

The temperature drift for full-scale calibration, unipolar offset, and bipolar offset specifies the maximum change from the initial (+25°C) value to the value at T_{MIN} or T_{MAX}.

POWER SUPPLY REJECTION

The standard specifications assume use of +5.00 V and ±15.00 V or ±12.00 V supplies. The only effect of power supply error on the performance of the device will be a small change in the full-scale calibration. This will result in a linear change in all lower-order codes. The specifications show the maximum full-scale change from the initial value with the supplies at the various limits.

CODE WIDTH

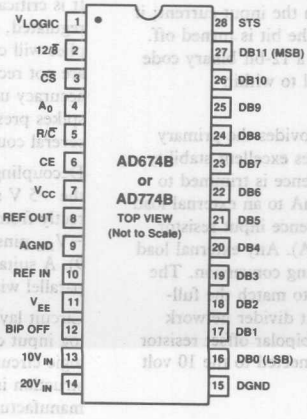
A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full-scale range or 2.44 mV out of 10 volts for a 12-bit ADC.

AD674B AND AD774B PIN DESCRIPTION

Symbol	Pin No.	Type	Name and Function
AGND	9	P	Analog Ground (Common).
A_0	4	DI	Byte Address/Short Cycle. If a conversion is started with A_0 Active LOW, a full 12-bit conversion cycle is initiated. If A_0 is Active HIGH during a convert start, a shorter 8-bit conversion cycle results. During Read (R/$\overline{C}$ = 1) with 12/$\overline{8}$ LOW, A_0 = LOW enables the 8 most significant bits, and A_0 = HIGH enables DB3–DB0 and sets DB7–DB4 = 0.
BIP OFF	12	AI	Bipolar Offset. Connect through a 50 Ω resistor to REF OUT for bipolar operation or to Analog Common for unipolar operation.
CE	6	DI	Chip Enable. Chip Enable is Active HIGH and is used to initiate a convert or read operation.
$\overline{CS}$	3	DI	Chip Select. Chip Select is Active LOW.
DB11–DB8	27–24	DO	Data Bits 11 through 8. In the 12-bit format (see 12/$\overline{8}$ and A_0 pins), these pins provide the upper 4 bits of data. In the 8-bit format, they provide the upper 4 bits when A_0 is LOW and are disabled when A_0 is HIGH.
DB7–DB4	23–20	DO	Data Bits 7 through 4. In the 12-bit format these pins provide the middle 4 bits of data. In the 8-bit format they provide the middle 4 bits when A_0 is LOW and all zeroes when A_0 is HIGH.
DB3–DB0	19–16	DO	Data Bits 3 through 0. In both the 12-bit and 8-bit format these pins provide the lower 4 bits of data when A_0 is HIGH; they are disabled when A_0 is LOW.
DGND	15	P	Digital Ground (Common).
REF OUT	8	AO	+10 V Reference Output.
R/$\overline{C}$	5	DI	Read/Convert. In the full control mode R/$\overline{C}$ is Active HIGH for a read operation and Active LOW for a convert operation. In the stand-alone mode, the falling edge of R/$\overline{C}$ initiates a conversion.
REF IN	10	AI	Reference Input is connected through a 50 Ω resistor to +10 V Reference for normal operation.
STS	28	DO	Status is Active HIGH when a conversion is in progress and goes LOW when the conversion is completed.
V_{CC}	7	P	+12 V/+15 V Analog Supply.
V_{EE}	11	P	−12 V/−15 V Analog Supply.
V_{LOGIC}	1	P	+5 V Logic Supply.
10 V_{IN}	13	AI	10 V Span Input, 0 to +10 V unipolar mode or −5 V to +5 V bipolar mode. When using the 20 V Span, 10 V_{IN} should not be connected.
20 V_{IN}	14	AI	20 V Span Input, 0 to +20 V unipolar mode or −10 V to +10 V bipolar mode. When using the 10 V Span, 20 V_{IN} should not be connected.
12/$\overline{8}$	2	DI	The 12/$\overline{8}$ pin determines whether the digital output data is to be organized as two 8-bit words (12/$\overline{8}$ LOW) or a single 12-bit word (12/$\overline{8}$ HIGH).

TYPE: AI = Analog Input
AO = Analog Output
DI = Digital Input
DO = Digital Output
P = Power

PIN CONFIGURATION



CIRCUIT OPERATION

The AD674B and AD774B are complete 12-bit monolithic A/D converters which require no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram is shown in Figure 5.

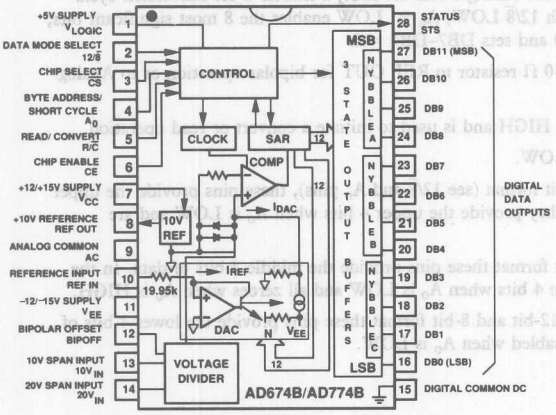


Figure 5. Block Diagram of AD674B and AD774B

When the control section is commanded to initiate a conversion (as described later), it enables the clock and resets the successive-approximation register (SAR) to all zeroes. Once a conversion cycle has begun, it cannot be stopped or restarted and data is not available from the output buffers. The SAR, timed by the clock, will sequence through the conversion cycle and return an end-of-convert flag to the control section. The control section will then disable the clock, bring the output status flag low, and enable control functions to allow data read by external command.

During the conversion cycle, the internal 12-bit current output DAC is sequenced by the SAR from the most-significant-bit (MSB) to least-significant-bit (LSB) to provide an output current which accurately balances the input signal current through the divider network. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2 LSB.

The temperature-compensated reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ±1%; it can supply up to 2.0 mA to an external load in addition to the requirements of the reference input resistor (0.5 mA) and bipolar offset resistor (0.5 mA). Any external load on the reference must remain constant during conversion. The thin film application resistors are trimmed to match the full-scale output current of the DAC. The input divider network provides a 10 V or 20 V input range. The bipolar offset resistor is grounded for unipolar operation and connected to the 10 volt reference for bipolar operation.

DRIVING THE ANALOG INPUT

The AD674B and AD774B are successive-approximation analog-to-digital converters. During the conversion cycle, the ADC input current is modulated by the DAC test current at approximately a 1 MHz rate. Thus it is important to recognize that the signal source driving the ADC must be capable of holding a constant output voltage under dynamically-changing load conditions.

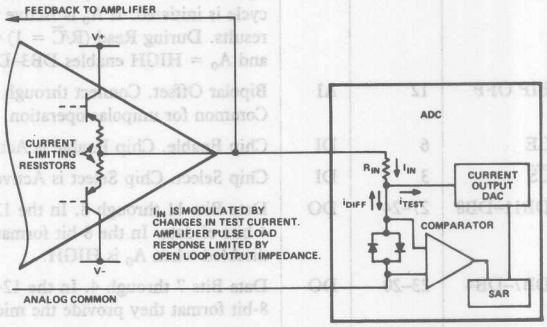


Figure 6. Op Amp–ADC Interface

The closed-loop output impedance of an op amp is equal to the open-loop output impedance (usually a few hundred ohms) divided by the loop gain at the frequency of interest. It is often assumed that the loop gain of a follower-connected op amp is sufficiently high to reduce the closed-loop output impedance to a negligibly small value, particularly if the signal is low frequency. However, the amplifier driving the ADC must either have sufficient loop gain at 1 MHz to reduce the closed-loop output impedance to a low value or have low open-loop output impedance. This can be accomplished by using a wideband op amp, such as the AD711.

If a sample-hold amplifier is required, the monolithic AD585 or AD781 is recommended, with the output buffer driving the AD674B or AD774B input directly. A better alternative is the AD1674 which is a 10 μs *sampling* ADC in the same pinout as the AD574A, AD674A or AD774B and is functionally equivalent.

SUPPLY DECOUPLING AND LAYOUT CONSIDERATIONS

It is critically important that the power supplies be filtered, well regulated, and free from high frequency noise. Use of noisy supplies will cause unstable output codes. Switching power supplies are not recommended for circuits attempting to achieve 12-bit accuracy unless great care is used in filtering any switching spikes present in the output. Few millivolts of noise represent several counts of error in a 12-bit ADC.

Decoupling capacitors should be used on all power supply pins; the +5 V supply decoupling capacitor should be connected directly from Pin 1 to Pin 15 (digital common) and the $+V_{CC}$ and $-V_{EE}$ pins should be decoupled directly to analog common (Pin 9). A suitable decoupling capacitor is a 4.7 μF tantalum type in parallel with a 0.1 μF ceramic disc type.

Circuit layout should attempt to locate the ADC, associated analog input circuitry, and interconnections as far as possible from logic circuitry. For this reason, the use of wire-wrap circuit construction is not recommended. Careful printed-circuit layout and manufacturing is preferred.

UNIPOLAR RANGE CONNECTIONS FOR THE AD674B and AD774B

The AD674B and AD774B contain all the active components required to perform a complete 12-bit A/D conversion. Thus, for most situations, all that is necessary is connection of the power supplies (+5 V, +12/+15 V and −12/−15 V), the analog input, and the conversion initiation command, as discussed on the next page.

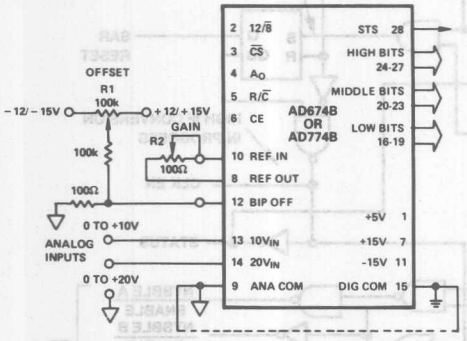


Figure 7. Unipolar Input Connections

All of the thin-film application resistors of the AD674B and AD774B are factory trimmed for absolute calibration. Therefore, in many applications, no calibration trimming will be required. The absolute accuracy for each grade is given in the specification tables. For example, if no trims are used, ±2 LSB max zero offset error and ±0.25% (10LSB) max full-scale error are guaranteed. If the offset trim is not required, Pin 12 can be connected directly to Pin 9; the two resistors and trimmer for Pin 12 are then not needed. If the full-scale trim is not required, a 50 Ω 1% metal film resistor should be connected between Pin 8 and Pin 10.

The analog input is connected between Pins 13 and 9 for a 0 to +10 V input range, between Pins 14 and 9 for a 0 to +20 V input range. Input signals beyond the supplies are easily accommodated. For the 10 volt span input, the LSB has a nominal value of 2.44 mV; for the 20 volt span, 4.88 mV. If a 10.24 V range is desired (nominal 2.5 mV/bit), the gain trimmer (R2) should be replaced by a 50 Ω resistor, and a 200 Ω trimmer inserted in series with the analog input to Pin 13 (for a full-scale range of 20.48 V (5 mV/bit), use a 500 Ω trimmer into Pin 14). The gain trim described below is now done with these trimmers. The nominal input impedance into Pin 13 is 5 kΩ, and 10 kΩ into Pin 14.

UNIPOLAR CALIBRATION

The connections for unipolar ranges are shown in Figure 7. The AD674B or AD774B is trimmed to a nominal 1/2 LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2 LSB (1.22 mV for 10 V range).

If Pin 12 is connected to Pin 9, the unit will behave in this manner, within specifications. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±15 mV of offset trim range.

The full-scale trim is done by applying a signal 1 1/2 LSB below the nominal full scale (9.9963 for a 10 V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 8. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient, one or both of the trimmers shown can be replaced by a 50 Ω ±1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal 1/2 LSB above negative full scale (−4.9988 V for the ±5 V range) is applied and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1 1/2 LSB below positive full scale (+4.9963 V for the ±5 V range) is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

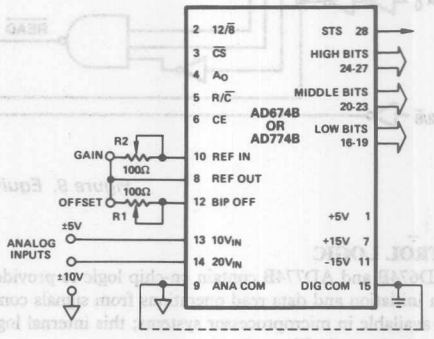


Figure 8. Bipolar Input Connections

GROUNDING CONSIDERATIONS

The analog common at Pin 9 is the ground reference point for the internal reference and is thus the "high quality" ground for the ADC; it should be connected directly to the analog reference point of the system. In order to achieve the high accuracy performance available from the ADC in an environment of high digital noise content, it is required that the analog and digital commons be connected together at the package. In some situations, the digital common at Pin 15 can be connected to the most convenient ground reference point; digital power return is preferred.

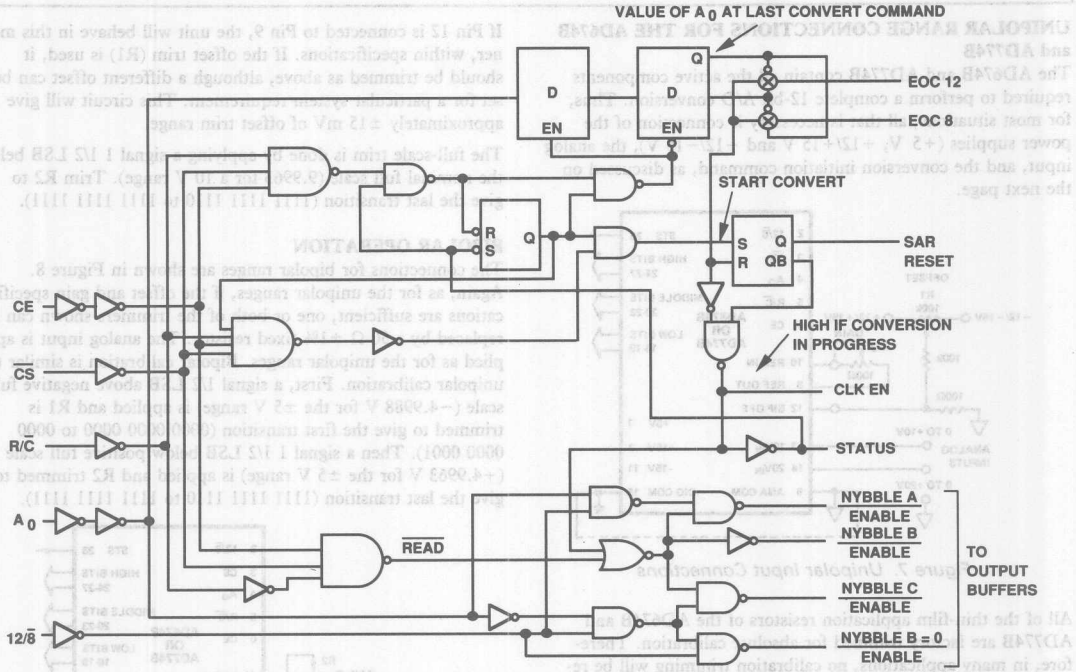


Figure 9. Equivalent Internal Logic Circuitry

CONTROL LOGIC

The AD674B and AD774B contain on-chip logic to provide conversion initiation and data read operations from signals commonly available in microprocessor systems; this internal logic circuitry is shown in Figure 9.

The control signals CE, $\overline{CS}$, and R/$\overline{C}$ control the operation of the converter. The state of R/$\overline{C}$ when CE and $\overline{CS}$ are both asserted determines whether a data read (R/$\overline{C}$ = 1) or a convert (R/$\overline{C}$ = 0) is in progress. The register control inputs A_0 and 12/$\overline{8}$ control conversion length and data format. If a conversion is started with A_0 low, a full 12-bit conversion cycle is initiated. If A_0 is high during a convert start, a shorter 8-bit conversion cycle results. During data read operations, A_0 determines whether the three-state buffers containing the 8 MSBs of the conversion result (A_0 = 0) or the 4 LSBs (A_0 = 1) are enabled. The 12/$\overline{8}$ pin determines whether the output data is to be organized as two 8-bit words (12/$\overline{8}$ tied to DIGITAL COMMON) or a single 12-bit word (12/$\overline{8}$ tied to V_{LOGIC}). In the 8-bit mode, the byte addressed when A_0 is high contains the 4 LSBs from the conversion followed by four trailing zeroes. This organization allows the data lines to be overlapped for direct interface to 8-bit buses without the need for external three-state buffers.

An output signal, STS, indicates the status of the converter. STS goes high at the beginning of a conversion and returns low when the conversion cycle is complete.

Table I. Truth Table

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-Bit Conversion
1	0	0	X	1	Initiate 8-Bit Conversion
1	0	1	1	X	Enable 12-Bit Parallel Output
1	0	1	0	0	Enable 8 Most Significant Bits
1	0	1	0	1	Enable 4 LSBs +4 Trailing Zeroes

The ADC may be operated in one of two modes, the full-control mode and the stand-alone mode. The full-control mode utilizes all the control signals and is useful in systems that address decode multiple devices on a single data bus. The stand-alone mode is useful in systems with dedicated input ports available. In general, the stand-alone mode is capable of issuing start-convert commands on a more precise basis and, therefore, produces higher accuracy results. The following sections describe these two modes in more detail.

FULL-CONTROL MODE

Chip Enable (CE), Chip Select ($\overline{CS}$) and Read/Convert (R/$\overline{C}$) are used to control Convert or Read modes of operation. Either CE or $\overline{CS}$ may be used to initiate a conversion. The state of R/$\overline{C}$ when CE and $\overline{CS}$ are both asserted determines whether a data Read (R/$\overline{C}$ = 1) or a Convert (R/$\overline{C}$ = 0) is in progress. R/$\overline{C}$ should be LOW before both CE and $\overline{CS}$ are asserted; if R/$\overline{C}$ is HIGH, a Read operation will momentarily occur, possibly resulting in system bus contention.

STAND-ALONE MODE

"Stand-alone" mode is useful in systems with dedicated input ports available and thus not requiring full bus interface capability. Stand-alone mode applications are generally able to issue conversion start commands more precisely than full-control mode, resulting in improved accuracy.

CE and 12/$\overline{8}$ are wired HIGH, $\overline{CS}$ and A_0 are wired LOW, and conversion is controlled by R/$\overline{C}$. The three-state buffers are enabled when R/$\overline{C}$ is HIGH and a conversion starts when R/$\overline{C}$ goes LOW. This gives rise to two possible control signals—a high pulse or a low pulse. Operation with a low pulse is shown in Figure 4a. In this case, the outputs are forced into the high impedance state in response to the falling edge of R/$\overline{C}$ and return to valid logic levels after the conversion cycle is completed. The STS line goes HIGH 200 ns after R/$\overline{C}$ goes LOW and returns low 600 ns after data is valid.

If conversion is initiated by a high pulse as shown in Figure 4b, the data lines are enabled during the time when R/$\overline{C}$ is HIGH. The falling edge of R/$\overline{C}$ starts the next conversion, and the data lines return to three-state (and remain three-state) until the next high pulse of R/$\overline{C}$.

CONVERSION TIMING

Once a conversion is started, the STS line goes HIGH. Convert start commands will be ignored until the conversion cycle is complete. The output data buffers can be enabled up to 1.2 µs prior to STS going LOW. The STS line will return LOW at the end of the conversion cycle.

The register control inputs, A_0 and 12/$\overline{8}$, control conversion length and data format. If a conversion is started with A_0 LOW, a full 12-bit conversion cycle is initiated. If A_0 is HIGH during a convert start, a shorter 8-bit conversion cycle results.

During data read operations, A_0 determines whether the three-state buffers containing the 8 MSBs of the conversion result (A_0 = 0) or the 4 LSBs (A_0 = 1) are enabled. The 12/$\overline{8}$ pin determines whether the output data is to be organized as two 8-bit words (12/$\overline{8}$ tied LOW) or a single 12-bit word (12/$\overline{8}$ tied HIGH). In the 8-bit mode, the byte addressed when A_0 is high contains the 4 LSBs from the conversion followed by four trailing zeroes. This organization allows the data lines to be overlapped for direct interface to 8-bit buses without the need for external three-state buffers.

GENERAL A/D CONVERTER INTERFACE CONSIDERATIONS

A typical A/D converter interface routine involves several operations. First, a write to the ADC address initiates a conversion. The processor must then wait for the conversion cycle to complete, since most integrated circuit ADCs take longer than one instruction cycle to complete a conversion. Valid data can, of course, only be read after the conversion is complete. The AD674B and AD774B provide an output signal (STS) which indicates when a conversion is in progress. This signal can be polled by the processor by reading it through an external three-state buffer (or other input port). The STS signal can also be used to generate an interrupt upon completion of conversion if the system timing requirements are critical and the processor has other tasks to perform during the ADC conversion cycle. Another possible time-out method is to assume that the ADC will take its maximum conversion time to convert, and insert a sufficient number of "no-op" instructions to ensure that this amount of processor time is consumed.

Once conversion is complete, the data can be read. For converters with more data bits than are available on the bus, a choice of data formats is required, and multiple read operations are needed. The AD674B and AD774B include internal logic to permit direct interface to 8-bit and 16-bit data buses, selected by the 12/$\overline{8}$ input. In 16-bit bus applications (12/$\overline{8}$ high) the data lines (DB11 through DB0) may be connected to either the 12 most significant or 12 least significant bits of the data bus. The remaining four bits should be masked in software. The interface to an 8-bit data bus (12/$\overline{8}$ low) is done in a left-justified format. The even address (A0 low) contains the 8 MSBs (DB11 through DB4). The odd address (A0 high) contains the 4 LSBs (DB3 through DB0) in the upper half of the byte, followed by four trailing zeroes, thus eliminating bit masking instructions.

It is not possible to rearrange the output data lines for right-justified 8-bit bus interface.

	D7							D0
XXX0 (EVEN ADDR)	DB11 (MSB)	DB10	DB9	DB8	DB7	DB6	DB5	DB4
XXX1 (ODD ADDR)	DB3	DB2	DB1	DB0 (LSB)	0	0	0	0

Figure 10. Data Format for 8-Bit Bus

FULL-CONTROL MODE

Chip Enable ($\overline{CE}$), Chip Select ($\overline{CS}$) and Read/$\overline{Convert}$ ($R/\overline{C}$) are used to control Convert or Read modes of operation. Either $\overline{CE}$ or $\overline{CS}$ may be used to initiate a conversion. The state of $R/\overline{C}$ when $\overline{CE}$ and $\overline{CS}$ are both asserted determines whether a data Read ($R/\overline{C}$ = 1) or a Convert ($R/\overline{C}$ = 0) is in progress. $R/\overline{C}$ should be LOW before both $\overline{CE}$ and $\overline{CS}$ are asserted; if $R/\overline{C}$ is HIGH, a Read operation will momentarily occur, possibly re-sulting in system bus contention.

STAND-ALONE MODE

"Stand-alone" mode is useful in systems with dedicated input ports available and thus not requiring full bus interface capabil-ity. Stand-alone mode applications are generally able to issue conversion start commands more precisely than full-control mode, resulting in improved accuracy.

$\overline{CE}$ and 12/$\overline{8}$ are wired HIGH, $\overline{CS}$ and A_0 are wired LOW, and conversion is controlled by $R/\overline{C}$. The three-state buffers are en-abled when $R/\overline{C}$ is HIGH and a conversion starts when $R/\overline{C}$ goes LOW. This gives rise to two possible control signals—a high pulse or a low pulse. Operation with a low pulse is shown in Figure 4a. In this case, the outputs are forced into the high im-pedance state in response to the falling edge of $R/\overline{C}$ and return to valid logic levels after the conversion cycle is completed. The STS line goes HIGH 200 ns after $R/\overline{C}$ goes LOW and returns low 600 ns after data is valid.

If conversion is initiated by a high pulse as shown in Figure 4b, the data lines are enabled during the time when $R/\overline{C}$ is HIGH. The falling edge of $R/\overline{C}$ starts the next conversion, and the data lines return to three-state (and remain three-state) until the next high pulse of $R/\overline{C}$.

CONVERSION TIMING

Once a conversion is started, the STS line goes HIGH. Convert start commands will be ignored until the conversion cycle is complete. The output data buffers can be enabled up to 1.2 µs prior to STS going LOW. The STS line will return LOW at the end of the conversion cycle.

The register control inputs, A_0 and 12/$\overline{8}$, control conversion length and data format. If a conversion is started with A_0 LOW, a full 12-bit conversion cycle is initiated. If A_0 is HIGH during a convert start, a shorter 8-bit conversion cycle results.

During data read operations, A_0 determines whether the three-state buffers containing the 8 MSBs of the conversion result (A_0 = 0) or the 4 LSBs (A_0 = 1) are enabled. The 12/$\overline{8}$ pin de-termines whether the output data is to be organized as two 8-bit words (12/$\overline{8}$ tied LOW) or a single 12-bit word (12/$\overline{8}$ tied HIGH). In the 8-bit mode, the byte addressed when A_0 is high contains the 4 LSBs from the conversion followed by four trail-ing zeros. This organization allows the data lines to be over-lapped for direct interface to 8-bit buses without the need for external three-state buffers.

GENERAL A/D CONVERTER INTERFACE CONSIDERATIONS

A typical A/D converter interface routine involves several opera-tions. First, a write to the ADC address initiates a conversion. The processor must then wait for the conversion cycle to com-plete, since most integrated circuit ADCs take longer than one instruction cycle to complete a conversion. Valid data can, of course, only be read after the conversion is complete. The ADC674B and ADJ774B provide an output signal (STS) which indicates when a conversion is in progress. This signal can be polled by the processor by reading it through an external three-state buffer (or other input port). The STS signal can also be used to generate an interrupt upon completion of conversion if the system timing requirements are critical and the processor has other tasks to perform during the ADC conversion cycle. Another possible time-out method is to assume that the ADC will take its maximum conversion time to convert, and insert a sufficient number of "no-op" instructions to ensure that this amount of processor time is consumed.

Once conversion is complete, the data can be read. For conver-ters with more data bits than are available on the bus, a choice of data formats is required, and multiple read operations are needed. The ADC674B and ADJ774B include internal logic to per-mit direct interface to 8-bit and 16-bit data buses, selected by the 12/$\overline{8}$ input. In 16-bit bus applications (12/$\overline{8}$ high) the data lines (DB11 through DB0) may be connected to either the 12 most significant or 12 least significant bits of the data bus. The remaining four bits should be masked in software. The interface to an 8-bit data bus (12/$\overline{8}$ low) is done in a left-justified format. The even address (A0 low) contains the 8 MSBs (DB11 through DB4). The odd address (A0 high) contains the 4 LSBs (DB3 through DB0) in the upper half of the byte, followed by four trailing zeros, thus eliminating bit masking instructions.

It is not possible to rearrange the output data lines for right-justified 8-bit bus interface.

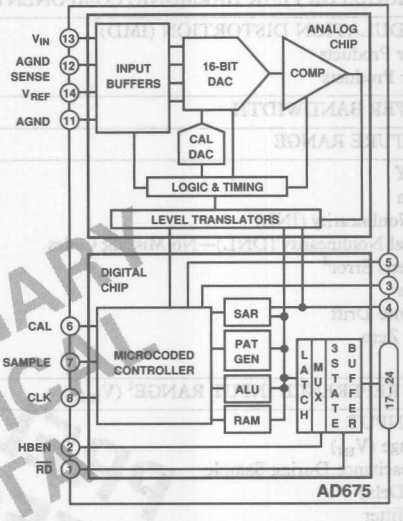
Figure 16. Data Format for 8-Bit Bus

AD675

FEATURES

AC and DC Specified
Autocalibrating
On-Chip Sample-Hold Function
Two-Byte or Serial Output
16-Bits No Missing Codes
±1 LSB INL
0.001% THD
90 dB S/(N+D)
1 MHz Full Power Bandwidth
24-Pin "Skinny" DIP Package

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD675 is a multipurpose 16-bit parallel output analog-to-digital converter which utilizes a switched capacitor/charge redistribution architecture to achieve a 100 kSPS conversion rate (10 µs total conversion time). Overall performance is optimized by digitally correcting internal nonlinearities through on-chip autocalibration.

The AD675 includes a sample-hold amplifier (SHA) and microprocessor compatible bus interface with three-state output buffers and two-byte read. Output data is also available in serial format.

The AD675 circuitry is segmented onto two monolithic chips—a digital control chip fabricated on Analog Devices' DSP CMOS process and an analog ADC chip fabricated on our BiMOS II process. Both chips are contained in a single package.

The AD675 is specified for ac (or "dynamic") parameters such as S/N+D Ratio, THD and IMD which are important in signal processing applications. In addition, dc parameters are specified which are important in measurement applications.

PRELIMINARY TECHNICAL DATA

The AD675 operates from +5 V and ±12 V supplies and typically consumes 235 mW during conversion. The digital supply (V_{DD}) is separated from the analog supplies (V_{CC}, V_{EE}) for reduced digital crosstalk. An analog ground sense is provided for the analog input. Separate analog and digital grounds are also provided.

The AD675 is available in a 24-pin plastic "skinny" DIP or 24-pin side-brazed "skinny" DIP ceramic package. Screening to MIL-STD-883C Class B is available.

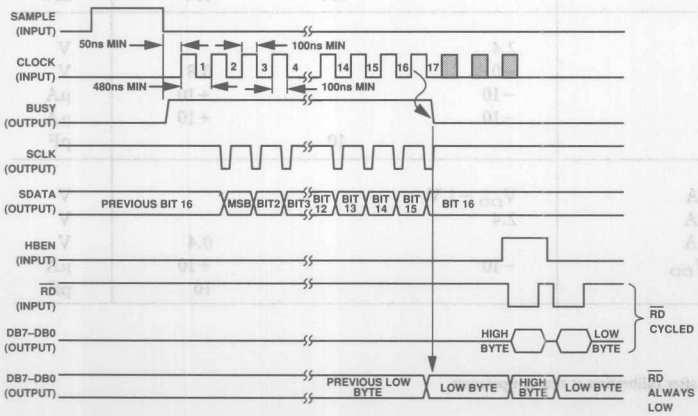
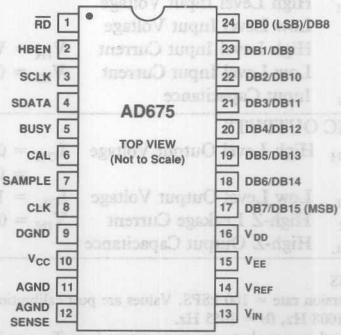


Figure 1. Conversion Timing

PIN CONFIGURATION



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD675—SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = + 12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)[1]

Parameter			Min	Typ	Max	Units
TOTAL HARMONIC DISTORTION (THD)						
−0.05 dB Input				−98	−90	dB
				0.0015	0.003	%
SIGNAL-TO-NOISE AND DISTORTION RATIO (S/(N+D))						
−0.05 dB Input, 50 kHz Bandwidth			87	90		dB
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT				−100	−92	dB
INTERMODULATION DISTORTION (IMD)[2]						
2nd Order Products				−102		dB
3rd Order Products				−98		dB
FULL POWER BANDWIDTH				1		MHz
TEMPERATURE RANGE			−40		+85	°C
ACCURACY						
Resolution			16			Bits
Integral Nonlinearity (INL)					±1	LSB
Differential Nonlinearity (DNL)—No Missing Codes			16			Bits
Bipolar Zero Error[3]					±1	LSB
Gain Error[3]					0.003	% FSR
Temperature Drift						
Bipolar Zero				0.002		% FSR
Gain				0.002		% FSR
VOLTAGE REFERENCE INPUT RANGE[1] (V_{REF})			5.0		10	V
ANALOG INPUT						
Input Range (V_{IN})					$\pm V_{REF}$	V
Input Capacitance During Sample				50		pF
Aperture Delay				6		ns
Aperture Jitter				100		ps
POWER SUPPLIES						
Power Supply Rejection						
V_{CC} = +12 V ± 5%				±1	±2	LSB
V_{EE} = −12 V ± 5%				±1	±2	LSB
V_{DD} = +5 V ± 10%				±1	±2	LSB
Operating Current						
I_{CC}				9	12	mA
I_{EE}				9	12	mA
I_{DD}				3	12	mA
Power Consumption				235	350	mW
LOGIC INPUTS						
V_{IH}	High Level Input Voltage		2.4			V
V_{IL}	Low Level Input Voltage		−0.3		0.8	V
I_{IH}	High Level Input Current	$V_{IH} = V_{DD}$	−10		+10	μA
I_{IL}	Low Level Input Current	V_{IL} = 0 V	−10		+10	μA
C_{IN}	Input Capacitance			10		pF
LOGIC OUTPUTS						
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	V_{DD} −1 V			V
		= 0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA			0.4	V
I_{OZ}	High-Z Leakage Current	V_{IN} = 0 or V_{DD}	−10		+10	μA
V_{OL}	High-Z Output Capacitance				10	pF

NOTES
[1]Conversion rate = 100 kSPS. Values are post calibration.
[2]fa = 1008 Hz, fb = 1055 Hz.
[3]Values shown apply to any temperature from T_{MIN} to T_{MAX} after calibration at that temperature.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

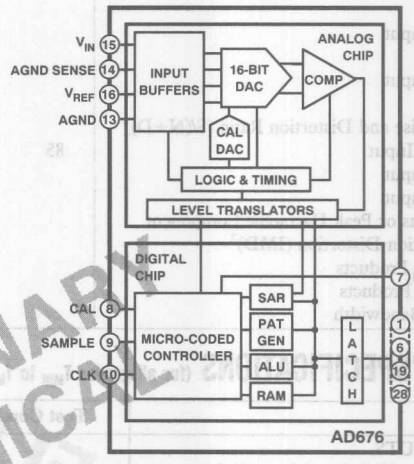
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16-Bit 100 kSPS Sampling ADC

AD676

FEATURES
Autocalibrating
On-Chip Sample-Hold Function
Twos Complement Parallel Output Format
16 Bits No Missing Codes
±1 LSB INL
0.002% THD
90 dB S/(N+D)
1 MHz Full Power Bandwidth

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

The AD676 is a multipurpose 16-bit parallel output analog-to-digital converter which utilizes a switched-capacitor/charge redistribution architecture to achieve a 100 kSPS conversion rate (10 μs total conversion time). Overall performance is optimized by digitally correcting internal nonlinearities through on-chip autocalibration.

The AD676 circuitry is segmented onto two monolithic chips—a digital control chip fabricated on Analog Devices DSP CMOS process and an analog ADC chip fabricated on our BiMOS II process. Both chips are contained in a single package.

The AD676 is specified for ac (or "dynamic") parameters such as S/(N+D) Ratio, THD and IMD which are important in signal processing applications. In addition, dc parameters are specified which are important in measurement applications.

The AD676 operates from +5 V and ±12 V supplies and typically consumes 235 mW during conversion. The digital supply (V_{DD}) is separated from the analog supplies (V_{CC}, V_{EE}) for reduced digital crosstalk. An analog ground sense is provided for the analog input. Separate analog and digital grounds are also provided.

The AD676 is available in a 28-pin plastic DIP or 28-pin side-brazed ceramic package.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD676—SPECIFICATIONS

AC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)[1]

Parameter	AD676J/A/T Min	AD676J/A/T Typ	AD676J/A/T Max	AD676K/B Min	AD676K/B Typ	AD676K/B Max	Units
Total Harmonic Distortion (THD)							
−0.05 dB Input		−95	−88		−98	−90	dB
		0.002	0.004		0.0015	0.003	%
−20 dB Input		−78			−80		dB
		0.01			0.01		%
−60 dB Input		−40			−45		dB
		1.0			0.05		%
Signal-to-Noise and Distortion Ratio (S/(N+D))							
−0.05 dB Input	85	88		87	90		dB
−20 dB Input		67			70		dB
−60 dB Input		32			34		dB
Peak Spurious or Peak Harmonic Component		−99	−89		−100	−92	dB
Intermodulation Distortion (IMD)[2]							
2nd Order Products		−102			−102		dB
3rd Order Products		−98			−98		dB
Full Power Bandwidth		1			1		MHz

DIGITAL SPECIFICATIONS (for all grades T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter		Test Conditions	Min	Typ	Max	Units
LOGIC INPUTS						
V_{IH}	High-Level Input Voltage		2.4			V
V_{IL}	Low-Level Input Voltage		−0.3		0.8	V
I_{IH}	High-Level Input Current	$V_{IH} = V_{DD}$	−10		+10	μA
I_{IL}	Low-Level Input Current	$V_{IL} = 0$ V	−10		+10	μA
C_{IN}	Input Capacitance			10		pF
LOGIC OUTPUTS						
V_{OH}	High-Level Output Voltage	I_{OH} = 0.1 mA	V_{DD} − 1 V			V
		= 0.5 mA	2.4			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 1.6 mA			0.4	V

NOTES

[1] V_{REF} = 10.0 V, Conversion Rate = 100 kSPS, f_{IN} = 1.0 kHz, V_{IN} = −0.05 dB, Bandwidth = 50 kHz unless otherwise indicated. All measurements referred to a 0 dB (20 V p–p) input signal. Values are post-calibration.

[2] fa = 1008 Hz, fb = 1055 Hz. See Definition of Specifications section and Figure 15.

Specifications subject to change without notice.

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DC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ±10%)[1]

Parameter	AD676J/A/T Min	AD676J/A/T Typ	AD676J/A/T Max	AD676K/B Min	AD676K/B Typ	AD676K/B Max	Units
TEMPERATURE RANGE							
J, K Grades	0		+70	0		+70	°C
A, B Grades	−40		+85	−40		+85	°C
T Grade	−55		+125	—		—	°C
ACCURACY							
Resolution	16			16			Bits
Integral Nonlinearity (INL)			±2			±1	LSB
Differential Nonlinearity (DNL)—No Missing Codes	15			16			Bits
Bipolar Zero Error[2]			±2			±1	LSB
Gain Error[2]			0.006			0.003	% FSR
Temperature Drift							
Bipolar Zero							
J, K Grades		0.003			0.001		% FSR
A, B Grades		0.004			0.002		% FSR
T Grade		0.007					% FSR
Gain							
J, K Grades		0.003			0.001		% FSR
A, B Grades		0.004			0.002		% FSR
T Grade		0.007					% FSR
VOLTAGE REFERENCE INPUT RANGE[3] (V_{REF})	5		10	5		10	V
ANALOG INPUT[4]							
Input Range (V_{IN})			±V_{REF}			±V_{REF}	V
Input Impedance		*			*		
Input Settling Time		2			2		µs
Input Capacitance During Sample			50*			50*	pF
Aperture Delay		6			6		ns
Aperture Jitter		100			100		ps
POWER SUPPLIES							
Power Supply Rejection							
V_{CC} = +12 V ± 5%		±1	±2		±1	±2	LSB
V_{EE} = −12 V ± 5%		±1	±2		±1	±2	LSB
V_{DD} = +5 V ± 10%		±1	±2		±1	±2	LSB
Operating Current							
I_{CC}		9	12		9	12	mA
I_{EE}		9	12		9	12	mA
I_{DD}		3	12		3	12	mA
Power Consumption		235	350		235	350	mW

NOTES
[1]V_{REF} = 5.0 V, Conversion Rate = 100 kSPS. Values are post-calibration.
[2]Values shown apply to any temperature from T_{MIN} to T_{MAX} after calibration at that temperature.
[3]See "APPLICATIONS" section for recommended voltage reference circuit, and Figure 12 for dynamic performance with other reference voltage values.
[4]See "APPLICATIONS" section for recommended input buffer circuit.
*For explanation of input characteristics, see "ANALOG INPUT" section.
Specifications subject to change without notice.

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TIMING SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%, V_{REF} = 10.0 V)[1]

Parameter	Symbol	Min	Typ	Max	Units
Conversion Period[2]	t_C	10		1000	µs
CLK Period	t_{CLK}	480			ns
Calibration Time	t_{CT}			85,530	t_C
Sampling Time (Included in t_C)	t_S	2			µs
CAL to BUSY Delay	t_{CALB}	0	20		ns
BUSY to SAMPLE Delay	t_{BS}	2			µs
SAMPLE to BUSY Delay	t_{SB}		20		ns
CLK HIGH[3]	t_{CH}	50			ns
CLK LOW[3]	t_{CL}	50			ns
SAMPLE LOW to 1st CLK Delay	t_{SC}	50			ns
SAMPLE LOW	t_{SL}	100			ns
Output Delay	t_{OD}		200		ns
Status Delay[4]	t_{SD}		20		ns
CAL HIGH Time	t_{CALH}	2			t_{CLK}

NOTES
[1]See the "CONVERSION CONTROL" and "AUTOCALIBRATION" sections for detailed explanations of the above timing.
[2]Depends upon external clock frequency; includes acquisition time and conversion time. The minimum sampling rate is specified to account for the droop of the internal sample/hold function. Operation at slower rates may degrade performance.
[3]t_{CH} + t_{CL} = t_{CLK} and must be greater than 480 ns.
[4]Tested with 100 pF load.

PRELIMINARY TECHNICAL DATA

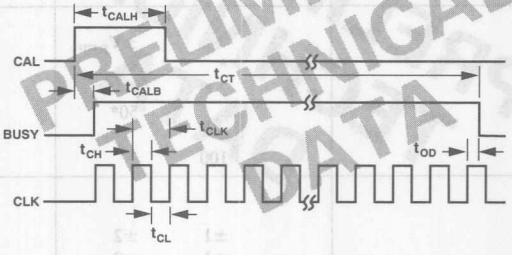


Figure 1. Calibration Timing

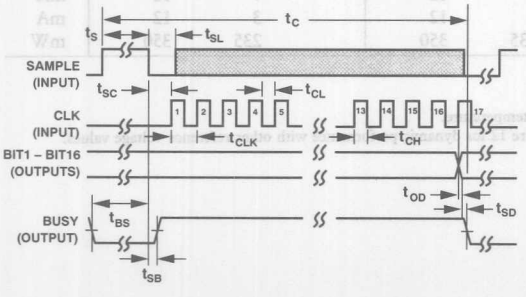


Figure 2a. General Conversion Timing

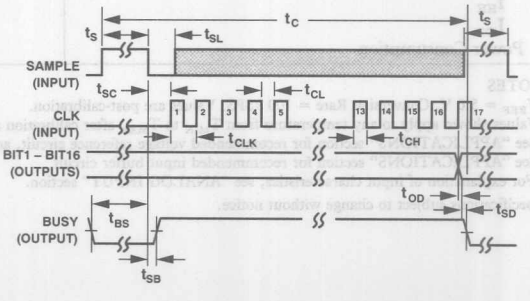


Figure 2b. Continuous Conversion Timing

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ORDERING GUIDE

Model	Temperature Range	S/(N+D)	INL	Package Description	Package Option*
AD676JN	0°C to +70°C	85 dB	±2 LSB	Plastic 28-Pin DIP	N-28
AD676KN	0°C to +70°C	87 dB	±1 LSB	Plastic 28-Pin DIP	N-28
AD676AD	−40°C to +85°C	85 dB	±2 LSB	Ceramic 28-Pin DIP	D-28
AD676BD	−40°C to +85°C	87 dB	±1 LSB	Ceramic 28-Pin DIP	D-28
AD676TD	−55°C to +125°C	85 dB	±2 LSB	Ceramic 28-Pin DIP	D-28

*D = Ceramic DIP; N = Plastic DIP. For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to DGND . . . . . 0 to +5.5 V
V_{CC} to AGND . . . . . 0 to +12.6 V
V_{EE} to AGND . . . . . 0 to −12.6 V
AGND to DGND . . . . . ±0.3 V
Digital Inputs to DGND . . . . . 0 to +5.5 V
Analog Inputs to AGND . . . . . $\pm V_{REF}$
Soldering . . . . . +300°C, 10 sec
Storage Temperature . . . . . −60°C to +100°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PRELIMINARY TECHNICAL DATA

CAUTION

The AD676 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD676 has been classified as a Category 1 Device.



Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment, and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam discharged to the destination socket before devices are removed. For further information on ESD precaution, refer to Analog Devices' *ESD Prevention Manual*.

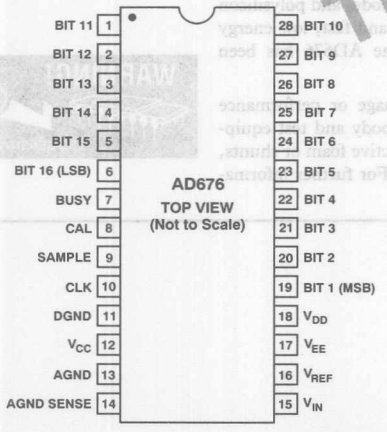
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PIN DESCRIPTION

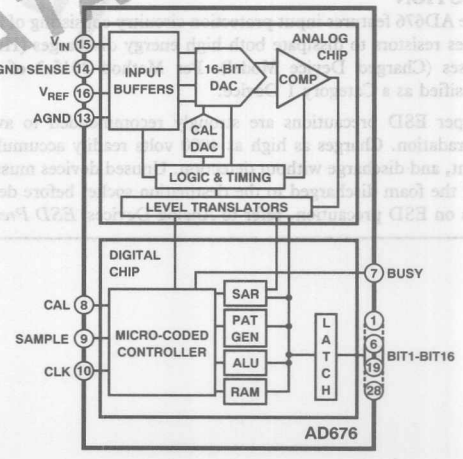
Pin	Name	Type	Description
1–6	BIT11–BIT16	DO	BIT11–BIT16 represent the six LSBs of data.
7	BUSY	DO	Status Line for Converter. Active HIGH, indicating a conversion or calibration in progress. BUSY should be buffered when capacitively loaded.
8	CAL	DI	Calibration Control Pin (Asynchronous).
9	SAMPLE	DI	V_{IN} Acquisition Control Pin. Active HIGH. During conversion, SAMPLE controls the state of the internal sample-hold amplifier and the falling edge initiates conversion (see "Conversion Control" paragraph). During calibration, SAMPLE should be held LOW. If HIGH during calibration, diagnostic information will appear on the two LSBs (Pins 5 and 6).
10	CLK	DI	Master Clock Input. The AD676 requires 17 clock cycles to execute a conversion.
11	DGND	P	Digital Ground.
12	V_{CC}	P	+12 V Analog Supply Voltage.
13	AGND	P/AI	Analog Ground.
14	AGND SENSE	AI	Analog Ground Sense.
15	V_{IN}	AI	Analog Input Voltage.
16	V_{REF}	AI	External Voltage Reference Input.
17	V_{EE}	P	−12 V Analog Supply Voltage.
18	V_{DD}	P	+5 V Logic Supply Voltage.
19–28	BIT1–BIT10	DO	BIT1–BIT10 represent the ten MSB of data.

Type: AI = Analog Input
DI = Digital Input
DO = Digital Output
P = Power

PRELIMINARY TECHNICAL DATA



Package Pinout



Functional Block Diagram

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NYQUIST FREQUENCY
An implication of the Nyquist sampling theorem, the "Nyquist frequency" of a converter is that input frequency which is one half the sampling frequency of the converter.

TOTAL HARMONIC DISTORTION
Total harmonic distortion (THD) is the ratio of the rms sum of the harmonic components to the rms value of a full-scale input signal and is expressed in percent (%) or decibels (dB). For input signals or harmonics that are above the Nyquist frequency, the aliased components are used.

SIGNAL-TO-NOISE PLUS DISTORTION RATIO
Signal-to-noise plus distortion is defined to be the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

GAIN ERROR
The last transition should occur at an analog value 1.5 LSB below the nominal full scale (4.99977 volts for a ±5 V range). The gain error is the deviation of the actual difference between the first and last code transition from the ideal difference between the first and last code transition.

BIPOLAR ZERO ERROR
Bipolar zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

DIFFERENTIAL NONLINEARITY (DNL)
In an ideal ADC, code transitions are one LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

INTEGRAL NONLINEARITY (INL)
The ideal transfer function for an ADC is a straight line drawn between "zero" and "full scale." The point used as "zero" occurs 1/2 LSB before the most negative code transition. "Full scale" is defined as a level 1.5 LSB beyond the most positive code transition. Integral nonlinearity is the worst-case deviation of a code from the straight line. The deviation of each code is measured from the middle of that code.

BANDWIDTH
The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb), and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (fa − 2 fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude, and the peak value of their sum is −0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

APERTURE DELAY
Aperture delay is the time required after SAMPLE pin is taken LOW for the internal sample-hold of the AD676 to open, thus holding the value of V_{IN}.

APERTURE JITTER
Aperture jitter is the variation in the aperture delay from sample to sample.

POWER SUPPLY REJECTION
DC variations in the power supply voltage will affect the full-scale transition point, resulting in gain error. Power supply rejection is the maximum change in the full-scale transition point due to a change in power-supply voltage from the nominal value. Additionally, there is another power supply variation to consider. AC ripple on the power supplies can couple noise into the ADC, resulting in degradation of dynamic performance. This is displayed in Figure 15.

INPUT SETTLING TIME
Settling time is a function of the SHA'a ability to track fast slewing signals. This is specified as the maximum time required in track mode after a full-scale step input to guarantee rated conversion accuracy.

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FUNCTIONAL DESCRIPTION

The AD676 is a multipurpose 16-bit analog-to-digital converter and includes circuitry which performs an input sample/hold function, ground sense, and autocalibration. These functions are segmented onto two monolithic chips—an analog signal processor and a digital controller. Both chips are contained within the AD676 package.

The AD676 employs a successive-approximation technique to determine the value of the analog input voltage. However, instead of the traditional laser-trimmed resistor-ladder approach, this device uses a capacitor-array, charge redistribution technique. Binary-weighted capacitors subdivide the input sample to perform the actual analog-to-digital conversion. The capacitor array eliminates variation in the linearity of the device due to temperature-induced mismatches of resistor values. Since a capacitor array is used to perform the data conversions, the sample/hold function is included without the need for additional external circuitry.

Initial errors in capacitor matching are eliminated by an autocalibration circuit within the AD676. This circuit employs an on-chip microcontroller and a calibration DAC to measure and compensate capacitor mismatch errors. As each error is determined, its value is stored in on-chip memory (RAM). Subsequent conversions use these RAM values to improve conversion accuracy. The autocalibration routine may be invoked at any time. Autocalibration insures high performance while eliminating the need for any user adjustments and is described in detail below.

The microcontroller controls all of the various functions within the AD676. These include the actual successive approximation algorithm, the autocalibration routine, the sample/hold operation, and the internal output data latch.

AUTOCALIBRATION

The AD676 achieves rated performance without the need for user trims or adjustments. This is accomplished through the use of on-chip autocalibration.

In the autocalibration sequence, sample/hold offset is nulled by internally connecting the input circuit to the ground sense circuit. The resulting offset voltage is measured and stored in RAM for later use. Next, the capacitor representing the most significant bit (MSB) is charged to the reference voltage. This charge is then transferred to a capacitor of equal size (composed of the sum of the remaining lower weight bits). The difference in the voltage that results and the reference voltage represents the amount of capacitor mismatch. A calibration digital-to-analog converter (DAC) adds an appropriate value of error correction voltage to cancel this mismatch. This correction factor is also stored in RAM. This process is repeated for each of the capacitors representing the remaining top eight bits. The accumulated values in RAM are then used during subsequent conversions to adjust conversion results accordingly.

As shown in Figure 1, when CAL is taken HIGH the AD676 internal circuitry is reset, the BUSY pin is driven HIGH, and the ADC prepares for calibration. This is an asynchronous hardware reset and will interrupt any conversion or calibration currently in progress. Actual calibration begins when CAL is taken LOW and completes in 85,530 clock cycles, indicated by BUSY going LOW. During calibration, it is preferable for SAMPLE to be held LOW. If SAMPLE is HIGH, diagnostic data will appear on Pins 5 and 6. This data is of no value to the user.

The AD676 requires one clock cycle after BUSY goes LOW to complete the calibration cycle. If this clock cycle is not provided, it will be taken from the first conversion, likely resulting in first conversion error.

In most applications, it is sufficient to calibrate the AD676 only upon power-up, in which case care should be taken that the power supplies and voltage reference have stabilized first.

CONVERSION CONTROL

The AD676 is controlled by two signals: SAMPLE and CLK, as shown in Figures 2a and 2b. It is assumed that the part has been calibrated and the digital I/O pins have the levels shown at the start of the timing diagram.

A conversion consists of an input acquisition followed by 17 clock pulses which execute the 16-bit internal successive approximation routine. The analog input is acquired by taking the SAMPLE line HIGH for a minimum sampling time of t_S. The actual sample taken is the voltage present on V_{IN} one aperture delay after the SAMPLE line is brought LOW, assuming the previous conversion has completed (signified by BUSY going LOW). Care should be taken to ensure that this negative edge is well defined and jitter free in ac applications to reduce the uncertainty (noise) in signal acquisition. With SAMPLE going LOW, the AD676 commits itself to the conversion—the input at V_{IN} is disconnected from the internal capacitor array, BUSY goes HIGH, and the SAMPLE input will be ignored until the conversion is completed (when BUSY goes LOW). SAMPLE must be held LOW for a minimum period of time t_{SL}. A period of time t_{SC} after bringing SAMPLE LOW, the 17 CLK cycles are applied; CLK pulses that start before this period of time are ignored. BUSY goes HIGH t_{SB} after SAMPLE goes LOW, signifying that a conversion is in process, and remains HIGH until the conversion is completed. BUSY goes LOW during the 17th CLK cycle at the point where the data outputs have changed and are valid. The AD676 will ignore CLK after BUSY has gone LOW and the output data will remain constant until a new conversion is completed. The data can, therefore, be read any time after BUSY goes LOW and before the 17th CLK of the next conversion (see Figures 2a and 2b). The section on Microprocessor Interfacing discusses how the AD676 can be interfaced to a 16-bit databus.

Typically BUSY would be used to latch the AD676 output data into buffers or to interrupt microprocessors or DSPs. It is recommended that the capacitive load on BUSY be minimized by driving no more than a single logic input. Higher capacitive loads such as cables or multiple gates may degrade conversion quality unless BUSY is buffered.

CONTINUOUS CONVERSION

For maximum throughput rate, the AD676 can be operated in a continuous convert mode (see Figure 2b). This is accomplished

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by utilizing the fact that SAMPLE will no longer be ignored after BUSY goes LOW, so an acquisition may be initiated even during the HIGH time of the 17th CLK pulse for maximum throughput rate while enabling full settling of the sample/hold circuitry. If SAMPLE is already HIGH when BUSY goes LOW at the end of a conversion, then an acquisition is immediately initiated and t_S and t_C start from that time. Data from the previous conversion may be latched up to t_{SD} before BUSY goes LOW or t_{OD} after the rising edge of the 17th clock pulse. However, it is preferred that latching occur on or after the falling edge of BUSY.

Care must be taken to adhere to the minimum/maximum timing requirements in order to preserve conversion accuracy.

GENERAL CONVERSION GUIDELINES

During signal acquisition and conversion, care should be taken with the logic inputs to avoid digital feedthrough noise. It is possible to run CLK continuously, even during the sample period. However, CLK edges during the sampling period, and especially when SAMPLE goes LOW, may inject noise into the sampling process. The AD676 is tested with no CLK cycles during the sampling period. The BUSY signal can be used to prevent the clock from running during acquisition, as illustrated in Figure 3. In this circuit BUSY is used to reset the circuitry which divides the system clock down to provide the AD676 CLK. This serves to interrupt the clock until after the input signal has been acquired, which has occurred when BUSY goes HIGH. When the conversion is completed and BUSY goes LOW, the circuit in Figure 3 truncates the 17th CLK pulse width which is tolerable because only its rising edge is critical.

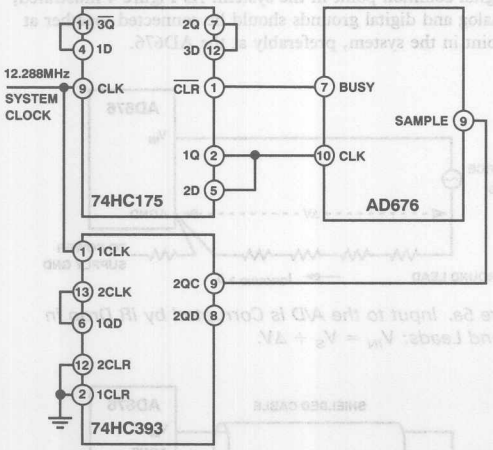


Figure 3.

Figure 3 also illustrates the use of a counter (74HC393) to derive the AD676 SAMPLE command from the system clock when a continuous convert mode is desirable. Pin 9 (2QC) provides a 96 kHz sample rate for the AD676 when used with a 12.288 MHz system clock. Alternately, Pin 8 (2QD) could be used for a 48 kHz rate.

If a continuous clock is used, then the user must avoid CLK edges at the instant of disconnecting V_{IN} which occurs at the falling edge of SAMPLE (see t_{SC} specification). The duty cycleof CLK may vary, but both the HIGH (t_{CH}) and LOW (t_{CL}) phases must conform to those shown in the timing specifications. The internal comparator makes its decisions on the rising edge of CLK. To avoid a negative edge transition disturbing the comparator's settling, t_{CL} should be at least half the value of t_{CLK}. To also avoid transitions disturbing the internal comparator's settling, it is not recommended that the SAMPLE pin change state toward the end of a CLK cycle.

During a conversion, internal dc error terms such as comparator voltage offset are sampled, stored on internal capacitors and used to correct for their corresponding errors when needed. Because these voltages are stored on capacitors, they are subject to leakage decay and so require refreshing. For this reason there is a maximum conversion time t_C.

Output coding for the AD676 is twos complement, as shown in the following table. By inverting the MSB, the coding can be converted to offset binary.

Table 1. Output Coding

V_{IN}	Output Code
Full Scale	011 . . . 11
Full Scale − 1 LSB	011 . . . 10
Midscale + 1 LSB	000 . . . 01
Midscale	000 . . . 00
Midscale − 1 LSB	111 . . . 11
−Full Scale + 1 LSB	100 . . . 01
−Full Scale	100 . . . 00

POWER SUPPLIES AND DECOUPLING

The AD676 has three power supply input pins. V_{CC} and V_{EE} provide the supply voltages to operate the analog portions of the AD676 including the ADC and sample-hold amplifier (SHA). V_{DD} provides the supply voltage which operates the digital portions of the AD676 including the data output buffers and the autocalibration controller.

As with most high performance linear circuits, changes in the power supplies can produce undesired changes in the performance of the circuit. Optimally, well regulated power supplies with less than 1% ripple should be selected. The ac output impedance of a power supply is a complex function of frequency, and in general will increase with frequency. In other words, high frequency switching such as that encountered with digital circuitry requires fast transient currents which most power supplies cannot adequately provide. This results in voltage spikes on the supplies. If these spikes exceed the ±5% tolerance of the ±12 V supplies or the ±10% limits of the +5 V supply, ADC performance will degrade. Additionally, spikes at frequencies higher than 100 kHz will also degrade performance. To compensate for the finite ac output impedance of the supplies, it is necessary to store "reserves" of charge in bypass capacitors. These capacitors can effectively lower the ac impedance presented to the AD676 power inputs which in turn will significantly reduce the magnitude of the voltage spikes. For bypassing to be effective, certain guidelines should be followed. Decoupling capacitors, typically 0.1 μF, should be placed as closely as possible to each power supply pin of the AD676. It is essential that these

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capacitors be placed physically close to the IC to minimize the inductance of the PCB trace between the capacitor and the supply pin. The logic supply (V_{DD}) should be decoupled to digital common and the analog supplies (V_{CC} and V_{EE}) to analog common. The reference input is also considered as a power supply pin in this regard and the same decoupling procedures apply. These points are displayed in Figure 4.

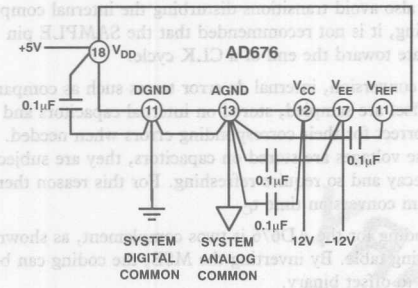


Figure 4. Grounding and Decoupling the AD676

Additionally, it is beneficial to have large capacitors (>47 μF) located at the point where the power connects to the PCB with 10 μF capacitors located in the vicinity of the ADC to further reduce low frequency ripple. In systems that will be subjected to particularly harsh environmental noise, additional decoupling may be necessary. RC-filtering on each power supply combined with dedicated voltage regulation can substantially decrease power supply ripple effects (this is further detailed in Figure 7).

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is a significant issue. A 1.22 mA current through a 0.5 Ω trace will develop a voltage drop of 0.6 mV, which is 4 LSBs at the 16-bit level for a 10 V full-scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals.

Analog and digital signals should not share a common return path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point at the AD676 to minimize interference between analog and digital circuitry. Analog signals should be routed as far as possible from digital signals and should cross them, if at all, only at right angles. A solid analog ground plane around the AD676 will isolate it from large switching ground currents. For these reasons, the use of wire wrap circuit construction will not provide adequate performance; careful printed circuit board construction is preferred.

GROUNDING

The AD676 has three grounding pins, designated ANALOG GROUND (AGND), DIGITAL GROUND (DGND) and ANALOG GROUND SENSE (AGND SENSE). The analog ground pin is the "high quality" ground reference point for the device, and should be connected to the analog common point in the system.

AGND SENSE is intended to be connected to the input signal ground reference point. This allows for slight differences in level between the analog ground point in the system and the input signal ground point. However no more than 100 mV is recommended between the AGND and the AGND SENSE pins for specified performance.

Using AGND SENSE to remotely sense the ground potential of the signal source can be useful if the signal has to be carried some distance to the A/D converter. Since all IC ground currents have to return to the power supply and no ground leads are free from resistance and inductance, there are always some voltage differences from one ground point in a system to another.

Over distance this voltage difference can easily amount to several LSBs (in a 10 V input span, 16-bit system each LSB is about 0.15 mV). This would directly corrupt the A/D input signal if the A/D measures its input with respect to power ground (AGND) as shown in Figure 5a. To solve this problem the AD676 offers an AGND SENSE pin. Figure 5b shows how the AGND SENSE can be used to eliminate the problem in Figure 5a. Figure 5b also shows how the signal wires should be shielded in a noisy environment to avoid capacitive coupling. If inductive (magnetic) coupling is expected to be dominant such as where motors are present, twisted-pair wires should be used instead.

The digital ground pin is the reference point for all of the digital signals that operate the AD676. This pin should be connected to the digital common point in the system. As Figure 4 illustrated, the analog and digital grounds should be connected together at one point in the system, preferably at the AD676.

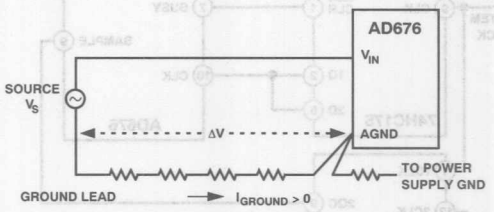


Figure 5a. Input to the A/D Is Corrupted by IR Drop in Ground Leads: $V_{IN} = V_S + \Delta V$.

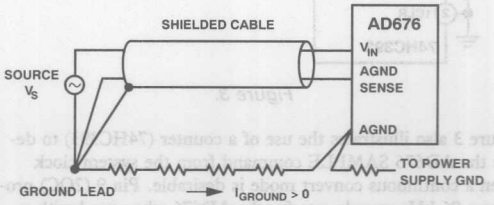


Figure 5b. AGND SENSE Eliminates the Problem in Figure 5a.

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VOLTAGE REFERENCE

The AD676 requires the use of an external voltage reference. The input voltage range is determined by the value of the reference voltage; in general, a reference voltage of n volts allows an input range of ±n volts. The AD676 is specified for both 10 V and 5.0 V references. A 10 V reference will typically require support circuitry operated from ±15 V supplies; a 5.0 V reference may be used with ±12 V supplies. Signal-to-noise performance is increased proportionately with input signal range. In the presence of a fixed amount of system noise, increasing the LSB size (which results from increasing the reference voltage) will increase the effective S/(N+D) performance. Figure 12 illustrates S/(N+D) as a function of reference voltage. In contrast, INL will be optimal at lower reference voltage values (such as 5 V) due to capacitor nonlinearity at higher voltage values.

During a conversion, the switched capacitor array of the AD676 presents a dynamically changing current load at the voltage reference as the successive-approximation algorithm cycles through various choices of capacitor weighting. The output impedance of the reference circuitry must be low so that the output voltage will remain sufficiently constant as the current drive changes. In some applications, this may require that the output of the voltage reference be buffered by an amplifier with low impedance at relatively high frequencies. In choosing a voltage reference, consideration should be made for selecting one with low noise. A capacitor connected between REF IN and AGND will reduce the demands on the reference by decreasing the magnitude of high frequency components required to be sourced by the reference.

Figures 6 and 7 represent typical design approaches.

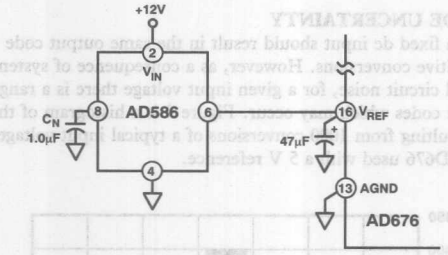


Figure 6.

Figure 6 shows a voltage reference circuit featuring the 5 V output AD586. The AD586 is a low cost reference which utilizes a buried Zener architecture to provide low noise and drift. Over the 0°C to +70°C range, the AD586L grade exhibits less than 2.25 mV output change from its initial value at +25°C. A noise-reduction capacitor, C_N, reduces the broadband noise of the AD586 output, thereby optimizing the overall performance of the AD676. It is recommended that a 10 µF to 47 µF high quality tantalum capacitor be tied between the V_{REF} input of the AD676 and ground to minimize the impedance on the reference.

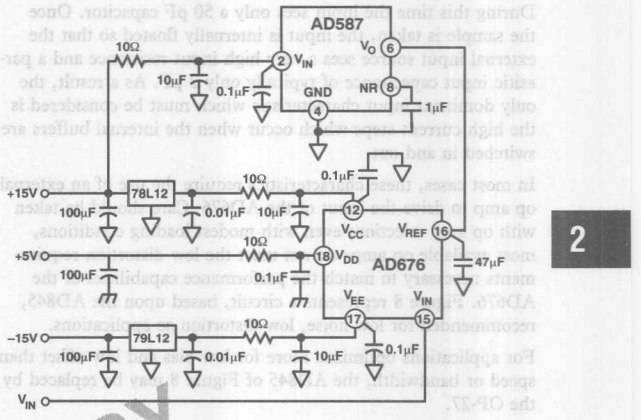


Figure 7.

Using the AD676 with ±10 V input range (V_{REF} = 10 V) typically requires ±15 V supplies to drive op amps and the voltage reference. If ±12 V is not available in the system, regulators such as 78L12 and 79L12 can be used to provide power for the AD676. This is also the recommended approach (for any input range) when the ADC system is subjected to harsh environments such as where the power supplies are noisy and where voltage spikes are present. Figure 7 shows an example of such a system based upon the 10 V AD587 reference, which provides a 300 µV LSB. Circuitry for additional protection against power supply disturbances has been shown. A 100 µF capacitor at each regulator prevents very large voltage spikes from entering the regulators. Any power line noise which the regulators cannot eliminate will be further filtered by an RC filter (10 Ω/10 µF) having a −3 dB point at 1.6 kHz. For best results the regulators should be within a few centimeters of the AD676.

ANALOG INPUT

As previously discussed, the analog input voltage range for the AD676 is ±V_{REF}. For purposes of ground drop and common mode rejection, the V_{IN} and V_{REF} inputs each have their own ground. V_{REF} is referred to the local analog system ground (AGND), and V_{IN} is referred to the analog ground sense pin (AGND SENSE) which allows a remote ground sense for the input signal.

The AD676 analog inputs (V_{IN}, V_{REF} and AGND SENSE) exhibit dynamic characteristics. When a conversion cycle begins, each analog input is connected to an internal, discharged 50 pF capacitor which then charges to the voltage present at the corresponding pin. The capacitor is disconnected when SAMPLE is taken LOW, and the stored charge is used in the subsequent conversion. In order to limit the demands placed on the external source by this high initial charging current, an internal buffer amplifier is employed between the input and this capacitance for a few hundred nanoseconds. During this time the input pin exhibits typically 20 kΩ input resistance, 10 pF input capacitance and ±40 µA bias current. Next, the input is switched directly

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to the now precharged capacitor and allowed to fully settle. During this time the input sees only a 50 pF capacitor. Once the sample is taken, the input is internally floated so that the external input source sees a very high input resistance and a parasitic input capacitance of typically only 2 pF. As a result, the only dominant input characteristic which must be considered is the high current steps which occur when the internal buffers are switched in and out.

In most cases, these characteristics require the use of an external op amp to drive the input of the AD676. Care should be taken with op amp selection; even with modest loading conditions, most available op amps do not meet the low distortion requirements necessary to match the performance capabilities of the AD676. Figure 8 represents a circuit, based upon the AD845, recommended for low noise, low distortion ac applications.

For applications optimized more for low bias and low offset than speed or bandwidth, the AD845 of Figure 8 may be replaced by the OP-27.

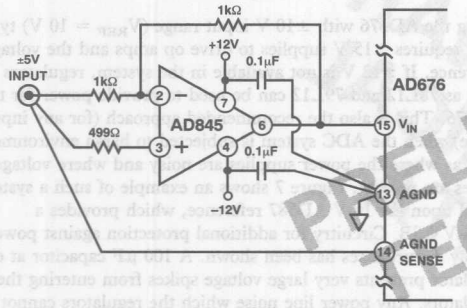


Figure 8.

AC PERFORMANCE

AC parameters, which include S/(N+D), THD, etc., reflect the AD676's effect on the spectral content of the analog input signal. Figures 12 through 16 provide information on the AD676's ac performance under a variety of conditions.

As a general rule, averaging the results from several conversions reduces the effects of noise, and therefore improves such parameters as S/(N+D). AD676 performance may be optimized by operating the device at its maximum sample rate of 100 kSPS and digitally filtering the resulting bit stream to the desired signal bandwidth. This succeeds in distributing noise over a wider frequency range, thus reducing the noise density in the frequency band of interest. This subject is discussed in the following section.

OVERSAMPLING AND NOISE FILTERING

The Nyquist rate for a converter is defined as one-half its sampling rate. This is established by the Nyquist theorem, which requires that a signal be sampled at a rate corresponding to at least twice its highest frequency component of interest in order to preserve the informational content. Oversampling is a conversion technique in which the sampling frequency is more than twice the frequency bandwidth of interest. In audio applications, the AD676 can operate at a 2 × F_S oversampling rate, where F_S = 48 kHz.

In quantized systems, the informational content of the analog input is represented in the frequency spectrum from dc to the Nyquist rate of the converter. Within this same spectrum are higher frequency noise and signal components. Antialias, or low pass, filters are used at the input to the ADC to reduce these noise and signal components so that their aliased components do not corrupt the baseband spectrum. However, wideband noise contributed by the AD676 will not be reduced by the antialias filter. The AD676 quantization noise is evenly distributed from dc to the Nyquist rate, and this fact can be used to minimize its overall affect.

The AD676 quantization noise effects can be reduced by oversampling—sampling at a rate higher than that defined by the Nyquist theorem. This spreads the noise energy over a bandwidth wider than the frequency band of interest. By judicious selection of a digital decimation filter, noise frequencies outside the bandwidth of interest may be eliminated.

The process of analog to digital conversion inherently produces noise, known as quantization noise. The magnitude of this noise is a function of the resolution of the converter, and manifests itself as a limit to the theoretical signal-to-noise ratio achievable. This limit is described by S/(N+D) = (6.02n + 1.76 + 10 log $F_S/2F_A$) dB, where n is the resolution of the converter in bits, F_S is the sampling frequency, and Fa is the signal bandwidth of interest. For audio bandwidth applications, the AD676 is capable of operating at a 2 × oversample rate (96 kSPS), which typically produces an improvement in S/(N+D) of 3 dB compared with operating at the Nyquist conversion rate of 48 kSPS. Oversampling has another advantage as well; the demands on the antialias filter are lessened. In summary, system performance is optimized by running the AD676 at or near its maximum sampling rate of 100 kHz and digitally filtering the resulting spectrum to eliminate undesired frequencies.

DC CODE UNCERTAINTY

Ideally, a fixed dc input should result in the same output code for repetitive conversions. However, as a consequence of system noise and circuit noise, for a given input voltage there is a range of output codes which may occur. Figure 9 is a histogram of the codes resulting from 1000 conversions of a typical input voltage by the AD676 used with a 5 V reference.

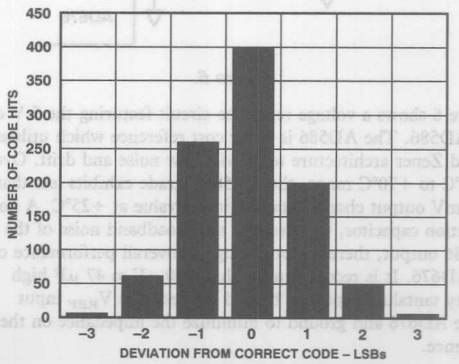


Figure 9. Distribution of Codes from 1000 Conversions, Relative to the Correct Code.

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The standard deviation of this distribution is approximately 1 LSB. If less uncertainty is desired, averaging multiple conversions will narrow this distribution by the inverse of the square root of the number of samples; i.e., the average of 4 conversions would have a standard deviation of 0.5 LSBs and the average of 16 conversions would have a standard deviation of 0.25 LSBs.

MICROPROCESSOR INTERFACE

The AD676 is ideally suited for use in both traditional dc measurement applications supporting a microprocessor, and in ac signal processing applications interfacing to a digital signal processor. The AD676 is designed to interface with a 16-bit data bus, providing all output data bits in a single read cycle. A variety of external buffers, such as 74HC541, can be used with the AD676 to provide 3-state outputs, high driving capability, and to prevent bus noise from coupling into the ADC. The following sections illustrate the use of the AD676 with a representative digital signal processor and microprocessor. These circuits provide general interface practices which are applicable to other processor choices.

ADSP-2101

Figure 10a shows the AD676 interfaced to the ADSP-2101 DSP processor. The AD676 buffers are mapped in the ADSP-2101's memory space, requiring one wait state when using a 12.5 MHz processor clock.

The falling edge of BUSY interrupts the processor, indicating that new data is ready. The ADSP-2101 automatically jumps to the appropriate service routine with minimal overhead. The interrupt routine then instructs the processor to read the new data using a memory read instruction.

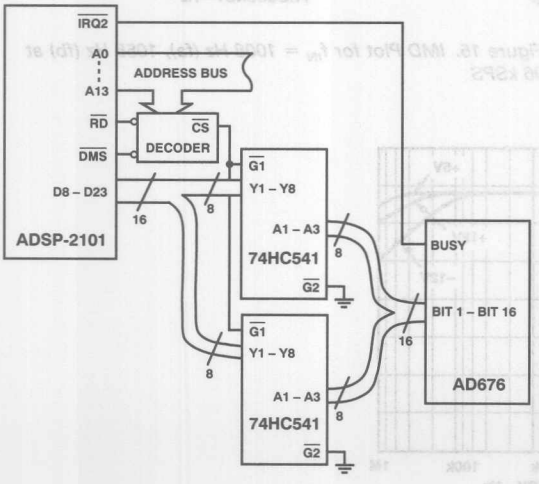


Figure 10a.

Figure 10b shows circuitry which would be included by a typical address decoder for the output buffers. In this case, a data memory access to any address in the range 3000H to 37FFH will result in the output buffers being enabled.

The AD676 CLK and SAMPLE can be generated by dividing down the system clock as described earlier (Figure 3), or if the ADSP-2101 serial port clocks are not being used, they can be programmed to generate CLK and SAMPLE.

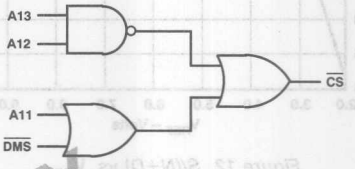


Figure 10b.

80286

The 80286 16-bit microprocessor can be interfaced to a buffered AD676 without any generation of wait states. As seen in Figure 11, BUSY can be used both to control the AD676 clock and to alert the processor when new data is ready. In the system shown, the 80286 should be configured in an edge triggered, direct interrupt mode (integrated controller provides the interrupt vector). Since the 80286 does not latch interrupt signals, the interrupt needs to be internally acknowledged before BUSY goes HIGH again during the next AD676 conversion (BUSY = 0). Depending on whether the AD676 buffers are mapped into memory or I/O space, the interrupt service routine will read the data by using either the MOV or the IN instruction. To be able to read all the 16 bits at once, and thereby increase the 80286's efficiency, the buffers should be located at an even address.

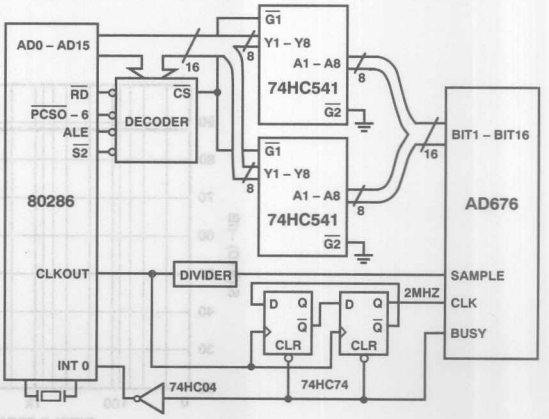


Figure 11.

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AD676—Typical Dynamic Performance

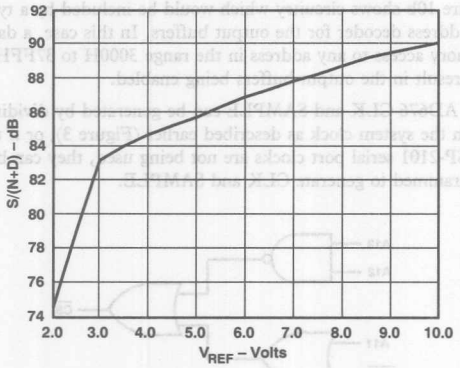


Figure 12. S/(N+D) vs. V_{REF}

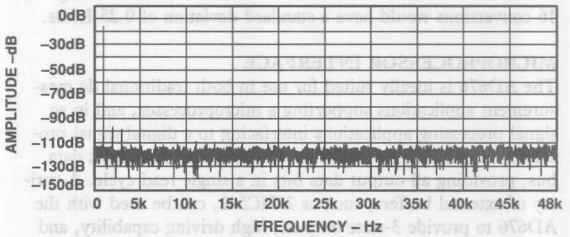


Figure 14. 4096 Point FFT at 96 kSPS, f_{IN} = 1.06 kHz

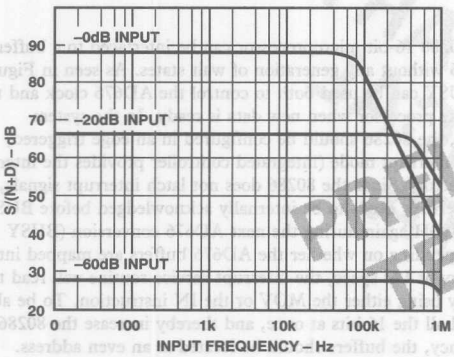


Figure 13. S/(N+D) vs. Input Frequency and Amplitude

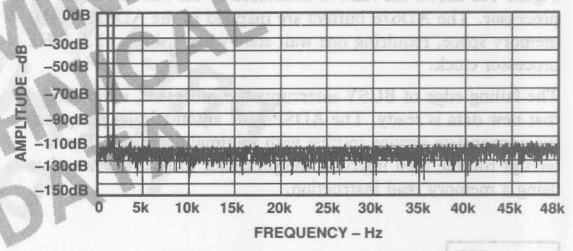


Figure 15. IMD Plot for f_{IN} = 1008 Hz (fa), 1055 Hz (fb) at 96 kSPS

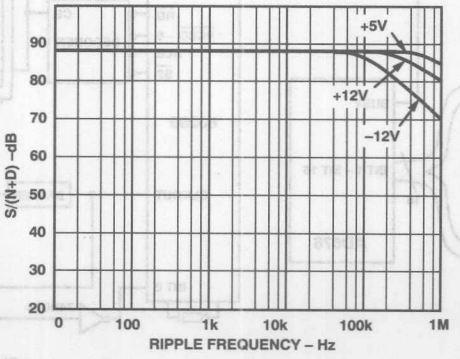


Figure 16. Power Supply Rejection (f_{IN} = 1.06 kHz) f_{SAMPLE} = 96 kSPS, V_{RIPPLE} = 0.13 V p–p

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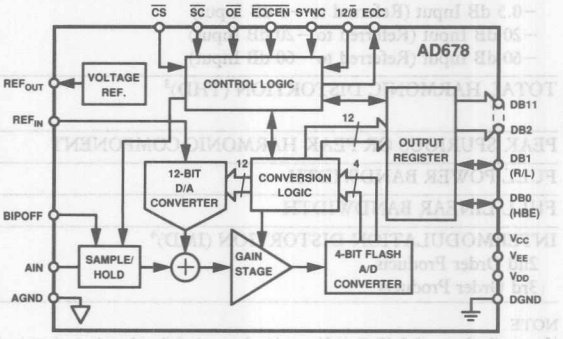
12-Bit 200 kSPS Complete Sampling ADC

AD678*

FEATURES

- AC and DC Characterized and Specified (K, B and T Grades)
- 200k Conversions per Second
- 1 MHz Full Power Bandwidth
- 500 kHz Full Linear Bandwidth
- 72 dB S/N+D (K, B, T Grades)
- Twos Complement Data Format (Bipolar Mode)
- Straight Binary Data Format (Unipolar Mode)
- 10 MΩ Input Impedance
- 8-Bit or 16-Bit Bus Interface
- On-Board Reference and Clock
- 10 V Unipolar or Bipolar Input Range
- Commercial, Industrial and Military Temperature Range Grades
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD678 is a complete, multipurpose 12-bit monolithic analog-to-digital converter, consisting of a sample-hold amplifier (SHA), a microprocessor compatible bus interface, a voltage reference and clock generation circuitry.

The AD678 is specified for ac (or "dynamic") parameters such as S/N+D ratio, THD and IMD which are important in signal processing applications. In addition, the AD678K, B and T grades are fully specified for dc parameters which are important in measurement applications.

The AD678 offers a choice of digital interface formats; the 12 data bits can be accessed by a 16-bit bus in a single read operation or by an 8-bit bus in two read operations (8+4), with right or left justification. Data format is straight binary for unipolar mode and twos complement binary for bipolar mode. The input has a full-scale range of 10 V with a full power bandwidth of 1 MHz and a full linear bandwidth of 500 kHz. High input impedance (10 MΩ) allows direct connection to unbuffered sources without signal degradation.

This product is fabricated on Analog Devices' BiMOS process, combining low power CMOS logic with high precision, low noise bipolar circuits; laser-trimmed thin-film resistors provide high accuracy. The converter utilizes a recursive subranging algorithm which includes error correction and flash converter circuitry to achieve high speed and resolution.

The AD678 operates from +5 V and ±12 V supplies and dissipates 560 mW (typ). The AD678 is available in 28-pin plastic DIP, ceramic DIP, and 44 J-leaded ceramic surface mount packages.

Screening to MIL-STD-883C Class B is also available.

***Protected by U.S. Patent Nos. 4,804,960; 4,814,767; 4,833,345; 4,250,445; 4,808,908; RE30,586.**

PRODUCT HIGHLIGHTS

1. COMPLETE INTEGRATION: The AD678 minimizes external component requirements by combining a high speed sample-hold amplifier (SHA), ADC, 5 V reference, clock and digital interface on a single chip. This provides a fully specified sampling A/D function unattainable with discrete designs.
2. SPECIFICATIONS: The AD678K, B and T grades provide fully specified and tested ac and dc parameters. The AD678J, A and S grades are specified and tested for ac parameters; dc accuracy specifications are shown as typicals. DC specifications (such as INL, gain and offset) are important in control and measurement applications. AC specifications (such as S/N+D ratio, THD and IMD) are of value in signal processing applications.
3. EASE OF USE: The pinout is designed for easy board layout, and the choice of single or two read cycle output provides compatibility with 16- or 8-bit buses. Factory trimming eliminates the need for calibration modes or external trimming to achieve rated performance.
4. RELIABILITY: The AD678 utilizes Analog Devices' monolithic BiMOS technology. This ensures long term reliability compared to multichip and hybrid designs.
5. UPGRADE PATH: The AD678 provides the same pinout as the 14-bit, 128 kSPS AD679 ADC.

AD678—SPECIFICATIONS

AC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%, f_{SAMPLE} = 200 kSPS, f_{IN} = 10.06 kHz unless otherwise noted)[1]

Parameter	AD678J/A/S Min	AD678J/A/S Typ	AD678J/A/S Max	AD678K/B/T Min	AD678K/B/T Typ	AD678K/B/T Max	Units
SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO[2]							
−0.5 dB Input (Referred to −0 dB Input)	70	71		72	73		dB
−20 dB Input (Referred to −20 dB Input)		51			53		dB
−60 dB Input (Referred to −60 dB Input)		11			13		dB
TOTAL HARMONIC DISTORTION (THD)[3]		−88	**−80**		−88	**−80**	dB
		0.004	0.010		0.004	0.010	%
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−87	**−80**		−87	**−80**	dB
FULL POWER BANDWIDTH		1			1		MHz
FULL LINEAR BANDWIDTH	500			500			kHz
INTERMODULATION DISTORTION (IMD)[4]							
2nd Order Products		−85	**−80**		−85	**−80**	dB
3rd Order Products		−90	**−80**		−90	**−80**	dB

NOTE
[1]f_{IN} amplitude = −0.5 dB (9.44 V p-p) bipolar mode full scale unless otherwise indicated. All measurements referred to a −0 dB (9.997 V p-p) input signal unless otherwise indicated.
[2]See Figures 13 and 14 for higher frequencies and other input amplitudes.
[3]See Figure 12.
[4]f_A = 9.08 kHz, f_B = 9.58 kHz, with f_{SAMPLE} = 200 KSPS. See Definition of Specifications section and Figure 16.
Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (All device types T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter		Test Conditions	Min	Max	Units
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		**2.0**	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	**0.8**	V
I_{IH}	High Level Input Current	V_{IN} = V_{DD}	**−10**	**+10**	μA
I_{IL}	Low Level Input Current	V_{IN} = 0 V	**−10**	**+10**	μA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	4.0		V
		I_{OH} = 0.5 mA	**2.4**		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		**0.4**	V
I_{OZ}	High Z Leakage Current	V_{IN} = 0 or V_{DD}	**−10**	**+10**	μA
C_{OZ}	High Z Output Capacitance			10	pF

NOTES
Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at T_{min}, +25°C and T_{max}. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.
Specifications subject to change without notice.

Parameter	AD678J/A/S Min	Typ	Max	AD678K/B/T Min	Typ	Max	Units
TEMPERATURE RANGE							
J, K Grades	0		+70	0		+70	°C
A, B Grades	−40		+85	−40		+85	°C
S, T Grades	−55		+125	−55		+125	°C
ACCURACY							
Resolution	**12**			**12**			Bits
Integral Nonlinearity (INL)		±1			±0.7	**±1**	LSB
Differential Nonlinearity (DNL)	**12**			**12**			Bits
Unipolar Zero Error (@ +25°C)[1]		±4			±2	**±3**	LSB
Bipolar Zero Error (@ +25°C)[1]		±4			±3	**±5**	LSB
Gain Error (@ +25°C)[1, 2]		±4			±3	**±6**	LSB
Temperature Drift							
Unipolar/Bipolar Zero							
J, K Grades		±2			±2	**±4**	LSB
A, B Grades		±4			±3	**±4**	LSB
S, T Grades		±5			±4	**±5**	LSB
Gain[3]							
J, K Grades		±4			±4	**±6**	LSB
A, B Grades		±7			±5	**±7**	LSB
S, T Grades		±10			±8	**±10**	LSB
Gain[4]							
J, K Grades		±2			±2	**±4**	LSB
A, B Grades		±4			±3	**±4**	LSB
S, T Grades		±6			±5	**±6**	LSB
ANALOG INPUT							
Input Ranges							
Unipolar Range	**0**		**+10**	**0**		**+10**	V
Bipolar Range	**−5**		**+5**	**−5**		**+5**	V
Input Resistance		10			10		MΩ
Input Capacitance		10			10		pF
Input Settling Time			1			1	μs
Aperture Delay		10			10		ns
Aperture Jitter		150			150		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage[5]	**4.98**		**5.02**	**4.98**		**5.02**	V
External Load							
Unipolar Mode			**+1.5**			**+1.5**	mA
Bipolar Mode			**+0.5**			**+0.5**	mA
POWER SUPPLIES							
Power Supply Rejection							
V_{CC} = +12 V ± 5%		±2				**±2**	LSB
V_{EE} = −12 V ± 5%		±2				**±2**	LSB
V_{DD} = +5 V ± 10%		±2				**±2**	LSB
Operating Current							
I_{CC}		18	**20**		18	**20**	mA
I_{EE}		25	**34**		25	**34**	mA
I_{DD}		8	**12**		8	**12**	mA
Power Consumption		560	**745**		560	**745**	mW

NOTES
[1]Adjustable to zero. See Figures 6 and 7.
[2]Includes internal voltage reference error.
[3]Includes internal voltage reference drift.
[4]Excludes internal voltage reference drift.
[5]With maximum external load applied.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at T_{min}, +25°C and T_{max}. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

TIMING SPECIFICATIONS

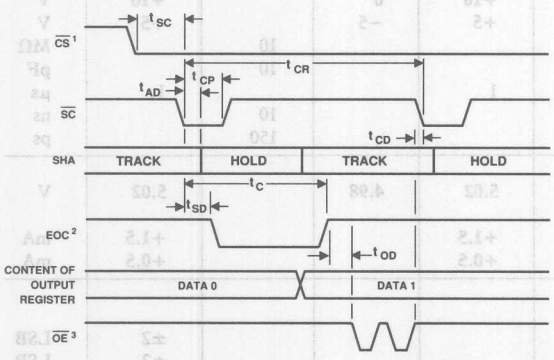
(All grades, T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10% unless otherwise noted)

Parameter	Symbol	Min	Max	Units
$\overline{SC}$ Delay	t_{SC}	**50**		ns
Conversion Time	t_C	3.0	4.4	µs
Conversion Rate[1]	t_{CR}		5	µs
Convert Pulse Width	t_{CP}	**97**		ns
Aperture Delay	t_{AD}	5	20	ns
Status Delay	t_{SD}	**0**	**400**	ns
Access Time[2, 3]	t_{BA}	10	**100**	ns
		10	57[4]	ns
Float Delay[5]	t_{FD}	**10**	**80**	ns
Output Delay	t_{OD}		**0**	ns
Format Setup[6]	t_{FS}	**47**		ns
$\overline{OE}$ Delay[6]	t_{OE}	**0**		ns
Read Pulse Width[6]	t_{RP}	**97**		ns
Conversion Delay	t_{CD}	**150**		ns
$\overline{EOCEN}$ Delay	t_{EO}	**0**		ns

NOTES
[1]Includes acquisition time.
[2]Measured from the falling edge of $\overline{OE}/\overline{EOCEN}$ (0.8 V) to the time at which the data lines/EOC cross 2.0 V or 0.8 V. See Figure 3.
[3]C_{OUT} = 100 pF.
[4]C_{OUT} = 50 pF.
[5]Measured from the rising edge of $\overline{OE}/\overline{EOCEN}$ (2.0 V) to the time at which the output voltage changes by 0.5 V. See Figure 3; C_{OUT} = 10 pF.
[6]See Figures 4 and 5.

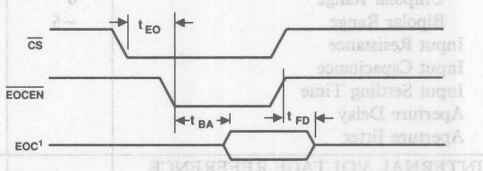
Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at T_{min}, +25°C and T_{max}. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.



NOTES
[1] IN ASYNCHRONOUS MODE, STATE OF $\overline{CS}$ DOES NOT AFFECT OPERATION. SEE THE START CONVERSION TRUTH TABLE FOR DETAILS.
[2] $\overline{EOCEN}$ = LOW; SEE FIGURE 2. IN SYNCHRONOUS MODE, EOC IS A THREE-STATE OUTPUT. IN ASYNCHRONOUS MODE, EOC IS AN OPEN DRAIN OUTPUT.
[3] DATA SHOULD NOT BE ENABLED DURING A CONVERSION.

Figure 1. Conversion Timing



NOTE
[1]SEE END-OF-CONVERT (EOC) PARAGRAPH FOR DETAILS.

Figure 2. EOC Timing

TEST	V_{CP}	C_{OUT}
ACCESS TIME HIGH Z TO LOGIC LOW	5 V	100 pF
FLOAT TIME LOGIC HIGH TO HIGH Z	0 V	10 pF
ACCESS TIME HIGH Z TO LOGIC HIGH	0 V	100 pF
FLOAT TIME LOGIC LOW TO HIGH Z	5 V	10 pF

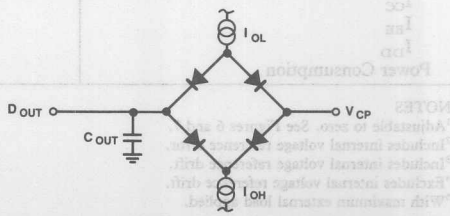


Figure 3. Load Circuit for Bus Timing Specifications

ABSOLUTE MAXIMUM RATINGS*

Specification	With Respect To	Min	Max	Units
V_{CC}	AGND	−0.3	+18	V
V_{EE}	AGND	−18	+0.3	V
V_{CC}	V_{EE}	−0.3	+26.4	V
V_{DD}	DGND	0	+7	V
AGND	DGND	−1	+1	V
AIN, REF_{IN}	AGND	V_{EE}	V_{CC}	V
Digital Inputs	DGND	−0.5	+7	V
Digital Outputs	DGND	−0.5	V_{DD} +0.3	V
Max Junction Temperature			175	°C

Specification	With Respect To	Min	Max	Units
Operating Temperature				
J and K Grades		0	+70	°C
A and B Grades		−40	+85	°C
S and T Grades		−55	+125	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec max)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

ESD SENSITIVITY

The AD678 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD678 has been classified as a Category 1 device.

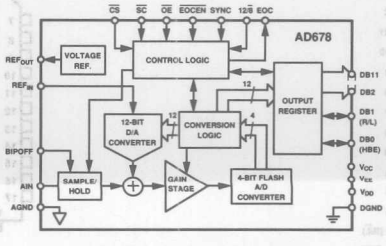


Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.

ORDERING GUIDE

Model[1]	Package	Temperature Range	Tested and Specified	Package Option[2]
AD678JN	28-Pin Plastic DIP	0°C to +70°C	AC	N-28A
AD678KN	28-Pin Plastic DIP	0°C to +70°C	AC + DC	N-28A
AD678JD	28-Pin Ceramic DIP	0°C to +70°C	AC	D-28A
AD678KD	28-Pin Ceramic DIP	0°C to +70°C	AC + DC	D-28A
AD678AD	28-Pin Ceramic DIP	−40°C to +85°C	AC	D-28A
AD678BD	28-Pin Ceramic DIP	−40°C to +85°C	AC + DC	D-28A
AD678AJ	44-Lead Ceramic JLCC	−40°C to +85°C	AC	J-44
AD678BJ	44-Lead Ceramic JLCC	−40°C to +85°C	AC + DC	J-44
AD678SJ	44-Lead Ceramic JLCC	−55°C to +125°C	AC	J-44
AD678TJ	44-Lead Ceramic JLCC	−55°C to +125°C	AC + DC	J-44
AD678SD	28-Pin Ceramic DIP	−55°C to +125°C	AC	D-28A
AD678TD	28-Pin Ceramic DIP	−55°C to +125°C	AC + DC	D-28A

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to Analog Devices Military Products Databook or /883 data sheet.
[2]N = Plastic DIP; D = Ceramic DIP; J = J-Leaded Ceramic Chip Carrier. For outline information see Package Information section.



Functional Block Diagram

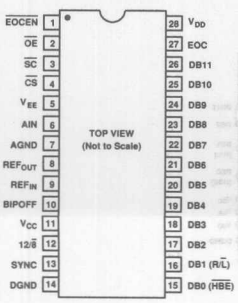
PIN DESCRIPTION

Symbol	28-Pin DIP Pin No.	44-Lead JLCC Pin No.	Type	Name and Function
AGND	7	11	P	Analog Ground. This is the ground return for AIN only.
AIN	6	10	AI	Analog Signal Input.
BIPOFF	10	15	AI	Bipolar Offset. Connect to AGND for +10 V input unipolar mode and straight binary output coding. Connect to REF_{OUT} through 50 Ω resistor for ±5 V input bipolar mode and twos complement binary output coding. See Figures 7 and 8.
$\overline{CS}$	4	6	DI	Chip Select. Active LOW.
DGND	14	23	P	Digital Ground
DB11–DB4	26–19	40, 39, 37, 36 35, 34, 33, 31	DO	Data Bits 11 through 4. In 12-bit format (see 12/$\overline{8}$ pin), these pins provide the upper 8 bits of data. In 8-bit format, these pins provide all 12 bits in two bytes (see R/$\overline{L}$ pin). Active HIGH.
DB3, DB2	18, 17	30, 27	DO	Data Bits 3 and 2. In 12-bit format, these pins provide Data Bit 3 and Data Bit 2. Active HIGH. In 8-bit format they are undefined and should be tied to V_{DD}.
DB1 (R/$\overline{L}$)	16	26	DO	In 12-bit format, Data Bit 1. Active HIGH.
DB0 ($\overline{HBE}$)	15	25	DO	In 12-bit format, Data Bit 0. Active HIGH.
EOC	27	42	DO	End-of-Convert. EOC goes LOW when a conversion starts and goes HIGH when the conversion is finished. In asynchronous mode, EOC is an open drain output and requires an external 3 kΩ pull-up resistor. See $\overline{EOCEN}$ and SYNC pins for information on EOC gating.
$\overline{EOCEN}$	1	1	DI	End-Of-Convert Enable. Enables EOC pin. Active LOW.
$\overline{HBE}$ (DB0)	15	25	DI	In 8-bit format, High Byte Enable. If LOW, output contains high byte. If HIGH, output contains low byte.
$\overline{OE}$	2	3	DI	Output Enable. The falling edge of $\overline{OE}$ enables DB11–DB0 in 12-bit format and DB11–DB4 in 8-bit format. Gated with $\overline{CS}$. Active LOW.
REF_{IN}	9	14	AI	Reference Input. +5 V input gives 10 V full scale range.
REF_{OUT}	8	12	AO	+5 V Reference Output. Tied to REF_{IN} through 50 Ω resistor for normal operation.
R/$\overline{L}$ (DB1)	16	26	DI	In 8-bit format, Right/Left justified. Sets alignment of 12-bit result within 16-bit field. Tied to V_{DD} for right-justified output and tied to DGND for left-justified output.
$\overline{SC}$	3	5	DI	Start Convert. Active LOW. See SYNC pin for gating.
SYNC	13	21	DI	SYNC Control. If tied to V_{DD} (synchronous mode), $\overline{SC}$, EOC and $\overline{EOCEN}$ are gated by $\overline{CS}$. If tied to DGND (asynchronous mode), $\overline{SC}$ and $\overline{EOCEN}$ are independent of $\overline{CS}$, and EOC is an open drain output. EOC requires an external 3 kΩ pull-up resistor in asynchronous mode.
V_{CC}	11	17	P	+12 V Analog Power.
V_{EE}	5	8	P	−12 V Analog Power.
V_{DD}	28	43	P	+5 V Digital Power.
12/$\overline{8}$	12	19	DI	Twelve/eight bit format. If tied HIGH, sets output format to 12-bit parallel. If tied LOW, sets output format to 8-bit multiplexed.
No Connect	—	2, 4, 7, 9, 13, 16, 18, 20, 22, 24, 28, 29, 32, 38, 41, 44	—	These pins are unused and should be connected to DGND or V_{DD}.

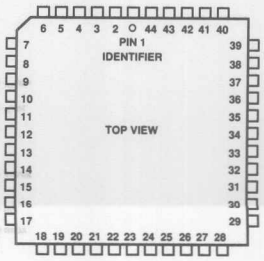
Type: AI = Analog Input; AO = Analog Output; DI = Digital Input (TTL and 5 V CMOS compatible); DO = Digital Output (TTL and 5 V CMOS compatible). All DO pins are three-state drivers; P = Power.

PIN CONFIGURATIONS

DIP PACKAGE



JLCC PACKAGE



NYQUIST FREQUENCY
An implication of the Nyquist sampling theorem, the "Nyquist Frequency" of a converter is that input frequency which is one-half the sampling frequency of the converter.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

TOTAL HARMONIC DISTORTION (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of a full-scale input signal and is expressed as a percentage or in decibels. For input signals or harmonics that are above the Nyquist frequency, the aliased component is used.

PEAK SPURIOUS OR PEAK HARMONIC COMPONENT
The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in decibels relative to the rms value of a full-scale input signal.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb) and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (fa − 2 fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude and the peak value of their sum is −0.5 dB from full scale (9.44 V p-p). The IMD products are normalized to a 0 dB input signal.

BANDWIDTH
The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

The full-linear bandwidth is the input frequency at which the slew rate limit of the sample-hold-amplifier (SHA) is reached. At this point, the amplitude of the reconstructed fundamental has degraded by less than −0.1 dB. Beyond this frequency, distortion of the sampled input signal increases significantly.

The AD678 has been designed to optimize input bandwidth, allowing the AD678 to undersample input signals with frequencies significantly above the converter's Nyquist frequency.

APERTURE DELAY
Aperture delay is a measure of the SHA's performance and is measured from the falling edge of Start Convert ($\overline{SC}$) to when the input signal is held for conversion. In synchronous mode, Chip Select ($\overline{CS}$) should be LOW before $\overline{SC}$ to minimize aperture delay.

APERTURE JITTER
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

INPUT SETTLING TIME
Settling time is a function of the SHA's ability to track fast slewing signals. This is specified as the maximum time required in track mode after a full-scale step input to guarantee rated conversion accuracy.

DIFFERENTIAL NONLINEARITY (DNL)
In an ideal ADC, code transitions are 1LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes (NMC) are guaranteed.

UNIPOLAR ZERO ERROR
In unipolar mode, the first transition should occur at a level 1/2 LSB above analog ground. Unipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

BIPOLAR ZERO ERROR
In the bipolar mode, the major carry transition (1111 1111 1111 to 0000 0000 0000) should occur at an analog value 1/2 LSB below analog ground. Bipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

GAIN ERROR
The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale (9.9963 volts for a 0–10 V range, 4.9963 volts for a ±5 V range). The gain error is the deviation of the actual difference between the first and last code transition from the ideal difference between the first and last code transition. This error can be adjusted as shown in the Input Connections and Calibration section.

INTEGRAL NONLINEARITY (INL)
The ideal transfer function for a linear ADC is a straight line drawn between "zero" and "full scale." The point used as "zero" occurs 1/2LSB before the first code transition. "Full scale" is defined as a level 1 1/2LSB beyond the last code transition. Integral nonlinearity is the worst-case deviation of a code from the straight line. The deviation of each code is measured from the middle of that code.

POWER SUPPLY REJECTION
Variations in power supply will affect the full-scale transition, but not the converter's linearity. Power Supply Rejection is the maximum change in the full-scale transition point due to a change in power-supply voltage from the nominal value.

TEMPERATURE DRIFT
This is the maximum change in the parameter from the initial value (@ 25°C) to the value at T_{min} or T_{max}.

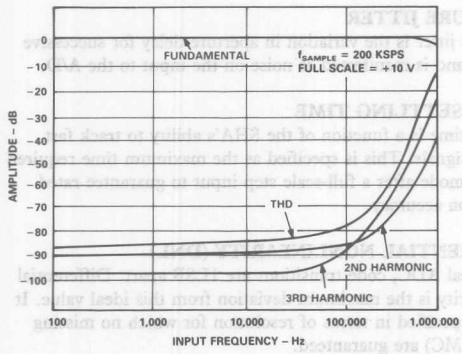


Figure 4. Harmonic Distortion vs. Input Frequency

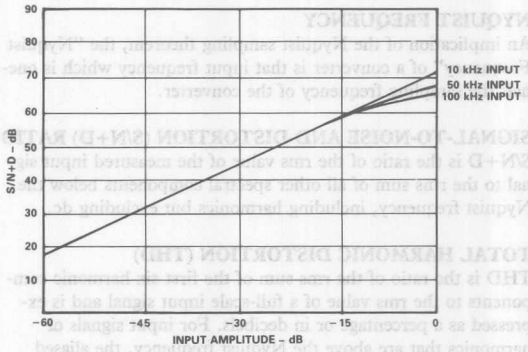


Figure 5. S/N&D vs. Input Amplitude (f_{SAMPLE} = 200 kSPS)

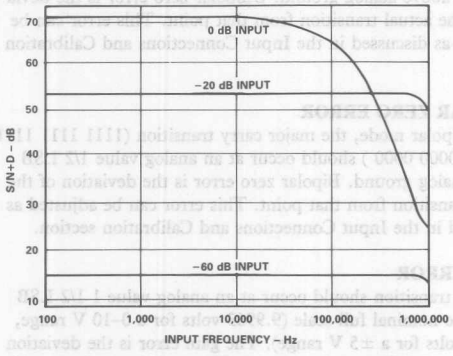


Figure 6. S/N&D vs. Input Frequency and Amplitude

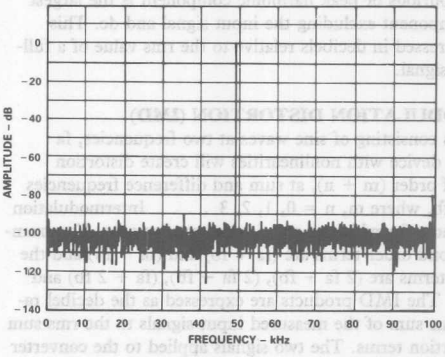


Figure 7. Nonaveraged 2048 Point FFT at 200 kSPS, f_{IN} = 49.902 kHz

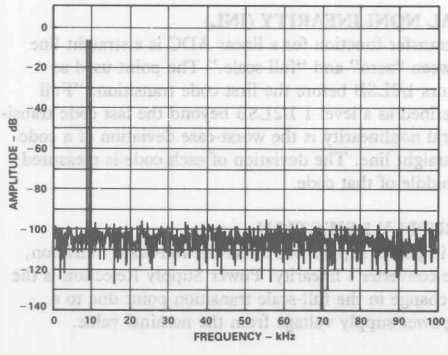


Figure 8. IMD Plot for f_{IN} = 9.08 kHz (fa), 9.58 kHz (fb)

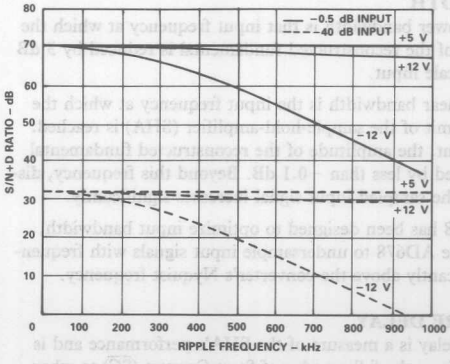


Figure 9. Power Supply Rejection (f_{IN} = 10 kHz, f_{SAMPLE} = 200 kSPS, V_{RIPPLE} = 0.1 V p-p)

CONVERSION CONTROL

In synchronous mode (SYNC = HIGH), both Chip Select ($\overline{CS}$) and Start Convert ($\overline{SC}$) must be brought LOW to start a conversion. $\overline{CS}$ should be LOW t_{SC} before $\overline{SC}$ is brought LOW. In asynchronous mode (SYNC = LOW), a conversion is started by bringing $\overline{SC}$ low, regardless of the state of $\overline{CS}$.

Before a conversion is started, End-of-Convert (EOC) is HIGH, and the sample-hold is in track mode. After a conversion is started, the sample-hold goes into hold mode and EOC goes LOW, signifying that a conversion is in progress. During the conversion, the sample-hold will go back into track mode and start acquiring the next sample. EOC goes HIGH when the conversion is finished.

In track mode, the sample-hold will settle to ±0.01% (12 bits) in 1 µs maximum. The acquisition time does not affect the throughput rate as the AD678 goes back into track mode more than 1 µs before the next conversion. In multichannel systems, the input channel can be switched as soon as EOC goes LOW if the maximum throughput rate is needed.

12-BIT MODE CODING FORMAT (1 LSB = 2.44 mV)

Unipolar Coding (Straight Binary)		Bipolar Coding (Twos Complement)	
V_{IN}*	Output Code	V_{IN}*	Output Code
0 V	000 . . . 0	−5.000 V	100 . . . 0
5.000 V	100 . . . 0	−0.002 V	111 . . . 1
9.9976 V	111 . . . 1	0.000 V	000 . . . 0
		+2.500 V	010 . . . 0
		+4.9976 V	011 . . . 1

*Code center.

OUTPUT ENABLE TRUTH TABLES

12-BIT MODE (12/$\overline{8}$ = HIGH)

INPUTS ($\overline{CS}$ U $\overline{OE}$)	OUTPUT DB11–DB0
1	High Z
0	Enable 12-Bit Output

8-BIT MODE (12/$\overline{8}$ = LOW)

	INPUTS			OUTPUTS							
	R/$\overline{L}$	HBE	($\overline{CS}$ U $\overline{OE}$)	DB11 . . . DB4							
	X	X	1	High Z							
	1	0	0	0	0	0	0	a	b	c	d
Unipolar	1	1	0	e	f	g	h	i	j	k	l
Mode	0	0	0	a	b	c	d	e	f	g	h
	0	1	0	i	j	k	l	0	0	0	0
	1	0	0	a	a	a	a	a	b	c	d
Bipolar	1	1	0	e	f	g	h	i	j	k	l
Mode	0	0	0	a	b	c	d	e	f	g	h
	0	1	0	i	j	k	l	0	0	0	0

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
U = Logical OR.
a = MSB.
1 = LSB.

END-OF-CONVERT

In asynchronous mode, End-of-Convert (EOC) is an open drain output (requiring a minimum 3 kΩ pull-up resistor) enabled by End-of-Convert ENable ($\overline{EOCEN}$). In synchronous mode, EOC is a three-state output which is enabled by $\overline{EOCEN}$ and $\overline{CS}$. See the Conversion Status Truth Table for details. Access (t_{BA}) and float (t_{FD}) timing specifications do not apply in asynchronous mode where they are a function of the time constant formed by the 10 pF output capacitance and the pull-up resistor.

START CONVERSION TRUTH TABLE

	INPUTS			
	SYNC	$\overline{CS}$	$\overline{SC}$	STATUS
Synchronous Mode	1	1	X	No Conversion
	1	0		Start Conversion
	1		0	Start Conversion (Not Recommended)
	1	0	0	Continuous Conversion (Not Recommended)
Asynchronous Mode	0	X	1	No Conversion
	0	X		Start Conversion
	0	X	0	Continuous Conversion (Not Recommended)

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
= HIGH to LOW transition. Must stay low for t = t_{CP}.

CONVERSION STATUS TRUTH TABLE

	INPUTS			OUTPUT	
	SYNC	$\overline{CS}$	$\overline{EOCEN}$	EOC	STATUS
Synchronous Mode	1	0	0	0	Converting
	1	0	0	1	Not Converting
	1	1	X	High Z	Either
	1	X	1	High Z	Either
Asynchronous Mode*	0	X	0	0	Converting
	0	X	0	High Z	Not Converting
	0	X	1	High Z	Either

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
*EOC requires a pull-up resistor in asynchronous mode.

OUTPUT ENABLE OPERATION

The data bits (DB11–DB0) are three-state outputs enabled by Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$). $\overline{CS}$ should be LOW t_{OE} before $\overline{OE}$ is brought LOW. Bits DB1 (R/$\overline{L}$) and DB0 ($\overline{HBE}$) are bidirectional. In 12-bit mode they are data output bits. In 8-bit mode they are inputs which define the format of the output register.

In unipolar mode (BIPOFF tied to AGND), the output coding is straight binary. In bipolar mode (BIPOFF tied to REF_{OUT}), output coding is twos complement binary.

When EOC goes HIGH, the conversion is completed and the output data may be read. Bringing $\overline{OE}$ LOW t_{OE} after $\overline{CS}$ is brought LOW makes the output register contents available on the data bits. A period of time t_{CD} is required after $\overline{OE}$ is brought HIGH before the next $\overline{SC}$ instruction may be issued.

Figure 10 illustrates the 8-bit read mode (12/$\overline{8}$ = LOW), where only DB11–DB4 are used as output lines onto an 8-bit bus. The output is read in two steps, with the high byte read first, followed by the low byte. High Byte Enable ($\overline{HBE}$) controls the output sequence. The 12-bit result can be right or left justified depending on the state of R/$\overline{L}$.

In 12-bit read mode (12/$\overline{8}$ = HIGH), a single READ operation accesses all 12 output bits on DB11–DB0 for interface to a 16-bit bus. Figure 11 provides the output timing relationships. Note that t_{CR} must be observed, in that $\overline{SC}$ pulses should not be issued at intervals closer than 5 μs. If $\overline{SC}$ is asserted sooner than 5 μs, conversion accuracy may deteriorate. For this reason, $\overline{SC}$ should not be held LOW in an attempt to operate in a continuously converting mode.

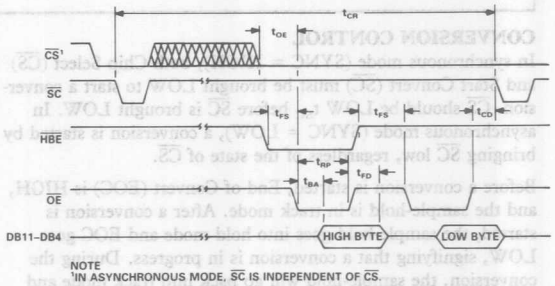


Figure 10. Output Timing, 8-Bit Read Mode

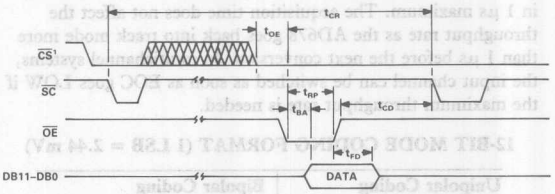


Figure 11. Output Timing, 12-Bit Read Mode

POWER-UP

The AD678 typically requires 10 μs after power-up to reset internal logic.

Application Information

INPUT CONNECTIONS AND CALIBRATION

The high (10 MΩ) input impedance of the AD678 eases the task of interfacing to high source impedances or multiplexer channel-to-channel mismatches of up to 1000 Ω. The 10 V p-p full-scale input range accepts the majority of signal voltages without the need for voltage divider networks which could deteriorate the accuracy of the ADC.

The AD678 is factory trimmed to minimize linearity, offset and gain errors. In unipolar mode, the only external component that is required is a 50 Ω ±1% resistor. Two resistors are required in bipolar mode. If offset and gain are not critical (as in some ac applications), even these components can be eliminated.

In some applications, offset and gain errors need to be trimmed out completely. The following sections describe the correct procedure for these various situations.

UNIPOLAR RANGE INPUTS

Offset and gain errors can be trimmed out by using the configuration shown in Figure 12. This circuit allows approximately ±25 mV of offset trim range (±10 LSB) and ±0.5% of gain trim (±20 LSB).

The first transition (from 0000 0000 0000 to 0000 0000 0001) should nominally occur for an input level of +1/2 LSB (1.22 mV above ground for a 10 V range). To trim unipolar zero to this nominal value, apply a 1.22 mV signal to AIN and adjust R1 until the first transition is located.

The gain trim is done by adjusting R2. If the nominal value is required, apply a signal 1 1/2 LSB below full scale (9.9963 V for a 10 V range) and adjust R2 until the last transition is located (1111 1111 1110 to 1111 1111 1111).

If offset adjustment is not required, BIPOFF should be connected directly to AGND. If gain adjustment is not required, R2 should be replaced with a fixed 50 Ω ±1% metal film resistor. If REF_{OUT} is connected directly to REF_{IN}, the additional gain error will be approximately 1%.

BIPOLAR RANGE INPUTS

The connections for the bipolar mode are shown in Figure 13. In this mode, data output coding will be in twos-complement binary. This circuit will allow approximately ±25 mV of offset trim range (±10 LSB) and ±0.5% of gain trim range (20 LSB).

Either or both of the trim pots can be replaced with 50 Ω ± 1% fixed resistors if the AD678 accuracy limits are sufficient for the application. If the pins are shorted together, the additional offset and gain errors will be approximately 1%.

To trim bipolar zero to its nominal value, apply a signal 1/2 LSB below midrange (−1.22 mV for a ±5 V range) and adjust R1 until the major carry transition is located (1111 1111 1111 to 0000 0000 0000). To trim the gain, apply a signal 1 1/2 LSB below full scale (+4.9963 V for a ±5 V range) and adjust R2 to give the last positive transition (0111 1111 1110 to 0111 1111 1111). These trims are interactive so several iterations may be necessary for convergence.

A single-pass calibration can be done by substituting a bipolar offset trim (error at minus full scale) for the bipolar zero trim (error at midscale), using the same circuit. First, apply a signal 1/2 LSB above minus full scale (−4.9988 V for a ±5 V range) and adjust R1 until the minus full-scale transition is located (1000 0000 0000 to 1000 0000 001). Then perform the gain error trim as outlined above.

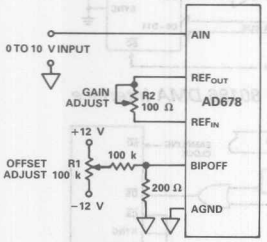


Figure 12. Unipolar Input Connections with Gain and Offset Trims

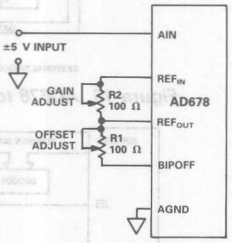


Figure 13. Bipolar Input Connections with Gain and Offset Trims

BOARD LAYOUT

Designing with high-resolution data converters requires careful attention to layout. Trace impedance is a significant issue. At the 12-bit level, a 5 mA current through a 0.5 Ω trace will develop a voltage drop of 2.5 mV, which is 1 LSB for a 10 V full-scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high-accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter out ac noise.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

The AD678 incorporates several features to help the user's layout. Analog pins (V_{EE}, AIN, AGND, REF_{OUT}, REF_{IN}, BIPOFF, V_{CC}) are adjacent to help isolate analog from digital signals. In addition, the 10 MΩ input impedance of AIN minimizes input trace impedance errors. Finally, ground currents have been minimized by careful circuit design. Current through AGND is 200 μA, with no code-dependent variation. The current through DGND is dominated by the return current for DB11–DB0 and EOC.

SUPPLY DECOUPLING

The AD678 power supplies should be well filtered, well regulated, and free from high-frequency noise. Switching power supplies are not recommended. These supplies generate spikes which can induce noise in the analog system.

Decoupling capacitors should be located as close as possible to all power supply pins. A 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic provides adequate decoupling. The power supply pins should be decoupled directly to AGND.

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD678, associated analog input circuitry and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD678 will isolate large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

GROUNDING

If a single AD678 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD678. If multiple AD678s are used or the AD678 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at each chip. This prevents large ground loops which inductively couple noise and allow digital currents to flow through the analog system.

INTERFACING THE AD678 TO MICROPROCESSORS

The I/O capabilities of the AD678 allow direct interfacing to general purpose and DSP microprocessor buses. The asynchronous conversion control feature allows complete flexibility and control with minimal external hardware.

The following examples illustrate typical AD678 interface configurations.

space. AD678 conversions are initiated by issuing an OUT instruction to Port 8. EOC status and the conversion result are read in with an IN instruction to Port 8. A single wait state is inserted by generating the processor READY input from $\overline{IS}$, Port 8 and $\overline{MSC}$. This configuration supports processor clock speeds of 20 MHz and is capable of supporting processor clock speeds of 40 MHz if a NOP instruction follows each AD678 read instruction.

AD678 TO 80186

Figure 15 shows the AD678 interfaced to the 80186 microprocessor. This interface allows the 80186's built-in DMA controller to transfer the AD678 output into a RAM based FIFO buffer of any length, with no microprocessor intervention.

In this application the AD678 is configured in the asynchronous mode, which allows conversions to be initiated by an external trigger source independent of the microprocessor clock. After each conversion, the AD678 EOC signal generates a DMA request to Channel 1 (DRQ1). The subsequent DMA READ operation resets the interrupt latch. The system designer must assign a sufficient priority to the DMA channel to ensure that the DMA request will be serviced before the completion of the next conversion. This configuration can be used with 6-MHz and 8-MHz 80186 processors.

AD678 TO ANALOG DEVICES ADSP-2101

Figure 16 demonstrates the AD678 interfaced to an ADSP-2101. With a clock frequency of 12.5 MHz, and instruction execution in one 80 ns cycle, the digital signal processor supports the AD678 interface with one wait state.

The converter is configured to run asynchronously using a sampling clock. The EOC output of the AD678 gets asserted at the end of each conversion and causes an interrupt. Upon interrupt, the ADSP-2101 immediately asserts its FO pin LOW. In the following cycle, the processor starts a data memory read by providing an address on the DMA bus. The decoded address generates $\overline{OE}$ for the converter, and the high byte of the conversion result is read over the data bus. The read operation is extended with one wait state and thus started and completed within two processor cycles (160 ns). Next, the ADSP-2101 asserts its FO pin HIGH. This allows the processor to start reading the lower byte of data. This read operation executes in a similar manner to the first and is completed during the next 160 ns.

AD678 TO ANALOG DEVICES ADSP-2100A

Figure 17 demonstrates the AD678 interfaced to an ADSP-2100A. With a clock frequency of 12.5 MHz, and instruction execution in one 80 ns cycle, the digital signal processor will support the AD678 data memory interface with three hardware wait states.

The converter is configured to run asynchronously using a sampling clock. The EOC output of the AD678 gets asserted at the end of each conversion and causes an interrupt. Upon interrupt, the ADSP-2100A immediately executes a data memory write instruction which asserts $\overline{HBE}$. In the following cycle, the processor starts a data memory read (high byte read) by providing an address on the DMA bus. The decoded address generates $\overline{OE}$ for the converter. $\overline{OE}$, together with logic and latch, is used to force the ADSP-2100A into a one cycle wait state by generating DMACK. The read operation is thus started and completed within two processor cycles (160 ns). $\overline{HBE}$ is released during "high byte read." This allows the processor to read the lower

is completed during the next 160 ns.

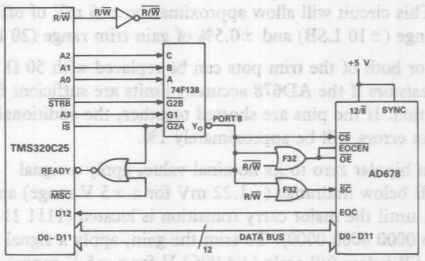


Figure 14. AD678 to TMS320C25 Interface

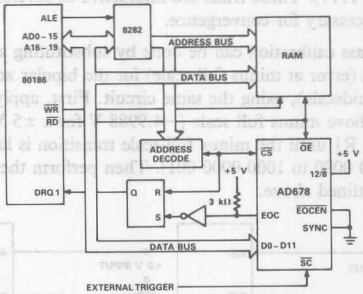


Figure 15. AD678 to 80186 DMA Interface

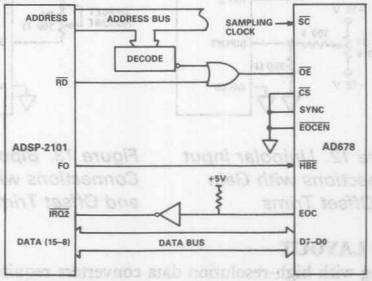


Figure 16. AD678 to ADSP-2101 Interface

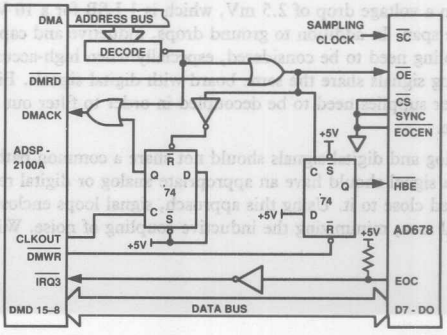


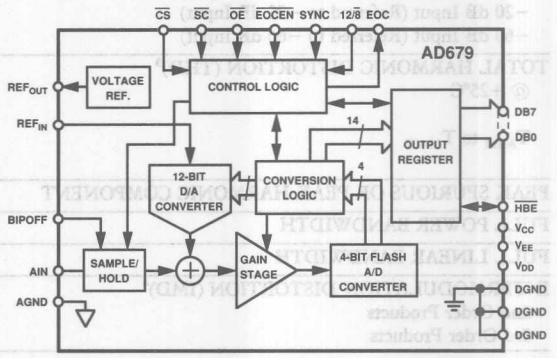
Figure 17. AD678 to ADSP-2100A Interface

AD679*

FEATURES

- AC and DC Characterized and Specified (K, B, T Grades)
- 128k Conversions per Second
- 1 MHz Full Power Bandwidth
- 500 kHz Full Linear Bandwidth
- 80 dB S/N+D (K, B, T Grades)
- Twos Complement Data Format (Bipolar Mode)
- Straight Binary Data Format (Unipolar Mode)
- 10 MΩ Input Impedance
- 8-Bit Bus Interface (See AD779 for 16-Bit Interface)
- On-Board Reference and Clock
- 10 V Unipolar or Bipolar Input Range
- Pin Compatible with AD678 12-Bit, 200 kSPS ADC
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD679 is a complete, multipurpose 14-bit monolithic analog-to-digital converter, consisting of a sample-hold amplifier (SHA), a microprocessor compatible bus interface, a voltage reference and clock generation circuitry.

The AD679 is specified for ac (or "dynamic") parameters such as S/N+D ratio, THD and IMD which are important in signal processing applications. In addition, the AD679K, B and T grades are fully specified for dc parameters which are important in measurement applications.

The 14 data bits are accessed in two read operations (8+6), with left justification. Data format is straight binary for unipolar mode and twos complement binary for bipolar mode. The input has a full-scale range of 10 V with a full power bandwidth of 1 MHz and a full linear bandwidth of 500 kHz. High input impedance (10 MΩ) allows direct connection to unbuffered sources without signal degradation. Conversions can be initiated either under microprocessor control or by an external clock asynchronous to the system clock.

This product is fabricated on Analog Devices' BiMOS process, combining low power CMOS logic with high precision, low noise bipolar circuits; laser-trimmed thin-film resistors provide high accuracy. The converter utilizes a recursive subranging algorithm which includes error correction and flash converter circuitry to achieve high speed and resolution.

The AD679 operates from +5 V and ±12 V supplies and dissipates 560 mW (typ.). 28-pin plastic DIP, ceramic DIP and 44 J-leaded ceramic surface mount packages are available.

***Protected by U.S. Patent Nos. 4,804,960; 4,814,767; 4,833,345; 4,250,445; 4,808,908; RE 30,586**

PRODUCT HIGHLIGHTS

1. COMPLETE INTEGRATION: The AD679 minimizes external component requirements by combining a high speed sample-hold amplifier (SHA), ADC, 5 V reference, clock and digital interface on a single chip. This provides a fully specified sampling A/D function unattainable with discrete designs.
2. SPECIFICATIONS: The AD679K, B and T grades provide fully specified and tested ac and dc parameters. The AD679J, A and S grades are specified and tested for ac parameters; dc accuracy specifications are shown as typicals. DC specifications (such as INL, gain and offset) are important in control and measurement applications. AC specifications (such as S/N+D ratio, THD and IMD) are of value in signal processing applications.
3. EASE OF USE: The pinout is designed for easy board layout, and the two read output provides compatibility with 8-bit buses. Factory trimming eliminates the need for calibration modes or external trimming to achieve rated performance.
4. RELIABILITY: The AD679 utilizes Analog Devices' monolithic BiMOS technology. This ensures long term reliability compared to multichip and hybrid designs.
5. UPGRADE PATH: The AD679 provides the same pinout as the 12-bit, 200 kSPS AD678 ADC.
6. The AD679 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD679/883B data sheet for detailed specifications.

AD679—SPECIFICATIONS

AC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%, f_{SAMPLE} = 128 kSPS, f_{IN} = 10.009 kHz unless otherwise noted)[1]

Parameter	AD679J/A/S Min	AD679J/A/S Typ	AD679J/A/S Max	AD679K/B/T Min	AD679K/B/T Typ	AD679K/B/T Max	Units
SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO[2]							
−0.5 dB Input (Referred to −0 dB Input)	78	79		80	81		dB
−20 dB Input (Referred to −20 dB Input)	58	59		60	61		dB
−60 dB Input (Referred to −60 dB Input)	18	19		20	21		dB
TOTAL HARMONIC DISTORTION (THD)[3]							
@ +25°C		−90	**−84**		−90	**−84**	dB
		0.003	**0.006**		0.003	**0.006**	%
T_{MIN} to T_{MAX}		−88	**−82**		−88	**−82**	dB
		0.004	**0.008**		0.004	**0.008**	%
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−90	**−84**		−90	**−84**	dB
FULL POWER BANDWIDTH		1			1		MHz
FULL LINEAR BANDWIDTH	500			500			kHz
INTERMODULATION DISTORTION (IMD)[4]							
2nd Order Products		−90	**−84**		−90	**−84**	dB
3rd Order Products		−90	**−84**		−90	**−84**	dB

NOTES

[1]f_{IN} amplitude = −0.5 dB (9.44 V p-p) bipolar mode full scale unless otherwise indicated. All measurements referred to a −0 dB (9.997 V p-p) input signal unless otherwise noted.

[2]See Figure 15 for higher frequencies and other input amplitudes.

[3]See Figures 13 and 14 for higher frequencies and other input amplitudes.

[4]f_A = 9.08 kHz, f_B = 9.58 kHz, with f_{SAMPLE} = 100 kSPS. See Definition of Specifications section.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (All device types T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter		Test Conditions	Min	Max	Units
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		**2.0**	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	**0.8**	V
I_{IH}	High Level Input Current	V_{IN} = 5 V	**−10**	**+10**	µA
I_{IL}	Low Level Input Current	V_{IN} = 0 V	**−10**	**+10**	µA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	4.0		V
		I_{OH} = 0.5 mA	**2.4**		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		**0.4**	V
I_{OZ}	High Z Leakage Current	V_{IN} = 0 or 5 V	**−10**	**+10**	µA
C_{OZ}	High Z Output Capacitance			10	pF

NOTES

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at T_{MIN}, +25°C and T_{MAX}. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10% unless otherwise indicated)

Parameter	AD679J/A/S Min	AD679J/A/S Typ	AD679J/A/S Max	AD679K/B/T Min	AD679K/B/T Typ	AD679K/B/T Max	Units
TEMPERATURE RANGE							
J, K, Grades	0		+70	0		+70	°C
A, B Grades	−40		+85	−40		+85	°C
S, T Grades	−55		+125	−55		+125	°C
ACCURACY							
Resolution	14			14			Bits
Integral Nonlinearity (INL)		±2			±1	±2	LSB
Differential Nonlinearity (DNL)	14			14			Bits
Unipolar Zero Error[1] (@ +25°C)		0.08			0.05	0.07	% FSR*
Bipolar Zero Error[1] (@ +25°C)		0.08			0.05	0.07	% FSR
Gain Error[1, 2] (@ +25°C)		0.12			0.09	0.11	% FSR
Temperature Drift							
Unipolar Zero[3]							
J, K Grades		0.04			0.04	0.05	% FSR
A, B Grades		0.05			0.05	0.07	% FSR
S, T Grades		0.09			0.09	0.10	% FSR
Bipolar Zero[3]							
J, K Grades		0.02			0.02	0.04	% FSR
A, B Grades		0.04			0.04	0.05	% FSR
S, T Grades		0.08			0.08	0.09	% FSR
Gain[3]							
J, K Grades		0.09			0.09	0.11	% FSR
A, B Grades		0.10			0.10	0.16	% FSR
S, T Grades		0.20			0.20	0.25	% FSR
Gain[4]							
J, K Grades		0.04			0.04	0.05	% FSR
A, B Grades		0.05			0.05	0.07	% FSR
S, T Grades		0.09			0.09	0.10	% FSR
ANALOG INPUT							
Input Ranges							
Unipolar Mode	0		+10	0		+10	V
Bipolar Mode	−5		+5	−5		+5	V
Input Resistance		10			10		MΩ
Input Capacitance		10			10		pF
Input Settling Time			1.5			1.5	µs
Aperture Delay		10			10		ns
Aperture Jitter		150			150		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage[5]	4.98		5.02	4.98		5.02	V
External Load							
Unipolar Mode			+1.5			+1.5	mA
Bipolar Mode			+0.5			+0.5	mA
POWER SUPPLIES							
Power Supply Rejection							
V_{CC} = + 12 V ± 5%		±6				±6	LSB
V_{EE} = −12 V ± 5%		±6				±6	LSB
V_{DD} = +5 V ± 10%		±6				±6	LSB
Operating Current							
I_{CC}		18	20		18	20	mA
I_{EE}		25	34		25	34	mA
I_{DD}		8	12		8	12	mA
Power Consumption		560	745		560	745	mW

NOTES
[1]Adjustable to zero. See Figures 5 and 6.
[2]Includes internal voltage reference error.
[3]Includes internal voltage reference drift.
[4]Excludes internal voltage reference drift.
[5]With maximum external load applied.
*% FSR = percent of full-scale range.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at T_{MIN}, 25°C and T_{MAX}. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

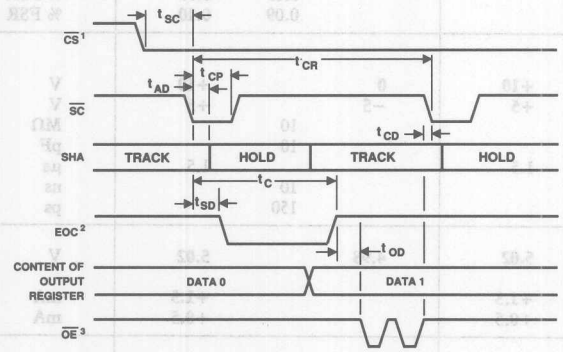
TIMING SPECIFICATIONS (All device types T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter	Symbol	Min	Max	Units
$\overline{SC}$ Delay	t_{SC}	50		ns
Conversion Time	t_C		6.3	µs
Conversion Rate[1]	t_{CR}		7.8	µs
Convert Pulse Width	t_{CP}	97		ns
Aperture Delay	t_{AD}	5	20	ns
Status Delay	t_{SD}	**0**	**400**	ns
Access Time[2, 3]	t_{BA}	10	**100**	ns
		10	**57**[4]	ns
Float Delay[5]	t_{FD}	**10**	**80**	ns
Output Delay	t_{OD}		**0**	ns
Format Setup	t_{FS}	**100**		ns
$\overline{OE}$ Delay	t_{OE}	**20**		ns
Read Pulse Width	t_{RP}	**195**		ns
Conversion Delay	t_{CD}	**400**		ns
$\overline{EOCEN}$ Delay	t_{EO}	**50**		ns

NOTES
[1]Includes Acquisition Time.
[2]Measured from the falling edge of $\overline{OE}$/$\overline{EOCEN}$ (0.8 V) to the time at which the data lines/EOC cross 2.0 V or 0.8 V. See Figure 4.
[3]C_{OUT} = 100 pF.
[4]C_{OUT} = 50 pF.
[5]Measured from the rising edge of $\overline{OE}$/$\overline{EOCEN}$ (2.0 V) to the time at which the output voltage changes by 0.5. See Figure 4; C_{OUT} = 10 pF.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at T_{MIN}, +25°C and T_{MAX}. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.



NOTES
[1]IN ASYNCHRONOUS MODE, STATE OF $\overline{CS}$ DOES NOT AFFECT OPERATION. SEE THE START CONVERSION TRUTH TABLE FOR DETAILS.
[2]$\overline{EOCEN}$ = LOW (SEE FIGURE 3). IN SYNCHRONOUS MODE, EOC IS A THREE-STATE OUTPUT. IN ASYNCHRONOUS MODE, EOC IS AN OPEN DRAIN OUTPUT.
[3]DATA SHOULD NOT BE ENABLED DURING A CONVERSION.

Figure 1. Conversion Timing

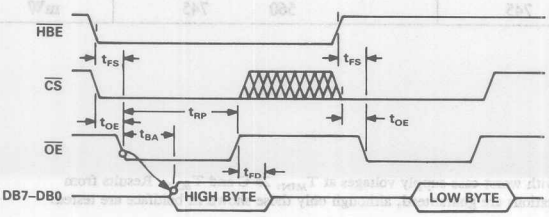
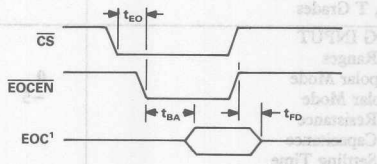


Figure 2. Output Timing



NOTE
[1]EOC IS A THREE-STATE OUTPUT IN SYNCHRONOUS MODE AND AN OPEN DRAIN OUTPUT IN ASYNCHRONOUS. ACCESS (t_{BA}) AND FLOAT (t_{FD}) TIMING SPECIFICATIONS DO NOT APPLY IN ASYNCHRONOUS MODE WHERE THEY ARE A FUNCTION THE TIME CONSTANT FORMED BY THE 10 pF OUTPUT CAPACITANCE AND THE PULL-UP RESISTOR.

Figure 3. EOC Timing

TEST	V_{CP}	C_{OUT}
ACCESS TIME HIGH Z TO LOGIC LOW	5 V	100 pF
FLOAT TIME LOGIC HIGH TO HIGH Z	0 V	10 pF
ACCESS TIME HIGH Z TO LOGIC HIGH	0 V	100 pF
FLOAT TIME LOGIC LOW TO HIGH Z	5 V	10 pF

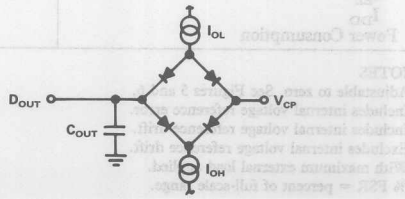


Figure 4. Load Circuit for Bus Timing Specifications

ABSOLUTE MAXIMUM RATINGS*

Specification	With Respect To	Min	Max	Units
V_{CC}	AGND	−0.3	+18	V
V_{EE}	AGND	−18	+0.3	V
V_{CC}	V_{EE}	−0.3	+26.4	V
V_{DD}	DGND	0	+7	V
AGND	DGND	−1	+1	V
AIN, REF_{IN}	AGND	V_{EE}	V_{CC}	V
Digital Inputs	DGND	−0.5	+7	V
Digital Outputs	DGND	−0.5	V_{DD} +0.3	V
Max Junction Temperature			175	°C

Specification	With Respect To	Min	Max	Units
Operating Temperature				
J and K Grades		0	+70	°C
A and B Grades		−40	+85	°C
S and T Grades		−55	+125	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec max)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

ESD SENSITIVITY

The AD679 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD679 has been classified as a Category 1 device.



Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.

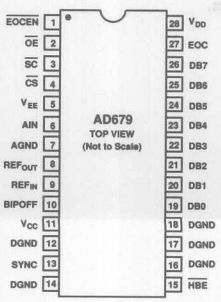
ORDERING GUIDE

Model	Package	Temperature Range	Tested and Specified	Package Option*
AD679JN	28-Pin Plastic DIP	0°C to +70°C	AC	N-28
AD679KN	28-Pin Plastic DIP	0°C to +70°C	AC + DC	N-28
AD679JD	28-Pin Ceramic DIP	0°C to +70°C	AC	D-28A
AD679KD	28-Pin Ceramic DIP	0°C to +70°C	AC + DC	D-28A
AD679AD	28-Pin Ceramic DIP	−40°C to +85°C	AC	D-28A
AD679BD	28-Pin Ceramic DIP	−40°C to +85°C	AC + DC	D-28A
AD679SD	28-Pin Ceramic DIP	−55°C to +125°C	AC	D-28A
AD679TD	28-Pin Ceramic DIP	−55°C to +125°C	AC + DC	D-28A
AD679AJ	44-Lead Ceramic JLCC	−40°C to +85°C	AC	J-44
AD679BJ	44-Lead Ceramic JLCC	−40°C to +85°C	AC + DC	J-44
AD679SJ	44-Lead Ceramic JLCC	−55°C to +125°C	AC	J-44
AD679TJ	44-Lead Ceramic JLCC	−55°C to +125°C	AC + DC	J-44

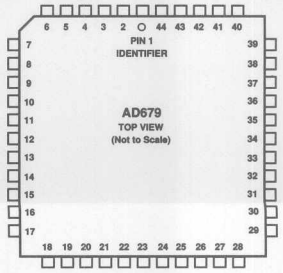
*N = Plastic DIP; D = Ceramic DIP; J = J-Leaded Ceramic Chip Carrier. For outline information, see Package Information section.

PIN CONFIGURATION

DIP Package



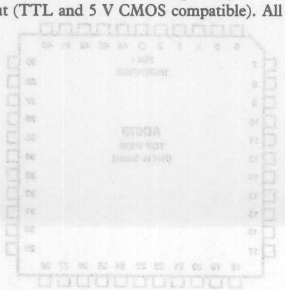
JLCC Package



PIN DESCRIPTION

Symbol	28-Pin DIP Pin No.	44-Lead JLCC Pin No.	Type	Name and Function
AGND	7	11	P	Analog Ground. This is the ground return for AIN only.
AIN	6	10	AI	Analog Signal Input.
BIPOFF	10	15	AI	Bipolar Offset. Connect to AGND for +10 V input unipolar mode and straight binary output coding. Connect to REF_{OUT} for ±5 V input bipolar mode and twos complement binary output coding.
$\overline{CS}$	4	6	DI	Chip Select. Active LOW.
DGND	12, 14	23	P	Digital Ground.
DB7–DB0	26–19	40, 39, 37 36, 35, 34 33, 31	DO	Data Bits. These pins provide all 14 bits in two bytes (8+6 bits). Active HIGH.
EOC	27	42	DO	End-of-Convert. EOC goes LOW when a conversion starts and goes HIGH when the conversion finishes. In asynchronous mode, EOC is an open drain output and requires an external 3 kΩ pull-up resistor. See $\overline{EOCEN}$ and SYNC pins for information on EOC gating.
$\overline{EOCEN}$	1	1	DI	End-of-Convert Enable. Enables EOC pin. Active LOW.
$\overline{HBE}$	15	25	DI	High Byte Enable. If LOW, output contains high byte. If HIGH, output contains low byte (corresponding to the most recently read high byte).
$\overline{OE}$	2	3	DI	Output Enable. A down-going transition on $\overline{OE}$ enables DB7–DB0. Gated with $\overline{CS}$. Active LOW.
REF_{IN}	9	14	AI	Reference Input. +5 V input gives 10 V full scale range.
REF_{OUT}	8	12	AO	+5 V Reference Output. Tied to REF_{IN} for normal operation.
$\overline{SC}$	3	5	DI	Start Convert. Active LOW. See SYNC pin for gating.
SYNC	13	21	DI	SYNC Control. If tied to V_{DD} (synchronous mode), $\overline{SC}$ and $\overline{EOCEN}$ are gated by $\overline{CS}$. If tied to DGND (asynchronous mode), $\overline{SC}$ and $\overline{EOCEN}$ are independent of $\overline{CS}$, and EOC is an open drain output. EOC requires an external 3 kΩ pull-up resistor in asynchronous mode.
V_{CC}	11	17	P	+12 V Analog Power.
V_{EE}	5	8	P	−12 V Analog Power.
V_{DD}	28	43	P	+5 V Digital Power.
—	16		U	Tie to DGND.
—	17–18	2, 4, 7, 9, 13 16, 18, 19, 20, 22, 24, 26, 27, 28, 29, 30, 32, 38, 41, 44	U	These pins are unused and should be connected to DGND or V_{DD}.

Type: AI = Analog Input.
AO = Analog Output.
DI = Digital Input (TTL and 5 V CMOS compatible).
DO = Digital Output (TTL and 5 V CMOS compatible). All DO pins are three-state drivers.
P = Power.
U = Unused.





NYQUIST FREQUENCY
An implication of the Nyquist sampling theorem, the "Nyquist Frequency" of a converter is that input frequency which is one-half the sampling frequency of the converter.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

TOTAL HARMONIC DISTORTION (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of a full-scale input signal and is expressed as a percentage or in decibels. For input signals or harmonics that are above the Nyquist frequency, the aliased component is used.

PEAK SPURIOUS OR PEAK HARMONIC COMPONENT
The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in decibels relative to the rms value of a full-scale input signal.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb) and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (fa − 2 fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude and the peak value of their sum is −0.5 dB from full scale (9.44 V p–p). The IMD products are normalized to a 0-dB input signal.

BANDWIDTH
The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

The full-linear bandwidth is the input frequency at which the slew rate limit of the sample-hold-amplifier (SHA) is reached. At this point, the amplitude of the reconstructed fundamental has degraded by less than −0.1 dB. Beyond this frequency, distortion of the sampled input signal increases significantly.

The AD679 has been designed to optimize input bandwidth, allowing it to undersample input signals with frequencies significantly above the converter's Nyquist frequency.

APERTURE DELAY
Aperture delay is a measure of the SHA's performance and is measured from the falling edge of Start Convert ($\overline{SC}$) to when the input signal is held for conversion. In synchronous mode, Chip Select ($\overline{CS}$) should be LOW before $\overline{SC}$ to minimize aperture delay.

APERTURE JITTER
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

INPUT SETTLING TIME
Settling time is a function of the SHA's ability to track fast slewing signals. This is specified as the maximum time required in track mode after a full-scale step input to guarantee rated conversion accuracy.

DIFFERENTIAL NONLINEARITY (DNL)
In an ideal ADC, code transitions are 1 LSB apart. Differential linearity is the deviation from this ideal value. It is often specified in terms of resolution for which no missing codes (NMC) are guaranteed.

INTEGRAL NONLINEARITY (INL)
The ideal transfer function for a linear ADC is a straight line drawn between "zero" and "full scale." The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition. Integral linearity error is the worst case deviation of a code from the straight line. The deviation of each code is measured from the middle of that code.

Note that the linearity error is not user adjustable.

POWER SUPPLY REJECTION
Variations in power supply will affect the full-scale transition, but not the converter's linearity. Power Supply Rejection is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

TEMPERATURE DRIFT
This is the maximum change in the parameter from the initial value (@+25°C) to the value at T_{MIN} or T_{MAX}.

UNIPOLAR ZERO ERROR
In unipolar mode, the first transition should occur at a level 1/2 LSB above analog ground. Unipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

BIPOLAR ZERO ERROR
In the bipolar mode, the major carry transition (11 1111 1111 1111 to 00 0000 0000 0000) should occur at an analog value 1/2 LSB below analog ground. Bipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

GAIN ERROR
The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale (9.9991 volts for a 0–10 V range, 4.9991 volts for a ±5 V range). The gain error is the deviation of the actual level at the last transition from the ideal level with the zero error trimmed out. This error can be adjusted as shown in the Input Connections and Calibration section.

CONVERSION CONTROL

In synchronous mode (SYNC = HIGH), both Chip Select ($\overline{CS}$) and Start Convert ($\overline{SC}$) must be brought LOW to start a conversion. $\overline{CS}$ should be LOW t_{SC} before $\overline{SC}$ is brought LOW. In asynchronous mode (SYNC = LOW), a conversion is started by bringing $\overline{SC}$ low, regardless of the state of $\overline{CS}$.

Before a conversion is started, End-of-Convert (EOC) is HIGH and the sample-hold is in track mode. After a conversion is started, the sample-hold goes into hold mode and EOC goes LOW, signifying that a conversion is in progress. During the conversion, the sample-hold will go back into track mode and start acquiring the next sample.

In track mode, the sample-hold will settle to ±0.003% (14 bits) in 1.5 µs maximum. The acquisition time does not affect the throughput rate as the AD679 goes back into track mode more than 2 µs before the next conversion. In multichannel systems, the input channel can be switched as soon as EOC goes LOW.

Bringing $\overline{OE}$ LOW t_{OE} after $\overline{CS}$ goes LOW makes the output register contents available on the output data bits (DB7–DB0). A period of time t_{CD} is required after $\overline{OE}$ is brought HIGH before the next $\overline{SC}$ instruction is issued.

If $\overline{SC}$ is held LOW, conversion accuracy may deteriorate. For this reason, $\overline{SC}$ should not be held low in an attempt to operate in a continuously converting mode.

START CONVERSION TRUTH TABLE

	INPUTS			
	SYNC	$\overline{CS}$	$\overline{SC}$	STATUS
Synchronous Mode	1	1	X	No Conversion
	1	0	↓	Start Conversion
	1	↓	0	Start Conversion (Not Recommended)
	1	0	0	Continuous Conversion (Not Recommended)
Asynchronous Mode	0	X	1	No Conversion
	0	X	↓	Start Conversion
	0	X	0	Continuous Conversion (Not Recommended)

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
↓ = HIGH to LOW transition. Must stay low for $t = t_{CP}$.

14-BIT MODE CODING FORMAT (1 LSB = 0.61 mV)

Unipolar Coding (Straight Binary)		Bipolar Coding (Twos Complement)	
V_{IN}*	Output Code	V_{IN}*	Output Code
0.00000 V	000 . . . 0	−5.00000 V	100 . . . 0
5.00000 V	100 . . . 0	−0.00061 V	111 . . . 1
9.99939 V	111 . . . 1	0.00000 V	000 . . . 0
		+2.50000 V	010 . . . 0
		+4.99939 V	011 . . . 1

*Code center.

END-OF-CONVERT

In asynchronous mode, End-of-Convert (EOC) is an open drain output (requiring a minimum 3 kΩ pull-up resistor) enabled by End-of-Convert Enable ($\overline{EOCEN}$). In synchronous mode, EOC is a three-state output which is enabled by $\overline{EOCEN}$ and $\overline{CS}$. See Conversion Status Truth Table. Access (t_{BA}) and float (t_{FD}) timing specifications do not apply in asynchronous mode where they are a function of the time constant formed by the external load capacitance and the pull-up resistor.

OUTPUT ENABLE OPERATION

The data bits (DB7–DB0) are three-state outputs that are enabled by Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$). $\overline{CS}$ should be LOW t_{OE} before $\overline{OE}$ is brought LOW.

When EOC goes HIGH, the conversion is completed and the output data may be read. The output is read in two steps as a 16-bit word, with the high byte read first, followed by the low byte. High Byte Enable ($\overline{HBE}$) controls the output sequence. The 14-bit result is left justified within the 16-bit field.

In unipolar mode (BIPOFF tied to AGND), the output coding is straight binary. In bipolar mode (BIPOFF tied to REF_{OUT}), output coding is twos-complement binary.

POWER-UP

The AD679 typically requires 10 µs after power-up to reset internal logic.

CONVERSION STATUS TRUTH TABLE

	INPUTS			OUTPUT	
	SYNC	$\overline{CS}$	$\overline{EOCEN}$	EOC	STATUS
Synchronous Mode	1	0	0	0	Converting
	1	0	0	1	Not Converting
	1	1	X	High Z	Either
	1	X	1	High Z	Either
Asynchronous Mode*	0	X	0	0	Converting
	0	X	0	High Z	Not Converting
	0	X	1	High Z	Either

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
*EOC requires a pull-up resistor in asynchronous mode.

OUTPUT ENABLE TRUTH TABLE

	INPUTS		OUTPUTS							
	$\overline{HBE}$	($\overline{CS}$ U $\overline{OE}$)	DB7 . . . DB0							
	X	1	← High Z →							
Unipolar or Bipolar	0	0	a	b	c	d	e	f	g	h
	1	0	i	j	k	l	m	n	0	0

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
U = Logical OR.
a = MSB.
n = LSB.
Data coding is binary for Unipolar Mode and 2s Complement Binary for Bipolar Mode.

INPUT CONNECTIONS AND CALIBRATION

The high (10 MΩ) input impedance of the AD679 eases the task of interfacing to high source impedances or multiplexer channel-to-channel mismatches of up to 300 Ω. The 10 V p–p full scale input range accepts the majority of signal voltages without the need for voltage divider networks which could deteriorate the accuracy of the ADC.

The AD679 is factory trimmed to minimize offset, gain and linearity errors. In unipolar mode, the only external component that is required is a 50 Ω ±1% resistor. Two resistors are required in bipolar mode. If offset and gain are not critical (as in some ac applications), even these components can be eliminated.

In some applications, offset and gain errors need to be trimmed out completely. The following sections describe the correct procedure for these various situations.

BIPOLAR RANGE INPUTS

The connections for the bipolar mode are shown in Figure 5. In this mode, data output coding will be twos complement binary. This circuit will allow approximately ±25 mV of offset trim range (±40 LSB) and ±0.5% of gain trim range (±80 LSB).

Either or both of the trim pots can be replaced with 50 Ω ±1% fixed resistors if the AD679 accuracy limits are sufficient for application. If the pins are shorted together, the additional offset and gain errors will be approximately 80 LSB.

To trim bipolar zero to its nominal value, apply a signal 1/2 LSB below midrange (−0.305 mV for a ±5 V range) and adjust R1 until the major carry transition is located (11 1111 1111 1111 to 00 0000 0000 0000). To trim the gain, apply a signal 1 1/2 LSB below full scale (+4.9991 V for a ±5 V range) and adjust R2 to give the last positive transition (01 1111 1111 1110 to 01 1111 1111 1111). These trims are interactive so several iterations may be necessary for convergence.

A single pass calibration can be done by substituting a bipolar offset trim (error at minus full scale) for the bipolar zero trim (error at midscale), using the same circuit. First, apply a signal 1/2 LSB above minus full scale (−4.9997 V for a ±5 V range) and adjust R1 until the minus full scale transition is located (10 0000 0000 0000 to 10 000 000 0001). Then perform the gain error trim as outlined above.

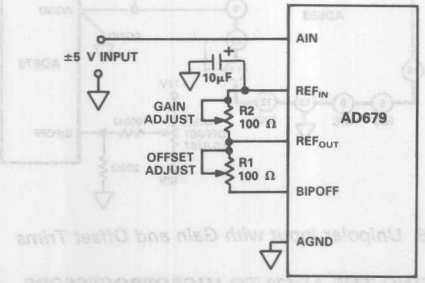


Figure 5. Bipolar Input Connections with Gain and Offset Trims

UNIPOLAR RANGE INPUTS

Offset and gain errors can be trimmed out by using the configuration shown in Figure 6. This circuit allows approximately ±25 mV of offset trim range (±40 LSB) and ±0.5% of gain trim range (±80 LSB).

The nominal offset is 1/2 LSB so that the analog range that corresponds to each code will be centered in the middle of that code (halfway between the transitions to the codes above and below it). Thus the first transition (from 00 0000 0000 0000 to 00 0000 0000 0001) should nominally occur for an input level of +1/2 LSB (0.305 mV above ground for a 10 V range). To trim unipolar zero to this nominal value, apply a 0.305 mV signal to AIN and adjust R1 until the first transition is located.

The gain trim is done by adjusting R2. If the nominal value is required, apply a signal 1 1/2 LSB below full scale (9.9997 V for a 10 V range) and adjust R2 until the last transition is located (11 1111 1111 1110 to 11 1111 1111 1111).

If offset adjustment is not required, BIPOFF should be connected directly to AGND. If gain adjustment is not required, R2 should be replaced with a fixed 50 Ω ±1% metal film resistor. If REF_{OUT} is connected directly to REF_{IN}, the additional gain error will be approximately 1%.

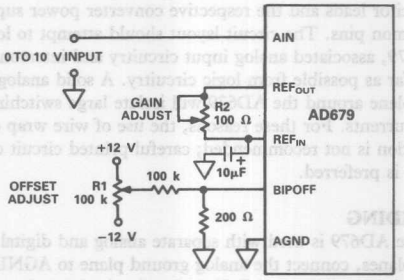


Figure 6. Unipolar Input Connections with Gain and Offset Trims

REFERENCE DECOUPLING

It is recommended that a 10 μF tantalum capacitor be connected between REF_{IN} (Pin 9) and ground. This has the effect of improving the S/N+D ratio through filtering possible broadband noise contributions from the voltage reference.

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is a significant issue. A 1.22 mA current through a 0.5 Ω trace will develop a voltage drop of 0.6 mV, which is 1 LSB at the 14 bit level for a 10 V full scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter out ac noise.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog

connection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

The AD679 incorporates several features to help the user's layout. Analog pins (V_{EE}, AIN, AGND, REF_{OUT}, REF_{IN}, BIPOFF, V_{CC}) are adjacent to help isolate analog from digital signals. In addition, the 10 MΩ input impedance of AIN minimizes input trace impedance errors. Finally, ground currents have been minimized by careful circuit architecture. Current through AGND is 200 μA, with no code dependent variation. The current through DGND is dominated by the return current for DB7–DB0 and EOC.

SUPPLY DECOUPLING

The AD679 power supplies should be well filtered, well regulated, and free from high frequency noise. Switching power supplies are not recommended due to their tendency to generate spikes which can induce noise in the analog system.

Decoupling capacitors should be used in very close layout proximity between all power supply pins and analog ground. A 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor provides adequate decoupling.

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD679, associated analog input circuitry and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD679 will isolate large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

GROUNDING

If a single AD679 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD679. If multiple AD679s are used or the AD679 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at each chip. This prevents large ground loops which inductively couple noise and allow digital currents to flow through the analog system.

USE OF EXTERNAL VOLTAGE REFERENCE

The AD679 features an on-chip voltage reference. For improved gain accuracy over temperature, a high performance external voltage reference may be used in place of the on-chip reference.

The AD586 and AD588 are popular references appropriate for use with high resolution converters. The AD586 is a low cost reference which utilizes a buried Zener architecture to provide low noise and drift. The AD588 is a higher performance reference which uses a proprietary ion-implanted buried Zener diode in conjunction with laser-trimmed thin-film resistors for low offset and low drift.

Figure 7 shows the use of the AD586 with the AD679 in a bipolar input mode. Over the 0 to +70°C range, the AD586 L-grade exhibits less than a 2.25 mV output change from its initial value at 25°C. REF_{IN} (Pin 9) scales its input by a factor of two; thus, AD679, this results in a total gain drift of 0.09% FSR, which is an improvement over the on-chip reference performance of 0.11% FSR. A noise-reduction capacitor, C_N, has been shown. This capacitor reduces the broadband noise of the AD586 output, thereby optimizing the overall ac and dc performance of the AD679.

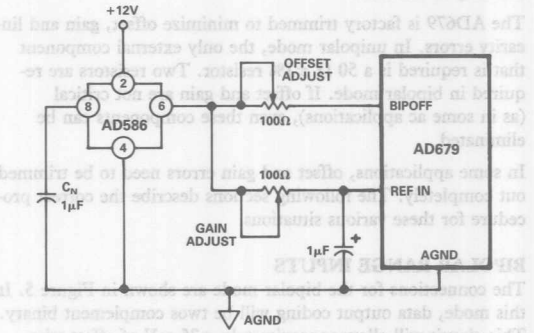


Figure 7. Bipolar Input with Gain and Offset Trims

Figure 8 shows the AD679 in unipolar input mode with the AD588 reference. The AD588 output is accurate to 0.65 mV from its value at 25°C over the 0 to 70°C range. This results in a 0.06% FSR total gain drift for the AD679, which is a substantial improvement over the on-chip reference performance of 0.11% FSR. A noise-reduction network on Pins 4, 6 and 7 has been shown. The 1 μF capacitors form low pass filters with the internal resistance of the AD588 Zener and amplifier cells and external resistance. This reduces the high frequency (to 1 MHz) noise of the AD588, providing optimum ac and dc performance of the AD679.

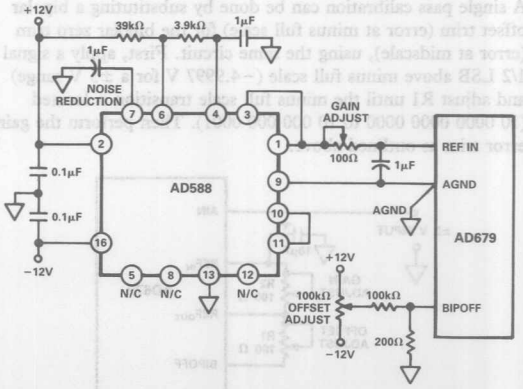


Figure 8. Unipolar Input with Gain and Offset Trims

INTERFACING THE AD679 TO MICROPROCESSORS

The I/O capabilities of the AD679 allow direct interfacing to general purpose and DSP microprocessor buses. The asynchronous conversion control feature allows complete flexibility and control with minimal external hardware.

The following examples illustrate typical AD679 interface configurations.

AD679 to TMS320C25

In Figure 9 the AD679 is mapped into the TMS320C25 I/O space. AD679 conversions are initiated by issuing an OUT instruction to Port 1. EOC status and the conversion result are read in with an IN instruction to Port 1. A single wait state is inserted by generating the processor READY input from $\overline{IS}$, Port 1 and $\overline{MSC}$. Address line A0 provides $\overline{HBE}$ decoding to select between the high and low bytes of data. This configuration supports processor clock speeds of 20 MHz and is capable of supporting processor clock speeds of 40 MHz if a NOP instruction follows each AD679 read instruction.

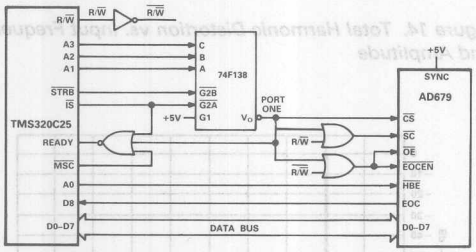


Figure 9. AD679 to TMS320C25 Interface

AD679 to 80186

Figure 10 shows the AD679 interfaced to the 80186 microprocessor. This interface allows the 80186's built-in DMA controller to transfer the AD679 output into a RAM based FIFO buffer of any length, with no microprocessor intervention.

In this application the AD679 is configured in the asynchronous mode, which allows conversions to be initiated by an external trigger source independent of the microprocessor clock. After each conversion, the AD679 EOC signal generates a DMA request to Channel 1 (DRQ1). The subsequent DMA READ sequences the high and low byte AD679 data and resets the interrupt latch. The system designer must assign a sufficient priority to the DMA channel to ensure that the DMA request will be serviced before the completion of the next conversion. This configuration can be used with 6 MHz and 8 MHz 80186 processors.

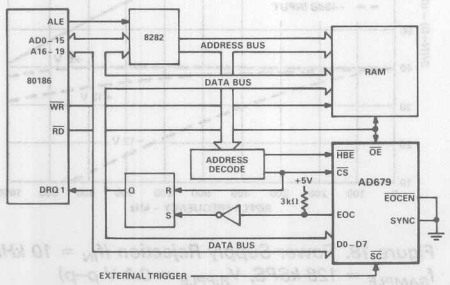


Figure 10. AD679 to 80186 DMA Interface

AD679 to Analog Devices ADSP-2101

Figure 11 demonstrates the AD679 interfaced to an ADSP-2101. With a clock frequency of 12.5 MHz, and instruction execution in one 80 ns cycle, the digital signal processor supports the AD679 interface with one wait state.

The converter is configured to run asynchronously using a sampling clock. The EOC output of the AD679 gets asserted at the end of each conversion and causes an interrupt. Upon interrupt, the ADSP-2101 immediately asserts its FO pin LOW. In the following cycle, the processor starts a data memory read by providing an address on the DMA bus. The decoded address generates $\overline{OE}$ for the converter, and the high byte of the conversion result is read over the data bus. The read operation is extended with one wait state and thus started and completed within two processor cycles (160 ns). Next, the ADSP-2101 asserts its FO HIGH. This allows the processor to start reading the lower byte of data. This read operation executes in a similar manner to the first and is completed during the next 160 ns.

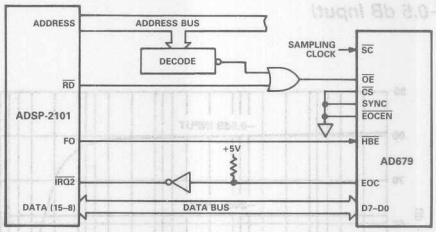


Figure 11. AD679 to ADSP-2101 Interface

AD679 to Analog Devices ADSP-2100A

Figure 12 demonstrates the AD679 interfaced to an ADSP-2100A. With a clock frequency of 12.5 MHz, and instruction execution in one 80 ns cycle, the digital signal processor will support the AD679 data memory interface with three hardware wait states.

The converter is configured to run asynchronously using a sampling clock. The EOC output of the AD679 gets asserted at the end of each conversion and causes an interrupt. Upon interrupt, the ADSP-2100A immediately executes a data memory write instruction which asserts $\overline{HBE}$. In the following cycle, the processor starts a data memory read (high byte read) by providing an address on the DMA bus. The decoded address generates $\overline{OE}$ for the converter. $\overline{OE}$, together with logic and latch, is used to force the ADSP-2100A into a one cycle wait state by generating DMACK. The read operation is thus started and completed within two processor cycles (160 ns). $\overline{HBE}$ is released during "high byte read." This allows the processor to read the lower byte of data as soon as "high byte read" is complete. The low byte read operation executes in a similar manner to the first and is completed during the next 160 ns.

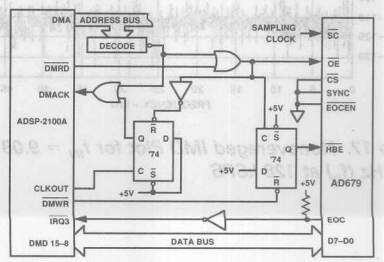


Figure 12. AD679 to ADSP-2100A Interface

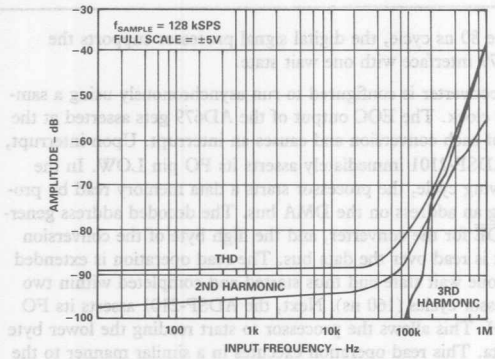


Figure 13. Harmonic Distortion vs. Input Frequency (−0.5 dB Input)

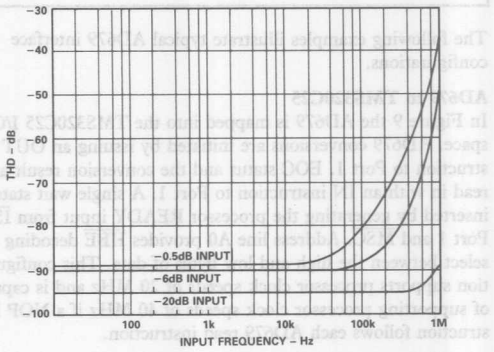


Figure 14. Total Harmonic Distortion vs. Input Frequency and Amplitude

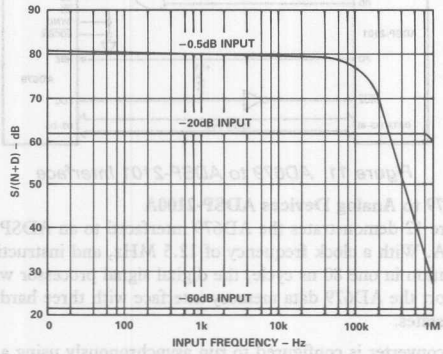


Figure 15. S/(N+D) vs. Input Frequency and Amplitude

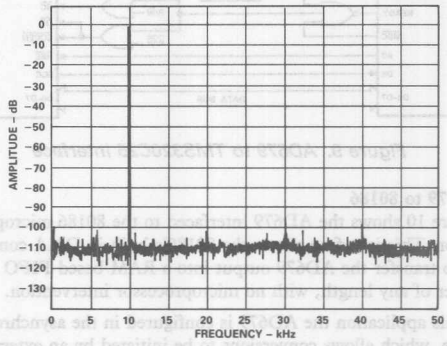


Figure 16. 5-Plot Averaged 2048 Point FFT at 128 kSPS, f_{IN} = 10.009 kHz

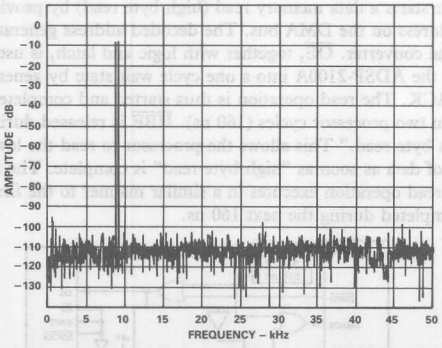


Figure 17. Nonaveraged IMD Plot for f_{IN} = 9.08 kHz (f_a), 9.58 kHz (f_b) at 128 kSPS

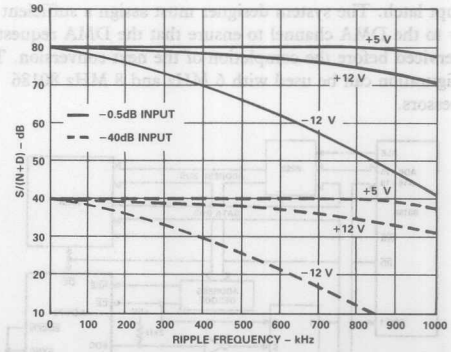


Figure 18. Power Supply Rejection (f_{IN} = 10 kHz, f_{SAMPLE} = 128 kSPS, V_{RIPPLE} = 0.1 V p–p)

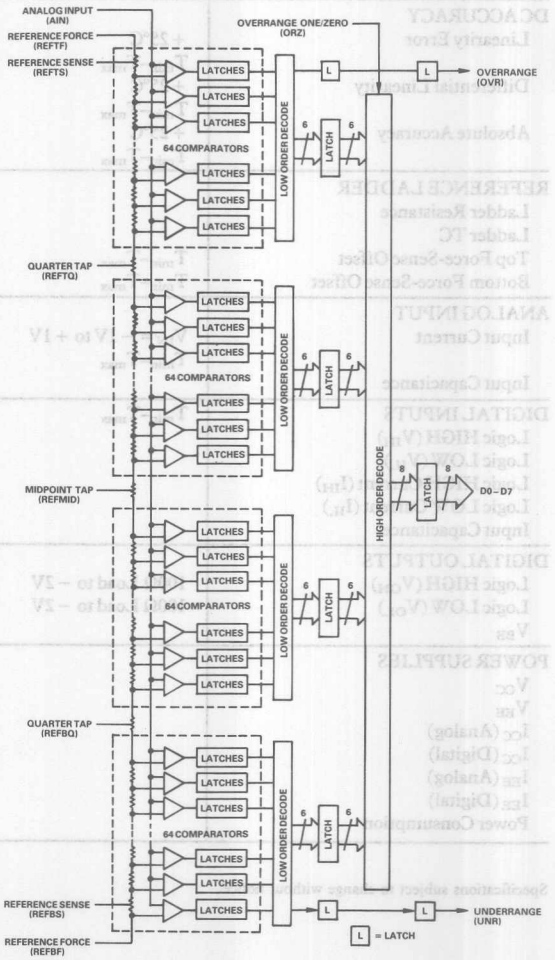
200 MSPS Wideband 8-Bit A/D Converter

AD770*

FEATURES

250MHz Full Power Bandwidth
200 MSPS Guaranteed Conversion Rate
19pF typ Input Capacitance
Unipolar and Bipolar Input Range
+5V/−5.2V Power Supplies
Overflow and Underflow Signals

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD770 is an 8-bit analog-to-digital converter that is designed for high-speed digitization of wide-bandwidth signals. It uses an advanced VLSI bipolar process and a proprietary design to achieve a combination of sampling rate and signal bandwidth previously unavailable in flash ADCs.

The AD770 incorporates 257 high speed comparators that are optimized for low input capacitance and wide bandwidth, unaffected by temperature or signal amplitude. The multistage comparator design reduces the probability of errors due to metastable states or insufficient gain.

The decoding logic further reduces errors by using a two-stage error-correcting architecture to virtually eliminate "sparkle codes." Inputs and outputs are ECL compatible. Output format controls allow stacking of two devices for 9-bit resolution. Overflow and underflow output signals are provided.

The AD770 can operate with unipolar and bipolar signal ranges up to 4V p-p. End-point reference Force and Sense connections are provided to preserve high accuracy and minimize temperature drift. Midpoint and quarter-point reference taps are also provided to allow linearity or transfer function corrections.

The AD770 is available in three grades. The JD and KD grades are specified for operation over the 0 to +70°C temperature range, while the SD grade is specified for the −55°C to +125°C temperature range. All grades are packaged in a 40-pin ceramic DIP. Other package options are available on request; please contact the factory.

PRODUCT HIGHLIGHTS

1. **Performance:** The AD770 is specified for operation at 200 MSPS. Full power bandwidth is 250MHz; small signal bandwidth is 400MHz.
2. **Ease of Use:** The AD770 input has a typical capacitance of 19pF, simplifying input buffering requirements. Bipolar and unipolar input signals can be converted without offsetting. Differential or single-ended clock inputs can be accommodated by pin-strapping.
3. **Features:** Taps are provided at mid- and quarter-scale points of the reference ladder to permit linearity trimming or piecewise-linear transfer function modification. Overflow and underflow signals are also provided. These can be wire-or'd to provide an indication that the input signal has exceeded the range of the converter.

*Protected by U.S. Patent No. 4,884,075.

Parameter	Conditions	AD770J/S Min	AD770J/S Typ	AD770J/S Max	AD770K Min	AD770K Typ	AD770K Max	Units
TEMPERATURE RANGE	AD770J, AD770K	0		+70	0		+70	°C
	AD770S	−55		+125				°C
RESOLUTION		8			8			Bits
DC ACCURACY								
Linearity Error	+25°C	−1		+1	−0.75		+0.75	LSB
	T_{min}–T_{max}	−1.25		+1.25	−1		+1	LSB
Differential Linearity	+25°C	−0.9		+0.9	−0.75		+0.75	LSB
	T_{min}–T_{max}	−1.25		+1.25	−0.9		+0.9	LSB
Absolute Accuracy	+25°C	−1.75		+1.75	−1		+1	LSB
	T_{min}–T_{max}	−2		+2	−1.25		+1.25	LSB
REFERENCE LADDER								
Ladder Resistance		160	200	260	160	200	260	Ω
Ladder TC			0.34			0.34		%/°C
Top Force-Sense Offset	T_{min}–T_{max}		3	5		3	5	LSB
Bottom Force-Sense Offset	T_{min}–T_{max}		3	5		3	5	LSB
ANALOG INPUT								
Input Current	V_{IN} = −1V to +1V			300			300	μA
	T_{min}–T_{max}			500			500	μA
Input Capacitance		17	19	22	17	19	22	pF
DIGITAL INPUTS	T_{min}–T_{max}							
Logic HIGH (V_{IH})		−1.0		−0.7	−1.0		−0.7	V
Logic LOW (V_{IL})		−1.9		−1.6	−1.9		−1.6	V
Logic HIGH Current (I_{IH})				200			200	μA
Logic LOW Current (I_{IL})				200			200	μA
Input Capacitance			3			3		pF
DIGITAL OUTPUTS								
Logic HIGH (V_{OH})	100Ω Load to −2V	−1.0		−0.7	−1.0		−0.7	V
Logic LOW (V_{OL})	100Ω Load to −2V	−1.9		−1.6	−1.9		−1.6	V
V_{BB}			−1.2			−1.2		V
POWER SUPPLIES								
V_{CC}		4.75	5.0	5.25	4.75	5.0	5.25	V
V_{EE}		−5.46	−5.2	−4.9	−5.46	−5.2	−4.9	V
I_{CC} (Analog)			210	269		210	269	mA
I_{CC} (Digital)			62	78		62	78	mA
I_{EE} (Analog)			54	69		54	69	mA
I_{EE} (Digital)			69	88		69	88	mA
Power Consumption			2000	2550		2000	2550	mW

Specifications subject to change without notice.

Parameter	Conditions		Min	Typ	Max	Min	Typ	Max	Units
TIMING	$T_{min}-T_{max}$, 100Ω Load to −2V								
Max Conversion Rate			**200**			**200**			MSPS
Aperture Delay				340			340		ps
Aperture Jitter				3			3		ps rms
Pipeline Delay			1.5		1.5	1.5		1.5	Clock Cycles
Output Delay			**2**		**6**	**2**		**6**	ns
Output Rise				1			1		ns
Output Fall				1			1		ns
Output Skew				1.4	**2.35**		1.4	**2.35**	ns
DYNAMIC PERFORMANCE (@200 MSPS)	F_{IN} (MHz)	Full Scale A_{IN} (Volts)							
Full-Power Bandwidth		±1		250			250		MHz
Small-Signal Bandwidth		±1		400			400		MHz
Harmonic Distortion[1]	1	±1		50			53		dB
	10	±1		43.5			45.5		dB
	50	±1		35.5			36		dB
	100	±1		25.5			26		dB
	1	±0.5		49			52		dB
	10	±0.5		42			43.5		dB
	50	±0.5		38			39		dB
	100	±0.5		31.5			32		dB
Signal-to-Noise Ratio[1]	1	±1		44.0 (7.0)			44.5 (7.1)		dB (ENOB)
	10	±1		41.5 (6.6)			42.0 (6.7)		dB (ENOB)
	50	±1		34.0 (5.4)			34.5 (5.4)		dB (ENOB)
	100	±1		25.0 (3.9)			25.5 (3.9)		dB (ENOB)
	1	±0.5		40.5 (6.4)			41.0 (6.5)		dB (ENOB)
	10	±0.5		39.0 (6.2)			39.5 (6.3)		dB (ENOB)
	50	±0.5		35.5 (5.6)			35.5 (5.6)		dB (ENOB)
	100	±0.5		30.0 (4.7)			31.0 (4.9)		dB (ENOB)

NOTES
[1]Signal-to-Noise Ratio includes harmonics in the noise factor.
Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

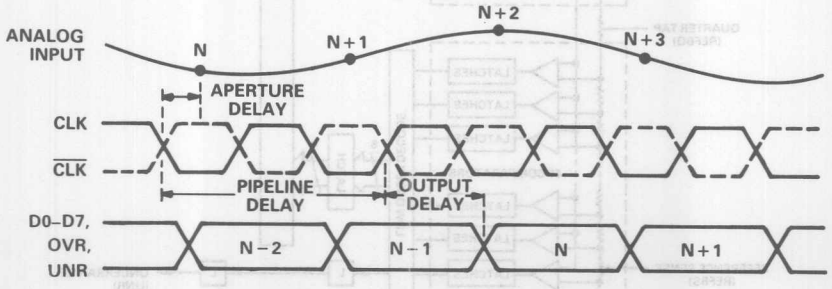
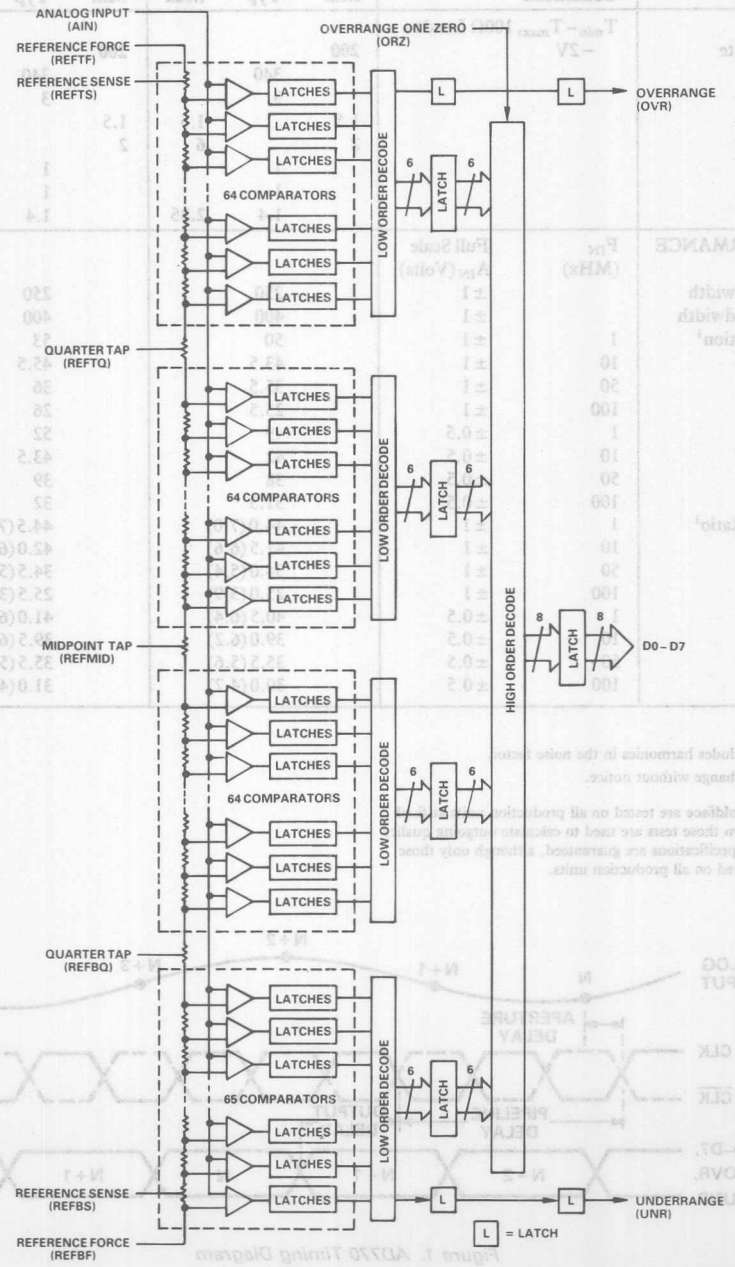


Figure 1. AD770 Timing Diagram

FUNCTIONAL BLOCK DIAGRAM

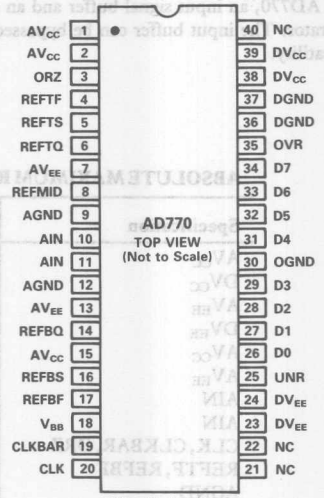


AD770 PIN DESCRIPTION

SYMBOL	PIN NO.	TYPE	NAME AND FUNCTION
AGND	9, 12	P	Analog Ground
AIN	10, 11	AI	Analog Input
AV_{CC}	1, 2, 15	P	+5V Analog Power
AV_{EE}	7, 13	P	5.2V Analog Power
CLK	20	DI	Clock Input
CLKBAR	19	DI	Complementary Clock Input
DGND	36, 37	P	Digital Ground
DV_{CC}	38, 39	P	+5V Digital Power
DV_{EE}	23, 24	P	5.2V Digital Power
D0	26	DO	Data Bit Output (LSB)
D1	27	DO	Data Bit Output
D2	28	DO	Data Bit Output
D3	29	DO	Data Bit Output
D4	31	DO	Data Bit Output
D5	32	DO	Data Bit Output
D6	33	DO	Data Bit Output
D7	34	DO	Data Bit Output (MSB)
DGND	30	P	Digital Output Ground (collectors of output transistors.)
ORZ	3	DI	Overrange Zero. Sets the Polarity of the Data Bits for Overrange Condition. If ORZ%HIGH, D0-D7 are LOW for Overrange Conditions.
OVR	35	DO	Overrange Output. Indicates that AIN$ (REFTS - 0.5LSB).
REFBF	17	AI	Negative Reference Force
REFBQ	14	AI	Negative Reference Quarter Point
REFBS	16	AO	Negative Reference Sense
REFMID	8	AI	Reference Midpoint
REFTF	4	AI	Positive Reference Force
REFTQ	6	AI	Positive Reference Quarter Point
REFTS	5	AO	Positive Reference Sense
UNR	25	DO	Underrange Output. UNR m= HIGH when AIN<(REFBS – 0.5 LSB).
V_{BB}	18	DO	ECL Threshold Output for Clocks

TYPE: AI = Analog Input
AO = Analog Output
DI = Digital Input
DO = Digital Output
P = Power

AD770 PINOUT (40-PIN DIP)



NC = NO CONNECT

2

EVALUATION BOARD

The ADEB770 Evaluation Board allows the designer to easily evaluate the performance of the AD770. The ADEB770 includes a pin-socketed AD770, an input signal buffer and an adjustable reference generator. The input buffer can be bypassed for maximum versatility.

On the output side, latched and buffered digital data is available at the output connector along with an output clock. Decimation hardware allows output data to be undersampled by factors of 16 through 2, allowing the user to interface the board to commonly available logic analyzers.

A reconstructed analog output is also provided by an on-board D/A converter.

ABSOLUTE MAXIMUM RATINGS*

Specification	With Respect to	Min	Max	Units
AV_{CC}	AGND	−0.3	5.5	V
DV_{CC}	DGND	−0.3	5.5	V
AV_{EE}	AGND	−5.72	0.3	V
DV_{EE}	DGND	−5.72	0.3	V
AV_{CC}	DV_{CC}	−0.5	0.5	V
AV_{EE}	DV_{EE}	−0.5	0.5	V
AIN	AGND	−3	+2.25	V
AIN	REFTF, REFBF	−4.3	4.3	V
CLK, CLKBAR, ORZ	AGND	−4.0	0	V
REFTF, REFBF	AGND	−3	+2.25	V
AGND	DGND	−0.5	0.5	V
CLK	CLKBAR	−4.5	4.5	V
I_{AIN}			110	mA
I_{REFTF}, I_{REFBF}			30	mA
I_{REFTS}, I_{REFBS}			3	mA
I_{REFMID}, I_{REFTQ}, I_{REFBQ}			30	mA
I_{BB}			4	mA
I_{CLK}, $I_{CLK\,BAR}$, I_{ORZ}			1	mA
$I_{D0\text{-}D7}$, I_{OVR}, I_{UNR}			40	mA
Junction Temperature			175	°C
Power Dissipation (+25°C)			3	W
Storage Temperature		−65	+150	°C
Thermal Resistance				
θ_{JA} (Still Air) (typ)			36	°C/W
θ_{JC} (typ)			10	°C/W

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Description	Temperature Range	Linearity Error Max @ +25°C	Package Option*
AD770JD	40-Pin Ceramic DIP	0°C to +70°C	±1	D-40
AD770KD	40-Pin Ceramic DIP	0°C to +70°C	±3/4	D-40
AD770SD	40-Pin Ceramic DIP	−55°C to +125°C	±1	D-40
AD770EB-1	Evaluation Board for AD770		±1	
AD770EB-2	Evaluation Board for AD770		±3/4	

*D = Ceramic DIP. For outline information see Package Information section.

DEFINITION OF SPECIFICATIONS

Linearity Error
Linearity Error is the deviation of the transfer function from a reference line. For the AD770, the linearity error is measured from the center of each code to the best-fit straight line.

Differential Linearity
In an ideal ADC, the code transitions are exactly 1LSB apart. The Differential Linearity is the deviation of the transition spacing from the ideal value. A Differential Linearity spec of less than 1LSB signifies that there are no missing output codes over the entire input range.

Absolute Accuracy
The Absolute Accuracy is the deviation of the center-point of each code from a straight line drawn between the reference sense points (REFTS, REFBS).

Force-Sense Offset
The Force-Sense Offset is the difference between the force and sense pin voltages divided by the input range. This offset will cause a corresponding offset error if the full-scale range is defined w.r.t. the reference force lines rather than with respect to the reference sense lines.

Aperture Delay
The delay between the falling edge of CLK and the time at which AIN is sampled.

Aperture Jitter
The sample-to-sample variation in aperture delay.

Pipeline Delay
The delay from the falling edge of CLK that samples the input to the rising edge of CLK that outputs the corresponding digital code.

Output Delay
The delay between the rising edge of CLK and the time when the output bits reach the logic threshold value for bits D0 to D7 and OVR.

Output Skew
The bit-to-bit variation in output delay for bits D0 to D7 and OVR.

Full-Power Bandwidth
The input frequency at which the amplitude of the reconstructed output signal is reduced by 3dB for a full-scale input.

Total Harmonic Distortion (THD)
The rms sum of the first six harmonic components divided by the output signal amplitude. For frequencies above the Nyquist frequency, the aliased components are used.

Signal-to-Noise Ratio (SNR)
The ratio of the signal amplitude to the rms sum of all other spectral components, including harmonics but excluding dc. SNR is expressed in dB and in Effective Number Of Bits (ENOB). These two notations are related by the following formula for full-scale inputs:

$$ENOB = (SNR - 1.8)/6.02$$

(For REFTS = +1.000V, REFBS = −1.000V)

Input			Output		
$A_{IN}>$	$A_{IN}<$	ORZ	D7 . . . . . D0	UNR	OVR
0.996V		0	1 1 1 1 1 1 1 1	0	1
0.996V		1	0 0 0 0 0 0 0 0	0	1
0.988V	0.996V	X	1 1 1 1 1 1 1 1	0	0
0.980V	0.988V	X	1 1 1 1 1 1 1 0	0	0
0.973V	0.980V	X	1 1 1 1 1 1 0 1	0	0
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
−0.004V	0.004V	X	1 0 0 0 0 0 0 0	0	0
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
−0.998V	0.980V	X	0 0 0 0 0 0 1 0	0	0
−0.996V	0.998V	X	0 0 0 0 0 0 0 1	0	0
−1.004	−0.996V	X	0 0 0 0 0 0 0 0	0	0
	−1.004V	X	0 0 0 0 0 0 0 0	1	0

X = Don't care

Table I. AD770 Truth Table

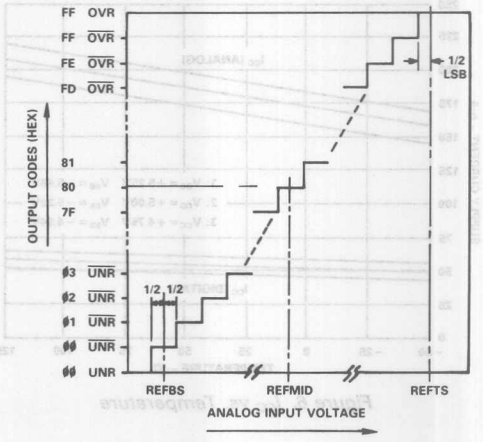


Figure 2. AD770 Transfer Function

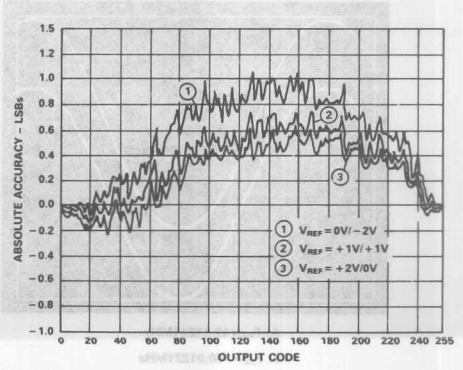


Figure 3. Typical Absolute Accuracy vs. Output Code for Various Range Offsets

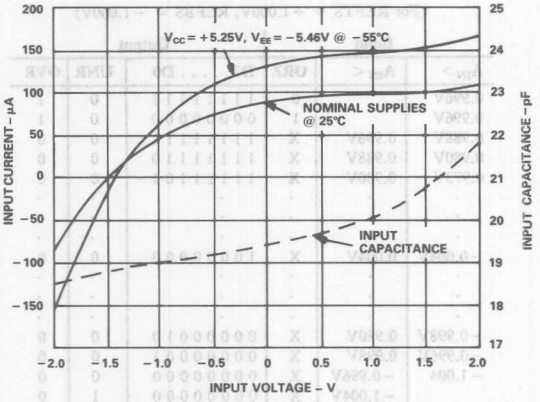


Figure 4. Input Current and Input Capacitance vs. Input Voltage

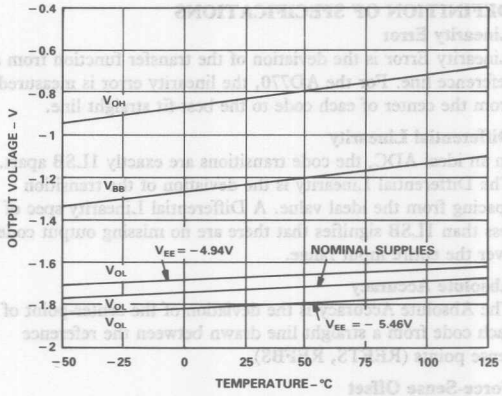


Figure 5. Logic Levels vs. Temperature

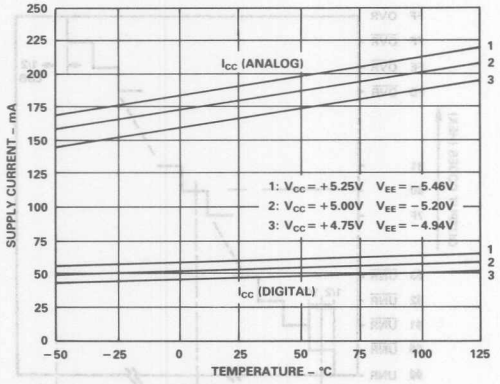


Figure 6. I_{CC} vs. Temperature

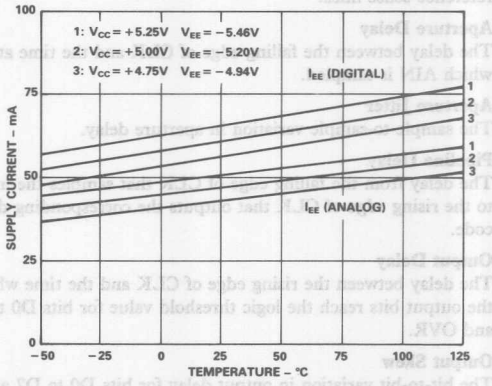


Figure 7. I_{EE} vs. Temperature

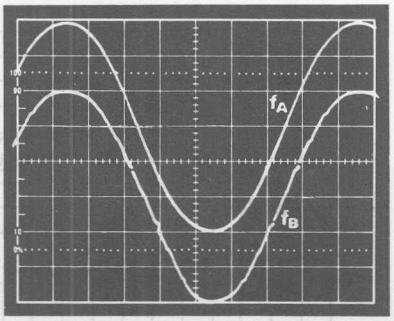


Figure 8. Reconstructed Output of AD770 Decimated by 1:32 @ 200MSPS

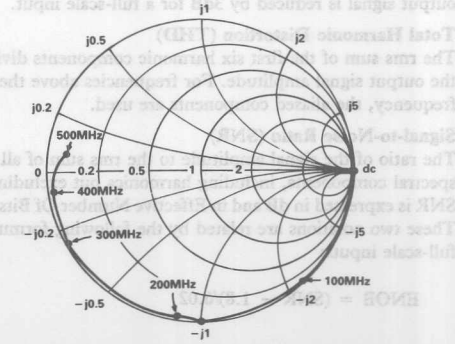


Figure 9. Smith Chart: Input Impedance Normalized to 50Ω vs. Input Frequency

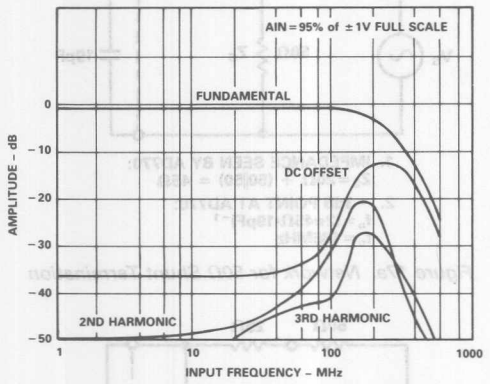


Figure 10. Harmonic Distortion vs. Input Frequency @ 200MSPS: Full Power

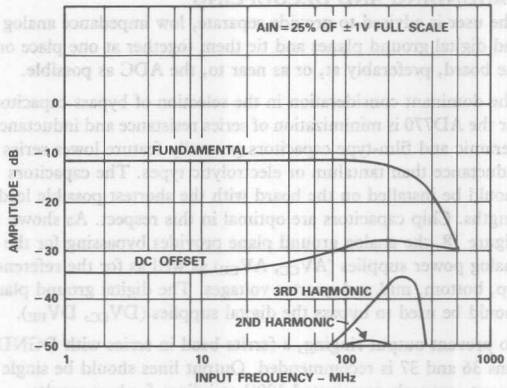


Figure 11. Harmonic Distortion vs. Input Frequency @ 200 MSPS: Small Signal

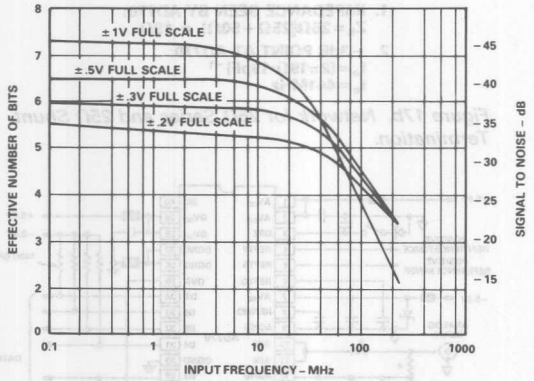


Figure 12. SNR vs. Input Frequency in ENOB and dB

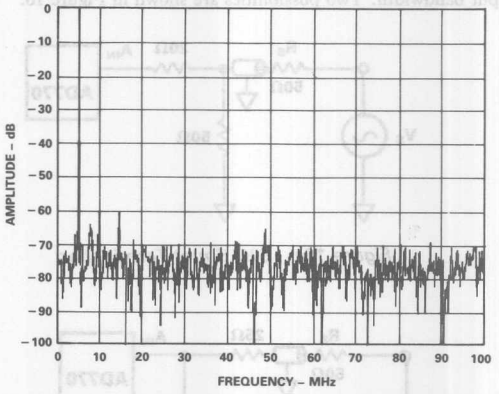


Figure 13. 1024pt FFT of AD770 Output @ 200 MSPS. F_{IN} = 5MHz at ±1V Full Scale

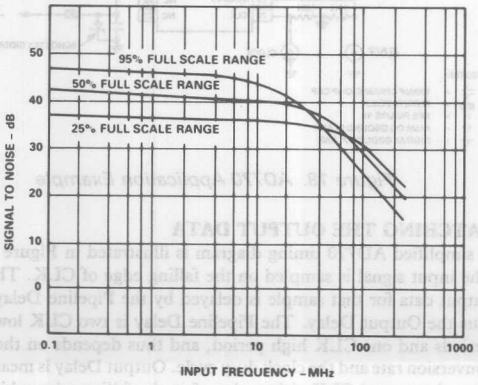


Figure 14. SNR vs. Input Frequency at ±1V F.S. Input

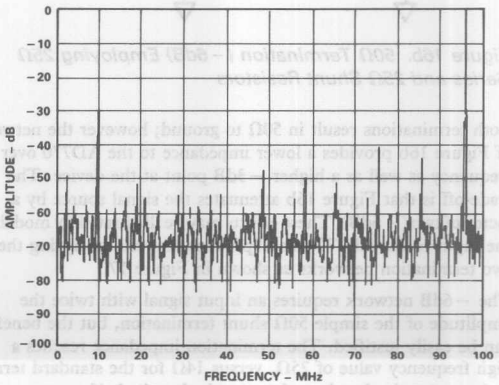


Figure 15. 1024pt FFT of AD770 Output @ 200 MSPS. F_{IN} = 95MHz at ±1V F.S.

The user is advised to provide separate, low impedance analog and digital ground planes and tie them together at one place on the board, preferably at, or as near to, the ADC as possible.

The dominant consideration in the selection of bypass capacitors for the AD770 is minimization of series resistance and inductance. Ceramic and film-type capacitors generally feature lower series inductance than tantalum or electrolytic types. The capacitors should be installed on the board with the shortest possible lead lengths. Chip capacitors are optimal in this respect. As shown in Figure 18, the analog ground plane provides bypassing for the analog power supplies (AV_{CC}, AV_{EE}) as well as for the reference top, bottom, mid and quarter voltages. The digital ground plane should be used to bypass the digital supplies (DV_{CC}, DV_{EE}).

To prevent output ringing, a ferrite bead in series with DGND Pins 36 and 37 is recommended. Output lines should be single fanout, properly terminated 100Ω striplines for best results.

DRIVING THE AD770

The AD770 can be driven directly from most signal sources. The termination of the signal source, however, will affect the input bandwidth. Two possibilities are shown in Figure 16.

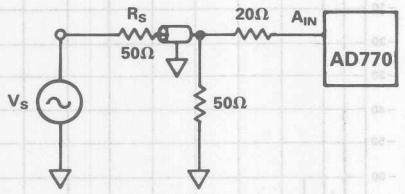


Figure 16a. 50Ω Shunt Termination

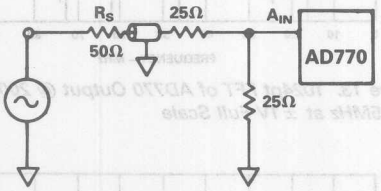
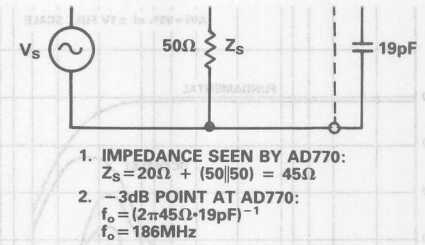


Figure 16b. 50Ω Termination (−6dB) Employing 25Ω Series and 25Ω Shunt Resistors

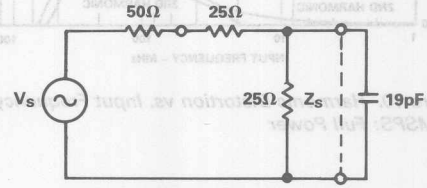
Both terminations result in 50Ω to ground; however the network of Figure 16b provides a lower impedance to the AD770 over frequency as well as a higher −3dB point at the device. The trade-off is that Figure 16b attenuates the signal source by a factor of two (−6dB). These effects may be illustrated by modeling the input to the AD770 as a 19pF capacitor and analyzing the two termination networks as shown in Figure 17.

The −6dB network requires an input signal with twice the amplitude of the simple 50Ω shunt termination, but the benefits can be easily justified. The termination impedance reaches a high frequency value of 25Ω, versus 14Ω for the standard termination network. Another advantage is that the half-power bandwidth is more than twice that of the standard 50Ω shunt network.



1. IMPEDANCE SEEN BY AD770:
   $Z_S = 20\Omega + (50 \| 50) = 45\Omega$
2. −3dB POINT AT AD770:
   $f_o = (2\pi 45\Omega \cdot 19pF)^{-1}$
   $f_o = 186MHz$

Figure 17a. Network for 50Ω Shunt Termination



1. IMPEDANCE SEEN BY AD770:
   $Z_S = 25\Omega \| 25\Omega + 50\Omega) = 19\Omega$
2. −3dB POINT AT AD770:
   $f_o = (2\pi 19\Omega \cdot 19pF)^{-1}$
   $f_o = 441MHz$

Figure 17b. Network for 25Ω Series and 25Ω Shunt Termination.

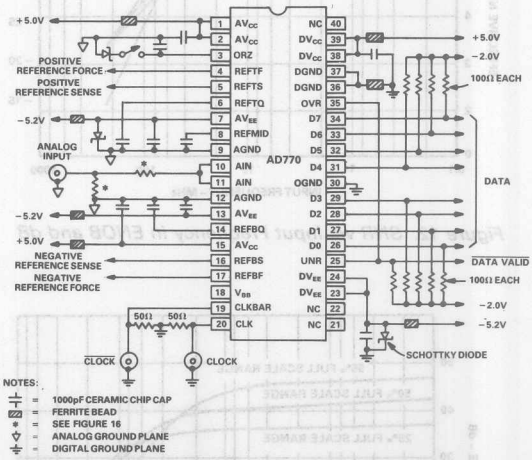


Figure 18. AD770 Application Example

LATCHING THE OUTPUT DATA

A simplified AD770 timing diagram is illustrated in Figure 19. The input signal is sampled on the falling edge of CLK. The output data for that sample is delayed by the Pipeline Delay plus the Output Delay. The Pipeline Delay is two CLK low periods and one CLK high period, and thus depends on the conversion rate and the clock duty cycle. Output Delay is measured from the second CLK rising edge after the falling edge which samples the analog input signal. Output Delay is not dependent on the conversion rate.

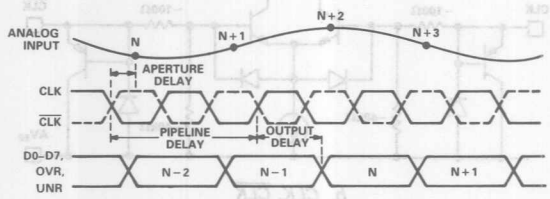


Figure 19. AD770 Timing Diagram

Output Delay varies from unit to unit due to manufacturing process variations. This factor, and the timing requirements of the external latch, must be considered when designing the output clock circuit.

Figure 20 shows a more detailed timing diagram that illustrates the effect of Output Delay variations and external latch timing requirements. Data bit transitions are shown for units at the extreme limits of Output Delay (T_D). For a unit with $T_D = T_{Dmin}$, the data bits will begin to slew after a delay of T_{Dmin}, and all bits will have settled after a further delay of T_{SK} (Output Skew). The data will then be stable until the next output data transition.

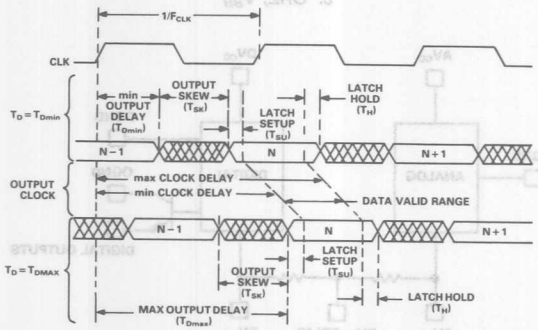


Figure 20. Detailed Timing Diagram Showing Output Delay Variation

However, the Setup and Hold times (T_{SU} and T_H) of the external latch must be subtracted to obtain the interval during which the external latch can be clocked (Data Valid Range). Thus:

$$\text{Data Valid Range} = 1/F_{CLK} - T_{SK} - T_{SU} - T_{TH}$$

The clock circuit will require a maximum delay that can also be easily derived:

$$\text{Max Clock Delay (for } T_D = T_{Dmin}) = 1/F_{CLK} + T_{Dmin} - T_H$$

For a unit with $T_D = T_{Dmax}$, the clock delay will be determined by the Maximum Output Delay (T_{Dmax}):

$$\text{Min Clock Delay (for } T_D = T_{Dmax}) = T_{Dmax} + T_{SU}$$

If the Maximum Clock Delay for $T_D = T_{Dmin}$ is greater than the Minimum Clock Delay for $T_D = T_{Dmax}$, a fixed clock delay set between these two values can be used to latch the output of the AD770.

$$T_{Dmax} + T_{SU} < \text{Fixed Clock Delay} < 1/F_{CLK} + T_{Dmin} - T_H$$

For example, a 120 MSPS system using 100K ECL logic would have the following conditions:

$T_{Dmax} = 6.0\text{ns}$
$T_{SU} = 0.7\text{ns}$
$F_{CLK} = 120\text{MHz}$
$T_{Dmin} = 2.0\text{ns}$
$T_H = 0.7\text{ns}$

$$\text{Max Clock Delay (for } T_D = T_{Dmin}) = 1/F_{CLK} + T_{Dmin} - T_H = 9.6\text{ns}$$

$$\text{Min Clock Delay (for } T_D = T_{Dmax}) = T_{Dmax} + T_{SU} = 6.7\text{ns}$$

A fixed clock delay could thus be used, with the following limits:

$$6.7\text{ns} < \text{Clock Delay} < 9.6\text{ns}$$

As the sample rate increases, the range of fixed clock delays becomes narrower. At 150 MSPS, using the same logic family, the range becomes:

$$6.7\text{ns} < \text{Clock Delay} < 8.0\text{ns}$$

At 200 MSPS, a fixed delay can no longer be used, since

Max Clock Delay (for $T_D = T_{Dmin}$) = 6.3ns
Min Clock Delay (for $T_D = T_{Dmax}$) = 6.7ns

The user should calculate whether a fixed delay can be used in the system. If a fixed delay cannot be used, a variable delay line is needed.

VARIABLE DELAY LINE

Continuing with the example above, we can determine the span of delays that is needed.

At 200 MSPS:

Max Clock Delay (for $T_D = T_{Dmin}$) = 6.3ns
Min Clock Delay (for $T_D = T_{Dmax}$) = 6.7ns
Data Valid Range (for each device) < 1.25ns.

The clock delay should have an adjustment range between (6.3 − 1.25/2) = 5.7ns and (6.7 + 1.25/2) = 7.3ns to center the clock edge in the middle of the Data Valid range for all devices.

If a variable delay line is used, some means must be provided to verify that the delay is correctly set for each device. This can be done by providing a test signal synchronized to the system timing and adjusting the delay to the centerpoint of the range that gives a stable output.

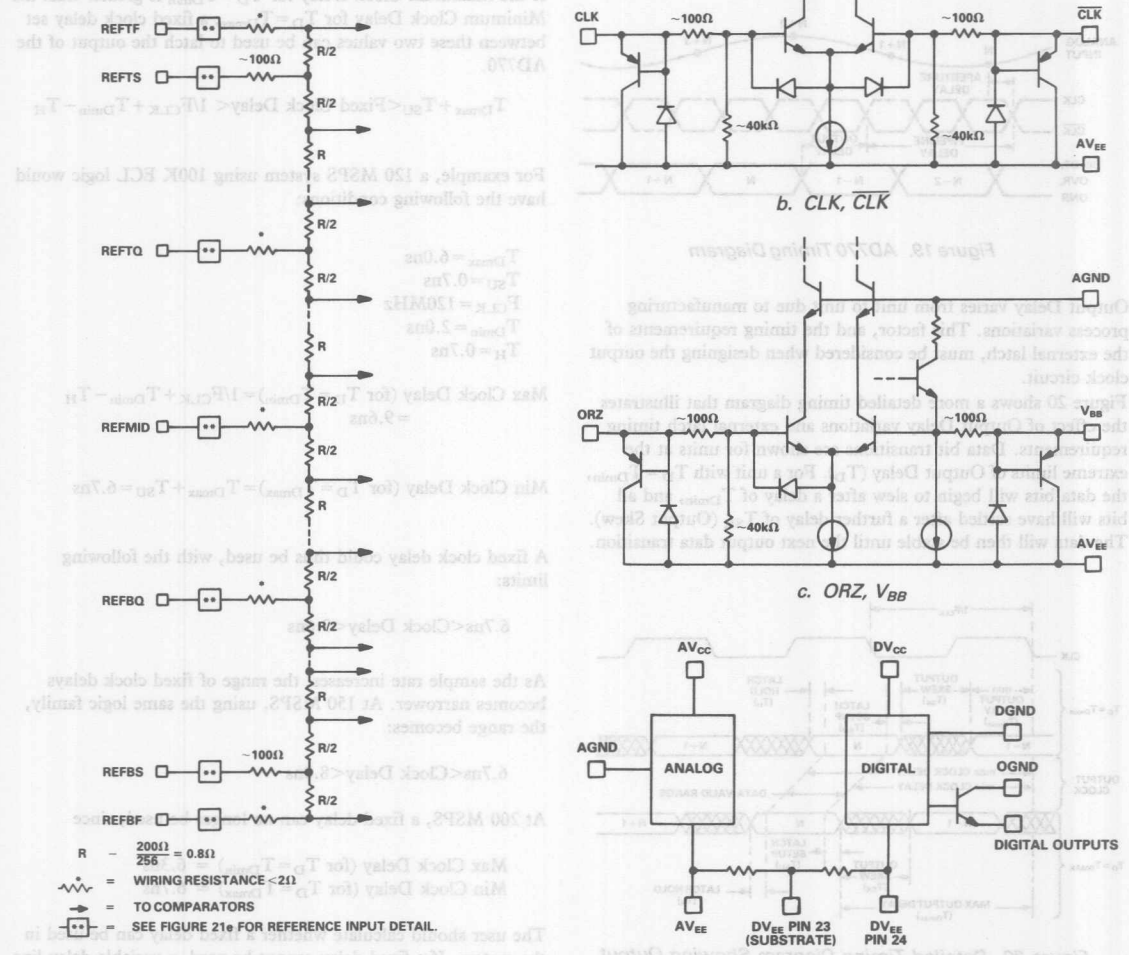


Figure 21. Equivalent Circuits

10-Bit 18 MSPS Monolithic A/D Converter

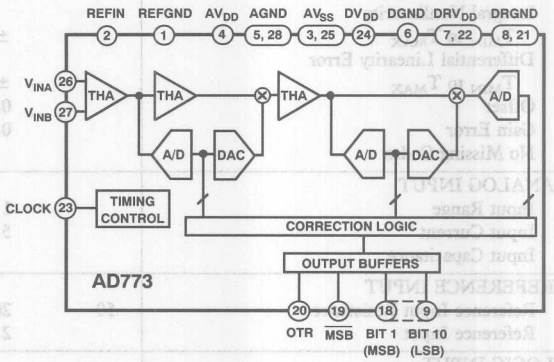
AD773

2

FEATURES

- Monolithic 10-Bit 18 MSPS A/D Converter
- Low Power Dissipation: 1.2 W
- Signal-to-Noise Plus Distortion Ratio
  - f_{IN} = 1 MHz: 55 dB
  - f_{IN} = 8 MHz: 52 dB
- Guaranteed No Missing Codes
- On-Chip Track-and-Hold Amplifier
- 100 MHz Full Power Bandwidth
- High Impedance Reference Input
- Out of Range Output
- Twos Complement and Binary Output Data
- Available in Commercial and Military Temperature Ranges

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD773 is a monolithic 10-bit, 18 MSPS analog-to-digital converter incorporating an on-board, high performance track-and-hold amplifier (THA). The AD773 converts video bandwidth signals without the use of an external THA. The AD773 implements a multistage differential pipelined architecture with output error correction logic. The AD773 offers accurate performance and guarantees no missing codes over the full operating temperature range.

Output data is presented in binary and twos complement format. An out of range (OTR) signal indicates the analog input voltage is beyond the specified input range. OTR can be decoded with the MSB/$\overline{\text{MSB}}$ pins to signal an underflow or overflow condition. The high impedance reference input allows multiple AD773s to be driven in parallel from a single reference.

The combined dc precision and dynamic performance of the AD773 is useful in a variety of applications. Typical applications include: video enhancement, HDTV, ghost cancellation, ultrasound imaging, radar and high speed data acquisition.

The AD773 was designed using Analog Devices' ABCMOS-1 process which utilizes high speed bipolar and 2-micron CMOS transistors on a single chip. High speed, precision analog circuits are now combined with high density logic circuits. Laser trimmed thin film resistors are used to optimize accuracy and temperature stability.

The AD773 is packaged in a 28-pin ceramic DIP and is available in commercial (0°C to +70°C) and military (−55°C to +125°C) grades.

PRODUCT HIGHLIGHTS

1. On-board THA
   The high impedance differential input THA eliminates the need for external buffering or sample and hold amplifiers. The THA offers the choice of differential or single-ended inputs. Input current is typically 5 μA.
2. High Impedance Reference Input
   The high impedance reference input (200 kΩ) allows direct connection with standard +2.5 V references, such as the AD680, AD580 and REF43.
3. Output Data Flexibility
   Output data is available in bipolar offset and bipolar twos complement binary format.
4. Out of Range (OTR)
   The OTR output bit indicates when the input signal is beyond the AD773's input range.

AD773—SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5 V ± 5%, AV_{SS} = −5 V ± 5%, DV_{DD} = +5 V ± 5%, DRV_{DD} = +5 V ± 5%, V_{REF} = +2.500 V unless otherwise indicated)

Parameter	AD773J Min	AD773J Typ	AD773J Max	AD773K Min	AD773K Typ	AD773K Max	Units
RESOLUTION	10			10			Bits
DC ACCURACY (+25°C)							
Integral Nonlinearity							LSB
T_{MIN} to T_{MAX}		±1			±0.75	±2	LSB
Differential Linearity Error							LSB
T_{MIN} to T_{MAX}		±1			±0.75	±1	LSB
Offset		0.5			0.5	3.5	% FSR
Gain Error		0.5			0.5	2.0	% FSR
No Missing Codes					GUARANTEED		
ANALOG INPUT							
Input Range		1			1		V p–p
Input Current		5	20		5	20	µA
Input Capacitance			10			10	pF
REFERENCE INPUT							
Reference Input Resistance	50	200		50	200		kΩ
Reference Input		2.5			2.5		Volts
LOGIC INPUT							
High Level Input Voltage	+3.5			+3.5			V
Low Level Input Voltage			+1.0			+1.0	V
High Level Input Current (V_{IN} = DV_{DD})	−10		+10	−10		+10	µA
Low Level Input Current (V_{IN} = 0 V)	−10		+10	−10		+10	µA
Input Capacitance		10			10		pF
LOGIC OUTPUTS							
High Level Output Voltage (I_{OH} = 0.5 mA)	+2.4			+2.4			V
Low Level Output Voltage (I_{OL} = 1.6 mA)			+0.4			+0.4	V
POWER SUPPLIES							
Operating Voltages							
AV_{DD}	+4.75		+5.25	+4.75		+5.25	Volts
AV_{SS}	−5.25		−4.75	−5.25		−4.75	Volts
DV_{DD}, DRV_{DD}	+4.75		+5.25	+4.75		+5.25	Volts
Operating Current							
IAV_{DD}		85	100		85	100	mA
IAV_{SS}		−140	−185		−140	−185	mA
IDV_{DD}		15	20		15	20	mA
$IDRV_{DD}$[1]		10	15		10	15	mA
POWER CONSUMPTION[2]		1.2	1.5		1.2	1.5	W
POWER SUPPLY REJECTION		6	16		6	16	mV/V
TEMPERATURE RANGE							
Specified (J/K)	0		+70	0		+70	°C

NOTES
[1]C_L = 15 pF typical.
[2]100% production tested.

Specifications subject to change without notice. See Definition of Specifications for additional information.

AC SPECIFICATIONS

(T_{MIN} to T_{MAX} with AV_{DD} = +5 V ± 5%, AV_{SS} = −5 V ± 5%, DV_{DD} = +5 V ± 5%, DRV_{DD} = +5 V ± 5%, V_{REF} = +2.500 V unless otherwise indicated, f_{SAMPLE} = 18 MSPS, f_{IN} amplitude = −0.3 dB)

Parameter	AD773J Min	AD773J Typ	AD773J Max	AD773K Min	AD773K Typ	AD773K Max	Units
DYNAMIC PERFORMANCE[1]							
Signal-to-Noise plus Distortion (S/N+D) Ratio							
f_{IN} = 1 MHz	52	56		54	56		dB
f_{IN} = 8.1 MHz	45	53		47	53		dB
f_{IN} = 9 MHz		53			53		dB
Effective Number of Bits (ENOB)							
f_{IN} = 1 MHz		9.0			9.0		Bits
f_{IN} = 8.1 MHz		8.5			8.5		Bits
f_{IN} = 9 MHz		8.5			8.5		Bits
Total Harmonic Distortion (THD)							
f_{IN} = 1 MHz		−64	−57		−64	−59	dB
f_{IN} = 8.1 MHz		−55	−46		−55	−48	dB
f_{IN} = 9 MHz		−56			−56		dB
Spurious Free Dynamic Range[2]		−67			−67		dB
Full Power Bandwidth		100			100		MHz
Intermodulation Distortion (IMD)[3]							
Second Order Products		−69			−69		dB
Third Order Products		−63			−63		dB
Differential Phase		0.2			0.2		Degree
Differential Gain		0.8			0.8		%
Transient Response		25			25		ns
Overvoltage Recovery Time		25			25		ns

NOTES
[1]For typical dynamic performance curves at f_{SAMPLE} = 16.2 MSPS and 18 MSPS, see Figures 2 through 13.
[2]f_{IN} = 1 MHz.
[3]fa = 1.0 MHz, fb = 1.05 MHz.
Specifications subject to change without notice.

TIMING SPECIFICATIONS

(for all grades T_{MIN} to T_{MAX} with AV_{DD} = +5 V ± 5%, AV_{SS} = −5 V ± 5%, DV_{DD} = +5 V ± 5%, DRV_{DD} = +5 V ± 5%, V_{REF} = +2.500 V unless otherwise indicated, f_{SAMPLE} = 18 MSPS)

	Symbol	Min	Typ	Max	Units
Conversion Rate				18	MSPS
Clock Period	t_{CLK}	55			ns
Clock High	t_{CH}	27			ns
Clock Low	t_{CL}	27			ns
Output Delay	t_{OD}		20		ns
Aperture Delay			7		ns
Aperture Jitter			9	32	ps
Pipeline Delay (Latency)				4	Clock Cycles

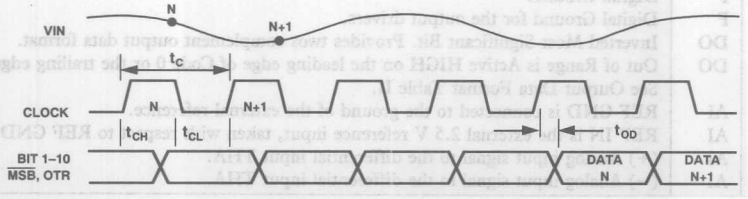


Figure 1. AD773 Timing Diagram

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AV_{DD}	AGND	−0.5	+6.5	V
AV_{SS}	AGND	−6.5	+0.5	V
DV_{DD}, DRV_{DD}	DGND, DRGND	−0.5	+6.5	V
AGND	DGND, DRGND	−1.0	+1.0	V
AV_{DD}, AV_{SS}	DV_{DD}, DRV_{DD}	−6.5	+0.5	V
CLK	DV_{DD}, DRV_{DD}	−6.5	+0.5	V
REFIN	REFGND, AGND	−0.5	+6.5	V
Junction Temperature			+150	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)			+300	°C

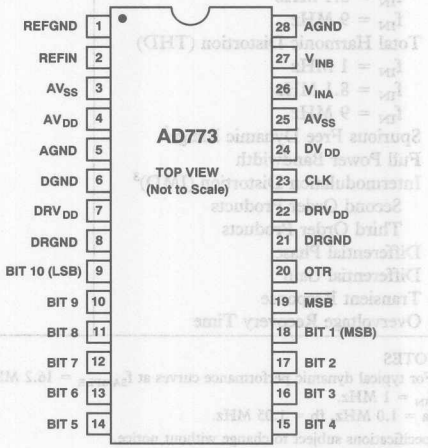
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Description	Package Option*
AD773JD	0°C to +70°C	28-Pin Ceramic DIP	D-28
AD773KD	0°C to +70°C	28-Pin Ceramic DIP	D-28

*D = Ceramic DIP. For outline information see Package Information section.

PIN CONFIGURATION



PIN DESCRIPTION

Symbol	Pin No.	Type	Name and Function
AGND	5, 28	P	Analog Ground.
AV_{DD}	4	P	+5 V Analog Supply.
AV_{SS}	3, 25	P	−5 V Analog Supply.
BIT 1 (MSB)	18	DO	Most Significant Bit.
BIT 2–BIT 9	17–10	DO	Data Bit 2 through Data Bit 9.
BIT 10 (LSB)	9	DO	Least Significant Bit.
CLK	23	DI	Clock Input. The AD773 will initiate a conversion on the falling edge of the clock input. See the Timing Diagram for details.
DV_{DD}	24	P	+5 V Digital Supply.
DRV_{DD}	7, 22	P	+5 V Digital Supply for the output drivers.
DGND	6	P	Digital Ground.
DRGND	8, 21	P	Digital Ground for the output drivers.
$\overline{MSB}$	19	DO	Inverted Most Significant Bit. Provides twos complement output data format.
OTR	20	DO	Out of Range is Active HIGH on the leading edge of Code 0 or the trailing edge of Code 1023. See Output Data Format Table II.
REF GND	1	AI	REF GND is connected to the ground of the external reference.
REF IN	2	AI	REF IN is the external 2.5 V reference input, taken with respect to REF GND.
V_{INA}	26	AI	(+) Analog input signal to the differential input THA.
V_{INB}	27	AI	(−) Analog input signal to the differential input THA.

Type: AI = Analog Input; DI = Digital Input; DO = Digital Output; P = Power.

INTEGRAL NONLINEARITY (INL)
Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale." The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line.

DIFFERENTIAL LINEARITY ERROR (DNL, NO MISSING CODES)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value.

OFFSET
The first transition should occur at a level 1/2 LSB above "zero." Offset is defined as the deviation of the actual first code transition from that point.

GAIN ERROR
The last code transition should occur for an analog value 1 1/2 LSB below the nominal full scale. The gain error is the deviation of the actual level at the last transition from the ideal level.

POWER SUPPLY REJECTION
One of the effects of power supply variation on the performance of the device will be a change in gain error. The specification shows the maximum gain error deviation as the supplies are varied from their nominal values to their specified limits.

SIGNAL-TO-NOISE PLUS DISTORTION (S/N+D) RATIO
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

EFFECTIVE NUMBER OF BITS (ENOB)
ENOB is calculated from the following expression:

S/N+D = 6.02N + 1.76, where N is equal to the effective number of bits.

TOTAL HARMONIC DISTORTION (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

SPURIOUS FREE DYNAMIC RANGE
The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in decibels relative to the rms value of a full-scale input signal.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mfa±nfb, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa+fb) and (fa−fb) and the third order terms are (2fa+fb), (2fa−fb), (fa+2fb) and (fa−2fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals are of equal amplitude and the peak value of their sums is −0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

DIFFERENTIAL GAIN
The percentage difference between the output amplitudes of a small high frequency sine wave at two stated levels of a low frequency signal on which it is superimposed.

DIFFERENTIAL PHASE
The difference in the output phase of a small high frequency sine wave at two stated levels of a low frequency signal on which it is superimposed.

TRANSIENT RESPONSE
The time required for the AD773 to achieve its rated accuracy after a full-scale step function is applied to its input.

OVERVOLTAGE RECOVERY TIME
The time required for the ADC to recover to full accuracy after an analog input signal 150% of full scale is reduced to 50% of the full-scale value.

APERTURE DELAY
The difference between the switch delay and the analog delay of the THA. This effective delay represents the point in time, relative to the rising edge of the CLOCK input, that the analog input is sampled.

APERTURE JITTER
The variations in aperture delay for successive samples.

PIPELINE DELAY (LATENCY)
The number of clock cycles between conversion initiation and the associated output data being made available. New output data is provided every clock cycle.

FULL POWER BANDWIDTH
The input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

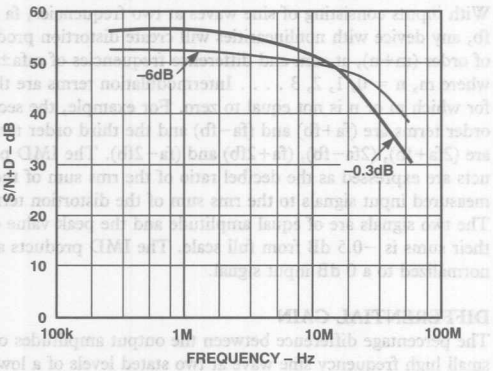


Figure 2. S/N+D vs. Input Frequency, f_{CLK} = 18 MSPS

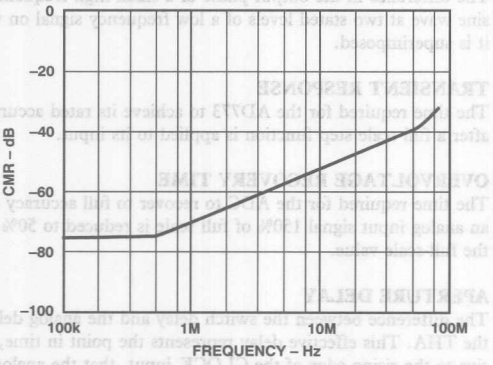


Figure 3. CMR vs. Input Frequency f_{CLK} = 18 MSPS

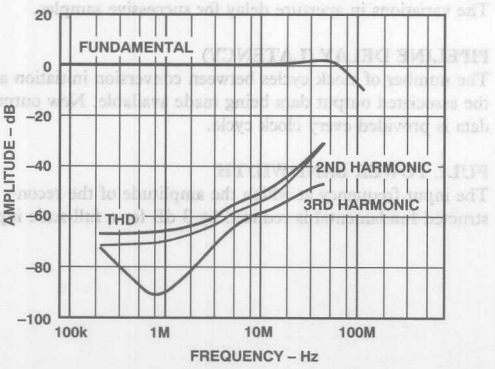


Figure 4. Harmonic Distortion vs. Input Frequency, f_{CLK} = 18 MSPS: Full Power

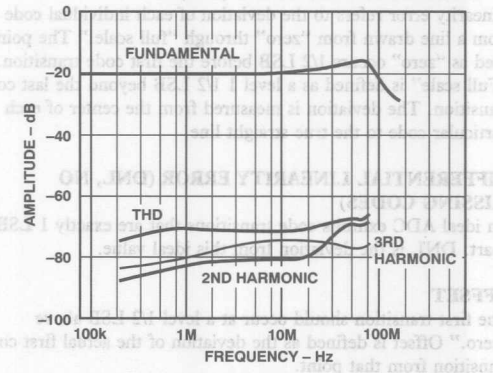


Figure 5. Harmonic Distortion vs. Input Frequency, f_{CLK} = 18 MSPS: Small Signal

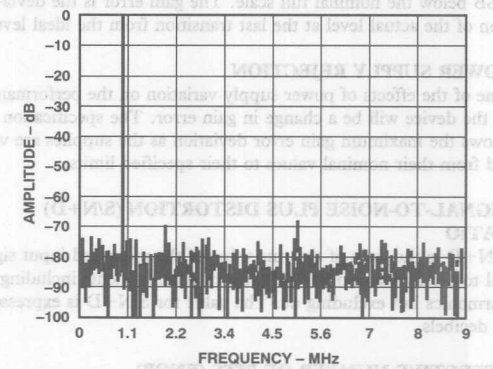


Figure 6. Typical FFT Plot of AD773, f_{CLK} = 18 MSPS, f_{IN} = 1 MHz at 1 V p–p

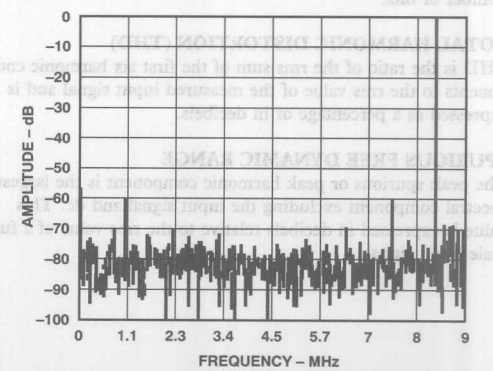


Figure 7. Typical FFT Plot of AD773, f_{CLK} = 18 MSPS, f_{IN} = 8.5 MHz at 1 V p–p

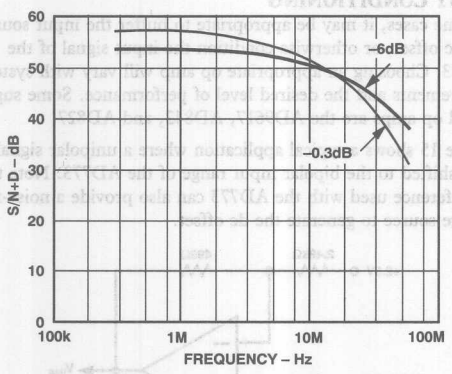


Figure 8. S/N+D vs. Input Frequency, f_{CLK} = 16.2 MSPS

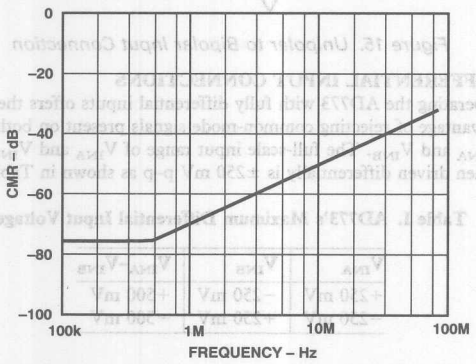


Figure 9. CMR vs. Input Frequency, f_{CLK} = 16.2 MSPS

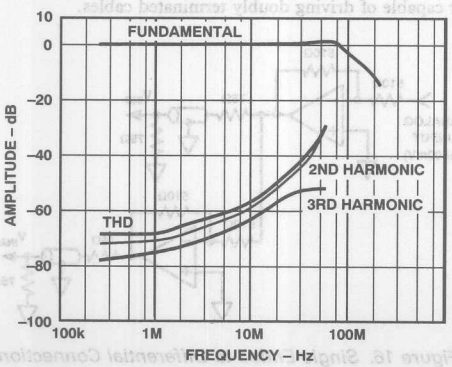


Figure 10. Harmonic Distortion vs. Input Frequency, f_{CLK} = 16.2 MSPS: Full Power

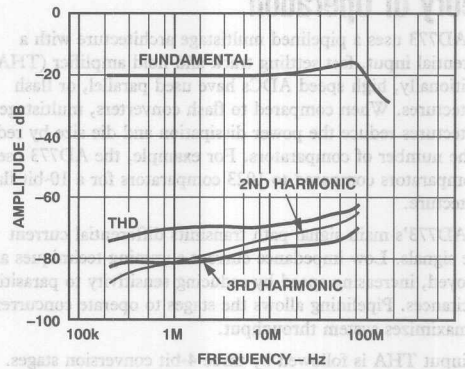


Figure 11. Harmonic Distortion vs. Input Frequency, f_{CLK} = 16.2 MSPS: Small Signal

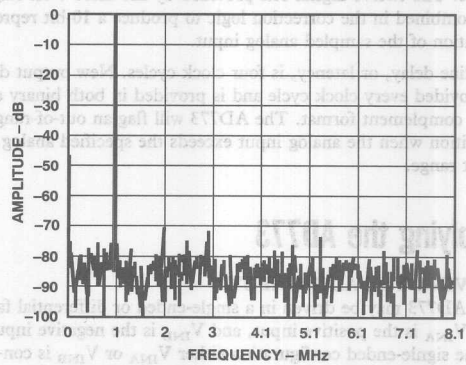


Figure 12. Typical FFT Plot of AD773, f_{CLK} = 16.2 MHz, f_{IN} = 1 MHz at 1 V p–p

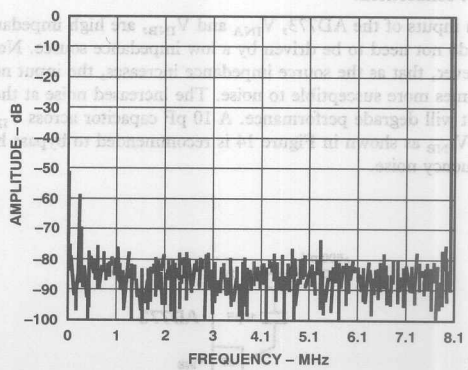


Figure 13. Typical FFT Plot of AD773, f_{CLK} = 16.2 MHz, f_{IN} = 8.05 MHz at 1 V p–p

Theory of Operation

The AD773 uses a pipelined multistage architecture with a differential input, fast settling track-and-hold amplifier (THA). Traditionally, high speed ADCs have used parallel, or flash architectures. When compared to flash converters, multistage architectures reduce the power dissipation and die size by reducing the number of comparators. For example, the AD773 uses 48 comparators compared to 1023 comparators for a 10-bit flash architecture.

The AD773's main signal path transmits differential current mode signals. Low impedance current summing techniques are employed, increasing speed by reducing sensitivity to parasitic capacitances. Pipelining allows the stages to operate concurrently and maximizes system throughput.

The input THA is followed by three 4-bit conversion stages. At any given time, the first stage operates on the most recent sample, while the second stage operates on a signal dependent on the previous sample. This process continues throughout all three stages. The twelve digital bits provided by the three 4-bit stages are combined in the correction logic to produce a 10-bit representation of the sampled analog input.

Pipeline delay, or latency, is four clock cycles. New output data is provided every clock cycle and is provided in both binary and twos complement format. The AD773 will flag an out-of-range condition when the analog input exceeds the specified analog input range.

Applying the AD773

DRIVING THE AD773 INPUT

The AD773 may be driven in a single-ended or differential fashion. V_{INA} is the positive input, and V_{INB} is the negative input. In the signle-ended configuration either V_{INA} or V_{INB} is connected to Analog Ground (AGND) while the other input is driven with a full-scale input of ±500 mV p–p. An inverted mode of operation can be achieved by simply interchanging the input connections.

Both inputs of the AD773, V_{INA} and V_{INB}, are high impedance and do not need to be driven by a low impedance source. Note, however, that as the source impedance increases, the input node becomes more susceptible to noise. The increased noise at the input will degrade performance. A 10 pF capacitor across V_{INA} and V_{INB} as shown in Figure 14 is recommended to bypass high frequency noise.

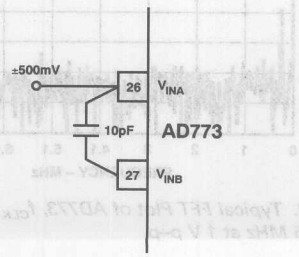


Figure 14. AD773 Single-Ended Input Connection

INPUT CONDITIONING

In some cases, it may be appropriate to buffer the input source, add dc offset, or otherwise condition the input signal of the AD773. Choosing an appropriate op amp will vary with system requirements and the desired level of performance. Some suggested op amps are the AD9617, AD842, and AD827.

Figure 15 shows a typical application where a unipolar signal is level shifted to the bipolar input range of the AD773. Note that the reference used with the AD773 can also provide a noise-free voltage source to generate the dc offset.

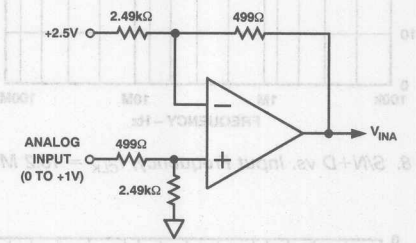


Figure 15. Unipolar to Bipolar Input Connection

DIFFERENTIAL INPUT CONNECTIONS

Operating the AD773 with fully differential inputs offers the advantage of rejecting common-mode signals present on both V_{INA} and V_{INB}. The full-scale input range of V_{INA} and V_{INB} when driven differentially is ±250 mV p–p as shown in Table I.

Table I. AD773's Maximum Differential Input Voltage

V_{INA}	V_{INB}	V_{INA}–V_{INB}
+250 mV	−250 mV	+500 mV
−250 mV	+250 mV	−500 mV

In some applications it may be desirable to convert a single-ended signal to a differential signal before being applied to the AD773. Figure 16 shows a single-ended to differential video line driver capable of driving doubly terminated cables.

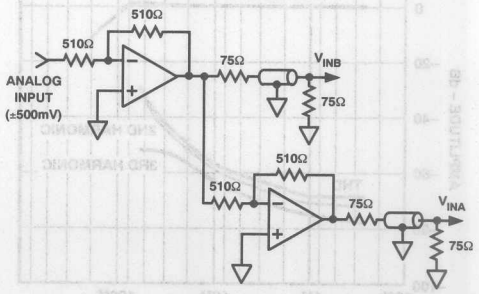


Figure 16. Single-Ended to Differential Connection

REFERENCE INPUT

The AD773's high impedance reference input allows direct connection with standard voltage references. Unlike the resistor ladder requirements of a flash converter the AD773's single pin, high impedance input can be driven from one low cost, low power reference. The high impedance input allows multiple AD773's to be driven from one reference thus minimizing drift errors.

Figure 17 shows the AD773 connected to the AD680. The AD680 is a single supply, low power, low cost 2.5 V reference with performance specifications ideally suited for the AD773. The low pass filter minimizes the AD680's wideband noise. Other recommended 2.5 V references are the AD580 and REF43.

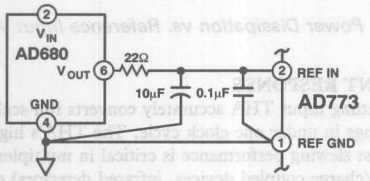


Figure 17. Recommended AD773 to AD680 Connection

CLOCK INPUT

The AD773's pipelined architecture operates on both the rising and falling edges of the clock input. A low jitter, symmetrical clock will provide the highest level of performance. The recommended logic families to drive the clock input are HC and F. The AD773's minimum clock half cycle may necessitate the use of an external divide-by-two circuit as shown in Figure 18. Power dissipation will vary with input clock frequency. Figure 19 shows the AD773's power dissipation vs. input clock frequency.

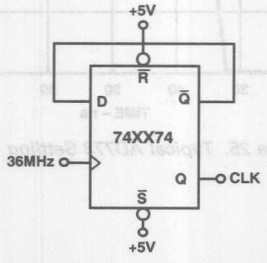


Figure 18. Divide-by-Two Clock Circuit

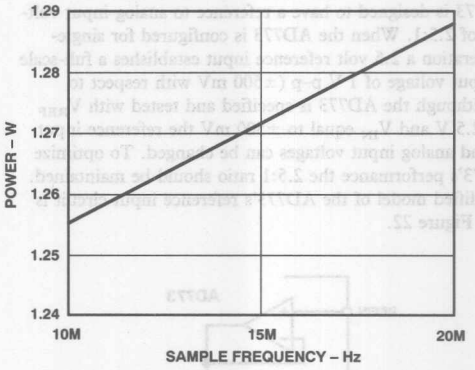


Figure 19. Power Dissipation vs. Sample Frequency

EQUIVALENT ANALOG INPUT CIRCUIT

The AD773 equivalent analog input circuit is shown in Figure 20. The typical input bias current is 5 µA, while input capacitance is typically 5 pF. In the single-ended input configuration one input is connected to AGND while the second input is driven to full scale (±500 mV). Under nominal conditions the collector of the input transistor is at +1.15 V. This allows signals to be offset by up to +0.65 V without significantly degrading performance. In the negative direction, the emitter of the input transistor should not drop below −1.25 V. Therefore, signals can be offset by −0.65 V without significant performance degradation. Figure 21 shows signal-to-noise ratio vs. common-mode input voltage.

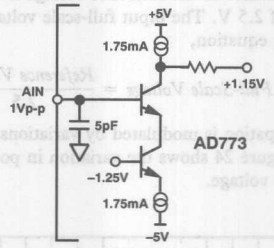


Figure 20. Equivalent Analog Input Circuit

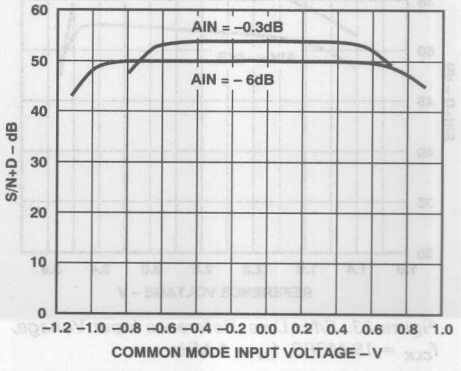


Figure 21. S/N+D vs. Common-Mode Input Voltage, f_{CLK} = 18 MSPS

EQUIVALENT REFERENCE INPUT CIRCUIT

The AD773 is designed to have a reference to analog input voltage ratio of 2.5:1. When the AD773 is configured for single-ended operation a 2.5 volt reference input establishes a full-scale analog input voltage of 1 V p–p (±500 mV with respect to V_{INB}). Although the AD773 is specified and tested with V_{REF} equal to 2.5 V and V_{IN} equal to ±500 mV the reference input voltage and analog input voltages can be changed. To optimize the AD773's performance the 2.5:1 ratio should be maintained. The simplified model of the AD773's reference input circuit is shown in Figure 22.

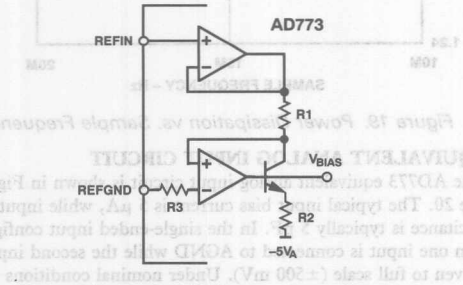


Figure 22. Typical Reference Input Circuit

The 2.5 V external reference is applied across resistor R1 producing a current which in turn generates a voltage V_{BIAS}. Multiple reference currents are generated from V_{BIAS} and are used throughout the converter. R3 is used to cancel errors induced by the input bias current of the REFGND buffer. Figure 23 shows the SNR performance as the reference voltage is varied from its nominal value of 2.5 V. The input full-scale voltage is defined by the following equation,

$$\textit{Input Full-Scale Voltage} = \frac{\textit{Reference Voltage}}{2.5}$$

The power dissipation is modulated by variations in the reference voltage. Figure 24 shows the variation in power dissipation versus reference voltage.

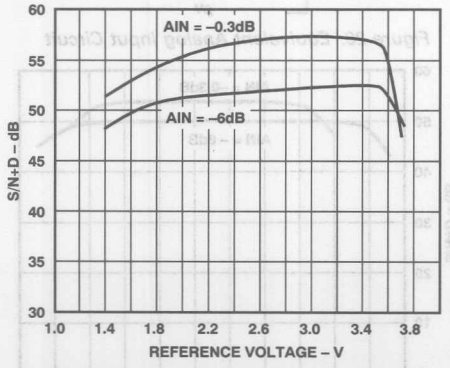


Figure 23. S/N+D vs. Reference Input Voltage, f_{CLK} = 18 MSPS, f_{IN} = 1 MHz

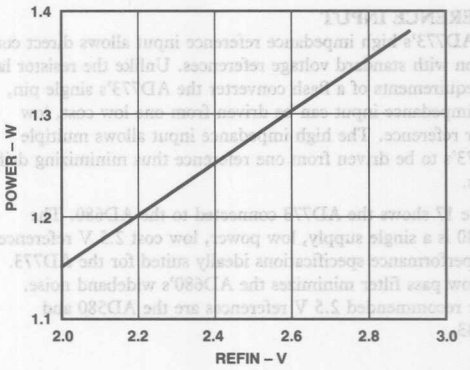


Figure 24. Power Dissipation vs. Reference Input Voltage

TRANSIENT RESPONSE

The fast settling input THA accurately converts full-scale input voltage swings in under one clock cycle. The THA's high impedance, fast slewing performance is critical in multiplexed or dc stepped (charge coupled devices, infrared detectors) systems. Figure 25 show the AD773's settling performance with an input signal stepped from −500 mV to 0V. As can be seen, the output code settles to its final value in under one clock cycle.

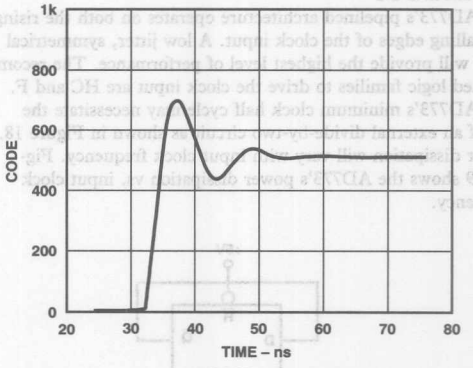


Figure 25. Typical AD773 Settling Time

OUTPUT DATA FORMAT

The AD773 provides both MSB and $\overline{MSB}$ outputs, delivering positive true offset binary and twos complement output data. Table II shows the AD773's output data format.

Table II. Output Data Format

Analog Input	Digital Output		
V_{INA}–V_{INB}	Offset Binary	Twos Complement	OTR
≥499.5 mV	11 1111 1111	01 1111 1111	1
499 mV	11 1111 1111	01 1111 1111	0
0 mV	10 0000 0000	00 0000 0000	0
−500 mV	00 0000 0000	10 0000 0000	0
≤−500.5 mV	00 0000 0000	10 0000 0000	1

OUT OF RANGE

An out-of-range condition exists when the analog input voltage is beyond the input range (±500 mV) of the converter. [Note the AD773 has a 4 clock cycle latency rating.] OTR (Pin 20) is set low when the analog input voltage is within the analog input range. OTR is set HIGH and will remain HIGH when the analog input voltage exceeds the input range by 1/2 LSB from the center of the ± full-scale output codes. OTR will remain HIGH until the analog input is within the input range. By logical ANDing OTR with the MSB and its complement, overrange high or underrange low conditions can be detected. Table III is a truth table for the over/under range circuit in Figure 26. Systems requiring programmable gain conditioning prior to the AD773 can immediately detect an out of range condition, thus eliminating gain selection iterations.

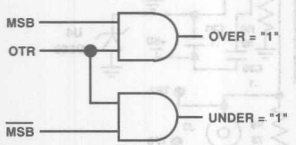


Figure 26. Overrange or Underrange Logic

Table III. Out-of-Range Truth Table

OTR	MSB	ANALOG INPUT IS
0	0	In Range
0	1	In Range
1	0	Underrange
1	1	Overrange

GROUNDING AND LAYOUT RULES

As is the case for any high performance device, proper grounding and layout techniques are essential in achieving optimal performance. The analog and digital grounds on the AD773 have been separated to optimize the management of return currents in a system. It is recommended that a 4-layer printed circuit board (PCB) which employs ground planes and power planes be used with the AD773. The use of ground and power planes offers distinct advantages:

1. The minimization of the loop area encompassed by a signal and its return path.
2. The minimization of the impedance associated with ground and power paths.
3. The inherent distributed capacitor formed by the power plane, PCB insulation, and ground plane.

These characteristics result in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout which prevents noise from coupling onto the input signal. The wide input bandwidth of the AD773 permits noise outside the desired Nyquist bandwidth to be digitized along with the desired signal. This can result in a higher overall level of spurious noise in the digitized spectrum. Digital signals should not be run in parallel with the input signal traces and should be routed away from the input circuitry. It is also suggested that the traces associated with V_{INA} and V_{INB} be the same length.

Separate analog and digital ground should be joined together directly under the AD773 (see Figure 30). A solid ground plane under the AD773 is also acceptable if care is taken in the management of the power and ground return currents. A general "rule-of-thumb" for mixed signal layouts dictate that the return currents from digital circuitry should not pass through critical analog circuitry.

POWER SUPPLY DECOUPLING

The analog and digital supplies of the AD773 have been separated to prevent the typically large transients associated with digital circuitry from coupling into the analog supplies (AV_{DD}, AV_{SS}). Each power supply pin should be decoupled with a 0.1 μF capacitor located as close to the pin as possible. Additional 0.1 μF capacitors in parallel with the DRV_{DD} and DDV_{DD} bypass capacitors are required to adequately suppress high capacitors are recommended. The inductance associated with the leads of through-hole ceramic capacitors typically render them ineffective at higher frequencies. A *complete* system will also incorporate tantalum capacitors in the 10–100 μF range to decouple low frequency noise and ferrite beads to limit high frequency noise.

The digital supplies have additionally been separated into DRV_{DD} and DV_{DD}. The DRV_{DD} pins provide power for the digital output drivers of the AD773 and are likely to contain high energy transients. Pin 22 should be decoupled directly to Pin 21 (DRGND) and Pin 7 should be decoupled directly to Pin 8 (DRGND) to minimize the length of the return path for these transients. A single +5 V supply is all that is required for DRV_{DD} and DV_{DD}, but decoupling DV_{DD} with an RC filter network is suggested (see Figure 27).

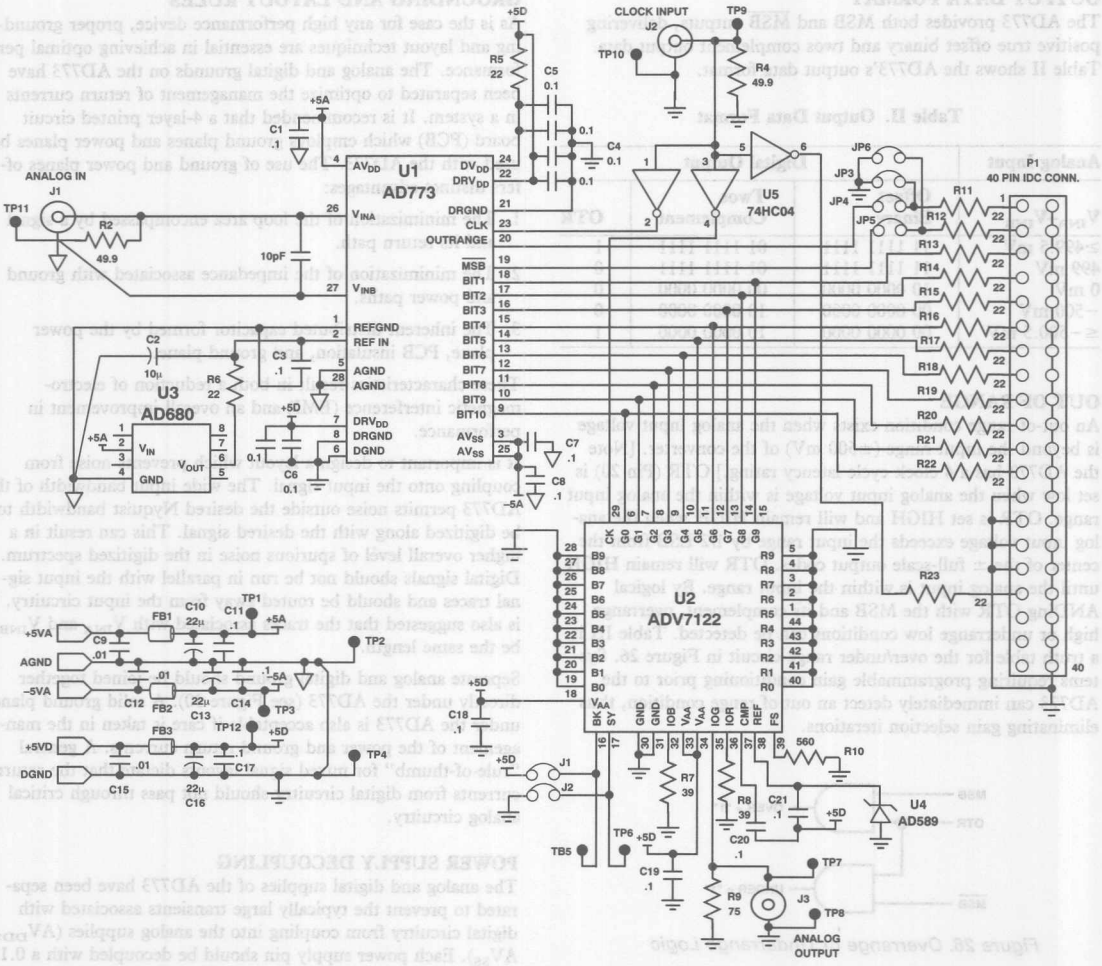


Figure 27. AD773 Evaluation Board Schematic

Table IV. Components List

Reference Designator	Description	Quantity
R2, R4	Resistor, 1%, 49.9 Ω	2
R5, R6, R11–R22	Resistor, 5%, 22 Ω	14
R7, R8	Resistor, 5%, 39 Ω	2
R9	Resistor, 5%, 75 Ω	1
R10	Resistor, 5%, 560 Ω	1
C1, C3–C8, C11, C14, C17–C21	Chip Cap, 0.1 µF	14
C2	Capacitor, Tantalum, 10 µF	1
C9, C12, C15	Chip Cap, 0.01 µF	3
C10, C13, C16	Capacitor, Tantalum, 22 µF	3
U1	AD773	1
U2	ADV7122	1
U3	AD680	1
U4	AD589	1
U5	74AS04	1
FB1–FB3	Ferrite Bead	3

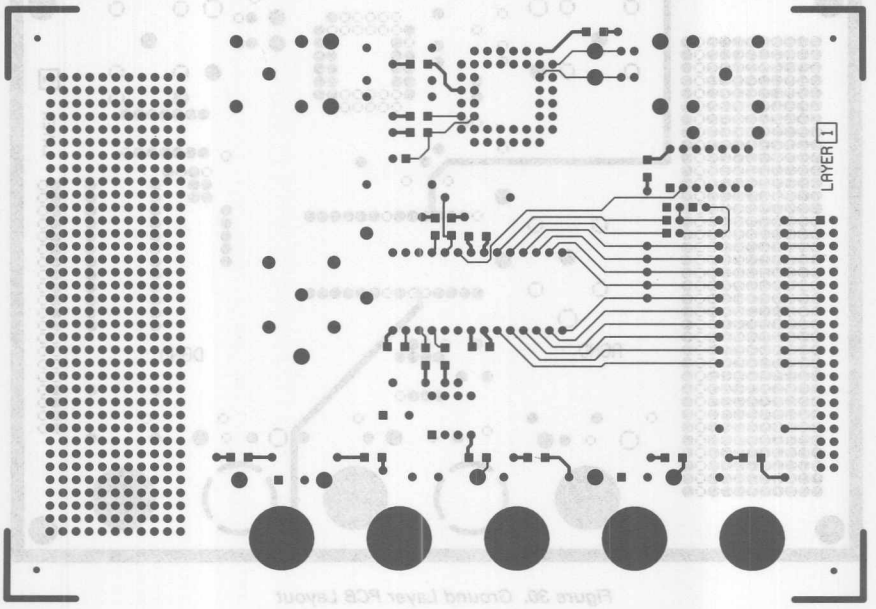


Figure 28. Component Side PCB Layout

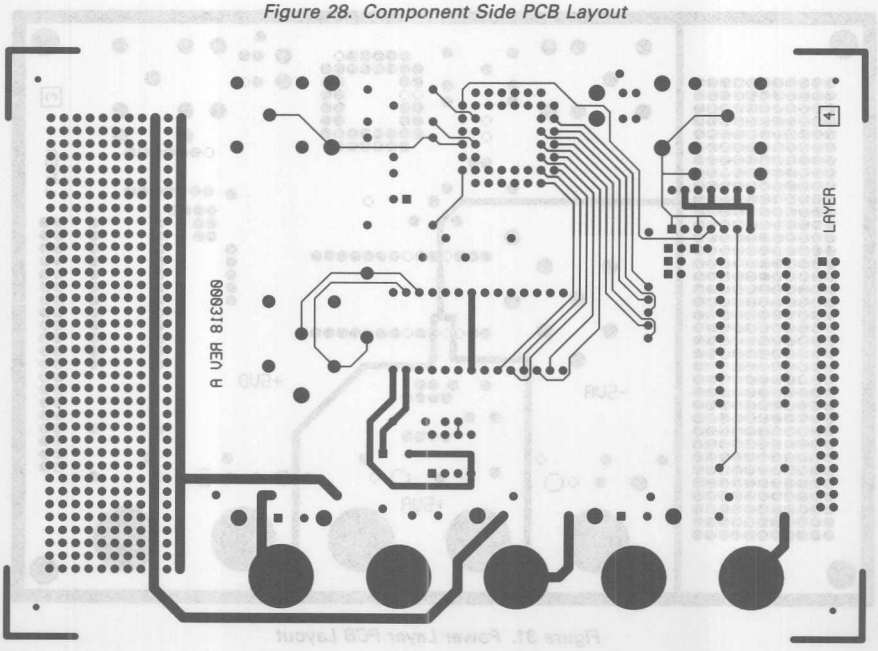


Figure 29. Solder Side PCB Layout

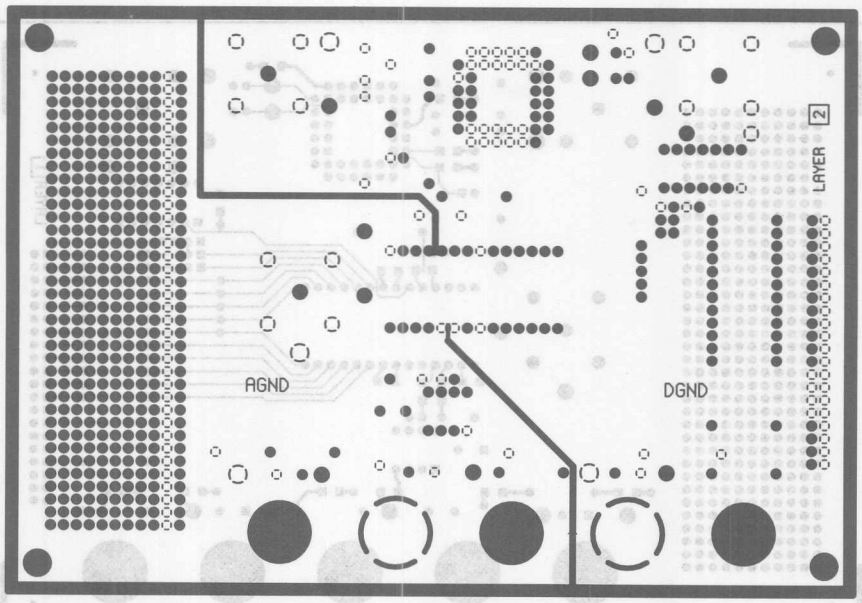


Figure 30. Ground Layer PCB Layout

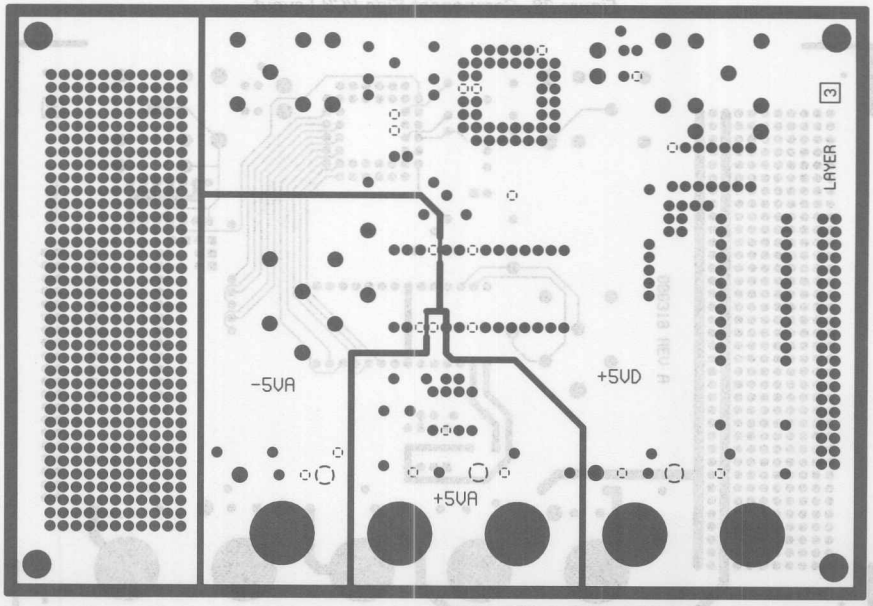


Figure 31. Power Layer PCB Layout

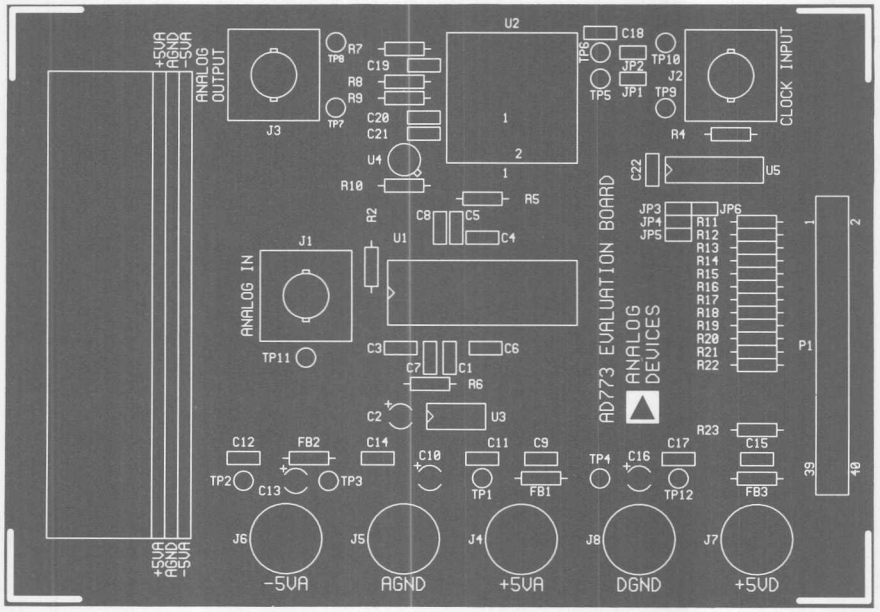
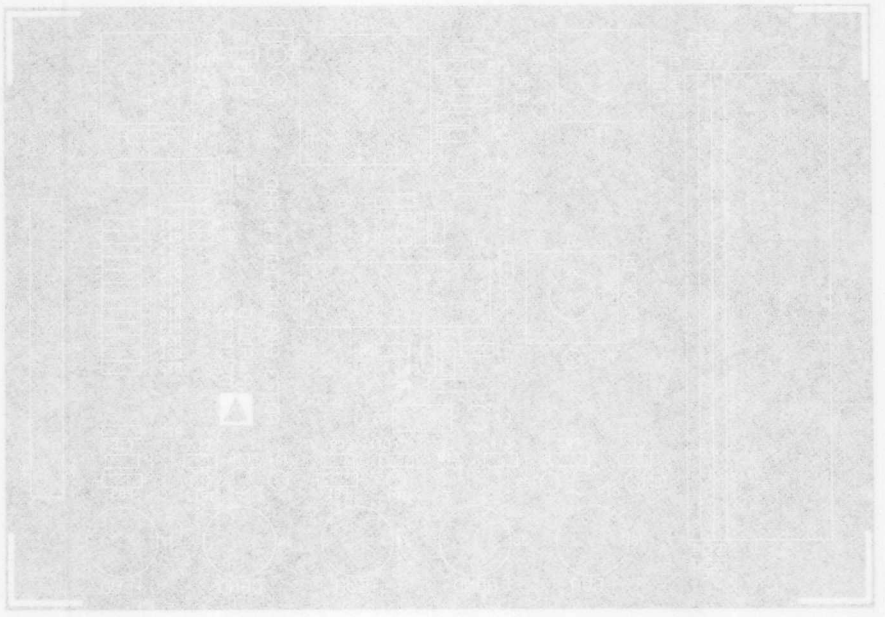


Figure 32. Silkscreen Layer PCB Layout

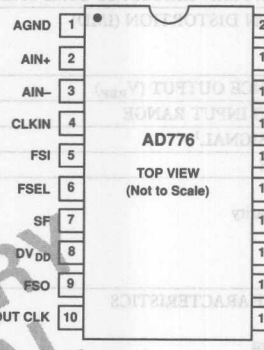


16-Bit 100 kSPS Oversampling ADC

AD776

FEATURES
Monolithic 16-Bit ADC
Third-Order Noise Shaping
96 dB Dynamic Range
90 dB S/(N+D)
16-Bit 100 kHz Output from FIR Filter
12-Bit 400 kHz Output from Comb Filter
No Missing Codes
<0.001 dB In-Band Ripple

PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD776 is a 16-bit sigma-delta oversampled ADC, incorporating a 1-bit noise shaping modulator and third order digital decimating filter. An on-chip voltage reference circuit is also included.

The AD776 does not require the use of sample-hold circuits or antialiasing filters as a result of its sigma-delta architecture. The output is available both before and after the final Finite Impulse Response (FIR) decimation filter. This provides the flexibility of optimizing conversion speed or resolution: 12-bit/400 kHz (from the Comb filter) or 16-bit/100 kHz (from the FIR filter). The AD776 may be used with an input multiplexer at a minimum output sampling period of 15 μs in the Comb filter output mode.

The AD776 is specified for ac (or "dynamic") parameters such as S/N+D Ratio, THD and IMD which are important in signal processing and audio applications.

The AD776 operates from a single +5 V supply and typically consumes 350 mW during conversion.

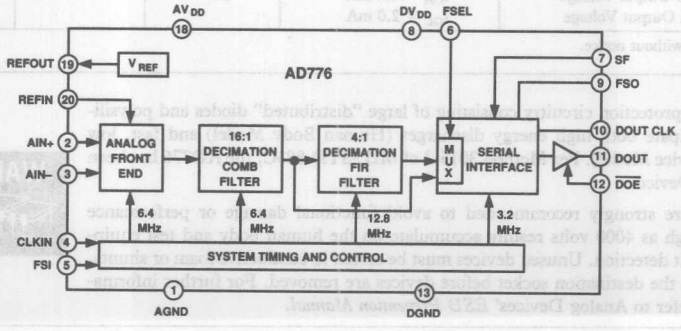
The AD776 is available in a 20-pin ceramic DIP (cerdip) or 20-pin plastic DIP package.

PRODUCT HIGHLIGHTS

1. Linear phase analog front end
2. Fully differential inputs
3. Serial Output Directly Compatible with a variety of processors
4. No sample-hold circuits or antialias filter required
5. 6.4 MHz maximum input sample rate
6. 12.8 MHz maximum internal clock rate

PRELIMINARY TECHNICAL DATA

FUNCTIONAL BLOCK DIAGRAM



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

RESOLUTION	16			Bits
TEMPERATURE RANGE	−40		+85	°C
TOTAL HARMONIC DISTORTION (THD)		−94	−90	dB
		0.002	0.003	%
SIGNAL-TO-NOISE DISTORTION RATIO (S/(N+D))				
45.5 kHz Bandwidth	85	90		dB
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−100	−92	dB
INTERMODULATION DISTORTION (IMD)				
2nd Order Products		−102		dB
3rd Order Products		−98		dB
VOLTAGE REFERENCE OUTPUT (V_{REF})		2		V
MAXIMUM ANALOG INPUT RANGE	0		$2 \times V_{REF}$	V
MAXIMUM INPUT SIGNAL[1]			$\pm 0.5\ V_{REF}$	V
INPUT IMPEDANCE		TBD		Ω
DC ACCURACY				
Differential Nonlinearity			±0.5	LSB
INL		TBD		LSB
Gain Error		TBD		%
Midscale Error		TBD		%
DIGITAL FILTER CHARACTERISTICS				
Passband Ripple			0.001	dB
Stopband Attenuation	TBD			dB
POWER SUPPLY REQUIREMENTS[2]				
Analog Supply Voltage (AV_{DD})	4.5	5.0	5.5	V
Digital Supply Voltage (DV_{DD})	4.5		AV_{DD}	V
Analog Supply Current		TBD		mA
Digital Supply Current		TBD		mA
Power Consumption		350	400	mW
Power Supply Rejection[3]		70		dB

NOTES
[1]The input signal may be centered at any choice of dc offset voltage as long as peak values are bounded by the Maximum Analog Input Range value.
[2]The AD776 may be operated from a single +5 V supply.
[3]with external voltage reference.

PRELIMINARY TECHNICAL DATA

DIGITAL SPECIFICATIONS

Parameter		Test Conditions	Min	Typ	Max	Units
LOGIC INPUTS						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		−0.5		0.8	V
I_{IH}	High Level Input Current	$V_{IH} = V_{DD}$	−10		+10	μA
I_{IL}	Low Level Input Current	$V_{IL} = 0$ V	−10		+10	μA
I_{LC}	Input Leakage Current				1.0	μA
C_{IN}	Input Capacitance				10	pF
I_Z	Hi-Z Input Current for SDO				10	μA
LOGIC OUTPUTS						
V_{OH}	High Level Output Voltage	$I_{OH} = 0.4$ mA	2.4			V
V_{OL}	Low Level Output Voltage	$I_{OL} = 2.0$ mA			0.5	V

Specifications subject to change without notice.

CAUTION

The AD776 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD776 has been classified as a Category 1 Device.



Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment, and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam discharged to the destination socket before devices are removed. For further information on ESD precaution, refer to Analog Devices' *ESD Prevention Manual*.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

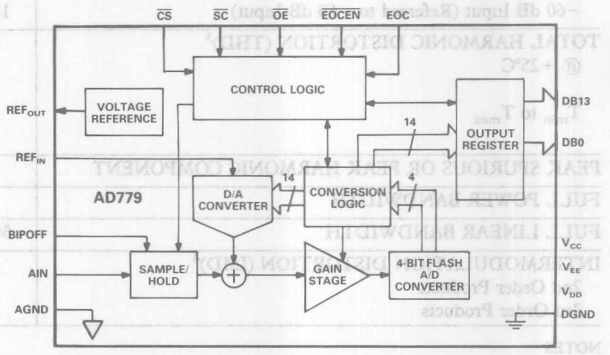
14-Bit 128 kSPS Complete Sampling ADC

AD779*

FEATURES

- AC and DC Characterized and Specified (K, B, T Grades)
- 128k Conversions per Second
- 1 MHz Full Power Bandwidth
- 500 kHz Full Linear Bandwidth
- 80 dB S/N+D (K, B, T Grades)
- Twos Complement Data Format (Bipolar Mode)
- Straight Binary Data Format (Unipolar Mode)
- 10 MΩ Input Impedance
- 16-Bit Bus Interface (See AD679 for 8-Bit Interface)
- On-Board Reference and Clock
- 10 V Unipolar or Bipolar Input Range
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD779 is a complete, multipurpose 14-bit monolithic analog-to-digital converter, consisting of a sample-hold amplifier (SHA), a microprocessor compatible bus interface, a voltage reference and clock generation circuitry.

The AD779 is specified for ac (or "dynamic") parameters such as S/N+D ratio, THD and IMD which are important in signal processing applications. In addition, the AD779K, B and T grades are fully specified for dc parameters which are important in measurement applications.

The 14 data bits are accessed by a 16-bit bus in a single read operation. Data format is straight binary for unipolar mode and twos complement binary for bipolar mode. The input has a full-scale range of 10 V with a full power bandwidth of 1 MHz and a full linear bandwidth of 500 kHz. High input impedance (10 MΩ) allows direct connection to unbuffered sources without signal degradation.

This product is fabricated on Analog Devices' BiMOS process, combining low power CMOS logic with high precision, low noise bipolar circuits; laser-trimmed thin-film resistors provide high accuracy. The converter utilizes a recursive subranging algorithm which includes error correction and flash converter circuitry to achieve high speed and resolution.

The AD779 operates from +5 V and ±12 V supplies and dissipates 560 mW (typ). Twenty-eight-pin plastic DIP, ceramic DIP, and 44-J-leaded ceramic surface mount packages are available.

***Protected by U.S. Patent Numbers 4,804,960; 4,814,767; 4,833,345; 4,250,445; 4,808,908; RE30,586.**

PRODUCT HIGHLIGHTS

1. COMPLETE INTEGRATION: The AD779 minimizes external component requirements by combining a high speed sample-hold amplifier (SHA), ADC, 5 V reference, clock and digital interface on a single chip. This provides a fully specified sampling A/D function unattainable with discrete designs.
2. SPECIFICATIONS: The AD779K, B and T grades provide fully specified and tested ac and dc parameters. The AD779J, A and S grades are specified and tested for ac parameters; dc accuracy specifications are shown as typicals. DC specifications (such as INL, gain and offset) are important in control and measurement applications. AC specifications (such as S/N+D ratio, THD and IMD) are of value in signal processing applications.
3. EASE OF USE: The pinout is designed for easy board layout, and the single cycle read output provides compatibility with 16-bit buses. Factory trimming eliminates the need for calibration modes or external trimming to achieve rated performance.
4. RELIABILITY: The AD779 utilizes Analog Devices' monolithic BiMOS technology. This ensures long term reliability compared to multichip and hybrid designs.
5. The AD779 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD779/883B data sheet for detailed specifications.

AD779—SPECIFICATIONS

AC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%, f_{SAMPLE} = 128 kSPS, f_{IN} = 10.009 kHz unless otherwise noted)[1]

Parameter	AD779J/A/S Min	AD779J/A/S Typ	AD779J/A/S Max	AD779K/B/T Min	AD779K/B/T Typ	AD779K/B/T Max	Units
SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO[2]							
−0.5 dB Input (Referred to −0 dB Input)	78	79		80	81		dB
−20 dB Input (Referred to −20 dB Input)	58	59		60	61		dB
−60 dB Input (Referred to −60 dB Input)	18	19		20	21		dB
TOTAL HARMONIC DISTORTION (THD)[3]							
@ +25°C		−90	−84		−90	−84	dB
		0.003	0.006		0.003	0.006	%
T_{min} to T_{max}		−88	−82		−88	−82	dB
		0.004	0.008		0.004	0.008	%
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−90	−84		−90	−84	dB
FULL POWER BANDWIDTH		1			1		MHz
FULL LINEAR BANDWIDTH	500			500			kHz
INTERMODULATION DISTORTION (IMD)[4]							
2nd Order Products		−90	−84		−90	−84	dB
3rd Order Products		−90	−84		−90	−84	dB

NOTES

[1] f_{IN} amplitude = −0.5 dB (9.44 V p-p) bipolar mode full scale unless otherwise indicated. All measurements referred to a −0 dB (9.997 V p-p) input signal unless otherwise noted.

[2] See Figure 15 for higher frequencies and other input amplitudes.

[3] See Figures 13 and 14 for higher frequencies and other input amplitudes.

[4] f_A = 9.08 kHz, f_B = 9.58 kHz, with f_{SAMPLE} = 128 kSPS. See Definition of Specifications section.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (All device types T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter		Test Conditions	Min	Max	Units
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		2.0	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	0.8	V
I_{IH}	High Level Input Current	V_{IN} = V_{DD}	−10	+10	μA
I_{IL}	Low Level Input Current	V_{IN} = 0 V	−10	+10	μA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	4.0		V
		I_{OH} = 0.5 mA	2.4		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		0.4	V
I_{OZ}	High Z Leakage Current	V_{IN} = V_{DD}	−10	+10	μA
C_{OZ}	High Z Output Capacitance			10	pF

NOTES

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at T_{min}, +25°C and T_{max}. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

DC SPECIFICATIONS

(T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10% unless otherwise indicated)

Parameter	AD779J/A/S Min	AD779J/A/S Typ	AD779J/A/S Max	AD779K/B/T Min	AD779K/B/T Typ	AD779K/B/T Max	Units
TEMPERATURE RANGE							
J, K Grades	0		+70	0		+70	°C
A, B Grades	−40		+85	−40		+85	°C
S, T Grades	−55		+125	−55		+125	°C
ACCURACY							
Resolution	**14**			**14**			Bits
Integral Nonlinearity (INL)		±2			±1	**±2**	LSB
Differential Nonlinearity (DNL)	**14**			**14**			Bits
Unipolar Zero Error[1] (@ +25°C)		0.08			0.05	**0.07**	% FSR*
Bipolar Zero Error[1] (@ +25°C)		0.08			0.05	**0.07**	% FSR
Gain Error[1, 2] (@ +25°C)		0.12			0.09	**0.11**	% FSR
Temperature Drift							
Unipolar Zero[3]							
J, K Grades		0.04			0.04	**0.05**	% FSR
A, B Grades		0.05			0.05	**0.07**	% FSR
S, T Grades		0.09			0.09	**0.10**	% FSR
Bipolar Zero[3]							
J, K Grades		0.02			0.02	**0.04**	% FSR
A, B Grades		0.04			0.04	**0.06**	% FSR
S, T Grades		0.08			0.08	**0.09**	% FSR
Gain[3]							
J, K Grades		0.09			0.09	**0.11**	% FSR
A, B Grades		0.10			0.10	**0.16**	% FSR
S, T Grades		0.20			0.20	**0.25**	% FSR
Gain[4]							
J, K Grades		0.04			0.04	**0.05**	% FSR
A, B Grades		0.05			0.05	**0.07**	% FSR
S, T Grades		0.09			0.09	**0.10**	% FSR
ANALOG INPUT							
Input Ranges							
Unipolar Mode	**0**		**+10**	**0**		**+10**	V
Bipolar Mode	**−5**		**+5**	**−5**		**+5**	V
Input Resistance		10			10		MΩ
Input Capacitance		10			10		pF
Input Settling Time			1.5			1.5	μs
Aperture Delay		10			10		ns
Aperture Jitter		150			150		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage[5]	**4.98**		**5.02**	**4.98**		**5.02**	V
External Load							
Unipolar Mode			**+1.5**			**+1.5**	mA
Bipolar Mode			**+0.5**			**+0.5**	mA
POWER SUPPLIES							
Power Supply Rejection							
V_{CC} = +12 V ± 5%		±6				**±6**	LSB
V_{EE} = −12 V ± 5%		±6				**±6**	LSB
V_{DD} = +5 V ± 10%		±6				**±6**	LSB
Operating Current							
I_{CC}		18	**20**		18	**20**	mA
I_{EE}		25	**34**		25	**34**	mA
I_{DD}		8	**12**		8	**12**	mA
Power Consumption		560	745		560	745	mW

NOTES
[1]Adjustable to zero. See Figures 5 and 6.
[2]Includes internal voltage reference error.
[3]Includes internal voltage reference drift.
[4]Excludes internal voltage reference drift.
[5]With maximum external load applied.
*% FSR = percent of full-scale range.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at T_{min}, +25°C and T_{max}. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

TIMING SPECIFICATIONS (All device types T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)

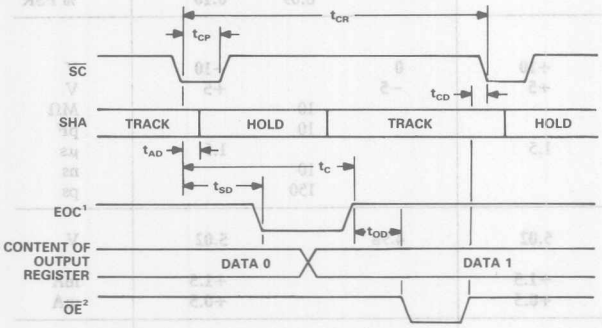
Parameter	Symbol	Min	Max	Units
Conversion Rate[1]	t_{CR}		7.8	µs
Convert Pulse Width	t_{CP}	97		ns
Aperture Delay	t_{AD}	5	20	ns
Conversion Time	t_C		6.3	µs
Status Delay	t_{SD}	0	400	ns
Access Time[2, 3]	t_{BA}	10	100	ns
		10	57[4]	ns
Float Delay[5]	t_{FD}	10	80	ns
Output Delay	t_{OD}		0	ns
$\overline{OE}$ Delay	t_{OE}	20		ns
Read Pulse Width	t_{RP}	100		ns
Conversion Delay	t_{CD}	400		ns

NOTES
[1]Includes Acquisition Time.
[2]Measured from the falling edge of $\overline{OE}/\overline{EOCEN}$ (0.8 V) to the time at which the data lines/EOC cross 2.0 V or 0.8 V. See Figure 4.
[3]C_{OUT} = 100 pF.
[4]C_{OUT} = 50 pF.
[5]Measured from the rising edge of $\overline{OE}/\overline{EOCEN}$ (2.0 V) to the time at which the output voltage changes by 0.5 V. See Figure 4; C_{OUT} = 10 pF.

Specifications shown in **boldface** are tested at final electrical test with worst case supply voltages at T_{min}, +25°C, and T_{max}. Results from those tests are used to calculate outgoing quality levels.

All min and max specifications are guaranteed although only those in boldface are tested.

Specifications subject to change without notice.



NOTES
[1]$\overline{EOCEN}$ = LOW.
[2]DATA SHOULD NOT BE ENABLED DURING A CONVERSION.

Figure 1. Conversion Timing

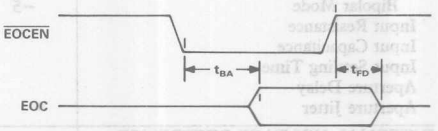


Figure 3. EOC Timing

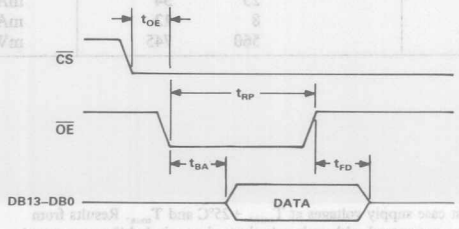


Figure 2. Output Timing

TEST	V_{CP}	C_{OUT}
ACCESS TIME HIGH Z TO LOGIC LOW	5 V	100 pF
FLOAT TIME LOGIC HIGH TO HIGH Z	0 V	10 pF
ACCESS TIME HIGH Z TO LOGIC HIGH	0 V	100 pF
FLOAT TIME LOGIC LOW TO HIGH Z	5 V	10 pF

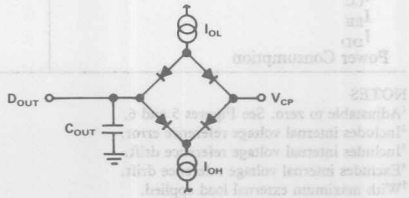


Figure 4. Load Circuit for Bus Timing Specifications

ABSOLUTE MAXIMUM RATINGS*

Specification	With Respect To	Min	Max	Units
V_{CC}	AGND	−0.3	+18	V
V_{EE}	AGND	−18	+0.3	V
V_{CC}	V_{EE}	−0.3	+26.4	V
V_{DD}	DGND	0	+7	V
AGND	DGND	−1	+1	V
AIN, REF_{IN}	AGND	V_{EE}	V_{CC}	V
Digital Inputs	DGND	−0.5	+7	V
Digital Outputs	DGND	−0.5	V_{DD} +0.3	V
Max Junction Temperature			175	°C
Operating Temperature				
J and K Grades		0	+70	°C
A and B Grades		−40	+85	°C
S and T Grades		−55	+125	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec max)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

ESD SENSITIVITY

The AD779 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD779 has been classified as a Category 1 device.



Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.

ORDERING GUIDE[1]

Model[2]	Package	Temperature Range	Tested and Specified	Package Option[3]
AD779JN	28-Pin Plastic DIP	0 to +70°C	AC	N-28A
AD779KN	28-Pin Plastic DIP	0 to +70°C	AC + DC	N-28A
AD779JD	28-Pin Ceramic DIP	0 to +70°C	AC	D-28A
AD779KD	28-Pin Ceramic DIP	0 to +70°C	AC + DC	D-28A
AD779AD	28-Pin Ceramic DIP	−40°C to +85°C	AC	D-28A
AD779BD	28-Pin Ceramic DIP	−40°C to +85°C	AC + DC	D-28A
AD779AJ	44-Lead Ceramic JLCC	−40°C to +85°C	AC	J-44
AD779BJ	44-Lead Ceramic JLCC	−40°C to +85°C	AC + DC	J-44
AD779SD	28-Pin Ceramic DIP	−55°C to +125°C	AC	D-28A
AD779TD	28-Pin Ceramic DIP	−55°C to +125°C	AC + DC	D-28A
AD779SJ	44-Lead Ceramic JLCC	−55°C to +125°C	AC	J-44
AD779TJ	44-Lead Ceramic JLCC	−55°C to +125°C	AC + DC	J-44

NOTES
[1]For two cycle read (8+16 bits) interface to 8-bit buses, see AD679.
[2]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD779/883B data sheet.
[3]D = Ceramic DIP; J = J-Leaded Ceramic; N = Plastic DIP. For outline information see Package Information section.

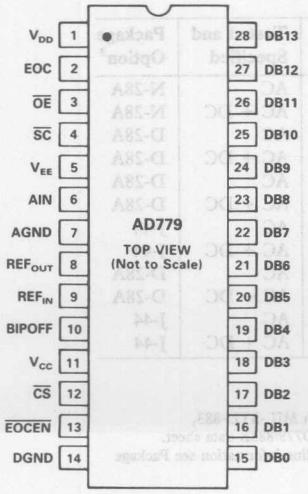
AD779 PIN DESCRIPTION

Symbol	28-Pin DIP Pin No.	44-Lead JLCC Pin No.	Type	Name and Function
AGND	7	11	P	Analog Ground. This is the ground return for AIN only.
AIN	6	10	AI	Analog Signal Input.
BIPOFF	10	15	AI	Bipolar Offset. Connect to AGND for +10 V input unipolar mode and straight binary output coding. Connect to REF_{OUT} for ±5 V input bipolar mode and twos-complement binary output coding.
$\overline{CS}$	12	19	DI	Chip Select. Active LOW.
DGND	14	23	P	Digital Ground
DB13–DB0	28–15	43, 42, 40, 39, 37, 36, 35, 34, 33, 31, 30, 27, 26, 25	DO	Data Bits. These pins provide all 14 bits in one 14 bit parallel output. Active HIGH
EOC	2	3	DO	End-of-Convert. EOC goes LOW when a conversion starts and goes HIGH when the conversion is finished. EOC is a three-state output. See $\overline{EOCEN}$ pin for information on EOC gating.
$\overline{EOCEN}$	13	21	DI	End-of-Convert Enable. Enables EOC pin. Active LOW.
$\overline{OE}$	3	5	DI	Output Enable. A down-going transition on $\overline{OE}$ enables data bits. Active LOW.
REF_{IN}	9	14	AI	Reference Input. +5 V input gives 10 V full scale range.
REF_{OUT}	8	12	AO	+5 V Reference Output. Tied to REF_{IN} for normal operation.
$\overline{SC}$	4	6	DI	Start Convert. Active LOW.
V_{CC}	11	17	P	+12 V Analog Power.
V_{EE}	5	8	P	−12 V Analog Power.
V_{DD}	1	1	P	+5 V Digital Power.

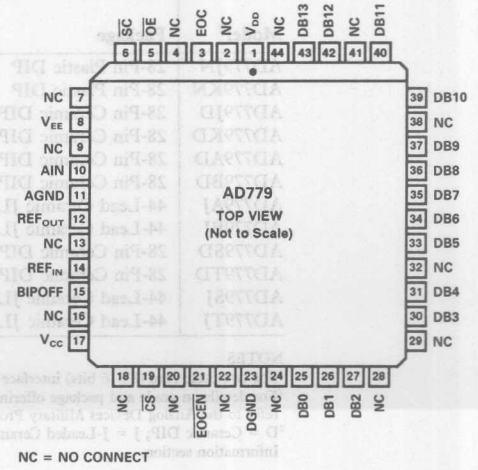
Type: AI = Analog Input.
AO = Analog Output.
DI = Digital Input.
DO = Digital Output. All DO pins are three-state drivers.
P = Power.

PIN CONFIGURATIONS

DIP Package



JLCC Package



NC = NO CONNECT

NYQUIST FREQUENCY
An implication of the Nyquist sampling theorem, the "Nyquist Frequency" of a converter is that input frequency which is one-half the sampling frequency of the converter.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

TOTAL HARMONIC DISTORTION (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of a full-scale input signal and is expressed as a percentage or in decibels. For input signals or harmonics that are above the Nyquist frequency, the aliased component is used.

PEAK SPURIOUS OR PEAK HARMONIC COMPONENT
The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in decibels relative to the rms value of a full-scale input signal.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb) and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (fa − 2 fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude and the peak value of their sum is −0.5 dB from full scale (9.44 V p–p). The IMD products are normalized to a 0-dB input signal.

BANDWIDTH
The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

The full-linear bandwidth is the input frequency at which the slew rate limit of the sample-hold-amplifier (SHA) is reached. At this point, the amplitude of the reconstructed fundamental has degraded by less than −0.1 dB. Beyond this frequency, distortion of the sampled input signal increases significantly.

The AD779 has been designed to optimize input bandwidth, allowing it to undersample input signals with frequencies significantly above the converter's Nyquist frequency.

APERTURE DELAY
Aperture delay is a measure of the SHA's performance and is measured from the falling edge of Start Convert ($\overline{SC}$) to when the input signal is held for conversion.

APERTURE JITTER
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

INPUT SETTLING TIME
Settling time is a function of the SHA's ability to track fast slewing signals. This is specified as the maximum time required in track mode after a full-scale step input to guarantee rated conversion accuracy.

DIFFERENTIAL NONLINEARITY (DNL)
In an ideal ADC, code transitions are 1 LSB apart. Differential linearity is the deviation from this ideal value. It is often specified in terms of resolution for which no missing codes (NMC) are guaranteed.

INTEGRAL NONLINEARITY (INL)
The ideal transfer function for a linear ADC is a straight line drawn between "zero" and "full scale." The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition. Integral nonlinearity error is the worst case deviation of a code from the straight line. The deviation of each code is measured from the middle of that code.

Note that the linearity error is not user adjustable.

POWER SUPPLY REJECTION
Variations in power supply will affect the full-scale transition, but not the converter's linearity. Power Supply Rejection is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

TEMPERATURE DRIFT
This is the maximum change in the parameter from the initial value (@+25°C) to the value at T_{min} or T_{max}.

UNIPOLAR ZERO ERROR
In unipolar mode, the first transition should occur at a level 1/2 LSB above analog ground. Unipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

BIPOLAR ZERO ERROR
In the bipolar mode, the major carry transition (11 1111 1111 1111 to 00 0000 0000 0000) should occur at an analog value 1/2 LSB below analog ground. Bipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

GAIN ERROR
The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale (9.9991 volts for a 0–10 V range, 4.9991 volts for a ±5 V range). The gain error is the deviation of the actual level at the last transition from the ideal level with the zero error trimmed out. This error can be adjusted as shown in the Input Connections and Calibration section.

bringing $\overline{SC}$ LOW, regardless of the state of $\overline{CS}$.

After a conversion is started, the sample-hold goes into hold mode and EOC goes LOW, signifying that a conversion is in progress. During the conversion, the sample-hold will go back into track mode and start acquiring the next sample.

In track mode, the sample-hold will settle to ±0.003% (14 bits) in 1.5 μs maximum. The acquisition time does not affect the throughput rate as the AD779 goes back into track mode more than 2 μs before the next conversion. In multichannel systems, the input channel can be switched as soon as EOC goes LOW if the maximum throughput rate is needed.

When EOC goes HIGH, the conversion is completed and the output data may be read. Bringing $\overline{OE}$ LOW makes the output register contents available on the output data bits (DB13–DB0). A period of time t_{CD} is required after $\overline{OE}$ is brought HIGH before the next $\overline{SC}$ instruction is issued.

If $\overline{SC}$ is held LOW, conversion accuracy may deteriorate. For this reason, $\overline{SC}$ should not be held low in any attempt to operate in a continuously converting mode.

END-OF-CONVERT

End-of-Convert (EOC) is a three-state output which is enabled by End-of-Convert Enable $\overline{EOCEN}$.

CONVERSION TRUTH TABLE

	INPUTS				OUTPUTS	
Mode	$\overline{SC}$	$\overline{EOCEN}$	$\overline{CS}$	$\overline{OE}$	EOC DB13 . . . DB0	Status
Start Conversion	1	X	X	X		No Conversion
	↓	X	X	X		Start Conversion
	0	X	X	X		Continuous Conversion (Not Recommended)
Conversion Status	X	0	X	X	0	Converting
	X	0	X	X	1	Not Converting
	X	1	X	X	High Z	Either
Data Access	X	X	X	1	High Z	Three-State
	X	X	1	X	High Z	Three-State
	X	X	0	0	MSB . . . LSB	Data Out

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
↓ = HIGH to LOW transition. Must stay LOW for $t = t_{CP}$.

be LOW t_{OE} before $\overline{OE}$ is brought LOW. The output is read in a single cycle as a 14-bit word.

In unipolar mode (BIPOFF tied to AGND), the output coding is straight binary. In bipolar mode (BIPOFF tied to REF_{OUT}), output coding is twos complement binary.

POWER-UP

The AD779 typically requires 10 μs after power-up to reset internal logic.

14-BIT MODE CODING FORMAT (1 LSB = 0.61 mV)

Unipolar Coding (Straight Binary)		Bipolar Coding (Twos Complement)	
V_{IN}	Output Code	V_{IN}	Output Code
0.00000 V	000 . . . 0	−5.00000 V	100 . . . 0
5.00000 V	100 . . . 0	−0.00061 V	111 . . . 1
9.99939 V	111 . . . 1	0.00000 V	000 . . . 0
		+2.50000 V	010 . . . 0
		+4.99939 V	011 . . . 1

INPUT CONNECTIONS AND CALIBRATION

The high (10 MΩ) input impedance of the AD779 eases the task of interfacing to high source impedances or multiplexer channel-to-channel mismatches of up to 300 Ω. The 10 V p-p full scale input range accepts the majority of signal voltages without the need for voltage divider networks which could deteriorate the accuracy of the ADC.

The AD779 is factory trimmed to minimize offset, gain and linearity errors. In unipolar mode, the only external component that is required is a 50 Ω ±1% resistor. Two resistors are required in bipolar mode. If offset and gain are not critical, even these components can be eliminated.

In some applications, offset and gain errors need to be more precisely trimmed. The following sections describe the correct procedure for these various situations.

BIPOLAR RANGE INPUTS

The connections for the bipolar mode are shown in Figure 5. In this mode, data output coding will be twos complement binary. This circuit will allow approximately ±25 mV of offset trim range (±40 LSB) and ±0.5% of gain trim range (±80 LSB).

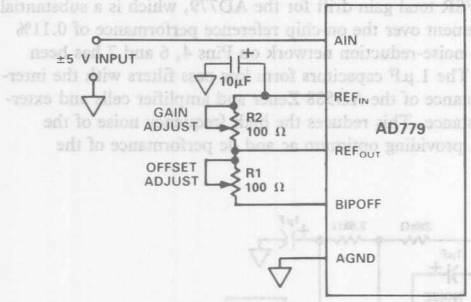


Figure 5. Bipolar Input Connections with Gain and Offset Trims

Either or both of the trim pots can be replaced with 50 Ω ±1% fixed resistors if the AD779 accuracy limits are sufficient for the application. If the pins are shorted together, the additional offset and gain errors will be approximately 80 LSB.

To trim bipolar zero to its nominal value, apply a signal 1/2 LSB below midrange (−0.305 mV for a ±5 V range) and adjust R1 until the major carry transition is located (11 1111 1111 1111 to 00 0000 0000 0000). To trim the gain, apply a signal 1 1/2 LSB below full scale (+4.9991 V for a ±5 V range) and adjust R2 to give the last positive transition (01 1111 1111 1110 to 01 1111 1111 1111). These trims are interactive so several iterations may be necessary for convergence.

A single pass calibration can be done by substituting a bipolar offset trim (error at minus full scale) for the bipolar zero trim (error at midscale), using the same circuit. First, apply a signal 1/2 LSB above minus full scale (−4.9997 V for a ±5 V range) and adjust R1 until the minus full scale transition is located (10 0000 0000 0000 to 10 000 000 0001). Then perform the gain error trim as outlined above.

UNIPOLAR RANGE INPUTS

Offset and gain errors can be trimmed out by using the configuration shown in Figure 6. This circuit allows approximately ±25 mV of offset trim range (±40 LSB) and ±0.5% of gain trim range (±80 LSB).

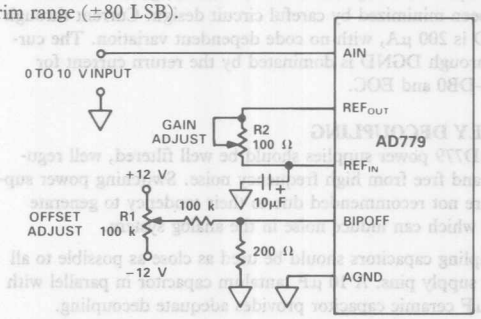


Figure 6. Unipolar Input Connections with Gain and Offset Trims

The first transition (from 00 0000 0000 0000 to 00 0000 0000 0001) should nominally occur for an input level of +1/2 LSB (0.305 mV above ground for a 10 V range). To trim unipolar zero to this nominal value, apply a 0.305 mV signal to AIN and adjust R1 until the first transition is located.

The gain trim is done by adjusting R2. If the nominal value is required, apply a signal 1 1/2 LSB below full scale (9.9997 V for a 10 V range) and adjust R2 until the last transition is located (11 1111 1111 1110 to 11 1111 1111 1111).

If offset adjustment is not required, BIPOFF should be connected directly to AGND. If gain adjustment is not required, R2 should be replaced with a fixed 50 Ω ±1% metal film resistor. If REF_{OUT} is connected directly to REF_{IN}, the additional gain error will be approximately 1%.

REFERENCE DECOUPLING

It is recommended that a 10 µF tantalum capacitor be connected between REF_{IN} (Pin 9) and ground. This has the effect of improving the S/N+D ratio through filtering possible broadband noise contributions from the voltage reference.

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is a significant issue. A 1.22 mA current through a 0.5 Ω trace will develop a voltage drop of 0.6 mV, which is 1 LSB at the 14-bit level for a 10 V full scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter out ac noise.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

The AD779 incorporates several features to help the user's layout. Analog pins (V_{EE}, AIN, AGND, REF_{OUT}, REF_{IN}, BIPOFF, V_{CC}) are adjacent to help isolate analog from digital signals. In addition, the 10 MΩ input impedance of AIN minimizes input trace impedance errors. Finally, ground currents have been minimized by careful circuit design. Current through AGND is 200 μA, with no code dependent variation. The current through DGND is dominated by the return current for DB13–DB0 and EOC.

SUPPLY DECOUPLING

The AD779 power supplies should be well filtered, well regulated, and free from high frequency noise. Switching power supplies are not recommended due to their tendency to generate spikes which can induce noise in the analog system.

Decoupling capacitors should be used as close as possible to all power supply pins. A 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor provides adequate decoupling.

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD779, associated analog input circuitry and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD779 will isolate large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

GROUNDING

If a single AD779 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD779. If multiple AD779s are used or the AD779 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at each chip. This prevents large ground loops which inductively couple noise and allow digital currents to flow through the analog system.

USE OF EXTERNAL VOLTAGE REFERENCE

The AD779 features an on-chip voltage reference. For improved gain accuracy over temperature, a high performance external voltage reference may be used in place of the on-chip reference.

The AD586 and AD588 are popular references appropriate for use with high resolution converters. The AD586 is a low cost reference which utilizes a buried Zener architecture to provide low noise and drift. The AD588 is a higher performance reference which uses a proprietary ion-implanted buried Zener diode in conjunction with laser-trimmed thin-film resistors for low offset and low drift.

Figure 7 shows the use of the AD586 with the AD779 in a bipolar input mode. Over the 0 to +70°C range, the AD586 L-grade exhibits less than a 2.25 mV output change from its initial value at 25°C. REF_{IN} (Pin 9) scales its input by a factor of two; thus, this change becomes effectively 4.5 mV. When applied to the AD779, this results in a total gain drift of 0.09% FSR which is an improvement over the on-chip reference performance of 0.11% FSR. A noise-reduction capacitor, C_N, has been shown. This capacitor reduces the broadband noise of the AD586 output, thereby optimizing the overall ac and dc performance of the AD779.

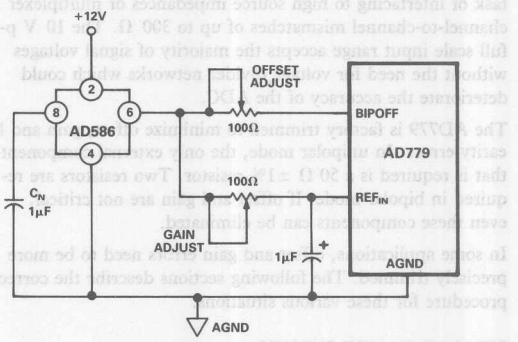


Figure 7. Bipolar Input with Gain and Offset Trims

Figure 8 shows the AD779 in unipolar input mode with the AD588 reference. The AD588 output is accurate to 0.65 mV from its value at 25°C over the 0 to 70°C range. This results in a 0.06% FSR total gain drift for the AD779, which is a substantial improvement over the on-chip reference performance of 0.11% FSR. A noise-reduction network on Pins 4, 6 and 7 has been shown. The 1 μF capacitors form low pass filters with the internal resistance of the AD588 Zener and amplifier cells and external resistance. This reduces the high frequency noise of the AD588, providing optimum ac and dc performance of the AD779.

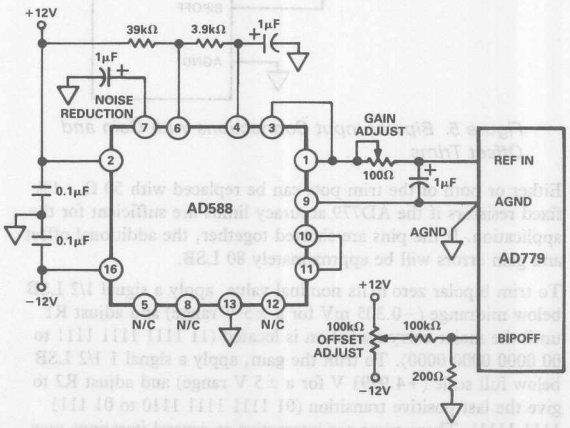


Figure 8. Unipolar Input with Gain and Offset Trims

INTERFACING THE AD779 TO MICROPROCESSORS

The I/O capabilities of the AD779 allow direct interfacing to general purpose and DSP microprocessor buses. The asynchronous conversion control feature allows complete flexibility and control with minimal external hardware.

The following examples illustrate typical AD779 interface configurations.

In Figure 9 the AD779 is mapped into the TMS320C25 I/O space. AD779 conversions are initiated by issuing an OUT instruction to Port 1. EOC status and the conversion result are read in with an IN instruction to Port 1. A single wait state is inserted by generating the processor READY input from $\overline{IS}$, Port 1 and $\overline{MSC}$. This configuration supports processor clock speeds of 20 MHz and is capable of supporting processor clock speeds of 40 MHz if a NOP instruction follows each AD779 read instruction.

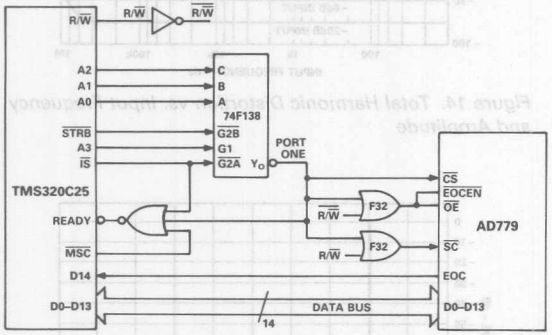


Figure 9. AD779 to TMS320C25 Interface

AD779 TO 80186

Figure 10 shows the AD779 interfaced to the 80186 microprocessor. This interface allows the 80186's built-in DMA controller to transfer the AD779 output into a RAM based FIFO buffer of any length, with no microprocessor intervention.

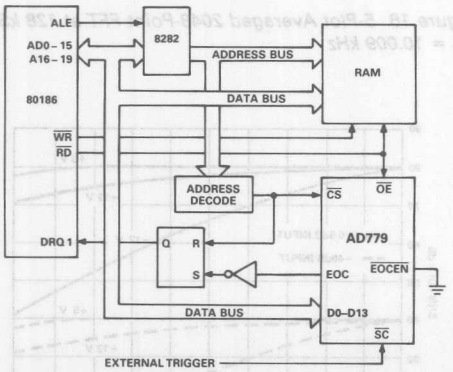


Figure 10. AD779 to 80186 DMA Interface

AD779 TO Z80

The AD779 can be interfaced to the Z80 processor in an I/O or memory mapped configuration. Figure 11 illustrates an I/O configuration, where the AD779 occupies several port addresses to allow separate polling of the EOC status and reading of the data. A useful feature of the Z80 is that a single wait state is automatically inserted during I/O operations, allowing the AD779 to be used with Z80 processors having clock speeds up to 8 MHz.

tiated by an external trigger source independent of the microprocessor clock. After each conversion, the AD779 EOC signal generates a DMA request to Channel 1 (DRQ1). The subsequent DMA READ resets the interrupt latch. The system designer must assign a sufficient priority to the DMA channel to ensure that the DMA request will be serviced before the completion of the next conversion. This configuration can be used with 6 MHz and 8 MHz 80186 processors.

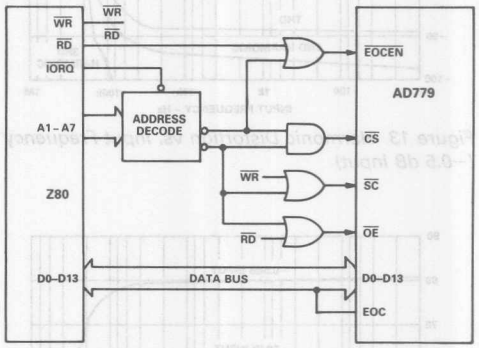


Figure 11. AD779 to Z80 Interface

AD779 TO ANALOG DEVICES ADSP-2100A

Figure 12 demonstrates the AD779 interfaced to an ADSP-2100A. With a clock frequency of 12.5 MHz, and instruction execution in one 80 ns cycle, the digital signal processor will support the AD779 data memory interface with two wait states.

The converter runs asychronously using a sampling clock. The EOC output to the AD779 gets asserted at the end of each conversion and causes an interrupt. Upon interrupt, the ADSP-2100A starts a data memory read by providing an address on the DMA bus. The decoded address generates $\overline{OE}$ for the converter. $\overline{OE}$, together with logic and latch, is used to force the ADSP-2100A into a one cycle wait state by generating DMACK. The read operation is thus started and completed within two processor cycles (160 ns).

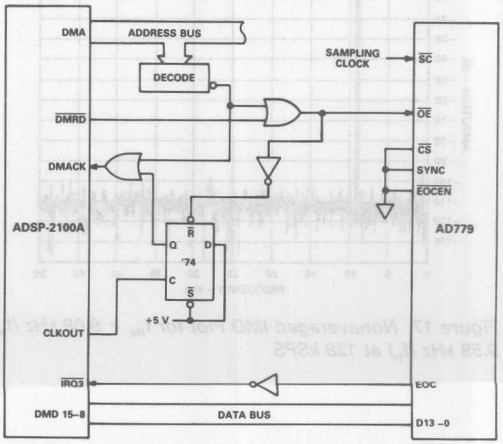


Figure 12. AD779 to ADSP-2100A Interface

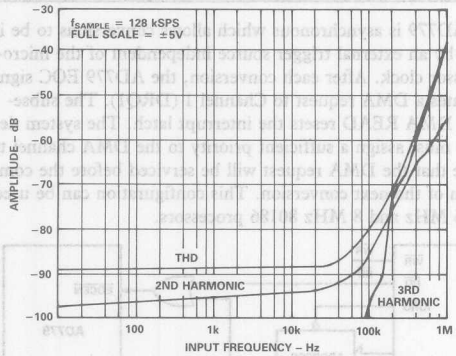


Figure 13. Harmonic Distortion vs. Input Frequency (−0.5 dB Input)

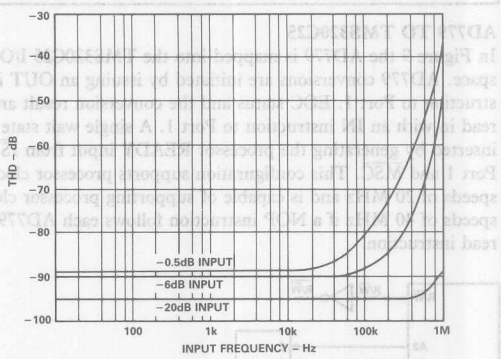


Figure 14. Total Harmonic Distortion vs. Input Frequency and Amplitude

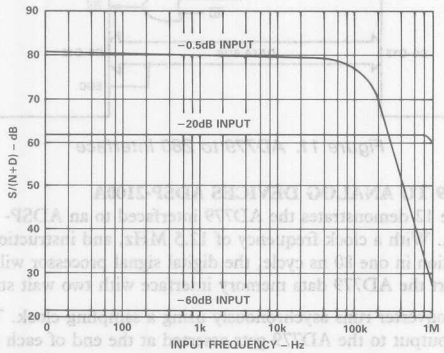


Figure 15. S/(N+D) vs. Input Frequency and Amplitude

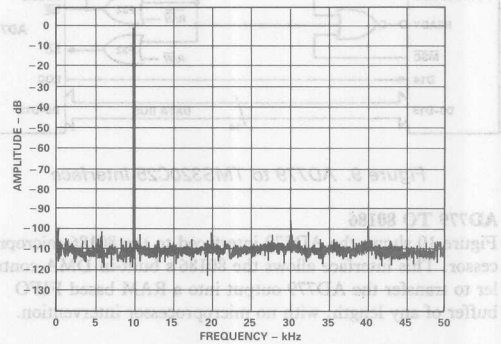


Figure 16. 5-Plot Averaged 2048-Point FFT at 128 kSPS, f_{IN} = 10.009 kHz

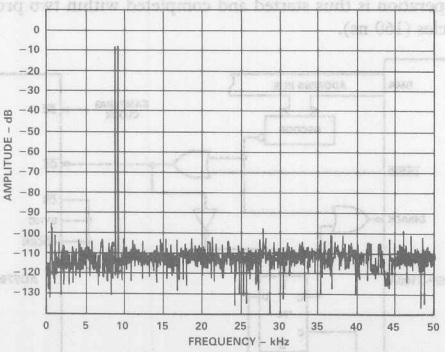


Figure 17. Nonaveraged IMD Plot for f_{IN} = 9.08 kHz (f_a), 9.58 kHz (f_b) at 128 kSPS

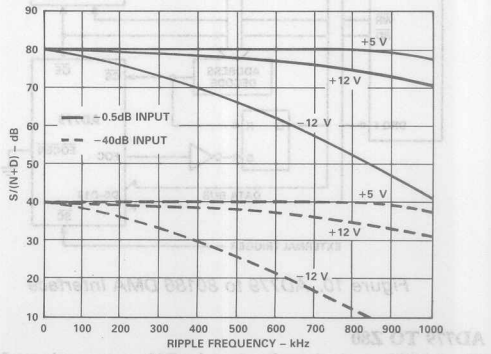


Figure 18. Power Supply Rejection (f_{IN} = 10 kHz, f_{SAMPLE} = 128 kSPS, V_{RIPPLE} = 0.1 V p–p)

High Resolution, Programmable Integrating A/D Converter

AD1170

FEATURES

Low Nonlinearity:
- **Integral: ±0.001%**
- **Differential: ±0.00035%**

Microcomputer-Based Design
- **Programmable Integration Time: 1 to 350ms with Resolution from 7 to 18 Bits**
- **Programmable Output Data Format**
- **Auto-Zeroed Operation and Electronic Calibration (No External Trim Potentiometers)**
- **Microprocessor Compatible Interface**

High Throughput: Over 50 Conversions/Second for Line Cycle Integration Period

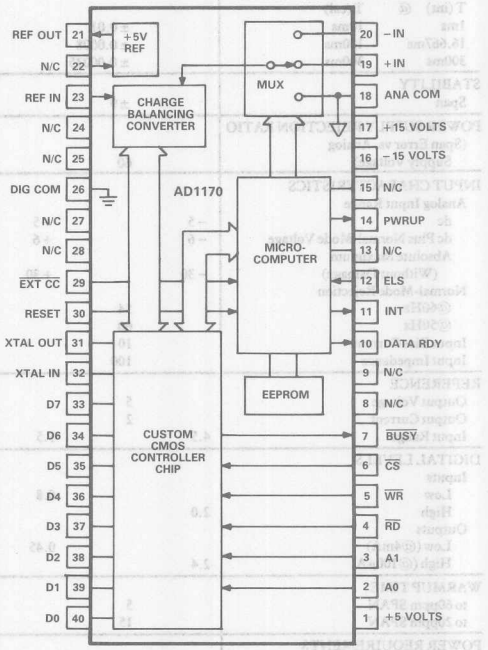
High Normal Mode Rejection: 54dB at 60Hz

Small Size: 1.24″ × 2.5″ × 0.55″ max

APPLICATIONS

Data Acquisition Systems
Scientific Instruments
Medical Instruments
Weighing Systems
Automatic Test Equipment

FUNCTIONAL BLOCK DIAGRAM



LEAVE N/C PINS UNCONNECTED

GENERAL DESCRIPTION

The AD1170 is a high resolution integrating A/D converter intended for applications requiring high accuracy and high throughput at low cost. A novel conversion architecture provides the user with outstanding accuracy, stability and ease of use.

The AD1170 is a complete microcomputer-based measurement subsystem, composed of three major elements: a highly precise charge balancing converter, a single chip microcomputer, and a custom CMOS controller chip. The AD1170 offers independently programmable integration time (from one millisecond to 350 milliseconds) and data format (offset binary or two's complement, from 7 to 22 bits). The converter is fully auto-zeroed and exhibits a span drift of only 9ppm/°C, assuring stable, accurate readings.

The AD1170 may be interfaced to any microcomputer based system in a memory mapped or I/O mapped fashion via an 8-bit data bus. The AD1170's advanced features are controlled by simple commands sent to it via this bus.

The converter utilizes surface mount technology and is housed in a small 1.24″ × 2.5″ × 0.55″ package. It operates from ±15V dc and +5V dc power.

PRODUCT HIGHLIGHTS

1. The AD1170, unlike dual slope converters, offers the user the capability of programming the integration time by selecting one of seven preset integration periods or by loading an arbitrary integration period over the interface bus.
2. The AD1170 architecture provides for user programmable data format independent of the integration time. All data is computed to 22-bit resolution and the user may specify any resolution from 7 to 22 bits. Usable resolution will typically be limited to 18-bits due to measurement and calibration noise error.
3. Electronic digital calibration eliminates the need for trim potentiometers. Calibration can be performed at any time by applying an external reference voltage to the input and invoking a calibration command. The calibration data is stored in an internal nonvolatile memory chip.
4. Internal calibration cycles may be programmed to occur whenever the converter is idle, assuring negligible offset drift and only 9ppm/°C span drift.
5. The conversion rate is greater than 50 conversions per second when programmed for 60Hz line cycle integration. The maximum conversion rate is greater than 250 conversions per second, using a one millisecond integration period.

AD1170—SPECIFICATIONS (typical @ +25°C, V_S = +15V, V_D = +5V unless otherwise specified.)

Model	Min	Typ	Max	Units
RESOLUTION[1]	7		18	Bits
ACCURACY				
Integral Nonlinearity[2]		±0.001		% SPAN
THROUGHPUT RATE[3]				
Time (Integrate) = 1ms	250			conv/S
Time (Integrate) = 16.667ms	50			conv/S
Time (Integrate) = 100ms	9			conv/S
DIFFERENTIAL NONLINEARITY				
T(int) @ T(cal)				
1ms 10ms		±0.01		% SPAN
16.667ms 100ms		±0.0008		% SPAN
300ms 300ms		±0.00035		% SPAN
STABILITY				
Span		±9		ppm SPAN/°C
POWER SUPPLY REJECTION RATIO				
(Span Error vs. Analog Supply Voltage)		60		ppm of Reading/V
INPUT CHARACTERISTICS				
Analog Input Range				
dc	−5		+5	V
dc Plus Normal-Mode Voltage	−6		+6	V
Absolute Maximum (Without Damage)	−30		+30	V
Normal-Mode Rejection				
@60Hz		54		dB
@50Hz		60		dB
Input Bias Current		10		nA
Input Impedance		100		MΩ
REFERENCE				
Output Voltage		5		V dc
Output Current		2		mA
Input Range	4.5		5.5	V dc
DIGITAL LEVELS				
Inputs				
Low			0.8	V
High	2.0			V
Outputs				
Low (@4mA)			0.45	V
High (@100μA)	2.4			V
WARMUP TIME				
to 60ppm SPAN		5		min
to 20ppm SPAN		15		min
POWER REQUIREMENTS				
$+V_S$ and $-V_S$	9	15	18	V
$+V_D$	4.75	5	5.25	V
Supply Current Drain				
@ ±15V		12		mA
@ +5V		110		mA
TEMPERATURE RANGE				
Rated Performance	0		+70	°C
Storage	−25		+85	°C
SIZE	1.24" × 2.5" × 0.55" max (31.4 × 63.5 × 14.0) mm			

NOTES

[1]The usable resolution is limited by noise, which is largely determined by the integration period and calibration period. Consult the chart in Figure 4 for typical peak-to-peak noise versus integration and calibration period.

[2]The integral linearity is defined as the deviation from a straight line drawn between the endpoints of the converter. This specification is independent of gain and/or offset errors.

[3]Throughput Rate is calculated by the formula: $\frac{1000}{T(int) + 3 \text{ milliseconds}}$ = minimum conversions/second

Where T(int) is expressed in number of milliseconds.

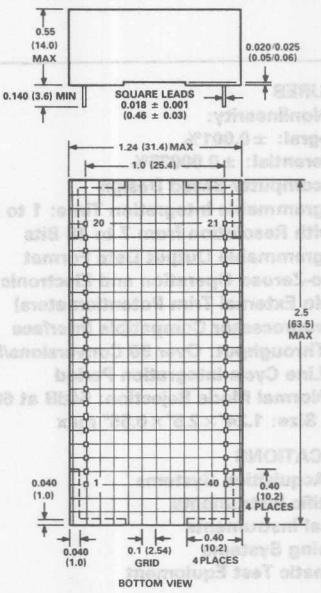
Specifications subject to change without notice.

IBM PC/XT/AT compatible evaluation board:* AC5004 (see last page of this data sheet for description).

*IBM PC/XT/AT is a trademark of International Business Machines Corp.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



BOTTOM VIEW



CAUTION: OBSERVE PROPER PLUG-IN POLARITY TO PREVENT DAMAGE TO CONVERTER

PIN DESCRIPTIONS

PIN	SIGNAL	DESCRIPTION
1	+5V	Digital Power Supply
2,3	A0, A1	Address Control Lines
4	$\overline{RD}$	Read Data Strobe
5	$\overline{WR}$	Write Data Strobe
6	$\overline{CS}$	Chip Select
7	$\overline{BUSY}$	When Low, Indicates Device Busy When High, Indicates Device Ready for Command
10	DTA RDY	When High, Indicates That Data From Most Recent Conversion Command is Ready
11	INT	When High, Indicates Device is Currently Integrating Input Signal. Goes Low to Indicate Integration Complete
12	ELS	External Line Sample Input. Used with ELS Command to Sense an Externally Provided Sample of the Line Frequency
14	PWR UP	When High, Indicates Power Up Initialization in Progress
16	−15V	Negative Analog Power Supply
17	+15V	Positive Analog Power Supply
18	ANA COM	Analog Common: the Reference Point for Analog Power Supplies
19	+IN	Positive Signal Input
20	−IN	Negative Signal Input
21	REF OUT	Internal +5V Reference Output
23	REF IN	Reference Input; Normally Connected to Ref Out
26	DIG COM	Digital Common; the Reference Point for the Digital Power Supply
29	$\overline{E_{XT}\,CC}$	External Convert Command Input
30	RESET	Reset Input; Usually Connected to an RC Network for Automatic Reset Upon Power Up
31,32	XTAL OUT, XTAL IN	Connections for 12MHz Crystal (Series Resonant, 30Ω ESR). Alternatively, Xtal In May Be Driven From an External 12MHz Logic Signal
33-40	D7-D0	Bidirectional Data Bus
8, 9, 13, 15, 22, 24 25, 27 28		DO NOT CONNECT

parameters as programmed by the user (such as the integration period, output data format, calibration coefficient, etc.). The AD1170 is calibrated at the factory with the following default settings:

FORMAT: 16-bit, offset binary
DEFAULT T(int): 16.667 milliseconds (code 2)
DEFAULT T(cal): 100 milliseconds (code 4)

AD1170 ARCHITECTURAL OVERVIEW

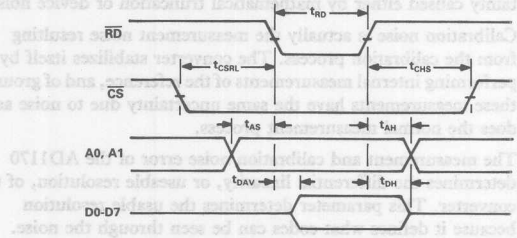
The AD1170 is a complete microcomputer-based measurement subsystem, containing three major elements: a highly precise charge balancing converter, a single chip microcomputer, and a custom CMOS controller chip.

The heart of the measurement technique is the charge balancing converter (essentially a voltage to frequency converter). This converter measures the input signal by balancing a proportional current against a train of precisely controlled reference current pulses using an integrator. The microprocessor, together with the counting and gating circuitry within the CMOS controller chip, measures the period of the reference current pulses by interpolating them using a 12MHz clock signal. The resulting

When the AD1170 is triggered to perform a conversion, two separate phases are performed: first, an integration phase, where the input signal is actually measured, and then a computation phase, where the data from the integration phase is processed, along with both the volatile and nonvolatile calibration data, and formatted for output as the user desires.

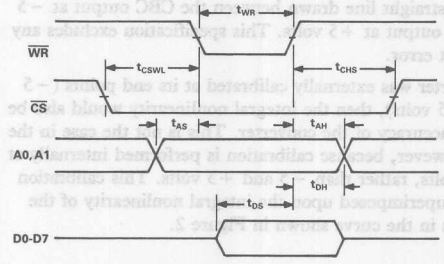
The duration of the integration phase can be programmed by the user, and may be as short as one millisecond, or as long as 350 milliseconds. The computation phase always lasts approximately three milliseconds and commences immediately after the integration phase is over. Therefore, the total conversion time will equal the user programmed integrate time plus a fixed 3 milliseconds. Status signals are provided to indicate when the data is ready and when the converter may be retriggered for the next conversion.

For maximum stability, the AD1170 periodically calibrates itself by performing measurements upon a zero input signal and a full-scale signal provided by the internal reference. This technique cancels any drift within the charge balancing converter itself, resulting in negligible offset drift, and gain stability equal to that of the reference. Calibration cycles may be programmed to take place whenever the AD1170 is idle, or they may be invoked under system control.



READ CYCLE TIMING REQUIREMENTS

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{RD}	RD Pulse Width	150			ns
t_{CSRL}	Chip Select to RD Low	0			ns
t_{CHS}	Chip Select Hold Time	0			ns
t_{AS}	Address Setup Time	10			ns
t_{AH}	Address Hold Time	0			ns
t_{DAV}	Data Valid Time			100	ns
t_{DH}	Data Hold Time			80	ns



WRITE CYCLE TIMING REQUIREMENTS

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{WR}	WR Pulse Width	0.10		20	µs
t_{CSWL}	Chip Select to WR Low	0			ns
t_{CHS}	Chip Select Hold Time	0			ns
t_{AS}	Address Setup Time	10			ns
t_{AH}	Address Hold Time	0			ns
t_{DS}	Data Setup Time	80			ns
t_{DH}	Data Hold Time	20			ns

Figure 1. Timing Diagrams and Requirements

The AD1170 contains no internal trims; its span accuracy is factory calibrated by using the ECAL (Electronic CALibration) feature. This feature is a firmware routine which measures an externally applied reference voltage, compares it to the internal reference voltage, and computes a span correction factor which is stored in nonvolatile memory. The correction factor is then applied to all subsequent measurements, thereby compensating for the reference error. The ECAL function may be invoked by the user at any time, thereby replacing the usual trim potentiometer with a totally electronic calibration capability.

UNDERSTANDING THE AD1170 SPECIFICATIONS

The AD1170, because of its unique conversion technique, is specified quite differently from more conventional integrating converters. The following sections will help the user to understand where the sources of error are, and how to extract the best possible performance from the converter.

There are two primary sources of error in the AD1170: integral nonlinearity of the charge balancing converter, which influences all conversions equally, regardless of the integration period and calibration period; and the noise error of the measurement/calibration process, which is a function of the integration period and calibration period as selected by the user.

INTEGRAL NONLINEARITY

The integral nonlinearity of the charge balancing converter (CBC) is ±10ppm (±0.001%) of Span. This specification is an "endpoint" nonlinearity measurement; i.e., the typical deviation seen from a straight line drawn between the CBC output at −5 volts and its output at +5 volts. This specification excludes any gain or offset error.

If the converter was externally calibrated at its end points (−5 volts and +5 volts), then the integral nonlinearity would also be the relative accuracy of the converter. This is not the case in the AD1170, however, because calibration is performed internally at 0 and +5 volts, rather than −5 and +5 volts. This calibration technique, superimposed upon the integral nonlinearity of the CBC, results in the curve shown in Figure 2.

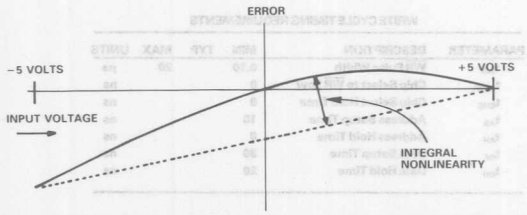


Figure 2. Relative Accuracy and Integral Nonlinearity when Calibrated

As shown in the diagram, the calibration technique tends to exaggerate the relative error at the negative end of the scale, and reduce the error between 0 and +5 volts. This characteristic happens to be most beneficial when using the AD1170 in systems where the input comes from a sensor whose signal is mostly positive, such as a thermocouple.

For systems where the user desires to minimize the relative error equally across the whole span of the converter, it is possible to intentionally introduce a span error during the ECAL procedure, as shown in Figure 3. This scheme sacrifices positive full-scale accuracy in order to minimize negative full scale error. The net result is a relative accuacy equal to the integral nonlinearity.

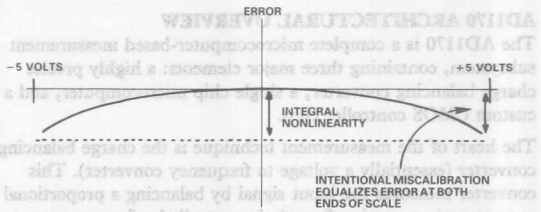


Figure 3. Relative Accuracy with Intentional Span Error at +F.S.

In both cases the accuracy of the input offset (which is servo controlled) is not compromised.

MEASUREMENT/CALIBRATION NOISE

Measurement noise refers to the conversion-to-conversion uncertainty caused either by mathematical truncation or device noise.

Calibration noise is actually the measurement noise resulting from the calibration process. The converter stabilizes itself by performing internal measurements of the reference, and of ground; these measurements have the same uncertainty due to noise as does the normal measurement process.

The measurement and calibration noise error of the AD1170 determines the differential linearity, or useable resolution, of the converter. This parameter determines the usable resolution because it defines what codes can be seen through the noise. The specified value is the amount of error, in either direction from the average reading, which will not be exceeded for 95% of all conversions. This parameter, as in all integrating converters, is a function of the integration time; long conversions result in very high resolution, while short conversions provide lower resolution. In the AD1170, all internal computations are always carried out to 22-bit resolution, but useable resolution is limited by the peak-to-peak noise, as determined by T(cal) and T(int).

The chart shown in Figure 4, illustrates the typical peak-to-peak noise (in ppm Span) versus T(int) and T(cal). These numbers can be used to indicate how much useable resolution can be

T(cal) =	1ms	10ms	16.7ms	20ms	100ms	166.7ms	300ms	CAL DISABLED	UNITS
T(int) = 1ms	208	115	115	114	113	112	111	110	±ppm of SPAN
10ms		24	18	16	13	13	13	12	
16.7ms			14	13	8	8	8	8	
20ms				12	7	7	7	7	
100ms					4.0	4.0	3.5	3.5	
166.7ms						4.0	3.5	3.5	
300ms							3.5	3.5	

Figure 4. Typical Peak-to-Peak Noise (in ppm Span) Versus T(int) and T(cal)

expected under a given set of operating conditions. For example, a peak-to-peak noise of ±8ppm is approximately analogous to a flicker of ±0.5LSB at 16 bits of resolution. Under these conditions, a user could set the default format for the AD1170 to 16-bit resolution, and observe no more than ±1/2LSB of differential error. See Table I for conversion of typical peak-to-peak noise to Differential Nonlinearity and Useable Resolution.

The chart in Figure 4 may also be used to determine the minimum effective calibration time for a specified integration period; the noise contributions of both the measurement cycle and the calibration cycle combine as the "root sum square", and the combined effect tends to asymptotically approach a baseline value determined by the shorter of the two. For example, a T(cal) greater than 10 milliseconds does little or nothing to improve the noise performance for conversions using a T(int) of 1 millisecond.

NOISE (ppm Span)	RESOLUTION AT 1/2LSB DNL ERROR (NO. OF BITS)	RESOLUTION AT 1LSB DNL ERROR (NO. OF BITS)	DIFFERENTIAL NONLINEARITY (% Span)
244	11	12	0.024
122	12	13	0.012
61	13	14	0.006
31	14	15	0.003
15	15	16	0.0015
8	16	17	0.00076
4	17	18	0.00038
2	18	19	0.00019

Table I. Conversion of Noise Error to DNL and Usable Resolution

SIGNAL INPUT CONNECTIONS

The AD1170 has both a positive input pin (+IN) as well as a negative input pin (−IN), but the AD1170 input is not a true differential input. The negative input pin is an input used during calibration cycles to establish the zero reference. In applications with static ground offsets, the −IN pin may be used as a ground sense input, to sense a signal reference point which is offset from analog common by a small differential. Both the −IN and +IN signals must have a bias current path back to analog common. Figure 5 illustrates the proper use of the input signal connections.

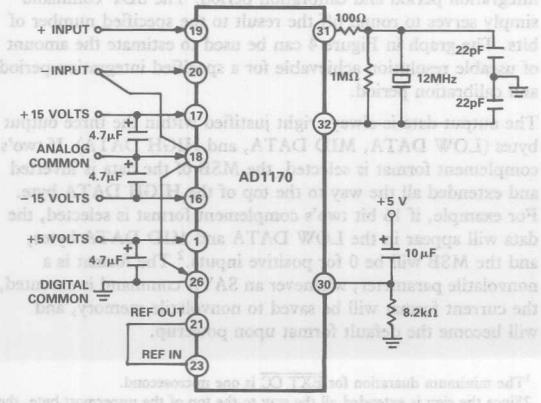


Figure 5. Input, Power, Reset, and Clock Connections

RESET

A reset sequence must be accomplished after power-up and before any access to the converter. The RESET line initializes the internal logic of the AD1170. This line may be driven from an external source, such as may exist in most computer based systems, or it may be connected to a simple RC circuit which will automatically invoke a reset sequence at power-up. Figure 5 illustrates the recommended circuit.

When driving the RESET line from an external source, the line must be held high for at least 2 microseconds after the oscillator is running and stable (typically 300 microseconds after power is applied) in order to assure a proper reset.

CLOCK

The AD1170 requires a 12MHz clock for operation. This clock may be supplied by connecting the XTAL OUT and XTAL IN pins to a 12MHz crystal, along with two resistors and two capacitors as shown in Figure 5.

The user may also supply a 12MHz logic signal from an external source, such as may be available in the user's system. In this case, the external clock should be applied to the XTAL IN pin, and the XTAL OUT pin should remain unconnected.

POWERING THE AD1170

For best performance, the user should pay careful attention to proper power supply bypassing, as well as grounding. Analog common and digital common are not connected internal to the module, but must be connected externally. Figure 5 illustrates the proper connection of power and ground to the AD1170[1].

REFERENCE CONNECTIONS

The internal +5 volt reference of the AD1170 is brought out to Pin 21 of the module; for normal operation, it should be connected to the reference input (Pin 23).

An external reference voltage of from 4.5 to 5.5 volts may be applied to the reference input (Pin 23), and the reference output may remain unconnected. The data will be ratiometric to that reference. The input impedance of the reference input is approximately 16K ohms. The reference input is not dynamic; any external reference voltage must be an essentially static DC signal.

INTERFACING TO THE AD1170

The AD1170 contains an eight-bit microprocessor compatible interface structure, including control lines. It can be interfaced to any microprocessor-based system in either a memory mapped or I/O mapped mode, and occupies four successive bytes of read/write address space, as shown in Figure 6.[1]

	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	FUNCTION
	H	X	X	X	X	Device Not Selected
WRITE	L	H	L	H	H	(Unused)
WRITE	L	H	L	H	L	Parameter 2 Write
WRITE	L	H	L	L	H	Parameter 1 Write
WRITE	L	H	L	L	L	Command Write
READ	L	L	H	H	H	High Data Read
READ	L	L	H	H	L	Mid Data Read
READ	L	L	H	L	H	Low Data Read
READ	L	L	H	L	L	Status Read

X = DON'T CARE

Figure 6. Control Functions

[1]Attempting to READ and WRITE at the same time ($\overline{RD}$ and $\overline{WR}$ set low) may alter the contents of the internal nonvolatile memory.

byte of the device image. Upon receipt of the command byte, the BUSY line is set low, indicating that command interpretation is in progress. The BUSY line returns high, following command interpretation and a command dependent execution time. This signals that the command execution has been completed, and another command may now be written. The logical inverse of the BUSY line is available in the STATUS byte for use in polling. See the section below about THE STATUS BYTE.

When the command requires one or two parameters, in addition to the command byte, they must be written into the second and third parameter bytes of the image *before* writing the command byte. This is because writing the command byte triggers the microprocessor to begin command interpretation.

Following the execution phase of any command, the CMD ERR bit in the STATUS byte will indicate acceptance or rejection of the command. When set, this bit indicates that there was a contextual or syntactic error in the command or parameters.

Conversions may be initiated either by bus command, or by a high to low transition of the EXT CC line[1]. Externally triggered conversions behave in the same way as bus triggered conversions, except that the BUSY line and the BUSY bit in the status word remain inactive; the end of execution of externally triggered conversions must be determined by examination of the DTA RDY line or the DTA RDY bit in the STATUS word.

THE STATUS BYTE

The lowest readable byte of the device image is the STATUS byte; it contains six bits of information about the current status of the AD1170. This byte may be examined by the host processor at any time. The individual bits in the status byte (see Figure 7) are assigned the following functions:

BIT0 The BUSY bit is an inverted version of the signal on Pin 7 of the module. When low, it indicates that the AD1170 is ready to receive a command. When high, it indicates that the AD1170 is busy executing the last command. Any commands loaded while the BUSY signal is high will be ignored.

BIT1 The DTA RDY bit (also available on Pin 10 of the module) goes high to indicate that the data from the most recent conversion is available in the LOW DATA, MID DATA, and HIGH DATA registers. This bit is cleared at the start of the next conversion. It may also be cleared by executing an EOI command.

BIT2 The DATA SAT bit is set by any conversion which is saturated, i.e., any conversion whose output data exceeds positive or negative full scale.

BIT3 The CMD ERR bit indicates that the most recently loaded command contained a contextual or syntactic error, or was not recognized. It is cleared when the next command is loaded.

BIT4 The INT bit (also available on Pin 11 of the module) goes high to indicate that the input signal is currently being integrated. It is used in multiplexed systems to determine when the input multiplexer may be switched.

BIT5 The PWRUP bit (also available on Pin 14 of the module) goes high when the module is powered up or when the RST command is executed. It remains high until device initialization is complete. This signal is used to indicate readiness of the converter after system initialization.

*	*	PWRUP	INT	CMD ERROR	DATA SAT	DATA RDY	BUSY

* UNUSED: CONTENTS INDETERMINATE

Figure 7. The Status Byte

OUTPUT DATA FORMAT

The AD1170 architecture allows a programmable data format independent of the integration time. The user may specify any resolution from 7 to 22 bits, and may specify either offset binary coding or two's complement coding. Programming the data format is accomplished via the use of the SDF command, using the format code described in the table in Figure 8 as the PARAMETER 1 value.

C_4	C_3	C_2	C_1	C_0	DATA FORMAT
H	X	X	X	X	Two's Complement
L	X	X	X	X	Offset Binary
X	H	H	H	H	22 Bits
X	H	H	H	L	21 Bits
X	H	H	L	H	20 Bits
X	H	H	L	L	19 Bits
X	H	L	H	H	18 Bits
X	H	L	H	L	17 Bits
X	H	L	L	H	16 Bits
X	H	L	L	L	15 Bits
X	L	H	H	H	14 Bits
X	L	H	H	L	13 Bits
X	L	H	L	H	12 Bits
X	L	H	L	L	11 Bits
X	L	L	H	H	10 Bits
X	L	L	H	L	9 Bits
X	L	L	L	H	8 Bits
X	L	L	L	L	7 Bits

X = DON'T CARE (C_7 C_6 C_5 = X FOR ALL DATA FORMATS)

Figure 8. Format Code

It should be noted that the AD1170 computes all data to 22 bit resolution. However, not all 22 bits are useable, since the differential performance is largely dependent upon factors such as integration period and calibration period. The SDF command simply serves to round off the result to the specified number of bits. The graph in Figure 4 can be used to estimate the amount of useable resolution achievable for a specified integration period and calibration period.

The output data is always right justified within the three output bytes (LOW DATA, MID DATA, and HIGH DATA). If two's complement format is selected, the MSB of the data is inverted and extended all the way to the top of the HIGH DATA byte. For example, if 16 bit two's complement format is selected, the data will appear in the LOW DATA and MID DATA bytes, and the MSB will be 0 for positive inputs.[2] The format is a nonvolatile parameter; whenever an SAVA command is executed, the current format will be saved to nonvolatile memory, and will become the default format upon powerup.

[1]The minimum duaration for $\overline{\text{EXT CC}}$ is one microsecond.

2Since the sign is extended all the way to the top of the uppermost byte, the HIGH DATA byte will be filled with the value of the MSB.

PROGRAMMING THE INTEGRATION PERIOD

The key parameter of any integrating A/D converter is the integration period. As shown in Figure 9, an integrating A/D converter provides maximum normal mode rejection at those frequencies which are integral multiples of 1/T(int), where T(int) is the integration period. The most common way to exploit this characteristic is to set the integration period equal to one period of the power line frequency so that ac hum will be rejected.

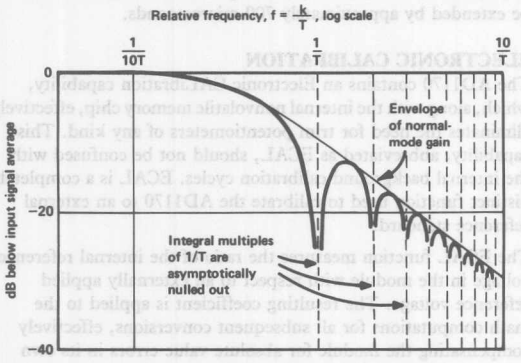


Figure 9. Normal Mode Rejection

The duration of the integration also affects the resulting resolution of the data; long integration times result in more usable resolution than do short integration periods.

The AD1170, unlike most dual slope converters, offers the user the capability of programming the integration time. This feature can be used to great advantage in systems design, since the integration time can be optimized for differing system conditions. For example, in systems whose inputs are severely polluted by 60Hz noise, the user may wish to program the AD1170 for a 100 millisecond integration time, which will result in excellent 60Hz normal mode rejection. In another application, a user may wish to scan a large number of channels rapidly, looking for gross input changes, then slow down in order to make a high resolution conversion before resuming rapid scanning.

The AD1170 offers the user a number of different ways to set the integration period. The simplest way is by using the SDI command to set the default integration period to one of seven preset periods (1ms, 10ms, 16.66ms, 20ms, 100ms, 166.66ms, 300ms). The first two preset periods offer fairly rapid scanning at reduced resolution; the other five represent American and European line voltage standards or multiples thereof. For single conversions without altering the default integration time, the CNVP command may be used, which also allows the selection of one of these seven preset periods. These preset periods and their corresponding codes are listed in the table of Figure 10.

Another way in which the integration period may be programmed is via the EIS command, which allows the user to load the externally definable period register with a binary value[1] proportional to the desired integration period. Using this technique, the user may specify any period from one millisecond to 350 milliseconds (with 200 microsecond accuracy). Access to this user definable period is via the SDI or CNVP commands; the last entry in Figure 10 is used to select the period defined by the EIS or ELS command.

C_2	C_1	C_0	INTEGRATION TIME	NOTES
L	L	L	1 Millisecond	
L	L	H	10 Milliseconds	
L	H	L	16.667 Milliseconds	1 cycle @ 60Hz
L	H	H	20 Milliseconds	1 cycle @ 50Hz
H	L	L	100 Milliseconds	50/60Hz
H	L	H	166.67 Milliseconds	10 cycles @ 60Hz
H	H	L	300 Milliseconds	50/60Hz
H	H	H	(See Note)	

NOTE
This code is used for externally loaded integration times (defined with the EIS Command) or externally measured times (from the ELS Command). The value can be anywhere from 1 Millisecond to 350 Milliseconds.

Figure 10. Preset Integration Periods

The third way to set the integration period is via the external line sampling feature, using the ELS command. This command samples the period of the logic signal presented to the ELS input pin (Pin 12), and sets the externally definable period register accordingly. This feature is most useful in environments with fluctuating line frequencies. By executing an occasional ELS command, the converter effectively "tracks" the line frequency. To use this feature, a clean, bounce free logic representation of the line frequency must be present at the ELS input during the execution of the ELS command. Once having performed the ELS command, the measured integration time may be selected using the SDI or CNVP commands along with the (HHH) code from the table in Figure 10[2].

It should be noted that the actual integration period used in the measurement process is accurate to about ±200μs, due to the limitations of the charge balancing converter. This is adequate, however, for greater than 50dB of normal mode rejection at 60Hz when using an integration period of 1/60 second. Even greater normal mode rejection may be obtained when the integration period is a multiple of the line frequency period.

CONTROLLING THE CALIBRATION CYCLE

The AD1170 achieves its excellent span and offset stability by calibrating itself against its internal reference voltages. The user can control the frequency of occurrence for calibration cycles and their duration.

The duration of the calibration cycle is an important parameter, because it affects the accuracy of the calibration cycle itself. Errors in the calibration cycle appear in the output data as instantaneous offset and span errors. If automatic "background" calibration is enabled, these errors effectively appear as noise. Just as in the case of input conversions, longer calibration times result in more accuracy and less noise.

Of course there may be system applications where there simply isn't sufficient time to perform a long calibration cycle. For this reason, the AD1170 offers the user the ability to specify the calibration period, using the SDC command.

The argument for the SDC command is the same three-bit code as is used for the SDI and CNVP commands. The reason for

[1]See the section titled "The AD1170 Command Set" for the formula used to compute the proper binary value.

[2]Caution is advised; if no signal is present at the ELS input when the ELS command is executed, or if the signal is not within acceptable frequency limits, the module may "hang" and require a hardware reset to continue operation.

this is that each calibration cycle consists essentially of two ordinary conversion cycles, performed upon the internal zero and span references. For example, if an SDC command with an argument of 3 is executed, the default calibration time will then be approximately 49 milliseconds (two conversions of 20 milliseconds plus approximately 9 milliseconds for the internal mathematics).

The user may also disable or enable background calibration. In systems where the AD1170 may be periodically idle, i.e., not performing input conversions, background calibration is a good choice. This mode is enabled with the CALEN command and will cause the AD1170 to continually initiate an internal calibration cycle whenever the converter is otherwise unoccupied. Any conversion commands received during a cal cycle will cause that cal cycle to be aborted in favor of the input conversion, thereby giving the user priority over calibration. This mode of operation is automatic and transparent.

The CALDI instruction is used to disable background calibration. When this instruction is executed, the converter will be completely idle between convert commands, and calibration cycles will only occur when invoked by the SCAL command. This mode of operation is best when the user would like to perform input conversions at the maximum rate, and/or when the system affords a specific convenient time to perform calibration.

There are no hard and fast rules about the best way to apply all of this flexibility, but best performance will be obtained if the following points are observed:

- Consult the chart in Figure 4 to determine the minimum effective calibration period for use with a desired integration period.
- Don't use automatic background calibration unless your system will allow the converter enough uninterrupted time to perform at least one calibration cycle. For example, if you are using a calibration period code of 3, your system must periodically allow at least 49 milliseconds without a convert command or calibration will not occur.
- Remember that the purpose of the calibration cycle is to cancel the intrinsic drift of the charge balancing converter within the AD1170 itself. If the converter is in a stable environment, calibration may be done less frequently. The best possible performance will be achieved in stable ambient temperatures, where calibration is manually invoked by the system at relatively long intervals, using the longest allowable calibration time.
- Very short calibration times, although allowed by the AD1170 firmware, are not especially useful because they introduce more error than they compensate. The only useful purpose of very short calibration times is in systems which are operating in rapidly changing ambient temperatures, and then only for relatively low resolution conversions.

COMPENSATION OF EXTERNAL OFFSETS

An electronic "null" feature compensates for offset errors of signal conditioning stages preceding the AD1170.

The null feature comprises three commands: NULL measures the input signal (using the current integration time) and stores it in internal RAM; NULEN subtracts the measured value from all subsequent conversions; NULDI cancels the NULEN command's effect.

The sum of the offset value plus the full-scale input should be less than the ±6 volts linear input range of the AD1170. The offset value to be nulled should ideally be no more than a few hundred millivolts in amplitude.

The NULL command does not need to be executed every time the AD1170 is powered up. Since the value measured by the NULL command is saved and restored by the SAVA and RESA commands, the value of the null will be the one saved during the last SAVA command. Execute a NULL command only when a new null measurement is desired.

When NULEN is in effect, the length of each conversion will be extended by approximately 700 microseconds.

ELECTRONIC CALIBRATION

The AD1170 contains an Electronic CALibration capability, which, along with the internal nonvolatile memory chip, effectively eliminates the need for trim potentiometers of any kind. This capability, abbreviated as ECAL, should not be confused with the internal background calibration cycles. ECAL is a completely distinct function used to calibrate the AD1170 to an external reference standard.

The ECAL function measures the ratio of the internal reference voltage in the module with respect to an externally applied reference voltage. The resulting coefficient is applied to the math computations for all subsequent conversions, effectively compensating the module for absolute value errors in its own reference. The ratio is stored in random access memory until the user invokes a SAVA command, which will save this coefficient (along with the other nonvolatile parameters) in the nonvolatile memory chip. When the module is powered up, the previously saved coefficient is recalled from nonvolatile memory and stored in random access memory.

In order to use the ECAL command, the input to the AD1170 must first be presented with an external +5 volt reference standard such as is usually found in many calibration labs. The ECAL command may then be invoked; the external reference voltage must remain at the input until command execution is complete. If the calibration is to be made nonvolatile, a SAVA command must then be invoked.[1]

ECAL may also be used as a means of making limited ratiometric measurements. For example, in some applications, it may be useful to be able to measure the output of some transducer with respect to its excitation; if the excitation can be scaled to the range of 4.5 to 5.5 volts, then it can be used as an excitation for the ECAL process. Having digitized the excitation, all subsequent conversions will be ratioed to the ECAL value. For example, if an ECAL procedure is performed upon a 4.5 volt source, and the converter subsequently digitizes a 2.25 volt signal, the converter output will be half of full scale, or 11000... (assuming offset binary coding). The converter can be restored to absolute calibration by executing a RESA command, which will restore the last nonvolatile ECAL coefficient to random access memory.

The user is cautioned that the nonvolatile memory used in the AD1170 has a finite endurance of 1000 write cycles minimum. Assuming that the AD1170 is calibrated weekly, this implies a device life span of greater than 19 years. Less frequent calibrations mean a proportionately longer life span. This means ECAL may be performed any number of times, but the user should limit the number of SAVA commands in order to extend the life span of the nonvolatile memory.

[1]Since the SAVA command saves all nonvolatile parameters, the user should be sure that the other default parameters, such as integration time and data format, are set to their desired values before SAVA is invoked.

NONVOLATILE MEMORY

The internal nonvolatile memory in the AD1170 is used to store the various nonvolatile parameters associated with A/D operation (for example, the integration period, data format, ECAL coefficient, etc.).

In addition, eight 16-bit words of the nonvolatile memory are made available to the user for general purpose use. They may be accessed using the RDNV and WRNV commands. Because the nonvolatile memory is specified for a finite endurance of 1000 write cycles minimum, it is best used for data which does not regularly need to change, such as configuration information or system calibration parameters.

FACTORY DEFAULT SETTINGS

The AD1170 is calibrated at the factory; the factory default settings are:

Format: 16-bit, offset binary
Default T(int): 16.667 milliseconds (code 2)
Default T(cal): 100 milliseconds (code 4)

THE AD1170 COMMAND SET

The AD1170 command code set includes 20 different functions. Some of the commands require no parameters, while others require one or two parameters which must be loaded into the PARAMETER 1 and PARAMETER 2 registers prior to loading the command register. Some commands (for example, CNVP) have their option parameter embedded in the lowest three bits of the command itself.

The execution time for any command depends on the command. Figure 11 is a synopsis of the available commands, as well as estimates of their execution times.

Each of the commands described below is preceded by an opcode name, along with the digital code (in binary).

CALEN 10110000

CALEN (CALibration ENable) enables automatic background calibration cycling. In this mode, background calibration cycles are executed automatically whenever the AD1170 is not otherwise occupied. If a command is received during a calibration cycle, that cycle will be aborted and the command will be executed.

CALDI 10111000

CALDI (CALibration DIsable) disables automatic background calibration. After executing this command, the AD1170 will be completely idle between commands. While in this state, a single calibration cycle may be invoked with the SCAL command.

CNV 00001000

CNV (CoNVert) causes a single conversion to be performed, using the current default integration time and data format.

CNVP $00010C_2C_1C_0$

CNVP (CoNVert using specific Preset time) causes a single conversion to be performed, using one of the eight preset integration times as listed in Figure 10. The default integration time is not changed. The three bit code for the desired integration time is embedded in the lowest three bits of the command code.

ECAL 00011000

ECAL (Electronic CALibration) causes an electronic calibration cycle to be performed. An external +5 volt reference voltage must be presented to the input before this command is executed, and the input must remain stable until the end of command execution is signaled by the BUSY line or the BUSY bit in the status word. The calibration data computed by this command is applied to all subsequent conversions, but is not made nonvolatile until a SAVA command is performed.

MNEMONIC	FUNCTIONAL DESCRIPTION	EXECUTION TIME (APPROX)
CNV	Perform a Single Conversion Using the Default Integration Time	T(int) + 3ms
CNVP	Perform a Single Conversion Using the Specified Integration Time	T(int) + 3ms
ELS	Measure Period of Signal at the ELS Input	2 × T(int) + 20ms
ECAL	Perform Electronic CALibration Routine	1.5 seconds
SDI	Set Default Integration Time for Input Measurements	150µs
SDC	Set Default Calibration Period	160µs
SDF	Set Default Data Format	140µs
RESA	Restore All Nonvolatile Parameters from Memory	2.3ms
SAVA	Save All Nonvolatile Parameters to Memory	150ms
WRNV	Write a Word to the User EEPROM Area	22ms
RDNV	Read a Word from the User EEPROM Area	600µs
EOI	Clear the Data Ready Flag	260µs
SCAL	Perform a Single Cal Cycle	2 × T(cal) + 9ms
CALEN	Enable Background Calibration	300µs
CALDI	Disable Background Calibration	310µs
EIS	Set Integration Time to Arbitrary Value	130µs
RST	Reset AD1170 to Power Up Conditions	210ms
NULL	Measure the Offset Voltage Value at the AD1170 Input and Store	T(int) + 3ms
NULEN	Subtract NULL Measured Value from All Subsequent Conversions	250µs
NULDI	Cancel the Effect of the NULEN Command	250µs

Figure 11. Synopsis of Commands

EOI 10001000

EOI (End Of Interrupt) clears the DTA RDY bit in the status byte, as well as the DTA RDY line (Pin 10). It is provided as a means of clearing the interrupt source in systems which use an interrupt upon data ready.

ELS 00100000

ELS (External Line Sample) measures the period of the logic signal applied to the ELS input (Pin 12)[1]. This period is loaded into the register associated with the last entry of the table in Figure 10. Input conversions using this measurement as the integration period may be performed by invoking a CNVP command, or by setting the default integration period with the SDI command. This command is intended for use in environments with varying line power frequency; periodically invoking this command allows effective tracking for improved normal mode rejection.

EIS 00101000

EIS (External Integration Set) is used to establish an arbitrary integration period from 1 millisecond to 350 milliseconds. To use this command, first load the PARAMETER 1 and PARAMETER 2 registers with the 16-bit binary number N, which is calculated using the following expression:

$$N = 2^{16} - T(int)/21.333E\text{-}6$$

After the low and high bytes representing N are loaded into the PARAMETER 1 and PARAMETER 2 registers respectively, execute the EIS command. Once this command is executed, the externally loaded integration time can be used via the CNVP or SDI commands.

RESA 01101000

RESA (REStore All) restores all configuration parameters (default integration time, default calibration time, data format, EIS/ELS period, NULL value and electronic calibration data) from nonvolatile memory. After executing this function, all parameters will be restored to their last value as saved by the SAVA command.

SAVA 01001000

SAVA (SAVe All) saves all programmable attributes (default integration time, default calibration time, data format, EIS/ELS period, NULL value and electronic calibration data) into nonvolatile memory.

SDI $00111C_2C_1C_0$

SDI (Set Default Integration time) sets the default integration time to one of the eight preset times listed in Figure 10. The three-bit code for the desired integration time is embedded in the lowest three bits of the command code.

SDF 00110000

SDF (Set Default Format) sets the default data format according to the five bit code loaded into the PARAMETER 1 register prior to execution of this command. The table in Figure 8 illustrates the construction of the five bit code according to the desired data format and resolution.

SCAL 11000000

SCAL (Single CALibration) performs a single background calibration cycle. This command is intended for use when automatic background calibration has been disabled via the CALDI command.

SDC $01000C_2C_1C_0$

SDC (Set Default Calibration time) sets the default calibration time (Tcal) according to the three bit code embedded in the lowest three bits of the command. The calibration times are shown in Figure 10. Note that the actual duration of a calibration cycle is approximately $2 \times T(cal) + 9$ milliseconds.

WRNV $10011A_2A_1A_0$

WRNV (WRite NonVolatile) writes the user supplied data, in the PARAMETER 1 and PARAMETER 2 registers, into the user accessible area of the AD1170's nonvolatile memory. Eight words of this memory are available, and are addressed by the lowest three bits of the command.

RDNV $10100A_2A_1A_0$

RDNV (ReaD NonVolatile) reads one word from the user accessible portion of the nonvolatile memory within the AD1170, and places the data into the LOW DATA and MID DATA registers for retrieval by the user. The address of the desired word is embedded into the lowest three bits of the command.

RST 10010000

RST (ReSeT) is effectively equivalent to a hardware reset of the AD1170. After executing this command, all nonvolatile parameters (including the ECAL coefficient, the default integration and calibration periods, EIS/ELS period, NULL value and the default format) will be restored to their last saved values, automatic calibration will be enabled, and NULL will be disabled.

NULL 01110000

NULL measures the input signal (using the curent integration time value) and stores the measurement in internal RAM. It allows the user to establish the value of offset voltage at the input and subtract that offset from subsequent conversions through the execution of the NULEN command. The user must insure that the sum of the offset value plus the full scale input is less than the ± 6 volts linear input range of the AD1170. Ideally the offset value to be nulled should be no more than a few hundred millivolts in amplitude. The value measured by the NULL command is saved and restored by the SAVA and RESA commands – maintaining this value through subsequent powerups. The NULL command need only be invoked when a new null measurement is desired.

NULEN 01111000

NULEN (NULl ENable) subtracts the value, measured and stored by the last NULL command, from all subsequent conversions. When NULEN is in effect, each conversion's length will be extended by approximately 700 microseconds.

NULDI 10000000

NULDI (NULl DIsable) cancels the effect of the NULEN command.

[1]This logic signal should be a TTL or CMOS compatible continuous waveform. It need not be symmetrical, but the HIGH or LOW time should not be less than 25 microseconds.

IBM PC INTERFACE

Figure 12 is an example of an AD1170/IBM interface suitable for the IBM PC or XT personal computers. In this case, the AD1170 is interfaced in the I/O space; the DIP switch controls the specific location of the AD1170 within the available address space.

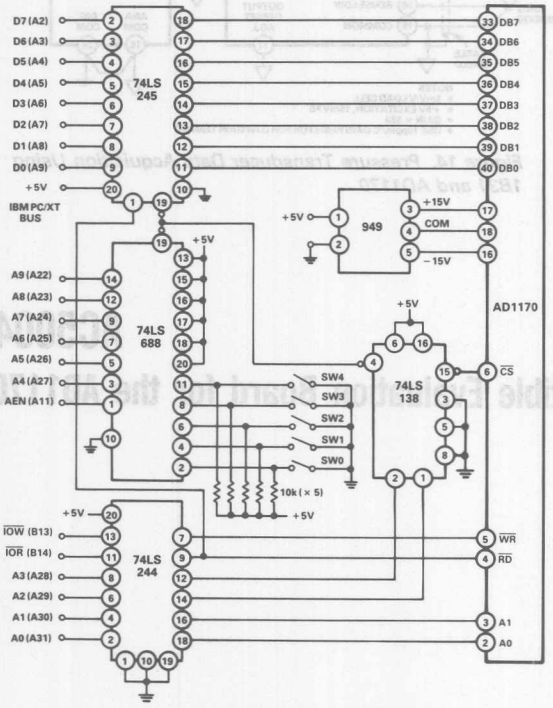


Figure 12. IBM PC/XT to AD1170 Interface

INTERFACING TO AN 8051 MICROCONTROLLER

Figure 13 shows how an AD1170 may be interfaced to an 8051 microcontroller using a technique commonly called "byte banging", where the control lines and data bus of a device are manipulated under firmware control. This "byte banging" technique can be adapted to most microprocessors and is useful in situations where a conventional bus structure is either nonexistent or unavailable for use.[1]

The AD1170's data bus is connected to the 8051 using I/O lines P2.0 through P2.7. The address lines A0 and A1 are connected to I/O lines P1.0 and P1.1 respectively. The RD/ and WR/ lines are connected to P1.2 and P1.3. The CS/ line of the AD1170 is grounded when it is the only device connected to the 8051, but multiple AD1170s could easily be connected in the same way if each CS/ line were separately controlled.

[1]Note that the 8051 microcontroller *does* contain a conventional bus structure; the "byte banging" interface shown here is presented as an example of an alternative technique.

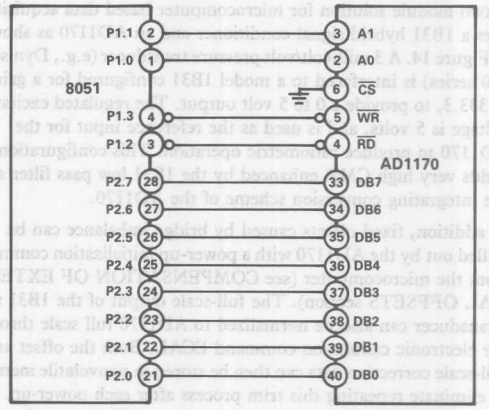


Figure 13. Simple 8051 to AD1170 Interface

To initialize the interface, first write "1"s to the port pins connected to the data bus and the RD/ and WR/ control lines. This puts the 8051 I/O lines into a lightly "pulled up" state, simulating a tri-stated condition on the bus to insure that neither RD/ or WR/ are selected:

```
INIT:   SETB  P1.2      ;DISABLE RD/
        SETB  P1.3      ;AND WR/
                        ;
        MOV   P2, #OFFH ;SET P2 TO ALL ONES
```

To write a command to the AD1170, first set the state of the P1.1 and P1.0 lines for the address corresponding to the byte to be written to. Set the P2 port to the command data, then strobe the WR/ line by first clearing the P1.3 line and then setting it:

```
WRCMD:  CLR   P1.0      ;FIRST CLEAR A0 AND A1
        CLR   P1.1      ;TO POINT TO CMD BYTE
                        ;
        MOV   P2, #CNV  ;CNV IS THE OPCODE FOR
                        ;A SINGLE CONVERSION
                        ;
        CLR   P1.3      ;STROBE THE WR/ LINE
        SETB  P1.3      ;ONE TIME
                        ;
        MOV   P2, #OFFH ;CLEAR DATA BUS TO
                        ;ALL ONES
```

To read a byte from the AD1170, first set the P1.0 and P1.1 lines to point to the address of the byte desired. Bring the RD/ line low, reading the contents of P2. Return the RD/ line high:

```
RDSTAT: CLR   P1.0      ;POINT TO STATUS BYTE
        CLR   P1.1      ;
                        ;
        CLR   P1.2      ;BRING RD/ LINE LOW
        MOV   A,P2      ;READ CONTENTS OF BUS
        SETB  P1.2      ;RESTORE RD/ LINE HIGH
```

in Figure 14. A 3 millivolt/volt pressure transducer (e.g., Dynisco's 800 series) is interfaced to a model 1B31 configured for a gain of 333.3, to provide a 0 to 5 volt output. The regulated excitation voltage is 5 volts, and is used as the reference input for the AD1170 to produce ratiometric operation. This configuration yields very high CMR enhanced by the 1B31 low pass filter and the integrating conversion scheme of the AD1170.

In addition, fixed offsets caused by bridge imbalance can be nulled out by the AD1170 with a power-up initialization command from the microcomputer (see COMPENSATION OF EXTERNAL OFFSETS section). The full-scale output of the 1B31 and Transducer can also be normalized to AD1170 full scale through the electronic calibration command ECAL. Both the offset and full-scale correction data can then be stored in nonvolatile memory to eliminate repeating this trim process after each power-up. The AD1170 eliminates a potentiometer or software overhead which might otherwise be needed for these functions.

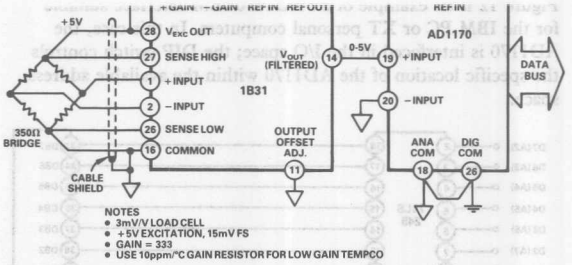


Figure 14. Pressure Transducer Data Acquisition Using 1B31 and AD1170

AC5004

. . . an IBM PC/XT/AT Compatible Evaluation Board for the AD1170

FEATURES

Compatible to the IBM PC/XT/AT or Equivalent
Menu-Driven Demonstration Software
Input Mating Connector
Full Documentation
Example Listings of BASIC Programs
Schematic
Assembly Drawing
Complete Set of Tools to Evaluate an AD1170 A/D Converter

GENERAL DESCRIPTION

The AC5004 was designed as a support tool to enable the user to easily and quickly evaluate Analog Devices' AD1170 high-resolution programmable integrating A/D converter. The AD1170 is inserted directly into an AC5004 board which is designed to plug into the backplane of an IBM PC/XT/AT. Thus, armed with an IBM PC, an AD1170, and an AC5004 evaluation board, the user is fully prepared to examine the operation of the AD1170.

A User's Manual provides all the information required to put the AC5004/AD1170 evaluation process into operation. In the manual are full descriptions of the AC5004 memory address and power source selection jumpers as well as a schematic documenting the interface of the AD1170 to a computer bus.

The package also contains a comprehensive demonstration program written in BASIC that completely exercises all the functions of the AD1170. The AC5004 is an accessory that will make readily available to the user all the tools needed to comprehensively test the AD1170.

PRODUCT HIGHLIGHTS

1. AC5004 plugs directly into IBM PC/XT/AT or compatibles. Standard short slot card size (5 7/8″ × 5″ × 1″).
2. The AC5004 enables the user to evaluate the AD1170 high-resolution, programmable, integrating A/D converter without having to build a bread-board or prototype.
3. The evaluation boards come complete with software and programming examples designed to exercise all of the AD1170's functions.
4. AC5004 schematic and assembly drawings are provided to be used as examples of how to interface the AD1170 to a microprocessor bus.

Please note:
Order *AC5004* (does not include AD1170).

Complete, High Speed 16-Bit A/D Converters

AD1376/AD1377

FEATURES

Complete 16-Bit Converters with Reference and Clock
±0.003% Maximum Nonlinearity
No Missing Codes to 14 Bits over Temperature
Fast Conversion
17 μs to 16 Bits (AD1376)
10 μs to 16 Bits (AD1377)
Short Cycle Capability
Adjustable Clock Rate
Parallel and Serial Outputs
Low Power: 645 mW Typical (AD1376)
585 mW Typical (AD1377)
Industry Standard Pin Out

PRODUCT DESCRIPTION

The AD1376 and AD1377 are high resolution, 16-bit analog-to-digital converters with internal reference, clock and laser-trimmed thin-film applications resistors. They are packaged in compact 32-pin, ceramic seam sealed (hermetic) dual-in-line packages (DIPs). Thin-film scaling resistors provide bipolar input ranges of ±2.5 V, ±5 V, ±10 V and unipolar input ranges of 0 to +5 V, 0 to +10 V, and 0 to +20 V.

Digital output data is provided in parallel and serial form with corresponding Clock and Status outputs. All digital inputs and outputs are TTL compatible.

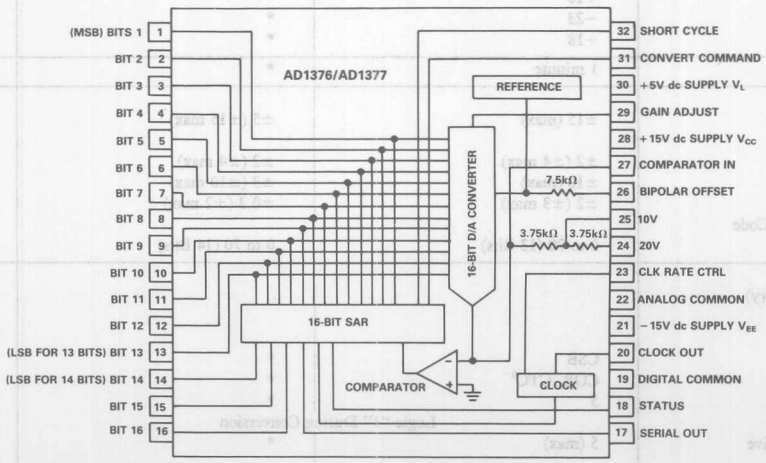
APPLICATIONS

The AD1376 and AD1377 are excellent for use in high resolution applications requiring moderate speed and high accuracy or stability over commercial (0°C to +70°C) temperature ranges. For extended temperature ranges, the pin compatible AD1378 is recommended. Typical applications include medical and analytic instrumentation, precision measurement for industrial robotics, automatic test equipment (ATE), and multichannel data acquisition systems, servo control systems, or anywhere wide dynamic range is required. A proprietary monolithic DAC and laser-trimmed thin-film resistors guarantee a maximum nonlinearity of ±0.003% (1/2 LSB_{14}.) The converters may be short cycled to achieve faster conversion times—15 μs to 14 bits for the AD1376, or 8 μs to 14 bits for the AD1377.

PRODUCT HIGHLIGHTS

1. The AD1376 and AD1377 provide 16-bit resolution with a maximum linearity error of ±0.003% (1/2 LSB_{14}) at +25°C.
2. AD1376 conversion time is 14 μs (typical) short cycled to 14 bits, and 16 μs to 16 bits.
3. AD1377 conversion time is 8 μs (typical) short cycled to 14 bits, and 9 μs to 16 bits.
4. Two binary codes are available on the digital output. They are CSB (Complementary Straight Binary) for unipolar input voltage ranges and COB (Complementary Offset Binary) for bipolar input ranges. Complementary Twos Complement (CTC) coding may be obtained by inverting Pin 1 (MSB).
5. The AD1376 and AD1377 include internal reference and clock, with external clock rate adjust pin, and serial and parallel digital outputs.

FUNCTIONAL BLOCK DIAGRAM



AD1376/AD1377–SPECIFICATIONS (typical at T_A = +25°C, V_S = ±15, +5 V unless otherwise noted)

Model	AD1376JD/AD1377JD	AD1376KD/AD1377KD	Units
RESOLUTION	16 (max)	*	Bits
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±2.5, ±5, ±10	*	Volts
Unipolar	0 to +5, 0 to +10, 0 to +20	*	Volts
Impedance (Direct Input)			
0 to +5 V, ±2.5 V	1.88	*	kΩ
0 to +10 V, ±5.0 V	3.75	*	kΩ
0 to +20 V, ±10 V	7.50	*	kΩ
DIGITAL INPUTS[1]			
Convert Command	Positive Pulse 50 ns Wide (min) Trailing Edge Initiates Conversion		
Logic Loading	1	*	LSTTL Load
TRANSFER CHARACTERISTICS[2]			
ACCURACY			
Gain Error	±0.05[3] (±0.2 max)	*	%
Offset Error			
Unipolar	±0.05[3] (±0.1 max)	*	% of FSR[4]
Bipolar	±0.05[3] (±0.2 max)	*	% of FSR
Linearity Error (max)	±0.006	±0.003	% of FSR
Inherent Quantization Error	±1/2	*	LSB
Differential Linearity Error	±0.003	*	% of FSR
POWER SUPPLY SENSITIVITY			
±15 V dc (±0.75 V)	0.0015	*	% of FSR/% ΔV_S
+5 V dc (±0.25 V)	0.001	*	% of FSR/% ΔV_S
CONVERSION TIME[5]			
12 Bits (AD1376)	11.5 (13 max)	*	µs
14 Bits (AD1376)	13.5 (15 max)	*	µs
16 Bits (AD1376)	15.5 (17 max)	*	µs
14 Bits (AD1377)	8.75 (max)	*	µs
16 Bits (AD1377)	10 (max)	*	µs
POWER SUPPLY REQUIREMENTS			
Rated Voltage, Analog	±15, ±0.5 (max)	*	V dc
Rated Voltage, Digital	+5, ±0.25 (max)	*	V dc
AD1376 Power Consumption	645 (800 max)	*	mW
+15 V Supply Drain	+16	*	mA
−15 V Supply Drain	−21	*	mA
+5 V Supply Drain	+18	*	mA
AD1377 Power Consumption	600 (800 max)	*	mW
+15 V Supply Drain	+10	*	mA
−15 V Supply Drain	−23	*	mA
+5 V Supply Drain	+18	*	mA
WARM-UP TIME	1 minute	*	Minutes
DRIFT[6]			
Gain	±15 (max)	±5 (±15 max)	ppm/°C
Offset			
Unipolar	±2 (±4 max)	±2 (±4 max)	ppm of FSR/°C
Bipolar	±10 (max)	±3 (±10 max)	ppm of FSR/°C
Linearity	±2 (±3 max)	±0.3 (±2 max)	ppm of FSR/°C
Guaranteed No Missing Code			
Temperature Range	0 to 70 (13 Bits)	0 to 70 (14 Bits)	°C
DIGITAL OUTPUT[1]			
(All Codes Complementary)			
Parallel & Serial			
Output Codes[7]			
Unipolar	CSB	*	
Bipolar	COB, CTC[8]	*	
Output Drive	5	*	LSTTL Loads
Status	Logic "1" During Conversion		
Status Output Drive	5 (max)	*	LSTTL Loads
Internal Clock[9]			
Clock Output Drive	5 (max)	*	LSTTL Loads
Frequency	1040/1750	*	kHz

Specification	0 to +70	*	°C
Operating	−25 to +85	*	°C
Storage	−55 to +125	*	°C

NOTES
[1]Logic "0" = 0.8 V, max. Logic "1" = 2.0 V, min for inputs. For digital outputs Logic "0" = +0.4 V max. Logic "1" = 2.4 V min.
[2]Tested on ±10 V and 0 to +10 V ranges.
[3]Adjustable to zero.
[4]Full-Scale Range.
[5]Conversion time may be shortened with "Short Cycle" set for lower resolution.
[6]Guaranteed but not 100% production tested.
[7]CSB–Complementary Straight Binary. COB–Complementary Offset Binary. CTC–Complementary Twos Complement.
[8]CTC coding obtained by inverting MSB (Pin 1).
[9]With Pin 23, clock rate controls tied to digital ground.
*Specifications same as AD1376JD/AD1377JD.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18 V
Logic Supply Voltage . . . . . +7 V
Analog Inputs (Pins 24 and 25) . . . . . ±25 V
Analog Ground to Digital Ground . . . . . ±0.3 V
Digital Inputs . . . . . −0.3 V to V_{DD} + 0.3 V
Junction Temperature . . . . . +175°C
Storage . . . . . +150°C
Lead Temperature (10 seconds) . . . . . +300°C

ORDERING GUIDE

Model	Temperature Range	Maximum Linearity Error	Conversion Time (16 Bits)	Package Option*
AD1376JD	0°C to +70°C	±0.006%	17 µs	DH-32E
AD1376KD	0°C to +70°C	±0.003%	17 µs	DH-32E
AD1377JD	0°C to +70°C	±0.006%	10 µs	DH-32E
AD1377KD	0°C to +70°C	±0.003%	10 µs	DH-32E

*DH-32E = Ceramic DIP. For outline information see Package Information section.

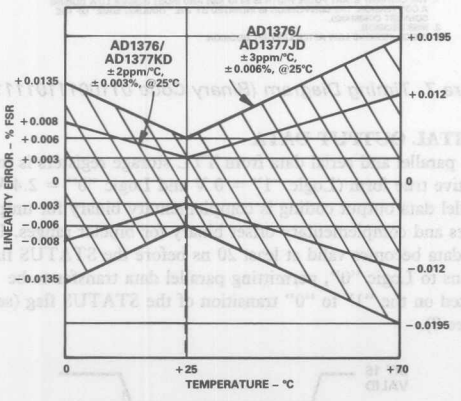


Figure 1. Linearity Error vs. Temperature

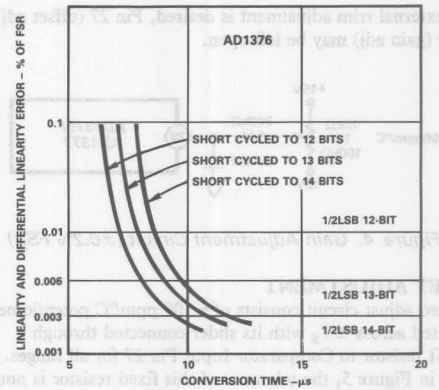


Figure 2. AD1376 Nonlinearity vs. Conversion Time

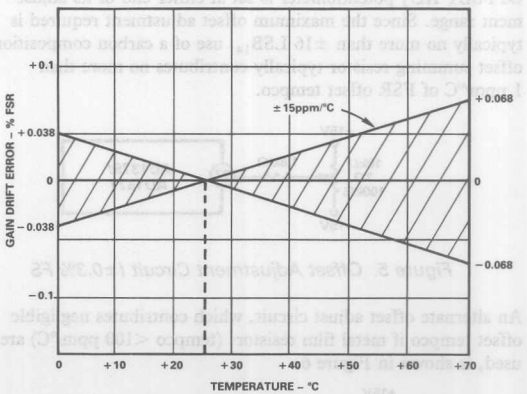


Figure 3. Gain Drift Error vs. Temperature

DESCRIPTION OF OPERATION

On receipt of a CONVERT START command, the AD1376 or AD1377 converts the voltage at its analog input into an equivalent 16-bit binary number. This conversion is accomplished as follows: the 16-bit successive-approximation register (SAR) has its 16-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

GAIN ADJUSTMENT

The gain adjust circuit consists of a 100 ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 300 kΩ resistor to the gain adjust Pin 29 as shown in Figure 4.

If no external trim adjustment is desired, Pin 27 (offset adj) and Pin 29 (gain adj) may be left open.

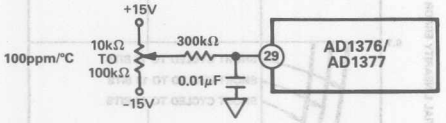


Figure 4. Gain Adjustment Circuit (±0.2% FSR)

OFFSET ADJUSTMENT

The zero adjust circuit consists of a 100 ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 1.8 MΩ resistor to Comparator Input Pin 27 for all ranges. As shown in Figure 5, the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a −1200 ppm/°C tempco contributes a worst-case offset tempco of 32 LSB_{14} × 61 ppm/LSB_{14} × 1200 ppm/°C = 2.3 ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±16 LSB_{14}, use of a carbon composition offset summing resistor typically contributes no more than 1 ppm/°C of FSR offset tempco.

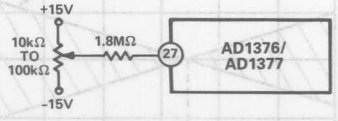


Figure 5. Offset Adjustment Circuit (±0.3% FS

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 6.

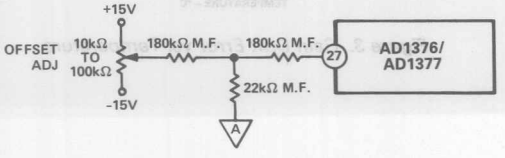


Figure 6. Low Tempco Zero Adjustment Circuit

In either adjust circuit, the fixed resistor connected to Pin 27 should be located close to this pin to keep the pin connection runs short. Comparator Input Pin 27 is quite sensitive to external noise pick-up and should be guarded by analog common.

TIMING

The timing diagram is shown in Figure 7. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 17 cycles. All the SAR parallel bits, STATUS flip-flops, and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 – B_{16} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is reset unconditionally. This sequence continues until the Bit 16 (LSB) decision (keep) is made at t_{16}. The STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the low Logic "0" state. Note that the clock remains low until the next conversion.

Corresponding parallel data bits become valid on the same positive-going clock edge.

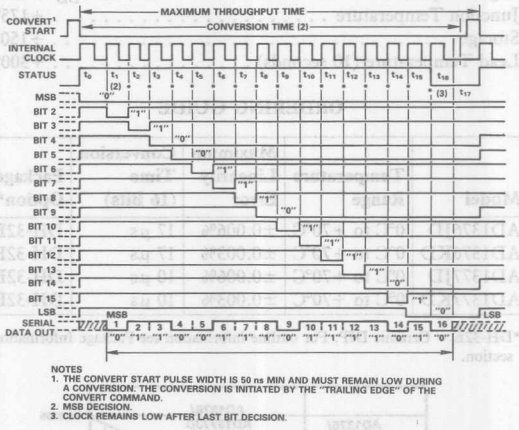


Figure 7. Timing Diagram (Binary Code 0110011101111010)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers is in negative true form (Logic "1" = 0 V and Logic "0" = 2.4 V). Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Parallel data becomes valid at least 20 ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag (see Figure 8).

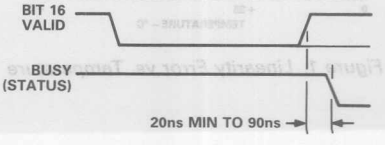


Figure 8. LSB Valid to Status Low

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (nonreturn-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 120 ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on the negative-going clock edges as shown in Figure 9. There are 17 negative-going clock edges in the complete 16-bit conversion cycle. The first negative edge shifts an invalid bit into the register, which is shifted out on the last negative-going clock edge.

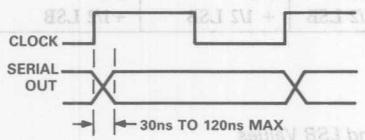


Figure 9. Clock High to Serial Out Valid

All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

Short Cycle Input: A Short Cycle Input, Pin 32, permits the timing cycle shown in Figure 7 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 16-bit resolution. When 10-bit resolution is desired, Pin 32 is connected to Bit 11 output Pin 11. The conversion cycle then terminates and the STATUS flag resets after the Bit 10 decision (timing diagram of Figure 7). Short cycle connections and associated 8-, 10-, 12-, 13-, 14-, and 15-bit conversion times are summarized in Table I, for a 1.6 MHz clock (AD1377) or 933 kHz clock (AD1376).

INPUT SCALING

The ADC inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 10 for circuit details.

Table I. Short Cycle Connections

Resolution Bits	Resolution (% FSR)	Maximum Conversion Time–μs (AD1377)	Maximum Conversion Time–μs (AD1376)	Status Flag Reset	Connect Short Cycle Pin 32 to Pin:
16	0.0015	10	17.1	t_{16}	N/C (Open)
15	0.003	9.4	16.1	t_{15}	16
14	0.006	8.7	15.0	t_{14}	15
13	0.012	8.1	13.9	t_{13}	14
12	0.024	7.5	12.9	t_{12}	13
10	0.100	6.3	10.7	t_{10}	11
8	0.390	5.0	8.6	t_{8}	9

Table II. Input Scaling Connections

Input Signal Line	Output Code	Connect Pin 26 to Pin	Connect Pin 24 to	Connect Input Signal to
±10 V	COB	27	Input Signal	24
±5 V	COB	27	Open	25
±2.5 V	COB	27	Pin 27	25
0 V to +5 V	CSB	22	Pin 27	25
0 V to +10 V	CSB	22	Open	25
0 V to +20 V	CSB	22	Input Signal	24

Note: Pin 27 is extremely sensitive to noise and should be guarded by analog common.

Table III. Transition Values vs. Calibration Codes

Code Under Test MSB	LSB	Range	Low Side Transition Values ±10 V	±5 V	±2.5 V	0 V to +10 V	0 V to +5 V
000 . . .	000*	+ Full Scale	+10 V −3/2 LSB	+5 V −3/2 LSB	+2.5 V −3/2 LSB	+10 V −3/2 LSB	+5 V −3/2 LSB
011 . . .	111	Mid Scale	0–1/2 LSB	0–1/2 LSB	0–1/2 LSB	+5 V–1/2 LSB	+2.5 V–1/2 LSB
111 . . .	110	− Full Scale	−10 V +1/2 LSB	−5 V +1/2 LSB	−2.5 V +1/2 LSB	0 V + 1/2 LSB	0 V +1/2 LSB

*Voltages given are the nominal value for transition to the code specified.
Note: For LSB value for range and resolution used, see Table IV.

Table IV. Input Voltage Range and LSB Values

Analog Input Voltage Range	±10 V	±5 V	±2.5 V	0 V to +10 V	0 V to +5 V	
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	FSR / 2^n	20 V / 2^n	10 V / 2^n	5 V / 2^n	10 V / 2^n	5 V / 2^n
	n = 8	78.13 mV	39.06 mV	19.53 mV	39.06 mV	19.53 mV
	n = 10	19.53 mV	9.77 mV	4.88 mV	9.77 mV	4.88 mV
	n = 12	4.88 mV	2.44 mV	1.22 mV	2.44 mV	1.22 mV
	n = 13	2.44 mV	1.22 mV	0.61 mV	1.22 mV	0.61 mV
	n = 14	1.22 mV	0.61 mV	0.31 mV	0.61 mV	0.31 mV
	n = 15	0.61 mV	0.31 mV	0.15 mV	0.31 mV	0.15 mV

NOTES
*COB = Complementary Offset Binary.
**CTC = Complementary Twos Complement — achieved by using an inverter to complement the most significant bit to product ($\overline{MSB}$).
***CSB = Complementary Straight Binary.

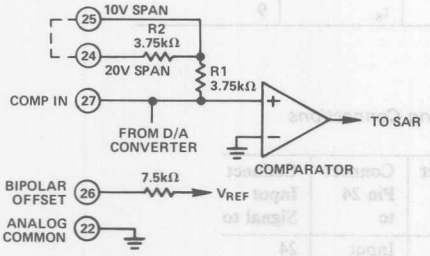


Figure 10. Input Scaling Circuit

Zero is now calibrated. Set analog input to +FSR − 2 LSB = + 9.99878 V. Adjust Gain for 00000000000001 digital output code; full scale (Gain) is now calibrated. Half scale calibration check: set analog input to +5.00000 V; digital output code should be 01111111111111.

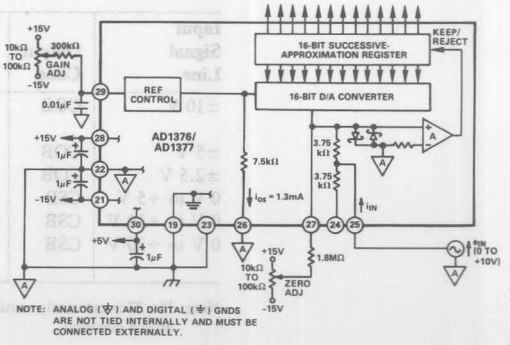


Figure 11. Analog and Power Connections for Unipolar 0 V to +10 V Input Range

CALIBRATION

(14-Bit Resolution Examples)

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 11 and 12, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and −FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 V to + 10 V Range: Set analog input to + 1 LSB_{14} = 0.00061 V. Adjust Zero for digital output = 11111111111110.

−10 V to +10 V Range: Set analog input to −9.99878 V; adjust zero for 1111111111110 digital output (complementary offset binary) code. Set analog input to 9.99756 V; adjust Gain for 00000000000001 digital output (complementary offset binary) code. Half scale calibration check: set analog input to 0.00000 V; digital output (complementary offset binary) code should be 01111111111111.

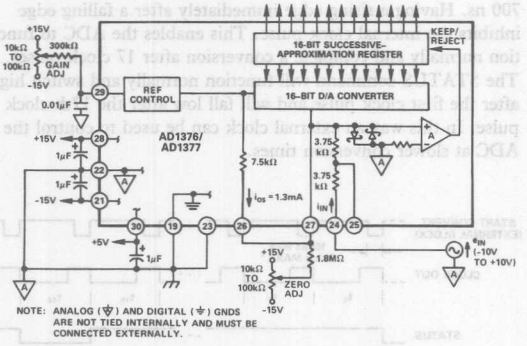


Figure 12. Analog and Power Connections for Bipolar +10 V to +10 V Input Range

Other Ranges: Representative digital coding for 0 V to +10 V and −10 V to +10 V ranges is given above. Coding relationships and calibration points for 0 V to +5 V, −2.5 V to +2.5 V and −5 V to +5 V ranges can be found by halving proportionally the corresponding code equivalents listed for the 0 V to +10 V and −10 V to +10 V ranges, respectively, as indicated in Table III.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/2 LSB using the static adjustment procedure described above. By summing a small sine or triangular wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in *Analog-Digital Conversion Handbook* , edited by D. H. Sheingold, Prentice-Hall, Inc., 1986.

GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return) and Analog Signal Ground. These grounds (Pins 19 and 22) must be tied together at one point for the ADC as close as possible to the converter. Ideally, a single solid analog ground plane under the converter would be desirable. Current flows through the wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system analog ground point and the ground pins of the ADC. Separate wide conductor stripe ground returns should be provided for high resolution converters to minimize noise and IR losses from the current flow in the path from the converter to the system ground point. In this way ADC supply currents and other digital logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the ADC supply terminals should be capacitively decoupled as close to the ADC as possible. A large value capacitor such as 1 μF in parallel with a 0.1 μF capacitor is usually sufficient. Analog supplies are to be bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

The metal cover is internally grounded with respect to the power supplies, grounds and electrical signals. Do not externally ground the cover.

CLOCK RATE CONTROL

The AD1376 and AD1377 may be operated at faster conversion times by connecting the Clock Rate Control (Pin 23) to an external multiturn trim potentiometer (TCR <100 ppm/°C) as shown in Figure 13.

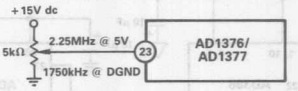


Figure 13. Clock Rate Control Circuit. AD1376 Clock Frequencies are 1.4 MHz (+5 V) and 1040 kHz (DGND).

HIGH RESOLUTION DATA ACQUISITION SYSTEM

The essential details of a high resolution data acquisition system using the AD386 and AD1376 or AD1377 are shown in Figure 14. Conversion is initiated by the falling edge of the CONVERT START pulse. This edge drives the AD1376's or AD1377's STATUS line high. The inverter then drives the AD386 into hold mode. STATUS remains high throughout the conversion and returns low once the conversion is completed. This allows the AD386 to reenter track mode.

This circuit can exhibit nonlinearities arising from transients produced at the A/D's input by the falling edge of CONVERT-START. This edge resets the A/D's internal DAC; the resulting transient depends on the SHA's present output voltage and the A/D's prior conversion result. In the circuit of Figure 14 the falling edge of CONVERT-START also places the SHA into hold mode (via the A/D's STATUS output), causing the reset transient to occur at the same moment as the SHA's track-and-hold transition. Timing skews and capacitive coupling can cause some of the transient signal to add to the signal being acquired by the SHA, introducing nonlinearity.

A much safer approach is to add a flip flop as shown in Figure 15. The rising edge of CONVERT START places the T/H into hold mode before the A/D reset transients begin. The falling edge of STATUS places the AD386 back into track mode. System throughput will be reduced if a long CONVERT START pulse is used. Throughput can be calculated from

$$Throughput = \frac{1}{T_{ACQ} + T_{CONV} + T_{CS}}$$

where T_{ACQ} is the T/H acquisition time, T_{CONV} is the time required for the A/D conversion, and T_{CS} is the duration of CONVERT START. The combination of the AD1376 and AD386

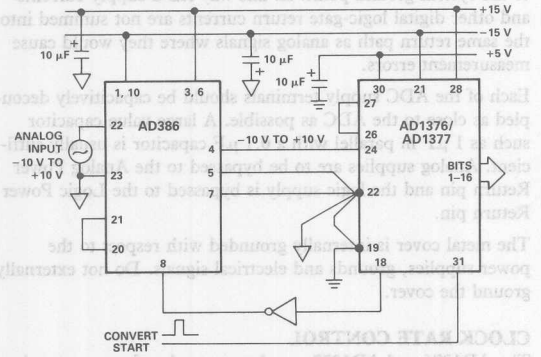


Figure 14. Basic Data Acquisition System Interconnections

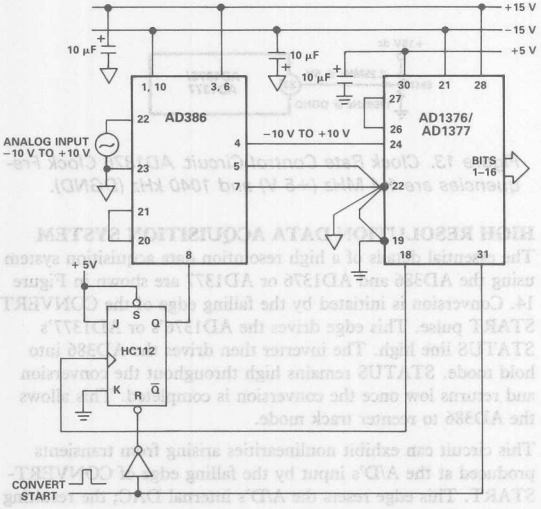


Figure 15. Improved Data Acquisition System

will provide greater than 50 kHz throughput. No significant T/H droop error will be introduced provided the width of CONVERT START is small compared with the A/D's conversion time.

Using the AD1376 or AD1377 at Slower Conversion Times

The user may wish to run the ADC at slower conversion times in order to synchronize the A/D with an external clock. This is accomplished by running a slower clock than the internal clock into the START CONVERT input. This clock must consist of narrow negative-going clock pulses, as seen in Figure 16. The pulse must be a minimum of 100 ns wide but not greater than 700 ns. Having a rising edge immediately after a falling edge inhibits the internal clock pulse. This enables the ADC to function normally and complete a conversion after 17 clock pulses. The STATUS command will function normally and switch high after the first clock pulse and will fall low after the 17th clock pulse. In this way an external clock can be used to control the ADC at slower conversion times.

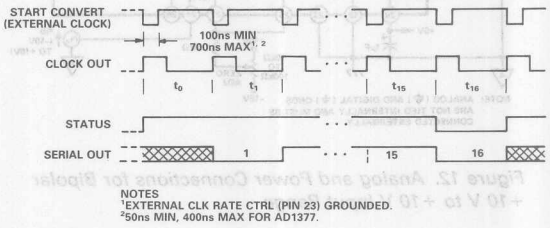


Figure 16. Timing Diagram for Use with an External Clock

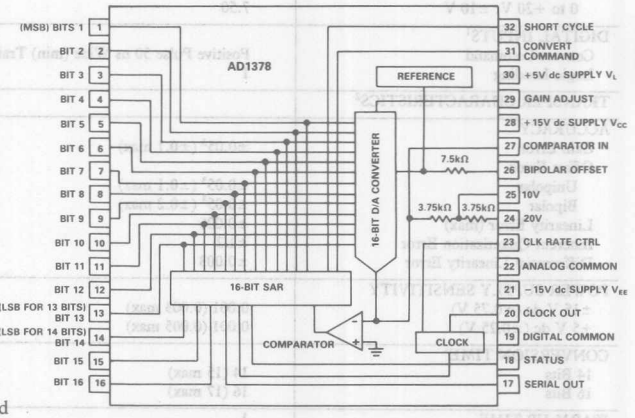
Complete, Wide Temperature 16-Bit A/D Converter

AD1378

FEATURES

Complete 16-Bit Converter with Reference and Clock
±0.003% Maximum Nonlinearity Over Temperature
Available with MIL-STD-883 Screening
Fast Conversion – 17 μs Maximum (16 Bit)
Short Cycle Capability
Parallel and Serial Outputs
Low Power: 800 mW Maximum
Industry Standard Pin Out
Specified Over Military Temperature Range

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1378 is a high resolution 16-bit hybrid IC analog-to-digital converter including reference, clock and laser-trimmed thin-film components. It is packaged in a compact 32-pin, ceramic DIP. The thin-film scaling resistors allow analog input ranges of ±2.5 V, ±5 V, ±10 V, 0 to +5 V, 0 to +10 V, and 0 to +20 V.

Important performance characteristics of the devices are maximum linearity error of ±0.003% of FSR, and maximum 14-bit conversion time of 15 μs. This performance is due to innovative design and the use of proprietary monolithic D/A converter chips. Laser-trimmed thin-film resistors provide the linearity and wide temperature range for no missing codes.

The AD1378 provides data in parallel and serial form with corresponding clock and status outputs. All digital inputs and outputs are TTL compatible.

APPLICATIONS

The AD1378 is excellent for use in applications requiring 14-bit accuracy over extended temperature ranges. Typical applications include multichannel data acquisition systems, servo control systems and anywhere that excellent stability and wide dynamic range in the smallest space is required. The device may be short cycled to achieve 14-bit conversions in 15 μs.

PRODUCT HIGHLIGHTS

1. The AD1378 provides 16-bit resolution with maximum linearity error less than ±0.003% (±0.006% for S grade) at +25°C.
2. Conversion time is 14 μs typical to 14 bits with short cycle capability, and 16 μs to 16 bits.
3. Two binary codes are available on the AD1378 output. They are complementary straight binary (CSB) for unipolar input voltage ranges and complementary offset binary (COB) for bipolar input ranges. Complementary twos complement (CTC) coding may be obtained by inverting Pin 1 (MSB).
4. The proprietary ICs used in this hybrid design provide excellent stability over temperature and lower chip count for improved reliability.
5. The AD1378 includes an internal reference and clock, with external clock adjust pin, and a serial output.

AD1378—SPECIFICATIONS (typical at T_A = +25°C, V_S = ±15, +5 V unless otherwise noted)

Model	AD1378SD	AD1378TD	Units
RESOLUTION	16 (max)	*	Bits
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±2.5, ±5, ±10	*	Volts
Unipolar	0 to +5, 0 to +10, 0 to +20	*	Volts
Impedance (Direct Input)			
0 to +5 V, ±2.5 V	1.88	*	kΩ
0 to +10 V, ±5.0 V	3.75	*	kΩ
0 to +20 V, ±10 V	7.50	*	kΩ
DIGITAL INPUTS[1]			
Convert Command	Positive Pulse 50 ns Wide (min) Trailing Edge Initiates Conversion		
Logic Loading	1	*	LS TTL Load
TRANSFER CHARACTERISTICS[2]			
ACCURACY			
Gain Error	±0.05[3] (±0.1 max)	*	%
Offset Error			
Unipolar	±0.05[3] (±0.1 max)	*	% of FSR[4]
Bipolar	±0.05[3] (±0.2 max)	*	% of FSR
Linearity Error (max)	±0.006	±0.003	% of FSR
Inherent Quantization Error	±1/2	*	LSB
Differential Linearity Error	±0.003	*	% of FSR
POWER SUPPLY SENSITIVITY			
±15 V dc (±0.75 V)	0.001 (0.003 max)	*	% of FSR/% ΔV_S
+5 V dc (±0.25 V)	0.001 (0.005 max)	*	% of FSR/% ΔV_S
CONVERSION TIME[5]			
14 Bits	14 (15 max)	*	µs
16 Bits	16 (17 max)	*	µs
WARM-UP TIME	1	*	Minutes
DRIFT			
Gain	±15 (max)	±5 (±15 max)	ppm/°C
Offset			
Unipolar	±2 (±4 max)	±2 (±4 max)	ppm of FSR/°C
Bipolar	±10 (max)	±3 (±10 max)	ppm of FSR/°C
Linearity	±2 (3 max)	±0.3 (2 max)	ppm of FSR/°C
Guaranteed No Missing Code			
Temperature Range	−55 to +125 (13 Bits)	−55 to +125 (14 Bits)	°C
DIGITAL OUTPUT[1]			
(All Codes Complementary)			
Parallel & Serial			
Output Codes[6]			
Unipolar	CSB	*	
Bipolar	COB, CTC[7]	*	
Output Drive	5	*	LSTTL Loads
Status	Logic "1" During Conversion	*	
Status Output Drive	5 (max)	*	LSTTL Loads
Internal Clock[8]			
Clock Output Drive	5 (max)	*	LSTTL Loads
Frequency	1040	*	kHz
POWER SUPPLY REQUIREMENTS			
Power Consumption	645 (800 max)	*	mW
Rated Voltage, Analog	±15 ±0.75 (max)	*	V dc
Rated Voltage, Digital	+5 ±0.25 (max)	*	V dc
Supply Drain +15 V dc	+25 (max)	*	mA
Supply Drain −15 V dc	−40 (max)	*	mA
Supply Drain +5 V dc	+25 (max)	*	mA
TEMPERATURE RANGE			
Specification	−55 to +125	*	°C
Storage	−65 to +150	*	°C

NOTES

[1]Logic "0" = 0.8 V, max. Logic "1" = 2.0 V, min for inputs. For digital outputs Logic "0" = +0.4 V max. Logic "1" = 2.7 V min.

[2]Tested on ±10 V and 0 to +10 V ranges.

[3]Adjustable to zero.

[4]Full-Scale Range.

[5]Conversion time may be shortened with "Short Cycle" set for lower resolution.

[6]CSB – Complementary Straight Binary. COB – Complementary Offset Binary. CTC – Complementary Twos Complement.

[7]CTC coding obtained by inverting MSB (Pin 1).

[8]With Pin 23, clock rate controls tied to digital ground.

*Specifications same as AD1378SD.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . ±18 V
Logic Supply Voltage . . . . . +7 V
Analog Inputs (Pins 24 & 25) . . . . . ±25 V
Digital Inputs . . . . . +5.5 V
Junction Temperature . . . . . +175°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Max Linearity Error	Temperature Range	Package Option*
AD1378SD	0.006% FSR	−55°C to +125°C	Ceramic DH-32E
AD1378TD	0.003% FSR	−55°C to +125°C	Ceramic DH-32E

*DH-32E = Bottom Brazed Ceramic DIP. For outline information see Package Information section.

2

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



THEORY OF OPERATION

A 16-bit conversion A/D converter partitions the range of analog inputs into 2^{16} discrete ranges or quanta. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2 LSB, associated with the resolution, in addition to the actual conversion errors.

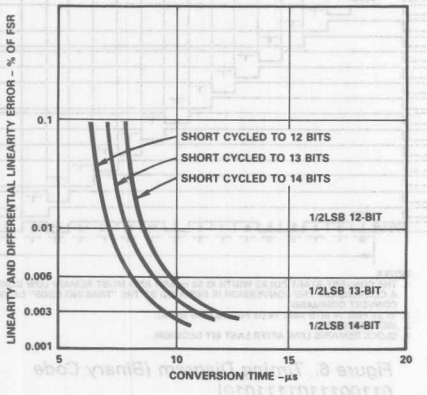


Figure 1. AD1378 Nonlinearity vs. Conversion Time

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of monolithic DACs that include the scaling network. The initial gain and offset errors are specified at ±0.2% FSR for gain and ±0.1% FSR for offset. These errors may be trimmed to zero by the use of external trim circuits as shown in Figures 3 and 4. Linearity error is defined for unipolar ranges as the deviation from a true straight line transfer characteristic from a zero voltage analog input, which calls for a zero digital output, to a point which is defined as a full scale. The linearity error is based on the DAC resistor ratios. It is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 2).

Monotonic behavior requires that the differential linearity error be less than 1 LSB, however a monotonic converter can have missing codes; the AD1378 is specified as having no missing codes over temperature ranges as specified on the data page.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right on the diagram over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero for unipolar ranges or minus full scale point for bipolar ranges. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G^2 + \epsilon_O^2 + \epsilon_L^2}$$

ϵ_G = Gain Drift Error (ppm/°C)
ϵ_O = Offset Drift Error (ppm of FSR/°C)
ϵ_L = Linearity Error (ppm of FSR/°C)

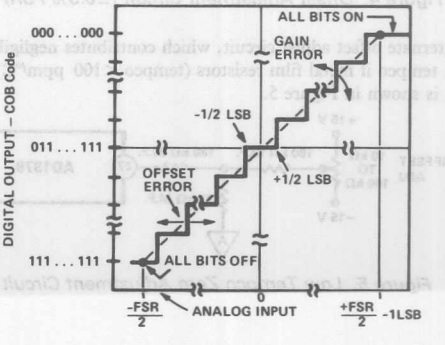


Figure 2. Transfer Characteristics for an Ideal Bipolar A/D

binary number. This conversion is accomplished as follows: the 16-bit successive-approximation register (SAR) has its 16-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

GAIN ADJUSTMENT

The gain adjust circuit consists of a 100-ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 300-kΩ resistor to the gain adjust Pin 29 as shown in Figure 3.

If no external trim adjustment is desired, Pin 27 (offset adj) and Pin 29 (gain adj) may be left open.

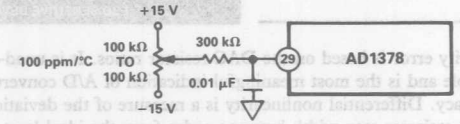


Figure 3. Gain Adjustment Circuit (±0.15% FSR)

OFFSET ADJUSTMENT

The zero adjust circuit consists of a 100-ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 1.8-MΩ resistor to Comparator Input Pin 27 for all ranges. As shown in Figure 4, the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a −1200-ppm/°C tempco contributes a worst-case offset tempco of 32 LSB_{14} × 61 ppm/LSB_{14} × 1200 ppm/°C = 2.3 ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±16 LSB_{14}, use of a carbon composition offset summing resistor typically contributes no more than 1 ppm/°C of FSR offset tempco.

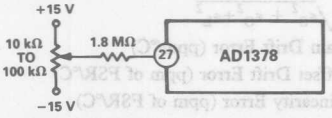


Figure 4. Offset Adjustment Circuit (±0.3% FSR)

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 5.

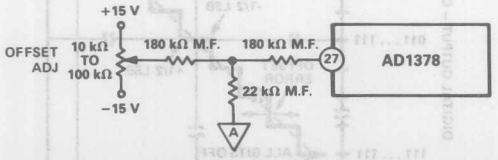


Figure 5. Low Tempco Zero Adjustment Circuit

nal noise pick-up and should be guarded by analog common.

TIMING

The timing diagram is shown in Figure 6. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 17 cycles. All the SAR parallel bits, STATUS flip-flops, and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and $B_2 - B_{16}$ are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is reset unconditionally. This sequence continues until the Bit 16 (LSB) decision (keep) is made at t_{16}. The STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the low Logic "0" state. Note that the clock remains low until the next conversion.

Corresponding parallel data bits become valid on the same positive-going clock edge.

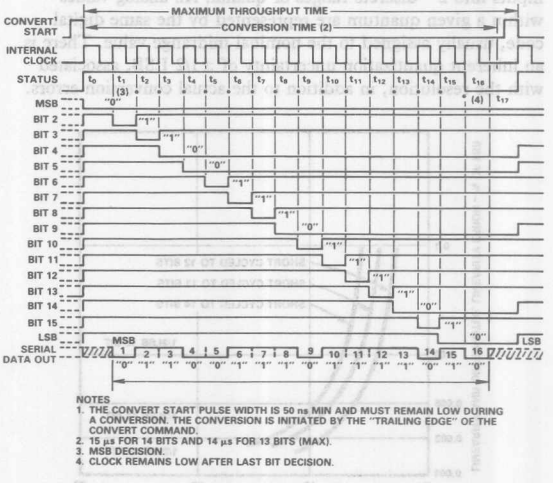


Figure 6. Timing Diagram (Binary Code 0110011101111010)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers is in negative true form (Logic "1" = 0 V and Logic "0" = 2.4 V). Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Parallel data becomes valid at least 20 ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag (see Figure 7).

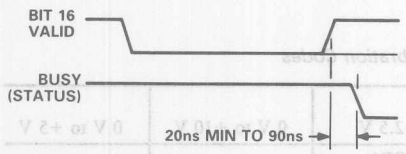


Figure 7. LSB Valid to Status Low

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 120 ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on the negative-going clock edges as shown in Figure 8. There are 17 negative-going clock edges in the complete 16-bit conversion cycle. The first negative edge shifts an invalid bit into the register, which is shifted out on the last negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

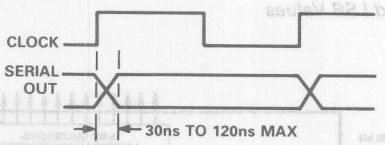


Figure 8. Clock High to Serial Out Valid

Short Cycle Input: A Short Cycle Input, Pin 32, permits the timing cycle shown in Figure 11 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 16-bit resolution. When 10-bit resolution is desired, Pin 32 is connected to Bit 11 output Pin 11. The conversion cycle then terminates and the STATUS flag resets after the Bit 10 decision (timing diagram of Figure 5). Short cycle connections and associated 8-, 10-, 12-, 13-, 14- and 15-bit conversion times are summarized in Table I, for a 933 kHz clock.

Resolution Bit	Resolution (%FSR)	Maximum Conversion Time (μs)	Status Flag Reset	Connect Short Cycle Pin 32 to Pin:
16	0.0015	17.1	t_{16}	N/C (Open)
15	0.003	16.1	t_{15}	16
14	0.006	15.0	t_{14}	15
13	0.012	13.9	t_{13}	14
12	0.024	12.9	t_{12}	13
10	0.100	10.7	t_{10}	11
8	0.390	8.6	t_8	9

Table I. Short Cycle Connections

INPUT SCALING

The AD1378 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 9 for circuit details.

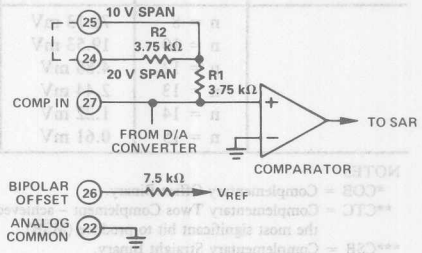


Figure 9. AD1378 Input Scaling Circuit

Input Signal Line	Output Code	Connect Pin 26 to Pin	Connect Pin 24 to	Connect Input Signal to
±10 V	COB	27	Input Signal	24
±5 V	COB	27	Open	25
±2.5 V	COB	27	Pin 27	25
0 V to +5 V	CSB	22	Pin 27	25
0 V to +10 V	CSB	22	Open	25
0 V to +20 V	CSB	22	Input Signal	24

Note: Pin 27 is extremely sensitive to noise and should be guarded by analog common.

Table II. AD1378 Input Scaling Connections

Code Under Test			Low Side Transition Values			
MSB LSB	Range	±10 V	±5 V	±2.5 V	0 to +10 V	0 to +5 V
000 . . . 000*	+Full Scale	+10 V −3/2 LSB	+ 5 V −3/2 LSB	+2.5 V −3/2 LSB	+10 V − 3/2 LSB	+5 V −3/2 LSB
011 . . . 111	Midscale	0–1/2 LSB	0–1/2 LSB	0–1/2 LSB	+5 V–1/2 LSB	+2.5 V–1/2 LSB
111 . . . 110	−Full Scale	−10 V +1/2 LSB	−5 V +1/2 LSB	−2.5 V +1/2 LSB	0 V +1/2 LSB	0 V +1/2 LSB

*Voltages given are the nominal value for transition to the code specified.
Note: For LSB value for range and resolution used, see Table IV.

Table III. Transition Values vs. Calibration Codes

Analog Input Voltage Range		±10 V	±5 V	±2.5 V	0 V to +10 V	0 V to +5 V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant (Bit LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13 mV	39.06 mV	19.53 mV	39.06 mV	19.53 mV
	n = 10	19.53 mV	9.77 mV	4.88 mV	9.77 mV	4.88 mV
	n = 12	4.88 mV	2.44 mV	1.22 mV	2.44 mV	1.22 mV
	n = 13	2.44 mV	1.22 mV	0.61 mV	1.22 mV	0.61 mV
	n = 14	1.22 mV	0.61 mV	0.31 mV	0.61 mV	0.31 mV
	n = 15	0.61 mV	0.31 mV	0.15 mV	0.31 mV	0.15 mV

NOTES
*COB = Complementary Offset Binary.
**CTC = Complementary Twos Complement – achieved by using an inverter to complement the most significant bit to produce ($\overline{MSB}$).
***CSB = Complementary Straight Binary.

Table IV. Input Voltage Range and LSB Values

CALIBRATION (14-Bit Resolution Examples)
External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 3 and 4, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and −FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10 V Range: Set analog input to +1 LSB_{14} = 0.00061 V. Adjust Zero for digital output = 11111111111110. Zero is now calibrated. Set analog input to +FSR − 2 LSB = + 9.99878 V. Adjust Gain for 00000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.00000 V; digital output code should be 01111111111111.

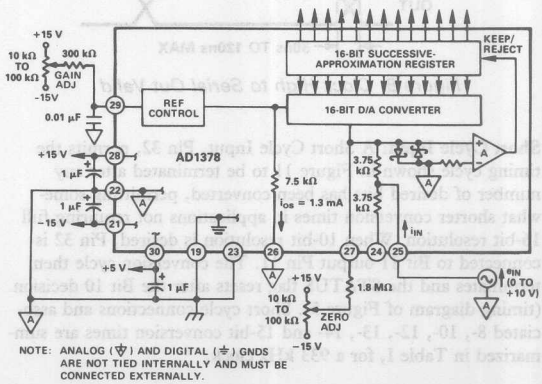


Figure 10. Analog and Power Connections for Unipolar 0 to +10 V Input Range

−10 V to + 10 V Range: Set analog input to −9.99878 V; adjust zero for 1111111111110 digital output (complementary offset binary) code. Set analog input to 9.99756 V; adjust Gain for 00000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.00000 V; digital output (complementary offset binary) code should be 0111111111111.

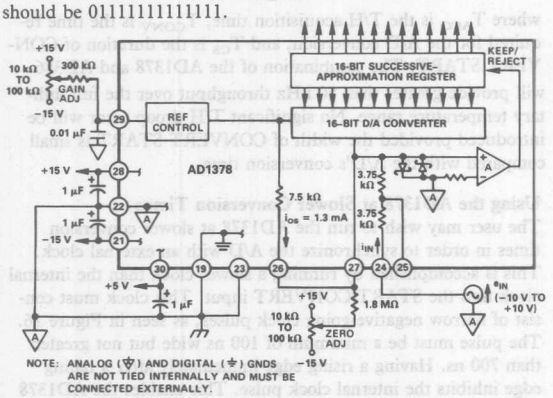


Figure 11. Analog and Power Connections for Bipolar −10 V to +10 V Input Range

Other Ranges: Representative digital coding for 0 to +10-V and −10-V to +10-V ranges is given above. Coding relationships and calibration points for 0 to +5-V, −2.5-V to +2.5-V and −5-V to +5-V ranges can be found by halving proportionally the corresponding code equivalents listed for the 0 to +10-V and −10-V to +10-V ranges, respectively, as indicated in Table III.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/2 LSB using the static adjustment procedure described above. By summing a small sine or triangular wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in *Analog-Digital Conversion Handbook*, edited by D. H. Sheingold, Prentice-Hall, Inc., 1986.

GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return) and Analog Signal Ground. These grounds (Pins 19 and 22) must be tied together at one point for the AD1378 as close as possible to the converter. Ideally, a single solid analog ground plane under the converter would be desirable. Current flows through the wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system analog ground point and the ground pins of the AD1378. Separate wide conductor stripe ground returns should be provided for high resolution converters to minimize noise and IR losses from the current flow in the path from the converter to the system ground point. In this way AD1378 supply currents and other digital logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD1378 supply terminals should be capacitively decoupled as close to the AD1378 as possible. A large value capacitor such as 1 µF in parallel with a 0.1 µF capacitor is usually sufficient. Analog supplies are to be bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

The metal cover is internally grounded with respect to the power supplies, grounds and electrical signals. Do not externally ground the cover.

CLOCK RATE CONTROL

The AD1378 may be operated at faster conversion times by connecting the Clock Rate Control (Pin 23) to an external multiturn trim potentiometer (TCR <100 ppm/°C) as shown in Figures 12 and 13. The integral linearity and differential linearity errors will vary with speed as shown in Figure 1.

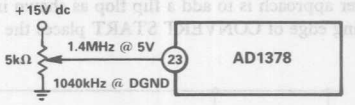


Figure 12. Clock Rate Control Circuit

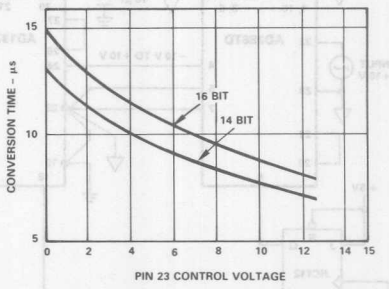


Figure 13. Conversion Time vs. Control Voltage

HIGH RESOLUTION DATA ACQUISITION SYSTEM

The essential details of a high resolution data acquisition system using the AD386 and AD1378 are shown in Figure 14. Conversion is initiated by the falling edge of the CONVERT START pulse. This edge drives the AD1378's STATUS line high. The inverter then drives the AD386 into hold mode. STATUS remains high throughout the conversion and returns low once the conversion is completed. This allows the AD386 to reenter track mode.

This circuit can exhibit nonlinearities arising from transients produced at the A/D's input by the falling edge of CONVERT-START. This edge resets the A/D's internal DAC; the resulting transient depends on the SHA's present output voltage and the A/D's prior conversion result. In the circuit of Figure 14 the falling edge of CONVERT-START also places the SHA into hold mode (via the A/D's STATUS output), causing the reset transient to occur at the same moment as the SHA's track-and-

hold transition. Timing skews and capacitive coupling can cause some of the transient signal to add to the signal being acquired by the SHA, introducing nonlinearity.

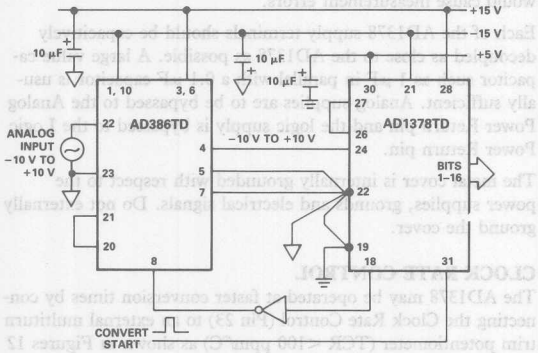


Figure 14. Basic Data Acquisition System Interconnections

A much safer approach is to add a flip flop as shown in Figure 15. The rising edge of CONVERT START places the T/H into hold mode before the A/D reset transients begin. The falling edge of STATUS places the AD386 back into track mode. System throughput will be reduced if a long CONVERT START pulse is used. Throughput can be calculated from

$$Throughput = \frac{1}{T_{ACQ} + T_{CONV} + T_{CS}}$$

where T_{ACQ} is the T/H acquisition time, T_{CONV} is the time required for the A/D conversion, and T_{CS} is the duration of CONVERT START. The combination of the AD1378 and AD386 will provide greater than 50 kHz throughput over the full military temperature range. No significant T/H droop error will be introduced provided the width of CONVERT START is small compared with the A/D's conversion time.

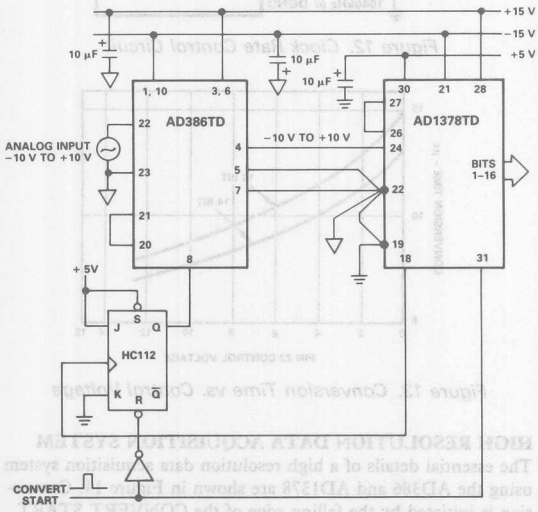


Figure 15. Improved Data Acquisition System

Using the AD1378 at Slower Conversion Times

The user may wish to run the AD1378 at slower conversion times in order to synchronize the A/D with an external clock. This is accomplished by running a slower clock than the internal clock into the START CONVERT input. This clock must consist of narrow negative-going clock pulses, as seen in Figure 16. The pulse must be a minimum of 100 ns wide but not greater than 700 ns. Having a rising edge immediately after a falling edge inhibits the internal clock pulse. This enables the AD1378 to function normally and complete a conversion after 17 clock pulses. The STATUS command will function normally and switch high after the first clock pulse and will fall low after the 17th clock pulse. In this way an external clock can be used to control the AD1378 at slower conversion times.

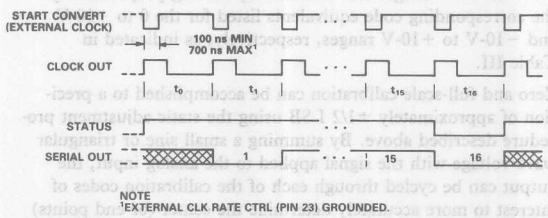


Figure 16. Timing Diagram for Use with an External Clock

Low Cost 16-Bit Sampling ADC

AD1380

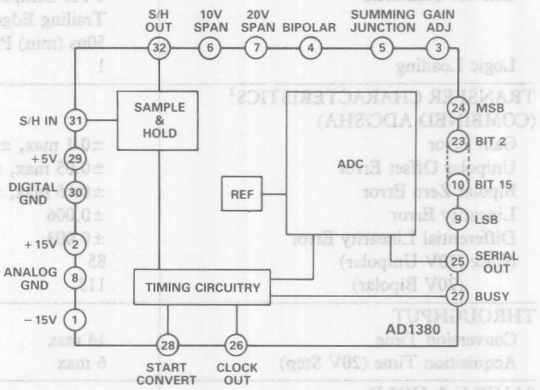
FEATURES

- Complete Sampling 16-Bit ADC With Reference and Clock
- 50kHz Throughput
- ±1/2LSB Nonlinearity
- Low Noise SHA: 300μV p-p
- 32-Pin Hermetic DIP
- Parallel and Serial Outputs
- Low Power: 900mW

APPLICATIONS

- Medical and Analytical Instrumentation
- Signal Processing
- Data Acquisition Systems
- Professional Audio
- Automatic Test Equipment (ATE)
- Telecommunications

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1380 is a complete, low cost 16-bit analog-to-digital converter, including internal reference, clock and sample/hold amplifier. Internal thin-film-on-silicon scaling resistors allow analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V and 0 to +10V.

Important performance characteristics of the AD1380 include maximum linearity error of ±0.003% of FSR (AD1380KD) and maximum 16-bit conversion time of 14μs. Transfer characteristics of the AD1380 (gain, offset and linearity) are specified for the combined ADC/SHA, so total performance is guaranteed as a system. The AD1380 provides data in parallel and serial form with corresponding clock and status outputs. All digital inputs and outputs are TTL or 5V CMOS compatible.

ORDERING GUIDE

Model	Max Linearity Error	Temperature Range	Package Option*
AD1380JD	0.006% FSR	0 to +70°C	Ceramic (DH-32E)
AD1380KD	0.003% FSR	0 to +70°C	Ceramic (DH-32E)

*DH-32E = Bottom Brazed Ceramic DIP. For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Logic Supply Voltage	+7V
Analog Ground to Digital Ground	±0.3V
Analog Inputs (Pins 6, 7, 31)	$\pm V_S$
Digital Input	−0.3V to V_{DD} +0.3V
Output Short Circuit Duration to Ground	
Sample/Hold	Indefinite
Data	1 sec for Any One Output
Junction Temperature	+175°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

AD1380—SPECIFICATIONS (typical @ T_A = +25°C, V_S = +15V, +5V combined sample and hold A/D converter unless otherwise noted)

Model	AD1380JD	AD1380KD	Units
RESOLUTION	16	*	Bits
ANALOG INPUTS			
Bipolar	±2.5, ±5, ±10	*	Volts
Unipolar	0 to +5, 0 to +10	*	Volts
DIGITAL INPUTS[1]			
Convert Command	TTL Compatible Trailing Edge of Positive 50ns (min) Pulse	*	
Logic Loading	1	*	LSTTL Load
TRANSFER CHARACTERISTICS[2] (COMBINED ADC/SHA)			
Gain Error	±0.1 max, ±0.05 typ[3]	*	% FSR[4]
Unipolar Offset Error	±0.05 max, ±0.02 typ[3]	*	% FSR
Bipolar Zero Error	±0.05 max, ±0.02 typ[3]	*	% FSR
Linearity Error	±0.006	±0.003	% FSR
Differential Linearity Error	±0.003	*	% FSR
Noise (10V Unipolar)	85	*	μV rms
(20V Bipolar)	115	*	μV rms
THROUGHPUT			
Conversion Time	14 max	*	μs
Acquisition Time (20V Step)	6 max	*	μs
SAMPLE & HOLD			
Input Resistance	4	*	kΩ
Small Signal Bandwidth	900	*	kHz
Aperture Time	50	*	ns
Aperture Jitter	100	*	ps rms
Droop Rate	50	*	μV/ms
T_{min} to T_{max}	1	*	mV/ms
Feedthrough	−80	*	dB
DRIFT (ADC & SHA)[5]			
Gain	±20 max	*	ppm/°C
Unipolar Offset	±5 max (±2 typ)	*	ppm/°C
Bipolar Zero	±5 max (±2 typ)	*	ppm/°C
No Missing Codes (Guaranteed)	0 to +70 (13 Bits)	0 to +70 (14 Bits)	°C
DIGITAL OUTPUTS	TTL Compatible	*	
All Codes Complementary	5	*	LSTTL Loads
Clock Frequency	1.1	*	MHz
POWER SUPPLY REQUIREMENTS			
Analog Supplies	±15 ±0.5	*	Volts
Digital Supply	+5 ±0.25	*	Volts
+15V Supply Current	25	*	mA
−15V Supply Current	30	*	mA
+5V Supply Current	15	*	mA
Power Dissipation	900	*	mW
TEMPERATURE RANGE			
Specified	0 to +70	*	°C
Operating	−25 to +85	*	°C

NOTE
[1]Logic "0" = 0.8V, max. Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = 0.4V max. Logic "1" = 2.4V min.
[2]Tested on ±10V and 0 to +10V ranges.
[3]Adjustable to zero.
[4]Full scale range.
[5]Guaranteed but not 100% production tested.
*Specifications same as AD1380JD.
Specifications subject to change without notice.

THEORY OF OPERATION

A 16-bit A/D converter partitions the range of analog inputs into 2^{16} discrete ranges or quanta. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of monolithic DACs that include the scaling network. The initial gain and offset errors are specified at ±0.1% FSR for gain and ±0.05% FSR for offset. These errors may be trimmed to zero by the use of external trim circuits as shown in Figures 2 and 3. Linearity error is defined for unipolar ranges as the deviation from a true straight line transfer characteristic from a zero voltage analog input, which calls for a zero digital output, to a point which is defined as a full scale. The linearity error is based on the DAC resistor ratios. It is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 1).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD1380 is specified as having no missing codes over temperature ranges as specified on the data page.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right on the diagram over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero for unipolar ranges or minus full scale point for bipolar ranges. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G^2 + \epsilon_O^2 + \epsilon_L^2}$$

ϵ_G = Gain Drift Error (ppm/°C)

ϵ_O = Offset Drift Error (ppm of FSR/°C)

ϵ_L = Linearity Error (ppm of FSR/°C)

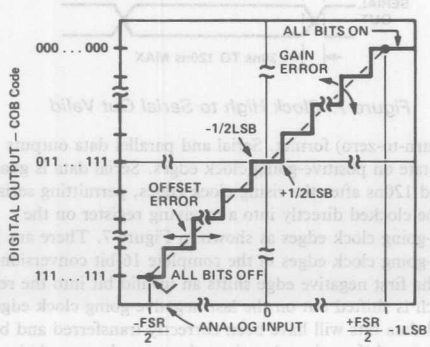


Figure 1. Transfer Characteristics for an Ideal Bipolar A/D

DESCRIPTION OF OPERATION

On receipt of a CONVERT START command, the AD1380 converts the voltage at its analog input into an equivalent 16-bit binary number. This conversion is accomplished as follows: the 16-bit successive approximation register (SAR) has its 16-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

GAIN ADJUSTMENT

The gain adjust circuit consists of a 100ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 300kΩ resistor to the gain adjust Pin 3 as shown in Figure 2.

If no external trim adjustment is desired, Pin 5 (OFFSET ADJ) and Pin 3 (GAIN ADJ) may be left open.

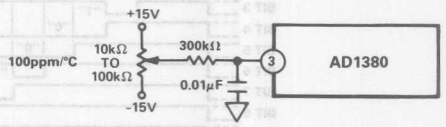


Figure 2. Gain Adjustment Circuit (±0.2% FSR)

OFFSET ADJUSTMENT

The zero adjust circuit consists of a 100ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input Pin 5 for all ranges. As shown in Figure 3, the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a −1200ppm/°C tempco contributes a worst-case offset tempco of $32LSB_{14} \times 61ppm/LSB_{14} \times 1200ppm/°C = 2.3ppm/°C$ of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than $\pm 16LSB_{14}$, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

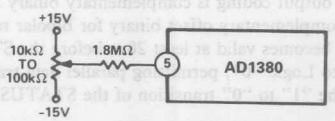


Figure 3. Offset Adjustment Circuit (±0.3% FSR)

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100ppm/°C) are used, is shown in Figure 4.

In either adjust circuit, the fixed resistor connected to Pin 5 should be located close to this pin to keep the pin connection runs short. Comparator Input Pin 5 is quite sensitive to external noise pickup and should be guarded by analog common.

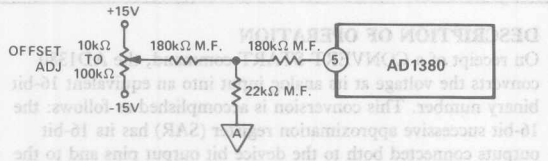
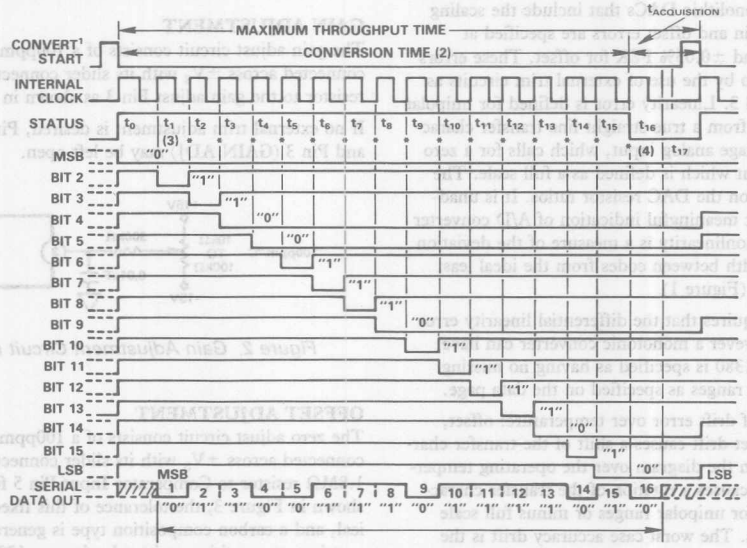


Figure 4. Low Tempco Zero Adjustment Circuit

TIMING

The timing diagram is shown in Figure 5. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock permitting it to run through 17 cycles. All the SAR parallel bits, STATUS flip-flops and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and $B_2 - B_{16}$ are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is reset unconditionally. This sequence continues until the Bit 16 (LSB) decision (keep) is made at t_{16}. The STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the low Logic "0" state. Note that the clock remains low until the next conversion.

Corresponding parallel data bits become valid on the same positive-going clock edge.



NOTES
1. THE CONVERT START PULSE WIDTH IS 50ns MIN AND MUST REMAIN LOW DURING A CONVERSION. THE CONVERSION IS INITIATED BY THE "TRAILING EDGE" OF THE CONVERT COMMAND.
2. t_{CONV} = 14µs (MAX), t_{ACQ} = 6µs (MAX).
3. MSB DECISION.
4. CLOCK REMAINS LOW AFTER LAST BIT DECISION.

Figure 5. Timing Diagram (Binary Code 0110011101111010)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers is in negative true form (Logic "1" = 0V and Logic "0" = 2.4V). Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Parallel data becomes valid at least 20ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag (see Figure 6).

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 120ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on the negative-going clock edges as shown in Figure 7. There are 17 negative-going clock edges in the complete 16-bit conversion cycle. The first negative edge shifts an invalid bit into the register, which is shifted out on the last negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

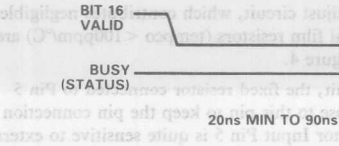


Figure 6. LSB Valid to Status Low

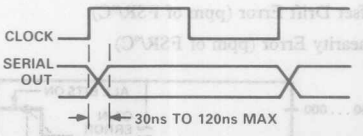


Figure 7. Clock High to Serial Out Valid

INPUT SCALING

The AD1380 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table I. See Figure 8 for circuit details.

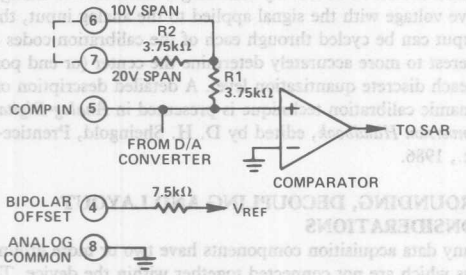


Figure 8. AD1380 Input Scaling Circuit

Input Signal Line	Output Code	Connect Pin 4 to Pin	Connect Pin 7 to	Connect Input Signal to	Connect Pin 32 to
±10V	COB	5	32	31	7
±5V	COB	5	Open	31	6
±2.5V	COB	5	Pin 5	31	6
0V to +5V	CSB	NC	Pin 5	31	6
0V to +10V	CSB	NC	Open	31	6

NOTE
Pin 5 is extremely sensitive to noise and should be guarded by analog common.

Table I. AD1380 Input Scaling Connections

Code Under Test MSB LSB	Range	Low Side Transition Value ±10V	±5V	± 2.5V	0 to +10V	0 to +5V
000 . . . 000*	+ Full Scale	+10V −3/2LSB	+5V −3/2LSB	+2.5V −3/2LSB	+10V −3/2LSB	+5V −3/2LSB
011 . . . 111	Mid Scale	0–1/2LSB	0–1/2LSB	0–1/2LSB	+5V–1/2LSB	+2.5V–1/2LSB
111 . . . 110	−Full Scale	−10V +1/2LSB	−5V +1/2LSB	−2.5V +1/2LSB	0V +1/2LSB	0V +1/2LSB

NOTE
For LSB value for range and resolution used, see Table III.
*Voltages given are the nominal value for transition to the code specified.

Table II. Transition Values vs. Calibration Codes

Analog Input Voltage Range		±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least FSR Significant (Bit LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
	n = 13	2.44mV	1.22mV	0.61mV	1.22mV	0.61mV
	n = 14	1.22mV	0.61mV	0.31mV	0.61mV	0.31mV
	n = 15	0.61mV	0.31mV	0.15mV	0.31mV	0.15mV

NOTES
*COB = Complementary Offset Binary.
**CTC = Complementary Twos Complement – achieved by using an inverter to complement the most significant bit to produce ($\overline{MSB}$).
***CSB = Complementary Straight Binary.

Table III. Input Voltage Range and LSB Values

CALIBRATION (14-Bit Resolution Examples)
External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 2 and 3, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and −FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to + 10V Range: Set analog input to + $1LSB_{14}$ = 0.00061V. Adjust Zero for digital output = 11111111111110. Zero is now calibrated. Set analog input to +FSR − 2LSB = + 9.99878V. Adjust Gain for 00000000000001 digital output code; full scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.00000V; digital output code should be 01111111111111.

−10V to + 10V Range: Set analog input to −9.99878V; adjust zero for 1111111111110 digital output (complementary offset binary) code. Set analog input to 9.99756V; adjust Gain for 00000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.00000V; digital output (complementary offset binary) code should be 01111111111111.

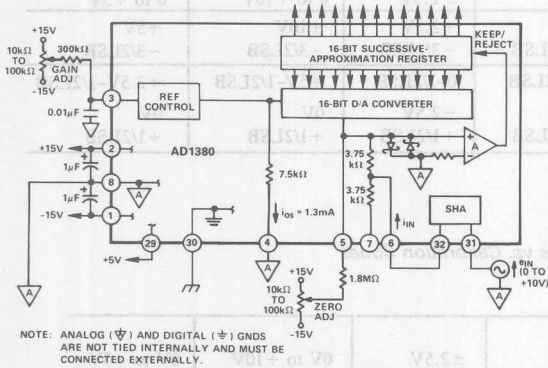


Figure 9. Analog and Power Connections for Unipolar 0 to +10V Input Range

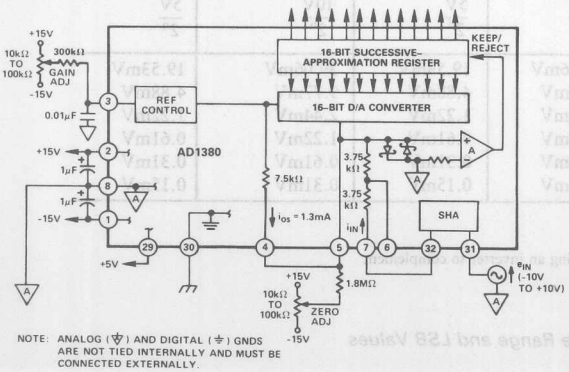


Figure 10. Analog and Power Connections for Bipolar −10V to +10V Input Range

Other Ranges: Representative digital coding for 0 to + 10V and −10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, −2.5V to +2.5V and −5V to +5V ranges can be found by halving proportionally the corresponding code equivalents listed for the 0 to +10V and −10V to +10V ranges, respectively, as indicated in Table II.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/2LSB using the static adjustment procedure described above. By summing a small sine or triangular wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in *Analog-Digital Conversion Handbook*, edited by D. H. Sheingold, Prentice-Hall, Inc., 1986.

GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS
Many data acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return) and Analog Signal Ground. These grounds (Pins 8 and 30) must be tied together at one point for the AD1380 as close as possible to the converter. Ideally, a single, solid analog ground plane under the converter would be desirable. Current flows through the wires and etch stripes on the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system analog ground point and the ground pins of the AD1380. Separate wide conductor stripe ground returns should be provided for high resolution converters to minimize noise and IR losses from the current flow in the path from the converter to the system ground point. In this way AD1380 supply currents and other digital logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD1380 supply terminals should be capacitively decoupled as close to the AD1380 as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are to be bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

The metal cover is internally grounded with respect to the power supplies, grounds and electrical signals. Do not externally ground the cover.

APPLICATION

AD1380 Dynamic Performance

High performance sampling analog-to-digital converters like the AD1380 require dynamic characterization to assure they meet or exceed their desired performance parameters for signal processing applications. Key dynamic parameters include signal-to-noise ratio (SNR) and total harmonic distortion (THD), which are characterized using Fast Fourier Transform (FFT) analysis techniques.

The results of that characterization are shown in Figure 11. In the test a 13.2kHz sine wave is applied as the analog input (f_O) at a level of 10dB below full scale; the AD1380 is operated at a word rate of 50kHz (its maximum sampling frequency).

The results of a 1024-point FFT demonstrate the exceptional performance of the converter, particularly in terms of low noise and harmonic distortion.

In Figure 11, the vertical scale is based on a full scale input referenced as 0dB. In this way, all (frequency) energy cells can be calculated with respect to full scale rms inputs.

The resulting signal-to-noise ratio is 83.2dB, which corresponds to a noise floor of −93.2dB.

Total harmonic distortion is calculated by adding the RMS energy of the first four harmonics and equals −97.5dB. Increasing the input signal amplitude to −0.4dB of full scale, causes THD to increase to −80.6dB as shown in Figure 12.

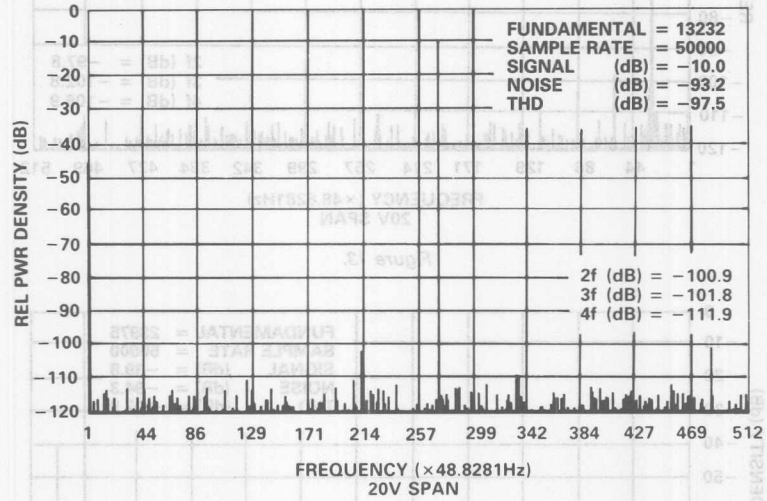


Figure 11.

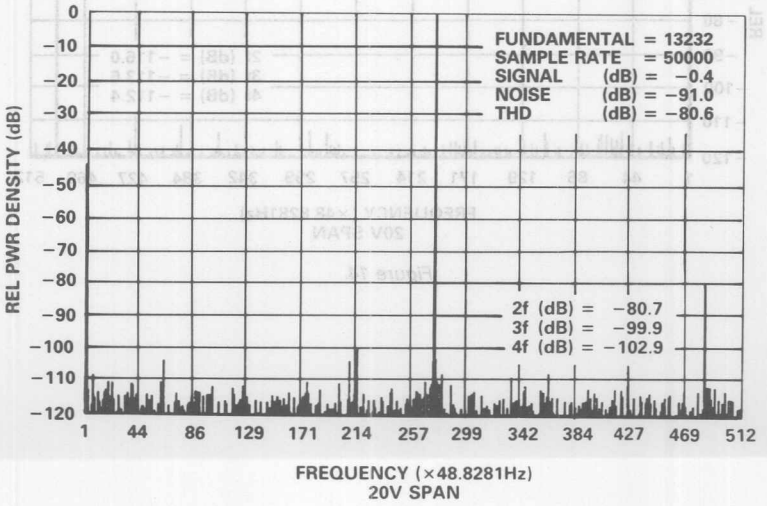


Figure 12.

At lower input frequencies, however, THD performance is improved. Figure 13 shows a full scale (−0.3dB) input signal at 1.41kHz. THD is now −96.0dB.

The ultimate noise floor can be seen with low level input signals of any frequency. In Figure 14 the noise floor is at −94dB, as demonstrated with an input signal of 24kHz at −39.8dB.

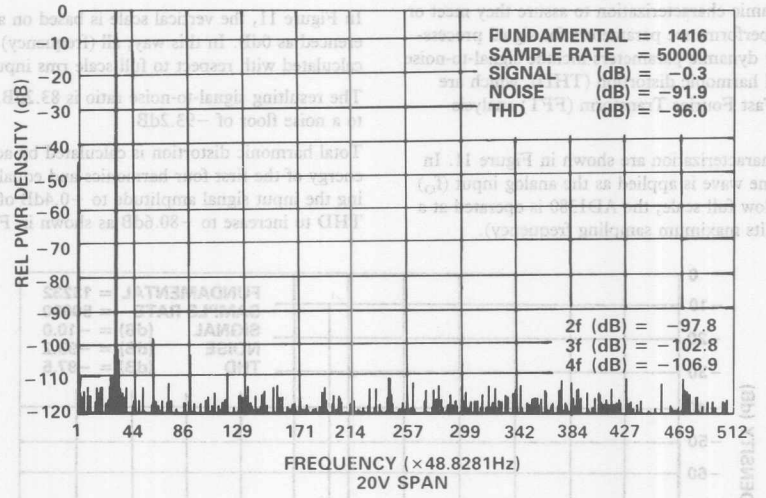


Figure 13.

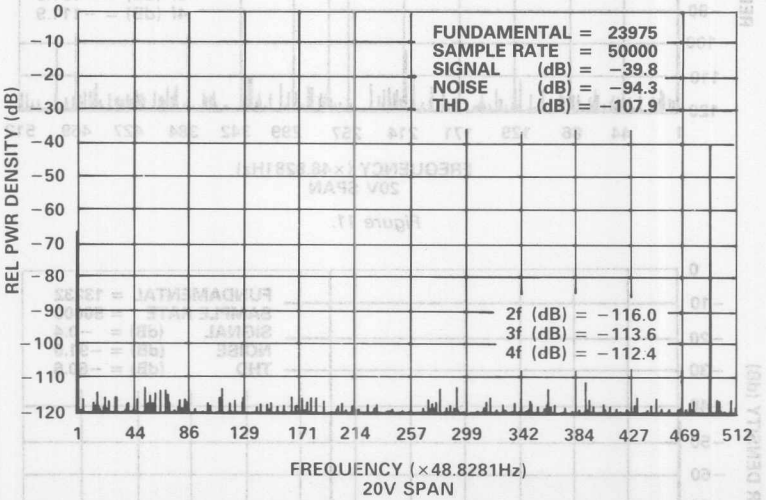


Figure 14.

16-Bit 500 kHz Sampling ADC

AD1382

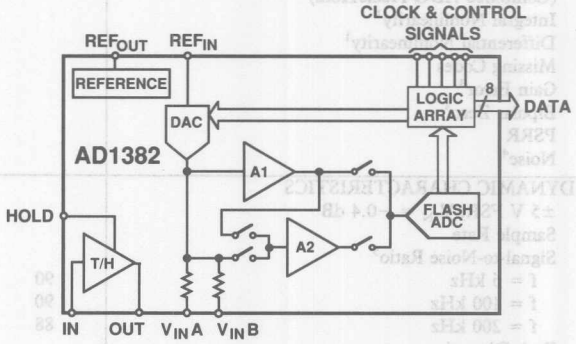
PRODUCT FEATURES

- Single Package
- 16-Bit Resolution
- 500 kHz Sampling Rate
- SNR 90 dB @ 100 kHz (min)
- THD −88 dB @ 100 kHz (min)
- 0.0015% FSR INL (typ)
- ±5, ±10 V Bipolar Input
- Zero Offset Autocalibration

APPLICATIONS

- Medical Imaging
  - CAT
  - Magnetic Resonance
- Vibration Analysis
- Parametric Measurement Unit (ATE)
- Waveform/Transient Recorders
- Analytical Instruments
- Sonar
- Radar

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1382 is a complete 500 kHz, 16-bit, sampling analog-to-digital converter contained in a single package. This high resolution, high speed converter offers outstanding noise and distortion performance along with excellent INL and DNL performance, all in a single dual-in-line package.

The AD1382 guarantees outstanding noise and distortion performance for both ±5 V and ±10 V input ranges. The AD1382 architecture includes a low noise and low distortion track/hold with a three-pass digitally corrected subranging ADC. Precision thin film resistors and a new proprietary DAC provide for outstanding dynamic and static performance. Output data is multiplexed over an eight-bit CMOS/TTL compatible data bus.

The AD1382 uses four power supplies, ±5 V and ±15 V, and an external 10 MHz clock. Power dissipation is nominally 2.8 W. Two user selectable bipolar input ranges, ±5 V and ±10 V are provided. Careful attention to grounding and a single package make it easy to design PCBs to achieve specified performance.

AD1382—SPECIFICATIONS (T_A = +25°C, V_S = ±15 V, V_{DD} = +5 V, V_{SS} = −5 V, 10 MHz External Clock, 5 Minute Warm-up, unless otherwise noted)

Parameter	AD1382KD Min	Typ	Max	Units
RESOLUTION	16			Bits
ANALOG INPUT				
Input Ranges		±5, ±10		V
Input Impedance	2.45	2.5	2.55	kΩ
TRANSFER CHARACTERISTICS				
(Combined ADC/Track/Hold)				
Integral Nonlinearity[1]		±0.0015		% FSR[2]
Differential Nonlinearity[1]		±0.0006	±0.0015	% FSR
Missing Codes			None	
Gain Error[3]		±0.07	±0.15	% FSR
Bipolar Zero[3]		±0.03	±0.10	% FSR
PSRR		±0.006	±0.10	% FSR/V
Noise[4]		55		μV RMS
DYNAMIC CHARACTERISTICS				
±5 V FSR, V_{IN} = −0.4 dB				
Sample Rate			500	kHz
Signal-to-Noise Ratio[5]				
f = 5 kHz	90	93		dB
f = 100 kHz	90	92		dB
f = 200 kHz	88	91		dB
Peak Distortion				
f = 5 kHz	−90	−98		dB
f = 100 kHz	−88	−93		dB
f = 200 kHz	−82	−85		dB
Total Harmonic Distortion[6]				
f = 5 kHz	−90	−96		dB
f = 100 kHz	−88	−92		dB
f = 200 kHz	−82	−85		dB
DYNAMIC CHARACTERISTICS				
±10 V FSR, V_{IN} = −0.4 dB				
Sample Rate			500	kHz
Signal-to-Noise Ratio[5]				
f = 5 kHz	90	95		dB
f = 100 kHz	90	94		dB
f = 200 kHz	88	93		dB
Peak Distortion				
f = 5 kHz	−90	−98		dB
f = 100 kHz	−80	−87		dB
f = 200 kHz	−74	−81		dB
Total Harmonic Distortion[6]				
f = 5 kHz	−90	−96		dB
f = 100 kHz	−80	−87		dB
f = 200 kHz	−74	−81		dB
DIGITAL INPUTS[9]				
Input Voltage				
V_{IL}			0.8	V
V_{IH}	2.0			V
Input Current			±200	μA
Input Capacitance		2		pF
Start Command				
Setup Time, t_{SCS}	10	3		ns
Hold Time, t_{SCH}	10	0		ns
Autozero				
Setup Time, t_{AZS}	10	0		ns
Hold Time, t_{AZH}	20	6		ns
Clock				
Frequency	2.5		10	MHz
Duty Cycle	40		60	%

Parameter	AD1382KD Min	Typ	Max	Units
DIGITAL INPUTS (Continued)				
Aperture Delay[7]		7		ns
DIGITAL OUTPUTS[8, 9]				
Output Voltage				
V_{OL} @ I_{OL} = 3.2 mA		0.2	0.4	V
V_{OH} @ I_{OH} = −3.2 mA	2.4	4.5		V
Output Capacitance		10		pF
Leakage, Outputs Disabled			±200	μA
Data Valid				
Setup Time, t_{DVS}	75	150		ns
Hold Time, t_{DVH}	25	50		ns
Hold Command Time, t_H		1300		ns
Hold Command Delay, t_{HD}		6		ns
Data Strobe Pulse Width, t_{DS}		200		ns
Data Strobe Delay, t_{DSD}		1650		ns
OUTPUT CODING		Complementary Offset Binary or Complementary Twos Complement		
PERFORMANCE OVER TEMPERATURE[8, 10]				
Operating Temperature Range	0		70	°C
Specified Temperature Range	10		40	°C
Missing Codes			None	
Gain Drift		8	15	ppm/°C
Offset Drift		5	15	ppm/°C
Differential Linearity		0.3		ppm/°C
INTERNAL REFERENCE				
Voltage	9.990		10.010	V
Current	2	10		mA
POWER REQUIREMENTS				
Operating Range				
$\pm V_S$	14.25		15.75	V
$+V_{DD}$	4.75		5.25	V
$-V_{SS}$	−5.25		−4.75	V
Current Drains				
$+V_S$		50	73	mA
$-V_S$		45	65	mA
$+V_{DD}$		115	160	mA
$-V_{SS}$		160	200	mA
Power Dissipation		2.8	3.9	Watts

NOTES

[1]Integral linearity is inferred from FFT. Differential linearity is derived from histogram.

[2]FSR, full-scale range.

[3]Adjustable to zero.

[4]Noise based on small signal FFT excluding quantization noise.

[5]SNR fundamental to noise minus harmonics 2–9.

[6]THD includes harmonics 2–9 of the fundamental.

[7]Aperture delay is the time from the rising edge on the Hold Command Input to the opening of the switch in the Track/Hold.

[8]Guaranteed but not 100% production tested.

[9]Timing based on 10 MHz clock. Refer to Figures 13 and 14.

[10]Case to ambient temperature is assumed to be 30°C. The AD1382 case temperature will stabilize about 30°C above ambient while operating in free air without a heat sink. Factory calibration is done in this condition. See the application section for further information.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

$+V_S$ to AGND . . . . . 18 V
$-V_S$ to AGND . . . . . −18 V
V_{DD} to PGND . . . . . 7 V
V_{SS} to PGND . . . . . −7 V
AGND to PGND . . . . . ±0.3 V
Analog Inputs . . . . . $\pm V_S$
Digital Inputs . . . . . −0.3 V to V_{DD} + 0.3 V
Output Short Circuit Duration
Reference Output . . . . . Indefinite
Track/Hold Output . . . . . 1 sec
Digital Outputs . . . . . 1 sec for Any One Output
Ambient Temperature (Operating) . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AD1382 PIN CONNECTIONS

The AD1382 is housed in a 48-pin bottom-brazed ceramic bathtub package. The pinout is as follows:

PIN	FUNCTION	PIN	FUNCTION
1	CLOCK IN	48	V_{DD2} (+5 V POWER)
2	POWER GROUND	47	POWER GROUND
3	B1/B9 MSB	46	V_{SS2} (−5 V POWER)
4	B2/B10	45	AUTOZERO
5	B3/B11	44	B1 SELECT
6	B4/B12	43	POWER GROUND
7	B5/B13	42	POWER GROUND
8	B6/B14	41	DNC
9	B7/B15	40	GAIN ADJUST
10	B8/B16 LSB	39	+10 V REFERENCE OUT
11	V_{DD1} (+5 V SIGNAL)	38	$-V_{S1}$ (−15 V)
12	POWER GROUND	37	SIGNAL GROUND
13	V_{SS1} (−5 V SIGNAL)	36	$+V_{S1}$ (+15 V)
14	SIGNAL GROUND	35	SIGNAL GROUND
15	DATA STROBE	34	DNC
16	HI/LO BYTE SELECT	33	DNC
17	OE DATA ENABLE	32	+10 V REFERENCE IN
18	START CONVERT	31	V_{IN} B
19	HOLD COMMAND OUT	30	V_{IN} A
20	SIGNAL GROUND	29	OFFSET ADJUST
21	$+V_{S2}$ (+15 V)	28	DNC
22	HOLD COMMAND IN	27	TRACK/HOLD OUTPUT
23	$-V_{S2}$ (−15 V)	26	SIGNAL GROUND
24	POWER GROUND	25	TRACK/HOLD INPUT

DNC = DO NOT CONNECT

CAUTION

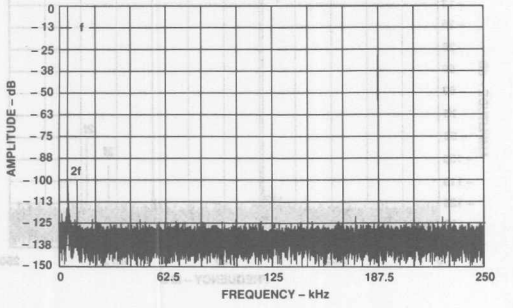
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



ORDERING GUIDE

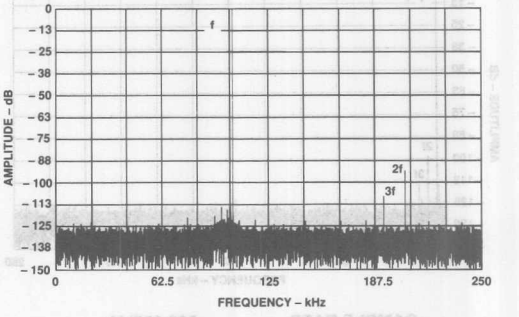
Model	Temperature Range	Package Option*
AD1382KD	10°C to 40°C Ambient (40°C to 70°C Case)	DH-48A

*DH-48A = Hermetic Ceramic DIP. For outline information see Package Information section.



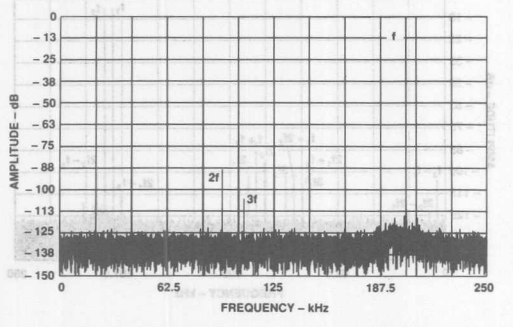
SAMPLE RATE	500.000kHz
INPUT FREQUENCY	5.279410kHz
INPUT AMPLITUDE	–0.3dB
2nd HARMONIC	–99.8dB
3rd HARMONIC	–116.9dB
4th HARMONIC	–117.1dB
SNR	93.1dB
THD	–99.2dB

Figure 1. Full-Scale Sine Wave Power Spectral Density, ±5 V Scale, 16384-Point FFT



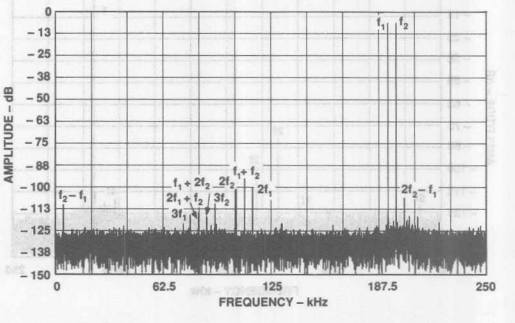
SAMPLE RATE	500.000kHz
INPUT FREQUENCY	102.50855kHz
INPUT AMPLITUDE	–0.4dB
2nd HARMONIC	–93.0dB
3rd HARMONIC	–107.4dB
4th HARMONIC	–115.6dB
SNR	92.5dB
THD	–92.7dB

Figure 2. Full-Scale Sine Wave Power Spectral Density, ±5 V Scale, 16384-Point FFT



SAMPLE RATE	500.000kHz
INPUT FREQUENCY	202.54516kHz
INPUT AMPLITUDE	–0.4dB
2nd HARMONIC	–88.2dB
3rd HARMONIC	–104.7dB
4th HARMONIC	–112.4dB
SNR	91.5dB
THD	–88.0dB

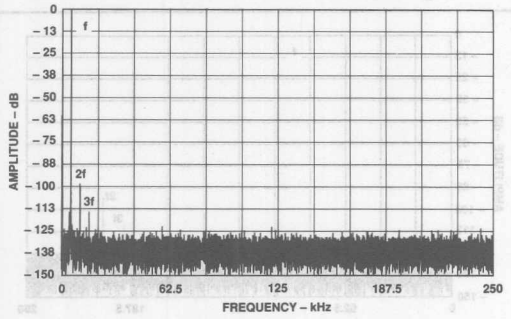
Figure 3. Full-Scale Sine Wave Power Spectral Density, ±5 V Scale, 16384-Point FFT



f_1 FREQUENCY	192.77954kHz		
f_1 AMPLITUDE	–6.1dB		
f_2 FREQUENCY	197.54028kHz		
f_2 AMPLITUDE	–6.0dB		
$f_2 - f_1$	–110.2dB	$f_2 + 2f_1$	–116.0dB
$f_2 + f_1$	–94.9dB	$2f_1$	–100.8dB
$2f_2 - f_1$	–106.0dB	$2f_2$	–101.2dB
$2f_1 - f_2$	–128.0dB	$3f_1$	–117.2dB
$f_1 + 2f_2$	–116.8dB	$3f_2$	–109.6dB

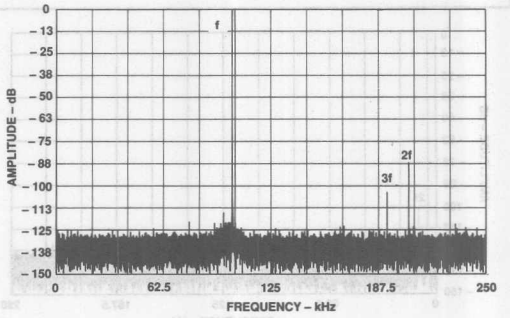
Figure 4. Intermodulation Performance, ±5 V Scale, 16384-Point FFT, 500 kHz Sample Rate

AD1382—Dynamic Performance



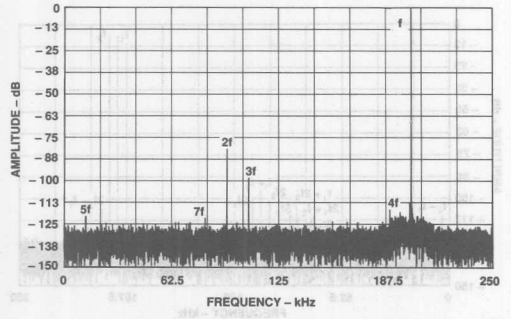
SAMPLE RATE	500.000kHz
INPUT FREQUENCY	5.279541kHz
INPUT AMPLITUDE	–0.3dB
2nd HARMONIC	–98.3dB
3rd HARMONIC	–112.9dB
4th HARMONIC	–116.9dB
SNR	94.8dB
THD	–97.9dB

Figure 5. Full-Scale Sine Wave Power Spectral Density, ±10 V Scale, 16384-Point FFT



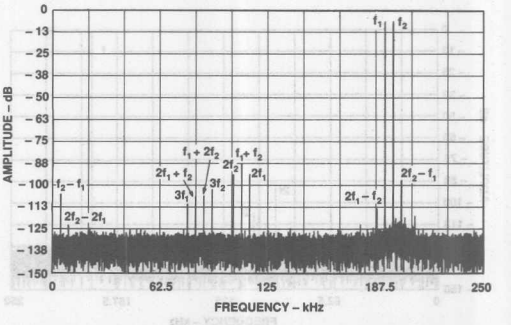
SAMPLE RATE	500.000kHz
INPUT FREQUENCY	102.50855kHz
INPUT AMPLITUDE	–0.4dB
2nd HARMONIC	–86.9dB
3rd HARMONIC	–103.4dB
4th HARMONIC	–118.1dB
SNR	94.1dB
THD	–86.8dB

Figure 6. Full-Scale Sine Wave Power Spectral Density, ±10 V Scale, 16384-Point FFT



SAMPLE RATE	500.000kHz
INPUT FREQUENCY	202.54516kHz
INPUT AMPLITUDE	–0.4dB
2nd HARMONIC	–81.6dB
3rd HARMONIC	–98.2dB
4th HARMONIC	–112.4dB
SNR	93.0dB
THD	–81.5dB

Figure 7. Full-Scale Sine Wave Power Spectral Density, ±10 V Scale, 16384-Point FFT



f_1 FREQUENCY	192.77954kHz		
f_1 AMPLITUDE	–6.1dB		
f_2 FREQUENCY	197.54028kHz		
f_2 AMPLITUDE	–6.0dB		
$f_2 - f_1$	–105.1dB	$f_2 + 2f_1$	–106.2dB
$f_2 + f_1$	–87.3dB	$2f_1$	–93.5dB
$2f_2 - f_1$	–96.9dB	$2f_2$	–93.7dB
$2f_1 - f_2$	–127.0dB	$3f_1$	–110.5dB
$f_1 + 2f_2$	–106.3dB	$3f_2$	–102.2dB

Figure 8. Intermodulation Performance, ±10 V Scale, 16384-Point FFT, 500 kHz Sample Rate

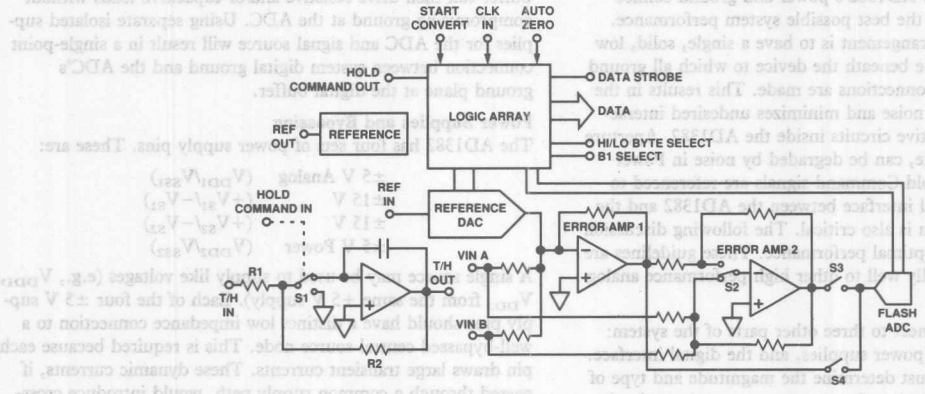


Figure 9. AD1382 Functional Block Diagram

THEORY OF OPERATION

The AD1382 performs conversions using a three-pass subranging technique. This proven circuit concept, implemented with state of the art components, allows the ADC, track-hold, and a low noise reference to fit into a single hermetic package, simplifying the task of board design. The T/H and ADC portions of the AD1382 are distinct circuits with inputs and outputs available on separate pins. This functional division allows greatest application flexibility. The AD1382's major functional blocks are shown in Figure 9.

The T/H uses a low noise high performance hybrid amplifier and high speed analog switches to achieve precision performance. It operates as an inverting amplifier during Track mode. Summing junction switch S1 disconnects the analog input to place the circuit into Hold mode; the amplifier's output stays constant because the dc path to its inverting input is broken. S1 also grounds the junction of R1 and R2 to minimize signal feedthrough. Pedestal is independent of the analog input level because all switching is done near ground. This ensures very low nonlinearity and distortion.

A precision reference DAC and an 8-bit flash ADC form the heart of the AD1382's subranging design. High speed amplifiers combine the analog input and DAC output to produce the voltages encoded by the flash ADC during each pass. A logic array provides all necessary timing, control, and computation.

The first rising clock edge after Start Convert goes high begins the conversion (provided the previous conversion is complete). The Hold Command goes high and switches the T/H into hold. The held signal from the T/H goes through S2, S3, and Error Amp 2 to the flash ADC. During this pass Error Amp 2 actually attenuates the ADC input to keep the voltage within the flash ADC's input range. The flash ADC is strobed after a 100 ns settling period. The 8-bit result is saved in the logic array and is routed to the MSBs of the reference DAC.

Error Amp 1 amplifies the difference between the reference DAC output and the held input signal during the second pass. S4 routes this error signal to the flash ADC, which is strobed a second time after Error Amp 1 has settled. The new 8-bit result is used to correct the previous result, increasing the accuracy of this intermediate answer to 13-bit precision. Following this the reference DAC is updated.

Both error amplifiers are active during the third pass. S2 is switched, allowing Error Amp 2 to amplify Error Amp 1's output. S3 now brings Error Amp 2's output to the flash ADC. The flash ADC is strobed a final time after the DAC and both error amplifiers have settled. The logic array combines the data from the third flash conversion with the earlier 13-bit word to produce the final 16-bit result. The T/H is returned to track mode, and Error Amp 2 is reconnected as an attenuator 50 ns after the completion of the third flash conversion to prepare for the next conversion.

The output data are placed on the data bus in two 8-bit bytes to be read by the host system. The Data Strobe output synchronizes the data transfer by providing a rising edge for the first byte and a falling edge for the second byte. The Hi/Lo Byte Select input allows the user to choose which data byte is presented first. B1 Select sets the polarity of the MSB to provide either twos complement or offset binary data.

CONNECTION AND OPERATION OF THE AD1382

Analog Input

The analog input should be connected to the Track/Hold Input (Pin 25). Two pin programmable operating ranges are available: ±5 V and ±10 V. Connect the Track/Hold Output to V_{IN} A and/or V_{IN} B as follows:

Desired Scale	Connect V_{IN} A to	Connect V_{IN} B to
±5 V	Track/Hold Output	Track/Hold Output
±10 V	Track/Hold Output	Analog Signal GND

Harmonic distortion is lower when using the ±5 V range, while noise is lower when using the ±10 V range.

The AD1382's noise and distortion performance exceed the capability of most signal sources. Maintaining this performance at the system level requires attention to every detail of grounding, bypassing, and signal sources. A low impedance high bandwidth signal source is essential to achieve low distortion. Few monolithic amplifiers exist which can maintain signal fidelity at levels comparable with the AD1382's performance, even at low frequencies. High bandwidth means increased noise and decreased SNR. See *Testing the AD1382* for techniques of achieving the lowest possible noise and distortion.

Grounding

Proper treatment of the AD1382's power and ground connections is vital to achieve the best possible system performance. The ideal grounding arrangement is to have a single, solid, low impedance ground plane beneath the device to which all ground and supply bypassing connections are made. This results in the lowest possible ground noise and minimizes undesired interactions between the sensitive circuits inside the AD1382. Aperture uncertainty, for example, can be degraded by noise in Power Ground because the Hold Command signals are referenced to this ground. The digital interface between the AD1382 and the rest of the user's system is also critical. The following discussion will help in obtaining optimal performance. These guidelines are general and apply equally well to other high performance analog and digital circuits.

The AD1382 must connect to three other parts of the system: the input signal(s), the power supplies, and the digital interface. The system designer must determine the magnitude and type of ground currents and whether they are constant or dynamic. A system block diagram is a valuable aid to understanding how grounds should be connected for good performance. Figure 10 shows recommended ground connections for the AD1382 in a typical system.

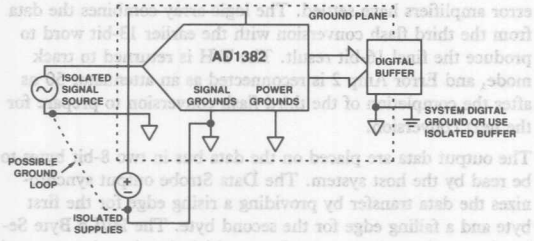


Figure 10. AD1382 Grounding

The AD1382 has a net ground current of about 40 mA. Most of this flows in the power grounds. There are also substantial dynamic currents in the power grounds. The signal grounds have primarily low level static (dc) currents. Signal and power grounds are separated inside the hybrid because the resistance and inductance inherent in thick-film construction would cause interactions between ground currents, leading to poor performance. (Remember that an LSB can be as small as 156 μV.)

Care must be taken to prevent the AD1382's ground currents from flowing in the signal ground between the signal source and the AD1382 if this ground has significant resistance. This is not usually a problem if the signal source is located on the same board as the AD1382 because the resistance can be made very low through the use of a ground plane.

The signal source's ground and supply currents must be considered when the source and ADC share common power supplies. A ground loop formed by the AD1382, the signal source, and the power supplies can cause significant errors.

The connection between the AD1382's ground plane and the system's digital ground is best made away from the AD1382. This will prevent noisy system ground currents from passing through critical parts of the ADC. In a very noisy environment it may be wise to isolate the entire analog circuit. Figure 10 shows the required isolation provided by a digital buffer. The buffer can then drive resistive and/or capacitive loads without compromising ground at the ADC. Using separate isolated supplies for the ADC and signal source will result in a single-point connection between system digital ground and the ADC's ground plane at the digital buffer.

Power Supplies and Bypassing

The AD1382 has four sets of power supply pins. These are:

±5 V Analog	(V_{DD1}/V_{SS1})
±15 V	($+V_{S1}/-V_{S1}$)
±15 V	($+V_{S2}/-V_{S2}$)
±5 V Power	(V_{DD2}/V_{SS2})

A single source may be used to supply like voltages (e.g., V_{DD1}, V_{DD2} from the same +5 V supply). Each of the four ±5 V supply pins should have a distinct low impedance connection to a well-bypassed central source node. This is required because each pin draws large transient currents. These dynamic currents, if passed through a common supply path, would introduce crosstalk and increase the AD1382's apparent noise. The two sets of ±15 V supplies need not be split in this fashion.

Every AD1382 supply pin should be bypassed to the ground plane with a high quality ceramic capacitor of 0.01 μF to 0.1 μF. This capacitor should be located as close as possible to the AD1382 to minimize lead lengths. Each V_{DD} and V_{SS} pin must also be bypassed to the ground plane with a 10 μF solid tantalum bypass capacitor located close to the AD1382. Ten microfarad bypass capacitors for $\pm V_{S2}$ (Pins 21 and 23) are also necessary. These power distribution concepts are shown in Figure 11.

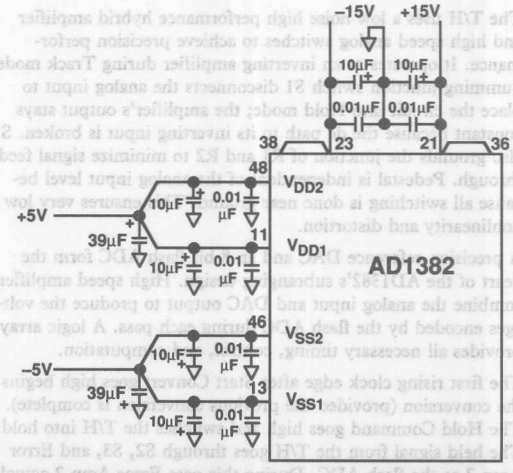


Figure 11. Recommended AD1382 Supply Distribution. All 10 μF and 0.01 μF Capacitors Must Be Located Close to the AD1382. Make All Ground Connections to Groundplane

All power supplies should be of the linear type. Switching power supplies are not recommended as they can introduce considerable high frequency noise into sensitive analog signal paths, degrading the AD1382's apparent performance.

Supply pins of equivalent voltage should not be allowed to differ by more than 0.3 V.

If separate ground planes are used for Signal and Power Ground, the supplies should be bypassed as follows:

Supply	Bypass to
±5 V Analog	Signal Ground
±15 V ($+V_{S1}/-V_{S1}$)	Signal Ground
±15 V ($+V_{S2}/-V_{S2}$)	Power Ground
±5 V Power	Power Ground

Care is also required when using a +5 V powered crystal oscillator to provide the AD1382's clock signal. These devices produce considerable supply noise and proper bypassing is essential. The oscillator should be bypassed with both ceramic and solid tantalum capacitors using minimum lead lengths. A 10 Ω resistor in series with the +5 V supply provides additional isolation and low pass filtering of transients produced by the oscillator.

Reference

The AD1382 has an excellent internal reference with a typical temperature coefficient of 5 ppm/°C. The Reference Out (Pin 39) is normally connected to Reference In (Pin 32). An external reference may be connected to the reference input if desired. The reference input pin requires negligible current. The reference input voltage should not exceed +11 V and must remain more positive than −0.3 V. The reference output requires no bypassing and should not be capacitively loaded. If an external reference is used, it must have low noise to avoid degrading the signal to noise ratio of the AD1382.

The reference output can source up to 2 mA of static (dc) current without affecting the performance of the AD1382.

DIGITAL INTERFACES

10 MHz Clock

The AD1382 requires a stable external clock. A 10 MHz clock provides a sample rate of 500 kilosamples per second. Since the ADC operates synchronously with this clock, clock phase noise will appear as jitter in the aperture time. Lower clock frequencies may be used, and the sample rate will be reduced proportionately.

Standard TTL and CMOS crystal oscillator modules may be used successfully to generate the required 10 MHz clock signal. These oscillators often create considerable power supply transient noise. The oscillator should be bypassed with both ceramic and solid tantalum capacitors using minimum lead lengths. A 10 Ω resistor in series with the +5 V supply provides additional isolation and low-pass filtering of transients produced by the oscillator. See Figure 12.

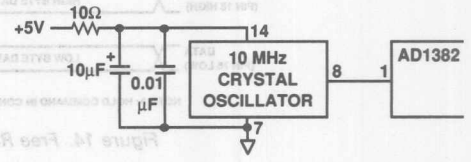


Figure 12. Isolating Clock Noise. Bypass Capacitors Should Be Located Close to the Oscillator

START CONVERT (Pin 18)

Synchronous Operation

The Start Convert signal acts like the data input of a flip-flop. A conversion begins on the first rising clock edge after Start Convert goes high (provided setup time requirements are met). This edge drives Hold Command Out high, switching the T/H into Hold mode. Hold Command Out (Pin 19) should be connected to Hold Command In (Pin 22) for synchronous operation. Continuous conversions at a 500 kHz rate may be obtained by holding Start Convert high. The 10 MHz clock may be divided down and used to drive the Start Convert input when a lower conversion rate is desired. This will provide clock-synchronized conversions at the lower rate. Synchronous conversion timing is shown in Figures 13 and 14.

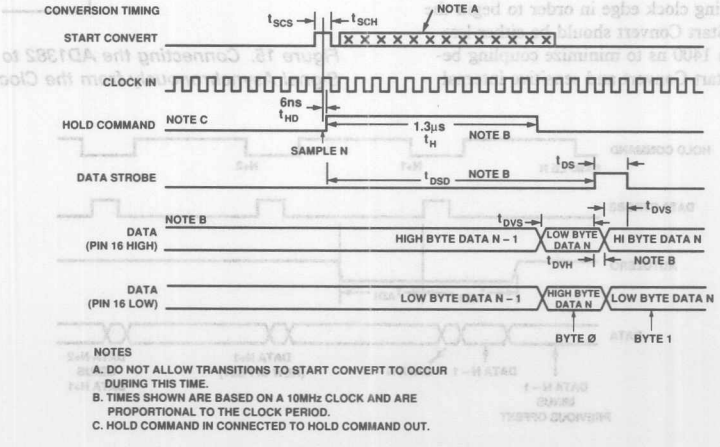


Figure 13. Start-Convert Controlled Conversion Timing

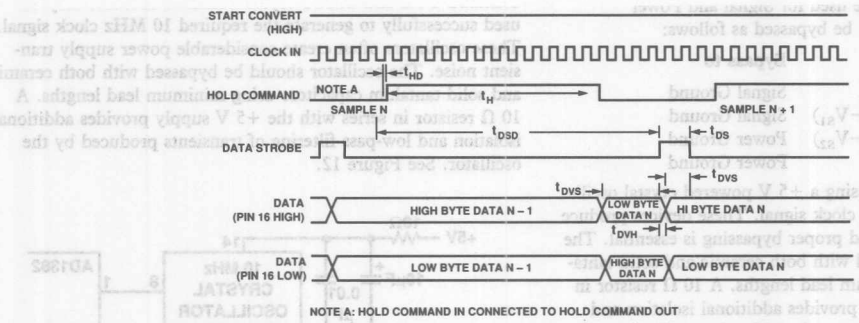


Figure 14. Free Running Conversion Timing

Start Convert may also be used as a gate to capture data only in a time window. The rising and falling edges of Start Convert define the beginning and end of the window during which conversions are desired.

Some restrictions apply to the timing of Start Convert. Transitions on the Start Convert pin should be limited to the 700 ns interval before the rising edge of Hold Command Out and to the 100 ns period after this edge. This minimizes coupling between Start Convert and sensitive internal circuit nodes.

Asynchronous Operation

In synchronous operation the T/H is placed into Hold mode by the first rising clock edge after Start Convert goes high. This mode of operation provides maximum rejection of system clock noise. Some applications may require the AD1382 to operate asynchronously, that is, with the Start Convert input directly controlling the track-to-hold transition. This may be achieved using a 2-input OR gate connected as shown in Figure 15. The rising edge of Start Convert places the T/H into Hold mode; the A/D conversion cycle begins with the first rising clock edge after the Start Convert transition, and Start Convert must remain high during at least one rising clock edge in order to begin the conversion. The width of Start Convert should be either less than 150 ns or greater than 1400 ns to minimize coupling between the falling edge of Start Convert and sensitive internal nodes. In asynchronous operation the T/H will remain in Hold mode as long either Hold Command Out or Start Convert is high. System timing requires careful scrutiny to ensure that the T/H has a minimum of 700 ns for signal acquisition before another conversion begins. The minimum width of Start Convert is 20 ns, the sum of t_{SCS} and t_{SCH}, the minimum setup and hold times.

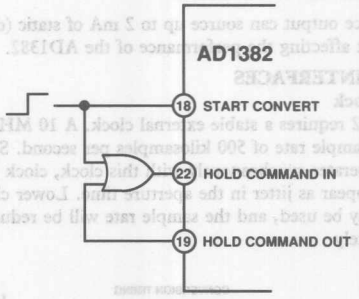


Figure 15. Connecting the AD1382 to Sample the Input Signal Asynchronously from the Clock

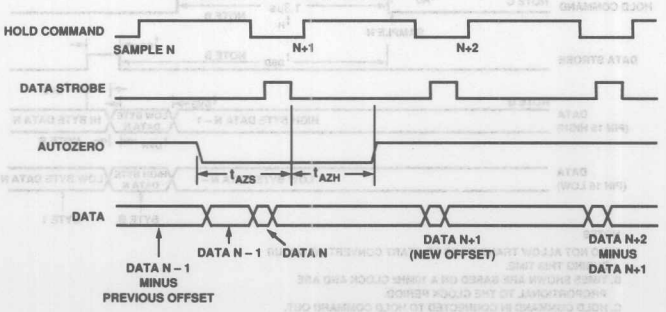


Figure 16. Autozero Cycle Operation

Output Data

The output data are multiplexed in two bytes onto an 8-bit data bus. Data are guaranteed to be stable at the time of the edges of Data Strobe (Pin 15). Hi/Lo Byte Select (Pin 16) controls which byte is presented first. If Hi/Lo Byte Select is high, then BYTE0 is B9–B16 and BYTE1 is B1–B8. The order of the data bytes is interchanged when Hi/Lo Byte Select is low. BYTE 0 and BYTE 1 are defined in the timing diagram Figure 13. B1 is the most significant bit of the reconstructed 16-bit data.

B1 SELECT (Pin 44) determines whether data is presented in complementary twos complement or complementary offset binary form. Complementary twos complement data is provided when B1 Select is LOW. $\overline{OE}$ may be used to place the data bus into a high impedance state.

The arithmetic unit in the AD1382 saturates at all 0s or all 1s if the input range is exceeded.

AUTOZERO (Pin 45)

The Autozero function may be used to digitally correct internal offsets in the Track/Hold and ADC as well as external offsets. To use Autozero the Track/Hold input must be connected to a zero reference prior to the zeroing conversion. This connection is external to the AD1382 and must be provided by the user; the resistance of this connection is not critical but should be less than 1000 Ω. An Autozero cycle forces the AD1382's digital output to indicate exactly zero when its input is at the zero point, nominally 0 V. (This assumes that the twos complement data format is used. Autozero forces the digital output to mid-scale when the selected data format is offset binary.) Autozero operates by storing the digital result of a zeroing conversion and subtracting it from all subsequent conversion results. This reduces the maximum nonsaturating input of the AD1382 a small amount at one end of its range depending on the magnitude and polarity of the offset.

The Autozero feature is enabled by driving the Autozero Input (Pin 45) low at the time of a falling edge at the Data Strobe output. Offset data will be stored on the first falling edge of Data Strobe after Autozero is brought high; the offset data are also available on the AD1382's data bus during this Data Strobe pulse. Autozero operation is illustrated in Figure 16. All subsequent A/D conversions will be digitally corrected by the offset term as long as Autozero remains high. The offset register is cleared when Autozero goes low and the contents of the data output registers will revert to their uncorrected value. Figure 17 shows Autozero timing requirements. Autozero cannot be activated until the first conversion after powerup has been completed.

The Autozero feature may be disabled by keeping Autozero low.

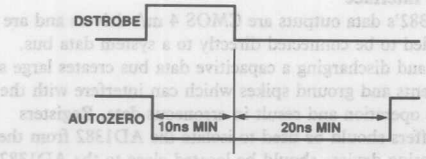


Figure 17. Autozero Setup and Hold Times

GAIN ADJUST (Pin 40)

The internal reference of the AD1382 may be adjusted by varying the voltage applied to the Gain Adjust pin. The input impedance of this pin is nominally 20 kΩ, with a tolerance of ±20%. A change of 1 V on Pin 40 will change the reference voltage by about 10 mV. The reference may be adjusted by ±150 mV without degrading the AD1382's performance. The simplest method of implementing the gain adjust is to connect a potentiometer between the ±15 V supplies, with the wiper connected to the Gain Adjust pin. Care should be taken to ensure that noise does not enter the ADC through the Gain Adjust pin.



Figure 18a. AD1382 Gain Adjust Circuit

OFFSET ADJUST (Pin 29)

The ADC's offset voltage may be adjusted by means of a voltage applied to the Offset Adjust pin. The nominal adjustment sensitivity is 0.005% FSR/V. The input impedance is 20 kΩ with a ±20% tolerance. The simplest way to implement the offset adjust is to connect a potentiometer between the ±15 V supplies, with the wiper connected to the Offset Adjust pin. Care should be taken to ensure that noise does not enter the ADC through the Offset Adjust pin.



Figure 18b. AD1382 Offset Adjust Circuit

APPLICATIONS

Mounting and Thermal Considerations

Although the AD1382 will operate over a wide temperature range, best performance is obtained by maintaining the case temperature between 40°C and 70°C. This can usually be achieved without a heat sink provided there is a moderate amount of air flow. Under these conditions the case temperature will rise about 20°C. Performance will degrade gradually outside the specified temperature range due to linearity drift in the reference DAC.

System thermal analysis or experimental evidence may show that a heat sink is necessary. A thin heat transfer plate can be mounted under the package to conduct heat into the ground plane. This plate may be made of metal or from an elastomeric heat conducting material. Elastomeric materials will conform to the board and to the AD1382 package to improve heat transfer while reducing mechanical stress. They also have the advantage of not requiring thermally conductive grease.

Testing the AD1382

It is difficult to test the AD1382 with ordinary test methods because of the part's very low distortion and noise. The number of output codes and the nature of the analog to digital conversion make static tests of performance especially cumbersome. Subranging converters with error correction circuitry can have flaws at any place in their transfer function and all codes must be exercised for a complete test.

Histograms provide a convenient way to measure all codes in a modest amount of time. Even histograms can be slow, though, when 20 million conversions (40 seconds) may be required to achieve statistically valid results.

Distortion and dynamic range tests based on FFTs are the most powerful tests. They quantify noise and nonlinearity as a function of input frequency. From them one can infer qualitative integral and differential nonlinearity performance while determining the ADC's specific dynamic performance. FFTs are especially useful for systems which require excellent dynamic response, such as magnetic resonance imaging. They also uncover performance problems that don't show up in static tests of linearity.

The difficulty in doing FFT tests stems from the requirement for ultra pure sine wave inputs at various frequencies over the operating bandwidth of the ADC. Even the best available generators are not capable of supplying signals with sufficiently low noise and low distortion for testing the AD1382. Few generators permit phase-locking to the ADC clock. Phase-locking makes it possible to obtain an integral number of cycles of the input sine wave within the FFT data window, which in turn eliminates the need for windowing functions and the spectral spreading they cause.

The best generator currently available for this purpose is the Brüel and Kjær Model 1051 (or 1049). This generator provides a programmable output frequency up to 250 kHz with better than 0.001 Hz resolution. The generator's distortion performance at frequencies below 20 kHz is better than the AD1382 but degrades at 100 kHz and higher. Noise is a problem at all frequencies, being about −85 dB over the AD1382's bandwidth. Both noise and distortion can be reduced to acceptable levels with filters. Passive filters with narrow bandwidth will reduce harmonic distortion to less than −100 dB. Inductors wound on large pot cores with air gaps can be made quite linear, and with careful winding will provide low loss and low capacitance. Such filters will reduce noise to negligible levels outside their pass band to provide a much better view of actual ADC performance. The effect of aperture jitter, for example, cannot be observed without a filter.

The FFTs shown in Figures 1–8 were produced using these methods. These tests are done as a normal part of production testing to guarantee the dynamic performance of the AD1382.

High Impedance Inputs

Using the AD1382 in multiplexed applications requires buffering the part's 2.5 kΩ input impedance to eliminate the distorting effects of nonlinear multiplexer on-resistance. The choice of buffer amplifier depends on the nature of the input signals.

"Static" Applications

Amplifier noise, CMRR linearity, and settling time are of primary importance when the inputs are low frequency or DC. This is the case in a CAT scan imager, for example, when signals are produced by integrating photocurrents. Noise limits ultimate system resolution. The AD1382 has a typical input-referred noise of 55 μV rms. Buffer noise must be added to this in a root-sum-squares fashion to determine total system noise. A buffer amplifier which adds noise of 18 μV rms, for example, will result in a system noise level of $(18^2+55^2)^{1/2} = 58$ μV rms, a negligible increase. Detailed system noise calculations require knowledge of the buffer's noise spectral density and equivalent noise bandwidth. The AD1382's equivalent noise bandwidth is 2.2 MHz. *Low Noise Electronic Design* (C.D. Motchenbacher and F.C. Fitchen, John Wiley and Sons, New York, 1973) provides excellent discussions of noise analysis and calculations.

Buffer amplifier CMRR produces an apparent gain error as long as the value of CMRR is independent of signal level. The size of this "gain error" is directly related to the actual value of CMRR; an amplifier with 60 dB CMRR will create an apparent gain error of 0.1%. The precise value of CMRR is not critical as long as it remains constant with signal level. Any variation in CMRR with input level will introduce nonlinearity. The smaller the value of CMRR (in dB), the more critical variations in this value become. An amplifier with CMRR ranging from 100 dB to 110 dB over the range of −10 V to +10 V will produce negligible nonlinearity, while an amplifier whose CMRR varies from 60 dB to 70 dB over the same range would be completely unacceptable.

Buffer settling time will affect the system's throughput. The system sample rate can be maintained at 500 kHz provided the buffer's settling time is less than about 1.7 microseconds. The input channel should be switched just after the AD1382's SHA enters Hold mode as indicated by a rising edge at Hold Command In (Pin 22).

"Dynamic" Applications

Dynamic applications complicate the choice of buffer amplifier. The amplifier's harmonic distortion performance now becomes as important as its noise, CMRR linearity, and settling behavior. Few manufacturers specify amplifier THD in the noninverting configuration. These specifications, when available, seldom address signals greater than 10 V p–p or at frequencies above 1 kHz. It may be necessary to characterize candidate amplifiers from several vendors to find the best fit to the particular amplitude and frequency requirements of a particular application. Such evaluations are easily performed using a spectrum analyzer. A notch filter tuned to the fundamental frequency greatly improves measurement resolution. It is also possible to use the AD1382 as the measuring device by performing FFTs on the output data. Refer to the discussion of signal sources in *Testing the AD1382*.

Unipolar Operation

The AD1382 does not provide a direct unipolar input capability. Unipolar inputs can be achieved using the circuits of Figures 19 and 20. The circuit in Figure 19 is suitable when a low input impedance is acceptable. Multiplexed applications should use the circuit of Figure 20. The discussions under High Impedance Inputs also apply to amplifier selection for unipolar operation.

Data Bus Interface

The AD1382's data outputs are CMOS 4 mA drivers and are not intended to be connected directly to a system data bus. Charging and discharging a capacitive data bus creates large supply transients and ground spikes which can interfere with the AD1382's operation and result in erroneous data. Registers and/or buffers should be used to isolate the AD1382 from the bus. Buffering devices should be located close to the AD1382 to minimize the capacitive load presented to the converter's data outputs. Control will be simplified by permanently grounding the AD1382's $\overline{OE}$ input when using buffers. A schematic of a typical 16-bit bus interface is shown in Figure 21.

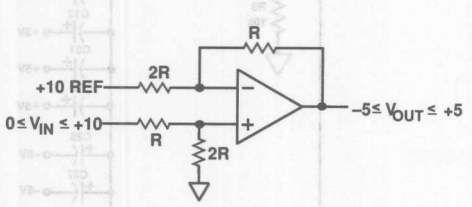


Figure 19. Unipolar-to-Bipolar Conversion (Low Input Impedance)

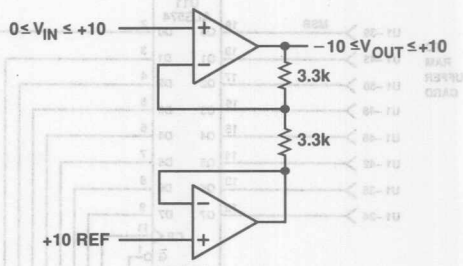


Figure 20. High Input Impedance Unipolar-to-Bipolar Conversion Circuit

Sample Board Layout

Figures 22–27 show the layout of an evaluation board for the AD1382. This layout incorporates the grounding, power distribution, and interface concepts described in previous sections. This 4-layer layout makes extensive use of ground and power planes and provides optimal AD1382 performance.

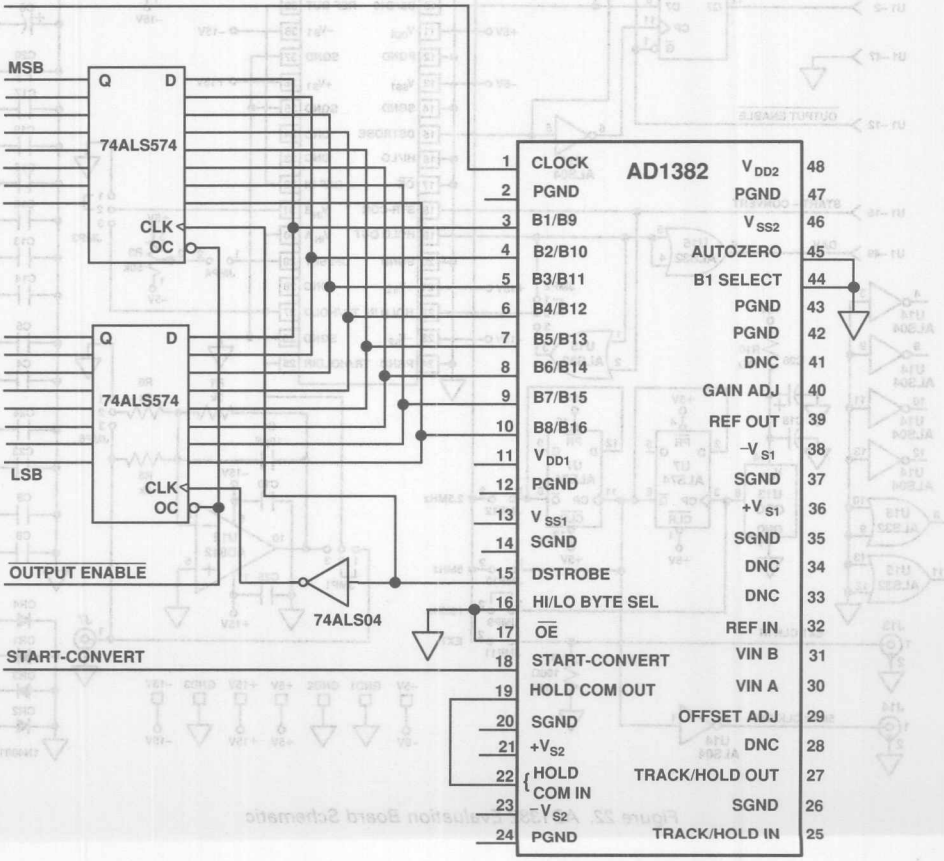


Figure 21. Basic AD1382 Digital Interface (16-Bit 2s Complement Data, Autozero Not Used)

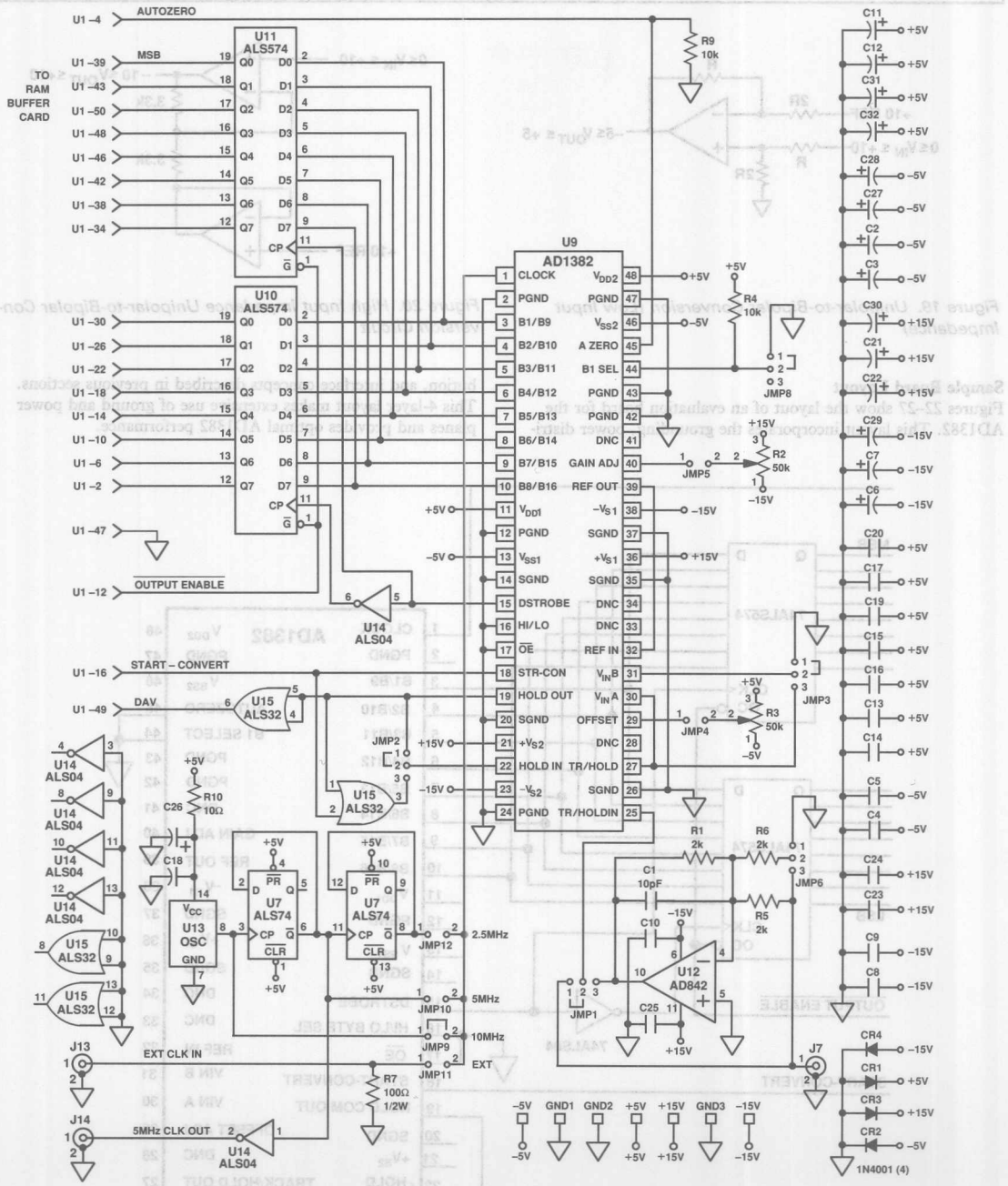


Figure 22. AD1382 Evaluation Board Schematic

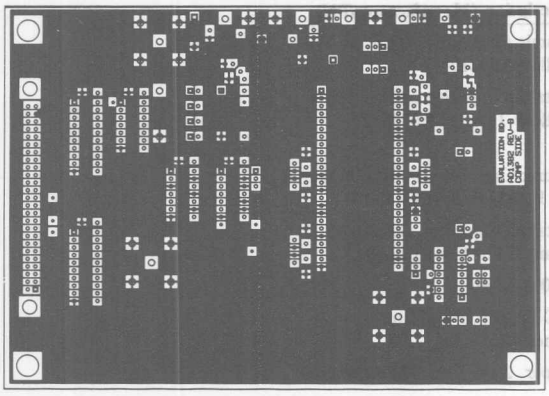


Figure 23. AD1382 Evaluation Board Layout, Layer 1 (Component Side)

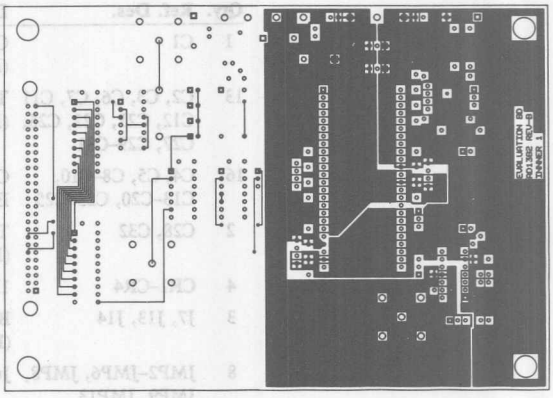


Figure 24. AD1382 Evaluation Board Layout, Layer 2

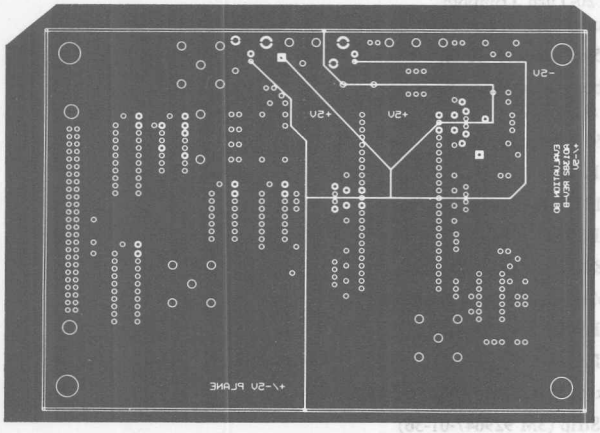


Figure 25. AD1382 Evaluation Board Layout, Layer 3

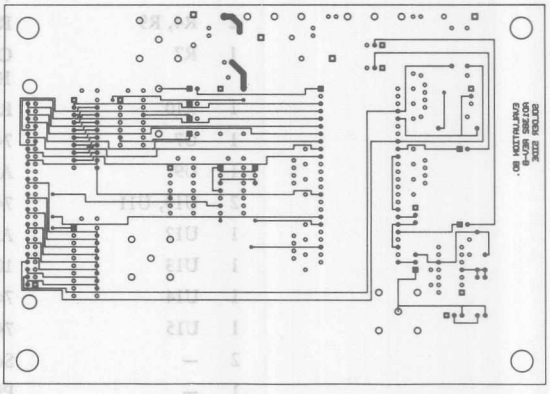


Figure 26. AD1382 Evaluation Board Layout, Layer 4 (Solder Side)

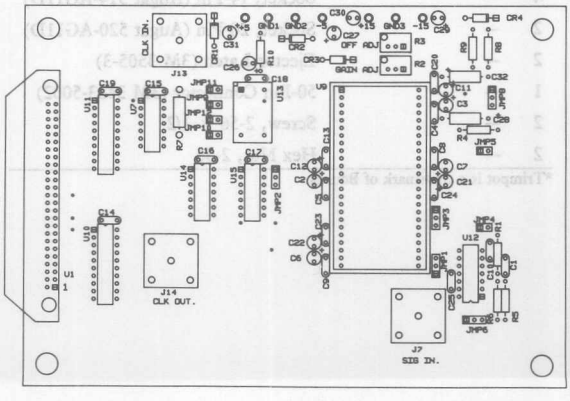


Figure 27. AD1382 Evaluation Board Silkscreen

Qty.	Ref. Des.	Description (Manufacturer/PN)
1	C1	Ceramic Capacitor, 10 pF, 50 V (Mallory CEC100J)
13	C2, C3, C6, C7, C11 C12, C21, C22, C26, C27, C29–C31	Tantalum Capacitor, 10 μF, 35 V (Mallory TDL106K035S1D)
16	C4, C5, C8–C10, C13–C20, C23–C25	Ceramic Cap, 0.1 μF, 100 V (Murata Erie RPE122Z5U104M100V)
2	C28, C32	Tantalum Capacitor, 39 μF, 10 V (Kemet T110B396K010AS)
4	CR1–CR4	1N4001 Diode
3	J7, J13, J14	BNC Female, PC Mount (Pomona 4578)
8	JMP2–JMP6, JMP8, JMP9, JMP13	Jumper, 2 Position (3M 929950-00)
3	R1, R5, R6	RN55C Resistor, 2.00k
2	R2, R3	50k 20-Turn Trimpot* (Bourns 3299W-1-503)
2	R4, R9	RN55C Resistor, 10.0k
1	R7	Carbon Composition Resistor, 100 Ω, 1/2 W
1	R10	RN55C Resistor, 10 Ω
1	U7	74ALS74
1	U9	AD1382KD (Analog Devices)
2	U10, U11	74ALS574
1	U12	AD842KN (Analog Devices)
1	U13	10 MHz DIP Crystal Oscillator
1	U14	74ALS04
1	U15	74ALS32
2	—	Socket Strip (SPC MPS1P-32-GG)
1	—	Pin Strip (3M 929647-01-36)
1	—	Socket, 14-Pin Oscillator (Augat 504-AG10D)
4	—	Socket, 14-Pin (Augat 514-AG11D)
2	—	Socket, 20-Pin (Augat 520-AG11D)
2	—	Ejector Latch (3M 3505-3)
1	—	50-Pin Connector (3M 3433-5002)
2	—	Screw, 2-56 × 1/2
2	—	Hex Nut, 2-56

*Trimpot is a trademark of Bourns.

16-Bit 500 kHz Wide Temperature Range Sampling ADC

AD1385

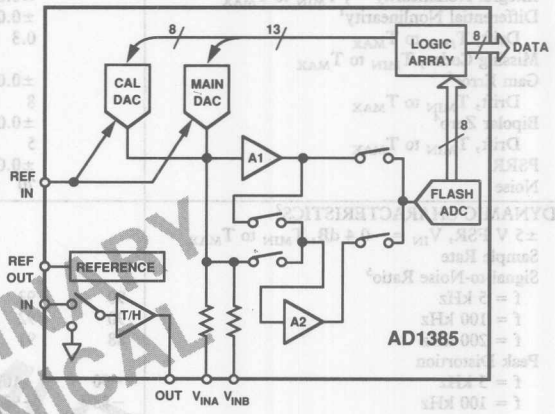
PRODUCT FEATURES

16-Bit Resolution
500 kHz Sampling Rate
Differential Linearity Autocalibration
Specified over −55°C to +125°C Range
SNR 90 dB @ 100 kHz (min)
THD −88 dB @ 100 kHz (min)
0.0006% FSR DNL (typ)
0.0015% FSR INL (typ)
±5, ±10 V Bipolar Input Ranges
Zero Offset Autocalibration

APPLICATIONS

Medical Imaging
CAT
Magnetic Resonance
Radar
Vibration Analysis
Parametric Measurement Unit (ATE)
Digital Storage Oscilloscopes
Waveform Recorders
Analytical Instruments

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

The AD1385 is a complete 500 kHz, 16-bit, sampling analog-to-digital converter contained in a single package. Its differential linearity autocalibration feature allows this high resolution, high speed converter to offer outstanding noise and distortion performance, as well as excellent INL and DNL specifications, over the full military temperature range. Autocalibration effectively eliminates DNL drift over temperature.

The AD1385 architecture includes a low noise, low distortion track/hold, a three pass digitally corrected subranging ADC, and linearity calibration circuitry. A complete linearity calibration requires only 15 ms. Precision thin-film resistors and a proprietary DAC contribute to the part's outstanding dynamic and static performance.

The AD1385 uses four power supplies, ±5 V and ±15 V, and an external 10 MHz clock. Power dissipation is nominally 2.76 W. Two user selectable bipolar input ranges, ±5 V and ±10 V, are provided. Careful attention to grounding and a single package make it easy to design PCBs to achieve specified performance.

The AD1385's pinout is nearly identical to that of the AD1382. Just two additional connections, to enable and monitor autocalibration, are required. This commonality provides an easy upgrade path to extend system performance and operating temperature range.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD1385—SPECIFICATIONS (T_A = +25°C, V_S = ±15 V, V_{DD} = +5 V, V_{SS} = −5 V, 10 MHz External Clock, unless otherwise noted)

Parameter	AD1385KD Min	AD1385KD Typ	AD1385KD Max	AD1385TD Min	AD1385TD Typ	AD1385TD Max	Units
RESOLUTION	16			16			Bits
ANALOG INPUT							
Input Ranges		±5, ±10			±5, ±10		V
Input Impedance	2.45	2.5	2.55	2.45	2.5	2.55	kΩ
TRANSFER CHARACTERISTICS							
(Combined ADC/Track/Hold)							
Integral Nonlinearity[1, 2], T_{MIN} to T_{MAX}		±0.0015			±0.0015		% FSR[3]
Differential Nonlinearity[1]		±0.0006	±0.0015		±0.0006	±0.0015	% FSR
Drift, T_{MIN} to T_{MAX}		0.3			0.3		ppm/°C
Missing Codes, T_{MIN} to T_{MAX}			None			None	
Gain Error[4]		±0.05	±0.15		±0.05	±0.15	% FSR
Drift, T_{MIN} to T_{MAX}		8	15		8	15	ppm/°C
Bipolar Zero[4]		±0.05	±0.10		±0.05	±0.10	% FSR
Drift, T_{MIN} to T_{MAX}		5	15		5	15	ppm/°C
PSRR		±0.006	±0.10		±0.006	±0.10	% FSR/V
Noise		70			70		μV RMS
DYNAMIC CHARACTERISTICS[2]							
±5 V FSR, V_{IN} = −0.4 dB, T_{MIN} to T_{MAX}							
Sample Rate			500			500	kHz
Signal-to-Noise Ratio[5]							
f = 5 kHz	90	93		90	93		dB
f = 100 kHz	90	92		90	92		dB
f = 200 kHz	88	91		88	91		dB
Peak Distortion							
f = 5 kHz	−90	−107		−90	−107		dB
f = 100 kHz	−88	−95		−88	−95		dB
f = 200 kHz	−82	−88		−82	−88		dB
Total Harmonic Distortion[6]							
f = 5 kHz	−90	−105		−90	−105		dB
f = 100 kHz	−88	−95		−88	−95		dB
f = 200 kHz	−82	−88		−82	−88		dB
DYNAMIC CHARACTERISTICS[2]							
±10 V FSR, V_{IN} = −0.4 dB, T_{MIN} to T_{MAX}							
Sample Rate			500			500	kHz
Signal-to-Noise Ratio[5]							
f = 5 kHz	90	95		90	95		dB
f = 100 kHz	90	94		90	94		dB
f = 200 kHz	88	93		88	93		dB
Peak Distortion							
f = 5 kHz	−90	−108		−90	−108		dB
f = 100 kHz	−80	−87		−80	−87		dB
f = 200 kHz	−74	−82		−74	−82		dB
Total Harmonic Distortion[6]							
f = 5 kHz	−90	−105		−90	−105		dB
f = 100 kHz	−80	−87		−80	−87		dB
f = 200 kHz	−74	−82		−74	−82		dB
DIGITAL INPUTS[7]							
Input Voltage							
V_{IL}			0.8			0.8	V
V_{IH}	2.25			2.25			V
Input Current			±200			±200	μA
Input Capacitance		2			2		pF
Start Command							
Setup Time, t_{SCS}	10			10			ns
Hold Time, t_{SCH}	10			10			ns
Autozero							
Setup Time, t_{AZS}	10			10			ns
Hold Time, t_{AZH}	20			20			ns
Calibrate Pulsewidth	20			20			ns
Clock							
Frequency	2.5		10	2.5		10	MHz
Duty Cycle	40		60	40		60	%
Aperture Delay[8]		7			7		ns

PRELIMINARY TECHNICAL DATA

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Parameter	AD1385KD Min	AD1385KD Typ	AD1385KD Max	AD1385TD Min	AD1385TD Typ	AD1385TD Max	Units
DIGITAL OUTPUTS[7]							
Output Voltage							
V_{OL} @ I_{OL} = 3.2 mA		0.2	0.4		0.2	0.4	V
V_{OH} @ I_{OH} = −3.2 mA	2.4	3.5		2.4	3.5		V
Output Capacitance		10			10		pF
Leakage, Outputs Disabled			±200			±200	μA
Data Valid							
Setup Time, t_{DVS}	75	125		75	125		ns
Hold Time, t_{DVH}	25	50		25	50		ns
Hold Command Time, t_H		1300			1300		ns
Hold Command Delay, t_{HD}		6			6		ns
Data Strobe Pulse Width, t_{DS}		200			200		ns
Data Strobe Delay, t_{DSD}		1650			1650		ns
Calibration Status Duration		15			15		ms
OUTPUT CODING	Complementary Offset Binary or Complementary Twos Complement						
INTERNAL REFERENCE							
Voltage	9.990		10.010	9.990		10.010	V
Current	2	5		2	5		mA
Drift		5	15		5	15	ppm/°C
TEMPERATURE RANGE, CASE							
Specified	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	°C
POWER REQUIREMENTS							
Specified Operating Range							
$\pm V_S$	14.25		15.75	14.25		15.75	V
$+V_{DD}$	4.75		5.25	4.75		5.25	V
$-V_{SS}$	−5.25		−4.75	−5.25		−4.75	V
Current Drains							
$+V_S$		52	80		52	80	mA
$-V_S$		48	75		48	75	mA
$+V_{DD}$		104	160		104	160	mA
$-V_{SS}$		148	200		148	200	mA
Power Dissipation		2.76	4.125		2.76	4.125	Watts

PRELIMINARY TECHNICAL DATA

NOTES
[1]Integral linearity is inferred from FFTs. Differential linearity is derived from histograms.
[2]Performance over temperature is specified within ±15°C of the temperature at which the last calibration was performed.
[3]FSR = Full-Scale Range.
[4]Adjustable to zero.
[5]SNR excludes harmonics 2–9 of the fundamental.
[6]THD includes harmonics 2–9 of the fundamental.
[7]Refer to Figures 17, 18 and 24. Guaranteed over operating temperature range, not 100% production tested.
[8]Aperture delay is the time from the rising edge on the Hold Command Input to the opening of the switch in the Track/Hold.
Specifications subject to change without notice.

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$-V_S$ to AGND	−18 V
V_{DD} to PGND	7 V
V_{SS} to PGND	−7 V
AGND to PGND	±0.3 V
Analog Inputs	$\pm V_S$
Reference Input	0 V to +11 V
Digital Inputs	−0.3 V to V_{DD} + 0.3 V
Output Short Circuit Duration	
Reference Output	Indefinite
Track/Hold Output	1 sec
Digital Outputs	1 sec for Any One Output
Case Temperature (Operating)	−55°C to +125°C
Storage Temperature	−65°C to +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range (Case)	Package Option*
AD1385KD	0°C to +70°C	DH-48A
Ad1385TD	−55°C to +125°C	DH-48A
AD1385TD/883B	−55°C to +125°C	DH-48A

*DH-48A = Bottom Brazed Ceramic DIP. For outline information see Package Information section.

tub package. The pinout is as follows:

Pin	Function	Pin	Function
1	CLOCK IN	48	V_{DD2} (+5 V POWER)
2	POWER GROUND	47	POWER GROUND
3	B1/B9 (MSB)	46	V_{SS2} (−5 V POWER)
4	B2/B10	45	AUTOZERO
5	B3/B11	44	B1 SELECT
6	B4/B12	43	POWER GROUND
7	B5/B13	42	POWER GROUND
8	B6/B14	41	$\overline{CAL}$
9	B7/B15	40	GAIN ADJUST
10	B8/B16 (LSB)	39	+10 V REFERENCE OUT
11	V_{DD1} (+5 V SIGNAL)	38	$-V_{S1}$ (−15 V)
12	POWER GROUND	37	SIGNAL GROUND
13	V_{SS1} (−5 V SIGNAL)	36	$+V_{S1}$ (+15 V)
14	SIGNAL GROUND	35	SIGNAL GROUND
15	DATA STROBE	34	DNC
16	HI/LO BYTE SELECT	33	DNC
17	$\overline{OE}$ DATA ENABLE	32	+10 V REFERENCE IN
18	START CONVERT	31	V_{IN} B
19	HOLD COMMAND OUT	30	V_{IN} A
20	SIGNAL GROUND	29	OFFSET ADJUST
21	$+V_{S2}$ (+15 V)	28	CAL STATUS
22	HOLD COMMAND IN	27	TRACK/HOLD OUTPUT
23	$-V_{S2}$ (−15 V)	26	SIGNAL GROUND
24	POWER GROUND	25	TRACK/HOLD INPUT

DNC = DO NOT CONNECT

PRELIMINARY TECHNICAL DATA

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



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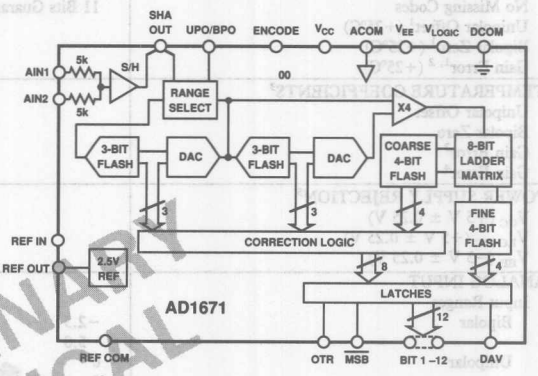
Complete 12-Bit 1.25 MSPS Monolithic A/D Converter

AD1671

FEATURES

Conversion Time: 800 ns
1.25 MHz Throughput Rate
Complete: On-Chip Sample-and-Hold Amplifier and Voltage Reference
Low Power Dissipation: 570 mW
No Missing Codes Guaranteed
Signal-to-Noise Plus Distortion Ratio
f_{IN} = 100 kHz: 69 dB Minimum
Pin Configurable Input Voltage Ranges
Twos Complement or Offset Binary Output Data
28-Pin DIP or 28-Pin Surface Mount Package
Out of Range Indicator

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1671 is a monolithic 12-bit, 1.25 MSPS analog-to-digital converter with an on-board, high performance sample-and-hold amplifier (SHA) and voltage reference. The AD1671 guarantees no missing codes over the full operating temperature range. The combination of a merged high speed bipolar/CMOS process and a novel architecture results in a combination of speed and power consumption far superior to previously available hybrid implementations. Additionally, the greater reliability of monolithic construction offers improved system reliability and lower costs than hybrid designs.

The fast settling input SHA is equally suited for both multiplexed systems that switch negative to positive full-scale voltage levels in successive channels and sampling inputs at frequencies up to and beyond the Nyquist rate. The AD1671 provides both reference output and reference input pins, allowing the on-board reference to serve as a system reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application.

The AD1671 uses a subranging flash conversion technique, with digital error correction for possible errors introduced in the first part of the conversion cycle. An on-chip timing generator provides strobe pulses for each of the four internal flash cycles. A single ENCODE pulse is used to control the converter. The digital output data is presented in twos complement or offset binary output format. An out-of-range signal indicates an overflow condition. It can be used with the most significant bit to determine low or high overflow.

The performance of the AD1671 is made possible by using high speed, low noise bipolar circuitry in the linear sections and low power CMOS for the logic sections. Analog Devices' ABCMOS-1 process provides both high speed bipolar and 2-micron CMOS devices on a single chip. Laser trimmed thin-film resistors are used to provide accuracy and temperature stability.

The AD1671 is available in two performance grades and three temperature ranges. The AD1671J and K grades are available over the 0°C to +70°C temperature range. The AD1671A grade is available over the −40°C to +85°C temperature range. The AD1671S grade is available over the −55°C to +125°C temperature range.

PRODUCT HIGHLIGHTS

The AD1671 offers a complete single chip sampling 12-bit, 1.25 MSPS analog-to-digital conversion function in a 28-pin package.

The AD1671 at 570 mW consumes a fraction of the power of currently available hybrids.

An OUT OF RANGE output bit indicates when the input signal is beyond the AD1671's input range.

Input signal ranges are 0 V to +5 V unipolar or ±5 V bipolar, selected by pin strapping, with an input resistance of 10 kΩ. The input signal range can also be pin strapped for 0 V to +2.5 V unipolar or ±2.5 V bipolar with an input resistance of 10 MΩ.

Output data is available in unipolar, bipolar offset or bipolar twos complement binary format.

PRELIMINARY TECHNICAL DATA

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AD1671—SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −5 V ± 5%, unless otherwise indicated)

Parameter	AD1671J/A/S Min	AD1671J/A/S Typ	AD1671J/A/S Max	AD1671K Min	AD1671K Typ	AD1671K Max	Units
RESOLUTION	12			12			Bits
CONVERSION TIME			800			800	ns
ACCURACY							
Integral Nonlinearity (INL)		±1.5	±2		±0.7	±1.5	LSB
Differential Nonlinearity (DNL)	11			12			Bits
No Missing Codes	11 Bits Guaranteed			12 Bits Guaranteed			
Unipolar Offset[1] (+25°C)			±8			±8	LSB
Bipolar Zero[1] (+25°C)			±10			±10	LSB
Gain Error[1, 2] (+25°C)		0.1	0.25		0.1	0.25	% FSR
TEMPERATURE COEFFICIENTS[3]							
Unipolar Offset			±10			±10	ppm/°C
Bipolar Zero			±15			±15	ppm/°C
Gain Error[3]			±30			±30	ppm/°C
Gain Error[4]			±20			±20	ppm/°C
POWER SUPPLY REJECTION[5]							
V_{CC} (+5 V ± 0.25 V)			±2			±2	LSB
V_{LOGIC} (+5 V ± 0.25 V)			±2			±2	LSB
V_{EE} (−5 V ± 0.25 V)			±2			±2	LSB
ANALOG INPUT							
Input Ranges							
Bipolar	−2.5		+2.5	−2.5		+2.5	Volts
	−5.0		+5.0	−5.0		+5.0	Volts
Unipolar	0		+2.5	0		+2.5	Volts
	0		+5.0	0		+5.0	Volts
Input Resistance							
(0 V to +2.5 V or ±2.5 V Range)		10			10		MΩ
(0 V to +5.0 V or ±5 V Range)	8	10	12	8	10	12	kΩ
Input Capacitance		10			10		pF
Aperture Delay		15			15		ns
Aperture Jitter		20			20		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage		2.5			2.5		Volts
Output Current							
Unipolar Mode			+2.5			+2.5	mA
Bipolar Mode			+1.0			+1.0	mA
LOGIC INPUTS							
High Level Input Voltage, V_{IH}	2.0			2.0			Volts
Low Level Input Voltage, V_{IL}			0.8			0.8	Volts
High Level Input Current, I_{IH} (V_{IN} = V_{LOGIC})	−10		+10	−10		+10	μA
Low Level Input Current, I_{IL} (V_{IN} = 0 V)	−10		+10	−10		+10	μA
Input Capacitance, C_{IN}		5			5		pF
LOGIC OUTPUTS							
High Level Output Voltage, V_{OH} (I_{OH} = 0.5 mA)	2.4			2.4			Volts
Low Level Output Voltage, V_{OL} (I_{OL} = 1.6 mA)			0.4			0.4	Volts
POWER SUPPLIES							
Operating Voltages							
V_{CC}	+4.75		+5.25	+4.75		+5.25	Volts
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	Volts
V_{EE}	−4.75		−5.25	−4.75		−5.25	Volts
Operating Current							
I_{CC}		55	68		55	68	mA
I_{LOGIC}[6]		3	5		3	5	mA
I_{EE}		−55	−68		−55	−68	mA
POWER CONSUMPTION		570	750		570	750	mW
TEMPERATURE RANGE (SPECIFIED)							
J/K	0		+70	0		+70	°C
A	−40		+85	−40		+85	°C
S	−55		+125	−55		+125	°C

NOTES
[1]Adjustable to zero with external potentiometers.
[2]Includes internal voltage reference error.
[3]+25°C to T_{MIN} and +25°C to T_{MAX}.
[4]Excludes internal reference drift.
[5]Change in gain error as a function of the dc supply voltage.
[6]Tested under static conditions. See Figure 10 for typical curve of I_{LOGIC} vs. load capacitance at maximum f_C.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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AC SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −5 V ± 5%, f_{SAMPLE} = 1 MSPS, f_{INPUT} = 100 kHz, unless otherwise noted)[1]

Parameter	AD1671J/A/S Min	AD1671J/A/S Typ	AD1671J/A/S Max	AD1671K Min	AD1671K Typ	AD1671K Max	Units
SIGNAL-TO-NOISE PLUS DISTORTION RATIO (S/N + D)							
−0.5 dB Input	69	70		70	71		dB
−20 dB Input		50			51		dB
EFFECTIVE NUMBER OF BITS (ENOB)	11.2			11.3			
TOTAL HARMONIC DISTORTION (THD)		−80	−75		−83	−78	dB
SPURIOUS FREE DYNAMIC RANGE		−80	−77		−81	−78	dB
SMALL SIGNAL BANDWIDTH		12			12		MHz
FULL POWER BANDWIDTH		2			2		MHz
INTERMODULATION DISTORTION (IMD)[2]							
2nd Order Products		−80	TBD		−80	TBD	dB
3rd Order Products		−85	TBD		−85	TBD	dB

NOTES
[1]f_{IN} amplitude = −0.5 dB (9.44 V p–p) bipolar mode full scale unless otherwise indicated. All measurements referred to a 0 dB (±5 V) input signal, unless otherwise indicated.
[2]f_A = 99 kHz, f_B = 100 kHz with f_{SAMPLE} = 1 MSPS.
Specifications subject to change without notice.

SWITCHING SPECIFICATIONS (For all grades T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −5 V ± 5%; V_{IL} = 0.8 V, V_{IH} = 2.0 V, V_{OL} = 0.4 V and V_{OH} = 2.4 V)

Parameters	Symbol	Min	Typ	Max	Units
Conversion Time	t_C			800	ns
ENCODE Pulse Width High (Figure 1a)	t_{ENC}	20		50	ns
ENCODE Pulse Width Low (Figure 1b)	t_{ENCL}	20			ns
DAV Pulse Width	t_{DAV}	150		300	ns
ENCODE Falling Edge Delay	t_F	0			ns
Start New Conversion Delay	t_R	20			ns
Data and OTR Delay from DAV Falling Edge	t_{DD}[1]	20	75		ns
Data and OTR Valid before DAV Rising Edge	t_{SS}[2]	20	75		ns

NOTES
[1]t_{DD} is measured from when the falling edge of DAV crosses 0.8 V to when the output crosses 0.4 V or 2.4 V with a 25 pF load capacitor on each output pin.
[2]t_{SS} is measured from when the outputs cross 0.4 V or 2.4 V to when the rising edge of DAV crosses 2.4 V with a 25 pF load capacitor on each output pin.
Specifications subject to change without notice.

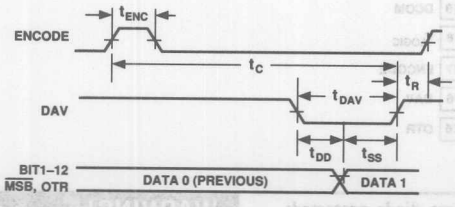


Figure 1a. Encode Pulse HIGH

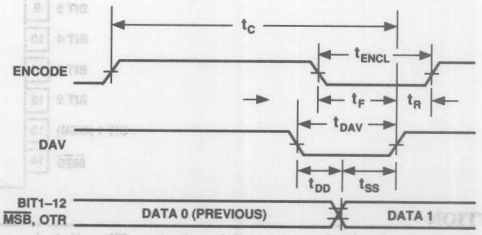


Figure 1b. Encode Pulse LOW

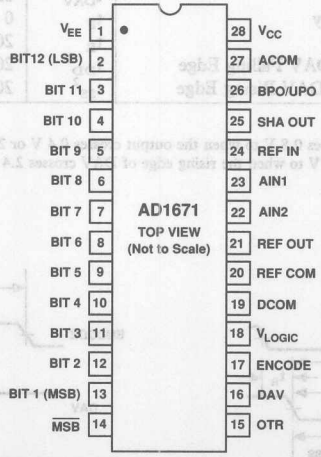
PRELIMINARY TECHNICAL DATA

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Symbol	Pin No.	Type	Name and Function
ACOM	27	P	Analog Ground.
AIN	22, 23	AI	Analog Inputs, AIN1 and AIN2. The AD1671 can be pin strapped for four input ranges: Range — Pin Strap — Signal Input 0 to +2.5 V, ±2.5 V — Connect AIN1 to AIN2 — AIN1 or AIN2 0 to +5 V, ±5 V — Connect AIN1 or AIN2 to ACOM — AIN1 or AIN2
BIT 1 (MSB)	13	DO	Most Significant Bit.
BIT 2–BIT 11	12–3	DO	Data Bits 2 through 11.
BIT 12 (LSB)	2	DO	Least Significant Bit.
BPO/UPO	26	AI	Bipolar or Unipolar Configuration Pin. See section on Input Range Connections for details.
DAV	16	DO	Data Available Output. The rising edge of DAV indicates an end of conversion and can be used to latch current data into an external register. The falling edge of DAV can be used to latch previous data into an external register.
DCOM	19	P	Digital Ground.
ENCODE	17	DI	The analog input is sampled on the rising edge of ENCODE.
$\overline{MSB}$	14	DO	Inverted Most Significant Bit. Provides twos complement output data format.
OTR	15	DO	Out of Range is Active HIGH when the analog input is out of range. See Output Data Format, Table III.
REF COM	20	AI	REF COM is the internal reference ground pin. REF COM should be connected as indicated in the Grounding and Decoupling Rules and Optional External Reference Connection Sections.
REF IN	24	AI	REF IN is the external 2.5 V reference input.
REF OUT	21	AO	REF OUT is the internal 2.5 V reference output.
SHA OUT	25	AO	No Connect for bipolar input ranges. Connect SHA OUT to BPO/UPO for unipolar input ranges.
V_{CC}	28	P	+5 V Analog Power.
V_{EE}	1	P	−5 V Analog Power.
V_{LOGIC}	18	P	+5 V Digital Power.

TYPE: AI = Analog Input; AO = Analog Output; DI = Digital Input; DO = Digital Output; P = Power.

PRELIMINARY TECHNICAL DATA



CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



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ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
V_{CC}	ACOM	−0.5	+6.5	Volts
V_{EE}	ACOM	−6.5	+0.5	Volts
V_{LOGIC}	DCOM	−6.5	+0.5	Volts
ACOM	DCOM	−1.0	+1.0	Volts
V_{CC}	V_{LOGIC}	−6.5	+6.5	Volts
ENCODE	DCOM	−0.5	V_{LOGIC}+0.5	Volts
REF IN	ACOM			
AIN	ACOM			
BPO/UPO	ACOM			
Junction Temperature			+150	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

ORDERING GUIDE

Model[1]	Linearity	Temperature Range	Package Option[2]
AD1671JN	±2 LSB	0°C to +70°C	N-28
AD1671KN	±1 LSB	0°C to +70°C	N-28
AD1671AQ	±2 LSB	−40°C to +85°C	Q-28
AD1671SQ	±2 LSB	−55°C to +125°C	Q-28

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to Analog Devices' Military Products Databook or current AD1671/883 data sheet.
[2]N = Plastic DIP; Q = Cerdip. For outline information see Package Information section.

PRELIMINARY TECHNICAL DATA

DEFINITIONS OF SPECIFICATIONS

INTEGRAL NONLINEARITY (INL)
Integral nonlinearity refers to the deviation of each individual code from a line drawn from "zero" through "full scale." The point used as "zero" occurs 1/2 LSB (1.22 mV for a 10 V span) before the first code transition (all zeros to only the LSB on). "Full-scale" is defined as a level 1 1/2 LSB beyond the last code transition (to all ones). The deviation is measured from the low side transition of each particular code to the true straight line.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from the ideal value. Thus every code has a finite width. Guaranteed no missing codes to 11 or 12-bit resolution indicates that all 2048 and 4096 codes, respectively, must be present over all operating ranges. No missing codes to 11 bits (in the case of a 12-bit resolution ADC) also means that no two consecutive codes are missing.

UNIPOLAR OFFSET
The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual from that point. This offset can be adjusted as discussed later. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustments.

BIPOLAR ZERO
In the bipolar mode the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

GAIN ERROR
The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1 1/2 LSB below the nominal full scale (4.9963 volts for 5.000 volts full scale). The gain error is the deviation of the actual level at the last transition from the ideal level. The gain error can be adjusted to zero as shown in Figures 4 through 7.

TEMPERATURE COEFFICIENTS
The temperature coefficients for unipolar offset, bipolar zero and gain error specify the maximum change from the initial (+25°C) value to the value at T_{MIN} or T_{MAX}.

POWER SUPPLY REJECTION
One of the effects of power supply error on the performance of the device will be a small change in gain. The specifications show the maximum full-scale change from the initial value with the supplies at the various limits.

DYNAMIC SPECIFICATIONS

SIGNAL-TO-NOISE PLUS DISTORTION (S/N+D) RATIO
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

EFFECTIVE NUMBER OF BITS (ENOB)
ENOB is calculated from the expression SNR = 6 .02N + 1.76 dB, where N is equal to the effective number of bits.

TOTAL HARMONIC DISTORTION (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products of order (m+n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb), and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (2fb − fa). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals are of equal amplitude and the peak value of their sum is −0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

PEAK SPURIOUS OR PEAK HARMONIC COMPONENT
The peak spurious or peak harmonic component is the largest spectral component, excluding the input signal and dc. This value is expressed in decibels relative to the rms value of a full-scale input signal.

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APERTURE DELAY

Aperture delay is the difference between the switch delay and the analog delay of the SHA. This delay represents the point in time, relative to the rising edge of ENCODE input, that the analog input is sampled.

APERTURE JITTER

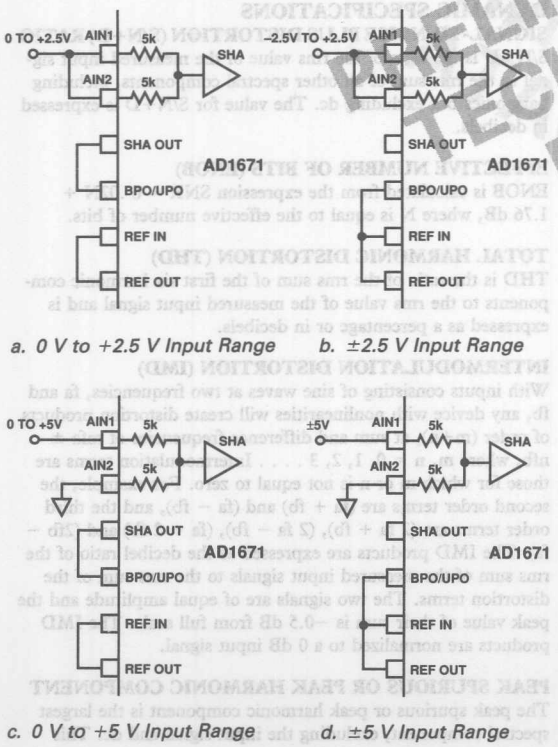
Aperture jitter is the variation in aperture delay for successive samples.

THEORY OF OPERATION

The AD1671 uses a successive subranging architecture. The analog-to-digital conversion takes place in four independent steps or flashes. The sampled analog input signal is subranged to an intermediate residue voltage for the final 12-bit result by utilizing multiple flashes with subtraction DACs (see the AD1671 functional block diagram).

The AD1671 can be configured to operate with unipolar (0 V to +5 V, 0 V to +2.5 V) or bipolar (±5 V, ±2.5 V) inputs by connecting AIN (Pins 22, 23), SHA OUT (Pin 25) and BPO/UPO (Pin 26) as shown in Figure 2.

The AD1671 conversion cycle begins by simply providing an active HIGH level on the ENCODE pin (Pin 17). The rising edge of the ENCODE pulse starts the conversion. The falling edge of the ENCODE pulse is specified to operate within a window of time, less than 50 ns after the rising edge of ENCODE or after the falling edge of DAV. The time window prevents digitally coupled noise from being introduced during the final stages of conversion. An internal timing generator circuit accurately controls SHA, flash and DAC timing.



a. 0 V to +2.5 V Input Range b. ±2.5 V Input Range

c. 0 V to +5 V Input Range d. ±5 V Input Range

Figure 2. AD1671 Input Range Connections

Upon receipt of an ENCODE command the input voltage is held by the front-end SHA and the first 3-bit flash converts the analog input voltage. The 3-bit result is passed to a correction logic register and a segmented current output DAC. The DAC output is connected through a resistor (within the Range/Span Select Block) to SHA OUT. A residue voltage is created by subtracting the DAC output from SHA OUT, which is less than one eighth of the full-scale analog input. The second flash has an input range that is configured with one bit of overlap with the previous DAC. The overlap allows for errors during the flash conversion. The first residue voltage is connected to the second 3-bit flash and to the noninverting input of a high speed, differential, gain of eight amplifier. The second flash result is passed to the correction logic register and to the second segmented current output DAC. The output of the second DAC is connected to the inverting input of the differential amplifier. The differential amplifier output is connected to a two-step, backend, 8-bit flash. This 8-bit flash consists of coarse and fine flash converters. The result of the coarse 4-bit flash converter, also configured to overlap one bit of DAC 2, is connected to the correction logic register and selects one of 16 resistors from which the fine 4-bit flash will establish its span voltage. The fine 4-bit flash is connected directly to the output latches.

The internal timing generator automatically places the SHA into the acquire mode when DAV goes LOW. Upon completion of conversion (when DAV is set HIGH), the SHA has acquired the analog input to the specified level of accuracy and will remain in the sample mode until the next ENCODE command.

The AD1671 will flag an out-of-range condition when the input voltage exceeds the analog input range. OTR (Pin 15) is active HIGH when an out-of-range high or low condition exists. Bits 1–12 are HIGH when the analog input voltage is greater than the selected input range and LOW when the analog input is less than the selected input range.

APPLYING THE AD1671

GROUNDING AND DECOUPLING RULES

Proper grounding and decoupling should be a primary design objective in any high speed, high resolution system. The AD1671 separates analog and digital grounds to optimize the management of analog and digital ground currents in a system. The AD1671 is designed to minimize the current flowing from REF COM (Pin 20) by directing the majority of the current from V_{CC} (+5 V–Pin 28) to V_{EE} (−5 V–Pin 1). Minimizing analog ground currents hence reduces the potential for large ground voltage drops. This can be especially true in systems that do not utilize ground planes or wide ground runs. REF COM is also configured to be code independent, therefore reducing input dependent analog ground voltage drops and errors. Code dependent ground current is diverted to ACOM (Pin 27). Also critical in any high speed digital design is the use of proper digital grounding techniques to avoid potential CMOS "ground bounce." Figure 3 is provided to assist in the proper layout, grounding and decoupling techniques.

PRELIMINARY TECHNICAL DATA

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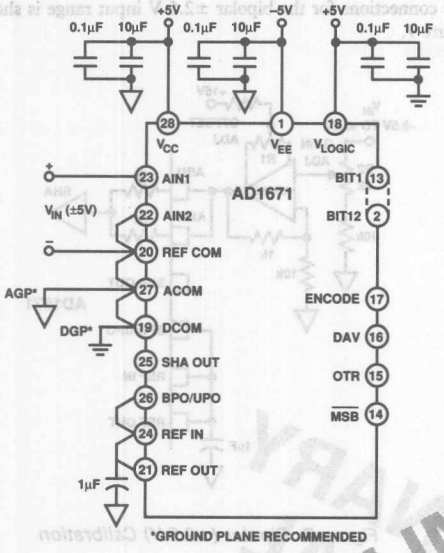


Figure 3. AD1671 Grounding and Decoupling

Table I is a list of grounding and decoupling rules that should be reviewed before laying out a printed circuit board.

Table I. Grounding and Decoupling Guidelines

Power Supply Decoupling	**Comment**
Capacitor Values	0.1 µF (Ceramic) and 1 µF (Tantalum) Surface Mount Chip Capacitors Recommended to Reduce Lead Inductance
Capacitor Locations	Directly at Positive and Negative Supply Pins to Common Ground Plane
Reference (REF OUT)	
Capacitor Value	1 µF (Tantalum) to ACOM
Grounding	
Analog Ground	Ground Plane or Wide Ground Return Connected to the Analog Power Supply
Reference Ground (REF COM)	Critical Common Connections Should be Star Connected to REF COM (as Shown in Figure 3)
Digital Ground	Ground Plane or Wide Ground Return Connected to the Digital Power Supply
Analog and Digital Ground	Connected Together Once at the AD1671

PRELIMINARY TECHNICAL DATA

UNIPOLAR (0 V TO +5 V) CALIBRATION

The AD1671 is factory trimmed to minimize offset, gain and linearity errors. In some applications the offset and gain errors of the AD1671 need to be externally adjusted to zero. This is accomplished by trimming the voltage at AIN2 (Pin 22). The circuit in Figure 4 is recommended for calibrating offset and gain errors of the AD1671 when configured in the 0 V to +5 V input range. If the offset trim resistor R1 is used, it should be trimmed as follows, although a different offset can be set for a particular system requirement. This circuit will give approximately ±5 mV of offset trim range. Nominally the AD1671 is intended to have a 1/2 LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above it and below it). Thus, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2 LSB (0.61 mV for 5 V range).

The gain trim is done by applying a signal 1 1/2 LSBs below the nominal full scale (4.998 for a 5 V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111). This circuit will give approximately ±0.5% FS of adjustment range.

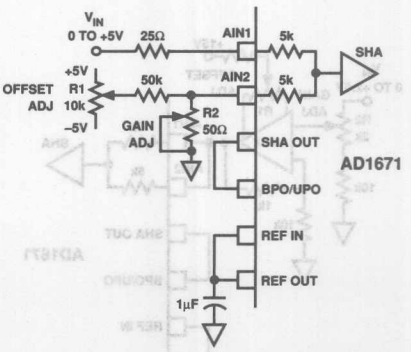


Figure 4. Unipolar (0 V to +5 V) Calibration

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BIPOLAR (±5 V) CALIBRATION

The connections for the bipolar ±5 V input range is shown in Figure 5.

Bipolar calibration is similar to unipolar calibration. First, a signal 1/2 LSB above negative full scale (−4.9988 V) is applied and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1 1/2 LSB below positive full scale (+4.9963 V) is applied and R2 is trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

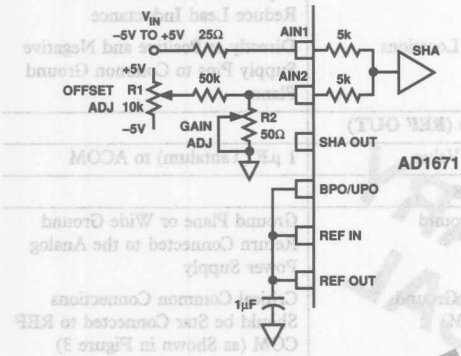


Figure 5. Bipolar (±5 V) Calibration

UNIPOLAR (0 V TO +2.5 V) CALIBRATION

The connections for the 0 V to +2.5 V input range calibration is shown in Figure 6. Figure 6 shows an example of how the offset error can be trimmed in front of the AD1671. The procedure for trimming the offset and gain errors is the same as for the unipolar 5 V range.

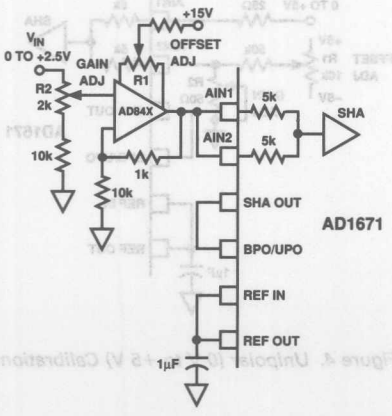


Figure 6. Unipolar (0 V to +2.5 V) Calibration

BIPOLAR (±2.5 V) CALIBRATION

The connections for the bipolar ±2.5 V input range is shown in Figure 7.

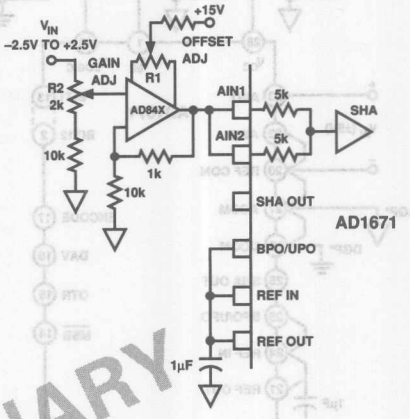


Figure 7. Bipolar (±2.5 V) Calibration

OUTPUT LATCHES

Figure 8 shows the AD1671 connected to the 74HC574 octal D-type edge-triggered latches with 3-state outputs. The latch can drive highly capacitive loads (i.e., bus lines, I/O ports) while maintaining the data signal integrity. The maximum setup and hold times of the 574 type latch must be less than 20 ns (t_{DD} and t_{SS} minimum). To satisfy the requirements of the 574 type latch the recommended logic families are S, AS, ALS, F or BCT. New data from the AD1671 is latched on the rising edge of the DAV (Pin 16) output pulse. Previous data can be latched by inverting the DAV output with a 7404 type inverter.

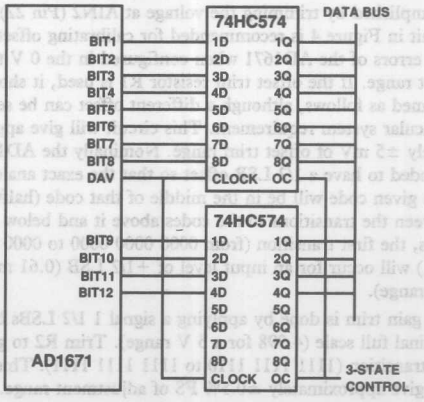


Figure 8. AD1671 to Output Latches

PRELIMINARY TECHNICAL DATA

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OUT OF RANGE

An out-of-range condition exists when the analog input voltage is beyond the input range (0 V to +2.5 V, 0 V to +5 V, ±2.5 V, ±5 V) of the converter. OTR (Pin 15) is set low when the analog input voltage is within the analog input range. OTR is set HIGH and will remain HIGH when the analog input voltage exceeds the input range by typically 1/2 LSB (OTR transition is tested to ±6 LSBs of accuracy) from the center of the ±full-scale output codes. OTR will remain HIGH until the analog input is within the input range and another conversion is completed. By logical ANDing OTR with the MSB and its complement, overrange high or underrange low conditions can be detected. Table II is a truth table for the over/under range circuit in Figure 9. Systems requiring programmable gain conditioning prior to the AD1671 can immediately detect an out-of-range condition, thus eliminating gain selection iterations.

Table II. Out-of-Range Truth Table

OTR	MSB	Analog Input Is
0	0	In Range
0	1	In Range
1	0	Underrange
1	1	Overrange

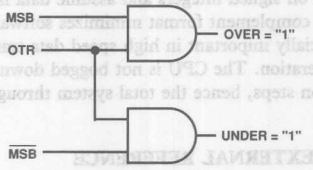


Figure 9. Overrange or Underrange Logic

Table III. Output Data Format

Input Range	Coding	Analog Input[1]	Digital Output	OTR[2]
0 V to +2.5 V	Straight Binary	≤ −0.0003 V	0000 0000 0000	1
		0 V	0000 0000 0000	0
		+2.5 V	1111 1111 1111	0
		≥ +2.5003 V	1111 1111 1111	1
0 V to +5 V	Straight Binary	≤ −0.0006 V	0000 0000 0000	1
		0 V	0000 0000 0000	0
		+5 V	1111 1111 1111	0
		≥ +5.0006 V	1111 1111 1111	1
−2.5 V to +2.5 V	Offset Binary	≤ −2.5006 V	0000 0000 0000	1
		−2.5 V	0000 0000 0000	0
		+2.5 V	1111 1111 1111	0
		≥ +2.4994 V	1111 1111 1111	1
−5 V to +5 V	Offset Binary	≤ −5.0012 V	0000 0000 0000	1
		−5 V	0000 0000 0000	0
		+5 V	1111 1111 1111	0
		≥ +4.9988 V	1111 1111 1111	1
−2.5 V to +2.5 V	2s Complement (Using $\overline{\text{MSB}}$)	≤ −2.5006 V	1000 0000 0000	1
		−2.5 V	1000 0000 0000	0
		+2.5 V	0111 1111 1111	0
		≥ +2.4994 V	0111 1111 1111	1
−5 V to +5 V	2s Complement	≤ −5.0012 V	1000 0000 0000	1
		−5 V	1000 0000 0000	0
		+5 V	0111 1111 1111	0
		≥ +4.9988 V	0111 1111 1111	1

NOTES
[1]Voltages listed are with offset and gain errors adjusted to zero.
[2]Typical performance.

PRELIMINARY TECHNICAL DATA

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The AD1671 provides both MSB and $\overline{MSB}$ outputs, delivering data in positive true straight binary for unipolar input ranges and positive true offset binary or twos complement for bipolar input ranges. Straight binary coding is used for systems that accept positive-only signals. If straight binary coding is used with bipolar input signals, a 0 V input would result in a binary output of 2048. The application software would have to subtract 2048 to determine the true input voltage. Host registers typically perform math on signed integers and assume data is in that format. Twos complement format minimizes software overhead which is especially important in high speed data transfers, such as a DMA operation. The CPU is not bogged down performing data conversion steps, hence the total system throughput is increased.

OPTIONAL EXTERNAL REFERENCE

The AD1671 includes an on-board +2.5 V reference. The reference input pin (REF IN) can be connected to reference output pin (REF OUT) or a standard external +2.5 V reference can be selected to meet specific system requirements. Fast switching input dependent currents are modulated at the reference input. The reference input voltage can be held with the use of a capacitor. To prevent the AD1671's on-board reference from oscillating when not connected to REF IN, REF OUT must be connected to analog ground. Connecting REF OUT to analog ground, due to its output circuit implementation shuts down the reference output.

Figure 10 is the typical logic supply current vs. conversion rate for various capacitor loads.

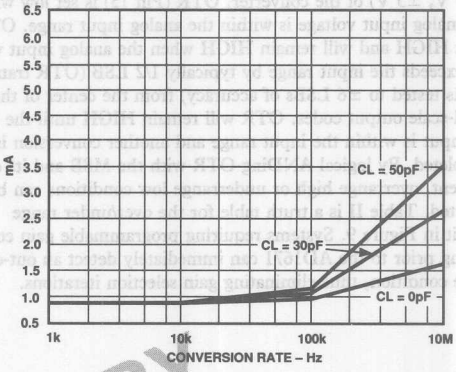


Figure 10. I_{LOGIC} vs. Conversion Rate for Various Capacitive Loads on the Digital Outputs

PRELIMINARY TECHNICAL DATA

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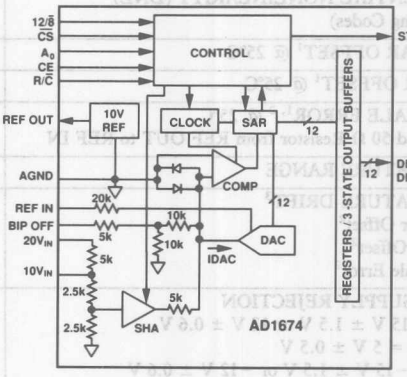
12-Bit 100 kSPS A/D Converter

AD1674*

FEATURES

- Complete Monolithic 12-Bit 10 μs Sampling ADC
- On-Board Sample-and-Hold Amplifier
- Industry Standard Pinout
- 8- and 16-Bit Microprocessor Interface
- AC and DC Specified and Tested
- Unipolar and Bipolar Inputs
- ±5 V, ±10 V, 0–10 V, 0–20 V Input Ranges
- Commercial, Industrial and Military Temperature Range Grades
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1674 is a complete, multipurpose, 12-bit analog-to-digital converter, consisting of a user-transparent on-board sample-and-hold amplifier (SHA), 10 volt reference, clock and three-state output buffers for microprocessor interface.

The AD1674 is pin compatible with the industry standard AD574A and AD674A, but includes a sampling function while delivering a faster conversion rate. The on-chip SHA has a wide input bandwidth supporting 12-bit accuracy over the full Nyquist bandwidth of the converter.

The AD1674 is fully specified for ac parameters (such as S/(N+D) ratio, THD, and IMD) and dc parameters (offset, full-scale error, etc.). With both ac and dc specifications, the AD1674 is ideal for use in signal processing and traditional dc measurement applications.

The AD1674 design is implemented using Analog Devices' BiMOS II process allowing high performance bipolar analog circuitry to be combined on the same die with digital CMOS logic.

Five different grades are available. The AD1674J and K grades are specified for operation over the 0°C to +70°C temperature range. The A and B grades are specified from −40°C to +85°C; the AD1674T grade is specified from −55°C to +125°C. The J and K grades are available in a 28-pin plastic DIP or 28-lead SOIC. All other grades are available in a 28-pin hermetically sealed ceramic DIP.

PRODUCT HIGHLIGHTS

1. Industry Standard Pinout: The AD1674 utilizes the pinout established by the industry standard AD574A and AD674A. In stand-alone mode, the AD1674 has identical interface requirements as the AD574A and AD674A. In full control mode, the AD1674 requires slight control timing modification.
2. Integrated SHA: The AD1674 has an integrated SHA which supports the full Nyquist bandwidth of the converter. The SHA function is transparent to the user; no wait-states are needed for SHA acquisition.
3. DC and AC Specified: In addition to traditional dc specifications, the AD1674 is also fully specified for frequency domain ac parameters such as total harmonic distortion, signal-to-noise ratio and input bandwidth. These parameters can be tested and guaranteed as a result of the on-board SHA.
4. Analog Operation: The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges: 0 to +10 V and 0 to +20 V unipolar, −5 V to +5 V and −10 V to +10 V bipolar. The AD1674 operates on +5 V and ±12 V or ±15 V power supplies.
5. Flexible Digital Interface: On-chip multiple-mode three-state output buffers and interface logic allow direct connection to most microprocessors.

*Protected by U. S. Patent Nos. 4,962,325; 4,250,445; 4,808,908; RE30586.

AD1674—SPECIFICATIONS

DC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −15 V ± 10% or −12 V ± 5% unless otherwise indicated)

Parameter	AD1674J Min	AD1674J Typ	AD1674J Max	AD1674K Min	AD1674K Typ	AD1674K Max	Units
RESOLUTION	12			12			Bits
INTEGRAL NONLINEARITY (INL)			±1			±1/2	LSB
DIFFERENTIAL NONLINEARITY (DNL) (No Missing Codes)	12			12			Bits
UNIPOLAR OFFSET[1] @ 25°C			±3			±2	LSB
BIPOLAR OFFSET[1] @ 25°C			±6			±4	LSB
FULL-SCALE ERROR[1, 2] @ 25°C (with Fixed 50 Ω Resistor from REF OUT to REF IN		0.1	0.25		0.1	0.25	% of FSR
TEMPERATURE RANGE	0		+70	0		+70	°C
TEMPERATURE DRIFT[3]							
Unipolar Offset[2]			±2			±1	LSB
Bipolar Offset[2]			±2			±1	LSB
Full-Scale Error[2]			±6			±3	LSB
POWER SUPPLY REJECTION							
V_{CC} = 15 V ± 1.5 V or 12 V ± 0.6 V			±2			±1	LSB
V_{LOGIC} = 5 V ± 0.5 V			±1/2			±1/2	LSB
V_{EE} = −15 V ± 1.5 V or −12 V ± 0.6 V			±2			±1	LSB
ANALOG INPUT							
Input Ranges							
Bipolar	−5		+5	−5		+5	Volts
	−10		+10	−10		+10	Volts
Unipolar	0		+10	0		+10	Volts
	0		+20	0		+20	Volts
Input Impedance							
10 Volt Span	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	kΩ
POWER SUPPLIES							
Operating Voltages							
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−16.5		−11.4	−16.5		−11.4	Volts
Operating Current							
I_{LOGIC}		5	8		5	8	mA
I_{CC}		10	14		10	14	mA
I_{EE}		14	18		14	18	mA
POWER DISSIPATION		385	575		385	575	mW
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1	Volts
Output Current (Available for External Loads) (External Load Should Not Change During Conversion)			2.0			2.0	mA

NOTES
[1]Adjustable to zero.
[2]Includes internal voltage reference error.
[3]Maximum change from 25°C value to the value at T_{min} or T_{max}.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at T_{min}, 25°C, and T_{max}. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

Parameter	AD1674A Min	AD1674A Typ	AD1674A Max	AD1674B Min	AD1674B Typ	AD1674B Max	AD1674T Min	AD1674T Typ	AD1674T Max	Units
RESOLUTION	12			12			12			Bits
INTEGRAL NONLINEARITY (INL) @ 25°C			±1			±1/2			±1/2	LSB
T_{min} to T_{max}			±1			±1/2			±1	LSB
DIFFERENTIAL NONLINEARITY (DNL) (no missing codes)	12			12			12			Bits
UNIPOLAR OFFSET[1] @ 25°C			±2			±2			±2	LSB
BIPOLAR OFFSET[1] @ 25°C			±6			±3			±3	LSB
FULL-SCALE ERROR[1, 2] @ 25°C (with Fixed 50 Ω Resistor from REF OUT to REF IN)		0.1	0.25		0.1	0.125		0.1	0.125	% of FSR
TEMPERATURE RANGE	−40		+85	−40		+85	−55		+125	°C
TEMPERATURE DRIFT[3]										
Unipolar Offset[2]			±2			±1			±1	LSB
Bipolar Offset[2]			±2			±1			±2	LSB
Full-Scale Error[2]			±8			±5			±7	LSB
POWER SUPPLY REJECTION										
V_{CC} = 15 V ± 1.5 V or 12 V ± 0.6 V			±2			±1			±1	LSB
V_{LOGIC} = 5 V ± 0.5 V			±1/2			±1/2			±1/2	LSB
V_{EE} = −15 V ± 1.5 V or −12 V ± 0.6 V			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar	−5		+5	−5		+5	−5		+5	Volts
	−10		+10	−10		+10	−10		+10	Volts
Unipolar	0		+10	0		+10	0		+10	Volts
	0		+20	0		+20	0		+20	Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
POWER SUPPLIES										
Operating Voltages										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−16.5		−11.4	−16.5		−11.4	−16.5		−11.4	Volts
Operating Current										
I_{LOGIC}		5	8		5	8		5	8	mA
I_{CC}		10	14		10	14		10	14	mA
I_{EE}		14	18		14	18		14	18	mA
POWER DISSIPATION		385	575		385	575		385	575	mW
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1	9.9	10.0	10.1	Volts
Output Current (Available for External Loads) (External Load Should Not Change During Conversion)			2.0			2.0			2.0	mA

AD1674—AC SPECIFICATIONS

(T_{min} to T_{max}, with V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −15 V ± 10% or −12 V ± 5%, f_{SAMPLE} = 100 kSPS, f_{IN} = 10 kHz, stand-alone mode unless otherwise noted)[1]

Parameter	AD1674J/A Min	AD1674J/A Typ	AD1674J/A Max	AD1674K/B/T Min	AD1674K/B/T Typ	AD1674K/B/T Max	Units
Signal to Noise and Distortion (S/N+D) Ratio[2, 3]	**69**	70		**70**	71		dB
Total Harmonic Distortion (THD)[4]		−90	**−82**		−90	**−82**	dB
			0.008			0.008	%
Peak Spurious or Peak Harmonic Component		−92	**−82**		−92	**−82**	dB
Full Power Bandwidth		1			1		MHz
Full Linear Bandwidth		500			500		kHz
Intermodulation Distortion (IMD)[5]							
Second Order Products		−90	**−80**		−90	**−80**	dB
Third Order Products		−90	**−80**		−90	**−80**	dB
SHA (specifications are included in overall timing specifications)							
Aperture Delay		15			15		ns
Aperture Jitter		150			150		ps
Acquisition Time		1			1		µs

DIGITAL SPECIFICATIONS

(for all grades T_{min} to T_{max}, with V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −15 V ± 10% or −12 V ± 5%)

Parameter		Test Conditions	Min	Max	Units
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		+2.0	V_{LOGIC} +0.5 V	V
V_{IL}	Low Level Input Voltage		−0.5	**+0.8**	V
I_{IH}	High Level Input Current (V_{IN} = 5 V)	V_{IN} = V_{LOGIC}	**−10**	**+10**	µA
I_{IL}	Low Level Input Current (V_{IN} = 0 V)	V_{IN} = 0 V	**−10**	**+10**	µA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.5 mA	**+2.4**		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		**+0.4**	V
I_{OZ}	High-Z Leakage Current	V_{IN} = 0 to V_{LOGIC}	**−10**	**+10**	µA
C_{OZ}	High-Z Output Capacitance			10	pF

NOTES

[1]f_{IN} amplitude = −0.5 dB (9.44 V p-p) 10 V bipolar mode unless otherwise indicated. All measurements referred to −0 dB (9.997 V p-p) input signal unless otherwise indicated.

[2]Specified at worst case temperatures and supplies after one minute warm-up.

[3]See Figures 12 and 13 for other input frequencies and amplitudes.

[4]See Figure 11.

[5]fa = 9.08 kHz, fb = 9.58 kHz with f_{SAMPLE} = 100 kHz. See *Definition of Specifications* section and Figure 15.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at T_{min}, 25°C, and T_{max}. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS

(for all grades T_{min} to T_{max} with V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = −15 V ± 10% or −12 V ± 5%; V_{IL} = 0.4 V, V_{IH} = 2.4 V unless otherwise noted)

CONVERTER START TIMING (Figure 1)

Parameter	Symbol	Min	Typ	Max	Units
Conversion Time					
8-Bit Cycle	t_C		7	8	µs
12-Bit Cycle	t_C		9	10	µs
STS Delay from CE @ 25°C	t_{DSC}			200	ns
T_{min} to T_{max}				250	ns
CE Pulse Width @ 25°C	t_{HEC}	50			ns
T_{min} to T_{max}		75			ns
$\overline{CS}$ to CE Setup	t_{SSC}	50			ns
$\overline{CS}$ Low During CE High @ 25°C	t_{HSC}	50			ns
T_{min} to T_{max}		75			ns
R/$\overline{C}$ to CE Setup	t_{SRC}	50			ns
R/$\overline{C}$ Low During CE High @ 25°C	t_{HRC}	50			ns
T_{min} to T_{max}		150			ns
A_0 to CE Setup	t_{SAC}	0			ns
A_0 Valid During CE High	t_{HAC}	50			ns

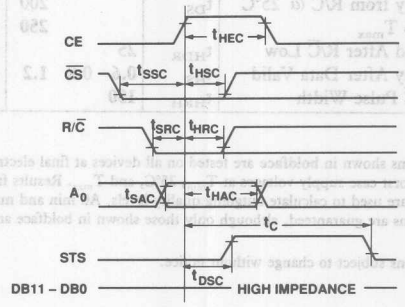


Figure 1. Converter Start Timing

READ TIMING – FULL CONTROL MODE (Figure 2)

Parameter	Symbol	Min	Typ	Max	Units
Access Time					
C_L = 100 pF	t_{DD}[1]		75	150	ns
Data Valid After CE Low	t_{HD}	25			ns
Output Float Delay	t_{HL}[2]			150	ns
$\overline{CS}$ to CE Setup	t_{SSR}	50			ns
R/$\overline{C}$ to CE Setup	t_{SRR}	0			ns
A_0 to CE Setup	t_{SAR}	50			ns
$\overline{CS}$ Valid After CE Low	t_{HSR}	0			ns
R/$\overline{C}$ High After CE Low	t_{HRR}	60			ns
A_0 Valid After CE Low	t_{HAR}	50			ns

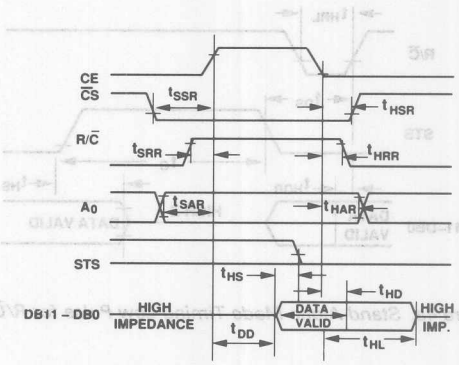


Figure 2. Read Timing

NOTES

[1] t_{DD} is measured with the load circuit of Figure 3 and is defined as the time required for an output to cross 0.4 V or 2.4 V.

[2] t_{HL} is defined as the time required for the data lines to change 0.5 V when loaded with the circuit of Figure 3.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at T_{min}, 25°C, and T_{max}. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

Test	V_{CP}	C_{OUT}
Access Time High Z to Logic Low	5 V	100 pF
Float Time Logic High to High Z	0 V	10 pF
Access Time High Z to Logic High	0 V	100 pF
Float Time Logic Low to High Z	5 V	10 pF

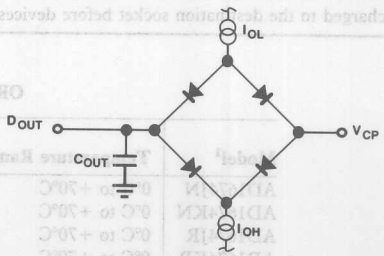


Figure 3. Load Circuit for Bus Timing Specifications

TIMING – STAND-ALONE MODE (Figures 4a and 4b)

Parameter	Symbol	Min	Typ	Max	Units
Data Access Time	t_{DDR}			150	ns
Low R/$\overline{C}$ Pulse Width	t_{HRL}	50			ns
STS Delay from R/$\overline{C}$ @ 25°C	t_{DS}			200	ns
T_{min} to T_{max}				250	ns
Data Valid After R/$\overline{C}$ Low	t_{HDR}	25			ns
STS Delay After Data Valid	t_{HS}	0.6	0.8	1.2	µs
High R/$\overline{C}$ Pulse Width	t_{HRH}	150			ns

NOTE
Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at T_{min}, 25°C, and T_{max}. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

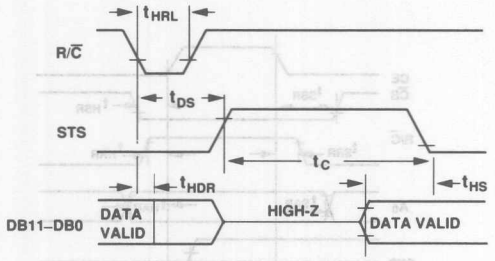


Figure 4a. Stand-Alone Mode Timing Low Pulse for R/$\overline{C}$

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Digital Common . . . . . 0 to +16.5 V
V_{EE} to Digital Common . . . . . 0 to −16.5 V
V_{LOGIC} to Digital Common . . . . . 0 to +7 V
Analog Common to Digital Common . . . . . ±1 V
Digital Inputs to Digital Common . −0.5 V to V_{LOGIC} +0.5 V
Analog Inputs to Analog Common . . . . . V_{EE} to V_{CC}
20 V_{IN} to Analog Common . . . . . ±24 V
REF OUT . . . . . Indefinite Short to Common
. . . . . Momentary Short to V_{CC}
Junction Temperature . . . . . +175°C
Power Dissipation . . . . . 825 mW
Lead Temperature, Soldering . . . . . 300°C, 10 sec
Storage Temperature . . . . . −65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

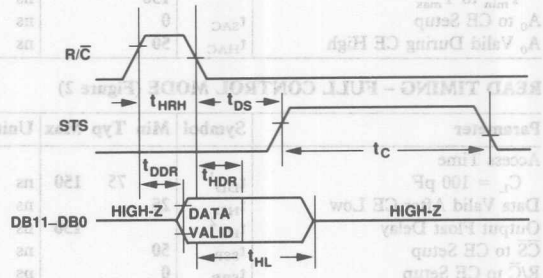


Figure 4b. Stand-Alone Mode Timing High Pulse for R/$\overline{C}$

CAUTION:
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



ORDERING GUIDE

Model[1]	Temperature Range	INL (T_{min} to T_{max})	S/(N+D) (T_{min} to T_{max})	Package Option[2]
AD1674JN	0°C to +70°C	±1 LSB	69 dB	N-28A
AD1674KN	0°C to +70°C	±1/2 LSB	70 dB	N-28A
AD1674JR	0°C to +70°C	±1 LSB	69 dB	R-28
AD1674KR	0°C to +70°C	±1/2 LSB	70 dB	R-28
AD1674AD	−40°C to +85°C	±1 LSB	69 dB	D-28A
AD1674BD	−40°C to +85°C	±1/2 LSB	70 dB	D-28A
AD1674TD	−55°C to +125°C	±1 LSB	70 dB	D-28A

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD1674/883B data sheet.
[2]N = Plastic DIP; D = Hermetic Ceramic DIP; R = plastic SOIC. For outline information see Package Information section.

DEFINITION OF SPECIFICATIONS

INTEGRAL NONLINEARITY (INL)

The ideal transfer function for an ADC is a straight line drawn between "zero" and "full scale." The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition. Integral nonlinearity is the worst-case deviation of a code from the straight line. The deviation of each code is measured from the middle of that code.

DIFFERENTIAL NONLINEARITY (DNL)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. The AD1674 guarantees no missing codes to 12-bit resolution; all 4096 codes are present over the entire operating range.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point at 25°C. This offset can be adjusted as shown in Figure 6.

BIPOLAR OFFSET

In the bipolar mode the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error specifies the deviation of the actual transition from that point at 25°C. This offset can be adjusted as shown in Figure 7.

FULL-SCALE ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1 1/2 LSB below the nominal full scale (9.9963 volts for 10 volts full scale). The full-scale error is the deviation of the actual level of the last transition from the ideal level at 25°C. The full-scale error can be adjusted to zero as shown in Figures 6 and 7.

TEMPERATURE DRIFT

The temperature drifts for full-scale error, unipolar offset and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

POWER SUPPLY REJECTION

The effect of power supply error on the performance of the device will be a small change in full scale. The specifications show the maximum full-scale change from the initial value with the supplies at various limits.

FREQUENCY-DOMAIN TESTING

The AD1674 is tested dynamically using a sine wave input and a 2048 point Fast Fourier Transform (FFT) to analyze the resulting output. Coherent sampling is used, wherein the ADC sampling frequency and the analog input frequency are related to each other by a ratio of integers. This ensures that an integral multiple of input cycles is captured, allowing direct FFT processing without windowing or digital filtering which could mask some of the dynamic characteristics of the device. In addition, the frequencies are chosen to be "relatively prime" (no common factors) to maximize the number of different ADC codes that are present in a sample sequence. The result, called Prime Coherent Sampling, is a highly accurate and repeatable measure of the actual frequency-domain response of the converter.

NYQUIST FREQUENCY

An implication of the Nyquist sampling theorem, the "Nyquist Frequency" of a converter is that input frequency which is one-half the sampling frequency of the converter.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO

S/(N+D) is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in decibels.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of a full-scale input signal and is expressed as a percentage or in decibels. For input signals or harmonics that are above the Nyquist frequency, the aliased component is used.

INTERMODULATION DISTORTION (IMD)

With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mfa ± nfb, where m,n = 0,1,2,3... Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb) and the third order terms are (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals are of equal amplitude and the peak value of their sums is −0.5 dB from full-scale. The IMD products are normalized to a 0 dB input signal.

FULL-POWER BANDWIDTH

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

FULL-LINEAR BANDWIDTH

The full-linear bandwidth is the input frequency at which the slew rate limit of the sample-hold-amplifier (SHA) is reached. At this point, the amplitude of the reconstructed fundamental has degraded by less than −0.1 dB. Beyond this frequency, distortion of the sampled input signal increases significantly.

APERTURE DELAY

Aperture delay is a measure of the SHA's performance and is measured from the falling edge of Read/Convert (R/$\overline{C}$) to when the input signal is held for conversion.

APERTURE JITTER

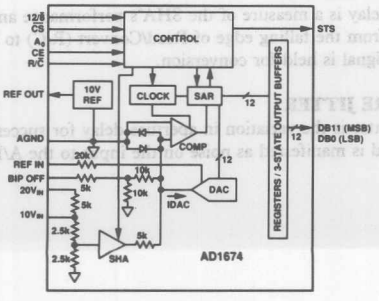
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

PIN DESCRIPTION

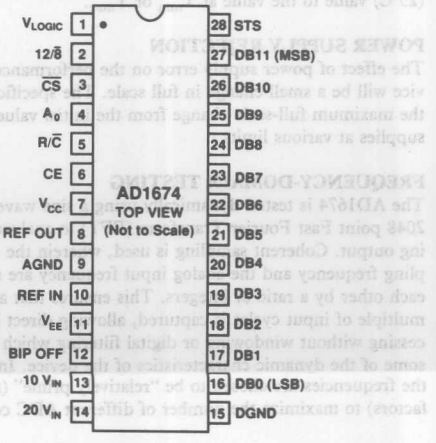
Symbol	Pin No.	Type	Name and Function
AGND	9	P	Analog Ground (Common).
A_0	4	DI	Byte Address/Short Cycle. If a conversion is started with A_0 Active LOW, a full 12-bit conversion cycle is initiated. If A_0 is Active HIGH during a convert start, a shorter 8-bit conversion cycle results. During Read ($R/\overline{C}$ = 1) with $12/\overline{8}$ LOW, A_0 = LOW enables the 8 most significant bits (DB4–DB11), and A_0 = HIGH enables DB3–DB0 and sets DB7–DB4 = 0.
BIP OFF	12	AI	Bipolar Offset. Connect through a 50 Ω resistor to REF OUT for bipolar operation or to Analog Common for unipolar operation.
CE	6	DI	Chip Enable. Chip Enable is Active HIGH and is used to initiate a convert or read operation.
$\overline{CS}$	3	DI	Chip Select. Chip Select is Active LOW.
DB11–DB8	27–24	DO	Data Bits 11 through 8. In the 12-bit format (see $12/\overline{8}$ and A_0 pins), these pins provide the upper 4 bits of data. In the 8-bit format, they provide the upper 4 bits when A_0 is LOW and are disabled when A_0 is HIGH.
DB7–DB4	23–20	DO	Data Bits 7 through 4. In the 12-bit format these pins provide the middle 4 bits of data. In the 8-bit format they provide the middle 4 bits when A_0 is LOW and all zeroes when A_0 is HIGH.
DB3–DB0	19–16	DO	Data Bits 3 through 0. In both the 12-bit and 8-bit format these pins provide the lower 4 bits of data when A_0 is HIGH; they are disabled when A_0 is LOW.
DGND	15	P	Digital Ground (Common).
REF OUT	8	AO	+10 V Reference Output.
$R/\overline{C}$	5	DI	Read/Convert. In the full control mode $R/\overline{C}$ is Active HIGH for a read operation and Active LOW for a convert operation. In the stand-alone mode, the falling edge of $R/\overline{C}$ initiates a conversion.
REF IN	10	AI	Reference Input is connected through a 50 Ω resistor to +10 V Reference for normal operation.
STS	28	DO	Status is Active HIGH when a conversion is in progress and goes LOW when the conversion is completed.
V_{CC}	7	P	+12 V/+15 V Analog Supply.
V_{EE}	11	P	−12 V/−15 V Analog Supply.
V_{LOGIC}	1	P	+5 V Logic Supply.
10 V_{IN}	13	AI	10 V Span Input, 0 to +10 V unipolar mode or −5 V to +5 V bipolar mode. When using the AD1674 in the 20 V Span 10 V_{IN} should not be connected.
20 V_{IN}	14	AI	20 V Span Input, 0 to +20 V unipolar mode or −10 V to +10 V bipolar mode. When using the AD1674 in the 10 V Span 20 V_{IN} should not be connected.
$12/\overline{8}$	2	DI	The $12/\overline{8}$ pin determines whether the digital output data is to be organized as two 8-bit words ($12/\overline{8}$ LOW) or a single 12-bit word ($12/\overline{8}$ HIGH).

TYPE: AI = Analog Input
AO = Analog Output
DI = Digital Input
DO = Digital Output
P = Power

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



GENERAL CIRCUIT OPERATION

The AD1674 is a complete 12-bit, 10 μs sampling analog-to-digital converter. A block diagram of the AD1674 is shown on the previous page.

When the control section is commanded to initiate a conversion (as described later), it places the sample-and-hold amplifier (SHA) in the hold mode, enables the clock, and resets the successive approximation register (SAR). Once a conversion cycle has begun, it cannot be stopped or restarted and data is not available from the output buffers. The SAR, timed by the clock, will sequence through the conversion cycle and return an end-of-convert flag to the control section when the conversion has been completed. The control section will then disable the clock, switch the SHA to sample mode, and delay the STS LOW going edge to allow for acquisition to 12-bit accuracy. The control section will allow data read functions by external command anytime during the SHA acquisition interval.

During the conversion cycle, the internal 12-bit, 1 mA full-scale current output DAC is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB) to provide an output that accurately balances the current through the 5 kΩ resistor from the input signal voltage held by the SHA. The SHA's input scaling resistors divide the input voltage by 2 for the 10 V input span and by 4 for the 20 V input span, maintaining a 1 mA full-scale output current through the 5 kΩ resistor for both ranges. The comparator determines whether the addition of each successively weighted bit current causes the DAC current sum to be greater than or less than the input current. If the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2 LSB.

CONTROL LOGIC

The AD1674 may be operated in one of two modes, the full-control mode and the stand-alone mode. The full-control mode utilizes all the AD1674 control signals and is useful in systems that address decode multiple devices on a single data bus. The stand-alone mode is useful in systems with dedicated input ports available and thus not requiring full bus interface capability. Table I is a truth table for the AD1674, and Figure 5 illustrates the internal logic circuitry.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-Bit Conversion
1	0	0	X	1	Initiate 8-Bit Conversion
1	0	1	1	X	Enable 12-Bit Parallel Output
1	0	1	0	0	Enable 8 Most Significant Bits
1	0	1	0	1	Enable 4 LSBs +4 Trailing Zeroes

Table I. AD1674A Truth Table

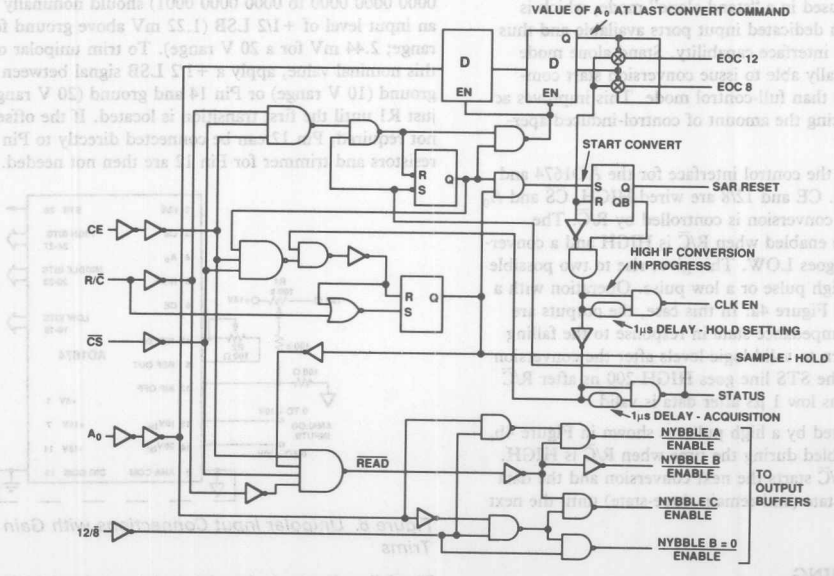


Figure 5. Equivalent Internal Logic Circuitry

FULL-CONTROL MODE

In full-control mode, the AD1674 departs slightly from the AD674A timing requirements. These differences are discussed in Table II. In full-control mode, AD1674 timing should be reviewed for compliancy with AD674A applications.

Specification	AD674A	AD1674
t_{HRC}	50 ns (min)	50 ns @ 25°C 150 ns T_{min} to T_{max}
t_{HRR}	0 ns (min)	60 ns
t_{DSC}	200 ns (max)	200 ns @ 25°C 250 ns T_{min} to T_{max}
t_{HS}	600 ns (max)	1 μs

Table II.

Chip Enable (CE), Chip Select ($\overline{CS}$) and Read/Convert (R/$\overline{C}$) are used to control Convert or Read modes of operation. Either CE or $\overline{CS}$ may be used to initiate a conversion. Note that the shortest delay path to the SHA control is from the R/$\overline{C}$ input (see Figure 5). SHA accuracy has been optimized for use in stand-alone mode and consequently results in the Table II differences for the full-control mode of operation. The state of R/$\overline{C}$ when CE and $\overline{CS}$ are both asserted determines whether a data Read (R/$\overline{C}$ = 1) or a Convert (R/$\overline{C}$ = 0) is in progress. R/$\overline{C}$ should be LOW before both CE and $\overline{CS}$ are asserted; if R/$\overline{C}$ is HIGH, a Read operation will momentarily occur, possibly resulting in system bus contention.

STAND-ALONE MODE

The AD1674 can be used in a "stand-alone" mode, which is useful in systems with dedicated input ports available and thus not requiring full bus interface capability. Stand-alone mode applications are generally able to issue conversion start commands more precisely than full-control mode. This improves ac performance by reducing the amount of control-induced aperture jitter.

In stand-alone mode, the control interface for the AD1674 and AD674A are identical. CE and 12/$\overline{8}$ are wired HIGH, $\overline{CS}$ and A_0 are wired LOW, and conversion is controlled by R/$\overline{C}$. The three-state buffers are enabled when R/$\overline{C}$ is HIGH and a conversion starts when R/$\overline{C}$ goes LOW. This gives rise to two possible control signals — a high pulse or a low pulse. Operation with a low pulse is shown in Figure 4a. In this case, the outputs are forced into the high-impedance state in response to the falling edge of R/$\overline{C}$ and return to valid logic levels after the conversion cycle is completed. The STS line goes HIGH 200 ns after R/$\overline{C}$ goes LOW and returns low 1 μs after data is valid.

If conversion is initiated by a high pulse as shown in Figure 4b, the data lines are enabled during the time when R/$\overline{C}$ is HIGH. The falling edge of R/$\overline{C}$ starts the next conversion and the data lines return to three-state (and remain three-state) until the next high pulse of R/$\overline{C}$.

CONVERSION TIMING

Once a conversion is started, the STS line goes HIGH. Convert start commands will be ignored until the conversion cycle is complete. The output data buffers can be enabled up to 1.2 μs prior to STS going LOW. The STS line will return LOW at the end of the conversion cycle.

The register control inputs, A_0 and 12/$\overline{8}$, control conversion length and data format. If a conversion is started with A_0 LOW, a full 12-bit conversion cycle is initiated. If A_0 is HIGH during a convert start, a shorter 8-bit conversion cycle results.

During data read operations, A_0 determines whether the three-state buffers containing the 8 MSBs of the conversion result (A_0 = 0) or the 4 LSBs (A_0 = 1) are enabled. The 12/$\overline{8}$ pin determines whether the output data is to be organized as two 8-bit words (12/$\overline{8}$ tied LOW) or a single 12-bit word (12/$\overline{8}$ tied HIGH). In the 8-bit mode, the byte addressed when A_0 is high contains the 4 LSBs from the conversion followed by four trailing zeroes. This organization allows the data lines to be overlapped for direct interface to 8-bit buses without the need for external three-state buffers.

INPUT CONNECTIONS AND CALIBRATION

The 10 V p–p and 20 V p–p full-scale input ranges of the AD1674 accept the majority of signal voltages without the need for external voltage divider networks which could deteriorate the accuracy of the ADC.

The AD1674 is factory trimmed to minimize offset, linearity, and full-scale errors. In many applications, no calibration trimming will be required and the AD1674 will exhibit the accuracy limits listed in the specification tables.

In some applications, offset and full-scale errors need to be trimmed out completely. The following sections describe the correct procedure for these various situations.

UNIPOLAR RANGE INPUTS

Figure 6 illustrates the external connections for the AD1674 in unipolar-input mode. The first output-code transition (from 0000 0000 0000 to 0000 0000 0001) should nominally occur for an input level of +1/2 LSB (1.22 mV above ground for a 10 V range; 2.44 mV for a 20 V range). To trim unipolar offset to this nominal value, apply a +1/2 LSB signal between Pin 13 and ground (10 V range) or Pin 14 and ground (20 V range) and adjust R1 until the first transition is located. If the offset trim is not required, Pin 12 can be connected directly to Pin 9; the two resistors and trimmer for Pin 12 are then not needed.

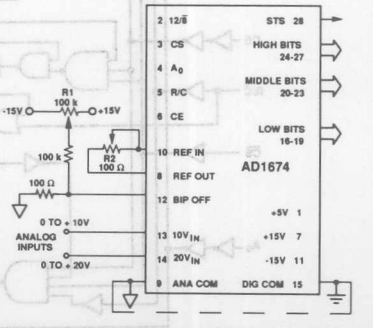


Figure 6. Unipolar Input Connections with Gain and Offset Trims

The full-scale trim is done by applying a signal 1 1/2 LSB below the nominal full scale (9.9963 V for a 10 V range) and adjusting R2 until the last transition is located (1111 1111 1110 to 1111 1111 1111). If full-scale adjustment is not required, R2 should be replaced with a fixed 50 Ω ±1% metal film resistor. If REF OUT is connected directly to REF IN, the additional full-scale error will be approximately 1%.

BIPOLAR RANGE INPUTS

The connections for the bipolar-input mode are shown in Figure 7. Either or both of the trimming potentiometers can be replaced with 50 Ω ± 1% fixed resistors if the specified AD1674 accuracy limits are sufficient for the application. If the pins are shorted together, the additional offset and gain errors will be approximately 1%.

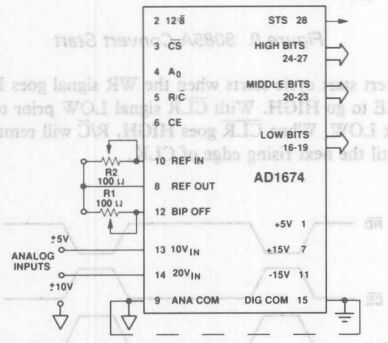


Figure 7. Bipolar Input Connections with Gain and Offset Trims

To trim bipolar offset to its nominal value, apply a signal 1/2 LSB below midrange (−1.22 mV for a ±5 V range) and adjust R1 until the major carry transition is located (0111 1111 1111 to 1000 0000 0000). To trim the full-scale error, apply a signal 1 1/2 LSB below full scale (+4.9963 V for a ±5 V range) and adjust R2 to give the last positive transition (1111 1111 1110 to 1111 1111 1111). These trims are interactive so several iterations may be necessary for convergence.

A single-pass calibration can be done by substituting a negative full-scale trim for the bipolar offset trim (error at midscale), using the same circuit. First, apply a signal 1/2 LSB above minus full scale (−4.9988 V for a ±5 V range) and adjust R1 until the minus full-scale transition is located (0000 0000 0001 to 0000 0000 0000). Then perform the gain error trim as outlined above.

REFERENCE DECOUPLING

It is recommended that a 10 μF tantalum capacitor be connected between REF IN (Pin 10) and ground. This has the effect of improving the S/(N+D) ratio through filtering possible broad-band noise contributions from the voltage reference.

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is a significant issue. At the 12-bit level, a 5 mA current through a 0.5 Ω trace will develop a voltage drop of 2.5 mV, which is 1 LSB for a 10 V full-scale range. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals. Finally, power supplies should be decoupled in order to filter out ac noise.

The AD1674 has a wide bandwidth sampling front end. This means that the AD1674 will "see" high frequency noise at the input, which nonsampling (or limited-bandwidth sampling) ADCs would ignore. Therefore, it's important to make an effort to eliminate such high frequency noise through decoupling or by using an anti-aliasing filter at the analog input of the AD1674.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them (if necessary) only at right angles.

The AD1674 incorporates several features to help the user's layout. Analog pins are adjacent to help isolate analog from digital signals. Ground currents have been minimized by careful circuit architecture. Current through AGND is 2.2 mA, with little code-dependent variation. The current through DGND is dominated by the return current for DB11–DB0.

SUPPLY DECOUPLING

The AD1674 power supplies should be well filtered, well regulated, and free from high frequency noise. Switching power supplies are not recommended due to their tendency to generate spikes which can induce noise in the analog system.

Decoupling capacitors should be used in very close layout proximity between all power supply pins and ground. A 10 μF tantalum capacitor in parallel with a 0.1 μF disc ceramic capacitor provides adequate decoupling over a wide range of frequencies.

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD1674, associated analog input circuitry, and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD1674 will isolate large switching ground currents. For these reasons, the use of wire-wrap circuit construction is not recommended; careful printed-circuit construction is preferred.

GROUNDING

If a single AD1674 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD1674. If multiple AD1674s are used or the AD1674 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at each chip. This prevents large ground loops which inductively couple noise and allow digital currents to flow through the analog system.

GENERAL MICROPROCESSOR INTERFACE CONSIDERATIONS

A typical A/D converter interface routine involves several operations. First, a write to the ADC address initiates a conversion. The processor must then wait for the conversion cycle to complete, since most ADCs take longer than one instruction cycle to complete a conversion. Valid data can, of course, only be read after the conversion is complete. The AD1674 provides an output signal (STS) which indicates when a conversion is in progress. This signal can be polled by the processor by reading it through

an external three-state buffer (or other input port). The STS signal can also be used to generate an interrupt upon completion of a conversion, if the system timing requirements are critical (bear in mind that the maximum conversion time of the AD1674 is only 10 microseconds) and the processor has other tasks to perform during the ADC conversion cycle. Another possible time-out method is to assume that the ADC will take 10 microseconds to convert, and insert a sufficient number of "no-op" instructions to ensure that 10 microseconds of processor time is consumed.

Once it is established that the conversion is finished, the data can be read. In the case of an ADC of 8-bit resolution (or less), a single data read operation is sufficient. In the case of converters with more data bits than are available on the bus, a choice of data formats is required, and multiple read operations are needed. The AD1674 includes internal logic to permit direct interface to 8-bit or 16-bit data buses, selected by the 12/$\overline{8}$ input. In 16-bit bus applications (12/$\overline{8}$ HIGH) the data lines (DB11 through DB0) may be connected to either the 12 most significant or 12 least significant bits of the data bus. The remaining four bits should be masked in software. The interface to an 8-bit data bus (12/$\overline{8}$ LOW) contains the 8 MSBs (DB11 through DB4). The odd address (A_0 HIGH) contains the 4 LSBs (DB3 through DB0) in the upper half of the byte, followed by four trailing zeroes, thus eliminating bit masking instructions.

	D7						D0
XXX0 (EVEN ADDR):	DB11 (MSB)	DB10	DB9	DB8	DB7	DB6	DB5	DB4
XXX1 (ODD ADDR):	DB3	DB2	DB1	DB0 (LSB)	0	0	0	0

AD1674 Data Format for 8-Bit Bus

8085A INTERFACE

Figure 8 illustrates the use of the AD1674 operating in full-control mode from the 8085A. This provides an example of the implementation of the timing modifications necessary when using the AD1674 in place of an existing AD674A application, discussed in Table II and associated text. Figure 9 shows the convert start timing diagram; Figure 10 provides information on read timing.

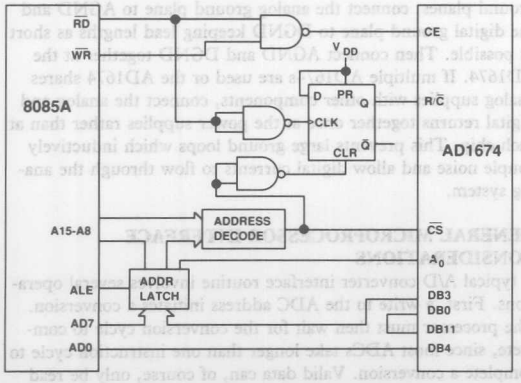


Figure 8. 8085A – AD1674 with R/$\overline{C}$-Delayed Control Interface

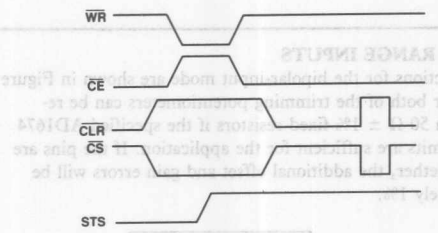


Figure 9. 8085A Convert Start

The convert start cycle starts when the WR signal goes LOW, forcing CE to go HIGH. With $\overline{CLR}$ signal LOW prior to this, R/$\overline{C}$ is set LOW. When $\overline{CLR}$ goes HIGH, R/$\overline{C}$ will remain LOW until the next rising edge of CLK.

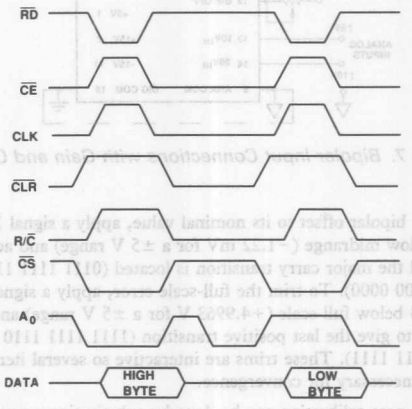


Figure 10. 8085A Read

The High Byte is read first. The Read cycle starts when $\overline{RD}$ goes LOW, causing CE to go HIGH. $\overline{CS}$ is already LOW, making $\overline{CLR}$ and PR HIGH on the D-flop. This causes R/$\overline{C}$ to go HIGH on the rising edge of CLK. R/$\overline{C}$ will not go LOW until $\overline{CS}$ goes HIGH, forcing $\overline{CLR}$ to go LOW thus putting the D-flop in a steady state of Q LOW. The cycle repeats for the Low Byte read.

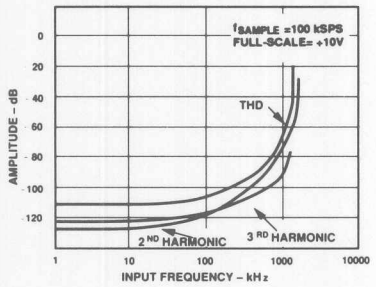


Figure 11. Harmonic Distortion vs. Input Frequency

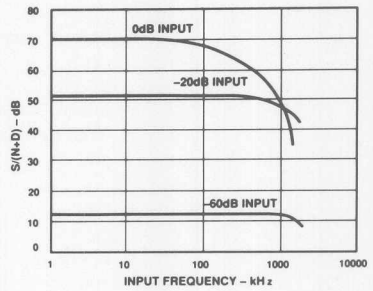


Figure 12. S/(N+D) vs. Input Frequency and Amplitude

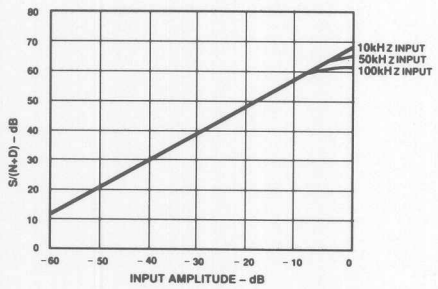


Figure 13. S/(N+D) vs. Input Amplitude

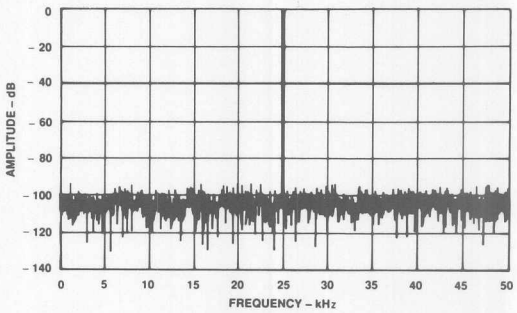


Figure 14. Nonaveraged 2048 Point FFT at 100 kSPS, f_{IN} = 25.049 kHz

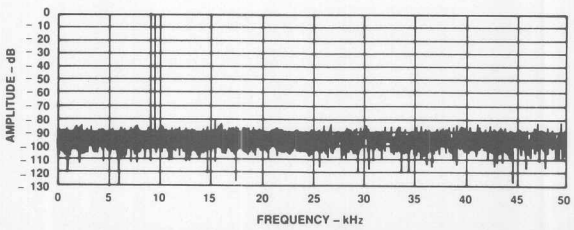
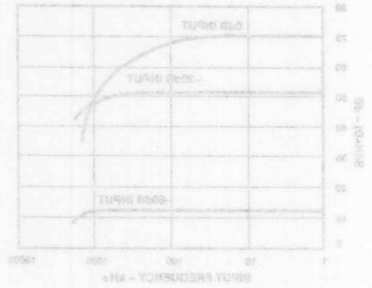
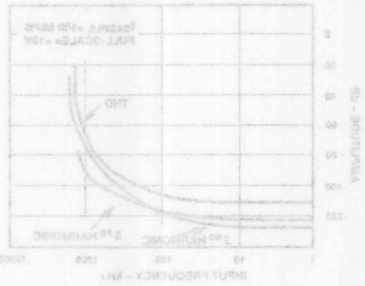
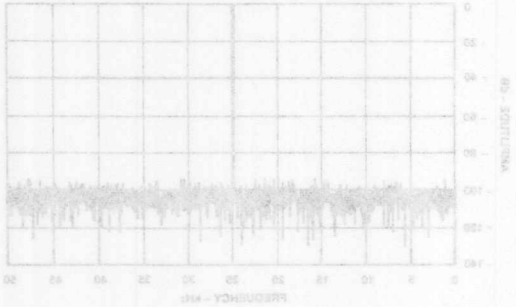
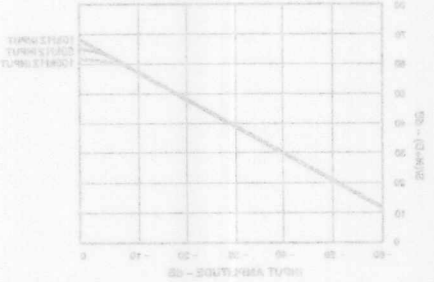


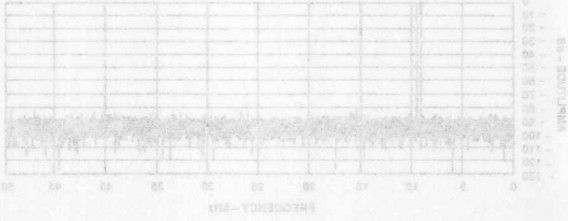
Figure 15. IMD Plot for f_{IN} = 9.08 kHz (fa), 9.58 kHz (fb)









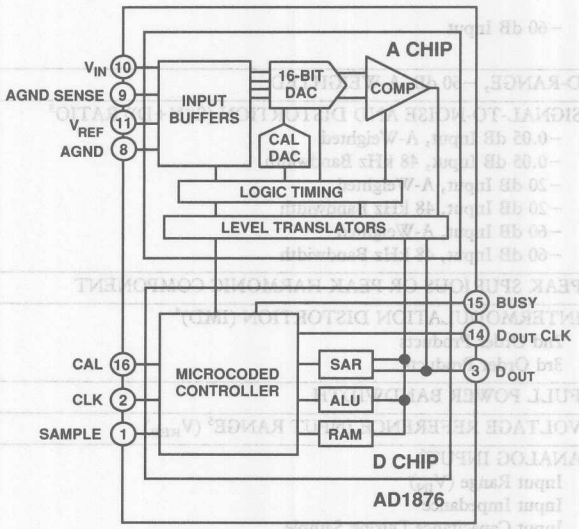


16-Bit 100 kSPS Sampling ADC

AD1876

FEATURES
Autocalibrating
0.002% THD
90 dB S/(N+D)
1 MHz Full Power Bandwidth
On-Chip Sample & Hold Function
2× Oversampling for Audio Applications
16-Pin DIP Package
Serial Twos Complement Output Format
Low Input Capacitance—typ 50 pF
AGND Sense for Improved Noise Immunity

FUNCTIONAL BLOCK DIAGRAM



PRODUCTION DESCRIPTION

The AD1876 is a 16-bit serial output sampling A/D converter which uses a switched capacitor/charge redistribution architecture to achieve a 100 kSPS conversion rate (10 μs total conversion time). Overall performance is optimized by digitally correcting internal nonlinearities through on-chip autocalibration.

The circuitry of the AD1876 is partitioned onto two monolithic chips, a digital control chip fabricated with Analog Devices' DSP CMOS process and an analog ADC chip fabricated with the BiMOS II process. Both chips are contained in a single package.

The serial output interface requires an external clock and sample command signal. The output data rate may be as high as 2.08 MHz, and is controlled by the external clock. The twos complement format of the output data is MSB first and is directly compatible with the NPC SM5805 digital decimation filter used in consumer audio products. The AD1876 is also compatible with a variety of DSP processors.

The AD1876 is packaged in a space saving 16-pin plastic DIP and operates from +5 V and ±12 V supplies; typical power consumption is 235 mW. The digital supply (V_{DD}) is isolated from the linear supplies (V_{EE} and V_{CC}) for reduced digital crosstalk. Separate analog and digital grounds are also provided.

AD1876—SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)[1]

Parameter	AD1876J Min	Typ	Max	Units
TEMPERATURE RANGE	0		70	°C
TOTAL HARMONIC DISTORTION (THD)[2]				
−0.05 dB Input		−95	**−88**	dB
		0.002	**0.004**	%
−20 dB Input		−78		dB
		0.01		%
−60 dB Input		−40		dB
		1.0		%
D-RANGE, −60 dB, A-WEIGHTED		92		dB
SIGNAL-TO-NOISE AND DISTORTION (S/(N+D)) RATIO[3]				
−0.05 dB Input, A-Weighted		92		dB
−0.05 dB Input, 48 kHz Bandwidth	**83**	90		dB
−20 dB Input, A-Weighted		73		dB
−20 dB Input, 48 kHz Bandwidth		70		dB
−60 dB Input, A-Weighted		34		dB
−60 dB Input, 48 kHz Bandwidth		31		dB
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−99	**−89**	dB
INTERMODULATION DISTORTION (IMD)[4]				
2nd Order Products		−102		dB
3rd Order Products		−98		dB
FULL POWER BANDWIDTH		1		MHz
VOLTAGE REFERENCE INPUT RANGE[5] (V_{REF})	3	5	10.0	V
ANALOG INPUT[6]				
Input Range (V_{IN})			±V_{REF}	V
Input Impedance		*		
Input Capacitance During Sample		50*		pF
Aperture Delay		6		ns
Aperture Jitter		100		ps
POWER SUPPLIES				
Operating Current				
I_{CC}		9	12	mA
I_{EE}		9	12	mA
I_{DD}		3	12	mA
Power Consumption		235	350	mW

NOTES

[1]V_{REF} = 5.00 V; conversion rate = 96 kSPS; f_{IN} = 1.06 kHz; V_{IN} = −0.05 dB unless otherwise indicated. All measurements referred to a 0 dB (10 V_{PP}) input signal. Values are post calibration.

[2]Includes first 19 harmonics.

[3]Minimum value of S/(N+D) corresponds to 5.0 V reference; typical values of S/(N+D) correspond to 10.0 V reference.

[4]f_a = 1008 Hz; f_b = 1055 Hz. See Definition of Specifications section and Figure 14.

[5]See Applications section for recommended voltage reference circuit and Figure 11 for performance with other reference voltage values.

[6]See Applications section for recommended input buffer circuit.

*For explanation of input characteristics, see "Analog Input" section.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all devices at final electrical test at worst case temperature. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

ORDERING GUIDE

Model	Temperature Range	THD dB	Package Description	Package Option*
AD1876JN	0°C to +70°C	−95	Plastic 16-Pin DIP	N-16

*N = Narrow Plastic DIP. For outline information see Package Information section.

DIGITAL SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter		Test Conditions	Min	Typ	Max	Units
LOGIC INPUTS						
V_{IH}	High Level Input Voltage		2.4			V
V_{IL}	Low Level Input Voltage		−0.3		0.8	V
I_{IH}	High Level Input Current	$V_{IH} = V_{DD}$	−10		+10	μA
I_{IL}	Low Level Input Current	V_{IL} = 0 V	−10		+10	μA
C_{IN}	Input Capacitance				10	pF
LOGIC OUTPUTS						
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	V_{DD}−1 V			V
		I_{OH} = 0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA			0.4	V

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all devices at final electrical test at worst case temperature. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to V_{EE} . . . . . −0.3 V to +26.4 V
V_{DD} to DGND . . . . . −0.3 V to +7 V
V_{CC} to AGND . . . . . −0.3 V to +18 V
V_{EE} to AGND . . . . . −18 V to +0.3 V
AGND to DGND . . . . . ±0.3 V
Digital Inputs to DGND . . . . . 0 V to 5.5 V
Analog Inputs, V_{REF} to AGND . . . . . (V_{CC} + 0.3 V) to (V_{EE} −0.3 V)
Soldering . . . . . +300°C, 10 sec
Storage Temperature . . . . . −60°C to +100°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

The AD1876 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD1876 has been classified as a Category 1 Device.



Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment, and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam discharged to the destination socket before devices are removed. For further information on ESD precaution, refer to Analog Devices' *ESD Prevention Manual.*

TIMING SPECIFICATIONS[1] (T_{min} to T_{max}, V_{CC} = +12 V ± 5%, V_{EE} = −12 V ± 5%, V_{DD} = +5 V ± 10%, V_{REF} = 5.00 V)

Parameter	Symbol	Min	Typ	Max	Units
Sampling Rate[2]	$f_S = 1/t_S$	1		100	kSPS
Sampling Period[2]	$t_S = 1/f_S$	10		1000	μs
Acquisition Time (Included in t_S)	t_A	2			μs
Calibration Time	t_{CT}			5000	t_C
CLK Period	t_C	480			ns
CAL to BUSY Delay	t_{CALB}	0			ns
CLK to BUSY Delay	t_{CB}	50	120	175	ns
CLK to D_{OUT} Hold Time	t_{CD}	10			ns
CLK HIGH	t_{CH}	160			ns
CLK LOW	t_{CL}	50			ns
D_{OUT} CLK LOW	t_{DCL}	30	80	200	ns
SAMPLE LOW to 1st CLK Delay	t_{SC}	50			ns
CAL HIGH Time	t_{CALH}	4			t_C
CLK to D_{OUT} CLK	t_{CDH}	150	200	275	ns
SAMPLE LOW	t_{SL}	50			ns

NOTES
[1]See Figure 1 and Figure 2 and the Conversion Control and Autocalibration sections for detailed explanations of the above timing.
[2]Depends upon external clock frequency; includes acquisition time and conversion time. The minimum sampling rate/maximum sampling period is specified to account for droop of the internal sample/hold. Operation at slower rates than specified may degrade performance.

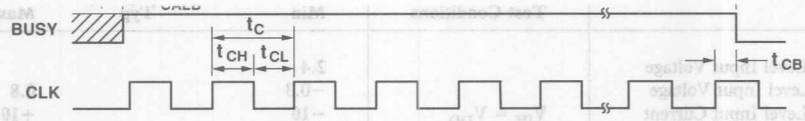


Figure 1. AD1876 Calibration Timing

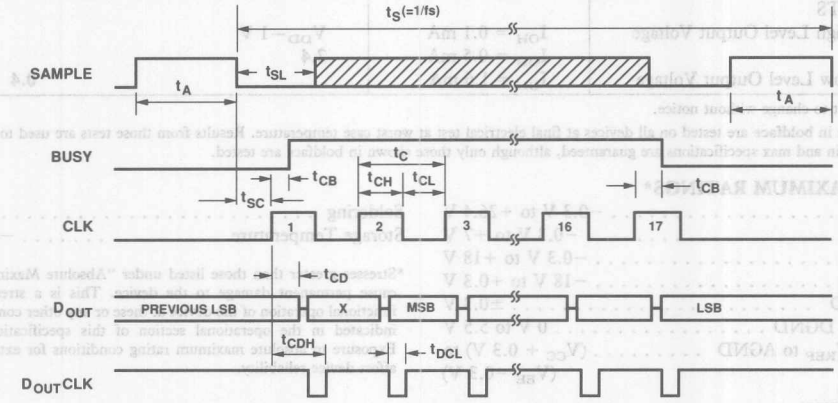


Figure 2. Recommended AD1876 Conversion Timing

Definition of Specifications

NYQUIST FREQUENCY

An implication of the Nyquist sampling theorem, the "Nyquist Frequency" of a converter is that input frequency which is one-half the sampling frequency of the converter.

TOTAL HARMONIC DISTORTION

Total harmonic distortion (THD) is measured as the ratio of the rms sum of the first nineteen harmonic components to the rms value of a 1 kHz full-scale sine wave input signal and is expressed in percent (%) or decibels (dB). For input signals or harmonics that are above the Nyquist frequency, the aliased component is used.

SIGNAL-TO-NOISE PLUS DISTORTION RATIO

Signal-to-noise plus distortion (S/N+D) is defined to be the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

D-RANGE DISTORTION

D-range distortion is the ratio of the distortion plus noise to the signal at a signal amplitude of −60 dB. In this case, an A-weight filter is used. The value specified for D-range performance is the ratio measured plus 60 dB.

BANDWIDTH

The full power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

INTERMODULATION DISTORTION (IMD)

With inputs consisting of sine waves at two frequencies, f_a and f_b, any device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of $mf_a \pm nf_b$, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are $(f_a + f_b)$ and $(f_a - f_b)$, and the third order terms are $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$ and $(f_a - 2f_b)$. The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude, and the peak value of their sum is −0.05 dB from full scale. The IMD products are normalized to a 0 dB input signal.

APERTURE DELAY

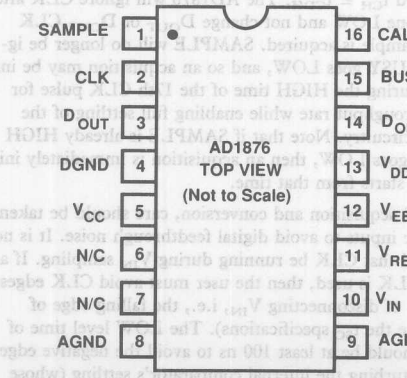
Aperture delay is the time required after SAMPLE is taken LOW for the internal sample-hold of the AD1876 to open, thus holding the value of V_{IN}.

APERTURE JITTER

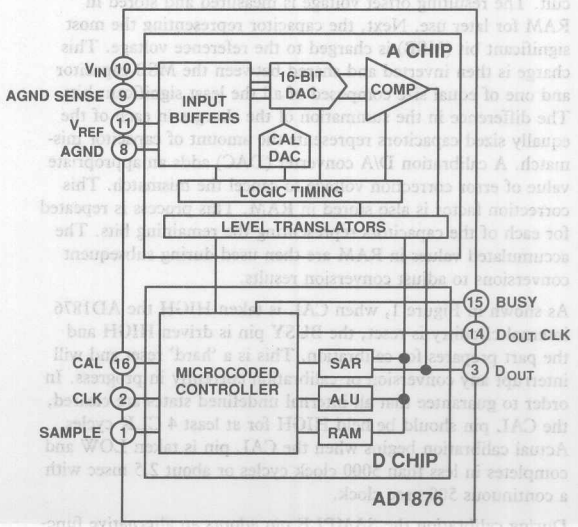
Aperature jitter is the variation in the aperture delay from sample to sample.

Pin No.	Name	Type	Description
1	SAMPLE	DI	V_{IN} Acquisition Control Pin. During conversion, SAMPLE controls the state of the internal Sample-Hold Amplifier and initiates conversion (see "Conversion Control" paragraph). During calibration, SAMPLE is active HIGH, forcing D_{OUT} (Pin 3) LOW. If SAMPLE is LOW during calibration, D_{OUT} will output diagnostic information (See "Autocalibration" paragraph.)
2	CLK	DI	Master Clock Input. The AD1876 requires 17 clock pulses to execute a conversion. CLK is also used to derive D_{OUT} CLK (Pin 14). During calibration, 5000 clock pulses are applied.
3	D_{OUT}	DO	Serial Output Data, Twos Complement format.
4	DGND	P	Digital Ground.
5	V_{CC}	P	+12 V Analog Supply Voltage.
6	N/C	–	No Connection.
7	N/C	–	No Connection.
8	AGND	P/AI	Analog Ground.
9	AGND SENSE	AI	Analog Ground Sense.
10	V_{IN}	AI	Analog Input Voltage, referred the AGND SENSE.
11	V_{REF}	AI	External Voltage Reference Input, referred to AGND.
12	V_{EE}	P	−12 V Analog Supply Voltage.
13	V_{DD}	P	+5 V Logic Supply Voltage.
14	D_{OUT} CLK	DO	The rising edge of D_{OUT} CLK may be used to latch D_{OUT} (Pin 3). D_{OUT} CLK is derived from CLK.
15	BUSY	DO	Status Line for Converter. Active HIGH, indicating a conversion or calibration in progress.
16	CAL	DI	Calibration Control Pin (asynchronous).

Type: AI = Analog Input.
DI = Digital Input.
DO = Digital Output.
P = Power.



Package Pinout



Functional Block Diagram

FUNCTIONAL DESCRIPTION

The AD1876 is a 16-bit analog-to-digital converter including a sample/hold input circuit, successive approximation register, ground sensing circuitry, serial output port and a microcontroller based autocalibration circuit. These functions are segmented onto two monolithic chips, an analog signal processor and a digital controller. Both chips are contained within the AD1876 package.

The AD1876 employs a successive-approximation technique to determine the value of the analog input voltage. However, instead of the traditional laser-trimmed resistor-ladder approach, the AD1876 uses a capacitor-array, charge-redistribution technique. An array of binary-weighted capacitors subdivides the input value to perform the actual analog to digital conversion. This capacitor array also serves a sample/hold function without the need for additional external circuitry.

The autocalibration circuit within the AD1876 employs a microcontroller and calibration DAC to measure and compensate capacitor mismatch errors. As each error is determined, its value is stored in on-chip memory (RAM). Subsequent conversions use these RAM values to improve conversion accuracy. The autocalibration routine may be invoked at any time. Autocalibration insures high performance while eliminating the need for any user adjustments, and is described in detail below.

The microcontroller controls all of the various functions within the AD1876. These include the actual successive approximation routine, the autocalibration routine, the sample/hold operation, and the serial data transmission.

AUTOCALIBRATION

The AD1876 achieves rated performance without the need for user trims or adjustments. This is accomplished through the use of on-chip autocalibration.

In the autocalibration sequence, sample/hold offset is nulled by internally connecting the input circuit to the ground sense circuit. The resulting offset voltage is measured and stored in RAM for later use. Next, the capacitor representing the most significant bit (MSB) is charged to the reference voltage. This charge is then inverted and shared between the MSB capacitor and one of equal size composed of all the least significant bits. The difference in the summation of the charges in each of the equally sized capacitors represents the amount of capacitor mismatch. A calibration D/A converter (DAC) adds an appropriate value of error correction voltage to cancel the mismatch. This correction factor is also stored in RAM. This process is repeated for each of the capacitors representing the remaining bits. The accumulated values in RAM are then used during subsequent conversions to adjust conversion results.

As shown in Figure 1, when CAL is taken HIGH the AD1876 internal circuitry is reset, the BUSY pin is driven HIGH and the part prepares for calibration. This is a 'hard' reset and will interrupt any conversion or calibration currently in progress. In order to guarantee that all internal undefined states are cleared, the CAL pin should be held HIGH for at least 4 CLK cycles. Actual calibration begins when the CAL pin is taken LOW and completes in less than 5000 clock cycles or about 2.5 msec with a continuous 500 nsec clock.

During calibration the SAMPLE pin adopts an alternative function. If it is held LOW, D_{OUT} provides diagnostic test information (not intended to be used by the customer). If SAMPLE is held HIGH, D_{OUT} will be forced LOW. In either case, D_{OUT} CLK will continue pulsing. Since the SAMPLE pin has no control over the actual calibration process, normal conversion timing may also be used for calibration. In this case, however, the D_{OUT} pin will output test information during those periods that SAMPLE is LOW. BUSY going LOW will always indicate the end of calibration.

A calibration sequence should be followed by one "dummy" conversion to clear the internal circuitry of the AD1876 in order to guarantee subsequent conversion accuracy.

In most applications, it is sufficient to calibrate the AD1876 only upon power-up, in which case care should be taken that the power supplies and voltage reference have stabilized first.

CONVERSION CONTROL

The AD1876 is controlled by two signals: SAMPLE and CLK, as shown in Figure 2. It is assumed that the part has been calibrated and the digital I/O pins have the levels shown at the start of the timing diagram.

A conversion consists of an input acquisition followed by 17 clock pulses which are required to run the 16-bit internal successive approximation routine. The analog input is acquired by taking the SAMPLE line HIGH for a minimum acquisition time of t_A. The actual sample taken is the voltage present on V_{IN} at the instant the SAMPLE pin is brought LOW. Care should be taken to ensure that this negative edge is well defined and jitter free to reduce the uncertainty (noise) in ac signal acquisition. On that edge the AD1876 commits itself to the initiated conversion—the input at V_{IN} is disconnected from the internal capacitor array and the SAMPLE input will be ignored until the conversion is completed (i.e., BUSY goes LOW). After a delay of at least t_{SC} (SAMPLE to CLK setup) the 17 CLK cycles are applied. BUSY is asserted after the first positive edge on CLK and reset after the 17th. Both the D_{OUT} and the D_{OUT} CLK outputs are generated in response to the rising edges of valid CLK pulses. As indicated in the timing diagram, the 2s complement output data is presented MSB first. This data may be captured with the rising edge of D_{OUT} CLK or the falling edge of CLK provided $t_{CH} \geq t_{CDH}$. The AD1876 will ignore CLK after BUSY has gone LOW and not change D_{OUT} or D_{OUT} CLK until a new sample is acquired. SAMPLE will no longer be ignored after BUSY goes LOW, and so an acquisition may be initiated even during the HIGH time of the 17th CLK pulse for maximum throughput rate while enabling full settling of the sample/hold circuitry. Note that if SAMPLE is already HIGH when BUSY goes LOW, then an acquisition is immediately initiated and t_A starts from that time.

During signal acquisition and conversion, care should be taken with the logic inputs to avoid digital feedthrough noise. It is not recommended that CLK be running during V_{IN} sampling. If a continuous CLK is used, then the user must avoid CLK edges at the instant of disconnecting V_{IN}, i.e., the falling edge of SAMPLE (see the t_{SC} specifications). The LOW level time of CLK (t_{CL}) should be at least 100 ns to avoid the negative edge transition disturbing the internal comparator's settling (whose decision is latched on the positive edge of each valid CLK). For the same reason, it is also not recommended that the SAMPLE pin change state during conversion (i.e., until after BUSY returns LOW).

Internal dc error terms such as comparator voltage offset are sampled, stored on internal capacitors and used to correct for their corresponding errors when needed. Because these voltages

are stored on capacitors, they are subject to leakage decay and so require refreshing. For this reason the part is required to be run continuously—i.e., there is a minimum t_S specification. If the part has been idle for too long (i.e., t_S has expired) then a dummy conversion cycle is required to refresh these correction voltages.

BUSY is HIGH during a conversion and goes LOW when the conversion is completed. The twos complement output data is presented MSB first, with MSB data valid on the rising edge of the second D_{OUT} CLK pulse. Subsequent data is valid on rising edges of subsequent D_{OUT} CLK pulses. Table I illustrates the AD1876 output coding.

V_{IN}	Output Code
−Full Scale	100. . . 00
−Full Scale + 1 LSB	100. . . 01
Midscale − 1 LSB	111. . . 11
Midscale	000. . . 00
Midscale + 1 LSB	000. . . .01
Full Scale − 1 LSB	011. . . 10
Full Scale	011. . . 11

Table I. Serial Output Coding Format (Twos Complement)

A simple method for generating the required signals for the AD1876 is to connect one or more AD1876s to an NPC SM5805 digital filter. This device supplies all signals required to operate the AD1876 at a 96 kHz sample rate, which is 2 × F_S for audio applications. This is more fully discussed in the applications section of this data sheet, accompanied by Figures 9 and 10.

APPLICATIONS

POWER SUPPLIES AND DECOUPLING

The AD1876 has three power supply input pins. V_{EE} and V_{CC} provide the supply voltages to operate the analog portions of the AD1876 including the ADC and SHA. V_{DD} provides the supply voltage which operates the digital portions of the AD1876 including the serial output port and the autocalibration controller.

Decoupling capacitors should be used on all power supply pins. These capacitors should be placed as close as possible to the package pins as well as the ground connections. The logic supply (V_{DD}) should be decoupled to digital common (DGND) with a 0.1 μF ceramic capacitor, and the analog supplies (V_{EE} and V_{CC}) should be decoupled to analog common (AGND) with 4.7 μF and 0.1 μF tantalum capacitors in parallel, represented by C1. An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The recommended decoupling scheme is illustrated in Figure 3.

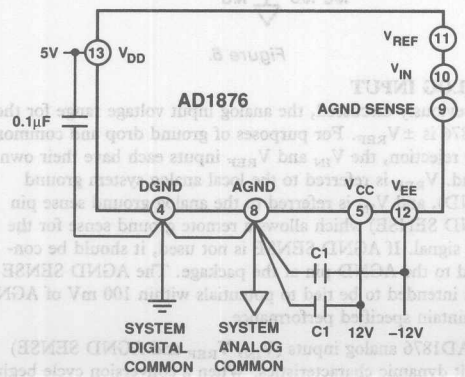


Figure 3. Grounding and Decoupling the AD1876

As with most high performance linear circuits, changes in the power supplies can produce undesired changes in the performance of the circuit. Analog Devices recommends that well regulated power supplies with less than 1% ripple be incorporated into the design of any system using these devices.

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is a significant issue. A 1.22 mA current through a 0.5 Ω trace will develop a voltage drop of 0.6 mV, which is 4 LSBs at the 16 bit level for a 10 V full-scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter ac noise.

Analog and digital signals should not share a common return path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them, if at all, only at right angles. A solid analog ground plane around the AD1876 will isolate large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

GROUNDING

The AD1876 has three grounding pins, designated ANALOG GROUND (AGND), DIGITAL GROUND (DGND) and ANALOG GROUND SENSE (AGND SENSE). The analog ground pin is the "high quality" ground reference point for the device. The analog ground pin should be connected to the analog common point in the system.

AGND SENSE is intended to be connected to the input signal ground reference point. This allows for slight differences in level between the analog ground point in the system and the input signal ground point. However, no more than 100 mV is recommended between the analog ground pin and the analog ground sense pin for specified performance.

The digital ground pin is the reference point for all of the digital signals that operate the AD1876. This pin should be connected to the digital common point in the system. As illustrated in Figure 3, the analog and digital grounds should be connected together at one point in the system.

The input voltage range is determined by the value of the reference voltage; in general, a reference voltage of n volts produces an input range of ±n volts. Signal-to-noise performance is increased proportionately with input signal range. The AD1876 is specified with a 5.0 V reference and an analog input of ±5 V. In the presence of a fixed amount of system noise, increasing the LSB size (which results from increasing the reference voltage) will increase the effective S/(N+D) performance for input values below the point where input distortion occurs. Figure 11 illustrates S/(N+D) as a function of input amplitude and reference voltage.

During a conversion, the switched capacitor array of the AD1876 presents a dynamically changing current load at the voltage reference as the successive-approximation algorithm cycles through various choices of capacitor weighting. The output impedance of the reference circuitry must be low so that the output voltage will remain sufficiently constant as the current drive changes. In most applications, this requires that the output of the voltage reference be buffered by an amplifier with low impedance at relatively high frequencies. A (10 μF or larger) capacitor connected between V_{REF} and AGND will reduce the demands on the reference by decreasing the magnitude of high frequency components.

The following two sections represent typical design approaches.

VOLTAGE REFERENCE—AUDIO APPLICATIONS

Audio applications require optimal ac performance over a relatively narrow temperature range, with low cost being important. Figure 4 shows one such approach towards attaining these goals. A voltage reference, consisting of a Zener diode, capacitor, resistor and op amp with typical component values, is shown. This simple circuit has the advantage of low cost, but the reference voltage value is sensitive to changes in the +12 V supply. Additionally, changes in the Zener value due to temperature variations will also be reflected in the reference voltage. R_{OPTION} may be required for other component selections if the Zener requires more current than the op amp can supply.

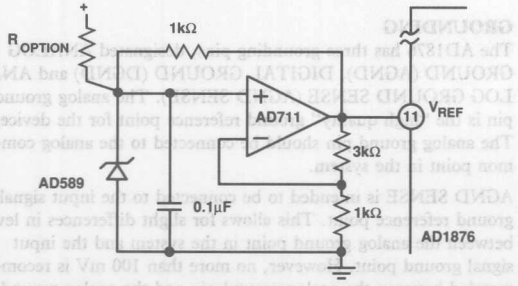


Figure 4. Low Cost Voltage Reference Circuit

VOLTAGE REFERENCE—PRECISION MEASUREMENT APPLICATIONS

In applications other than audio, parameters such as low drift over temperature and static accuracy are important. Figure 5 shows a voltage reference circuit featuring the 5 V AD586. The AD586 is a low cost reference which utilizes a buried Zener architecture to provide low noise and drift. Over the 0°C to +70°C tor, C_N, reduces the broadband noise of the AD586 output, thereby optimizing the overall performance of the AD1876.

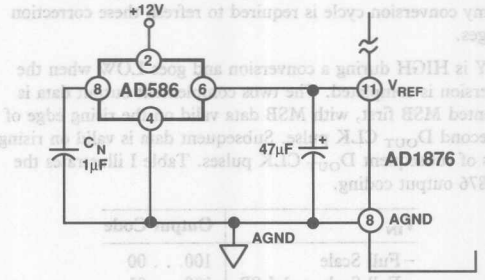


Figure 5.

For higher performance needs, the AD588 reference provides improved drift, low noise, and excellent initial accuracy. The AD588 uses a proprietary ion-implanted buried Zener diode in conjunction with laser-trimmed thin-film resistors for low offset and gain. The AD588 output is accurate to 0.65 mV from its value at +25°C over the 0°C to +70°C range. The circuit shown in Figure 6 includes a noise-reduction network on Pins 4, 6 and 7. The 1 μF capacitors form low pass filters with the internal resistance of the AD588 and external 3.9 kΩ resistor. This reduces the wide-band (to 1 MHz) noise of the AD588, providing optimum performance of the AD1876.

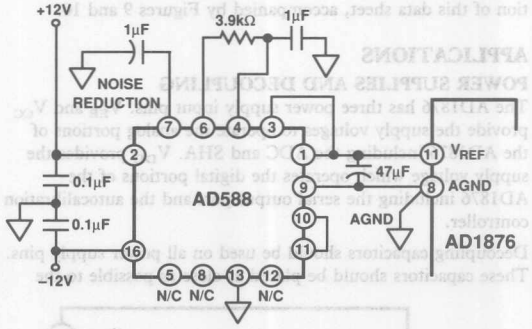


Figure 6.

ANALOG INPUT

As previously discussed, the analog input voltage range for the AD1876 is $\pm V_{REF}$. For purposes of ground drop and common-mode rejection, the V_{IN} and V_{REF} inputs each have their own ground. V_{REF} is referred to the local analog system ground (AGND), and V_{IN} is referred to the analog ground sense pin (AGND SENSE) which allows a remote ground sense for the input signal. If AGND SENSE is not used, it should be connected to the AGND pin at the package. The AGND SENSE pin is intended to be tied to potentials within 100 mV of AGND to maintain specified performance.

The AD1876 analog inputs (V_{IN}, V_{REF} and AGND SENSE) exhibit dynamic characteristics. When a conversion cycle begins, each analog input is connected to an internal, discharged 50 pF capacitor which then charges to the voltage present at the corresponding pin. The capacitor is disconnected when SAMPLE is

external source by this high initial charging current, an internal buffer amplifier is employed between the input and this capacitance for a few hundred nanoseconds. During this time the input pin exhibits typically 20 kΩ input resistance, 10 pF input capacitance and ±40 μA bias current. Next, the input is switched directly to the now precharged capacitor and allowed to fully settle, after which SAMPLE is taken LOW. During this time the input sees only a 50 pF capacitor. Once the sample is taken, the input is internally floated so that the external input source sees a very high input resistance and a parasitic input capacitance of typically only 2 pF. As a result, the only dominant input characteristic which must be considered is the high current steps which occur when the internal buffers are switched in and out.

In most cases, it is desirable to use external op amps to drive the AD1876. For ac applications where low cost and low distortion are desired, the AD711 may be used as shown in Figure 7. Another option is the 5532/5534 series. Care should always be taken with op amp selection—many available op amps do not meet the necessary low distortion requirements with even moderate loading conditions.

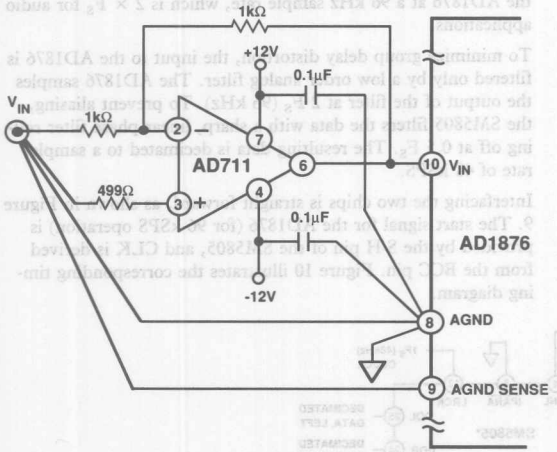


Figure 7.

TESTING THE AD1876

Analog Devices employs a high performance mixed signal VLSI tester to verify the electrical performance of every AD1876. The test system consists of two main sections, an input signal generator and a digital data and control section.

The stimulus section is responsible for providing a high purity, noise-free, band limited tone to the input of the device. This input frequency is 1.06 kHz. The test tone is passed through a bandpass filter to remove distortion products and then buffered by a high performance op amp. An external 5.000 V reference voltage is also supplied by this section.

The control section of the test equipment provides an external clock and the control signals for calibration, conversion and data transmission. This section of the tester also contains the processing unit that calculates the actual performance of the device under test.

under test digitizes the input waveform. This conversion is performed at a 96 kSPS rate and transmits the resulting serial data to the tester. The tester performs an FFT on the test data and determines the actual performance of the device.

AC PERFORMANCE

Using the aforementioned test methodology, ac performance of the AD1876 is measured. AC parameters, which include S/(N+D), THD, etc., reflect the AD1876's effect on the spectral content of the analog input signal. Figures 11 through 15 provide information on the AD1876's ac performance under a variety of conditions.

As a general rule, averaging the results from several conversions reduces the effects of noise and, therefore, improves such parameters as S/(N+D) and THD. AD1876 performance is optimized by operating the device at its maximum sample rate of 100 kSPS and digitally filtering the resulting bit stream to the desired signal bandwidth. This succeeds in distributing noise over a wider frequency range, thus reducing the noise density in the frequency band of interest. This subject is discussed in the following section.

OVERSAMPLING AND NOISE FILTERING

The Nyquist rate for a converter is defined as one-half its sampling rate. This is established by the Nyquist theorem, which requires that a signal be sampled at a rate corresponding to at least twice its widest bandwidth of interest in order to preserve the information content. Oversampling is a conversion technique in which the sampling frequency is an integral (2 or more) multiple of twice the frequency bandwidth of interest. In audio applications, the AD1876 can operate at a 2× oversampling rate.

In quantized systems, the information content of the analog input is represented in the frequency spectrum from dc to the Nyquist rate of the converter. Within this same spectrum are higher frequency aliased noise components. Antialias, or lowpass, filters are used at the input to the ADC to remove the portion of these noise components attributed to high frequency analog input noise. However, wideband noise contributed by the AD1876 will not be reduced by the antialias filter. The AD1876 contributed noise is evenly distributed from dc to the Nyquist rate, and this fact can be used to minimize its overall effect.

The AD1876 contributed noise effects can be reduced by oversampling—sampling at a rate higher than defined by the Nyquist theorem. This spreads the noise energy over a distribution of frequencies wider than the frequency band of interest, and by judicious selection of a digital filter, noise frequencies outside the bandwidth of interest may be eliminated. The process of quantization inherently produces noise, known as quantization noise. The magnitude of this noise is a function of the resolution of the converter, and manifests itself as a limit to the theoretical signal-to-noise ratio achievable. This limit is described by $S/(N+D) = (6.02\ n + 1.76 + 10 \log F_S/2\ F_a)$ dB, where n is the resolution of the converter in bits, F_S is the sampling frequency, and F_a is the signal bandwidth of interest. For audio bandwidth applications, the AD1876 is capable of operating at a 2× oversample rate (96 kSPS), which typically produces an improvement in S/(N+D) of 3 dB compared with operating at the Nyquist conversion rate of 48 kSPS. Oversampling has another advantage as well; the demands on the antialias filter are

lessened. In summary, system performance is optimized by running the AD1876 at or near its maximum sampling rate of 100 kHz and digitally filtering the resulting spectrum to eliminate undesired frequencies.

DSP INTERFACE

Figure 8 illustrates the use of the Analog Devices ADSP-2101 digital signal processor with the AD1876. The ADSP-2101 FO (flag out) pin of serial port 1 (SPORT 1) is connected to the SAMPLE line and is used to control acquisition of data. The ADSP-2101 timer is used to provide precise timing of the FO pin.

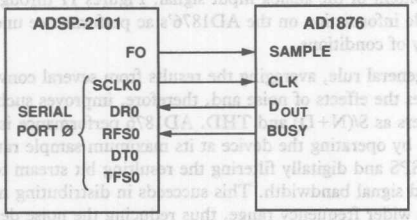


Figure 8. ADSP-2101 Interface

The SCLK pin of the ADSP-2101 SPORT0 provides the CLK input for the AD1876. The clock should be programmed to be approximately 2 MHz to comply with AD1876 specifications. To minimize digital feedthrough, the clock should be disabled (by setting Bit 14 in SPORT0 control register to 0) during data acquisition. Since the clock floats when disabled, a pulldown resistor of 12 k–15 kΩ should be connected to SCLK to ensure it will be LOW at the falling edge of SAMPLE. To maximize the conversion rate, the serial clock should be enabled immediately after SAMPLE is brought LOW (hold mode).

The AD1876 BUSY signal is connected to RF0 to notify SPORT0 when a new data word is coming. SPORT0 should be configured in normal, external, noninverting framing mode and can be programmed to generate an interrupt after the last data bit is received. To maximize the conversion rate, SAMPLE should be brought HIGH immediately after the last data bit is received.

SIGNAL PROCESSING

An audio spectrum analyzer can be produced by combining an AD1876 and an ADSP-2101 signal processing microcomputer. This system can analyze signals from dc to 50 kHz depending on the sample rate. This is ideal for applications such as audio analysis, but could also be applied to vibration analysis as well.

AUDIO DELAY LINE

A high performance, 16-bit stereo delay line can be constructed from two AD1876 audio ADCs, a signal processing microcomputer and two AD1856 audio DACs. Depending on the length of the internal buffer which produces the delay, a variable delay is possible. Other applications are also possible with only a change in software. For example, a reverb or echo effect could be generated as well.

AD1876 AND SM5805 DIGITAL FILTER @ 2 F_S

A simple method for generating the required signals for the AD1876 is to connect one or more AD1876s to an NPC SM5805 digital filter. This device supplies all signals required to operate the AD1876 at a 96 kHz sample rate, which is 2 × F_S for audio applications.

To minimize group delay distortion, the input to the AD1876 is filtered only by a low order analog filter. The AD1876 samples the output of the filter at 2 F_S (96 kHz). To prevent aliasing, the SM5805 filters the data with a sharp, linear phase filter rolling off at 0.5 F_S. The resulting data is decimated to a sample rate of 48 kSPS.

Interfacing the two chips is straight forward, as shown in Figure 9. The start signal for the AD1876 (for 96 kSPS operation) is provided by the S/H pin of the SM5805, and CLK is derived from the BCC pin. Figure 10 illustrates the corresponding timing diagram.

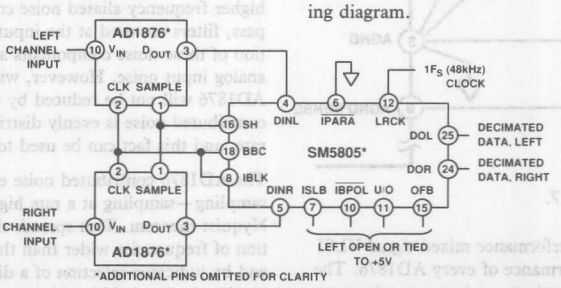


Figure 9. AD1876 and SM5805 Digital Filter

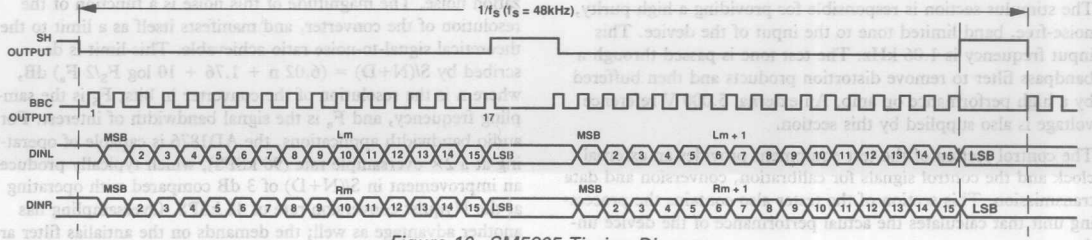


Figure 10. SM5805 Timing Diagram

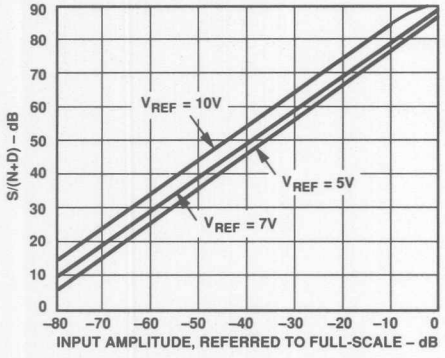


Figure 11. S/(N+D) vs. V_{REF} vs. Input Amplitude

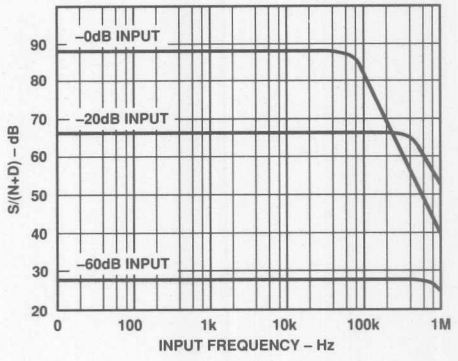


Figure 12. S/(N+D) vs. Input Frequency and Amplitude

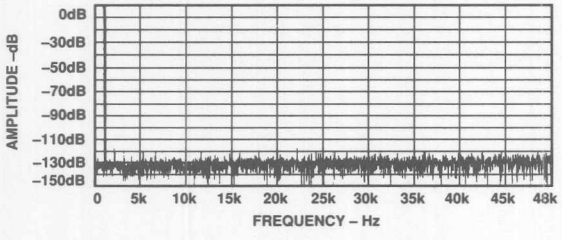


Figure 13. 4096 Point FFT at 96 kSPS, f_{IN} = 1.06 kHz

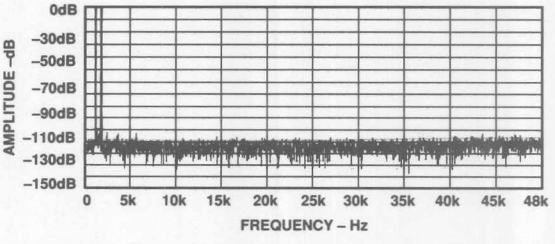


Figure 14. IMD Plot for f_{IN} = 1008 Hz (f_a), 1055 Hz (f_b) at 96 kSPS

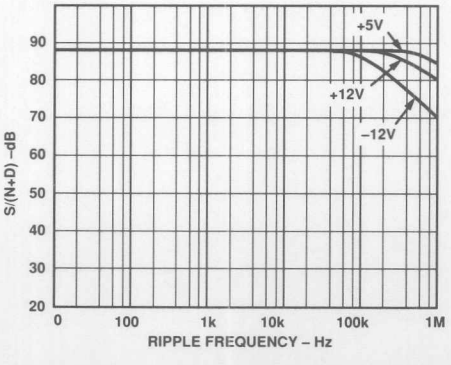
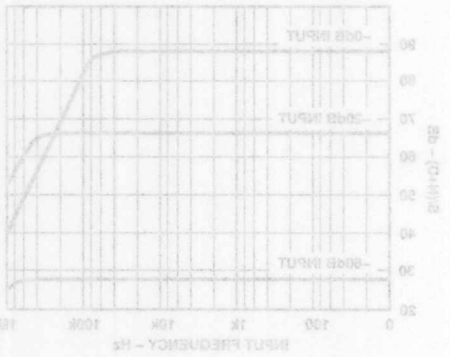
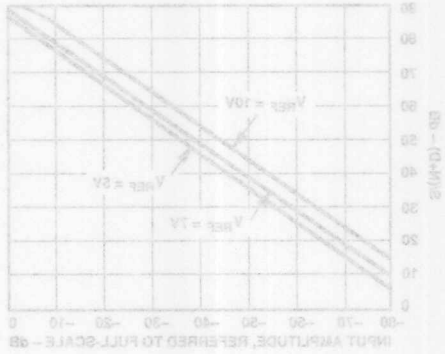
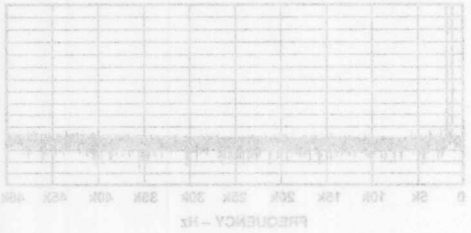
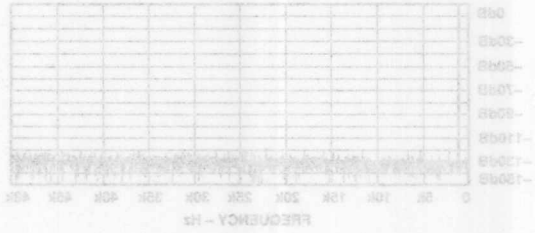


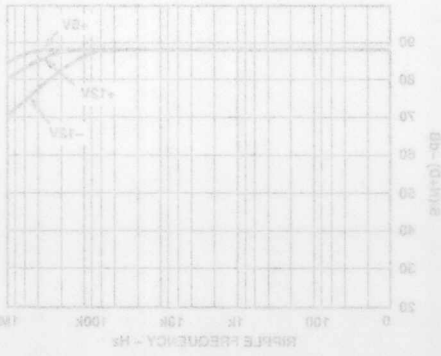
Figure 15. Power Supply Rejection (f_{IN} = 1.06 kHz, f_{SAMPLE} = 96 kSPS, V_{RIPPLE} = 0.3 V p–p)











16-Bit Oversampled ADC

AD1878

FEATURES

- Dual Channel
- 98 dB Signal-to-Noise Ratio
- 98 dB THD+N
- 0.0004 dB Passband Ripple
- 115 dB Stopband Attenuation
- 64× Oversampling
- Linear Phase

APPLICATIONS

- DAT and DCC Tape Players
- Direct-to-Disc Recorders
- Digital Audio Editors
- Digital Mixing Consoles

PRODUCT DESCRIPTION

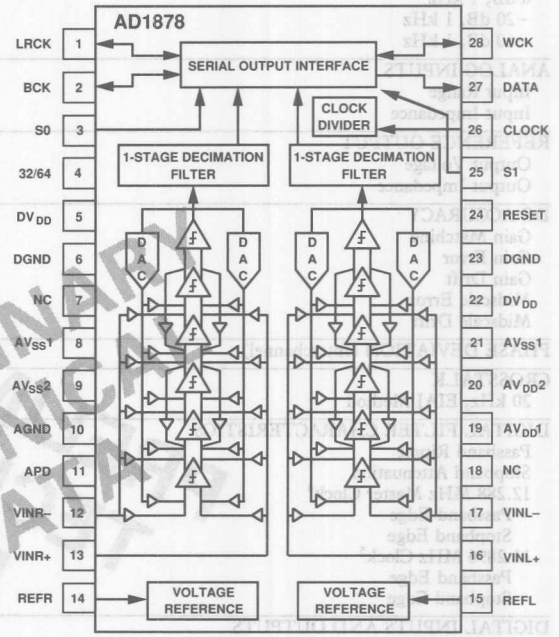
The AD1878 is a two-channel, 16-bit oversampled digital audio ADC. Each channel incorporates a high performance one-bit noise shaping modulator and a digital decimating filter. An on-board voltage reference is also included. ADC output data is transmitted from a flexible serial data port. The circuitry of the AD1878 is segmented between two monolithic chips.

The voltage reference and one-bit modulators are fabricated on a BiCMOS chip. The reference circuitry provides a reference voltage that is stable over temperature and time. Using an external master clock, the one-bit modulators operate at a 64 × F_S oversampling ratio. This oversampling ratio permits the antialias filters to be simple resistor-capacitor combinations and results in linear phase throughout the passband. The modulators are 5th order and employ differential switched capacitor filters to provide the required noise shaping characteristics and extremely low distortion.

The digital decimating filters and serial port are fabricated using a CMOS process. Using a proprietary technique, these single-stage digital filters provide a narrow transition band, deep stopband attenuation and low passband ripple.

The output port provides a single, serial bit stream which can operate in several MASTER or SLAVE modes. It is controlled by a clock and mode select pins. The format of the data is twos complement, MSB first. The output signals are TTL and 5 volt CMOS compatible. Output words may be transmitted in a right-justified, I^2S or user-defined format.

FUNCTIONAL BLOCK DIAGRAM



The AD1878 operates with ±5 volt power supplies. Separate digital and analog power supplies and ground connections are provided for reduced digital crosstalk. The AD1878 is guaranteed to operate over a temperature range of −25°C to +70°C and is packaged in a 28-pin plastic DIP.

PRODUCT HIGHLIGHTS

1. 64 × F_S sampling rate.
2. From 2.5 kHz to 50 kHz output word rates.
3. Passband ripple is less than 0.001 dB.
4. Stopband attenuation is 115 dB.
5. Excellent low level signal performance is achieved.
6. No sample-and-hold circuits are required.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD1878—SPECIFICATIONS @ ± 5 volt Supplies, T_A = +25°C, Clock = 12.288 MHz

Parameter	Target	Units
RESOLUTION	18	Bits
OVERSAMPLING RATIO	64	× F_S
DYNAMIC RANGE, 0 kHz to 20 kHz, No A-Weight Filter		
Stereo Mode[1]	98	dB
Mono Mode[2]	101	dB
SIGNAL TO (NOISE + DISTORTION)		
0 dB, 1 kHz	98	dB
−20 dB, 1 kHz	85	dB
−60 dB, 1 kHz	45	dB
ANALOG INPUTS		
Input Range	±3	V
Input Impedance	12.8	kΩ
REFERENCE OUTPUT		
Output Voltage	3	V
Output Impedance	TBD	
DC ACCURACY		
Gain Matching	TBD	dB
Gain Error	TBD	%
Gain Drift	TBD	ppm/°C
Midscale Error	20	LSBs
Midscale Drift	TBD	ppm/°C
PHASE DEVIATION (Interchannel)	Below Measurable Limit	Degrees
CROSSTALK		
20 kHz, EIAJ Method	105	dB
DIGITAL FILTER CHARACTERISTICS		
Passband Ripple	0.001	dB
Stopband Attenuation	115	dB
12.288 MHz Master Clock[4]		
Passband Edge	21.7	kHz
Stopband Edge	26.2	kHz
11.2896 MHz Clock[5]		
Passband Edge	20	kHz
Stopband Edge	24.1	kHz
DIGITAL INPUTS AND OUTPUTS		
V_{IH}	2.0	V
V_{IL}	0.8	V
I_{IH} @ V_{IH} = 5 V	10	µA
I_{IL} @ V_{IL} = 0 V	10	µA
V_{OH} @ I_{OH} = 4 mA	4.5	V
V_{OL} @ I_{OL} = 4 mA	0.5	V
NOMINAL MASTER CLOCK FREQUENCY	12.288	MHz
POWER SUPPLIES		
Voltage, $+V_L$ and $+V_S$	5	V
Voltage, $-V_L$ and $-V_S$	−5	V
Current, $+I_L$ and $+I_S$	TBD	mA
Current, $-I_L$ and $-I_S$	TBD	mA
POWER DISSIPATION		
Operation	900	mW
Power Down APD = "1"	400	mW
POWER SUPPLY REJECTION RATIO	67	dB
TEMPERATURE RANGE		
Specification	25	°C
Operation	−25 to +70	°C
Storage	−60 to +100	°C

PRELIMINARY TECHNICAL DATA

NOTES
[1]Stereo Mode uses output of each channel independently.
[2]Mono Mode sums output words to derive higher Dynamic Range.
[3]16-bit LSBs.
[4]Master Clock Frequency for 48 kHz sample rate.
[5]Master Clock Frequency for 44.1 kHz sample rate.
Specifications subject to change without notice.

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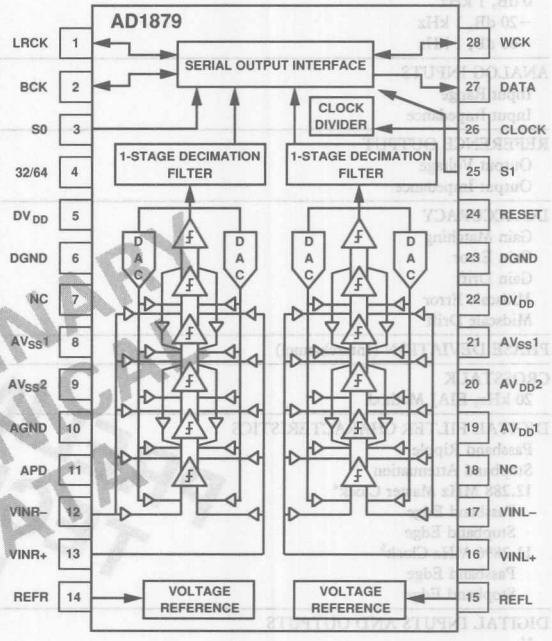
High Performance Stereo 18-Bit Oversampled ADC

AD1879

FEATURES
- Dual Channel
- 103 dB Signal-to-Noise Ratio
- 98 dB THD+N
- 0.0004 dB Passband Ripple
- 115 dB Stopband Attenuation
- 64× Oversampling
- Linear Phase

APPLICATIONS
- Pro Audio Digital Tape Recorders
- Direct-to-Disc Recorders
- Digital Audio Editors
- Digital Mixing Consoles

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1879 is a two-channel, 18-bit oversampled digital audio ADC. Each channel incorporates a high performance one-bit noise shaping modulator and a digital decimating filter. An on-board voltage reference is also included. ADC output data is transmitted from a flexible serial data port. The circuitry of the AD1879 is segmented between two monolithic chips.

The voltage reference and one-bit modulators are fabricated on a BiCMOS chip. The reference circuitry provides a reference voltage that is stable over temperature and time. Using an external master clock, the one-bit modulators operate at a 64 × F_S oversampling ratio. This oversampling ratio permits the antialias filters to be simple resistor-capacitor combinations and results in linear phase throughout the passband. The modulators are 5th order and employ differential switched capacitor filters to provide the required noise shaping characteristics and extremely low distortion.

The digital decimating filters and serial port are fabricated using a CMOS process. Using a proprietary technique, these single-stage digital filters provide a narrow transition band, deep stopband attenuation and low passband ripple.

The output port provides a single, serial bit stream which can operate in several MASTER or SLAVE modes. It is controlled by clock and mode select pins. The format of the data is twos complement, MSB first. The output signals are TTL and 5 volt CMOS compatible. Output words may be transmitted in a right-justified, I^2S or user-defined format.

The AD1879 operates with ±5 volt power supplies. Separate digital and analog power supplies and ground connections are provided for reduced digital crosstalk. The AD1879 is guaranteed to operate over a temperature range of −25°C to +70°C and is packaged in a 28-pin plastic DIP.

PRODUCT HIGHLIGHTS

1. 64 × F_S sampling rate.
2. Passband ripple is less than 0.001 dB.
3. Stopband attenuation is 115 dB.
4. Excellent low level signal performance is achieved.
5. No sample-and-hold circuits are required.
6. Fully differential analog inputs.
7. Extremely flexible serial data output port.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	Range	Units
RESOLUTION	18	Bits
OVERSAMPLING RATIO	64	$\times F_S$
DYNAMIC RANGE, 0 kHz to 20 kHz, No A-Weight Filter		
Stereo Mode[1]	103	dB
Mono Mode[2]	106	dB
SIGNAL TO (NOISE + DISTORTION)		
0 dB, 1 kHz	98	dB
−20 dB, 1 kHz	85	dB
−60 dB, 1 kHz	45	dB
ANALOG INPUTS		
Input Range	±3	V
Input Impedance	12.8	kΩ
REFERENCE OUTPUT		
Output Voltage	3	V
Output Impedance	TBD	
DC ACCURACY		
Gain Matching	TBD	dB
Gain Error	TBD	%
Gain Drift	TBD	ppm/°C
Midscale Error	20	LSBs
Midscale Drift	TBD	ppm/°C
PHASE DEVIATION (Interchannel)	Below Measurable Limit	Degrees
CROSSTALK		
20 kHz, EIAJ Method	105	dB
DIGITAL FILTER CHARACTERISTICS		
Passband Ripple	0.001	dB
Stopband Attenuation	115	dB
12.288 MHz Master Clock[4]		
Passband Edge	21.7	kHz
Stopband Edge	26.2	kHz
11.2896 MHz Clock[5]		
Passband Edge	20	kHz
Stopband Edge	24.1	kHz
DIGITAL INPUTS AND OUTPUTS		
V_{IH}	2.0	V
V_{IL}	0.8	V
I_{IH} @ V_{IH} = 5 V	10	μA
I_{IL} @ V_{IL} = 0 V	10	μA
V_{OH} @ I_{OH} = 4 mA	4.5	V
V_{OL} @ I_{OL} = 4 mA	0.5	V
NOMINAL MASTER CLOCK FREQUENCY	12.288	MHz
POWER SUPPLIES		
Voltage, $+V_L$ and $+V_S$	5	V
Voltage, $-V_L$ and $-V_S$	−5	V
Current, $+I_L$ and $+I_S$	TBD	mA
Current, $-I_L$ and $-I_S$	TBD	mA
POWER DISSIPATION		
Operation	900	mW
Power Down APD = "1"	400	mW
POWER SUPPLY REJECTION RATIO	67	dB
TEMPERATURE RANGE		
Specification	25	°C
Operation	−25 to +70	°C
Storage	−60 to +100	°C

NOTES
[1]Stereo mode uses output of each channel independently.
[2]Mono mode sums output words to derive higher dynamic range.
[3]16-bit LSBs.
[4]Master Clock Frequency for 48 kHz sample rate.
[5]Master Clock Frequency for 44.1 kHz sample rate.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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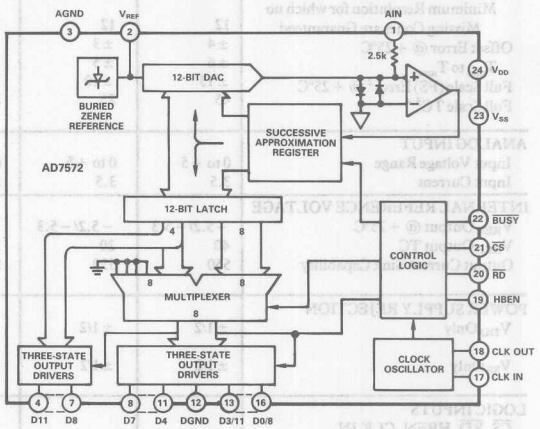
LC²MOS Complete, High Speed 12-Bit ADC

AD7572

FEATURES

- 12-Bit Resolution and Accuracy
- Fast Conversion Time
  - AD7572XX05: 5μs
  - AD7572XX12: 12.5μs
- Complete with On-Chip Reference
- Fast Bus Access Time: 90ns
- Low Power: 135mW
- Small, 0.3", 24-Pin Package and 28-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7572 is a complete, 12-bit ADC that offers high speed performance combined with low, CMOS power levels. The AD7572 uses an accurate, high speed DAC and comparator in a successive-approximation loop to achieve a fast conversion time. An on-chip, buried Zener diode provides a stable reference voltage to give low drift performance over the full temperature range and the specified accuracy is achieved without any user trims. An on-chip clock circuit is provided, which may be used with a crystal for stand-alone operation, or the clock input may be driven from an external clock source such as a divided-down microprocessor clock. The only other external components required for basic operation of the AD7572 are decoupling capacitors for the supply voltages and reference output.

The AD7572 has a high speed digital interface with three-state data outputs and can operate under the control of standard microprocessor Read ($\overline{RD}$) and decoded address ($\overline{CS}$) signals. Interface timing is sufficiently fast to allow the AD7572 to operate with most popular microprocessors, with three-state enable times of only 90ns and bus relinquish times of 75ns.

The AD7572 is fabricated in Analog Devices Linear Compatible CMOS process (LC²MOS), an advanced, all ion-implanted process that combines fast CMOS logic and linear, bipolar circuits on a single chip, thus achieving excellent linear performance while still retaining low CMOS power levels.

The AD7572 is available in both 0.3" wide , 24-pin DIPs and in a 28-terminal plastic leaded chip carrier (PLCC) and leadless ceramic chip carrier (LCCC).

PRODUCT HIGHLIGHTS

1. Fast, 5μs and 12.5μs conversion times make the AD7572 ideal for a wide range of applications in telecommunications, sonar and radar signal processing or any wideband data acquisition system.
2. On-chip buried-Zener reference has temperature coefficient as low as 25ppm/°C, giving low full-scale drift over the operating temperature range.
3. Stable DAC and comparator give excellent linearity and low zero error over the full temperature range.
4. Fast, easy-to-use digital interface has three-state bus access times of 90ns and bus relinquish times of 75ns, allowing the AD7572 to interface to most popular microprocessors.
5. LC²MOS circuitry gives low power drain (135mW) from +5, −15 volt supplies.
6. 24-pin 0.3" package offers space saving over parts in 28-pin 0.6" DIP.

AD7572—SPECIFICATIONS

(V_{DD} = 5V ± 5%, V_{SS} = −15V ± 5%, f_{CLK}: 2.5MHz for AD7572XX05, 1MHz for AD7572XX12. All Specifications T_{min} to T_{max} unless otherwise noted. Specifications apply to Slow Memory Mode.)

Parameter	J, A, S Versions[1]	K, B, T Versions	L Version	C, U Versions	Units	Test Conditions/Comments
ACCURACY						
Resolution	12	12	12	12	Bits	
Integral Nonlinearity @ +25°C	±1	±1	±1/2	±1/2	LSB max	
T_{min} to T_{max}	±1	±1	±1/2	±3/4	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	
Minimum Resolution for which no Missing Codes are Guaranteed	12	12	12	12	Bits	
Offset Error @ +25°C	±4	±3	±3	±3	LSB max	
T_{min} to T_{max}	±6	±5	±4	±4	LSB max	Typical Change over Temp Is ±1LSB
Full Scale (FS) Error[2] @ +25°C	±15	±10	±10	±10	LSB max	V_{DD} = 5V; V_{SS} = −15V; FS = 5V
Full Scale TC[3,4]	45	25	25	25	ppm/°C max	Ideal Last Code Transition = FS − 3/2LSBs
ANALOG INPUT						
Input Voltage Range	0 to +5	0 to +5	0 to +5	0 to +5	Volts	For Bipolar Operation See
Input Current	3.5	3.5	3.5	3.5	mA max	Figures 10 & 12
INTERNAL REFERENCE VOLTAGE						
V_{REF} Output @ +25°C	−5.2/−5.3	−5.2/−5.3	−5.2/−5.3	−5.2/−5.3	V min/V max	−5.25V ±1%
V_{REF} Output TC	40	20	20	20	ppm/°C typ	
Output Current Sink Capability	550	550	550	550	µA max	External Load Should Not Change During Conversion
POWER SUPPLY REJECTION						
V_{DD} Only	±1/2	±1/2	±1/2	±1/2	LSB typ	FS Change, V_{SS} = −15V V_{DD} = +4.75V to +5.25V
V_{SS} Only	±1/2	±1/2	±1/2	±1/2	LSB typ	FS Change, V_{DD} = 5V V_{SS} = −14.25V to −15.75V
LOGIC INPUTS						
$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN						
V_{INL}, Input Low Voltage	+0.8	+0.8	+0.8	+0.8	V max	V_{DD} = 5V ±5%
V_{INH}, Input High Voltage	+2.4	+2.4	+2.4	+2.4	V min	
C_{IN},[5] Input Capacitance	10	10	10	10	pF max	
$\overline{CS}$, $\overline{RD}$, HBEN						
I_{IN}, Input Current	±10	±10	±10	±10	µA max	V_{IN} = 0 to V_{DD}
CLK IN						
I_{IN}, Input Current	±20	±20	±20	±20	µA max	V_{IN} = 0 to V_{DD}
LOGIC OUTPUTS						
D11–D0/8, $\overline{BUSY}$, CLK OUT						
V_{OL}, Output Low Voltage	+0.4	+0.4	+0.4	+0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	+4.0	+4.0	+4.0	+4.0	V min	I_{SOURCE} = 200µA
D11–D0/8						
Floating State Leakage Current	±10	±10	±10	±10	µA max	
Floating State Output Capacitance[5]	15	15	15	15	pF max	
CONVERSION TIME						
AD7572XX05						
Synchronous Clock	5	5	5	5	µs max	f_{CLK} = 2.5MHz. See Under
Asynchronous Clock	4.8/5.2	4.8/5.2	4.8/5.2	4.8/5.2	µs min/max	Control Inputs Synchronization
AD7572XX12						
Synchronous Clock	12.5	12.5	12.5	12.5	µs max	f_{CLK} = 1MHz
Asynchronous Clock	12/13	12/13	12/13	12/13	µs min/µs max	
POWER REQUIREMENTS						
V_{DD}	+5	+5	+5	+5	V NOM	±5% for Specified Performance
V_{SS}	−15	−15	−15	−15	V NOM	±5% for Specified Performance
I_{DD}[6]	7	7	7	7	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V
I_{SS}[6]	12	12	12	12	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V
Power Dissipation	135	135	135	135	mW typ	
	215	215	215	215	mW max	

NOTES

[1]Temperature range as follows: J, K, L Versions; 0 to +70°C.
A, B, C Versions; −25°C to +85°C.
S, T, U Versions; −55°C to +125°C.

[2]Includes internal voltage reference error.

[3]Full-Scale TC = ΔFS/ΔT, where ΔFS is Full-Scale change from T_A = +25°C to T_{min} or T_{max}.

[4]Includes internal voltage reference drift.

[5]Sample tested to ensure compliance.

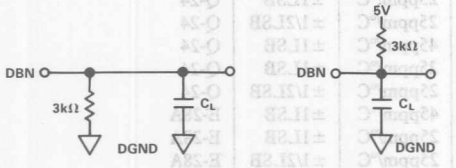
[6]Power supply current is measured when AD7572 is inactive, i.e., $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = HIGH.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = 5V, V_{SS} −15V)

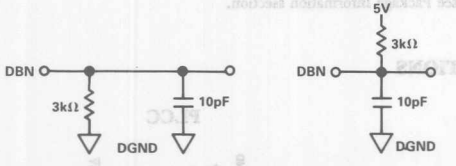
Parameter	Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (J, K, L, A, B, C Grades)	Limit at T_{min}, T_{max} (S, T, U Grades)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_2	190	230	270	ns max	$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay
t_3[2]	90	110	120	ns max	Data Access Time after $\overline{RD}$, C_L = 20pF
	125	150	170	ns max	Data Access Time after $\overline{RD}$, C_L = 100pF
t_4	t_3	t_3	t_3	ns min	$\overline{RD}$ Pulse Width
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6[2]	70	90	100	ns max	Data Setup Time after $\overline{BUSY}$
t_7[3]	20	20	20	ns min	Bus Relinquish Time
	75	85	90	ns max	
t_8	0	0	0	ns min	HBEN to $\overline{RD}$ Setup Time
t_9	0	0	0	ns min	HBEN to $\overline{RD}$ Hold Time
t_{10}	200	200	200	ns min	Delay Between Successive Read Operations

NOTES
[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[3]t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.



a. High-Z to V_{OH} (t_3) and V_{OL} to V_{OH} (t_6) *b. High-Z to V_{OL} (t_3) and V_{OH} to V_{OL} (t_6)*

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 2. Load Circuits for Output Float Delay

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND	−0.3V to +7V
V_{SS} to DGND	+0.3V to −17V
AGND to DGND	−0.3V, V_{DD} + 0.3V
AIN to AGND	−15V to +15V
Digital Input Voltage to DGND (CLK IN, HBEN, $\overline{RD}$, $\overline{CS}$)	−0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND (D11–D0/8, CLK OUT, $\overline{BUSY}$)	−0.3V, V_{DD} +0.3V
Operating Temperature Range	
Commercial (J, K, L Versions)	0 to +70°C
Industrial (A, B, C Versions)	−25°C to +85°C
Extended (S, T, U Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C
Power Dissipation (Any Package) to +75°C	1,000mW
Derates above +75°C by	10mW/°C

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



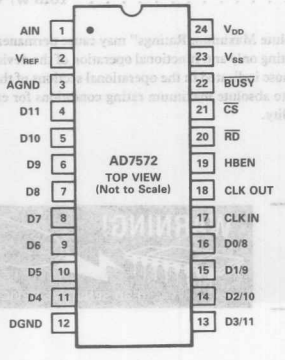
ORDERING GUIDE[1]

Model[2]	Conversion Time	Temperature Range	Full-Scale TC	Accuracy Grade	Package Option[3]
AD7572JN05	5µs	0 to +70°C	45ppm/°C	±1LSB	N-24
AD7572KN05	5µs	0 to +70°C	25ppm/°C	±1LSB	N-24
AD7572LN05	5µs	0 to +70°C	25ppm/°C	±1/2LSB	N-24
AD7572JP05	5µs	0 to +70°C	45ppm/°C	±1LSB	P-28A
AD7572KP05	5µs	0 to +70°C	25ppm/°C	±1LSB	P-28A
AD7572LP05	5µs	0 to +70°C	25ppm/°C	±1/2LSB	P-28A
AD7572AQ05	5µs	−25°C to +85°C	45ppm/°C	±1LSB	Q-24
AD7572BQ05	5µs	−25°C to +85°C	25ppm/°C	±1LSB	Q-24
AD7572CQ05	5µs	−25°C to +85°C	25ppm/°C	±1/2LSB	Q-24
AD7572SQ05	5µs	−55°C to +125°C	45ppm/°C	±1LSB	Q-24
AD7572TQ05	5µs	−55°C to +125°C	25ppm/°C	±1LSB	Q-24
AD7572UQ05	5µs	−55°C to +125°C	25ppm/°C	±1/2LSB	Q-24
AD7572SE05	5µs	−55°C to +125°C	45ppm/°C	±1LSB	E-28A
AD7572TE05	5µs	−55°C to +125°C	25ppm/°C	±1LSB	E-28A
AD7572UE05	5µs	−55°C to +125°C	25ppm/°C	±1/2LSB	E-28A
AD7572JN12	12.5µs	0 to +70°C	45ppm/°C	±1LSB	N-24
AD7572KN12	12.5µs	0 to +70°C	25ppm/°C	±1LSB	N-24
AD7572LN12	12.5µs	0 to +70°C	25ppm/°C	±1/2LSB	N-24
AD7572JP12	12.5µs	0 to +70°C	45ppm/°C	±1LSB	P-28A
AD7572KP12	12.5µs	0 to +70°C	25ppm/°C	±1LSB	P-28A
AD7572LP12	12.5µs	0 to +70°C	25ppm/°C	±1/2LSB	P-28A
AD7572AQ12	12.5µs	−25°C to +85°C	45ppm/°C	±1LSB	Q-24
AD7572BQ12	12.5µs	−25°C to +85°C	25ppm/°C	±1LSB	Q-24
AD7572CQ12	12.5µs	−25°C to +85°C	25ppm/°C	±1/2LSB	Q-24
AD7572SQ12	12.5µs	−55°C to +125°C	45ppm/°C	±1LSB	Q-24
AD7572TQ12	12.5µs	−55°C to +125°C	25ppm/°C	±1LSB	Q-24
AD7572UQ12	12.5µs	−55°C to +125°C	25ppm/°C	±1/2LSB	Q-24
AD7572SE12	12.5µs	−55°C to +125°C	45ppm/°C	±1LSB	E-28A
AD7572TE12	12.5µs	−55°C to +125°C	25ppm/°C	±1LSB	E-28A
AD7572UE12	12.5µs	−55°C to +125°C	25ppm/°C	±1/2LSB	E-28A

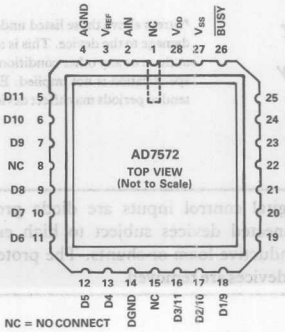
NOTES
[1]Analog Devices Reserves the right to ship ceramic (D-24A) in lieu cerdip (Q-24) hermetic package.
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD) see DESC Drawing #5962-87591.
[3]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information ssection.

PIN CONFIGURATIONS

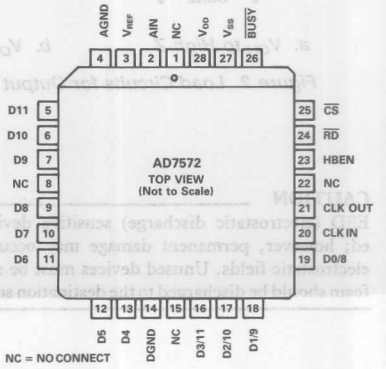
DIP



LCCC



PLCC



LC²MOS Complete, High Speed 12-Bit ADC

AD7572A

FEATURES

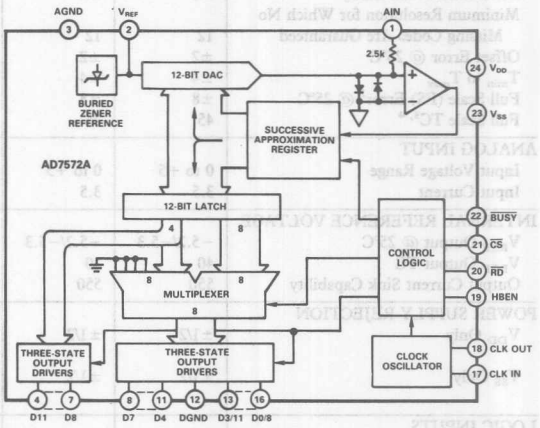
Improved AD7572
- **Faster Conversion Time**
  - **AD7572AXX03: 3 μs**
  - **AD7572AXX10: 10 μs**
- **5 V and −12 V or −15 V Power Supply Operation**
- **Better Offset and Gain Error Specifications**

Extended Plastic Temperature Range (−40°C to +85°C)

Low Power: 100 mW

Small 24-Pin, 0.3″ Wide DIP and SOIC DIP Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7572A is an enhanced replacement for the industry standard AD7572. Improvements include faster conversion times of 3 μs for the AD7572AXX03 and 10 μs for the AD7572AXX10. The required power supplies are 5 V and −12 V or −15 V. Additional features are better offset and gain error specifications over the original AD7572.

The AD7572A is a complete 12-bit ADC that offers high speed performance combined with low, CMOS power levels. The part uses an accurate, high speed DAC and comparator in a successive-approximation loop to achieve a fast conversion time. An on-chip buried Zener diode provides a stable reference voltage to give low drift performance over the full temperature range and the specified accuracy is achieved without any user trims. An on-chip clock circuit is provided, which may be used with a crystal for stand-alone operation, or the clock input may be driven from an external clock source such as a divided-down microprocessor clock. The only other external components required for basic operation of the AD7572A are decoupling capacitors for the supply voltages and reference output.

The AD7572A has a high speed digital interface with three-state data outputs and can operate under the control of standard microprocessor Read ($\overline{RD}$) and decoded address ($\overline{CS}$) signals. Interface timing is sufficiently fast to allow the AD7572A to operate with most microprocessors, with three-state enable times of only 90 ns and bus relinquish times of 75 ns.

The AD7572A is fabricated in Analog Devices Linear Compatible CMOS process (LC²MOS), an advanced all ion-implanted process that combines fast CMOS logic and linear, bipolar circuits on a single chip, thus achieving excellent linear performance while retaining low CMOS power levels.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time
   Fast, 3 μs and 10 μs conversion times make the AD7572A ideal for DSP applications and wideband data acquisition systems.
2. Wide Power Supply Range
   The AD7572A operates from 5 V and −12 V or −15 V power supplies.
3. Microprocessor Interface
   Fast, easy-to-use digital interface has three-state bus access times of 90 ns and bus relinquish times of 75 ns allowing the AD7572A to interface to most microprocessors.
4. Low Power
   LC²MOS circuitry gives low power drain (100 mW) from +5, −12 volt supplies.
5. 24-pin 0.3″ DIP and SOIC packages offer space saving over parts in 28-pin 0.6″ DIP.

Parameter	J, A Versions[1]	L Version[1]	S Version[1]	Units	Test Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Integral Nonlinearity @ 25°C	±1	±1/2	±1	LSB max	
T_{min} to T_{max}	±1	±1/2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	LSB max	
Minimum Resolution for Which No Missing Codes Are Guaranteed	12	12	12	Bits	
Offset Error @ 25°C	±2	±2	±2	LSB max	
T_{min} to T_{max}	±4	±4	±4	LSB max	Typical Change over Temp is ±1 LSB
Full Scale (FS) Error[2] @ 25°C	±8	±8	±8	LSB max	FS = 5 V
Full Scale TC[3, 4]	45	25	45	ppm/°C max	Ideal Last Code Transition = FS −3/2 LSBs
ANALOG INPUT					
Input Voltage Range	0 to +5	0 to +5	0 to +5	Volts	For Bipolar Operation See Figures 10
Input Current	3.5	3.5	3.5	mA max	and 12
INTERNAL REFERENCE VOLTAGE					
V_{REF} Output @ 25°C	−5.2/−5.3	−5.2/−5.3	−5.2/−5.3	V min/V max	−5.25 V ±1%
V_{REF} Output TC	40	20	40	ppm/°C typ	External Load Should Not
Output Current Sink Capability	550	550	550	µA max	Change During Conversion
POWER SUPPLY REJECTION					
V_{DD} Only	±1/2	±1/2	±1/2	LSB typ	FS Change, V_{SS} = −12 V or −15 V V_{DD} = 4.5 V to 5.5 V
V_{SS} Only	±1/2	±1/2	±1/2	LSB typ	FS Change, V_{DD} = 5 V V_{SS} = −11.4 V to −16.5 V
LOGIC INPUTS					
$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN					
V_{INL}, Input Low Voltage	+0.8	+0.8	+0.8	V max	V_{DD} = 5 V ±5%
V_{INH}, Input High Voltage	+2.4	+2.4	+2.4	V min	
C_{IN}, Input Capacitance[5]	10	10	10	pF max	
$\overline{CS}$, $\overline{RD}$, HBEN					
I_{IN}, Input Current	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
CLK IN					
I_{IN}, Input Current	±20	±20	±20	µA max	V_{IN} = 0 V to V_{DD}
LOGIC OUTPUTS					
D11–D0/8, $\overline{BUSY}$, CLK OUT					
V_{OL}, Output Low Voltage	+0.4	+0.4	+0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	+4.0	+4.0	+4.0	V min	I_{SOURCE} = 200 µA
D11–D0/8					
Floating-State Leakage Current	±10	±10	±10	µA max	
Floating-State Output Capacitance[5]	15	15	15	pF max	
CONVERSION TIME					
AD7572AXX03					
Synchronous Clock	3.125	3.125	3.125	µs max	f_{CLK} = 4 MHz. See Under
Asynchronous Clock	3/3.25	3/3.25	3/3.25	µs min/µs max	Control Inputs Synchronization
AD7572AXX10					
Synchronous Clock	10	10	–	µs max	f_{CLK} = 1.25 MHz
Asynchronous Clock	9.6/10.4	9.6/10.4	–	µs min/µs max	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−12 to −15	−12 to −15	−12 to −15	V nom	−11.4 V to −16.5 V for Specified Performance
I_{DD}[6]	4	4	7	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5 V
I_{SS}[6]	9	9	12	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5 V
Power Dissipation	100	100	120	mW typ	V_{SS} = −12 V
	128/155	128/155	179/215	mW max	V_{SS} = −12 V/−15 V

NOTES

[1]Temperature ranges are as follows: J, L Versions, 0 to +70°C; A Version, −40°C to +85°C; S Version, −55°C to +125°C.

[2]Includes internal voltage reference error.

[3]Full-Scale TC = ΔFS/ΔT where ΔFS is Full-Scale change from T_A = +25°C to T_{min} or T_{max}.

[4]Includes internal voltage reference drift.

[5]Sample tested to ensure compliance.

[6]Power supply current is measured when the AD7572A is inactive, i.e., $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = HIGH.

Specifications subject to change without notice.

TIMING CHARACTERISTICS (V_{DD} = 5 V ± 5%, V_{SS} = −11.4 V to −16.5 V)

Parameter	Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (J, L, A Grades)	Limit at T_{min}, T_{max} (S Grade)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_2	190	230	270	ns max	$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay
t_3[2]	90	110	120	ns max	Data Access Time after $\overline{RD}$, C_L=20 pF
	125	150	170	ns max	Data Access Time after $\overline{RD}$, C_L=100 pF
t_4	t_3	t_3	t_3	ns min	$\overline{RD}$ Pulse Width
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6[2]	70	90	100	ns max	Data Setup Time after $\overline{BUSY}$
t_7[3]	15	15	15	ns min	Bus Relinquish Time
	75	85	90	ns max	
t_8	0	0	0	ns min	HBEN to $\overline{RD}$ Setup Time
t_9	0	0	0	ns min	HBEN to $\overline{RD}$ Hold Time
t_{10}	200	200	200	ns min	Delay Between Successive Read Operations

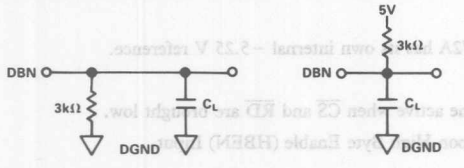
NOTE

[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[2]t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

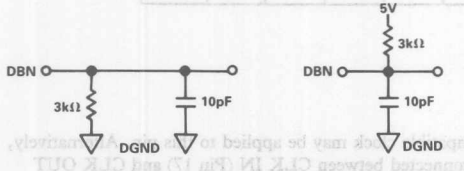
[3]t_7 is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.

Specifications subject to change without notice.



a. High-Z to V_{OH} (t_3) and V_{OL} to V_{OH} (t_6) *b. High-Z to V_{OL} (t_3) and V_{OH} to V_{OL} (t_6)*

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 2. Load Circuits for Output Float Delay

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND . . . . . −0.3 V to +7 V
V_{SS} to DGND . . . . . +0.3 V to −17 V
AGND to DGND . . . . . −0.3 V, V_{DD} + 0.3 V
AIN to AGND . . . . . −15 V to +15 V
Digital Input Voltage to DGND
(CLK IN, HBEN, $\overline{RD}$, $\overline{CS}$) . . . . . −0.3 V, V_{DD} +0.3 V
Digital Output Voltage to DGND
(D11-D0/8, CLK OUT, $\overline{BUSY}$) . . . . . −0.3 V, V_{DD} +0.3 V
Operating Temperature Range
Commercial (J, L Versions) . . . . . 0 to +70°C
Industrial (A Version) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1,000 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

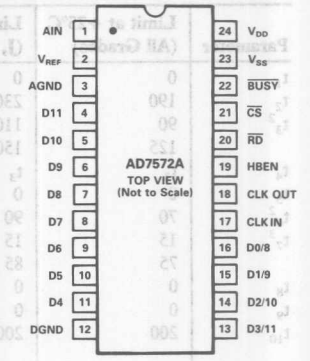


ORDERING GUIDE

Model	Conversion Time	Temperature Range	Full-Scale TC	Accuracy Grade	Package Option[1]
AD7572AJN03	3 µs	0°C to +70°C	45 ppm/°C	±1 LSB	N-24
AD7572AAN03	3 µs	−40°C to +85°C	45 ppm/°C	±1 LSB	N-24
AD7572ASQ03[2]	3 µs	−55°C to +125°C	45 ppm/°C	±1 LSB	Q-24
AD7572ALN03	3 µs	0°C to +70°C	25ppm/°C	±1/2 LSB	N-24
AD7572AAQ03	3 µs	−40°C to +85°C	45 ppm/°C	±1 LSB	Q-24
AD7572AJR03	3 µs	0°C to +70°C	45 ppm/°C	±1 LSB	R-24
AD7572AAR03	3 µs	−40°C to +85°C	45 ppm/°C	±1 LSB	R-24
AD7572AJN10	10 µs	0°C to +70°C	45 ppm/°C	±1 LSB	N-24
AD7572AAN10	10 µs	−40°C to +85°C	45 ppm/°C	±1 LSB	N-24
AD7572ALN10	10 µs	0°C to +70°C	25 ppm/°C	±1/2 LSB	N-24
AD7572AJR10	10 µs	0°C to +70°C	45 ppm/°C	±1 LSB	R-24

NOTES
[1]N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.
[2]AD7572ASQ03 will be available to /883B processing only. Contact your local sales office for release information.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Description
1	AIN	Analog Input.
2	V_{REF}	Voltage Reference Output. The AD7572A has its own internal −5.25 V reference.
3	AGND	Analog Ground.
4 . . . 11	D11 . . . D4	Three State Data Outputs. They become active when $\overline{CS}$ and $\overline{RD}$ are brought low.
13 . . . 16	D3/11 . . . D0/8	Individual pin function is dependent upon High Byte Enable (HBEN) Input.

DATA BUS OUTPUT, $\overline{CS}$ & $\overline{RD}$ = LOW

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = LOW	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = HIGH	DB11	DB10	DB9	DB8	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

NOTES
*D11 . . . D0/8 are the ADC data output pins.
DB11 . . . DB0 are the 12-bit conversion results, DB11 is the MSB.

12	DGND	Digital Ground.
17	CLK IN	Clock Input Pin. An external TTL compatible clock may be applied to this pin. Alternatively, a crystal or ceramic resonator may be connected between CLK IN (Pin 17) and CLK OUT (Pin 18).
18	CLK OUT	Clock Output Pin. An inverted CLK IN signal appears at CLK OUT when an external clock is used. See CLK IN (Pin 17) description for crystal (resonator).
19	HBEN	High Byte Enable Input. Its primary function is to multiplex the 12 bits of conversion data onto the lower D7 . . . D0/8 outputs (4 MSBs or 8 LSBs). See Pin Description 4 . . . 11 and 13 . . . 16. It also disables conversion start when HBEN is high.
20	$\overline{RD}$	READ Input. This active LOW signal, in conjunction with $\overline{CS}$, is used to enable the output data three-state drivers and initiate a conversion if $\overline{CS}$ and HBEN are low.
21	$\overline{CS}$	CHIP SELECT Input. This active LOW signal, in conjunction with $\overline{RD}$ is used to enable the output data three-state drivers and initiate a conversion if $\overline{RD}$ and HBEN are low.
22	$\overline{BUSY}$	$\overline{BUSY}$ Output indicates converter status. $\overline{BUSY}$ is LOW during conversion.
23	V_{SS}	Negative Supply, −12 V to −15 V.
24	V_{DD}	Positive Supply, +5 V.

OPERATIONAL DIAGRAM

An operational diagram for the AD7572A is shown in Figure 3. The AD7572A is a 12-bit successive approximation A/D converter. The addition of just a crystal/ceramic resonator and a few capacitors enables the device to perform the analog-to-digital function.

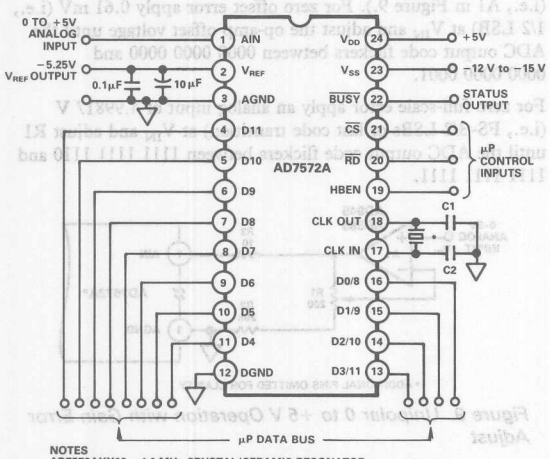


Figure 3. AD7572A Operational Diagram

CONVERTER DETAILS

Conversion start is controlled by the $\overline{CS}$, $\overline{RD}$ and HBEN inputs. At the start of conversion the successive approximation register (SAR) is reset and the three-state data outputs are enabled. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit voltage mode DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 4, the AIN input connects to the comparator input via 2.5 kΩ.

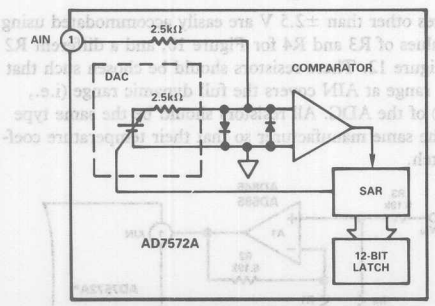


Figure 4. AD7572A AIN Input

The DAC which has a similar 2.5 kΩ output impedance connects to the same comparator input. Bit decisions are made by the comparator (zero crossing detector) which checks the addition of each successive weighted bit from the DAC output. The MSB decision is made 80 ns (typically) after the second falling edge of CLK IN following a conversion start. Similarly, the succeeding bit decisions are made approximately 80 ns after a CLK IN edge until conversion is finished. At the end of conversion, the DAC output current balances the AIN input current. The SAR contents (12-bit data word) which represent the AIN input signal is loaded into a 12-bit latch.

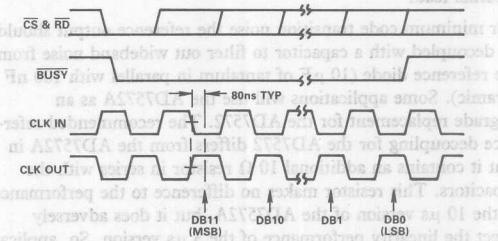


Figure 5. Operating Waveforms Using an External Clock Source for CLK IN

CONTROL INPUTS SYNCHRONIZATION

In applications where the $\overline{RD}$ control input is not synchronized with the ADC clock then conversion time can vary from 12 to 13 CLK IN periods. This is because the ADC waits for the first falling CLK IN edge after conversion start before the conversion procedure begins. Without synchronization, this delay can vary from zero to an entire clock period. If a constant conversion time is required, then the following approach ensures a fixed 3.125 µs conversion time for the AD7572AXX03 and 10 µs for the AD7572AXX10: when initiating a conversion, $\overline{RD}$ must go low on either the rising edge of CLK IN or the falling edge of CLK OUT.

DRIVING THE ANALOG INPUT

During conversion, the AIN input current is modulated by the DAC output current at a rate equal to the CLK IN frequency (i.e., 4 MHz when CLK IN = 4 MHz). The analog input voltage must remain fixed during this period and as a result must be driven from an op amp or sample-and-hold with a low output impedance. The output impedance of an op amp is equal to the open loop output impedance divided by the loop gain at the frequency of interest.

Suitable devices capable of driving the AD7572A AIN input are the AD845 op amp or the AD585 sample-and-hold.

INTERNAL CLOCK OSCILLATOR

Figure 6 shows the AD7572A internal clock circuit. A crystal or ceramic resonator may be connected between CLK IN (Pin 17) and CLK OUT (Pin 18) to provide a clock oscillator for the ADC timing. Alternatively the crystal/resonator may be omitted and an external clock source may be connected to CLK IN. For an external clock the mark/space ratio can vary from 45/55 to 55/45. An inverted CLK IN signal will appear at the CLK OUT pin as shown in the operating waveforms of Figure 5.

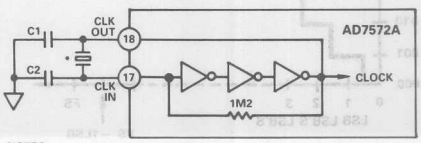


Figure 6. AD7572A Internal Clock Circuit

INTERNAL REFERENCE

The AD7572A has an on-chip, buffered, temperature-compensated, buried Zener reference, which is factory trimmed to −5.25 V ±1%. It is internally connected to the DAC and is also available at Pin 2 to provide up to 550 μA current to an external load.

For minimum code transition noise the reference output should be decoupled with a capacitor to filter out wideband noise from the reference diode (10 μF of tantalum in parallel with 100 nF ceramic). Some applications will use the AD7572A as an upgrade replacement for the AD7572. The recommended reference decoupling for the AD7572 differs from the AD7572A in that it contains an additional 10 Ω resistor in series with the capacitors. This resistor makes no difference to the performance of the 10 μs version of the AD7572A, but it does adversely affect the linearity performance of the 3 μs version. So, applications using the AD7572A as a 3 μs upgrade of the AD7572 must replace the 10 Ω reference resistor with a wire link.

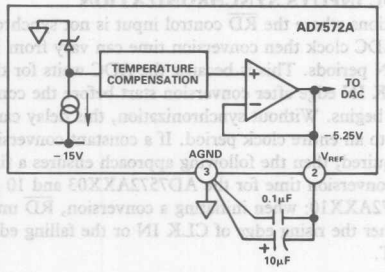


Figure 7. AD7572A Internal −5.25 V Reference

UNIPOLAR OPERATION

Figure 8 shows the ideal input/output characteristic for the 0 to 5 volt input range of the AD7572A. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS–3/2 LSBs). The output code is natural binary with 1 LSB = FS/4096 = (5/4096) V = 1.22 mV.

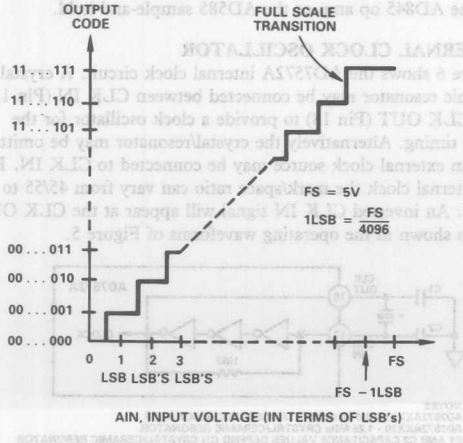


Figure 8. AD7572A Ideal Input/Output Transfer Characteristic

UNIPOLAR OFFSET AND FULL-SCALE ERROR ADJUSTMENT

In applications where absolute accuracy is important then offset and full-scale error can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 9 shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset of the op amp driving AIN (i.e., A1 in Figure 9.). For zero offset error apply 0.61 mV (i.e., 1/2 LSB) at V_{IN} and adjust the op-amp offset voltage until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

For zero full-scale error apply an analog input of 4.99817 V (i.e., FS–3/2 LSBs or last code transition) at V_{IN} and adjust R1 until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

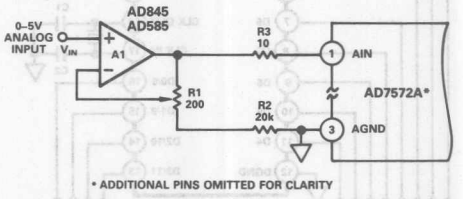


Figure 9. Unipolar 0 to +5 V Operation with Gain Error Adjust

BIPOLAR OPERATION

Figures 10 and 12 show how bipolar operation can be achieved with the AD7572A. Both circuits use an op amp to offset the analog signal (V_{IN}) by 2.5 V. Alternatively, the op amp (A1) can be replaced by a sample hold as shown in Figure 24. The op amp transfer functions are given below:

Figure 10: AIN = (V_{IN} + 2.5) volts
Figure 12: AIN = (−V_{IN} + 2.5) volts

Both circuits have an analog input range of ±2.5 V and an LSB size of 1.22 mV. The output codes are offset binary for Figure 10 and complementary offset binary for Figure 12. Their ideal input/output transfer characteristics after offset and full-scale adjustment are shown in Figures 11 and 13.

Signal ranges other than ±2.5 V are easily accommodated using different values of R3 and R4 for Figure 10, and a different R2 value for Figure 12. These resistors should be chosen such that the voltage range at AIN covers the full dynamic range (i.e., 0 V to 5 V) of the ADC. All resistors should be the same type and from the same manufacturer so that their temperature coefficients match.

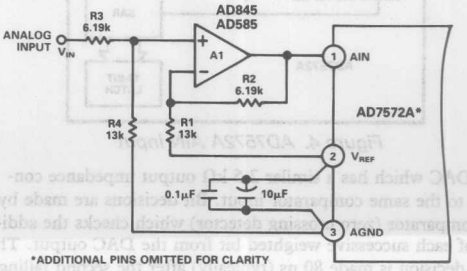


Figure 10. AD7572A Bipolar Operation – Output Code is Offset Binary

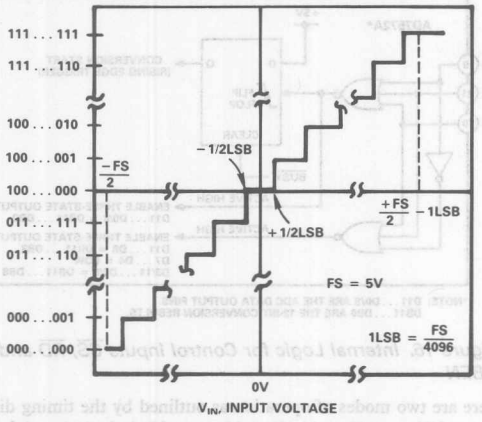


Figure 11. Ideal Input/Output Transfer Characteristic for the Bipolar Circuit of Figure 10

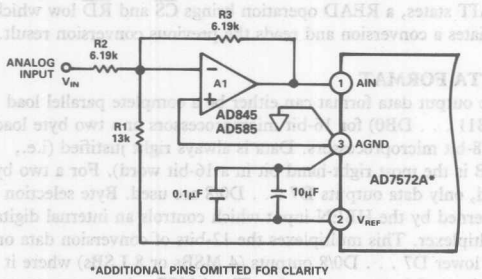


Figure 12. AD7572A Bipolar Operation - Output Code is Complementary Offset Binary

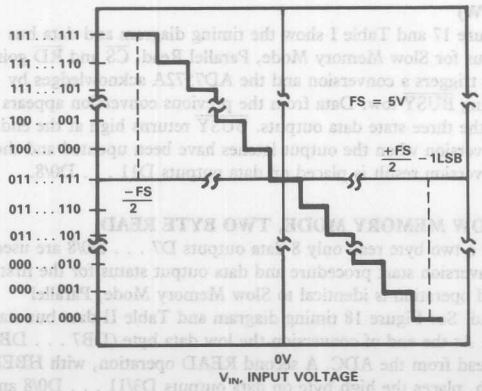


Figure 13. Ideal Input/Output Transfer Characteristic for the Bipolar Circuit of Figure 12

OFFSET AND FULL-SCALE ERROR

In most Digital Signal Processing (DSP) applications offset and full-scale error have little or no effect on system performance. A typical example is a digital filter, where an analog signal is quantized, digitally processed and recreated using a DAC. In these types of applications the offset error can be eliminated by ac coupling the recreated signal. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. An important parameter in DSP applications is Differential Nonlinearity and this is not affected by either offset or full-scale error.

In measurement applications where absolute accuracy is required, offset and full-scale error can be adjusted to zero as in Figure 14.

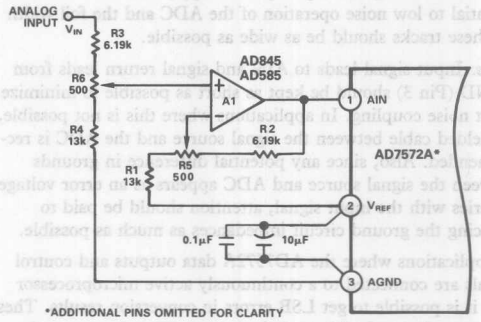


Figure 14. AD7572A Bipolar Operation with Offset and Gain Error Adjust

BIPOLAR OFFSET AND FULL-SCALE ERROR ADJUSTMENT

The bipolar circuit of Figure 10 can be adjusted for offset and full-scale errors, by including two potentiometers R5 and R6, as shown in Figure 14. Offset must be adjusted before full-scale error. This is achieved by applying an analog input of 0.61 mV (1/2 LSB) at V_{IN} and adjusting R5 until the ADC output code flickers between 1000 0000 0000 and 1000 0000 0001.

For full-scale error adjustment, the analog input must be at 2.49817 volts (i.e., FS/2 –3/2 LSBs or last transition point). Then R6 is adjusted until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

A similar offset and full-scale error adjustment procedure may be employed for Figure 12 by making R1 and R2 variable. Offset must again be adjusted before full scale error. This is achieved by applying an analog input of 0.61 mV at V_{IN} and adjusting R1 until the ADC output code flickers between 0111 1111 1110 and 0111 1111 1111.

For full-scale error adjustment, apply a signal source of 2.49817 V at V_{IN} and adjust R2 until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

APPLICATION HINTS

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the AD7572A a printed circuit board is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the AD7572A. The analog input should be screened by AGND.

A single point analog ground (STAR ground) separate from the logic system ground should be established at Pin 3 (AGND) or as close as possible to the AD7572A as shown in Figure 15. Pin 12 (AD7572A DGND) and all other analog grounds should be connected to this single analog ground point. No other digital grounds should be connected to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible.

Noise: Input signal leads to AIN and signal return leads from AGND (Pin 3) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible, a shielded cable between the signal source and the ADC is recommended. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

In applications where the AD7572A data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get LSB errors in conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion (see Slow Memory Mode interfacing), or by using three-state buffers to isolate the AD7572A data bus.

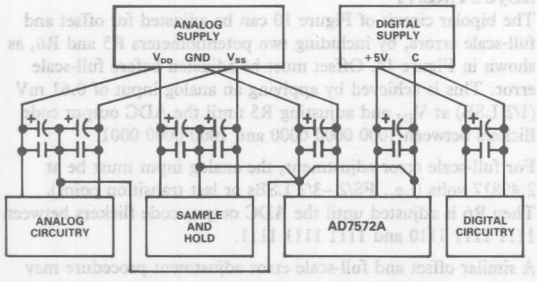


Figure 15. Power Supply Grounding Practice

TIMING AND CONTROL

Conversion start and data read operations are controlled by three AD7572A digital inputs; HBEN, $\overline{CS}$ and $\overline{RD}$. Figure 16 shows the logic structure associated with these inputs. The three signals are internally gated so that a logic "0" is required on all three inputs to initiate a conversion. Once initiated it cannot be restarted until conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output, and this is low while conversion is in progress.

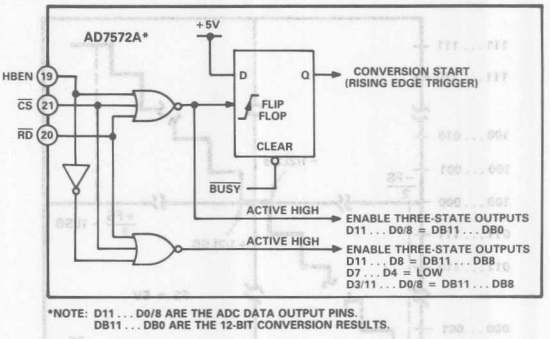


Figure 16. Internal Logic for Control Inputs $\overline{CS}$, $\overline{RD}$ and HBEN

There are two modes of operation as outlined by the timing diagrams of Figures 17 to 20. Slow Memory Mode is designed for microprocessors which can be driven into a WAIT state, a READ operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and data is read when conversion is complete. The second is the ROM Mode which does not require microprocessor WAIT states, a READ operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and reads the previous conversion result.

DATA FORMAT

The output data format can either be a complete parallel load (DB11 . . . DB0) for 16-bit microprocessors or a two byte load for 8-bit microprocessors. Data is always right justified (i.e., LSB is the most right-hand bit in a 16-bit word). For a two byte read, only data outputs D7 . . . D0/8 are used. Byte selection is governed by the HBEN input which controls an internal digital multiplexer. This multiplexes the 12-bits of conversion data onto the lower D7 . . . D0/8 outputs (4 MSBs or 8 LSBs) where it can be read in two read cycles. The 4 MSBs always appear on D11 . . . D8 whenever the three-state output drivers are turned on.

SLOW MEMORY MODE, PARALLEL READ (HBEN = LOW)

Figure 17 and Table I show the timing diagram and data bus status for Slow Memory Mode, Parallel Read. $\overline{CS}$ and $\overline{RD}$ going low triggers a conversion and the AD7572A acknowledges by taking $\overline{BUSY}$ low. Data from the previous conversion appears on the three state data outputs. $\overline{BUSY}$ returns high at the end of conversion when the output latches have been updated and the conversion result is placed on data outputs D11 . . . D0/8.

SLOW MEMORY MODE, TWO BYTE READ

For a two byte read only 8 data outputs D7 . . . D0/8 are used. Conversion start procedure and data output status for the first read operation is identical to Slow Memory Mode, Parallel Read. See Figure 18 timing diagram and Table II data bus status. At the end of conversion the low data byte (DB7 . . . DB0) is read from the ADC. A second READ operation, with HBEN high, places the high byte on data outputs D3/11 . . . D0/8 and disables conversion start. Note the 4MSBs appear on data outputs D11 . . . D8 during the two READ operations above.

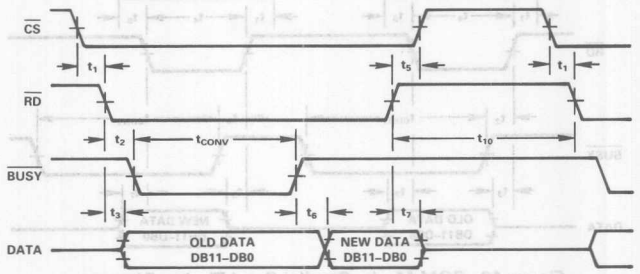


Figure 17. Slow Memory Mode, Parallel Read Timing Diagram

Table I. Slow Memory Mode, Parallel Read Data Bus Status

AD7572A Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

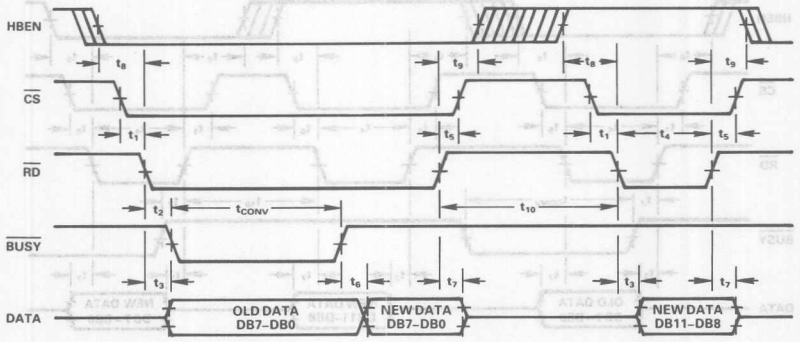


Figure 18. Slow Memory Mode, Two Byte Read Timing Diagram

Table II. Slow Memory Mode, Two Byte Read Data Bus Status

AD7572A Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

ROM MODE, PARALLEL READ (HBEN = LOW)

The ROM Mode avoids placing a microprocessor into a wait state. A conversion is started with a READ operation, and the 12-bits of data from the previous conversion are available on data outputs D11 . . . D0/8 (see Figure 19 and Table III). This data may be disregarded if not required. A second READ operation reads the new data (DB11 . . . DB0) and starts another conversion. A delay at least as long as the AD7572A conversion time must be allowed between READ operations.

ROM MODE, TWO BYTE READ

As previously mentioned for a two byte read, only data outputs D7 . . . D0/8 are used. Conversion is started in the normal way with a READ operation and the data output status is the same as the ROM Mode, Parallel Read. See Figure 20 timing diagram and Table IV data bus status. Two more READ operations are required to access the new conversion result. A delay equal to the AD7572A conversion time must be allowed between conversion start and the second data READ operation. The second READ operation, with HBEN high, disables conversion start and places the high byte (4 MSBs) on data outputs D3/11 . . . D0/8. A third READ operation accesses the low data byte (DB7 . . . DB0) and starts another conversion. The 4MSBs appear on data outputs D11 . . . D8 during all three read operations above.

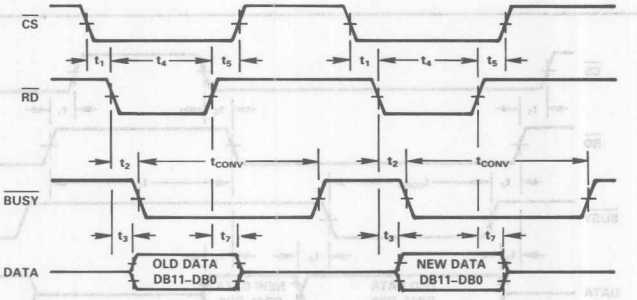


Figure 19. ROM Mode, Parallel Read Timing Diagram

Table III. ROM Mode, Parallel Read Data Bus Status

AD7572A Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

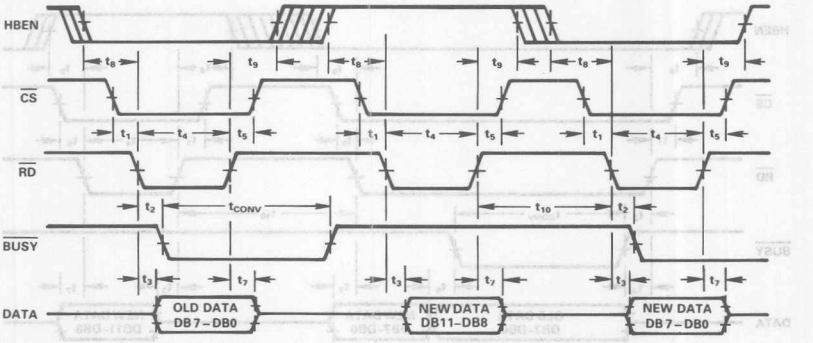


Figure 20. ROM Mode, Two Byte Read Timing Diagram

Table IV. ROM Mode, Two Byte Read Data Bus Status

AD7572A Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8
Third Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

MICROPROCESSOR INTERFACING

The AD7572A is designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. The HBEN input serves as a data byte select for 8-bit processors and is normally connected to the microprocessor address bus.

MC68000 Microprocessor

Figure 21 shows a typical interface for the 68000. The AD7572A is operating in the Slow Memory Mode. Assuming the AD7572A is located at address C000, then the following single 16-bit MOVE instruction both starts a conversion and reads the conversion result.

Move.W $C000,D0

At the beginning of the instruction cycle when the ADC address is selected, $\overline{BUSY}$ and $\overline{CS}$ assert $\overline{DTACK}$, so that the 68000 is forced into a WAIT state. At the end of conversion $\overline{BUSY}$ returns high and the conversion result is placed in the D0 register of the µP.

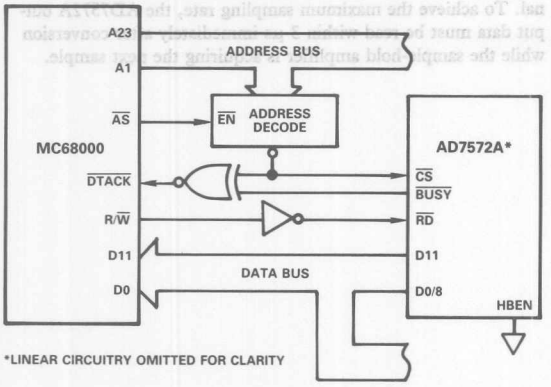


Figure 21. AD7572A–MC68000 Interface

8085A, Z80 MICROPROCESSOR

Figure 22 shows an AD7572A interface for the Z80 and 8085A. The AD7572A is operating in the Slow Memory Mode and a two byte read is required. Not shown in the figure is the 8-bit latch required to demultiplex the 8085A common address/data bus. A0 is used to assert HBEN, so that an even address (HBEN = LOW) to the AD7572A will start a conversion and read the low data byte. An odd address (HBEN = HIGH) will read the high data byte. This is accomplished with the single 16-bit LOAD instruction below.

For the 8085A LHLD (B000)
For the Z80 LD HL, (B000)

This is a two byte read instruction which loads the ADC data (address B000) into the HL register pair. During the first read operation, BUSY forces the microprocessor to WAIT for the AD7572A conversion. No WAIT states are inserted during the second read operation when the microprocessor is reading the high data byte.

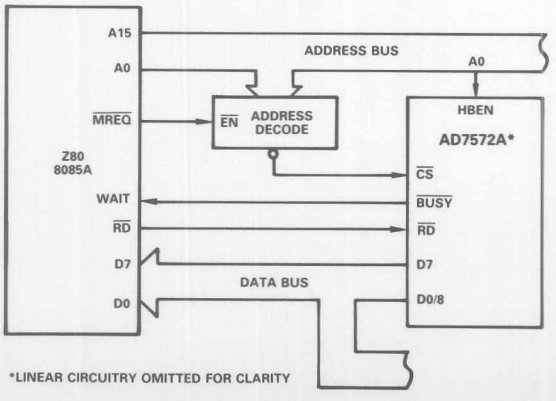


Figure 22. AD7572A–8085/Z80 Interface

TMS32010 MICROCOMPUTER

Figure 23 shows an AD7572A-TMS32010 interface. The AD7572A is operating in the ROM Mode. The interface is designed for a maximum TMS32010 clock frequency of 18 MHz but will typically work over the full TMS32010 clock frequency range.

The AD7572A is mapped at a port address. The following I/O instruction starts a conversion and reads the previous conversion result into data memory.

IN A,PA (PA = PORT ADDRESS)

When conversion is complete, a second I/O instruction reads the up-to-date data into data memory and starts another conversion. A delay at least as long as the ADC conversion time must be allowed between I/O instructions.

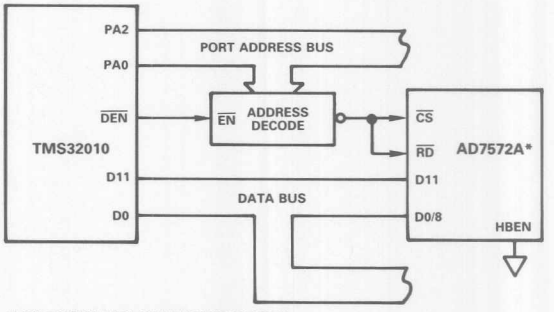


Figure 23. AD7572A–TMS32010 Interface

AD7572A–AD585 SAMPLE-HOLD INTERFACE

Figure 24 shows an AD585 sample-hold amplifier driving the AIN input of the AD7572A. The interface contains resistors R1, R2, R3 and R4 to allow a bipolar input signal range of ±2.5 volts. The maximum sampling frequency is 166 kHz for the AD7572AXX03 (3 μs conversion) and 77 kHz for the AD7572AXX10 (10 μs conversion). This includes the sample-hold amplifier acquisition time (3 μs).

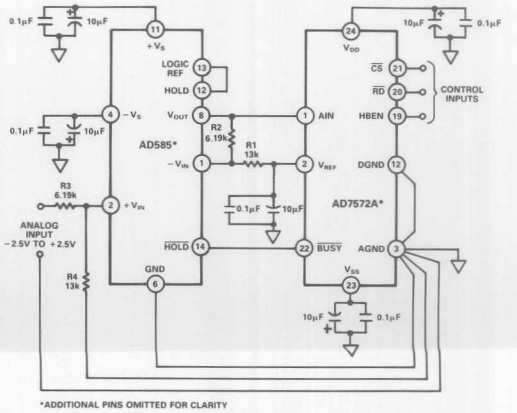
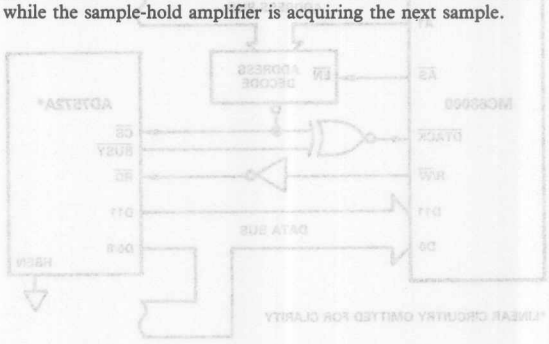


Figure 24. AD7572A–AD585 Sample-and-Hold Interface

When an AD7572A conversion is initiated, the converter $\overline{BUSY}$ output goes low indicating conversion is in progress. The falling edge of this $\overline{BUSY}$ output signal places the sample-hold amplifier into the HOLD mode "freezing" the input signal to the AD7572A. When conversion is finished, the $\overline{BUSY}$ output returns HIGH allowing the sample-hold to track the input signal. To achieve the maximum sampling rate, the AD7572A output data must be read within 3 µs immediately after conversion while the sample-hold amplifier is acquiring the next sample.



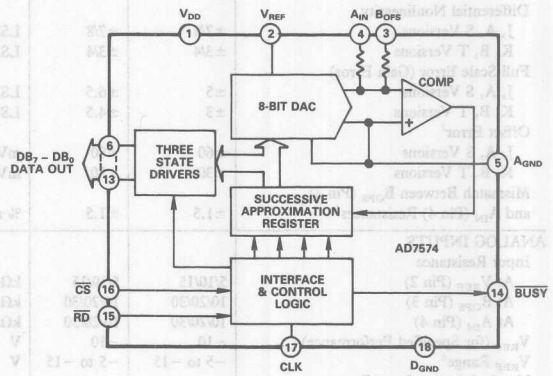
CMOS µP-Compatible 8-Bit ADC

AD7574

FEATURES

- 8-Bit Resolution
- No Missed Codes over Full Temperature Range
- Fast Conversion Time: 15µs
- Interfaces to µP like RAM, ROM or Slow - Memory
- Low Power Dissipation: 30mW
- Ratiometric Capability
- Single +5V Supply
- Low Cost
- Internal Comparator and Clock Oscillator

FUNCTIONAL BLOCK DIAGRAM



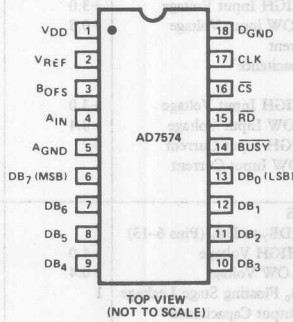
GENERAL DESCRIPTION

AD7574 is a low-cost, 8-bit µP compatible ADC which uses the successive-approximations technique to provide a conversion time of 15µs.

Designed to be operated as a memory mapped input device, the AD7574 can be interfaced like static RAM, ROM, or slow memory. Its $\overline{CS}$ (decoded device address) and $\overline{RD}$ ($\overline{READ}/\overline{WRITE}$ control) inputs are available in all µP memory systems. These two inputs control all ADC operations such as starting conversion or reading data. The ADC output data bits use three-state logic, allowing direct connection to the µP data bus or system input port.

Internal clock, +5V operation, on-board comparator and interface logic, as well as low power dissipation (30mW) and fast conversion time make the AD7574 ideal for most ADC/µP interface applications. Small size (18-pin DIP) and monolithic reliability will find wide use in avionics, instrumentation, and process automation applications.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Differential Nonlinearity (LSB)	Package Option*
AD7574JN	0°C to +70°C	±7/8 max	N-24
AD7574KN	0°C to +70°C	±3/4 max	N-24
AD7574AQ	−25°C to +85°C	±7/8 max	Q-24
AD7574BQ	−25°C to +85°C	±3/4 max	Q-24
AD7574SQ	−55°C to +125°C	±7/8 max	Q-24
AD7574TQ	−55°C to +125°C	±3/4 max	Q-24

*N = Plastic DIP; Q = Cerdip. For outline information see Package Information section.

AD7574—SPECIFICATIONS

DC SPECIFICATIONS (V_{DD} = +5V, V_{REF} = −10V, Unipolar Configuration, R_{CLK} = 180kΩ, C_{CLK} = 100pF, unless otherwise noted)

Parameter	Limits T_A = +25°C	Limits T_{min}, T_{max}[1]	Units	Conditions/Comments
ACCURACY				
Resolution	8	8	Bits	
Relative Accuracy Error				
J, A, S Versions	±3/4	±3/4	LSB max	Relative Accuracy and Differential Nonlinearity are measured
K, B, T Versions	±1/2	±1/2	LSB max	dynamically using the external clock circuit of Figure 7b.
Differential Nonlinearity				Clock frequency is 500kHz (conversion time 15µs).
J, A, S Versions	±7/8	±7/8	LSB max	
K, B, T Versions	±3/4	±3/4	LSB max	
Full Scale Error (Gain Error)				Full Scale Error is measured after calibrating out offset error. See
J, A, S Versions	±5	±6.5	LSB max	Figure 8a and associated calibration procedure for offset. Max Full
K, B, T Versions	±3	±4.5	LSB max	Scale change from +25°C to T_{min} or T_{max} is ±2LSB.
Offset Error[2]				
J, A, S Versions	±60	±80	mV max	Maximum Offset change from +25°C to T_{min} or T_{max} is ±20mV.
K, B, T Versions	±30	±50	mV max	
Mismatch Between B_{OFS} (Pin 3) and A_{IN} (Pin 4) Resistances[3]	±1.5	±1.5	% max	
ANALOG INPUTS				
Input Resistance				
At V_{REF} (Pin 2)	5/10/15	5/10/15	kΩ min/typ/max	
At B_{OFS} (Pin 3)	10/20/30	10/20/30	kΩ min/typ/max	
At A_{IN} (Pin 4)	10/20/30	10/20/30	kΩ min/typ/max	
V_{REF} (for Specified Performance)	−10	−10	V	±5% for specified transfer accuracy.
V_{REF} Range[4]	−5 to −15	−5 to −15	V	Degraded transfer accuracy.
Nominal Analog Input Range				
Unipolar Mode	0 to $+\lvert V_{REF}\rvert$		V	
Bipolar Mode	$-\lvert V_{REF}\rvert$ to $+\lvert V_{REF}\rvert$		V	
LOGIC INPUTS				
$\overline{RD}$ (Pin 15), $\overline{CS}$ (Pin 16)				
V_{INH} Logic HIGH Input Voltage	+3.0	+3.0	V min	
V_{INL} Logic LOW input Voltage	+0.8	+0.8	V max	
I_{IN} Input Current	1	10	µA max	V_{IN} = 0V, V_{DD}
C_{IN} Input Capacitance[5]	5	5	pF max	
CLK (Pin 17)				
V_{INH} Logic HIGH Input Voltage	+3.0	+3.0	V min	
V_{INL} Logic LOW Input Voltage	+0.4	+0.4	V max	
I_{INH} Logic HIGH Input Current	+2	+2	mA max	During Conversion: $V_{IN(CLK)} \geq V_{INH(CLK)}$
I_{INL} Logic LOW Input Current	1	10	µA max	During Conversion $V_{IN(CLK)} \leq V_{INL(CLK)}$ (see circuit of Figure 7b if external clock operation is required).
LOGIC OUTPUTS				
BUSY (Pin 14), DB_7 to DB_0 (Pins 6–13)				
V_{OH} Output HIGH Voltage	+4.0	+4.0	V min	I_{SOURCE} = 40µA
V_{OL} Output LOW Voltage	+0.4	+0.8	V max	I_{SINK} = 1.6mA
I_{LKG} DB_7 to DB_0 Floating Stage Leakage	1	10	µA max	V_{OUT} = 0V or V_{DD}
Floating State Output Capacitance (DB_7 to DB_0)[5]	7	7	pF max	
Output Code	Unipolar Binary, Offset Binary			See Figures 8a, 9a, 10a, and 8b, 9b, 10b.
POWER REQUIREMENTS				
V_{DD}	+5	+5	V	±5% for specified performance.
I_{DD} (STANDBY)	5	5	mA max	A_{IN} = 0V, ADC in RESET condition.
I_{REF}	V_{REF} divided by 5kΩ		max	Conversion complete, prior to RESET.

NOTES

[1]Temperature ranges as follows: J, K, Versions, 0°C to +70°C; A, B Versions, −25°C to +85°C; S, T Versions; −55°C to +125°C.

[2]Typical offset temperature coefficient is ±150µV/°C.

[3]R_{BOFS}/R_{AIN} mismatch causes transfer function rotation about positive Full Scale. The effect is an offset and a gain term when using the circuit of Figure 9a.

[4]Typical value, not guaranteed or subject to test.

[5]Guaranteed but not tested.

Specifications subject to change without notice.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



AC SPECIFICATIONS (V_{DD} = +5V, C_{CLK} = 100pF, R_{CLK} = 180kΩ unless otherwise noted)

Symbol	Specification	Limit at T_A = +25°C	Limit at T_A = T_{min}	Limit at T_A = T_{max}	Conditions
STATIC RAM INTERFACE MODE (See Figure 1 and Table I)					
t_{CS}	$\overline{CS}$ Pulse Width Requirement	100ns min	150ns min	150ns min	
t_{WSCS}	$\overline{RD}$ to $\overline{CS}$ Setup Time	0 min	0 min	0 min	
t_{CBPD}	$\overline{CS}$ to BUSY Propagation Delay	90ns typ	70ns typ	150ns typ	
		120ns max	120ns max	180ns max	$\overline{BUSY}$ Load = 20pF
		120ns type	100ns typ	180ns typ	
		150ns max	150ns max	200ns max	$\overline{BUSY}$ Load = 100pF
t_{BSR}	$\overline{BUSY}$ to $\overline{RD}$ Setup Time	0 min	0 min	0 min	
t_{BSCS}	$\overline{BUSY}$ to $\overline{CS}$ Setup Time	0 min	0 min	0 min	
t_{RAD}	Data Access Time	120ns typ	100ns typ	180ns typ	
		150ns max	150ns max	220ns max	DB_0–DB_7 Load = 100pF
		240ns typ	220ns typ	300ns typ	
		300ns max	300ns max	400ns max	DB_0–DB_7 Load = 100pF
t_{RHD}	Data Hold Time	80ns typ	40ns typ	120ns typ	
		50ns min	30ns min	80ns min	
		120ns max	80ns max	180ns max	
t_{RHCS}	$\overline{CS}$ to $\overline{RD}$ Hold Time	250ns max	200 ns max	500ns max	
t_{RESET}	Reset Time Requirement	3µs min	3µs min	3µs min	
$t_{CONVERT}$	Conversion Time				
	Using Internal Clock Oscillator		See Typical Data of Figure 7a		
$t_{CONVERT}$	Conversion Time				f_{CLK} = 500kHz
	Using External Clock	15µs	15µs	15µs	Circuit of Figure 7b
ROM INTERFACE MODE (See Figure 2 and Table II)					
t_{RAD}	Data Access Time		Same as RAM Mode		
t_{RHD}	Data Hold Time		Same as RAM Mode		
t_{WBPD}	RD HIGH to BUSY	400ns typ	350ns typ	1µs typ	
	Propagation Delay	1.5µs	1.0µs	2.0µs	$\overline{BUSY}$ Load = 20 pF
t_{BSR}	BUSY to RD LOW Setup Time	RD can go LOW prior to BUSY = HIGH, but must not return HIGH until = BUSY HIGH. See Table II.			
$t_{CONVERT}$	Conversion Time	See Typical data of Figure 7a. Add 2µs to			
	Using Internal Clock Oscillator	data shown in Figure 7a for ROM Mode			
SLOW – MEMORY INTERFACE MODE (See Figure 3 and Table III)					
t_{CBPD}	CS to BUSY Propagation Delay		Same as RAM Mode		
t_{RESET}	Reset Time Requirement		Same as RAM Mode		
t_{RAD}	Data Access Time		Same as RAM Mode		
t_{RHD}	Data Hold Time		Same as RAM Mode		
$t_{CONVERT}$	Conversion Time		Same as RAM Mode		

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to A_{GND} . . . . . 0V, +7.0V
V_{DD} to D_{GND} . . . . . 0V, +7.0V
A_{GND} to D_{GND} . . . . . −0.3V, V_{DD}
Digital Input Voltage to D_{GND} (Pins 15 and 16) . . . . −0.3V, +15.0V
Digital Output Voltage to D_{GND} (Pins 6–14) . . . . . −0.3V, V_{DD}
CLK Input Voltage (Pin 17) to D_{GND} . . . . . −0.3V, V_{DD}
V_{REF} (Pin 2) . . . . . ±20V
V_{BOFS} (Pin 3) . . . . . ±20V
V_{AIN} (Pin 4) . . . . . ±20V
Operating Temperature Range
Commercial (J, K Versions) . . . . . 0°C to +70°C
Industrial (A, B Versions) . . . . . −25°C to +85°C
Extended (S, T Versions) . . . . . −55°C to +150°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (soldering, 10 secs) . . . . . +300°CV
Power Dissipation (Package)
Plastic (Suffix N)
to +70°C 670mW
Derate above +70°C by . . . . . 8.3mW/°C
Cerdip (Suffix Q)
to +75°C 450mW
Derate above +75°C by . . . . . 6mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

TERMINOLOGY

RESOLUTION: Resolution is a measure of the *nominal* analog change required for a 1-bit change in the A/D converter's digital output. While normally expressed in a number of bits, the analog resolution of an n-bit unipolar A/D converter is (2^{-n}) V_{REF}). Thus, the AD7574, an 8-bit A/D converter, can resolve analog voltages as small as (1/256) (V_{REF}) when operated in a unipolar mode. When operated in a bipolar mode, the resolution is (1/128) (V_{REF}). Resolution does not imply accuracy. *Usable* resolution is limited by the differential nonlinearity of the A/D converter.

RELATIVE ACCURACY: Relative accuracy is the deviation of the ADC's actual code transition points from a straight line drawn between the devices' measured zero and measured full scale transition points. Relative accuracy, therefore, is a measure of code *position*.

DIFFERENTIAL NONLINEARITY: Differential nonlinearity in an ADC is a measure of the size of an anlog voltage range associated with any digitial output code. As such, differential nonlinearity specifies code width (usable resolution). An ADC with a specified differential nonlinearity of ±n bits will exhibit codes ranging in width from 1LSB −n LSB to 1LSB +n LSB. A specified differential nonlinearity of less than ±1LSB guarantees no-missing-codes operation.

ments for AD7574 operation as a static RAM.

A convert start is initiated by executing a memory WRITE instruction to the address location occupied by the AD7574 (once conversion has started, subsequent memory WRITES have no effect). A data READ is performed by executing a memory READ instruction to the AD7574 address location.

$\overline{BUSY}$ must be HIGH before a data READ is attempted, i.e. the total delay between a convert start and a data READ must be at least as great as the AD7574 conversion time. The delay

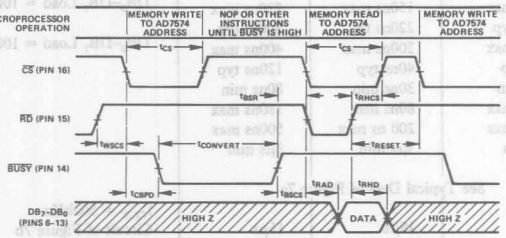


Figure 1. Static RAM Mode Timing Diagram

sion complete), a data READ is performed by executing a memory READ instruction to the address location occupied by the AD7574. The data readout is destructive, i.e. when RD returns HIGH, the converter is internally reset.

The RAM interface mode uses distinctly different commands to start conversion (memory WRITE) or read the data (memory READ). This is in contrast to the ROM mode where a memory READ causes a data READ *and* a conversion restart.

Table I. Truth Table, Static RAM Mode

AD7574 INPUTS		AD7574 OUTPUTS		AD7574 OPERATION
$\overline{CS}$	$\overline{RD}$	$\overline{BUSY}$	$DB_7 \cdot DB_0$	
L	H	H	HIGH Z	WRITE CYCLE (START CONVERT)
L	⊓	H	HIGH Z → DATA	READ CYCLE (DATA READ)
L	⊔	H	DATA → HIGH Z	RESET CONVERTER
H	X[1]	X	HIGH Z	NOT SELECTED
L	H	L	HIGH Z	NO EFFECT, CONVERTER BUSY
L	⊓	L	HIGH Z	NO EFFECT, CONVERTER BUSY
L	⊔	L	HIGH Z	NOT ALLOWED, CAUSES INCORRECT CONVERSION

Note 1: If $\overline{RD}$ goes LOW to HIGH when $\overline{CS}$ is LOW, the ADC is internally reset. $\overline{RD}$ has no effect while $\overline{CS}$ is HIGH. See application hint No. 1.

ROM INTERFACE MODE

Table II and Figure 2 show the truth table and timing requirements for interfacing the AD7574 like Read Only Memory.

$\overline{CS}$ is held LOW and converter operation is controlled by the $\overline{RD}$ input. The AD7574 $\overline{RD}$ input is derived from the decoded device address. MEMRD should be used to enable the address decoder in 8080 systems. VMA should be used to enable the address decoder in 6800 systems. A data READ is initiated by executing a memory READ instruction to the AD7574 address location. The converter is automatically restarted when $\overline{RD}$ returns HIGH. As in the RAM mode, attempting a data READ before $\overline{BUSY}$ is HIGH will result in incorrect data being read.

The advantage of the ROM mode is its simplicity. The major disadvantage is that the data obtained is relatively poorly defined in time inasmuch as executing a data READ automatically starts a new conversion. This problem can be overcome by executing two READs separated by NO-OPS (or other program instructions) and using only the data obtained from the second READ.

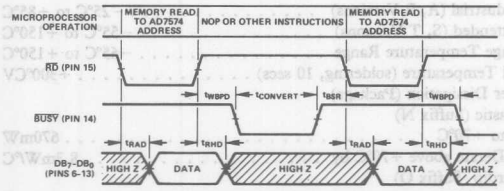


Figure 2. ROM Mode Timing Diagram ($\overline{CS}$ Held LOW)

Table II. Truth Table, ROM Mode

AD7574 INPUTS		AD7574 OUTPUTS		AD7574 OPERATION
$\overline{CS}$	$\overline{RD}$	$\overline{BUSY}$	$DB_7 \cdot DB_0$	
L	⊓	H	HIGH Z → DATA	DATA READ
L	⊔	H	DATA → HIGH Z	RESET AND START NEW CONVERSION
L	⊓	L	HIGH Z	NO EFFECT, CONVERTER BUSY
L	⊔	L	HIGH Z	NOT ALLOWED, CAUSES INCORRECT CONVERSION

SLOW-MEMORY INTERFACE MODE

Table III and Figure 3 show the truth table and timing requirements for interfacing the AD7574 as a slow-memory. This mode is intended for use with processors which can be forced into a WAIT state for at least 12μs (such as the 8080, 8085 and SC/MP). The major advantage of this mode is that it allows the μP to start conversion, WAIT, and then READ data with a single READ instruction.

In the slow-memory mode, $\overline{CS}$ and $\overline{RD}$ are tied together. It is suggested that the system ALE signal (8085 system) or SYNC signal (8080 system) be used to latch the address. The decoded device address is subsequently used to drive the AD7574 $\overline{CS}$ and $\overline{RD}$ inputs. $\overline{BUSY}$ is connected to the microprocessor READY input.

When the AD7574 is NOT addressed, the $\overline{CS}$ and $\overline{RD}$ inputs are HIGH. Conversion is initiated by executing a memory READ to the AD7574 address. $\overline{BUSY}$ subsequently goes LOW (forcing the μP READY input LOW) placing the μP in a WAIT state. When conversion is complete ($\overline{BUSY}$ is HIGH) the μP completes the memory READ.

Do not attempt to perform a memory WRITE in this mode, since three-state bus conflicts will arise.

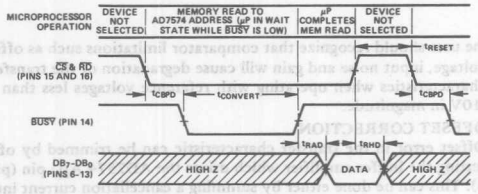


Figure 3. Slow Memory Mode Timing Diagram (CS and RD Tied Together)

Table III. Truth Table, Slow Memory Mode

AD7574 INPUTS	AD7574 OUTPUTS		AD7574 OPERATION
CS & RD	BUSY	DB_7 - DB_0	
H	H	HIGH Z	NOT SELECTED
⌐	H → L	HIGH Z	START CONVERSION
L	L	HIGH Z	CONVERSION IN PROGRESS, μP IN WAIT STATE
L	⌐	HIGH Z → DATA	CONVERSION COMPLETE, μP READS DATA
⌐	H	DATA → HIGH Z	CONVERTER RESET AND DESELECTED
H	H	HIGH Z	NOT SELECTED

2

GENERAL CIRCUIT INFORMATION

BASIC CIRCUIT DESCRIPTION

The AD7574 uses the successive approximations technique to provide an 8-bit parallel digital output. The control logic was designed to provide easy interface to most microprocessors. Most applications require only passive clock components (R & C), a -10V reference, and +5V power.

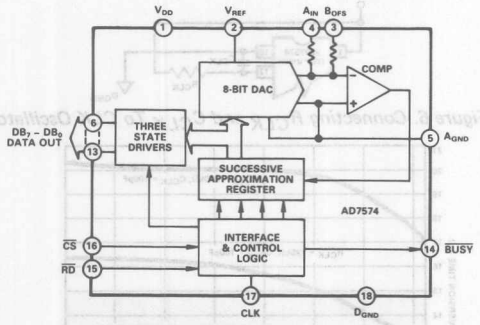


Figure 4. AD7574 Functional Diagram

Figure 4 shows the AD7574 functional diagram. Upon receipt of a start command either via the $\overline{CS}$ or $\overline{RD}$ pins, $\overline{BUSY}$ goes low indicating conversion is in progress. Successive bits, starting with the most significant bit (MSB) are applied to the input of a DAC. The comparator determines whether the addition of each successive bit causes the DAC output to be greater than or less than the analog input, A_{IN}. If the sum of the DAC bits is less than A_{IN}, the trial bit is left ON, and the next smaller bit is tried. If the sum is greater than A_{IN}, the trial bit is turned OFF and the next smaller bit is tried.

Each successively smaller bit is tried and compared to A_{IN} in this manner until the least significant bit (LSB) decision has been made. At this time $\overline{BUSY}$ goes HIGH (conversion is complete) indicating the successive approximation register contains a valid representation of the analog input. The $\overline{RD}$ control (see the previous page for details) can then be exercised to activate the three-state buffers, placing data on the DB_0 – DB_7 data output pins. $\overline{RD}$ returning HIGH causes the clock oscillator to run for 1 cycle, providing an internal ADC reset (i.e. the SAR is loaded with code 10000000).

DAC CIRCUIT DETAILS

The current weighting D/A converter is a precision multiplying DAC. Figure 5 shows the functional diagram of the DAC as used in the AD7574. It consists of a precision Silicon Chromium thin film R/2R ladder network and 8 N-channel MOSFET switches operated in single-pole-double-throw.

The currents in each 2R shunt arm are binarily weighted, i.e. the current in the MSB arm is V_{REF} divided by 2R, in the second arm is V_{REF} divided by 4R, etc. Depending on the DAC logic input (A/D output) from the successive approximation register, the current in the individual shunt arms is steered either to A_{GND} or to the comparator summing point.

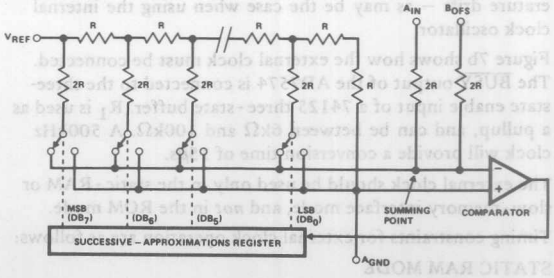


Figure 5. D/A Converter As Used In AD7574

OPERATING THE AD7574

APPLICATION HINTS

1. TIMING & CONTROL
   In the AD7574 when a conversion is finished the fresh data must be read before a new conversion can be started.
   Failure to observe the timing restrictions of Figures 1, 2 or 3 may cause the AD7574 to change interface modes. For example, in the RAM mode, holding $\overline{CS}$ LOW too long after $\overline{RD}$ goes HIGH will cause a new convert start (i.e. the converter moved into the ROM mode).
2. LOGIC DEGLITCHING IN uP APPLICATIONS
   Unspecified states on the address bus (due to different rise and fall times on the address bus) can cause glitches at the AD7574 $\overline{CS}$ or $\overline{RD}$ terminals. These glitches can cause unwanted convert starts, reads, or resets. The best way to avoid glitches is to gate the address decoding logic with RD or WR (8080) or VMA (6800) when in the ROM or RAM mode. When in the slow-memory mode, the ALE (8085) or SYNC (8080) signal should be used to latch the address.
3. INPUT LOADING AT V_{REF}, A_{IN} AND B_{OFS}
   To prevent loading errors due to the finite input resistance at the V_{REF}, A_{IN} or B_{OFS} pins, low impedance driving sources must be used (i.e. op amp buffers or low output-Z reference).
4. RATIOMETRIC OPERATION
   Ratiometric performance is inherent to A/D converters such as the AD7574 which use a multiplying DAC weighting network. However, the user should recognize that comparator limitations such as offset voltage, input noise and gain will cause degradation of the transfer characteristics when operating with reference voltages less than -10V in magnitude.
5. OFFSET CORRECTION
   Offset error in the transfer characteristic can be trimmed by offsetting the buffer amplifier which drives the AD7574 A_{IN} pin (pin 4). This can be done either by summing a cancellation current into the amplifier's summing junction, or by tapping a voltage divider which sits between V_{DD} and V_{REF} and applying the tap voltage to the amplifier's positive input (an example of a resistive tap offset adjust is shown in Figure 10a where R_8, R_9 and R_{10} can be used to offset the ADC).
6. ANALOG AND DIGITAL GROUND
   It is recommended that A_{GND} and D_{GND} be connected locally to prevent the possibility of injecting noise into the AD7574. In systems where the A_{GND}-D_{GND} intertie is not local, connect back-to-back diodes (IN914 or equivalent) between the AD7574 A_{GND} and D_{GND} pins.
7. INITIALIZATION AFTER POWER – UP
   Execute a memory READ to the AD7574 address location, and subsequently ignore the data. The AD7574 is internally reset when reading out data, i.e. the data readout is destructive.

CLOCK OSCILLATOR

The AD7574 has an internal asynchronous clock oscillator which starts upon receipt of a convert start command, and ceases oscillating when conversion is complete.

The clock oscillator requires an external R and C as shown in Figure 6. Nominal conversion times versus R_{CLK} and C_{CLK} is shown in Figure 7a. The curves shown in Figure 7a are applicable when operating in the RAM or slow-memory interface modes. When operating in the ROM interface mode, add 2μs to the typical conversion time values shown.

The AD7574 is guaranteed to provide transfer accuracy to published specifications for conversion times down to 15μs, as indicated by the unshaded region of Figure 7a. Conversion times faster than 15μs can cause transfer accuracy degradation.

OPERATION WITH EXTERNAL CLOCK

For applications requiring a conversion time close to or equal to 15μs, an external clock is recommended. Using an external clock precludes the possibility of converting faster than 15μs (which can cause transfer accuracy degradation) due to temperature drift – as may be the case when using the internal clock oscillator.

Figure 7b shows how the external clock must be connected. The $\overline{BUSY}$ output of the AD7574 is connected to the three-state enable input of a 74125 three-state buffer. R_1 is used as a pullup, and can be between 6kΩ and 100kΩ. A 500kHz clock will provide a conversion time of 15μs.

The external clock should be used only in the static-RAM or slow-memory interface mode, and *not* in the ROM mode.

Timing constraints for external clock operation are as follows:

STATIC RAM MODE

1. When initiating a conversion, $\overline{CS}$ should go LOW on a positive clock edge to provide optimum settling time for the MSB.
2. A data READ can be initiated any time after $\overline{BUSY}$ = 1.

SLOW-MEMORY MODE

1. When initiating a conversion, $\overline{CS}$ and $\overline{RD}$ should go LOW on a positive clock edge to provide optimum settling time for the MSB.

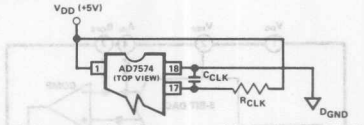


Figure 6. Connecting R_{CLK} and C_{CLK} To CLK Oscillator

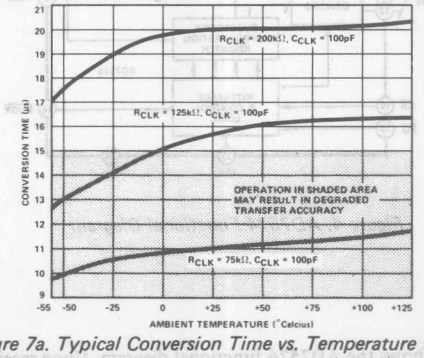


Figure 7a. Typical Conversion Time vs. Temperature For Different R_{CLK} and C_{CLK} (Applicable to RAM and Slow-Memory Modes. For ROM Mode add 2μs to values shown)

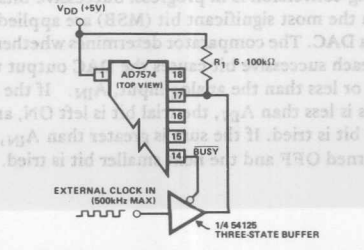


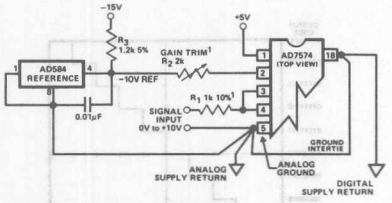
Figure 7b. External Clock Operation (Static RAM and Slow-Memory Mode)

Figures 8a and 8b show the analog circuit connections and typical transfer characteristic for unipolar operation. An AD584 is used as the -10V reference.

Calibration is as follows:

OFFSET

Offset must be trimmed out in the signal conditioning circuitry used to drive the signal input terminals shown in Figure 8a. An example of an offset trim is shown in Figure 10a, where R_8, R_9 and R_{10} comprise a simple voltage tap which is applied to the amplifier's positive input.



Note 1: R_1 and R_2 can be omitted if gain trim is not required

Figure 8a. AD7574 Unipolar (0V to +10V) Operation (Output Code is Straight Binary)

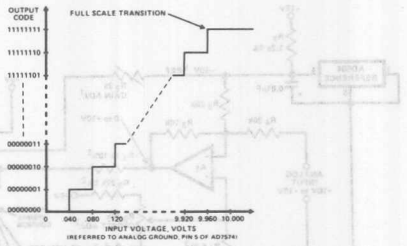
fier used to drive R_1 (i.e. +39.1mV at R_1).

2. While performing continuous conversions, adjust the offset potentiometer (described above) until DB_7 - DB_1 are LOW and the LSB (DB_0) flickers.

GAIN (FULL SCALE)

Offset adjustment must be performed before gain adjustment.

1. Apply -9.961V to the input of the buffer amplifier used to drive R_1 (i.e. +9.961V at R_1).
2. While performing continuous conversions, adjust trim pot R_2 until DB_7 - DB_1 are HIGH and the LSB (DB_0) flickers.



Note: Approximate bit weights are shown for illustration. Nominal bit weight for a -10V reference is ≈ 39.1mV

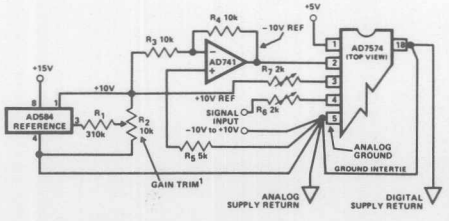
Figure 8b. Nominal Transfer Characteristic For Unipolar Circuit of Figure 8a

BIPOLAR (OFFSET BINARY) OPERATION

Figures 9a and 9b illustrate the analog circuitry and transfer characteristic for bipolar operation. Output coding is offset binary. As in unipolar operation, offset correction can be performed at the buffer amplifier used to drive the signal input terminals of Figure 9a (Resistors R_8, R_9 and R_{10} in Figure 10a show how offset trim can be done at the buffer amplifier).

Calibration is as follows:

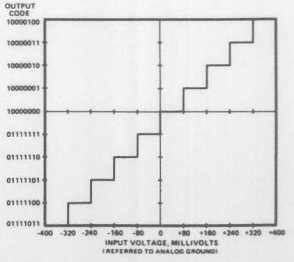
1. Adjust R_6 and R_7 for minimum resistance across the potentiometers.
2. Apply +10.000V to the buffer amplifier used to drive the signal input (i.e. -10.000V at R_6).
3. While performing continuous conversions, trim R_6 or R_7 (whichever required) until DB_7 - DB_1 are LOW and the LSB (DB_0) flickers.



Note 1: R_1 and R_2 can be omitted if gain trim is not required

Figure 9a. AD7574 Bipolar (-10V to +10V) Operation (Output Code is Offset Binary)

4. Apply 0V to the buffer amplifier used to drive the signal input terminals.
5. Doing continuous conversions, trim the offset circuit of the buffer amplifier until the ADC output code flickers between 01111111 and 10000000.
6. Apply +10.000V to the input of the buffer amplifier (i.e. -10.000V as applied to R_6).
7. Doing continuous conversions, trim R_2 until DB_7 - DB_1 are LOW and the LSB (DB_0) flickers.
8. Apply -9.922V to the input of the buffer amplifier (i.e. +9.922V at the input side of R_6).
9. If the ADC output code is not 11111110 ±1 bit, repeat the calibration procedure.



Note: Approximate bit weights are shown for illustration. Nominal bit weight for ± 10V full scale is ≈ 78.1mV

Figure 9b. Nominal Transfer Characteristic Around Major Carry for Bipolar Circuit of Figure 9a

BIPOLAR (COMPLEMENTARY OFFSET BINARY) OPERATION

Figure 10a shows the analog connections for complementary offset binary operation. The typical transfer characteristic is shown in Figure 10b. In this bipolar mode, the ADC is fooled into believing it is operated in a unipolar mode - i.e. the +10V to –10V analog input is conditioned into a 0 to +10V signal range. R_2 is the gain adjust, while R_9 is the offset adjust.

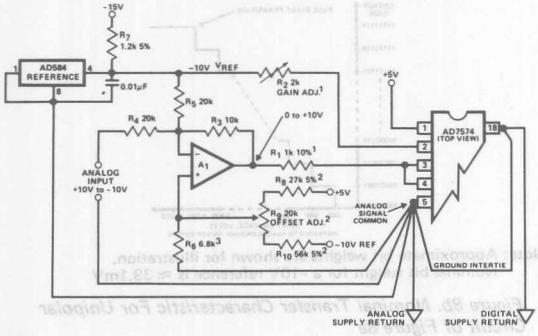
Calibration is as follows (adjust offset before gain):

OFFSET

1. Apply OV to the analog input shown in Figure 10a.
2. While performing continuous conversions, adjust R_9 until the converter output flickers between codes 01111111 and 10000000.

GAIN (FULL SCALE)

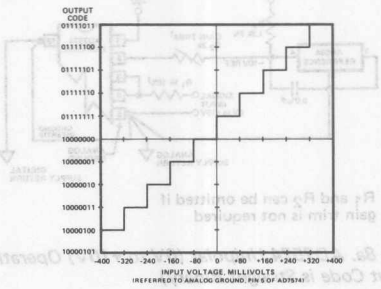
1. Apply –9.922V across the analog input terminals shown in Figure 10a.
2. While performing continuous conversions, adjust R_2 until DB_7 - DB_1 are HIGH and the LSB (DB_0) flickers between HIGH and LOW.



Notes:

1. R_1 and R_2 can be omitted if gain trim is not required
2. R_8, R_9 and R_{10} can be omitted if offset trim is not required
3. $R_6 \| R_8 \| R_{10} = 5k\Omega$. If R_8, R_9 and R_{10} not used, make $R_6 = 5k\Omega$

Figure 10a. AD7574 Bipolar Operation (–10V to +10V) (Output Code is Complementary Offset Binary)



Note: Approximate bit weights are shown for illustration. Nominal bit weight for ±10V full scale is ≈ 78.1mV

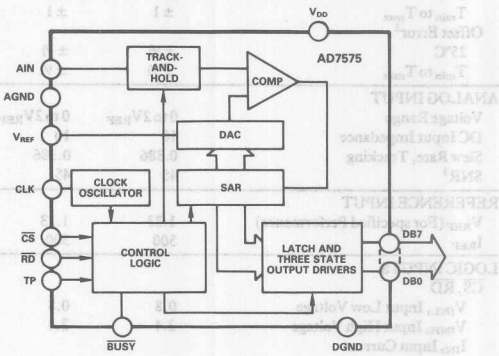
Figure 10b. Nominal Transfer Characteristic Around Major Carry for Bipolar Circuit of Figure 10a

LC²MOS
5μs 8-Bit ADC with Track/Hold
AD7575

FEATURES

- Fast Conversion Time: 5μs
- On-Chip Track/Hold
- Low Total Unadjusted Error: 1LSB
- Full Power Signal Bandwidth: 50kHz
- Single +5V Supply
- 100ns Data Access Time
- Low Power (15mW typ)
- Low Cost
- Standard 18-Pin DIPs or 20-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7575 is a high-speed 8-bit ADC with a built-in track/hold function. The successive approximation conversion technique is used to achieve a fast conversion time of 5μs, while the built-in track/hold allows full-scale signals up to 50kHz (386mV/μs slew rate) to be digitized. The AD7575 requires only a single +5V supply and a low-cost, 1.23V bandgap reference in order to convert an input signal range of 0 to $2V_{REF}$.

The AD7575 is designed for easy interfacing to all popular 8-bit microprocessors using standard microprocessor control signals ($\overline{CS}$ and $\overline{RD}$) to control starting of the conversion and reading of the data. The interface logic allows the AD7575 to be easily configured as a memory mapped device and the part can be interfaced as SLOW-MEMORY or ROM. All data outputs of the AD7575 are latched and three-state buffered to allow direct connection to a microprocessor data bus or I/O port.

The AD7575 is fabricated in an advanced, all ion-implanted high speed Linear Compatible CMOS (LC^2MOS) process and is available in a small, 0.3" wide, 18-pin DIP or in 20-terminal surface mount packages.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time/Low Power
   The fast, 5μs conversion time of the AD7575 makes it suitable for digitizing wideband signals at audio and ultrasonic frequencies, while retaining the advantage of low CMOS power consumption.
2. On-Chip Track/Hold
   The on-chip track/hold function is completely self-contained and requires no external hold capacitor. Signals with slew rates up to 386mV/μs (e.g., 2.46V peak-to-peak 50kHz sine waves) can be digitized with full accuracy.
3. Low Total Unadjusted Error
   The zero, full-scale and linearity errors of the AD7575 are so low that the total unadjusted error at any point on the transfer function is less than 1LSB and offset and gain adjustments are not required.
4. Single Supply Operation
   Operation from a single +5V supply with a low-cost +1.23V bandgap reference allows the AD7575 to be used in 5V microprocessor systems without any additional power supplies.
5. Fast Digital Interface
   Fast interface timing allows the AD7575 to interface easily to the fast versions of most popular microprocessors such as the Z80H, 8085A-2, 6502B, 68B09 and the DSP processor, the TMS32010.

AD7575—SPECIFICATIONS (V_{DD} = +5V, V_{REF} = +1.23V, AGND = DGND = 0V; f_{CLK} = 4MHz external; All specifications T_{min} to T_{max} unless otherwise specified)

Parameter	J, A Versions[1]	K, B Versions	S Version	T Version	Units	Conditions/Comments
ACCURACY						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error	±2	±1	±2	±1	LSB max	
Relative Accuracy	±1	±½	±1	±½	LSB max	
Minimum Resolution for which						
No Missing Codes is Guaranteed	8	8	8	8	Bits max	
Full Scale Error						
25°C	±1	±1	±1	±1	LSB max	Full Scale TC is typically 5ppm/°C
T_{min} to T_{max}	±1	±1	±1	±1	LSB max	
Offset Error[2]						
25°C	±½	±½	±½	±½	LSB max	Offset TC is typically 5ppm/°C
T_{min} to T_{max}	±½	±½	±½	±½	LSB max	
ANALOG INPUT						
Voltage Range	0 to $2V_{REF}$	0 to $2V_{REF}$	0 to $2V_{REF}$	0 to $2V_{REF}$	Volts	1LSB = $2V_{REF}$/256; See Figure 16
DC Input Impedance	10	10	10	10	MΩ min	
Slew Rate, Tracking	0.386	0.386	0.386	0.386	V/μs max	
SNR[3]	45	45	45	45	dB min	V_{IN} = 2.46V p-p @ 10kHz; See Figure 11
REFERENCE INPUT						
V_{REF} (For specified Performance)	1.23	1.23	1.23	1.23	Volts	±5%
I_{REF}	500	500	500	500	μA max	
LOGIC INPUTS						
$\overline{CS}$, $\overline{RD}$						
V_{INL}, Input Low Voltage	0.8	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	2.4	V min	
I_{IN}, Input Current						
25°C	±1	±1	±1	±1	μA max	V_{IN} = 0 or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	V_{IN} = 0 or V_{DD}
C_{IN}, Input Capacitance[3]	10	10	10	10	pF max	
CLK						
V_{INL}, Input Low Voltage	0.8	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	2.4	V min	
I_{INL}, Input Low Current	700	700	800	800	μA max	V_{INL} = 0V
I_{INH}, Input High Current	700	700	800	800	μA max	V_{INH} = V_{DD}
LOGIC OUTPUTS						
$\overline{BUSY}$, DB0 to DB7						
V_{OL}, Output Low Voltage	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 40μA
DB0 to DB7						
Floating State Leakage Current	±1	±1	±10	±10	μA max	V_{OUT} = 0 to V_{DD}
Floating State Output Capacitance[3]	10	10	10	10	pF max	
CONVERSION TIME[4]						
With External Clock	5	5	5	5	μs	f_{CLK} = 4MHz
With Internal Clock, T_A = 25°C	5	5	5	5	μs min	Using recommended clock
	15	15	15	15	μs max	components shown in Figure 15.
POWER REQUIREMENTS[5]						
V_{DD}	+5	+5	+5	+5	Volts	±5% for Specified Performance
I_{DD}	6	6	7	7	mA max	Typically 3mA with V_{DD} = +5V
Power Dissipation	15	15	15	15	mW typ	
Power Supply Rejection	±¼	±¼	±¼	±¼	LSB max	4.75V≤V_{DD}≤5.25V

NOTES

[1]Temperature Ranges are as follows:
J, K Versions; 0 to +70°C
A, B Versions; −25°C to +85°C
S, T Versions; −55°C to +125°C

[2]Offset error is measured with respect to an ideal first code transition which occurs at 1/2LSB.

[3]Sample tested at 25°C to ensure compliance.

[4]Accuracy may degrade at conversion times other than those specified.

[5]Power supply current is measured when AD7575 is inactive i.e. when $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = logic HIGH.

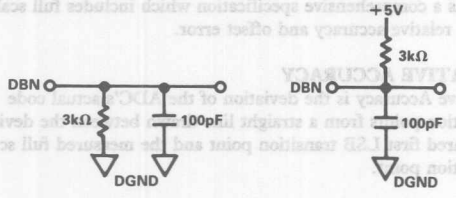
Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +5V, V_{REF} = +1.23V, AGND = DGND = 0V)

Parameter	Limit at +25°C (All Versions)	Limit at T_{min}, T_{max} (J, K, A, B Versions)	Limit at T_{min}, T_{max} (S, T Versions)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_2	100	100	120	ns max	$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay
t_3[2]	100	100	120	ns max	Data Access Time after $\overline{RD}$
t_4	100	100	120	ns min	$\overline{RD}$ Pulse Width
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6[2]	80	80	100	ns max	Data Access Time after $\overline{BUSY}$
t_7[3]	10	10	10	ns min	Data Hold Time
	80	80	100	ns max	
t_8	0	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Delay

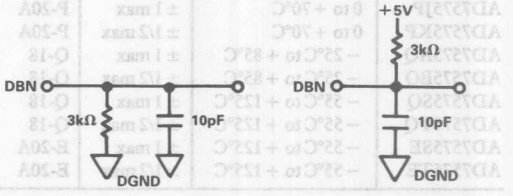
NOTES
[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[3]t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.

Test Circuits



a. High-Z to V_{OH} b. High-Z to V_{OL}

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High-Z b. V_{OL} to High-Z

Figure 2. Load Circuits for Data Hold Time Test

ABSOLUTE MAXIMUM RATINGS*

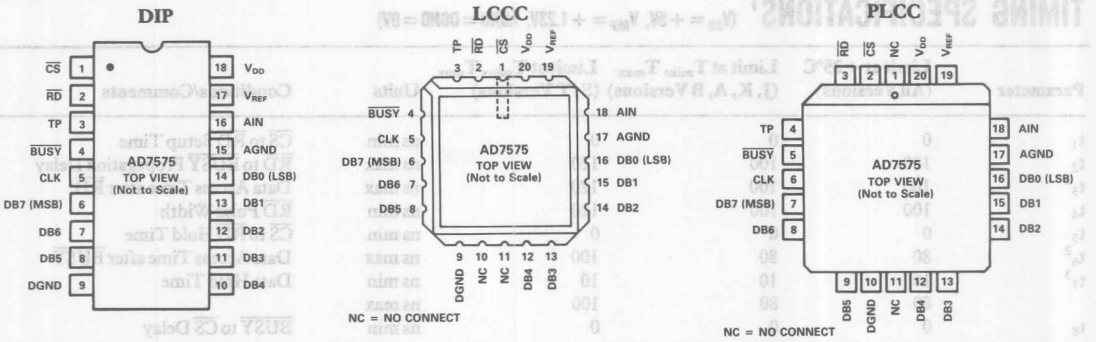
V_{DD} to AGND	−0.3V, +7V
V_{DD} to DGND	−0.3V, +7V
AGND to DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND	−0.3V, V_{DD} +0.3V
CLK Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{REF} to AGND	−0.3V, V_{DD}
AIN to AGND	−0.3V, V_{DD}
Operating Temperature Range	
Commercial (J, K Versions)	0 to +70°C
Industrial (A, B Versions)	−25°C to +85°C
Extended (S, T Versions)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation (Any Package) to +75°C	450mW
Derates above +75°C by	6mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.





ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy (LSB)	Package Options[2]
AD7575JN	0 to +70°C	±1 max	N-18
AD7575KN	0 to +70°C	±1/2 max	N-18
AD7575JP	0 to +70°C	±1 max	P-20A
AD7575KP	0 to +70°C	±1/2 max	P-20A
AD7575AQ	−25°C to +85°C	±1 max	Q-18
AD7575BQ	−25°C to +85°C	±1/2 max	Q-18
AD7575SQ	−55°C to +125°C	±1 max	Q-18
AD7575TQ	−55°C to +125°C	±1/2 max	Q-18
AD7575SE	−55°C to +125°C	±1 max	E-20A
AD7575TE	−55°C to +125°C	±1/2 max	E-20A

NOTES
[1]To order MIL-STD-883, Class B process parts, add /883B to part number. Contact local sales office for military data sheet. For U.S. Standard Military Drawing (SMD), see DESC drawing #5962-87762.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

TERMINOLOGY

LEAST SIGNIFICANT BIT (LSB)
An ADC with 8-bits resolution can resolve 1 part in 2^8 (i.e., 256) of full scale. For the AD7575 with +2.46V full scale one LSB is 9.61mV.

TOTAL UNADJUSTED ERROR
This is a comprehensive specification which includes full scale error, relative accuracy and offset error.

RELATIVE ACCURACY
Relative Accuracy is the deviation of the ADC's actual code transition points from a straight line drawn between the devices measured first LSB transition point and the measured full scale transition point.

SNR
Signal-to-Noise Ratio (SNR) is the ratio of the desired signal to the noise produced in the sampled and digitized analog signal. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine wave input is given by

SNR = (6.02N + 1.76)dB

where N is the number of bits in the ADC.

FULL SCALE ERROR (GAIN ERROR)
The gain of a unipolar ADC is defined as the difference between the analog input levels required to produce the first and the last digital output code transitions. Gain error is a measure of the deviation of the actual span from the ideal span of FS – 2LSB's.

ANALOG INPUT RANGE
With V_{REF} = +1.23V the maximum analog input voltage range is 0 to +2.46V. The output data in LSB's is related to the analog input voltage by the integer value of the following expression:

$$\text{Data (LSB's)} = \frac{256\ \text{AIN}}{2V_{REF}} + 0.5$$

SLEW RATE
Slew Rate is the maximum allowable rate of change of input signal such that the digital sample values are not in error. Slew Rate limitations may restrict the analog signal bandwidth for full-scale analog signals below the bandwidth allowed from sampling theorem considerations.

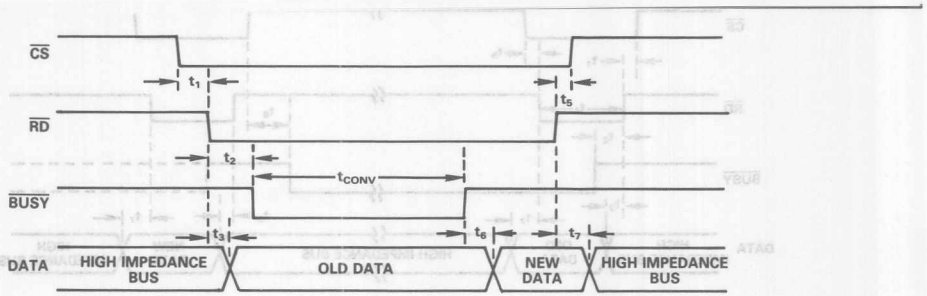


Figure 3. Slow Memory Interface Timing Diagram

TIMING AND CONTROL OF THE AD7575

The two logic inputs on the AD7575, $\overline{CS}$ and $\overline{RD}$, control both the starting of conversion and the reading of data from the part. A conversion is initiated by bringing both these control inputs LOW. Two interface options then exist for reading the output data from the AD7575. These are the Slow Memory Interface and ROM Interface and their operation is outlined below. It should be noted that the TP pin of the AD7575 must be hardwired HIGH to ensure correct operation of the part. This pin is used in testing the device and should not be used as a feedthrough pin in double-sided printed circuit boards.

SLOW MEMORY INTERFACE

The first interface option is intended for use with microprocessors which can be forced into a WAIT STATE for at least 5μs (such as the 8085A). The microprocessor starts a conversion and is halted until the result of the conversion is read from the converter. Conversion is initiated by executing a memory READ to the AD7575 address bringing $\overline{CS}$ and $\overline{RD}$ LOW. $\overline{BUSY}$ subsequently goes LOW (forcing the microprocessor READY input LOW) placing the processor into a WAIT state. The input signal, which had been tracked by the analog input, is held on the third falling clock edge of the input clock after $\overline{CS}$ and $\overline{RD}$ have gone LOW (see Figure 12). The AD7575 then performs a conversion on this acquired input signal value. When the conversion is complete ($\overline{BUSY}$ goes HIGH), the processor completes the memory READ and acquires the newly-converted data. The timing diagram for this interface is shown in Figure 3.

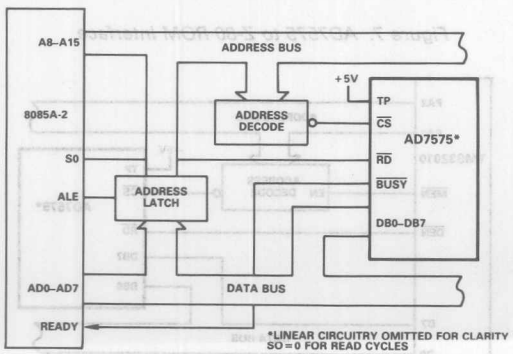


Figure 4. AD7575 to 8085A-2 Slow Memory Interface

The major advantage of this interface is that it allows the microprocessor to start conversion, WAIT and then READ data with a single READ instruction. The fast conversion time of the AD7575 ensures that the microprocessor is not placed in a WAIT state for an excessive amount of time.

Faster versions of many processors, including the 8085A-2, test the condition of the READY input very soon after the start of an instruction cycle. Therefore, $\overline{BUSY}$ of the AD7575 must go LOW very early in the cycle for the READY input to be effective in forcing the processor into a WAIT state. When using the 8085A-2, the processor S0 status signal provides the earliest possible indication that a READ operation is about to occur. Hence, S0 (which is LOW for a READ cycle) provides the READ signal to the AD7575. The connection diagram for the AD7575 to 8085A-2 Slow-Memory interface is shown in Figure 4.

ROM INTERFACE

The alternative interface option on the AD7575 avoids placing the microprocessor into a WAIT state. In this interface, a conversion is started with the first READ instruction and the second READ instruction accesses the data and starts a second conversion. The timing diagram for this interface is shown in Figure 5. It is possible to avoid starting another conversion on the second READ (see below).

Conversion is initiated by executing a memory READ instruction to the AD7575 address causing $\overline{CS}$ and $\overline{RD}$ to go LOW. Data is also obtained from the AD7575 during this instruction. This is old data and may be disregarded if not required. $\overline{BUSY}$ goes LOW indicating that conversion is in progress and returns HIGH when conversion is complete. Once again the input signal is held on the third falling edge of the input clock after $\overline{CS}$ and $\overline{RD}$ have gone LOW.

The $\overline{BUSY}$ line may be used to generate an interrupt to the microprocessor or monitored to indicate that conversion is complete. The processor then reads the newly-converted data. Alternatively, the delay between the convert start (first READ instruction) and the data READ (second READ instruction) must be at least as great as the AD7575 conversion time. For the AD7575 to operate correctly in the ROM interface mode $\overline{CS}$ and $\overline{RD}$ should not go LOW before $\overline{BUSY}$ returns HIGH.

Normally, the second READ instruction starts another conversion as well as accessing the output data. However, if $\overline{CS}$ and $\overline{RD}$ are brought LOW within one external clock period of $\overline{BUSY}$ going HIGH then a second conversion does not occur.

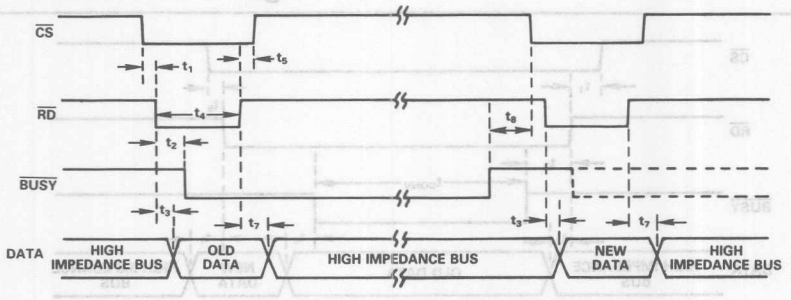


Figure 5. ROM Interface Timing Diagram

Figures 6 and 7 show connection diagrams for interfacing the AD7575 in the ROM Interface mode. Figure 6 shows the AD7575 interface to the 6502/6809 microprocessors while the connection diagram for interfacing to the Z-80 is shown in Figure 7.

As a result of its very fast interface timing the AD7575 can also be interfaced to the DSP processor, the TMS32010. The AD7575 will interface (within specifications) to the TMS32010 running at up to 18MHz but will typically work over the full clock frequency range of the TMS32010. Figure 8 shows the connection diagram for this interface. The AD7575 is mapped at a port address. Conversion is initiated using an IN A, PA instruction where PA is the decoded port address for the AD7575. The conversion result is obtained from the part using a second IN A, PA instruction and the resultant data is placed in the TMS32010 accumulator.

In many applications it is important that the signal sampling occurs at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. The interfaces outlined previously require that for sampling at equi-distant intervals the user must count clock cycles or match software delays. This is especially difficult in interrupt driven systems where uncertainty in interrupt servicing delays would require that the AD7575 would have to have priority interrupt status and even then redundant software delays may be necessary to equalize loop delays.

This problem can be overcome by using a real time clock to control the starting of conversion. This can be derived from the clock source used to drive the AD7575 CLK pin. Since the sampling instant occurs three clock cycles after $\overline{CS}$ and $\overline{RD}$ go LOW then the input signal sampling intervals are equi-distant. The resultant data is placed in a FIFO latch which can be accessed by the microprocessor at its own rate whenever it requires the data. This ensures that data is not READ from the AD7575 during a conversion. If a data READ is performed during a conversion, valid data from the previous conversion will be accessed but the conversion in progress may be interfered with and an incorrect result is likely.

If $\overline{CS}$ and $\overline{RD}$ go LOW within 20ns of a falling clock edge the AD7575 may or may not see that falling edge as the first of the three falling clock edges to the sampling instant. In this case the sampling instant could vary by one clock period. If it is important to know the exact sampling instant, $\overline{CS}$ and $\overline{RD}$ should not go LOW within 20ns of a falling clock edge.

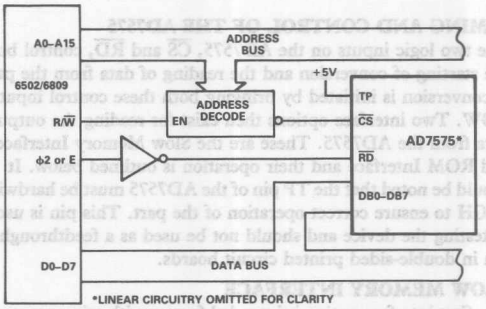


Figure 6. AD7575 to 6502/6809 ROM Interface

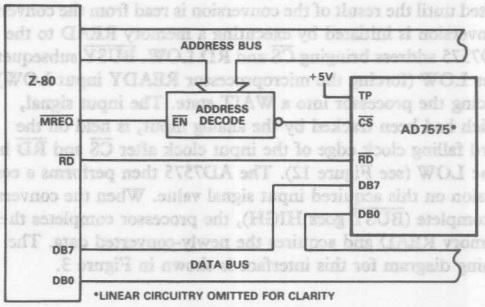


Figure 7. AD7575 to Z-80 ROM Interface

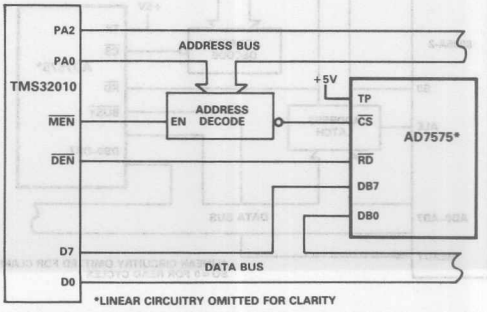


Figure 8. AD7575 to TMS32010 ROM Interface

A SAMPLED-DATA INPUT

The AD7575 makes use of a sampled-data comparator. The equivalent input circuit is shown in Figure 9. When a conversion starts, switch S1 is closed and the equivalent input capacitance is charged to V_{IN}. With a switch resistance of typically 500Ω and an input capacitance of typically 2pF the input time constant is 1ns. Thus C_{IN} becomes charged to within ±1/4LSB in 6.9 time constants or about 7ns. Since the AD7575 requires two input clock cycles (at a clock frequency of 4MHz) before going into the compare mode, there is ample time for the input voltage to settle before the first comparator decision is made. Increasing the source resistance increases the settling time required. Input bypass capacitors placed directly at the analog input act to average the input charging currents. The average current flowing through any source impedance can cause full-scale errors.

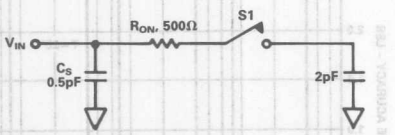


Figure 9. AD7575 Equivalent Input Circuit

REFERENCE INPUT

The reference input impedance on the AD7575 is code dependent and varies by a ratio of approximately 3-to-1 over the digital code range. The typical resistance range is from 6kΩ to 18kΩ. As a result of the code dependent input impedance, the V_{REF} input must be driven from a low impedance source. Figure 10 shows how an AD589 can be configured to produce a nominal reference voltage of +1.23V.

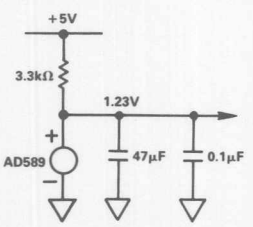


Figure 10. Reference Circuit

TRACK-AND-HOLD

The on-chip track-and-hold on the AD7575 means that input signals with slew rates up to 386mV/μs can be converted without error. This corresponds to an input signal bandwidth of 50kHz for a 2.46V peak-to-peak sine wave. Figure 11 shows a typical plot of signal-to-noise ratio versus input frequency, over the input bandwidth of the AD7575. The SNR figures are generated using a 200kHz sampling frequency and the reconstructed sine wave passes through a filter with a cutoff frequency of 50kHz.

The improvement in the SNR figures seen at the higher frequencies is due to the sharp cut-off of the filter (50kHz, 8th order Chebyshev) used in the test circuit.

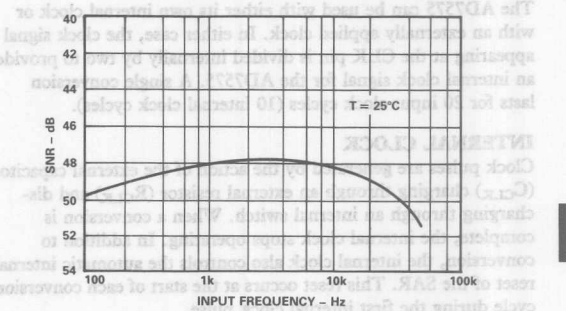


Figure 11. SNR vs. Input Frequency

The input signal is held on the third falling edge of the input clock after $\overline{CS}$ and $\overline{RD}$ go LOW. This is indicated in Figure 12 for the Slow Memory Interface. In between conversions the input signal is tracked by the AD7575 track-and-hold. Since the sampled signal is held on a small, on-chip capacitor it is advisable that the data bus be kept as quiet as possible during a conversion.

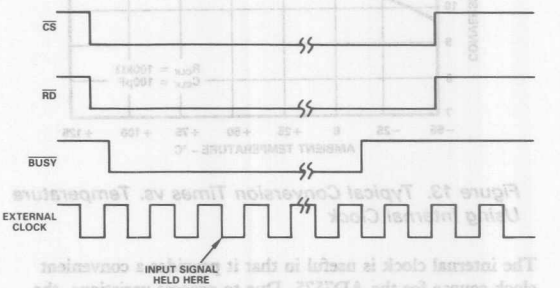


Figure 12a. Track-and-Hold (Slow Memory Interface) with External Clock

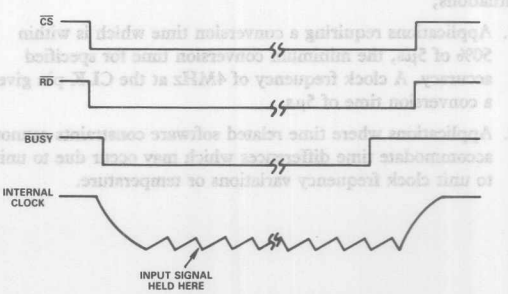


Figure 12b. Track-and-Hold (Slow Memory Interface) with Internal Clock

INTERNAL/EXTERNAL CLOCK

The AD7575 can be used with either its own internal clock or with an externally applied clock. In either case, the clock signal appearing at the CLK pin is divided internally by two to provide an internal clock signal for the AD7575. A single conversion lasts for 20 input clock cycles (10 internal clock cycles).

INTERNAL CLOCK

Clock pulses are generated by the action of the external capacitor (C_{CLK}) charging through an external resistor (R_{CLK}) and discharging through an internal switch. When a conversion is complete, the internal clock stops operating. In addition to conversion, the internal clock also controls the automatic internal reset of the SAR. This reset occurs at the start of each conversion cycle during the first internal clock pulse.

Nominal conversion times versus temperature for the recommended R_{CLK} and C_{CLK} combination are shown in Figure 13.

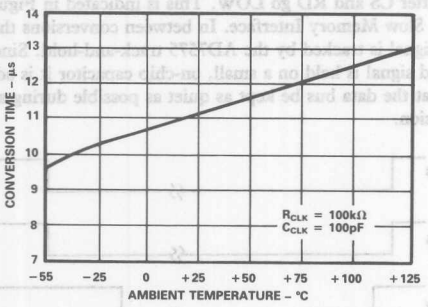


Figure 13. Typical Conversion Times vs. Temperature Using Internal Clock

The internal clock is useful in that it provides a convenient clock source for the AD7575. Due to process variations, the actual operating frequency for this R_{CLK}/C_{CLK} combination can vary from device to device by up to ±50%. For this reason it is recommended that an external clock be used in the following situations;

1. Applications requiring a conversion time which is within 50% of 5µs, the minimum conversion time for specified accuracy. A clock frequency of 4MHz at the CLK pin gives a conversion time of 5µs.
2. Applications where time related software constraints cannot accommodate time differences which may occur due to unit to unit clock frequency variations or temperature.

EXTERNAL CLOCK

The CLK input of the AD7575 may be driven directly from 74HC, 4000B series buffers (such as 4049) or from LS TTL with a 5.6kΩ pull-up resistor. When conversion is complete, the internal clock is disabled even if the external clock is still applied. This means that the external clock can continue to run between conversions without being disabled. The mark/space ratio of the external clock can vary from 70/30 to 30/70.

The AD7575 is specified for operation at a 5µs conversion rate with a 4MHz input clock frequency. If the part is operated at slower clock frequencies, it may result in slightly degraded accuracy performance from the part. This is a result of leakage effects on the hold capacitor. Figure 14 shows a typical plot of accuracy versus conversion time for the AD7575.

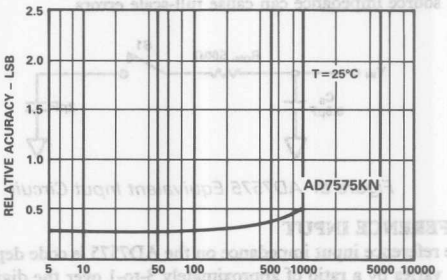


Figure 14. Accuracy vs. Conversion Time

UNIPOLAR OPERATION

The basic operation for the AD7575 is in the unipolar single supply mode. Figure 15 shows the circuit connections to achieve this while the nominal transfer characteristic for unipolar operation is given in Figure 16. Since the offset and full-scale errors on the AD7575 are very small, in many cases it will not be necessary to adjust out these errors. If calibration is required the procedure is as follows:

Offset Adjust

Offset error adjustment in single-supply systems is easily achievable by means of the offset null facility of an op-amp when used as a voltage follower for the analog input signal, AIN. The op-amp chosen should be able to operate from a single supply and allow a common-mode input voltage range that includes 0V (e.g., TLC271). To adjust for zero offset the input signal source is set to +4.8mV (i.e., 1/2LSB) while the op-amp offset is varied until the ADC output code flickers between 000 . . . 00 and 000 . . . 01.

Full Scale Adjust

The full scale or gain adjustment is made by forcing the analog input AIN to +2.445V (i.e., Full-Scale Voltage −3/2LSB). The magnitude of the reference voltage is then adjusted until the ADC output code flickers between 111 . . . 10 and 111 . . . 11.

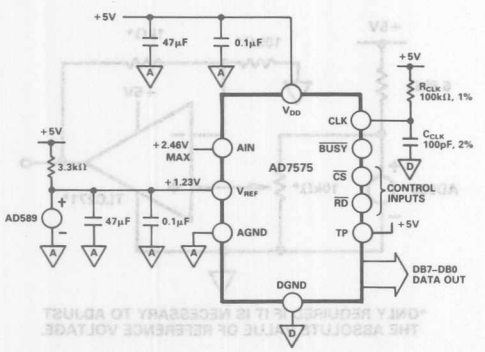


Figure 15. AD7575 Unipolar Configuration

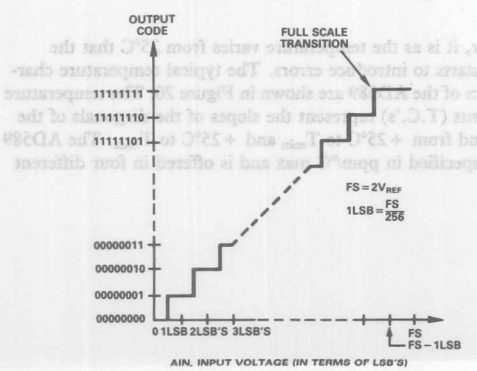


Figure 16. Nominal Transfer Characteristic for Unipolar Operation

BIPOLAR OPERATION

The circuit of Figure 17 shows how the AD7575 can be configured for bipolar operation. The output code provided by the AD7575 is offset binary. The analog input voltage range is ±5V, although the voltage appearing at the AIN pin of the AD7575 is in the range 0V to +2.46V. Figure 18 shows the transfer function for bipolar operation. The LSB size is now 39.06mV. Calibration of the bipolar operation is outlined below. Once again, because the errors are small it may not be necessary to adjust them. To maintain specified performance without the calibration all resistors should be 0.1% tolerance with R4 and R5 replaced by one 3.3kΩ resistor and R2 and R3 replaced by one 2.5kΩ resistor.

Offset Adjust

Offset error adjustment is achieved by applying an analog input voltage of −4.9805V (−FS +1/2LSB). Resistor R3 is then adjusted until the output code flickers between 000 . . . 00 and 000 . . . 01.

Full Scale Adjust

Full scale or gain adjustment is made by applying an analog input voltage of +4.9414V (+FS −3/2LSB). Resistor R4 is then adjusted until the output code flickers between 111 . . . 10 and 111 . . . 11.

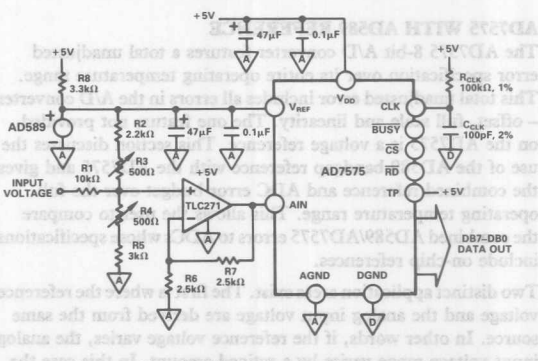


Figure 17. AD7575 Bipolar Configuration

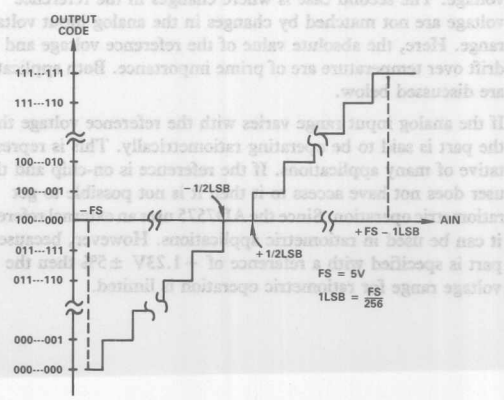


Figure 18. Nominal Transfer Characteristic for Bipolar Operation

APPLICATION HINTS

1. NOISE: Both the input signal lead to AIN, and the signal return lead from AGND should be kept as short as possible to minimize input-noise coupling. In applications where this is not possible, either a shielded cable or a twisted pair transmission line between source and ADC is recommended. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedance as much as possible. In general, the source resistance should be kept below 2kΩ. Larger values of source resistance can cause undesired system noise pickup.
2. PROPER LAYOUT: Layout for a printed circuit board should ensure that digital and analog lines are kept separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track. Both the analog input and the reference input should be screened by AGND. A single point analog ground which is separate from the logic system ground should be established at or near the AD7575. This single point analog ground subsystem should be connected to the digital system ground by a single-track connection only. Any reference bypass capacitors, analog input filter capacitors or input signal shielding should be returned to the analog ground point.

AD7575 WITH AD589 REFERENCE

The AD7575 8-bit A/D converter features a total unadjusted error specification over its entire operating temperature range. This total unadjusted error includes all errors in the A/D converter – offset, full scale and linearity. The one feature not provided on the AD7575 is a voltage reference. This section discusses the use of the AD589 bandgap reference with the AD7575 and gives the combined reference and ADC error budget over the full operating temperature range. This allows the user to compare the combined AD589/AD7575 errors to ADCs whose specifications include on-chip references.

Two distinct application areas exist. The first is where the reference voltage and the analog input voltage are derived from the same source. In other words, if the reference voltage varies, the analog input voltage range varies by a ratioed amount. In this case the user is not worried about the absolute value of the reference voltage. The second case is where changes in the reference voltage are not matched by changes in the analog input voltage range. Here, the absolute value of the reference voltage and its drift over temperature are of prime importance. Both applications are discussed below.

If the analog input range varies with the reference voltage then the part is said to be operating ratiometrically. This is representative of many applications. If the reference is on-chip and the user does not have access to it then it is not possible to get ratiometric operation. Since the AD7575 uses an external reference, it can be used in ratiometric applications. However, because the part is specified with a reference of +1.23V ±5% then the voltage range for ratiometric operation is limited.

The error analysis over temperature of ratiometric applications is different from nonratiometric ones. Since the reference and analog input voltage range are ratioed to each other, temperature variations in the reference are matched by variations in the analog input range. Therefore, the AD589 contributes no additional errors over temperature to the system errors and the combined total unadjusted error specification for the AD589 and AD7575 is as per the total unadjusted error specification in this data sheet.

With nonratiometric applications, however, the analog input range stays the same if the reference varies and a full-scale error is introduced. The amount which the reference varies determines the amount of error introduced. The AD589 is graded on temperature coefficient and therefore selection of different grades allows the user to tailor the amount of error introduced to suit the system requirements. The reference voltage from the AD589 can lie between 1.2V and 1.25V. This reference voltage can be adjusted for the desired full-scale voltage range using the circuit outlined in Figure 19. For example, if an analog input voltage range of 0 to +2.46V is required, the reference should be adjusted to +1.23V. Once the reference is adjusted to the desired value at 25°C the total error is as per the total unadjusted error specification on the AD7575 specification pages. (To reduce this even further, offset and full-scale errors of the AD7575 can be adjusted out using the calibration procedure outlined in this data sheet.)

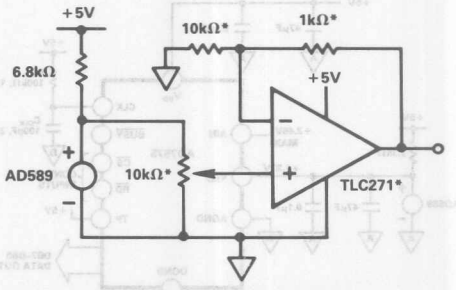


Figure 19. Reference Adjust Circuit

However, it is as the temperature varies from 25°C that the AD589 starts to introduce errors. The typical temperature characteristics of the AD589 are shown in Figure 20. The temperature coefficients (T.C.'s) represent the slopes of the diagonals of the error band from +25°C to T_{min} and +25°C to T_{max}. The AD589 T.C. is specified in ppm/°C max and is offered in four different grades.

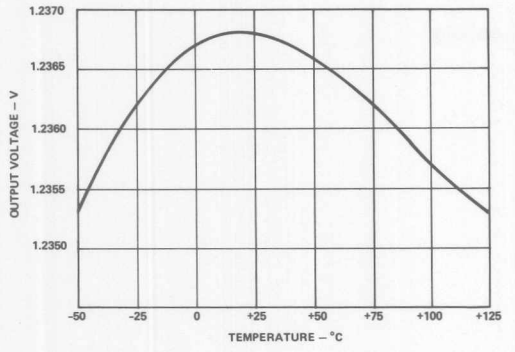


Figure 20. Typical AD589 Temperature Characteristics

The effect which the T.C. has on the system error is that it introduces a full-scale error in the ADC. This in turn affects the total unadjusted error specification. For example, using the AD589KH with a 50ppm/°C max T.C. the change in reference voltage from 25°C to 70°C is going to be from 1.23V to 1.22724V, a change of −2.76mV. This results in a change in the full-scale range of the ADC of −5.52mV, since the full-scale range on the AD7575 is $2V_{REF}$. Since the LSB size for the AD7575 is 9.61mV this means that the AD589 introduces an additional full-scale error of −0.57LSBs on top of the existing full-scale error specification for the ADC. Since the total unadjusted error specification for the ADC includes the full-scale error, there is also a corresponding increase in the total unadjusted error of −0.57LSBs. The change in reference voltage at 0°C is −1.5mV, resulting in a full-scale change of −3mV or −0.31LSBs worth of full-scale error. Table I shows the amount of additional total unadjusted error which is introduced by the temperature variation of the AD589, for different grades and for different temperature ranges. This table only applies to nonratiometric applications since the temperature variation of the reference does not affect the system error in ratiometric applications as outlined earlier. It shows the amount of error introduced over T_{min} to T_{max} for a system in which the reference has been adjusted to the desired value at 25°C. The final or right-most column of the table gives the total combined error for the AD589 and the top grade AD7575.

Taking the 25°C measurement as the starting point, the full-scale error introduced is always in the negative direction whether the temperature goes to T_{min} or T_{max}. This can be seen from the AD589 temperature characteristic shown in Figure 20. If the reference voltage is adjusted for 1.23V at 45°C (for the 0 to +70°C range) and 75°C (for the −55°C to +125°C range) the magnitude of the error introduced is reduced since it is distributed in both the positive and negative directions. Alternatively, this can be achieved, not by adjusting at these temperatures which would be impractical, but by adjusting the reference to 1.231V instead of 1.23V (for the extended temperature range) at 25°C. This has the required effect of distributing the plot of Figure 20 more evenly about the desired value.

An additional error source is the mismatch between the temperature coefficients (T.C.'s) of the 10kΩ and 1kΩ resistors in the feedback loop of the TLC271. If these resistors have ±50ppm/°C absolute T.C.'s then the worst case difference in drift between both resistors is 100ppm/°C. From +25°C to +125°C this introduces a worst case shift of 1.22mV which results in an additional full-scale error of 0.25LSB. If ±25ppm/°C resistors are used, then the worst case error is 0.13LSB. Over the 0 to +70°C range the ±50ppm/°C resistors introduce an additional full-scale error of 0.11LSB. All these errors are worst case and assume that the resistance values drift in opposite directions. In practice resistors of the same type and from the same manufacturer would drift in the same direction and hence the above error would be considerably reduced. An additional error source is the offset drift of the TLC271. This is only significant over the −55°C to +125°C range and even in this case it contributes <0.1LSB worth of full-scale error.

The error outlined in the right-hand column of Table I is a total unadjusted error specification excluding resistor and offset drift (the effect of these can be controlled by the user). It consists of errors from two error sources; a ±1LSB contribution from the AD7575 (including full-scale, offset and relative accuracy errors) and the remainder is a full-scale error introduced by the AD589. It is important to note that the variation of the AD589 voltage only introduces a full-scale error and that the relative accuracy (or endpoint nonlinearity) of the system, with a top grade AD7575, is still ±1/2LSB (i.e. 8-bits accurate).

AD589 Grade	Temperature Range (°C)	Full-Scale Error Introduced by AD589 @ T_{max} (Worst Case) (LSBs)	Combined Worst Case AD589/AD7575 T.U.E. @ T_{max} (LSBs)
AD589JH	0 to +70	−1.15	−2.15
AD589KH	0 to +70	−0.57	−1.57
AD589LH	0 to +70	−0.29	−1.29
AD589MH	0 to +70	−0.115	−1.115
AD589SH	−55 to +125	−2.56	−3.56
AD589TH	−55 to +125	−1.28	−2.28
AD589UH	−55 to +125	−0.64	−1.64

*Excluding resistor and offset drift.

Table I. AD589/AD7575 Errors over Temperature (Nonratiometric Applications)

Figure 20. Typical AD589 Temperature Characteristics

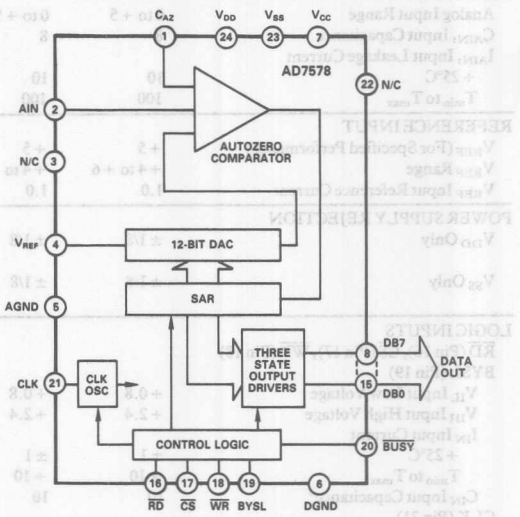
CMOS 12-Bit Successive Approximation ADC

AD7578

FEATURES

- 12-Bit Successive Approximation ADC
- No Missed Codes Over Full Temperature Range
- Low Total Unadjusted Error ±1LSB max
- High Impedance Analog Input
- Autozero Cycle for Low Offset Voltage
- Low Power, 75mW typ
- Small Size: 0.3", 24-Pin Package
- Conversion Time of 100μs

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7578 is a medium speed, monolithic 12-bit CMOS A/D converter which uses the successive approximation technique to provide a conversion time of 100μs. An auto-zero cycle occurs at the start of each conversion resulting in very low system offset voltages, typically less than 100μV. The device is designed for easy microprocessor interfacing using standard control signals; $\overline{CS}$ (decoded device address), $\overline{RD}$ ($\overline{READ}$) and $\overline{WR}$ ($\overline{WRITE}$).

Conversion results are available in two bytes, 8LSBs and 4MSBs, over an 8-bit three state output bus. Either byte can be read first. Two converter busy flags are available to facilitate polling of the converter's status.

The analog input voltage range is 0V to +5V when using a reference voltage of +5V.

PRODUCT HIGHLIGHTS

1. The AD7578 is a complete 12-bit A/D converter in a 24-pin package requiring only a few passive components and a voltage reference.
2. Autozero cycle realizes very low offset voltages, typically 100μV.
3. Standard microprocessor control signals to allow easy interfacing to most popular 8- and 16-bit microprocessors.
4. Monolithic construction for increased reliability and small 0.3", 24-pin package.

Resolution	12	12	12	Bits	
Total Unadjusted Error[2]	±1	±1	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	LSB max	No missing codes guaranteed
Full Scale Error (Gain Error)	±1/4	±1/4	±1/4	LSB max	Full Scale TC is typically 1ppm/°C
Offset Error	±1/4	±1/4	±1/4	LSB max	Offset Error TC is typically 1ppm/°C
ANALOG INPUT					
Analog Input Range	0 to +5	0 to +5	0 to +5	V	V_{REF} = +5.0V
C_{AIN}, Input Capacitance	8	8	8	pF typ	AIN; 0 to +5V
I_{AIN}, Input Leakage Current					
+25°C	10	10	10	nA max	
T_{min} to T_{max}	100	100	100	nA max	
REFERENCE INPUT					
V_{REF} (For Specified Performance)	+5	+5	+5	V	±5%
V_{REF} Range	+4 to +6	+4 to +6	+4 to +6	V	Degraded transfer accuracy
V_{REF} Input Reference Current	1.0	1.0	1.0	mA max	V_{REF} = +5.0V
POWER SUPPLY REJECTION					
V_{DD} Only	±1/8	±1/8	±1/8	LSB typ	V_{DD} = +14.25V to +15.75V V_{SS} = −5V
V_{SS} Only	±1/8	±1/8	±1/8	LSB typ	V_{SS} = −4.75V to −5.25V V_{DD} = +15V
LOGIC INPUTS					
$\overline{RD}$ (Pin 16), $\overline{CS}$ (Pin 17), $\overline{WR}$ (Pin 18)					
BYSL (Pin 19)					
V_{IL} Input Low Voltage	+0.8	+0.8	+0.8	V max	V_{CC} = +5V ±5%
V_{IH} Input High Voltage	+2.4	+2.4	+2.4	V min	
I_{IN} Input Current					
+25°C	±1	±1	±1	µA max	V_{IN} = 0 to V_{CC}
T_{min} to T_{max}	+10	+10	+10	µA max	
C_{IN} Input Capacitance[3]	10	10	10	pF max	
CLK (Pin 21)					
V_{IL}, Input Low Voltage	+0.8	+0.8	+0.8	V max	V_{CC} = +5V ±5%
V_{IH}, Input High Voltage	+3.0	+3.0	+3.0	V min	
I_{IL}, Input Low Current	±10	±10	±10	µA max	
I_{IH}, Input High Current	+1.5	+1.5	+1.5	mA max	
LOGIC OUTPUTS					
DB0–DB7 (Pins 8–15), $\overline{BUSY}$ (Pin 20)[4]					
V_{OL}, Output Low Voltage	+0.4	+0.4	+0.4	V max	V_{CC} = +5V ±5%, I_{SINK} = 1.6mA[4]
V_{OH}, Output High Voltage	+4.0	+4.0	+4.0	V min	V_{CC} = +5V ±5%, I_{SOURCE} = 200µA
Floating State Leakage Current					
(Pins 8–15)	±1	±1	±1	µA max	V_{OUT} = 0V to V_{CC}
Floating State Output Capacitance	15	15	15	pF max	
CONVERSION TIME[5]					
With External Clock	100	100	100	µs min	f_{CLK} = 140kHz
With Internal Clock, T_A = +25°C	100/150	100/150	100/150	µs min/max	Using recommended clock components as shown in Figure 6.
POWER REQUIREMENTS[6]					
V_{DD}	+15	+15	+15	V NOM	±5% for specified performance
V_{SS}	−5	−5	−5	V NOM	±5% for specified performance
V_{CC}	+5	+5	+5	V NOM	±5% for specified performance
I_{DD}	7.5	7.5	7.5	mA max	Typically 4mA with V_{DD} = +15V
I_{SS}	7.5	7.5	7.5	mA max	Typically 3mA with V_{SS} = −5V
I_{CC}	100	100	100	µA typ	V_{IN} = V_{IL} or V_{IH}
	1.0	1.0	1.0	mA max	
Power Dissipation	75	75	75	mW typ	$\overline{WR}$ = $\overline{RD}$ = $\overline{CS}$ = $\overline{BUSY}$ = Logic HIGH

NOTES

[1]Temperature Range as follows: K Version; 0 to +70°C
B Version; −25°C to +85°C
T Version; −55°C to +125°C

[2]Includes Full Scale Error, Offset Error and Relative Accuracy.

[3]Sample tested to ensure compliance.

[4]I_{SINK} for $\overline{BUSY}$ (pin 20) is 1.0 milliamp.

[5]Conversion Time includes autozero cycle time.

[6]Power supply current is measured when AD7578 is inactive i.e., $\overline{WR}$ = $\overline{RD}$ = $\overline{CS}$ = $\overline{BUSY}$ = Logic HIGH.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +15V, V_{CC} = +5V, V_{SS} = −5V, V_{REF} = +5V)

Parameter	Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (K & B Grades)	Limit at T_{min}, T_{max} (T Grade)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2(INT)[2]	200	240	280	ns min	$\overline{WR}$ Pulse Width (Internal Clock Operation)
t_2(EXT)[2]	10	10	10	μs min	$\overline{WR}$ Pulse Width (External Clock Operation)
t_3	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_4	130	160	200	ns typ	
	200	250	300	ns max	$\overline{WR}$ to $\overline{BUSY}$ Propagation Delay
t_5	0	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Setup Time
t_6	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_7	200	240	280	ns min	$\overline{RD}$ Pulse Width
t_8	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_9	50	50	50	ns min	BYSL to $\overline{RD}$ Setup Time
t_{10}	0	0	0	ns min	BYSL to $\overline{RD}$ Hold Time
t_{11}[3]	150	180	200	ns typ	
	200	240	280	ns max	$\overline{RD}$ to Valid Data (Bus Access Time)
t_{12}[4]	20	20	20	ns min	$\overline{RD}$ to Three State Output
	130	160	180	ns max	(Bus Relinquish Time)

NOTES
[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with $t_r = t_f = 20$ns (10% to 90% of +5V) and timed from a voltage level of +1.6V. Data is timed from V_{OH}, V_{OL}.
[2]When using an external clock source the $\overline{WR}$ pulse width must be extended to provide the minimum auto-zero cycle time of 10μs. See "External Clock Operation".
[3]t_{11} is measured with the load circuits of Figure 3 and defined as the time required for an output to cross 0.8V or 2.4V.
[4]t_{12} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 4.
Specifications subject to change without notice.

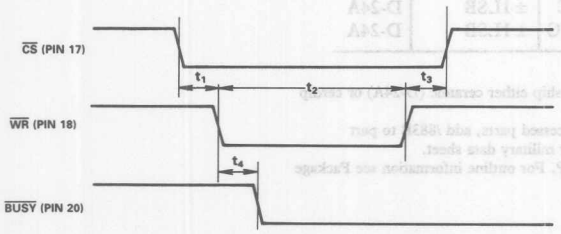
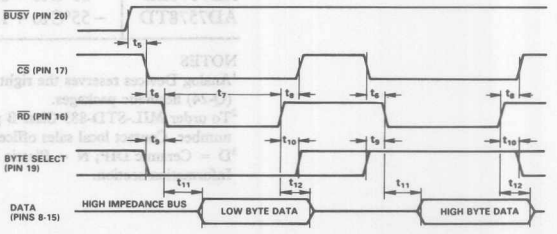
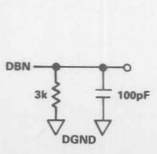


Figure 1. Start Cycle Timing

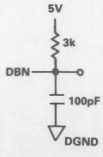


NOTES
THE TWO-BYTE CONVERSION RESULT CAN BE READ IN EITHER ORDER. FIGURE IS FOR LOW BYTE, HIGH BYTE ORDER.
IF BYSL CHANGES WHILE CS & RD ARE LOW THE DATA WILL CHANGE TO REFLECT THE BYSL INPUT.

Figure 2. Read Cycle Timing

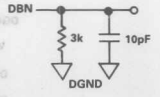


a. High-Z to V_{OH}

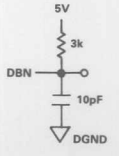


b. High-Z to V_{OL}

Figure 3. Load Circuits for Access Time Test (t_{11})



a. V_{OH} to High-Z



b. V_{OL} to High-Z

Figure 4. Load Circuits for Output Float Delay Test (t_{12})

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} to DGND	−0.3V, +17V
V_{SS} to DGND	+0.3V, −7V
AGND to DGND	−0.3V, V_{REF} +0.3V
V_{CC} to DGND	−0.3V, V_{DD} +0.3V
V_{REF} to AGND	−0.3V, V_{DD} +0.3V
AIN to AGND	−0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND (Pins 16-19, 21)	−0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND (Pins 8-15, 20)	−0.3V, V_{DD} +0.3V
Operating Temperature Range	
Commercial (K Version)	0 to +70°C
Industrial (B Version)	−25°C to +85°C
Extended (T Version)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C
Power Dissipation (Any Package) to +75°C	1,000mW
Derate above +75°C by	10mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



ORDERING GUIDE

Model[1, 2]	Temperature Range	Total Unadjusted Error T_{MIN} −T_{MAX}	Package Option[3]
AD7578KN	0°C to +70°C	±1LSB	N-24
AD7578BD	−25°C to +85°C	±1LSB	D-24A
AD7578TD	−55°C to +125°C	±1LSB	D-24A

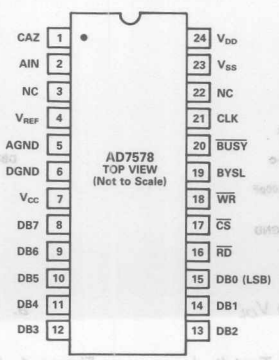
NOTES

[1]Analog Devices reserves the right to ship either ceramic (D-24A) or cerdip (Q-24) hermetic packages.

[2]To order MIL-STD-883 Class B processed parts, add /883B to part number. Contact local sales office for military data sheet.

[3]D = Ceramic DIP; N = Plastic DIP. For outline information see Package Information section.

DIP PIN CONFIGURATION



NC = NO CONNECT

PIN	MNEMONIC	DESCRIPTION
1	CAZ	Autozero Capacitor Input. Connect other side of capacitor to AGND.
2	AIN	Analog Input
3	N/C	No Connect pin
4	V_{REF}	Voltage reference input. The AD7578 is specified with $V_{REF} = +5.0V$.
5	AGND	Analog Ground
6	DGND	Digital Ground
7	V_{CC}	Logic Supply. For $V_{CC} = +5V$ digital inputs and outputs are TTL compatible.
8-15		Three state data outputs. They become active when $\overline{CS}$ & $\overline{RD}$ are brought low. Individual pin function is dependent upon the Byte Select (BYSL) input.

DATA BUS OUTPUT, $\overline{CS}$ & $\overline{RD}$ = LOW

	BYSL = HIGH	BYSL = LOW
Pin 8	BUSY[1]	DB7
Pin 9	LOW[2]	DB6
Pin 10	LOW[2]	DB5
Pin 11	LOW[2]	DB4
Pin 12	DB11 (MSB)	DB3
Pin 13	DB10	DB2
Pin 14	DB9	DB1
Pin 15	DB8	DB0 (LSB)

[1]BUSY (Pin 8) is a converter status flag and is HIGH during a conversion.
[2]Pins 9-11 output a logic LOW when BYSL is HIGH.
DB11–DB0 are the 12-bit conversion results, DB11 is the MSB.

16	$\overline{RD}$	READ input. This active LOW signal, in combination with $\overline{CS}$, is used to enable the output data three-state drivers.
17	$\overline{CS}$	CHIP SELECT Input. Decoded device address, active LOW. Used in combination with either $\overline{RD}$ or $\overline{WR}$ for control.
18	$\overline{WR}$	WRITE Input. This active LOW signal, in combination with $\overline{CS}$, is used to start a new conversion. When the AD7578 internal clock is used, the minimum $\overline{WR}$ pulse width is t2 (INT). When an external clock source is used, the minimum $\overline{WR}$ pulse width must be extended to include the autozero cycle time. For external clock operation, the minimum $\overline{WR}$ pulse width is t2 (EXT).
19	BYSL	BYTE SELECT. This control input determines whether the high or low byte of data is placed on the output data bus during a data READ operation ($\overline{CS}$ & $\overline{RD}$ LOW). See description of pins 8-15.
20	$\overline{BUSY}$	BUSY indicates converter status. $\overline{BUSY}$ is LOW during conversion, otherwise $\overline{BUSY}$ is held at a logic HIGH.
21	CLK	CLOCK Input for internal/external clock operation. Internal : Connect R_{CLK} and C_{CLK1}/C_{CLK2} timing components. See Figure 6 and Figure 7. External : Connect external 74HC compatible clock source as shown in Figure 8.
22	N/C	No connect pin.
23	V_{SS}	Negative supply, −5V.
24	V_{DD}	Positive supply, +15V.

Operating Information

OPERATIONAL DIAGRAM

An operational diagram for the AD7578 is shown in Figure 5. The only passive components required are the autozero capacitor C_{AZ} and timing components R_{CLK}, C_{CLK1} & C_{CLK2} for the internal clock oscillator. If the AD7578 is to be used with an external clock source, then only C_{AZ} is required. Individual pin functions are described in detail on the previous page.

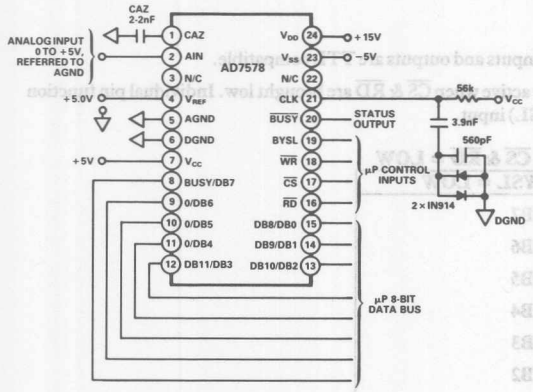


Figure 5. AD7578 Operational Diagram

INTERNAL CLOCK OPERATION

The clock circuitry for internal clock operation is shown in Figure 6 and the AD7578 operating waveforms are shown in Figure 7.

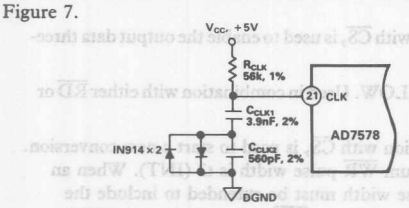


Figure 6. Circuitry Required for Internal Clock Operation

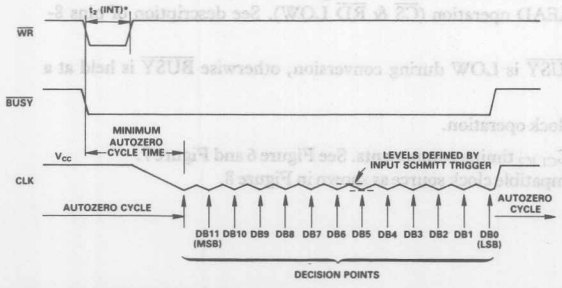


Figure 7. Operating Waveforms – Internal Clock

Between conversions ($\overline{BUSY}$ = HIGH) the AD7578 is in the autozero cycle. When $\overline{WR}$ goes LOW (with $\overline{CS}$ LOW) to start a new conversion, the autozero capacitor C_{AZ} charges to AIN – V_{OS} where V_{OS} is the input offset voltage of the autozero comparator.

A minimum time of 10µs is required for this autozero cycle. In applications using the internal clock oscillator, it is not necessary for $\overline{WR}$ to remain LOW for this period of time since it is automatically provided by the AD7578. This is achieved by switching a constant current load across the clock capacitors, C_{CLK1} and C_{CLK2}, causing the voltage at the CLK input pin to slowly decay from V_{CC}. This occurs after $\overline{WR}$ returns HIGH. The Schmitt trigger circuit monitoring the voltage on the CLK input ends the autozero cycle when its LOW input trigger level is reached. At this point, the constant current load across the clock capacitors is removed allowing them to charge towards V_{CC} via R_{CLK}. When the voltage at the CLK input reaches the HIGH trigger level, the constant current load is replaced across C_{CLK1} and C_{CLK2}. The MSB decision is made when the LOW trigger level is reached. This cycle repeats itself 12 times to provide 12 clock pulses for the conversion cycle. The circuit arrangement of Figure 6 provides the relatively slow autozero cycle time at the beginning of a conversion while allowing the clock oscillator to speed up once the autozero cycle is complete.

EXTERNAL CLOCK OPERATION

For external clock operation R_{CLK}, C_{CLK1} and C_{CLK2} are discarded and the CLK input is driven from a 74HC compatible clock source. The mark/space ratio of the external clock can vary from 40/60 to 60/40. The AD7578 $\overline{WR}$ pulse width must now be extended to provide the minimum autozero cycle time of 10µs since this is no longer provided automatically by the AD7578. Referring to the operating waveforms of Figure 9, the minimum $\overline{WR}$ pulse width when using an external clock source is t_2 (EXT). The $\overline{CS}$ input must now remain valid for the extended $\overline{WR}$ pulse width. One approach to stretching the available µP signals is shown in the general 8-bit µP interface circuit of Figure 20. It is not necessary to synchronize the external clock source with the extended $\overline{WR}$ pulse width, the MSB decision being made on the second falling edge of the clock input after the $\overline{WR}$ input returns HIGH.

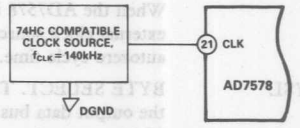


Figure 8. External Clock Operation

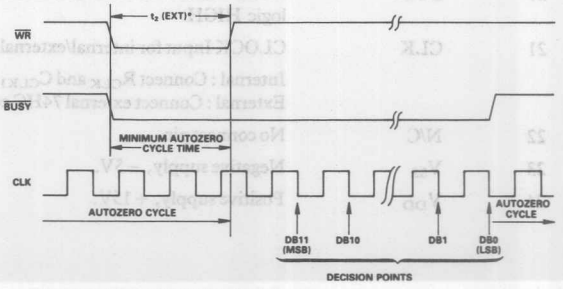


Figure 9. Operating Waveforms – External Clock

READING DATA

The 12-bit conversion data plus a converter status flag are available over an 8-bit wide data bus. Data is transferred from the AD7578 in right-justified format (i.e., the LSB is the most right-hand bit in a 16-bit word). Two READ operations are required, the Byte Select (BYSL) input determining which byte–8 least significant bits or 4 most significant bits plus status flag–is to be read first.

Since the AD7578 uses the successive approximation register (SAR) to hold conversion results (refer to Functional Diagram), it is necessary to wait until a conversion is finished before reading valid 12-bit data. Executing a READ instruction (HIGH or LOW byte) to the AD7578 while a conversion is in progress will place the existing contents of the SAR onto the data bus. Three different approaches can ensure valid 12-bit data is available for reading.

1. Insert a software delay greater than the ADC conversion time between the conversion start instruction and the data read instructions.
2. At user-defined intervals after a conversion start instruction, poll the internal converter status flag, BUSY. This signal is available on pin 8 during a HIGH byte READ instruction and is the most left-hand bit in a 16-bit right-justified word. The status bit can be shifted into a microprocessor's accumulator-carry position for testing (BUSY is HIGH during conversion).
3. Use the externally available $\overline{\text{BUSY}}$ (pin 20) signal as an interrupt to the microprocessor. This signal is LOW during a conversion and returns HIGH at conversion end.

Executing a WRITE instruction to the AD7578 while a conversion is in progress will restart the conversion.

COMPONENT SELECTION

1. Autozero Capacitor, C_{AZ}
   The autozero capacitor must be a low leakage, low dielectric absorption type such as polystyrene, polypropylene or teflon. To minimize noise connect the outside foil of C_{AZ} to AGND (pin 5), the analog system ground. C_{AZ} should be 2,200pF.
2. Clock Oscillator Components, R_{CLK}, C_{CLK1} and C_{CLK2}
   Clock pulses are generated by the action of series connected capacitors, C_{CLK1} and C_{CLK2} charging through an external resistor R_{CLK} and discharging through an internal switch. Nominal conversion time versus temperature for the recommended R_{CLK} and C_{CLK1}/C_{CLK2} combination is shown in Figure 10. Due to process variations, the actual operating frequency for this R_{CLK} and C_{CLK1}/C_{CLK2} combination can vary from device to device by up to 20%. For this reason, Analog Devices recommends using an external clock in the following situations:
   a. Applications requiring a conversion time which is within 20% of 100μs, the minimum conversion time for specified accuracy (a 140kHz clock frequency gives a 100μs conversion time).
   b. Applications which cannot accommodate conversion time differences which may occur due to unit clock frequency variations or temperature variations.

   It is possible to replace the fixed R_{CLK} resistor with a 50k potentiometer in series with a fixed 22kΩ resistor to allow individual adjustment of internal clock frequency in applications where 100μs conversion times are required. Reducing the value of R_{CLK} from 56k to 47k decreases the conversion time by typically 15μs.

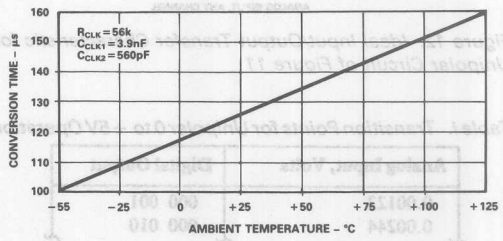


Figure 10. Typical Conversion Time vs. Temperature Using Internal Clock

APPLYING THE AD7578

The high input impedance of the analog input, AIN, allows simple analog interfacing. Zero to +5V signal sources can be connected directly to the analog input without additional buffering for source impedances up to 5kΩ (see Figure 11). The input/output transfer characteristic and transition points for this input signal range are shown in Figure 12 and Table I respectively. The designed transition points on the AD7578 transfer characteristic occur on integer multiples of 1LSB. The output code is Natural Binary with 1LSB = (F.S.) (1/4096) = (5/4096)V = 1.22mV.

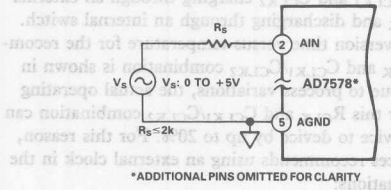


Figure 11. Unipolar 0 to +5V Operation

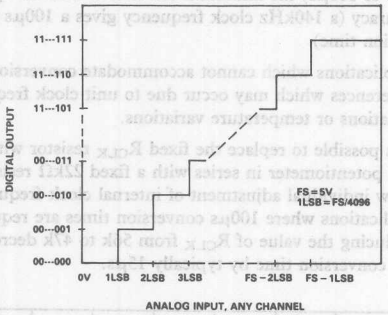


Figure 12. Ideal Input/Output Transfer Characteristic for Unipolar Circuit of Figure 11

Table I. Transition Points for Unipolar 0 to +5V Operation

Analog Input, Volts	Digital Output
0.00122	000 001
0.00244	000 010
2.49878	011 111
2.50000	100 000
2.50122	100 001
4.99756	111 110
4.99878	111 111

Signal ranges other than 0 to +5V are easily accommodated by using resistor divider networks to produce 0 to +5V signal ranges at the AD7578 input pins. Figure 13 shows a divider network to allow an input signal range of 0 to +10V. The input resistors must be selected to match within 0.01% and should be the same type and from the same manufacturer so that their temperature coefficients match. Note that since the source impedance has not been included in the resistor divider ratio, it must now be as low as possible. For Figure 13 with a source impedance of 0.5Ω the maximum error across the network is approximately 0.5LSB. The LSB size is (F.S.)(1/4096) = (10/4096)V = 2.44mV.

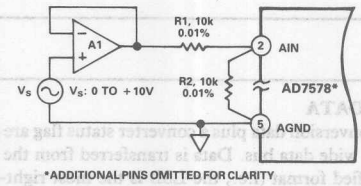


Figure 13. Unipolar 0 to +10V Operation

Bipolar signal ranges of −5V to +5V are accommodated by referencing the resistor divider network to V_{REF} as shown in Figure 14. With the resistor values shown, the signal source must be capable of sinking 0.5mA. The input/output transfer characteristic and transition points for this ±5V signal range are shown in Figure 15 and Table II respectively. The output code is Offset Binary with an LSB size of (F.S.)(1/4096) = (10/4096)V = 2.44mV.

With an analog input (V_S) of −1.22mV, the input offset voltage of A1 should be adjusted until the ADC output flickers between 0111 1111 1111 and 1000 0000 0000. Alternatively the −1/2LSB signal offset can be included in the signal conditioning electronics.

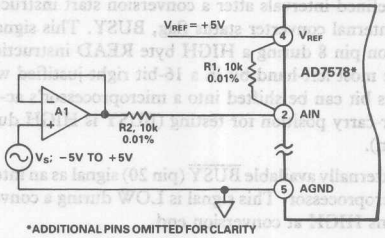


Figure 14. Bipolar −5V to +5V Operation

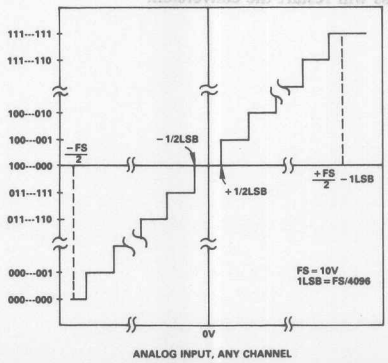


Figure 15. Ideal Input/Output Transfer Characteristic for Bipolar Circuit of Figure 14

Table II. Transition Points for Bipolar −5V to +5V Operation

Analog Input, Volts	Digital Output
−4.99878	000 001
−4.99634	000 010
−0.00122	100 000
+0.00122	100 001
+4.99389	111 110
+4.99634	111 111

Applications

Power Supply Decoupling: All power supplies to the AD7578 should be bypassed with either 10μF tantulum or electrolytic capacitors. To ensure good high frequency performance, each capacitor should be bypassed with an 0.01μF disc ceramic capacitor. All capacitors should be placed as close as possible to the AD7578.

Reference Circuit: Figure 16 shows how to configure an AD584LH to produce a reference voltage of 5.00V. R2 provides a typical adjustment range of ±75mV. The AD584LH will contribute less than 1LSB of gain error over the commercial temperature range.

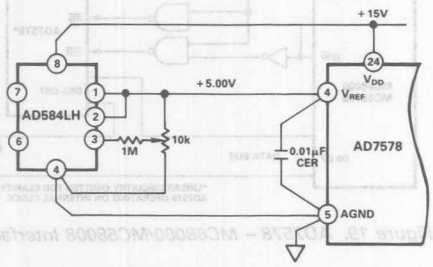


Figure 16. AD584LH as Reference Generator

Transient currents flow at the V_{REF} input during a conversion. To avoid dynamic errors place a 0.01μF disc ceramic capacitor from the V_{REF} pin to AGND.

Proper Layout: Layout for a printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or close to the autozero capacitor. The analog inputs, the reference input and the autozero input should be screened by AGND.

A single point analog ground separate from the logic system ground should be established at pin 5 (AGND) or as close as possible to the AD7578. This single point analog ground should be connected to the digital system ground, to which pin 6 (DGND) is connected, at one point only and as close to the AD7578 as possible. The autozero capacitor, bypass capacitors for the reference input and the analog supplies, AIN common and any input signal screening should be returned to the analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible.

Noise: Input signal leads to AIN and signal return leads from AGND (pin 5) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible, a shielded cable between source and ADC is recommended. Also since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

In applications where the AD7578 data outputs are connected to a continuously busy (and noisy) microprocessor bus it is possible to get LSB errors in conversion results. These errors are due to feedthrough from the microprocessor bus to the autozero comparator. The problem exists only for ceramic package versions of the AD7578, the electrically isolated metal lid acting like a conductor to distribute the digital noise around the package.

Grounding the lid to DGND eliminates this problem. Alternatively the AD7578 can be isolated from the microprocessor bus by means of three-state buffers.

Microprocessor Interfacing

MICROPROCESSOR INTERFACING

When the AD7578 is used with its own internal clock oscillator, microprocessor interfacing is straightforward and requires at most a few external gates (see Figures 17 through 19, 21 and 22). When the AD7578 is used with an external clock source, additional circuitry is required to extend the μP control signals (see Figure 20).

MC6800, MC6809 and 6502 MICROPROCESSORS

A typical interface to the AD7578 with any of the above microprocessors is shown in Figure 17. The decoder can be enabled high using VMA in 6800 systems or enabled low by NOR'ing ϕ_0 and ϕ_2 in 6502 systems or by NOR'ing E and Q in 6809 systems. Address line A2 of the 6800 has been tied to BYSL of the AD7578. Assuming the AD7578 is assigned a memory block starting at address 8000H, a write instruction to any address in this block will start a conversion. To read the conversion results, it is necessary only to bring control inputs $\overline{CS}$ and $\overline{RD}$ low. The BYSL input (tied to A2 of the μP) determines whether the data high or low byte is placed onto the 8-bit data bus. A read instruction to address 8000H will result in the low byte of data being transferred to the μP (BYSL = Low). Similarly a read instruction to any address having A2 HIGH and within the assigned memory block, e.g., 8004H, transfers the high byte of data to the μP. The converter status flag BUSY can be polled at intervals to check whether the present conversion has finished and valid 12-bit data is available. This is accomplished by the following instructions on the 6800:

```
LDA   A   $8004     Load Flag from AD7578
ASL   A             Shift Flag into Carry
BCC       FETCH     Branch to Data Fetch
                    Subroutine if BUSY is LOW
```

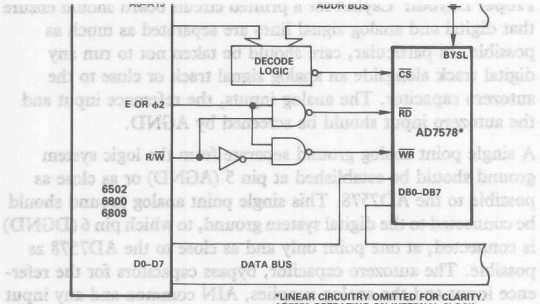


Figure 17. AD7578 – MC6800, 6809, 6502 Interface

8085A, Z80 MICROPROCESSORS

A typical interface to either of these microprocessors is shown in Figure 18. Not shown in the figure is the 8-bit latch required to demultiplex the 8085A common address/data bus. This interface uses slightly different low-level address decoding than the previous interface. Address line A0 of the µP has been tied to BYSL of the AD7578. This allows the 16-bit data move instructions on both the 8085A and the Z80 to be used when reading conversion results. Assuming the AD7578 is again assigned a memory block starting at address 8000H, a write instruction to any address in this block will start a conversion. The 12-bit conversion results can be read (low byte first then high byte) by a single read instruction;

On the 8085A

LHLD 8000

moves the conversion results into register pair HL

On the Z80

LD BC, (8000)

moves the conversion results into register pair BC

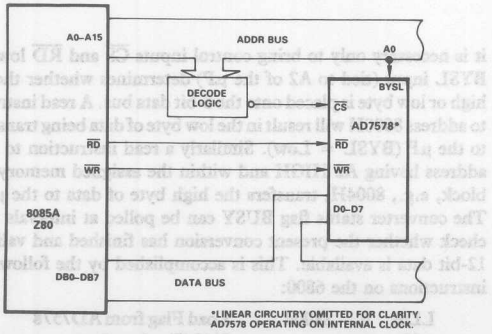


Figure 18. AD7578 – 8085A, Z80 Interface

MC68000, MC68008 MICROPROCESSOR

Figure 19 shows an AD7578–MC68000/MC68008 interface. Address line A1 of the µP has been connected to BYSL of the AD7578. With the simple decoding logic shown in Figure 19, the AD7578 is decoded in a memory block from C000H to FFFFH. A write instruction to any one of these addresses will start a conversion, i.e.,

starts a conversion. When the conversion is complete, the µP acquires the result by reading from the AD7578, i.e,

MOVEP. W $000 (A2), D0

This instruction places the conversion data in the D0 register of the µP. Address register A2 should contain an odd-order address (having A1 high) for the AD7578, e.g., $C003.

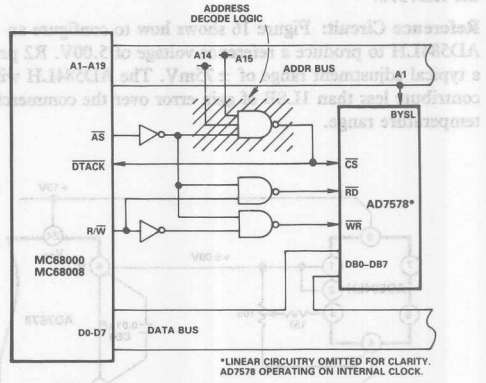


Figure 19. AD7578 – MC68000/MC68008 Interface

MICROPROCESSOR INTERFACE TO AD7578 WITH EXTERNAL CLOCK

Figure 20 shows the additional circuitry generally required to interface an 8-bit µP to the AD7578 operating from an external clock source. During a write operation, the 74121 monostable (one-shot) is triggered to latch the low level on the $\overline{CS}$ input into the 7477, a 4-bit bistable latch. The monostable timing components (not shown in Figure 20) should be chosen to provide an output pulse width corresponding to t_2 (EXT), the minimum autozero cycle time. To avoid any possibility of spurious triggering, the monostable should be enabled by a valid memory address signal. During a data read cycle, the 7477 latch is transparent and data is read normally. Note that the µP write and read cycle times are unaffected by the interface circuitry.

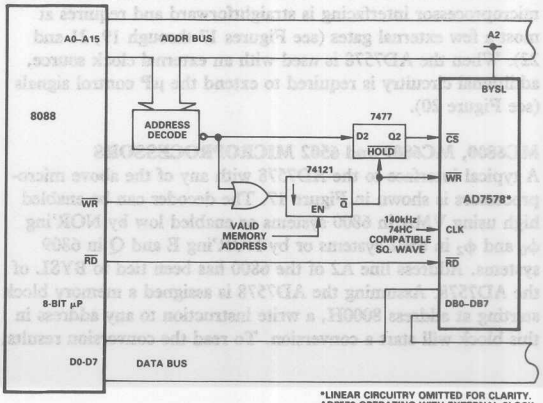


Figure 20. Interface to AD7578 Using External Clock

8088, 8086 MICROPROCESSORS

Figure 21 shows an AD7578–8088 interface.

Address line A0 of the μP is connected to BYSL of the AD7578. With the simple decoding shown in Figure 21 the AD7578 is decoded in a memory block from 4000H to 7FFFH.

A write instruction to any one of these addresses will start a conversion, i.e,

MOV 4004, AX

starts a conversion. When the conversion is finished the 8088 acquires the result by reading from the AD7578, i.e.,

MOV AX, 4000

places the conversion data in the accumulator.

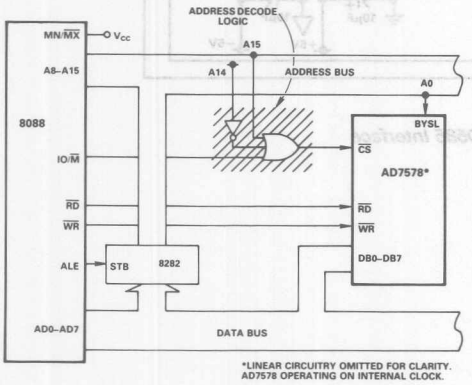


Figure 21. AD7578 – 8088 Interface

Figure 22 shows an AD7578–8086 interface. Address line A1 of the μP is connected to BYSL of the AD7578. The AD7578 is again decoded in a memory block from 4000H to 7FFFH.

A write instruction to any one of these addresses will start a conversion, i.e,

MOV 4008, AX

starts a conversion. When the conversion is finished, the 8086 acquires the result by reading from the AD7578 in two read cycles, i.e.,

MOV AL, 4000
MOV AH, 4002

places the conversion data in the accumulator.

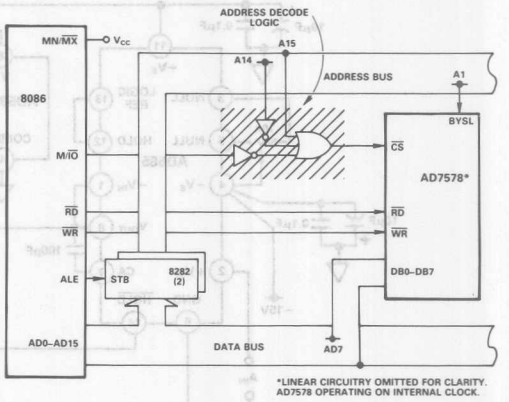


Figure 22. AD7578 – 8086 Interface

AD7578-AD585 SAMPLE-HOLD INTERFACE

Figure 23 shows an AD585 Sample-Hold Amplifier driving the analog input of the AD7578. At a sampling frequency of 8kHz the maximum input signal frequency is 4kHz. The AD7578 is configured for bipolar operation to allow an input signal swing of ±5V. No clock components are shown for the AD7578 but the conversion time should be adjusted for 100 microseconds. With an external hold capacitor of 100pF, the acquisition time for the sample-hold amplifier is 10 microseconds. The circuit operates from 0°C to +70°C.

To take a sample of the input, a WRITE instruction is executed to the AD7578 control inputs. The converter busy flag, $\overline{\text{BUSY}}$, is driven low indicating that a conversion is in progress. The falling edge of this $\overline{\text{BUSY}}$ signal places the sample-hold amplifier into the HOLD mode "freezing" the input signal to the AD7578. After 100 microseconds the conversion is finished and the $\overline{\text{BUSY}}$ signal is brought high. This allows a time of 25 microseconds for the AD585 to come out of the hold mode and acquire the input signal in time for the next sample. Between the end of one conversion and the start of the next, the conversion results must be read from the converter.

Careful circuit layout and power supply decoupling are necessary to obtain maximum performance from the system. Decoupling capacitors in the diagram are all 10μF electroytics in parallel with 0.01μF disc ceramics.

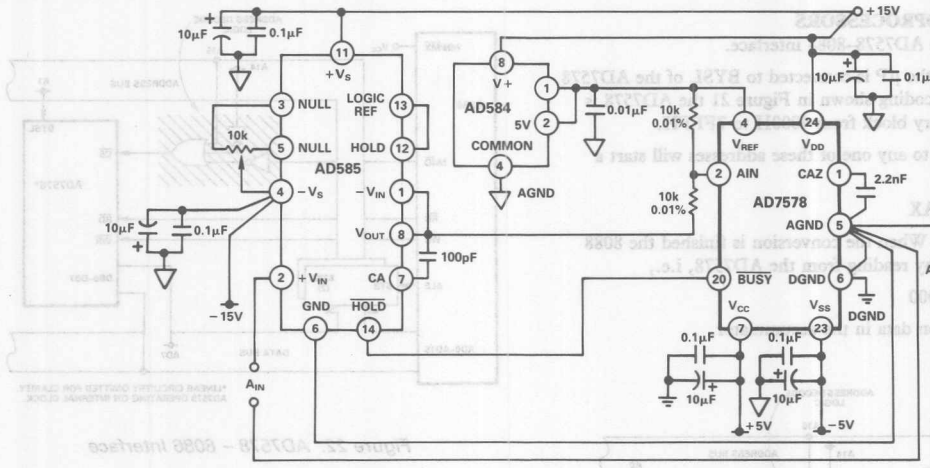
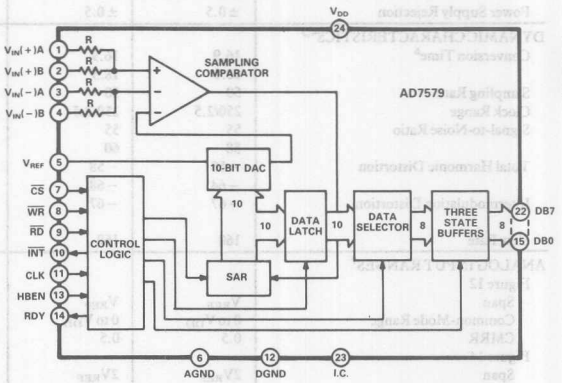


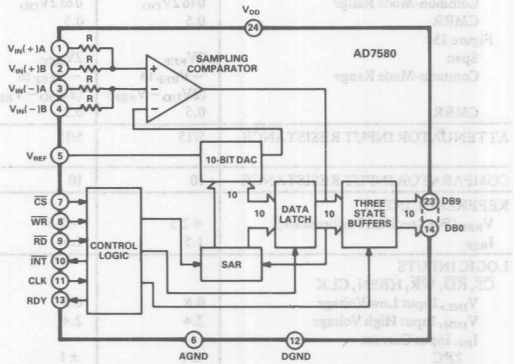
Figure 23. AD7578 – AD585 Interface

LC²MOS
10-Bit Sampling A/D Converters
AD7579/AD7580

FEATURES
- 20μs Conversion Time
- On-Chip Sample-Hold
- 50kHz Sampling Rate
- 25kHz Full-Power Input Bandwidth
- Choice of Data Formats
- Single +5V Supply
- Low Power (50mW)
- Skinny 24-Pin DIP and 28-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAMS





GENERAL DESCRIPTION

The AD7579 and AD7580 are 10-bit, successive approximation ADCs. They have differential analog inputs that will accept unipolar or bipolar input signals while operating from only a single +5V supply. Input ranges of 0 to +2.5V, 0 to +5V and ±2.5V are possible with no external signal conditioning. Only an external 2.5V reference and clock and control signals are required to make them operate.

With conversion time of less than 20μs and an on-chip sample-hold amplifier, the devices are ideally suited for digitizing ac signals. The maximum sampling rate is 50kHz, giving an input bandwidth of 25kHz. The parts are specified not only with traditional static specifications such as linearity and offset but also with dynamic specifications (SNR, Harmonic Distortion, IMD).

The AD7579 and AD7580 are microprocessor-compatible with standard microprocessor control inputs ($\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RDY, $\overline{INT}$) and data outputs capable of interfacing to high-speed data buses. There is a choice of data formats, with the AD7579 offering an (8+2) read and the AD7580 offering a 10-bit parallel word.

Space saving and low power are also features of these devices. They dissipate less than 50mW from a single +5V supply and are offered in a 0.3″, 24-pin package and in plastic/ceramic chip carrier for surface mounting.

PRODUCT HIGHLIGHTS

1. 20μs conversion time with on-chip sample-hold makes the AD7579 and AD7580 ideal for audio and higher bandwidth signals, e.g., modem applications.
2. Differential analog inputs can accept unipolar or bipolar input signals, but only a single, +5V power supply is needed.
3. Versatile and easy-to-use digital interface has fast bus access/relinquish times, allowing connection to most popular microprocessors.

AD7579/AD7580—SPECIFICATIONS

(V_{DD} = +5V ± 5%, V_{REF} = +2.5V, AGND = DGND = 0V; f_{CLK} = 2.5MHz; All specifications T_{MIN} to T_{MAX} unless otherwise noted. Test conditions as in Figure 12 unless otherwise stated).

Parameter	J, A Versions	K, B Versions	S Version	Units	Conditions/Comments
STATIC CHARACTERISTICS					These specifications apply for the
Resolution	10	10	10	Bits	three Analog Input Ranges.
					See Differential Applications.
Integral Nonlinearity	±1	±1/2	±1	LSB max	No missing codes guaranteed over the
Differential Linearity Error	±0.9	±0.9	±0.9	LSB max	full temperature range[2].
Full-Scale Error	±5	±5	±5	LSB max	
Zero Code Error[3]	±2	±1	±2	LSB max	Connected as in Figure 12.
	±3	±2	±3	LSB max	Connected as in Figure 14 or 15.
Power Supply Rejection	±0.5	±0.5	±0.5	LSB max	4.75V<V_{DD}<5.25V
DYNAMIC CHARACTERISTICS[4,5]					
Conversion Time[6]	16.9	16.9	16.9	µs min	f_{CLK} = 2.5MHz, t_{WR} = 100ns.
	18.5	18.5	18.5	µs max	See Functional Description.
Sampling Rate	50	50	50	kHz max	
Clock Range	250/2.5	250/2.5	250/2.5	kHz min/MHz max	
Signal-to-Noise Ratio	55	55	55	dB min	See Terminology. T_A = 25°C.
	58	60	58	dB typ	
Total Harmonic Distortion	−58	−58	−58	dB max	T_A = 25°C.
	−64	−68	−64	dB typ	
Intermodulation Distortion	−67	−67	−67	dB typ	This is characterized to both SMPTE
					and CCITT standards. T_A = 25°C.
Slew Rate	160	160	160	mV/µs max	See Terminology
ANALOG INPUT RANGES[7]					
Figure 12					AD7579/AD7580 connected as in Figure 12
Span	V_{REF}	V_{REF}	V_{REF}	V max	
Common-Mode Range	0 to V_{DD}	0 to V_{DD}	0 to V_{DD}	V max	
CMRR	0.5	0.5	0.5	LSB/V typ	
Figure 14					AD7579/AD7580 connected as in Figure 14
Span	$2V_{REF}$	$2V_{REF}$	$2V_{REF}$	V max	
Common-Mode Range	0 to $2V_{DD}$	0 to $2V_{DD}$	0 to $2V_{DD}$	V max	
CMRR	0.5	0.5	0.5	LSB/V typ	
Figure 15					AD7579/AD7580 connected as in Figure 15
Span	$2V_{REF}$	$2V_{REF}$	$2V_{REF}$	V max	
Common-Mode Range	$-V_{REF}$ to	$-V_{REF}$ to	$-V_{REF}$ to	V max	
	($2V_{DD} - V_{REF}$)	($2V_{DD} - V_{REF}$)	($2V_{DD} - V_{REF}$)		
CMRR	0.5	0.5	0.5	LSB/V typ	
ATTENUATOR INPUT RESISTANCE	5/15	5/15	5/15	kΩ min/kΩ max	10kΩ typical. Resistance measured between $V_{IN}(+)A$, $V_{IN}(+)B$ or $V_{IN}(-)A$, $V_{IN}(-)B$
COMPARATOR INPUT RESISTANCE	10	10	10	MΩ min	AD7579/AD7580 connected as in Figure 12
REFERENCE INPUT					
V_{REF} (For Specified Performance)	+2.5	+2.5	+2.5	V	±5%
I_{REF}	1.5	1.5	1.5	mA max	
LOGIC INPUTS					
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, HBEN, CLK					
V_{INL}, Input Low Voltage	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	V min	
I_{IN}, Input Current					
25°C	±1	±1	±1	µA max	V_{IN} = 0 or V_{DD}
T_{min} to T_{max}	±10	±10	±10	µA max	V_{IN} = 0 or V_{DD}
C_{IN}, Input Capacitance[4]	10	10	10	pF max	
LOGIC OUTPUTS					
DB0 to DB7 (DB9)					
V_{OL}, Output Low Voltage	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	4.0	4.0	4.0	V min	I_{SOURCE} = 400µA
Floating State Leakage Current	±1	±1	±10	µA max	V_{OUT} = 0 to V_{DD}
Floating State Output Capacitance[4]	10	10	10	pF max	
RDY, $\overline{INT}$					
V_{OL}, Output Low Voltage	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
POWER REQUIREMENT					
V_{DD}	+5	+5	+5	V	±5% for Specified Performance
I_{DD}	10	10	10	mA max	Typically 5mA with V_{DD} = +5V
Power Dissipation	50	50	50	mW max	

NOTES
[1]Temperature Ranges as follows:
J, K Versions; 0 to +70°C
A, B Versions; −25°C to +85°C
S Version; −55°C to +125°C
[2]Zero code error and gain error adjusted to zero.
[3]Zero code error is measured with respect to an ideal first code transition which occurs at 1/2LSB.
[4]Sample tested at 25°C to ensure compliance.
[5]These specifications apply for full-scale input signals up to 20kHz.
[6]Accuracy may degrade at conversion times other than those specified.
[7]$V_{IN}(+)$ must always be equal to or more positive than $V_{IN}(-)$, in Figures 12, 14, 15.
Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +5V ±5%, V_{REF} = +2.5V, AGND = DGND = 0V)

Parameter[2,3,4]	Limit at 25°C (All Grades)	Limit at T_{min}, T_{max} (J, K, A, B Grades)	Limit at T_{min}, T_{max} (S Grade)	Units	Test Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	40	50	50	ns min	$\overline{WR}$ Pulse Width
t_3	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_4	100	100	120	ns max	$\overline{WR}$ to $\overline{INT}$ Propagation Delay
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_6	t_{12}	t_{12}	t_{12}	ns min	$\overline{RD}$ Pulse Width
t_7	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_8	20	20	30	ns min	HBEN to $\overline{RD}$ Setup Time
t_9	10	10	10	ns min	HBEN to $\overline{RD}$ Hold Time
t_{10}	110	135	150	ns min	RDY Access Time
t_{11}	100	100	120	ns max	$\overline{RD}$ to $\overline{INT}$ Propagation Delay
t_{12}	110	135	150	ns max	Data Access Time After $\overline{RD}$
t_{13}	10	10	10	ns min	Data Hold Time, RDY Hold Time
	65	80	90	ns max	

NOTES
1. Timing specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with $t_R = t_F$ = 20ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.
2. t_4, t_{10}, t_{11} and t_{12} are measured with the load circuits of Figures 3 and 5 and defined as the time required for an output to cross 0.8V or 2.4V.
3. t_{13} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 4.
4. $\overline{INT}$ and RDY are open-drain outputs and need 3kΩ external pull-up resistors for operation.

Specifications subject to change without notice.

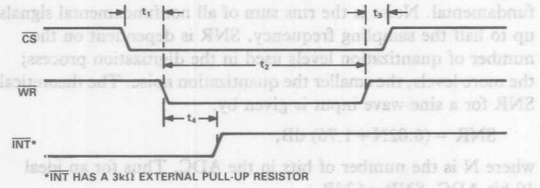


Figure 1. AD7579/AD7580 Start Cycle Timing

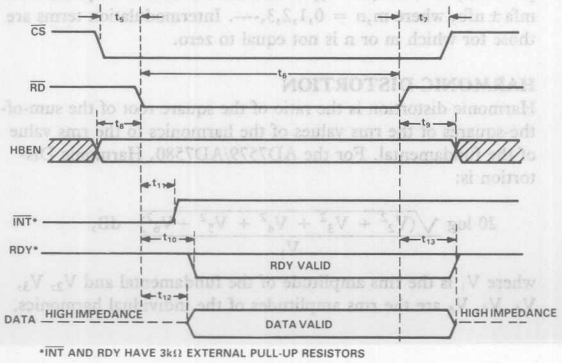
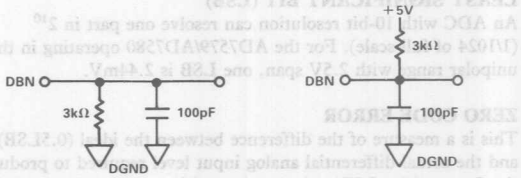
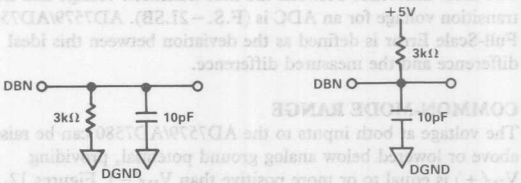


Figure 2. AD7579/AD7580 Read Cycle Timing



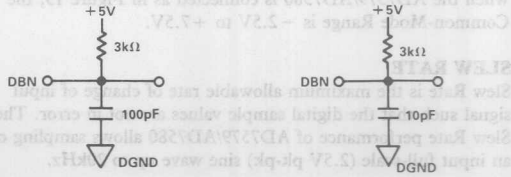
a. High-Z to V_{OH} *b. High-Z to V_{OL}*

Figure 3. Load Circuits for Access Time Tests (t_{12})



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 4. Load Circuits for Output Float Delay (t_{13})



a. High-Z to V_{OL} *b. V_{OL} to High-Z*

Figure 5. Load Circuit for $\overline{INT}$ Propagation Delays

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND	−0.3V to +7V
V_{DD} to DGND	+0.3V to +7V
AGND to DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND	−0.3V, V_{DD} +0.3V
CLK Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{REF} to AGND	−0.3V, V_{DD}
$V_{IN}(+)A$, $V_{IN}(+)B$ to AGND (Figure 12)	−0.3V, V_{DD} +0.3V
$V_{IN}(-)A$, $V_{IN}(-)B$ to AGND (Figure 12)	−0.3V, V_{DD} +0.3V
$V_{IN}(+)A$ to AGND (Figure 14)	−0.6V, $2V_{DD}$ +0.6V
$V_{IN}(-)A$ to AGND (Figure 14)	−0.6V, $2V_{DD}$ +0.6V
$V_{IN}(+)A$ to AGND (Figure 15)	$-V_{REF}$ −0.6V, $2V_{DD}$ $-V_{REF}$ +0.6V
$V_{IN}(-)A$ to AGND (Figure 15)	$-V_{REF}$ −0.6V, $2V_{DD}$ $-V_{REF}$ +0.6V
Operating Temperature Range	
Commercial (J, K Versions)	0 to +70°C
Industrial (A, B Versions)	−25°C to +85°C
Extended (S Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C
Power Dissipation (Any Package) to +75°C	450mW
Derates Above +75°C by	6mW/°C

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



TERMINOLOGY

LEAST SIGNIFICANT BIT (LSB)

An ADC with 10-bit resolution can resolve one part in 2^{10} (1/1024 of full scale). For the AD7579/AD7580 operating in the unipolar range with 2.5V span, one LSB is 2.44mV.

ZERO CODE ERROR

This is a measure of the difference between the ideal (0.5LSB) and the actual differential analog input level required to produce the first positive LSB code transition (00 . . . 00 to 00 . . . 01).

FULL-SCALE ERROR

The ideal difference between the first transition voltage and last transition voltage for an ADC is (F.S. − 2LSB). AD7579/AD7580 Full-Scale Error is defined as the deviation between this ideal difference and the measured difference.

COMMON-MODE RANGE

The voltage at both inputs to the AD7579/AD7580 can be raised above or lowered below analog ground potential, providing $V_{IN}(+)$ is equal to or more positive than $V_{IN}(-)$. Figures 12, 14, and 15 show circuits for various Analog Input Ranges. The Common-Mode Range represents the voltage extremes which can be applied to the circuits of Figure 12, 14 or 15. For example, when the AD7579/AD7580 is connected as in Figure 15, the Common-Mode Range is −2.5V to +7.5V.

SLEW RATE

Slew Rate is the maximum allowable rate of change of input signal such that the digital sample values are not in error. The Slew Rate performance of AD7579/AD7580 allows sampling of an input full-scale (2.5V pk-pk) sine wave up to 20kHz.

SIGNAL-TO-NOISE RATIO

Signal-to-Noise Ratio (SNR) is measured signal to noise at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine-wave input is given by:

$$SNR = (6.02N + 1.76)\ dB,$$

where N is the number of bits in the ADC. Thus for an ideal 10-bit ADC, SNR = 62dB.

INTERMODULATION DISTORTION

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa ± nfb, where m,n = 0,1,2,3,----. Intermodulation terms are those for which m or n is not equal to zero.

HARMONIC DISTORTION

Harmonic distortion is the ratio of the square root of the sum-of-the-squares of the rms values of the harmonics to the rms value of the fundamental. For the AD7579/AD7580, Harmonic Distortion is:

$$20 \log \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)}}{V_1}\ dB,$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, V_6 are the rms amplitudes of the individual harmonics.

ORDERING GUIDE

Model[1,2]	Temperature Range	INL	Package Option[3]
AD7579JN	0°C to +70°C	±1LSB	N-24
AD7579KN	0°C to +70°C	±1/2LSB	N-24
AD7579JP	0°C to +70°C	±1LSB	P-28A
AD7579KP	0°C to +70°C	±1/2LSB	P-28A
AD7579AQ	−25°C to +85°C	±1LSB	Q-24
AD7579BQ	−25°C to +85°C	±1/2LSB	Q-24
AD7579SQ	−55°C to +125°C	±1LSB	Q-24
AD7579SE	−55°C to +125°C	±1LSB	E-28A

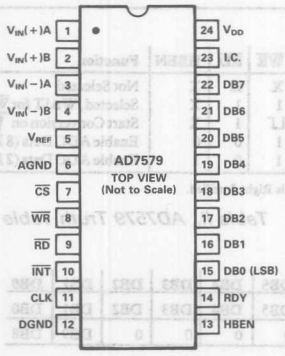
NOTES
[1]Analog Devices reserves the right to ship ceramic (D-24A) in lieu of cerdip (Q-24) hermetic packages.
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[3]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

Model[1,2]	Temperature Range	INL	Package Option[3]
AD7580JN	0°C to +70°C	±1LSB	N-24
AD7580KN	0°C to +70°C	±1/2LSB	N-24
AD7580JP	0°C to +70°C	±1LSB	P-28A
AD7580KP	0°C to +70°C	±1/2LSB	P-28A
AD7580AQ	−25°C to +85°C	±1LSB	Q-24
AD7580BQ	−25°C to +85°C	±1/2LSB	Q-24
AD7580SQ	−55°C to +125°C	±1LSB	Q-24
AD7580SE	−55°C to +125°C	±1LSB	E-28A

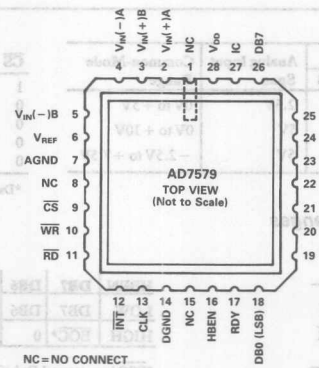
NOTES
[1]Analog Devices reserves the right to ship ceramic (D-24A) in lieu of cerdip (Q-24) hermetic packages.
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[3]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

PIN CONFIGURATIONS

DIP

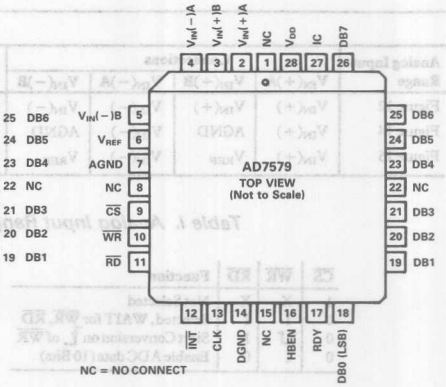


LCCC

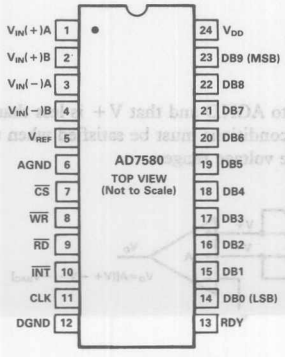


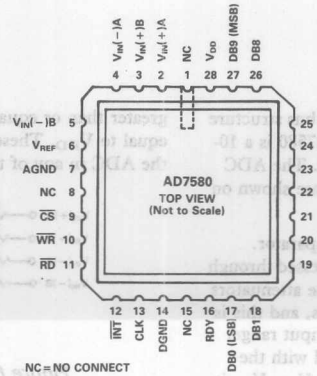
NC = NO CONNECT

PLCC

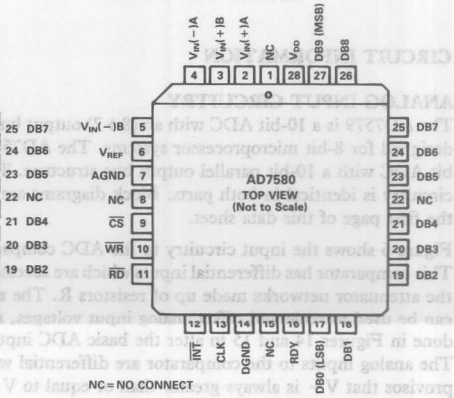


NC = NO CONNECT





NC = NO CONNECT



NC = NO CONNECT

PIN FUNCTION DESCRIPTION (DIP PACKAGE)

Mnemonic	Pin Number AD7579	Pin Number AD7580	Description
$V_{IN}(+)A$	1	1	Analog Input Pin.
$V_{IN}(+)B$	2	2	Analog Input Pin.
$V_{IN}(-)A$	3	3	Analog Input Pin.
$V_{IN}(-)B$	4	4	Analog Input Pin. The four analog input pins connect to the on-chip input attenuator (see Figure 6) and may be configured as in Table I for various input ranges.
V_{REF}	5	5	V_{REF} Input. This is nominally +2.5V.
AGND	6	6	Analog Ground
$\overline{CS}$	7	7	Chip Select Input.
$\overline{WR}$	8	8	Write Input. Used with $\overline{CS}$ to start conversion. See Tables II, III.
$\overline{RD}$	9	9	Read Input. Used with $\overline{CS}$ to read data. See Tables II, III.
$\overline{INT}$	10	10	Open Drain Output. High impedance during conversion. Goes low when conversion is complete.
CLK	11	11	Clock Input.
DGND	12	12	Digital Ground.
HBEN	13	–	High Byte Enable Input. Used in AD7579 for 2 Byte Reading. See Tables II, IV. Either the High Byte or the Low Byte may be read first.
RDY	14	13	Open Drain Output. This is accessed during Read Cycle. When accessed, it is low during conversion and high impedance when conversion is complete.
DB0-DB7	15-22	–	Three-State Data Outputs on AD7579. The data format is right justified.
DB0-DB9	–	14-23	Three-State Data Outputs on AD7580.
I.C.	23	–	Internal connection. This pin is connected internally on the AD7579. It should be left open and not used as a feed-through pin in double-sided printed circuit boards.
V_{DD}	24	24	Positive Power Supply. This is +5V nominal.

Analog Input Range	Connections $V_{IN}(+)A$	$V_{IN}(+)B$	$V_{IN}(-)A$	$V_{IN}(-)B$	Analog Input Span	Common-Mode Range
Figure 12	$V_{IN}(+)$	$V_{IN}(+)$	$V_{IN}(-)$	$V_{IN}(-)$	2.5V	0V to +5V
Figure 14	$V_{IN}(+)$	AGND	$V_{IN}(-)$	AGND	5V	0V to +10V
Figure 15	$V_{IN}(+)$	V_{REF}	$V_{IN}(-)$	V_{REF}	5V	−2.5V to +7.5V

Table I. Analog Input Ranges

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Function
1	X	X	Not Selected
0	1	1	Selected, WAIT for $\overline{WR}$, $\overline{RD}$
0	⊔	1	Start Conversion on ↓ of $\overline{WR}$
0	1	0	Enable ADC data (10 Bits)

Table III. AD7580 Truth Table

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	HBEN	Function
1	X	X	X	Not Selected
0	1	1	X	Selected, WAIT for $\overline{WR}$, $\overline{RD}$
0	⊔	1	X	Start Conversion on ↓ of $\overline{WR}$
0	1	0	0	Enable ADC Data (8 LSBs)*
0	1	0	1	Enable ADC Data (2 MSBs)*

*Data is Right Justified.

Table II. AD7579 Truth Table

HBEN	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
LOW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HIGH	$\overline{EOC}$*	0	0	0	0	0	DB9	DB8

*$\overline{EOC}$ is an internal End of Conversion flag.

Table IV. AD7579 Output Data Format

CIRCUIT INFORMATION

ANALOG INPUT CIRCUITRY

The AD7579 is a 10-bit ADC with an (8+2) output bus structure designed for 8-bit microprocessor systems. The AD7580 is a 10-bit ADC with a 10-bit parallel output bus structure. The ADC circuitry is identical in both parts. Block diagrams are shown on the first page of this data sheet.

Figure 6 shows the input circuitry to the ADC comparator. This comparator has differential inputs which are accessed through the attenuator networks made up of resistors R. The attenuators can be used to scale and offset analog input voltages, and this is done in Figures 14 and 15 to alter the basic ADC input range. The analog inputs to the comparator are differential with the provisos that V+ is always greater than or equal to V−, V− is greater than or equal to AGND and that V+ is less than or equal to V_{DD}. These conditions must be satisfied when using the ADC in any of the voltage ranges.

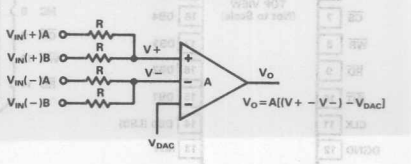


Figure 6. AD7579/AD7580 Input Circuit

Figure 7 shows an ac equivalent input circuit for the AD7579/AD7580 when used in the 2.5V Unipolar Mode of Figure 12. The ADC comparator is a sampled data comparator and the input circuitry for this is represented by S_A, Req and C_A. Req is a combination of the switch-on resistance and the input impedance of the comparator. When conversion starts, $V_{IN}(+)$ is sampled for at least ($2t_{CLK} + t_{WR} + 200ns$) before the comparator goes into the hold mode. This means that the analog input has a minimum of 1.1μs (f_{CLK} = 2.5MHz, t_{WR} = 100ns) to settle before the comparator makes a decision. By using the typical values in Figure 7 for R, Req and C_A, the input time constant is 50ns. Settling to ±1/4LSB in a 10-bit system takes 8.3 time constants or 415ns in this case. This means that $V_{IN}(+)$ has plenty of time to settle before the ADC comparison cycle begins. It is important to remember that any source resistance or source capacitance appearing at the input will also increase the settling time and this should be kept to a minimum in all cases.

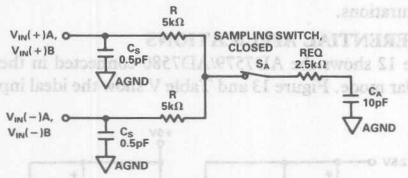


Figure 7. AD7579/AD7580 Equivalent Input Circuit During Sampling

With a 2.5MHz clock, the AD7579/AD7580 has a maximum conversion time of 18.5μs. If 1μs is allowed for reading the data outputs, the maximum sampling rate for the device is 50kHz. This means that the maximum analog input frequency is 25kHz according to the Nyquist theory. The ADC input impedance in the Unipolar Configuration of Figure 12 is 10MΩ. A medium bandwidth op amp will drive this at 25kHz. When the input attenuators are used for signal conditioning, the input impedance is 10kΩ. The drive requirements on the amplifier will now be greater but any errors resulting will be gain errors only. Suitable op amps for driving the AD7579/AD7580 in any of the input configurations are the AD711, AD OP-27, AD544. These will deliver specified device performance over the input bandwidth.

REFERENCE INPUT

The AD7579/AD7580 V_{REF} input is connected to the on-chip DAC. The input impedance of this is code dependent and the greatest variation occurs when the DAC resistors are at their lower limit. In this case, the impedance changes from 1.75kΩ to 5.25kΩ as the DAC is switched. To ensure that the error during conversion is less than 1/2LSB, the Reference output impedance should be less than 1Ω. References which satisfy this are the AD580 (shown in Figure 8) and the AD1403 from Analog Devices. If a trimmable reference such as the AD584 is used, it is possible to trim out the ADC full-scale error by adjusting the reference output.

INTERNAL SAMPLE-AND-HOLD

When an ADC without sample-and-hold is used to digitize ac signals, the analog input must not change by more than 1/2LSB during the conversion. This puts severe limitations on the allowable input signal bandwidth to such devices. A sample-and-hold amplifier must be used in front of the ADC if increased bandwidth is required. The charge balanced comparator used in the AD7579/AD7580 for the A/D conversion provides the user with an inherent sample-and-hold function. The ADC is specified to work with sampling rates up to 50kHz. This rate allows time to do a conversion and read the result into memory. Since at least two samples are needed to define an input sine wave according to the Nyquist theory, the analog input signal bandwidth for the AD7579/AD7580 is 25kHz. Figures 20, 21 and 22 show the performance of the ADC when digitizing ac signals.

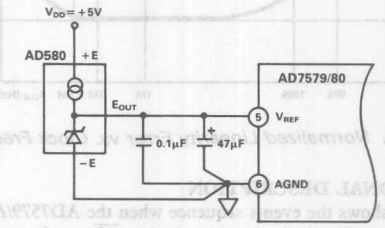


Figure 8. Using the AD580 as the Reference for the AD7579/AD7580

While the AD7579/AD7580 is converting, V+ (see Figure 6) is held and V− is being tracked. This limits the rate of change, $^{dv}/_{dt}$, on $V_{IN}(-)$. For example, if the Common-Mode frequency is 60Hz, then the allowable amplitude of this to introduce no more than 1/2LSB linearity error is 160mV pk-pk. As the Common-Mode frequency increases, this allowable amplitude decreases. Figure 9 shows how a 100mV pk-pk Common-Mode signal affects linearity error as its frequency is increased up to 1kHz.

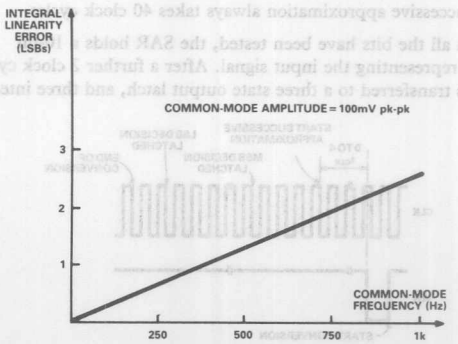


Figure 9. AD7579/AD7580 Error vs. Common-Mode Frequency

clock on the CLK input pin. This pin may be driven directly by CMOS or TTL buffers. The mark/space ratio on the clock can vary from 40/60 to 60/40. As the clock frequency is slowed down, it can result in slightly degraded accuracy performance. This is due to leakage effects on the hold capacitor in the internal sample-and-hold. Figure 10 is a typical plot of accuracy versus clock frequency for the ADC.

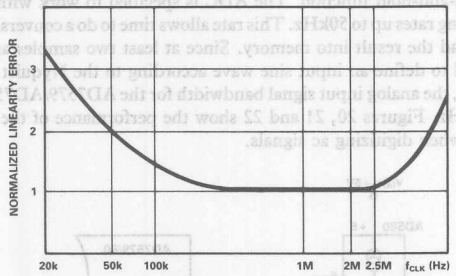


Figure 10. Normalized Linearity Error vs. Clock Frequency

FUNCTIONAL DESCRIPTION

Figure 11 shows the events sequence when the AD7579/AD7580 is converting. The device is selected when $\overline{CS}$ goes low and the first phase of conversion begins when $\overline{WR}$ goes low. This is an initializaton phase and causes the internal DAC to be set to full scale, comparators set to auto-zero and V+ (see Figure 6) to be sampled. The second phase begins some time after $\overline{WR}$ goes back high. This time can vary between 0 and 4 clock periods and depends on the state of an on-chip divide-by-4 counter which is used for internal synchronization. This is the start of the successive approximation procedure. V+ is held after 2-1/2 clock periods have elapsed. V− is sampled and the DAC output is switched into the comparator. There is $(1\text{-}1/2 \times t_{CLK})$ left for comparison and then the MSB result is latched. The MSB test takes 4 clock cycles as do each of the succeeding bit tests. Thus, the successive approximation always takes 40 clock cycles.

When all the bits have been tested, the SAR holds a 10-bit word representing the input signal. After a further 2 clock cycles this is transferred to a three state output latch, and three internal

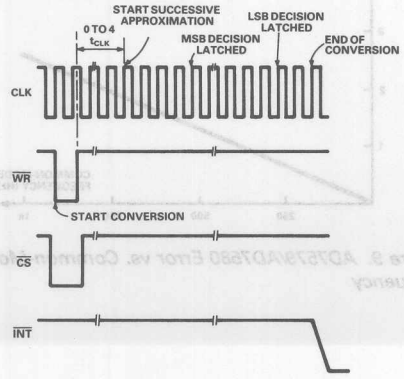


Figure 11. AD7579/AD7580 Conversion Sequence

both open drain outputs with RDY accessed by RD and INT being permanently available. When $\overline{INT}$ is loaded with the circuit of Figure 5(a), it typically takes 60ns to reach V_{OL}. $\overline{EOC}$ is only available on the AD7579 (see Table V). It appears on DB7, when reading the high Byte.

When the ADC is finished the conversion, the conditions of V+, V− and the comparators are maintained and the ADC is now ready to start a new conversion. If $\overline{WR}$ and CLK are asynchronous, the total time from start to end of conversion is variable. Minimum conversion time is $(t_{WR} + 42\ t_{CLK})$, and maximum conversion time is $(t_{WR} + 46\ t_{CLK})$.

APPLYING THE AD7579/AD7580

The AD7579/AD7580 has a flexible input stage consisting of two input attenuators. It is possible to realize various analog input ranges by reconfiguring these attenuators. The following diagrams show the ADC connected in the most popular configurations.

DIFFERENTIAL APPLICATIONS

Figure 12 shows the AD7579/AD7580 connected in the standard unipolar mode. Figure 13 and Table V show the ideal input/output

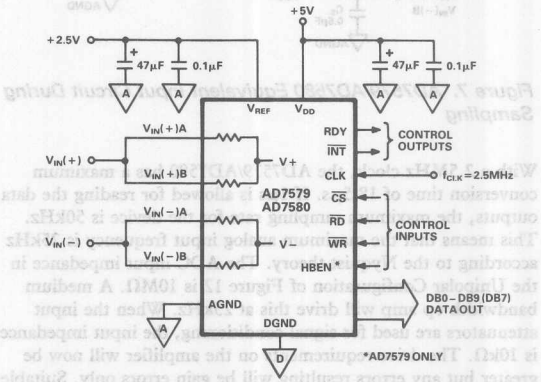


Figure 12. Unipolar 2.5V Operational Diagram

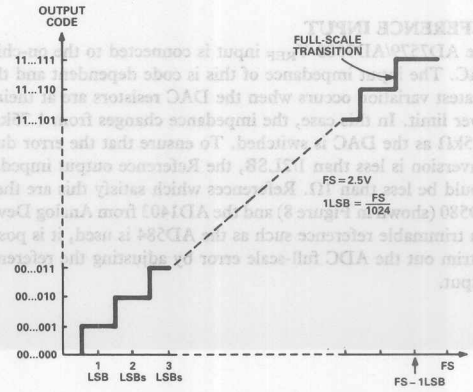


Figure 13. Ideal Input/Output Transfer Characteristic

Differential Analog Input, Volts	Digital Output DB9	DB0
+0.000	00 0000	0000
+0.00244	00 0000	0001
+1.24756	01 1111	1111
+1.25	10 0000	0000
+1.25244	10 0000	0001
+2.49512	11 1111	1110
+2.49756	11 1111	1111

Table V. Input/Output Code Table for Figure 12

transfer characteristic and the input/output code table respectively. Code transitions occur between successive integer LSB values (i.e., 1/2LSB, 3/2LSBs, etc.). The output code is straight binary with 1LSB = FS/1024 = 2.5/1024V = 2.4mV. The input voltage span is 2.5V and the common-mode range is 0V to +5V, when V_{DD} = 5V. This means that the lowest voltage which can be tolerated at any of the analog inputs is 0V, and the highest voltage which can be tolerated is +5V.

Figures 14 and 15 show the input attenuators on the AD7579/AD7580 configured to change the basic range of the device. A 5V range can be configured by grounding one end of each attenuator and applying the differential input to the other ends. This is shown in Figure 14. The span is 5V and the common-mode range is 0 to +10V. In Figure 15, one end of each attenuator is tied to V_{REF} (2.5V), and this allows each of the other legs to go to −2.5V without causing the comparator input to go negative. Assuming V_{REF} is 2.5V, the span of this circuit is 5V and the common-mode range is −2.5V to +7.5V. Note that reducing V_{DD} below 5 volts causes a corresponding reduction in CMR. See Specifications page for full details.

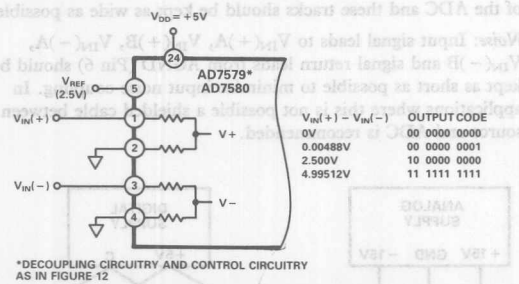


Figure 14. 5V Span with 0 to 10V CMR

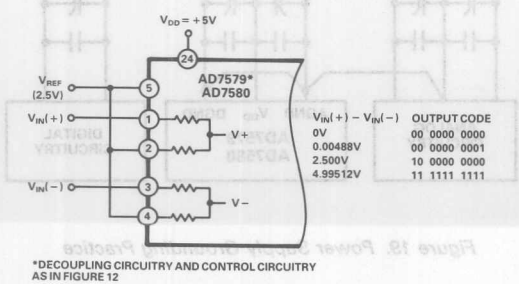


Figure 15. 5V Span with −2.5V to +7.5V CMR

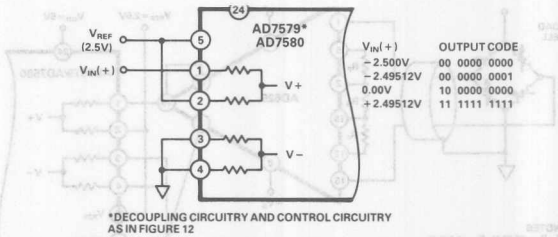


Figure 16. Single-Ended Bipolar Operation, −2.5V to +2.5V

SINGLE-ENDED APPLICATIONS

In many cases, users of the AD7579/AD7580 will want to measure single-ended input voltages (i.e., ground referred signals). The circuits of Figures 12, 14 and 15 can be easily adapted to accept such signals. If $V_{IN}(-)$ in Figure 12 is tied to AGND, then the analog input range is 0V to +2.5V. By connecting $V_{IN}(-)$ of Figure 14 to AGND, the analog input range becomes 0V to +5V. Figure 15 can be modified as in Figure 16 to accept input voltages in the range −2.5V to +2.5V. Each of these circuits are special cases of the Differential Input circuits and are achieved by making the negative input to the internal comparator equal to AGND.

OFFSET AND FULL-SCALE ADJUSTMENT

Figure 17 shows the AD7579/AD7580 connected in the single-ended Unipolar 2.5V range with offset and full-scale calibration circuitry. The zero error of the ADC is the deviation of the actual LSB transition from the ideal LSB transition. In many cases, the zero of the ADC will not need adjustment. When it does, R1 in Figure 17 provides 25mV of adjustment which is sufficient to null out both the op amp and ADC offset error. Resistors R3 and R4 bias $V_{IN}(-)$ to approximately 8mV and ensure that the offset error is never positive. This allows the error to be nulled in the single supply system of Figure 17. Apply +0.5LSB to V_{IN} and adjust R1 until the ADC output code flickers between 00 ..... 000 and 00 ..... 001.

For full-scale calibration, apply a voltage of (2.5V − 1.5LSB) to V_{IN}. Then adjust R2 until the output code flickers between 11 ..... 110 and 11 ..... 111. When the full-scale calibration is complete, return to the offset adjustment procedure and check that further adjustment is not necessary.

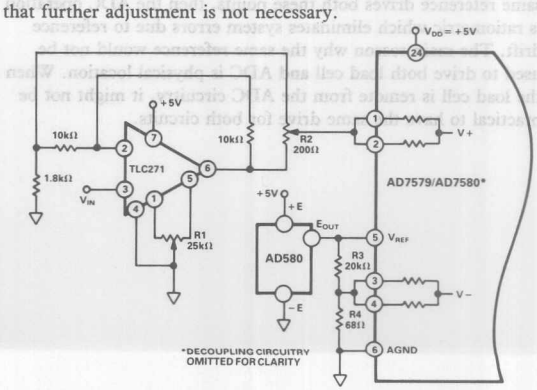


Figure 17. Offset and Full-Scale Calibration for Single-Ended Circuit

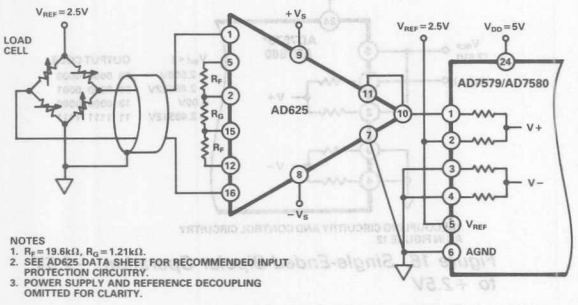


Figure 18a. AD7579/AD7580 and AD625 in a Data Acquisition System

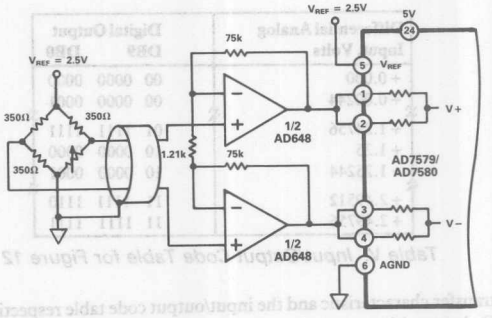


Figure 18b. AD7579/AD7580 and AD648 in a Data Acquisition System

AD7579/AD7580 IN DATA ACQUISITION SYSTEMS

The AD7579/AD7580 is suitable for many data acquisition circuits. Figure 18a shows one such circuit in which a load cell is used to produce a signal in response to an applied force. Typically these transducers produce 30mV full scale per volt of excitation. Since the excitation in this case is 2.5V, the output from the load cell is ±75mV when the maximum specified force is applied. The AD625 Instrumentation Amplifier is set for a gain of 33.33 which means that the input signal to the ADC is ±2.5V. Thus, the AD7579/AD7580 is configured in the single-ended, ±2.5V range of Figure 16. When no force is applied to the load cell, the ADC output will sit at mid-scale. With maximum negative force applied the ADC output will be all zeros; whereas, with maximum positive force the output will be all 1s. Offset and gain calibration of this system can be accomplished by trimming the offsets and gain of the instrumentation amplifier.

Figure 18b shows a differential transducer unbalanced by ≈10Ω supplying a 0 to 20mV maximum signal. The resistors are chosen for a gain of 125, and the ADC is configured to accept 0 to 2.5V differential signal. This is a lower-cost alternative to using an instrumentation amplifier.

Note that in the circuits of Figure 18, V_{REF} for the ADC and the excitation voltage for the load cell are both +2.5V. If the same reference drives both these points, then the ADC operation is ratiometric which eliminates system errors due to reference drift. The main reason why the same reference would not be used to drive both load cell and ADC is physical location. When the load cell is remote from the ADC circuitry, it might not be practical to have the same drive for both circuits.

APPLICATIONS HINTS

Layout: To obtain the best performance from the AD7579/AD7580, lay it out on a printed circuit board. Digital and analog lines on the board should be separated as much as possible. In particular, take care not to run any digital track adjacent to an analog signal track or underneath the AD7579/AD7580. The analog inputs should be screened by AGND.

Grounding: Establish a single-point analog ground (STAR ground) at Pin 6 (AGND) or as close as possible to the AD7579/AD7580. This is shown in Figure 19. Pin 12 (AD7579/AD7580 DGND) and all other analog grounds should be connected to this single analog ground point. However, do not connect any other digital grounds to this analog ground point. Low impedance analog and digital power supply returns are essential to low noise operation of the ADC and these tracks should be kept as wide as possible.

Noise: Input signal leads to $V_{IN}(+)A$, $V_{IN}(+)B$, $V_{IN}(-)A$, $V_{IN}(-)B$ and signal return leads from AGND (Pin 6) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible a shielded cable between source and ADC is recommended.

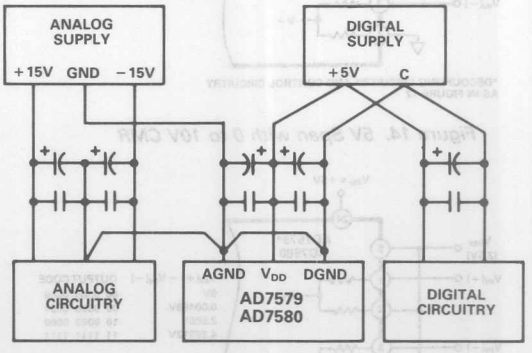


Figure 19. Power Supply Grounding Practice

DIGITAL SIGNAL PROCESSING APPLICATIONS

In Digital Signal Processing (DSP) application areas like voice recognition, echo cancellation and adaptive filtering, the dynamic characteristics (SNR, Harmonic Distortion, Intermodulation Distortion) of ADCs are critical. For this reason, the AD7579/AD7580 is specified dynamically as well as with standard D.C. specifications (linearity error, offset error, etc.).

Figure 20 shows a 2048 point FFT plot of an AD7579/AD7580 with an input signal of 3.58kHz. The SNR is 60.1dBs. The largest harmonic appears at $2f_O$ (7.16kHz) and is 70dB down from the fundamental. Harmonics above $3f_O$ are in the noise floor. Note that when SNR is calculated, it includes harmonics.

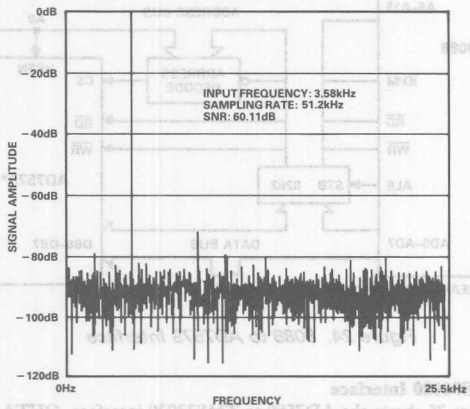


Figure 20. AD7579/AD7580 Spectral Response

If these were excluded the SNR figure would be closer to the ideal of 62dB for a 10-bit ADC. The relationship between Signal-to-Noise Ratio (SNR) and ADC resolution is expressed in the following equation:

$$SNR = (6.02N + 1.76)dB$$

This is for an ideal ADC with no differential or integral linearity errors. These errors will cause a degradation in SNR. By working backwards in the above equation it is possible to get a measure of ADC performance expressed in effective number of bits. This is shown over frequency in Figure 21 for the AD7579/AD7580. The effective number of bits typically falls between 9.7 and 9.8 corresponding to SNRs of 60.0 and 60.6dBs.

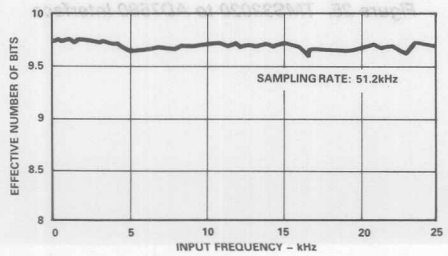


Figure 21. AD7579/AD7580 Effective Number of Bits

When a sine wave of specified frequency is applied to the AD7579/AD7580 and several thousand samples are taken, it is possible to plot a histogram showing the frequency of occurrence of each of 1024 ADC codes. A perfect ADC would produce a cusp probability density function described by the equation

$$p(V) = \frac{1}{(A^2 - V^2)^{1/2}}$$

A is the peak amplitude of the sine wave and p(V) the probability of occurrence at the voltage V. If a particular step is wider than the ideal width, then the code associated with that step will accumulate more counts than the code for an ideal step. Likewise, a step narrower than ideal width will have fewer counts. Missing codes are easily seen because a missing code means zero counts for a particular code. The absence of large spikes in the histogram indicates small differential nonlinearity. The actual histogram obtained is shown in Figure 22 and corresponds very well with the ideal cusp shape. It shows that the AD7579/AD7580 has very small differential nonlinearity and no missing codes with an input frequency of 25kHz.

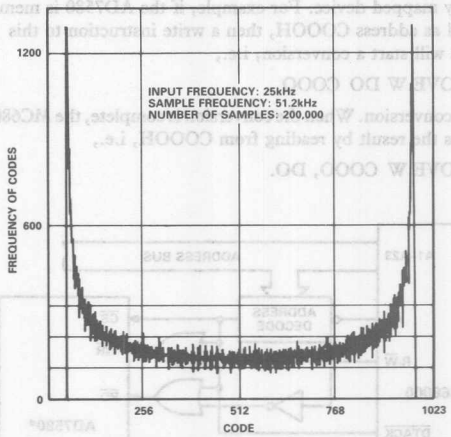


Figure 22. Histogram Plot for AD7579/AD7580

Whenever the AD7579/AD7580 is used to sample ac signals, it is essential that the signal sampling occurs at exactly equal intervals. This minimizes errors due to sampling uncertainty or jitter. The $\overline{WR}$ command for the AD7579/AD7580 needs to be synchronized with the CLK input to ensure equal interval sampling.

Two conditions must be satisfied to ensure proper synchronization: 1) The time interval between successive $\overline{WR}$ signals needs to be long enough to allow a conversion to finish and the data to be read into memory. 2) Because of the internal operation of the ADC, the number of clock pulses between successive write signals must be a multiple of four.

The conversion time for the AD7579/AD7580 has a maximum value of (t_{WR} + 46 t_{CLK}). If 4 t_{CLK} is allowed for reading the data outputs into a buffer then the interval between successive $\overline{WR}$ signals must be at least 50 t_{CLK}. The easiest way to satisfy both this requirement and number 2 above is to divide f_{CLK} by 64 to produce the $\overline{WR}$ signal. Alternatively, if a programmable timer/counter on a processor board is available, then it will be possible to easily divide f_{CLK} by 52.

Reading Data

Conversion is started in the AD7579/AD7580 by bringing $\overline{WR}$ low. It is recommended that the user wait until conversion is complete before reading data. This can be achieved in any of the following ways:

1. Insert a software delay greater than the ADC conversion time between the conversion start instruction and the data read instructions.
2. Use the externally available $\overline{INT}$ signal to interrupt the microprocessor. This is an open drain output which goes low at the end of conversion.
3. On the AD7579, it is possible to interrogate the $\overline{EOC}$ status flag (See Table IV) to determine when conversion is complete. Reading may then proceed.

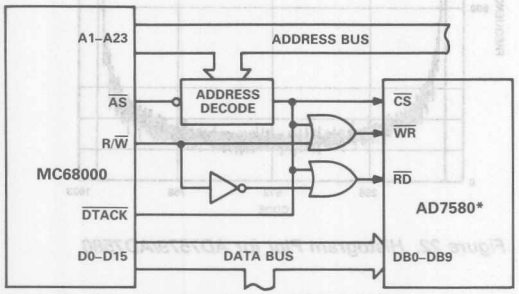
MC68000 Interface

Figure 23 shows an interface diagram for the AD7580 and the MC68000. The address decoding means that the AD7580 is a memory mapped device. For example, if the AD7580 is memory mapped as address COOOH, then a write instruction to this address will start a conversion, i.e.,

MOVE.W DO COOO

starts a conversion. When the conversion is complete, the MC68000 acquires the result by reading from COOOH, i.e.,

MOVE.W COOO, DO.

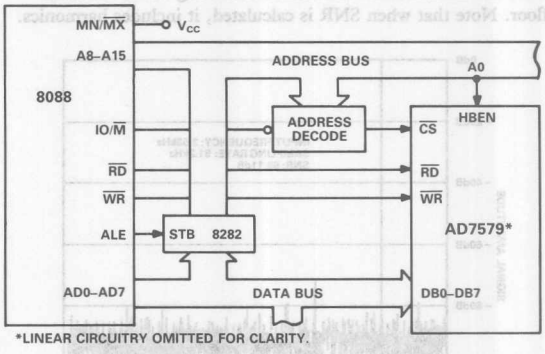


*LINEAR CIRCUITRY OMITTED FOR CLARITY.

Figure 23. MC68000 to AD7580 Interface

The AD7579, with its (8 + 2) data format, is ideal for use with the 8088 microprocessor. Figure 24 is the interface diagram. Again, a write instruction is required to start a conversion and a read at the end of conversion reads data into the processor. For the 8088 the appropriate instructions are:

MOV COOO, AX	Start a conversion
MOV AX, COO1	Read 2 MSBs of data
MOV AX, COOO	Read 8 LSBs of data

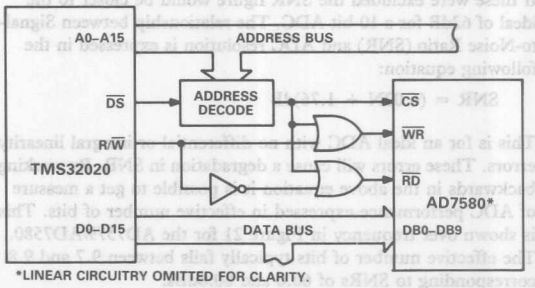


*LINEAR CIRCUITRY OMITTED FOR CLARITY.

Figure 24. 8088 to AD7579 Interface

TMS32020 Interface

Figure 25 shows the AD7580 to TMS32020 interface. OUTA,PA starts a conversion and INA,PA reads data from the ADC when conversion is complete. PA is the Port Address.



*LINEAR CIRCUITRY OMITTED FOR CLARITY.

Figure 25. TMS32020 to AD7580 Interface

PRINTED CIRCUIT BOARD LAYOUT

Figure 26 is a circuit diagram showing the AD7579 or AD7580 being used to digitize an analog signal. The circuit board contains the ADC, reference, and a grid where the user can add additional circuitry. If the AD7580 is used, then links L6 and L8 should be inserted; and if AD7579 is used, L7 should be inserted with L6 and L8 omitted. Note that Pins 13 to 23 are not labelled. Depending on which ADC is used the function of these pins changes. See the Pin Function Description section for full details.

Links L1 to L5 at the analog input allow the user to choose various analog input ranges. With L1, L2 and L3 in place and the others omitted, the input range is 0V to +2.5V. Omitting L3 allows the user to measure input voltages which have a common-mode signal. The 0V to +5V range is achieved by inserting L2, L3 and L4 and omitting L1 and L5. With L2, L3 and L5 in place and L1, L4 omitted, the Analog input range is −2.5V to +2.5V.

IC2 (AD580) provides the +2.5V reference for the ADC. All the input and output control signals enter and leave the board through J1, which can be a Eurocard connector or a standard edge connector. Resistors R1 and R2 are the pull-ups required for the RDY and $\overline{INT}$ open-drain outputs. Note that the complete circuit operates from a +5V power supply.

The printed circuit board layout is shown in Figures 27 and 28. Figure 27 is the component side layout and Figure 28 is the solder side layout. The component overlay is shown in Figure 29.

In the layout, the AD580 is kept as close to the AD7579/AD7580 as possible. The STAR ground point is located at Pin 6 (AGND) of the ADC. Pin 12 (DGND), reference ground and the analog ground plane are connected to this point.

To ensure optimum performance, the AD7579/AD7580 power supply is decoupled with C1 and C2. The V_{REF} input to the ADC is decoupled with C3 and C4. Note how all the decoupling capacitors are placed as close as possible to the ADC.

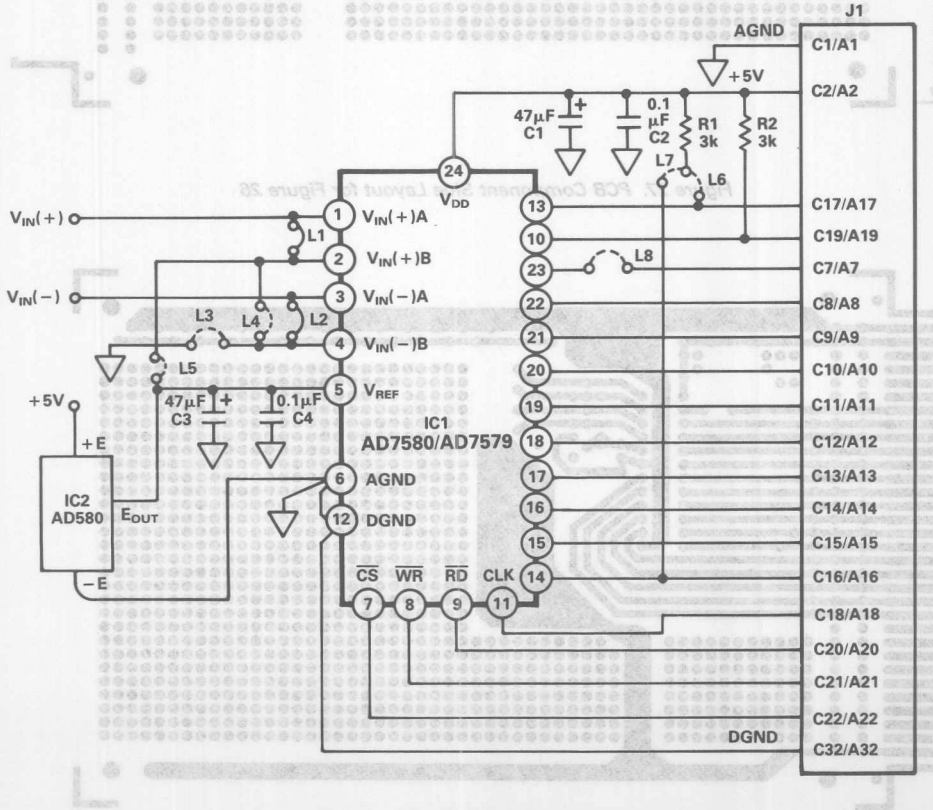


Figure 26. Schematic for AD7579/AD7580 Board

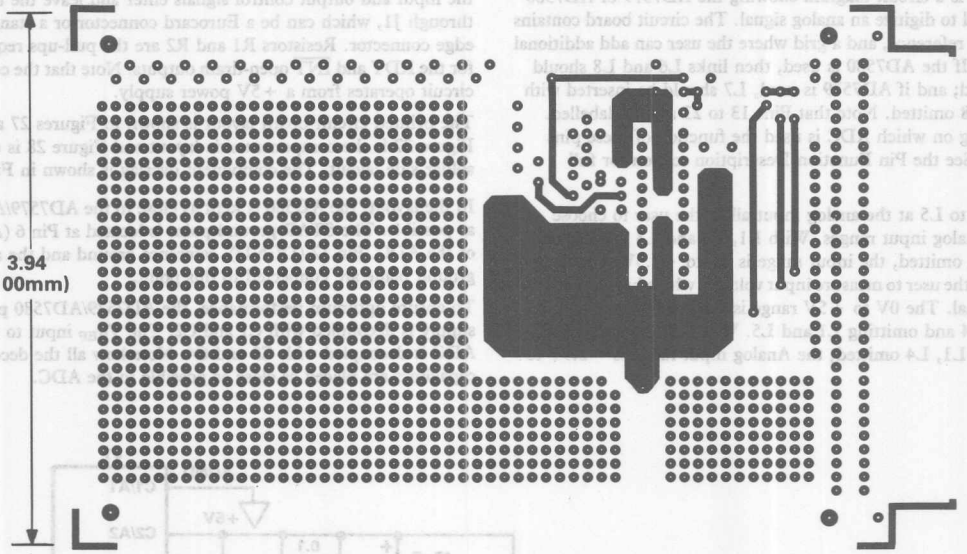


Figure 27. PCB Component Side Layout for Figure 26

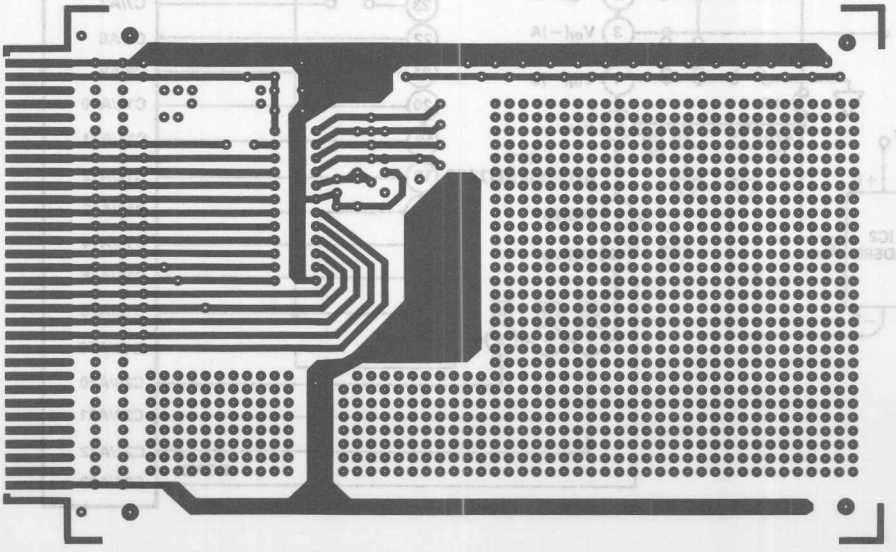


Figure 28. PCB Solder Side Layout for Figure 26

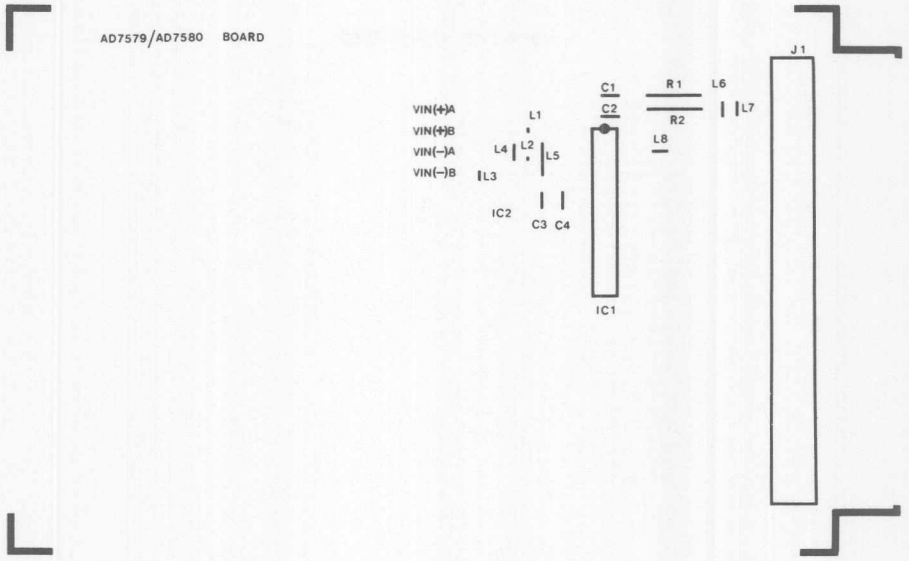


Figure 29. Component Overlay for Circuit of Figure 26

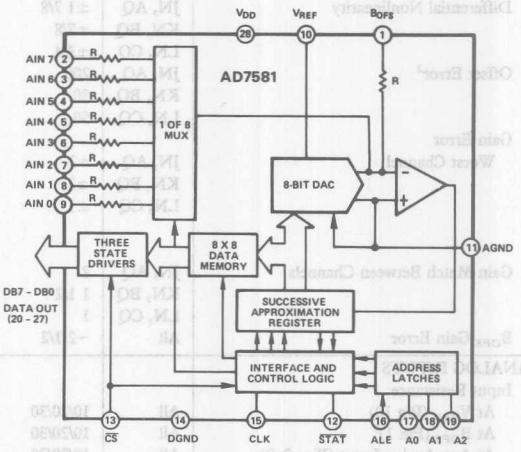
8-Bit, 8-Channel DAS

AD7581

FEATURES

- 8-Bit Resolution
- On-Chip 8 X 8 Dual-Port Memory
- No Missed Codes Over Full Temperature Range
- Interfaces Directly to Z80/8085/6800
- CMOS, TTL Compatible Digital Inputs
- Three-State Data Drivers
- Ratiometric Capability
- Interleaved DMA Operation
- Fast Conversion
- A/D Process Totally Transparent to μP
- Low Cost

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7581 is a microprocessor compatible 8 bit, 8 channel, memory buffered, data-acquisition system on a monolithic CMOS chip. It consists of an 8 bit successive approximation A/D converter, an 8 channel multiplexer, 8 X 8 dual-port RAM, three-state DATA drivers (for interface), address latches and microprocessor compatible control logic. The device interfaces directly to 8080, 8085, Z80, 6800 and other microprocessor systems.

The successive approximation conversion takes place on a continuous, channel sequencing, basis using microprocessor control signals for the clock. Data is automatically transferred to its proper location in the 8 X 8 dual-port RAM at the end of each conversion. When under microprocessor control, a READ DATA operation is allowed at any time for any channel since on-chip logic provides interleaved DMA. The facility to latch the address inputs ($A_0 - A_2$) with ALE enables the AD7581 to interface with μP systems which feature either shared or separate address and data buses.

Parameter	Version[1]	Typical at +25°C	Limit Over Temperature	Units	Conditions/Comments
ACCURACY					
Resolution	All	8	8	Bits	
Relative Accuracy	JN, AQ	±1 7/8	±1 7/8 max	LSB	
	KN, BQ	±3/4	±3/4 max	LSB	
	LN, CQ	±1/2	±1/2 max	LSB	
Differential Nonlinearity	JN, AQ	±1 7/8	±1 7/8 max	LSB	
	KN, BQ	±7/8	±7/8 max	LSB	
	LN, CQ	±3/4	±3/4 max	LSB	
Offset Error[2]	JN, AQ	200	200 max	mV	Adjustable to zero, See Figure 7a.
	KN, BQ	80	80 max	mV	
	LN, CQ	50	50 max	mV	
Gain Error					
Worst Channel	JN, AQ	±3	±6 max	LSB	Adjustable to zero, See Figure 7a.
	KN, BQ	±2	±4 max	LSB	Gain Error Is Measured After Offset
	LN, CQ	±1	±2 max	LSB	Calibration. Max Full Scale Change for Any Channel from +25°C to T_{min} or T_{max} Is ±2LSB.
Gain Match Between Channels	JN, AQ	2	3 max	LSB	Adjustable to zero, See Figure 7a.
	KN, BQ	1 1/2	2 max	LSB	
	LN, CQ	1	1 max	LSB	
B_{OFS} Gain Error	All	−2 1/2	–	LSB	
ANALOG INPUTS					
Input Resistance					
At V_{REF} (Pin 10)	All	10/20/30	10/20/30	kΩ min/typ/max	
At B_{OFS} (Pin 1)[3]	All	10/20/30	10/20/30	kΩ min/typ/max	
At Any Analog Input (Pins 2–9)	All	10/20/30	10/20/30	kΩ min/typ/max	
V_{REF} (For Specified Performance)	All	−10	−10	V	±5%
V_{REF} Range[4]	All	−5 to −15	−5 to −15	V	
Nominal Analog Input Range					
Unipolar Mode	All	0 to $+V_{REF}$	0 to $+V_{REF}$	V	See Figure 7 and 8.
		0 to $-V_{REF}$	0 to $-V_{REF}$	V	
Bipolar Mode	All	$-VB_{OFS} \leq VA_{IN} \leq \lvert V_{REF} \rvert - VB_{OFS}$			See Figure 9
DIGITAL INPUTS					
$\overline{CS}$ (Pin 13), ALE (Pin 16) $A_0 - A_2$ (Pin 17-19), CLK (Pin 15)					
V_{INH} Logic HIGH Input Voltage	All	+2.2	+2.4 min	V	
V_{INL} Logic LOW Input Voltage	All	+1.2	+0.8 max	V	
I_{IN} Input Current	All	0.01	1 max	μA	V_{IN} = 0V, V_{DD}
C_{IN} Input Capacitance[5]	All	4	5 max	pF	
DIGITAL OUTPUTS					
$\overline{STAT}$ (Pin 12), DB_7 to DB_0 (Pins 20–27)					
V_{OH} Output HIGH Voltage	All	+4.8	+4.5 min	V	I_{SOURCE} = 40μA
V_{OL} Output LOW Voltage	All	+0.4	+0.6 max	V	I_{SINK} = 1.6mA
I_{LKG} DB_7 to DB_0 Floating State Leakage	All	0.3	10 max	μA	
Floating State Output Capacitance (DB_7–DB_0)	All	5	10 max	pF	V_{OUT} = 0V to V_{DD}
Output Code	All	Unipolar Binary Figure 7 Complementary Binary Figure 8 Offset Binary Figure 9			
POWER REQUIREMENTS					
V_{DD}	All	+5	+5	V	
I_{DD} – Static	All	3 typ	5 max	mA	
I_{DD} – Dynamic	All	3 typ	8 max	mA	f_{CLK}=1MHz

NOTES
[1]Temperature range as follows: JN, KN, LN (0 to +70°C); AQ, BQ, CQ (−25°C to +85°C).
[2]Typical offset temperature coefficient is ±150μV/°C.
[3]R_{BOFS}/R_{AIN} (0–7) mismatch causes transfer function rotation about positive full scale. The effect is an offset and a gain term when using the circuits of Figure 8a and Figure 9a.
[4]Typical value, not guaranteed or subject to test.
[5]Guaranteed but not tested.
[6]Typical change in B_{OFS} gain from +25°C to T_{min} to T_{max} is ±2LSBs.
Specifications subject to change without notice.

AC SPECIFICATIONS (V_{DD} = +5V, V_{REF} = −10V, Unipolar Operation, unless otherwise stated.)

Symbol	Specification	Typical at +25°C	Limit Over Temperature	Units	Conditions
t_H	ALE pulse width	50	80 min	ns	See "Switching Terminology"
t_{ALS}	Address valid to latch set-up time	45	70 min	ns	
t_{ALH}	Address valid to latch hold time	10	20 min	ns	
t_{LCS}	Address latch to $\overline{CS}$ set-up time	10	20 min	ns	
t_{ACC}	$\overline{CS}$ to output propagation delay	200	250 max	ns	C_L = 100pF
t_{CW}	$\overline{CS}$ pulse width	250	280 min	ns	
t_{CF}	$\overline{CS}$ to output float propagation delay	50	80 max	ns	
t_{CLZ}	$\overline{CS}$ to low impedance bus	100	150 max	ns	
f_{CLK}	Clock frequency for stated accuracy	1600	1200 max[1]	kHz	

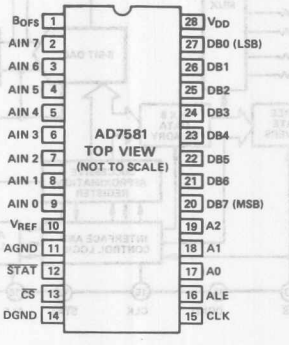
[1] Guaranteed conversion time of 66.6μs/channel with 1200kHz clock.

2

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND . . . . . +7V
V_{DD} to DGND . . . . . +7V
AGND to DGND . . . . . −0.3V, V_{DD}
Digital Input Voltage to DGND
(Pins 13, 16–19) . . . . . −0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND
(Pins 12, 20–27) . . . . . −0.3V, V_{DD} +0.3V
CLK (Pin 15) Input Voltage to DGND . −0.3V, V_{DD} +0.3V
V_{REF} (Pin 10) to AGND . . . . . ±25V
V_{BOFS} (Pin 1) to AGND . . . . . ±17V
AIN (0–7)(Pin 9–2) . . . . . ±17V
Operating Temperature Range
Commercial (J, K, L Versions) . . . . . 0 to +70°C
Industrial (A, B, C Versions) . . . . . −25°C to +85°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C
Power Dissipation (Any Package)
to +75°C 1,000mW
Derate above +75°C by . . . . . 10mW/°C

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



ORDERING GUIDE

Model	Temperature Range	Differential Nonlinearity (LSB)	Package Option*
AD7581JN	0 to +70°C	±1 7/8 max	N-28
AD7581KN	0 to +70°C	±7/8 max	N-28
AD7581LN	0 to +70°C	±3/4 max	N-28
AD7581AQ	−25°C to +85°C	±1 7/8 max	Q-28
AD7581BQ	−25°C to +85°C	±7/8 max	Q-28
AD7581CQ	−25°C to +85°C	±3/4 max	Q-28

NOTE
*N = Plastic DIP; Q = Cerdip. For outline information see Package Information section.

GENERAL CIRCUIT INFORMATION

BASIC CIRCUIT DESCRIPTION

The AD7581 accepts eight analog inputs and sequentially converts each input into an eight-bit binary word using the successive approximation technique. The conversion results are stored in an 8 X 8 bit dual-port RAM. The device runs either directly from the microprocessor clock (in 6800 type systems) or from some suitable signal (e.g. ALE in 8085 type systems). Most applications require only a –10V reference and a +5V supply. Start-up logic is included on the device to establish the correct sequences on power-up. A maximum of 800 clock pulses are required for this period. Figure 1 shows the AD7581 functional diagram.

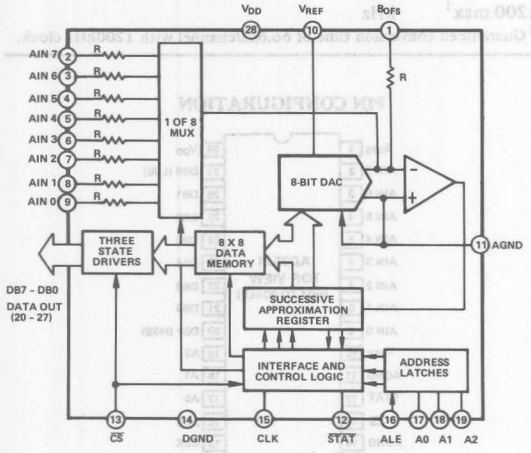


Figure 1. AD7581 Functional Diagram

Conversion of a single channel requires 80 input clock periods and a complete scan through all channels requires 640 input clock periods. When a channel conversion is complete, the successive approximation register contents are loaded into the proper channel location of the 8 X 8 RAM. At this time a status signal output, $\overline{STAT}$ (pin 12), gives a short negative going pulse (8 clock periods). This negative going $\overline{STAT}$ pulse is extended to 72 clock periods when channel 1 conversion is complete. An external pulse-width detector connected to the status pin can be used to derive conversion-related timing signals for microprocessor interrupts (see Channel Identification opposite page). Simultaneous with $\overline{STAT}$ going low, the MUX address is decremented. Eight clock periods later the next conversion is started.

Automatic interleaved DMA is provided by on-chip logic to ensure that memory updates take place at instants when the microprocessor is not addressing memory. Memory locations are addressed by A_0, A_1 and A_2. This address may be latched by ALE for systems which feature a multiplexed address/data bus or alternatively, for systems which have separate address and data buses, the address latches can be made transparent by tying ALE (pin 16) HIGH. $\overline{CS}$ (pin 13) activates three-state buffers to place addressed data on the $DB_0 - DB_7$ data output pins.

A/D CIRCUIT DETAILS

In the successive approximation technique, successive bits, starting with the most significant bit (DB_7), are applied to the input of the D/A converter. The DAC output is then compared to the unknown analog input voltage, A_{IN} (n), using a comparator. If the DAC output is greater than $A_{IN}(n)$, the data latch for the trial bit is reset to zero, and the next smaller data bit is tried. If the DAC output is less than $A_{IN}(n)$, the trial data bit stays in the "1" state, and the next smaller data bit is tried. Each successive bit is tried, compared to $A_{IN}(n)$, and set or reset in this manner until the least significant bit (DB_0) decision is made. The successive approximation register now contains a valid digital representation of $A_{IN}(n)$. $A_{IN}(n)$ is assumed to be stable during conversion.

The current weighting D/A converter is a precision multiplying DAC. Figure 2 shows the functional diagram of the DAC as used in the AD7581. It consists of a precision Silicon Chromium thin film R/2R ladder network and 8 N-channel MOSFET switches operated in single-pole-double-throw.

The currents in each 2R shunt arm are binarily weighted i.e., the current in the MSB arm is V_{REF} divided by 2R, in the second arm is V_{REF} divided by 4R, etc. Depending on the D/A logic input (A/D output) from the successive approximation register, the current in the individual shunt arms is steered either to A_{GND} or to the comparator summing point.

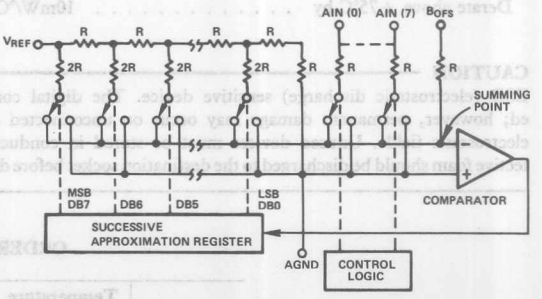


Figure 2. D/A Converter as Used in AD7581

TIMING AND CONTROL OF THE AD7581

CHANNEL SELECTION

Table I shows the truth table for the address inputs. The input address is latched when ALE goes LOW. When ALE is HIGH the address input latch is transparent.

A2	A1	A0	ALE	Channel Data To Be Read
0	0	0	1	Channel 0
0	0	1	1	Channel 1
0	1	0	1	Channel 2
0	1	1	1	Channel 3
1	0	0	1	Channel 4
1	0	1	1	Channel 5
1	1	0	1	Channel 6
1	1	1	1	Channel 7

Table I. Channel Selection Truth Table

TIMING AND CONTROL

A typical timing diagram is shown in Figure 3. When $\overline{CS}$ is HIGH, the three-state data drivers are in the high-impedance state. When $\overline{CS}$ goes LOW the data drivers switch to the low-impedance state (i.e., low impedance to DGND or to V_{DD}). Output data is valid after time t_{ACC}.

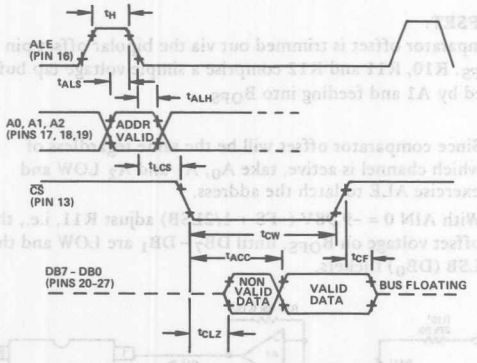


Figure 3. Timing Diagram for the AD7581

SWITCHING TERMINOLOGY

t_H: ALE pulse width requirement.
t_{ALH}: Address Valid to latch hold time.
t_{ALS}: Address Valid to latch set-up time.
t_{LCS}: Address latch to Chip Select set-up time.
t_{CW}: Chip Select pulse width requirement.
t_{ACC}: Chip Select to valid data propagation delay.
t_{CF}: Chip Select to output data float propagation delay.
t_{CLZ}: Chip Select to low impedance data bus.

CHANNEL IDENTIFICATION

In some real-time applications, it may be necessary to provide an interrupt signal when a particular channel receives updated data. To achieve this, it is necessary to identify which channel is currently under conversion. The $\overline{STAT}$ output provides an identifying signal by staying low for an additional 64 clock periods over normal (8 clock periods) when channel 0 is active. This is illustrated in Figure 4. Memory update takes place on a rising edge of a clock pulse and is completed in 200ns. This occurs 6 clock periods before $\overline{STAT}$ goes low.

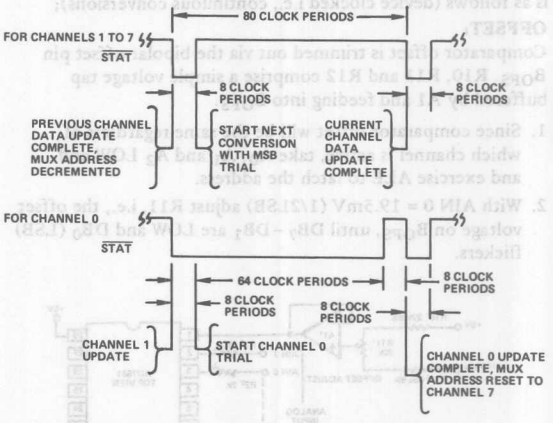


Figure 4. $\overline{STAT}$ Output for Channel Identification

One simple circuit using the $\overline{STAT}$ output is shown in Figure 5. The time constant RC is chosen such that X_2 ignores the normal $\overline{STAT}$ low pulse width (8 clock periods wide) but respond to the much wider $\overline{STAT}$ low pulse width (72 clock periods wide) occurring during channel 0 conversion. Typically for a 1μs clock period C = 0.022μF, R = 1.8kΩ.

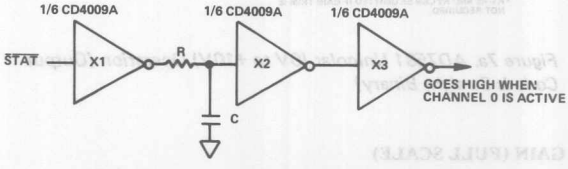


Figure 5. Hardware Channel Identification

Another possibility is to use the microprocessor to interrogate the $\overline{STAT}$ output and hence determine channel identity. A simple routine is shown in Figure 6.

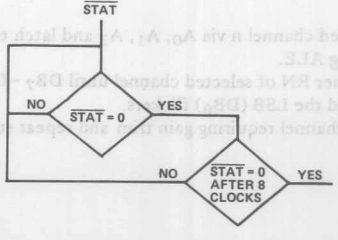


Figure 6. Software Channel Identification

UNIPOLAR BINARY OPERATION

Figures 7a and 7b show the analog circuit connections and typical transfer characteristic for unipolar operation (0V to +10V). An AD584 is used for the -10V reference. Calibration is as follows (device clocked i.e., continuous conversions);

OFFSET:

Comparator offset is trimmed out via the bipolar offset pin B_{OFS}. R10, R11 and R12 comprise a simple voltage tap buffered by A1 and feeding into B_{OFS}.

1. Since comparator offset will be the same regardless of which channel is active, take A_0, A_1 and A_2 LOW and and exercise ALE to latch the address.
2. With AIN 0 = 19.5mV (1/2LSB) adjust R11, i.e., the offset voltage on B_{OFS}, until $DB_7 - DB_1$ are LOW and DB_0 (LSB) flickers.

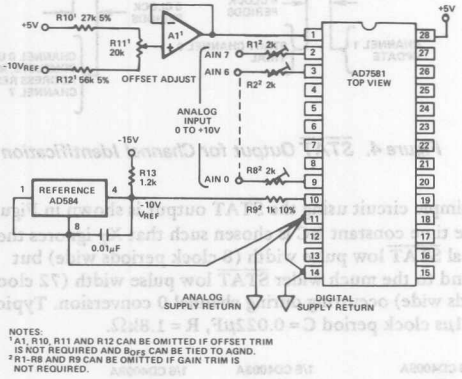


Figure 7a. AD7581 Unipolar (0V to +10V) Operation (Output Code is Straight Binary)

GAIN (FULL SCALE)

In many applications gain adjustment is not required thus removing the need for trimmers in the analog channels. For channels requiring gain trim, the following procedure is recommended. Offset adjustment must be performed before gain adjustment.

1. Apply +9.941V (FS - 3/2LSB) to all input channels AIN (0-7).
2. Select required channel n via A_0, A_1, A_2 and latch the Address using ALE.
3. Adjust trimmer RN of selected channel until $DB_7 - DB_1$ are HIGH and the LSB (DB_0) flickers.
4. Select next channel requiring gain trim and repeat steps 2 and 3.

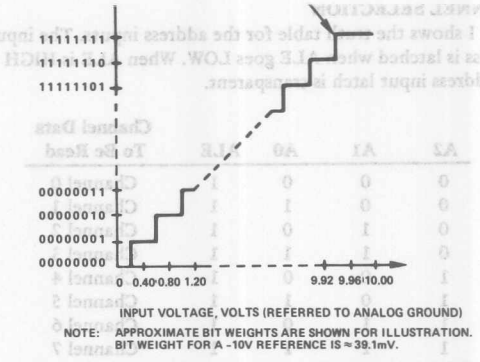


Figure 7b. Transfer Characteristic for Unipolar Circuit of Figure 7a

UNIPOLAR (COMPLEMENTARY BINARY) OPERATION

Figures 8a and 8b show the analog circuit connections and typical transfer characteristic for unipolar (complementary binary) operation.
Calibration is as follows (continuous conversions);

OFFSET:

Comparator offset is trimmed out via the bipolar offset pin B_{OFS}. R10, R11 and R12 comprise a simple voltage tap buffered by A1 and feeding into B_{OFS}.

1. Since comparator offset will be the same regardless of which channel is active, take A_0, A_1 and A_2 LOW and exercise ALE to latch the address.
2. With AIN 0 = -9.98V (-FS + 1/2LSB) adjust R11, i.e., the offset voltage on B_{OFS}, until $DB_7 - DB_1$ are LOW and the LSB (DB_0) flickers.

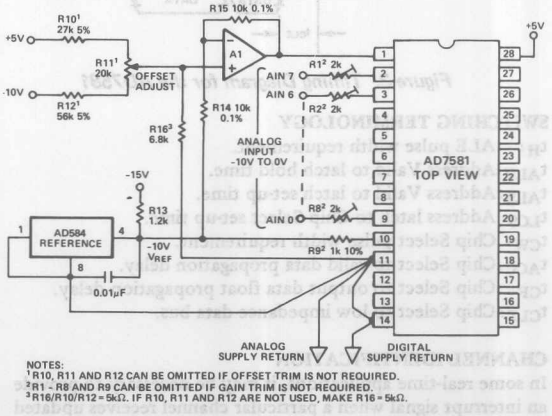


Figure 8a. AD7581 (0V to -10V) Operation (Output Code is Complementary Binary)

In many applications gain adjustment is not required thus removing the need for trimmers in the analog channels. For channels requiring gain trim, the following procedure is recommended. Offset adjustment must be performed before gain adjustment.

1) Apply -58.6mV (3/2LSB) to all input channels AIN (0-7).
2) Select required channel n via A_0, A_1, A_2 and exercise ALE to latch the address.
3) Adjust trimmer RN of selected channel until DB_7 - DB1 are HIGH and the LSB (DB_0) flickers.
4) Select next channel requiring gain trim and repeat step 2 and 3.

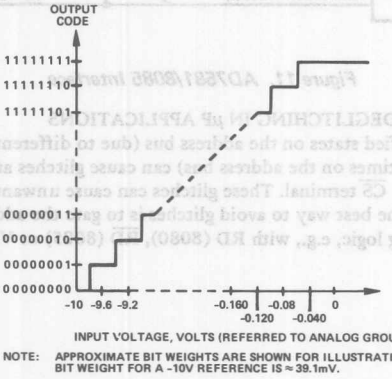


Figure 8b. Transfer Characteristic for Unipolar Circuit of Figure 8a

BIPOLAR (OFFSET BINARY) OPERATION

Figures 9a and 9b illustrate the analog circuitry and transfer characteristic for ±5V bipolar operation. Output coding is offset binary. Comparator offset correction is again applied to the B_{OFS} pin.

Calibration is as follows (continuous conversions);

OFFSET:

1. Apply -4.980V (-FS/2 + 1/2LSB) to all input channels AIN (0-7).
2. Trim R11 of the comparator offset circuit until DB_7 - DB_1 are LOW and the LSB (DB_0) flickers.

GAIN (FULL SCALE)

1. Apply +4.941V (+FS/2 -3/2LSB) to all input channels, A_{IN} (0-7).
2. Select required channel n via A_0, A_1, A_2, and latch the address using ALE.
3. Adjust trimmer RN of selected channel until DB_7 - DB_1 are HIGH and the LSB (DB_0) flickers.

2 and 3.

5. Apply -19.5mV to each gain-trimmed channel. If the ADC output code does not flicker between 01111111 and 10000000 repeat the calibration procedure.

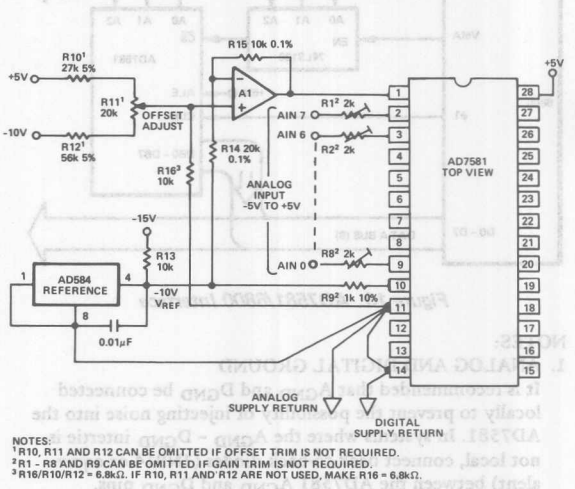


Figure 9a. AD7581 Bipolar (-5V to +5V) Operation (Output Code is Offset Binary)

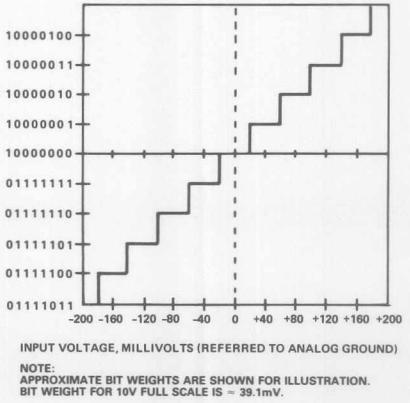


Figure 9b. Transfer Characteristic Around Major Carry for Bipolar Circuit of Figure 9a

INTERFACING THE AD7581

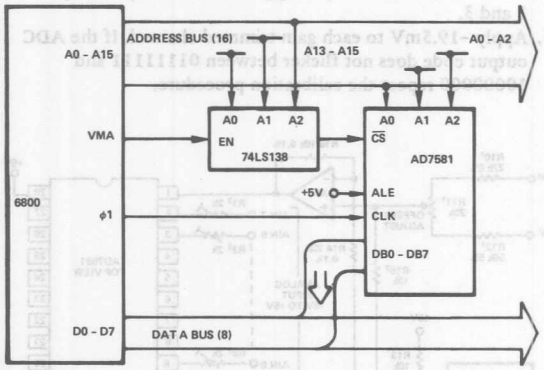


Figure 10. AD7581/6800 Interface

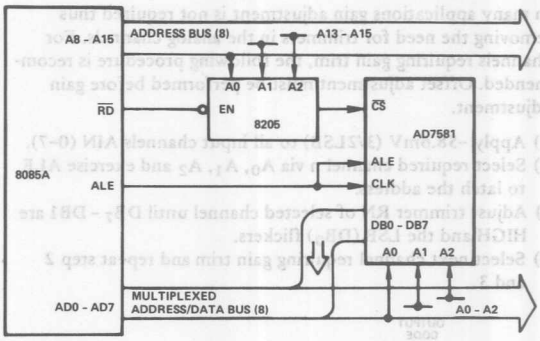


Figure 11. AD7581/8085 Interface

NOTES:

1. ANALOG AND DIGITAL GROUND
   It is recommended that A_{GND} and D_{GND} be connected locally to prevent the possibility of injecting noise into the AD7581. In systems where the A_{GND} – D_{GND} intertie is not local, connect back-to-back diodes (1N914 or equivalent) between the AD7581 A_{GND} and D_{GND} pins.

2. LOGIC DEGLITCHING IN μP APPLICATIONS
   Unspecified states on the address bus (due to different rise and fall times on the address bus) can cause glitches at the AD7581 $\overline{CS}$ terminal. These glitches can cause unwanted reads. The best way to avoid glitches is to gate the address decoding logic, e.g., with RD (8080), $\overline{RD}$ (8085) or VMA (6800).

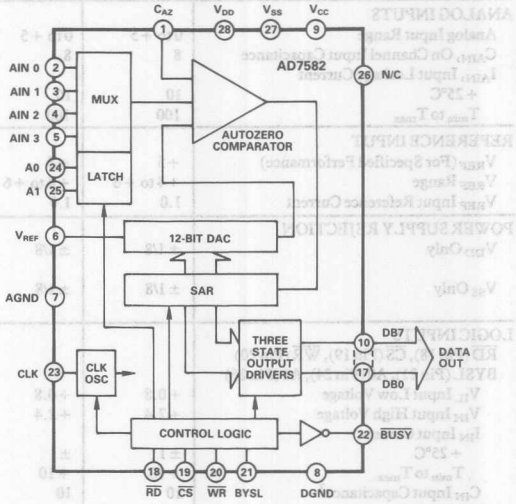
CMOS 12-Bit Successive Approximation ADC

AD7582

FEATURES

- 12-Bit Successive Approximation ADC
- Four High Impedance Input Channels
- Analog Input Voltage Range of 0 to +5V with Positive Reference of +5V
- Conversion Time of 100μs per Channel
- No Missed Codes Over Full Temperature Range
- Low Total Unadjusted Error ±1LSB max
- Autozero Cycle for Low Offset Voltage
- Monolithic Construction

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7582 is a medium speed, 4-channel 12-bit CMOS A/D converter which uses the successive approximation technique to provide a conversion time of 100μs per channel. An auto-zero cycle occurs at the start of each conversion resulting in very low system offset voltages, typically less than 100μV. The device is designed for easy microprocessor interface using standard control signals; $\overline{CS}$ (decoded device address), $\overline{RD}$ ($\overline{READ}$) and $\overline{WR}$ ($\overline{WRITE}$). The 4-channel input multiplexer is controlled via address inputs A0 and A1.

Conversion results are available in two bytes, 8LSB's and 4MSB's, over an 8-bit three state output bus. Either byte can be read first. Two converter busy flags are available to facilitate polling of the converter's status.

The analog input voltage range is 0V to +5V when using a reference voltage of +5V. The four analog inputs are all high impedance inputs with tight channel-to-channel matching–typically 0.1LSBs.

PRODUCT HIGHLIGHTS

1. The AD7582 is a complete 4 channel 12-bit A/D converter in either a 28-pin DIP or 28-terminal surface mount package requiring only a few passive components and a voltage reference.
2. Autozero cycle realizes very low offset voltages, typically 100μV.
3. The four channel input multiplexer (user addressable) features high input impedance and excellent channel-to-channel matching.
4. Standard microprocessor control signals to allow easy interfacing to most popular 8- and 16-bit microprocessors.

AD7582—SPECIFICATIONS (V_{DD} = +15V, V_{CC} = +5V, V_{SS} = −5V, V_{REF} = +5.0V f_{CLK} = 140kHz external, all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	K Version[1]	B Version[1]	T Version[1]	Units	Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Total Unadjusted Error[2]	±1	±1	±1	LSB max	All channels, AIN0–AIN3
Differential Nonlinearity	±1	±1	±1	LSB max	No missing codes guaranteed
Full Scale Error (Gain Error)	±1/4	±1/4	±1/4	LSB max	All channels, AIN0–AIN3 Full Scale TC is typically 5ppm/°C
Offset Error	±1/4	±1/4	±1/4	LSB max	All channels, AIN0–AIN3 Offset Error TC is typically 5ppm/°C
Channel to Channel Mismatch	±1/4	±1/4	±1/4	LSB max	
ANALOG INPUTS					
Analog Input Range	0 to +5	0 to +5	0 to +5	V	V_{REF} = +5.0V
C_{AIN}, On Channel Input Capacitance	8	8	8	pF typ	
I_{AIN}, Input Leakage Current					AIN0–AIN3; 0 to +5V
+25°C	10	10	10	nA max	
T_{min} to T_{max}	100	100	100	nA max	
REFERENCE INPUT					
V_{REF} (For Specified Performance)	+5	+5	+5	V	±5%
V_{REF} Range	+4 to +6	+4 to +6	+4 to +6	V	Degraded transfer accuracy
V_{REF} Input Reference Current	1.0	1.0	1.0	mA max	V_{REF} = +5.0V
POWER SUPPLY REJECTION					
V_{DD} Only	±1/8	±1/8	±1/8	LSB typ	V_{DD} = +14.25V to +15.75V V_{SS} = −5V
V_{SS} Only	±1/8	±1/8	±1/8	LSB typ	V_{SS} = −4.75V to −5.25V V_{DD} = +15V
LOGIC INPUTS					
$\overline{RD}$ (Pin 18), $\overline{CS}$ (Pin 19), $\overline{WR}$ (Pin 20)					
BYSL (Pin 21), A0 (Pin 24), A1 (Pin 25)					
V_{IL} Input Low Voltage	+0.8	+0.8	+0.8	V max	V_{CC} = +5V ±5%
V_{IH} Input High Voltage	+2.4	+2.4	+2.4	V min	
I_{IN} Input Current					
+25°C	±1	±1	±1	μA max	V_{IN} = 0 to V_{CC}
T_{min} to T_{max}	+10	+10	+10	μA max	
C_{IN} Input Capacitance[3]	10	10	10	pF max	
CLK (Pin 23)					
V_{IL}, Input Low Voltage	+0.8	+0.8	+0.8	V max	V_{CC} = +5V ±5%
V_{IH}, Input High Voltage	+3.0	+3.0	+3.0	V min	
I_{IL}, Input Low Current	±10	±10	±10	μA max	
I_{IH}, Input High Current	+1.5	+1.5	+1.5	mA max	
LOGIC OUTPUTS					
DB0–DB7 (Pins 10–17), $\overline{BUSY}$ (Pin 22)[4]					
V_{OL}, Output Low Voltage	+0.4	+0.4	+0.4	V max	V_{CC} = +5V ±5%, I_{SINK} = 1.6mA[4]
V_{OH}, Output High Voltage	+4.0	+4.0	+4.0	V min	V_{CC} = +5V ±5%, I_{SOURCE} = 200μA
Floating State Leakage Current					
(Pins 10–17)	±1	±1	±1	μA max	V_{OUT} = 0V to V_{CC}
Floating State Output Capacitance	15	15	15	pF max	
CONVERSION TIME[5]					
With External Clock	100	100	100	μs min	f_{CLK} = 140kHz
With Internal Clock, T_A = +25°C	100/150	100/150	100/150	μs min/max	Using recommended clock components as shown in Figure 6.
POWER REQUIREMENTS[6]					
V_{DD}	+15	+15	+15	V NOM	±5% for specified performance
V_{SS}	−5	−5	−5	V NOM	±5% for specified performance
V_{CC}	+5	+5	+5	V NOM	±5% for specified performance
I_{DD}	7.5	7.5	7.5	mA max	Typically 4mA with V_{DD} = +15V
I_{SS}	7.5	7.5	7.5	mA max	Typically 3mA with V_{SS} = −5V
I_{CC}	100	100	100	μA typ	V_{IN} = V_{IL} or V_{IH}
	1.0	1.0	1.0	mA max	
Power Dissipation	75	75	75	mW typ	$\overline{WR}$ = $\overline{RD}$ = $\overline{CS}$ = $\overline{BUSY}$ = Logic HIGH

NOTES

[1]Temperature Range as follows: K Version; 0 to +70°C
B Version; −25°C to +85°C
T Version; −55°C to +125°C

[2]Includes Full Scale Error, Offset Error and Relative Accuracy.

[3]Sample tested to ensure compliance.

[4]I_{SINK} for $\overline{BUSY}$ (pin 22) is 1.0 milliamp.

[5]Conversion Time includes autozero cycle time.

[6]Power supply current is measured when AD7582 is inactive i.e., $\overline{WR}$ = $\overline{RD}$ = $\overline{CS}$ = $\overline{BUSY}$ = Logic HIGH.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +15V, V_{CC} = +5V, V_{SS} = −5V, V_{REF} = +5V)

Parameter	Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (K & B Grades)	Limit at T_{min}, T_{max} (T Grade)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2 (INT)[2]	200	240	280	ns min	$\overline{WR}$ Pulse Width (Internal Clock Operation)
t_2 (EXT)[2]	10	10	10	µs min	$\overline{WR}$ Pulse Width (External Clock Operation)
t_3	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_4	130	160	200	ns typ	
	200	250	300	ns max	$\overline{WR}$ to $\overline{BUSY}$ Propagation Delay
t_5	0	0	0	ns min	A0, A1 Valid to $\overline{WR}$ Setup Time
t_6	20	20	20	ns min	A0, A1 Valid to $\overline{WR}$ Hold Time
t_7	0	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Setup Time
t_8	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_9	200	240	280	ns min	$\overline{RD}$ Pulse Width
t_{10}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_{11}	50	50	50	ns min	BYSL to $\overline{RD}$ Setup Time
t_{12}	0	0	0	ns min	BYSL to $\overline{RD}$ Hold Time
t_{13}[3]	150	180	200	ns typ	
	200	240	280	ns max	$\overline{RD}$ to Valid Data (Bus Access Time)
t_{14}[4]	20	20	20	ns min	$\overline{RD}$ to Three State Output
	130	160	180	ns max	(Bus Relinquish Time)

NOTES
[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with $t_r = t_f = 20$ns (10% to 90% of +5V) and timed from a voltage level of +1.6V. Data is timed from V_{IH}, V_{IL} or V_{OH}, V_{OL}.
[2]When using an external clock source the $\overline{WR}$ pulse width must be extended to provide the minimum auto-zero cycle time of 10µs. See "External Clock Operation".
[3]t_{13} is measured with the load circuits of Figure 3 and defined as the time required for an output to cross 0.8V or 2.4V.
[4]t_{14} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 4.
Specifications subject to change without notice.

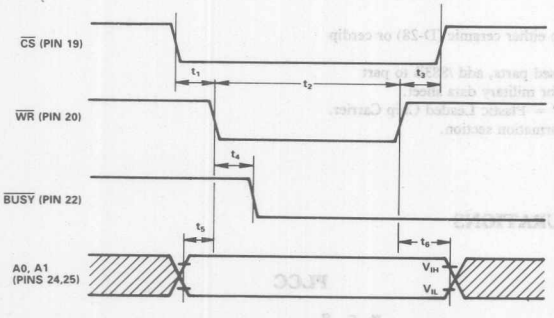


Figure 1. Start Cycle Timing

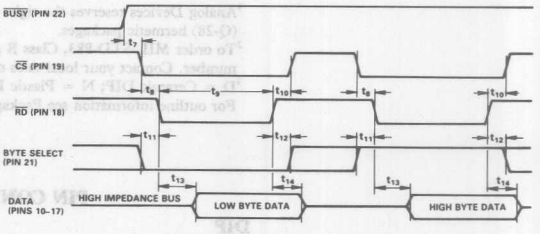
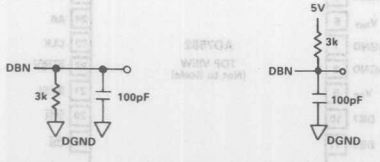
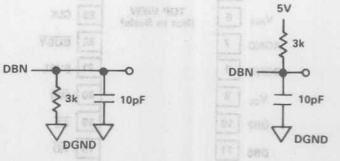


Figure 2. Read Cycle Timing



a. High-Z to V_{OH} b. High-Z to V_{OL}

Figure 3. Load Circuits for Access Time Test (t_{13})



a. V_{OH} to High-Z b. V_{OL} to High-Z

Figure 4. Load Circuits for Output Float Delay Test (t_{14})

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} to DGND	−0.3V, +17V
V_{SS} to DGND	+0.3V, −7V
AGND to DGND	−0.3V, V_{REF} +0.3V
V_{CC} to DGND	−0.3V, V_{DD} +0.3V
V_{REF} to AGND	−0.3V, V_{DD} +0.3V
AIN (0-3) to AGND	−0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND (Pins 18-21, 23-25)	−0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND (Pins 10-17, 22)	−0.3V, V_{DD} +0.3V
Operating Temperature Range	
Commercial (K Version)	0 to +70°C
Industrial (B Version)	−25°C to +85°C
Extended (T Version)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C
Power Dissipation (any Package) to +75°C	1,000mW
Derate above +75°C by	10mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



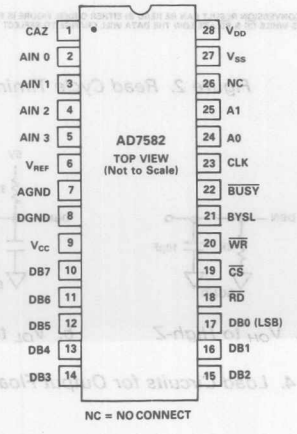
ORDERING GUIDE[1]

Model[2]	Temperature Range	Total Unadjusted Error T_{MIN}–T_{MAX}	Package Option[3]
AD7582KN	0°C to +70°C	±1LSB	N-28
AD7582BD	−25°C to +85°C	±1LSB	D-28
AD7582TD	−55°C to +125°C	±1LSB	D-28
AD7582KP	0°C to +70°C	±1LSB	P-28A

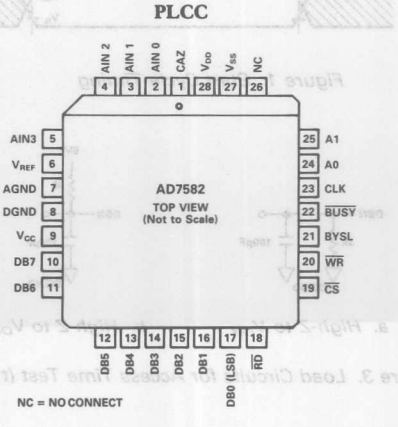
NOTES
[1]Analog Devices reserves the right to ship either ceramic (D-28) or cerdip (Q-28) hermetic packages.
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[3]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

PIN CONFIGURATIONS

DIP



PLCC



PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	CAZ	Autozero Capacitor Input. Connect other side of capacitor to AGND.
2	AIN 0	Analog Input, channel 0
3	AIN 1	Analog Input, channel 1
4	AIN 2	Analog Input, channel 2
5	AIN 3	Analog Input, channel 3
6	V_{REF}	Voltage reference input. The AD7582 is specified with $V_{REF} = +5.0V$.
7	AGND	Analog Ground
8	DGND	Digital Ground
9	V_{CC}	Logic Supply. For $V_{CC} = +5V$ digital inputs and outputs are TTL compatible.
10-17		Three state data outputs. They become active when $\overline{CS}$ & $\overline{RD}$ are brought low. Individual pin function is dependent upon the Byte Select (BYSL) input.

DATA BUS OUTPUT, $\overline{CS}$ & $\overline{RD}$ = LOW

	BYSL = HIGH	BYSL = LOW
Pin 10	BUSY[1]	DB7
Pin 11	LOW[2]	DB6
Pin 12	LOW[2]	DB5
Pin 13	LOW[2]	DB4
Pin 14	DB11 (MSB)	DB3
Pin 15	DB10	DB2
Pin 16	DB9	DB1
Pin 17	DB8	DB0 (LSB)

[1]BUSY (Pin 10) is a converter status flag and is HIGH during a conversion.
[2]Pins 11-13 output a logic LOW when BYSL is HIGH.
DB11–DB0 are the 12-bit conversion results, DB11 is the MSB.

18	$\overline{RD}$	READ input. This active LOW signal, in combination with $\overline{CS}$, is used to enable the output data three-state drivers.
19	$\overline{CS}$	CHIP SELECT Input. Decoded device address, active LOW. Used in combination with either $\overline{RD}$ or $\overline{WR}$ for control.
20	$\overline{WR}$	WRITE Input. This active LOW signal, in combination with $\overline{CS}$, is used to start a new conversion on a selected channel. When the AD7582 internal clock is used, the minimum $\overline{WR}$ pulse width is t2 (INT). When an external clock source is used, the minimum $\overline{WR}$ pulse width must be extended to include the autozero cycle time. For external clock operation, the minimum $\overline{WR}$ pulse width is t2 (EXT).
21	BYSL	BYTE SELECT. This control input determines whether the high or low byte of data is placed on the output data bus during a data READ operation ($\overline{CS}$ & $\overline{RD}$ LOW). See description of pins 10-17.
22	$\overline{BUSY}$	$\overline{BUSY}$ indicates converter status. $\overline{BUSY}$ is LOW during conversion, otherwise $\overline{BUSY}$ is held at a logic HIGH.
23	CLK	CLOCK Input for internal/external clock operation. Internal : Connect R_{CLK} and C_{CLK1}/C_{CLK2} timing components. See Figure 6 and Figure 7. External : Connect external 74HC compatible clock source as shown in Figure 8.
24	AO	Address Input AO. See pin 25 description.
25	A1	Address Input A1. Address inputs AO and A1 select the input channel to be converted. The address input latch is transparent when $\overline{CS}$ & $\overline{WR}$ are LOW. The address inputs are latched by $\overline{WR}$ returning HIGH.

A1	A0	CHANNEL SELECTED
0	0	AIN 0
0	1	AIN 1
1	0	AIN 2
1	1	AIN 3

26	N/C	No connect pin.
27	V_{SS}	Negative supply, −5V.
28	V_{DD}	Positive supply, +15V.

OPERATIONAL DIAGRAM

An operational diagram for the AD7582 is shown in Figure 5. The only passive components required are the autozero capacitor C_{AZ} and timing components R_{CLK}, C_{CLK1} & C_{CLK2} for the internal clock oscillator. If the AD7582 is to be used with an external clock source, then only C_{AZ} is required. Individual pin functions are described in detail on the previous page.

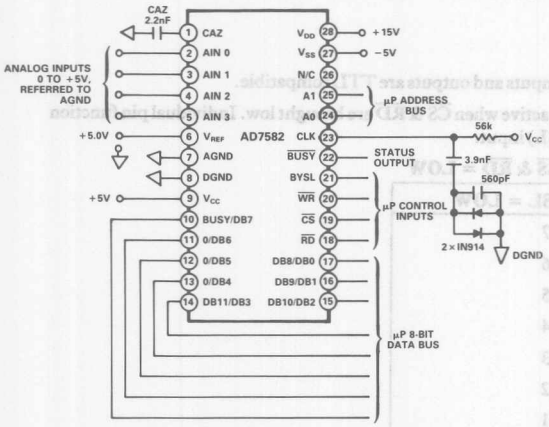


Figure 5. AD7582 Operational Diagram

INTERNAL CLOCK OPERATION

The clock circuitry for internal clock operation is shown in Figure 6 and the AD7582 operating waveforms are shown in Figure 7.

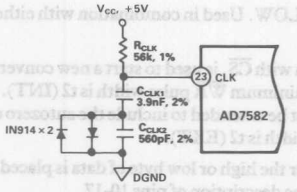


Figure 6. Circuitry Required for Internal Clock Operation

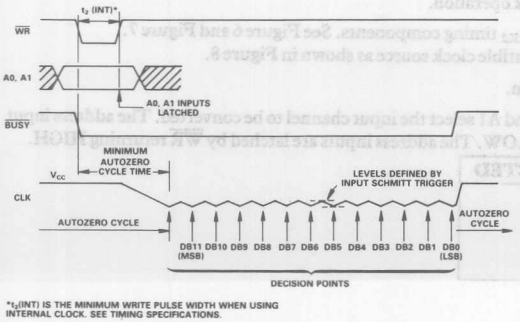


Figure 7. Operating Waveforms – Internal Clock

between conversions (BUSY = HIGH) the AD7582 is in the autozero cycle. When $\overline{WR}$ goes LOW (with $\overline{CS}$ LOW) to start a new conversion, the input multiplexer is switched to the selected channel N, via address inputs A0, A1. The autozero capacitor C_{AZ} now charges to AIN N–V_{OS} where V_{OS} is the input offset voltage of the autozero comparator.

A minimum time of 10μs is required for this autozero cycle. In applications using the internal clock oscillator, it is not necessary for $\overline{WR}$ to remain LOW for this period of time since it is automatically provided by the AD7582. This is achieved by switching a constant current load across the clock capacitors, C_{CLK1} and C_{CLK2}, causing the voltage at the CLK input pin to slowly decay from V_{CC}. This occurs after $\overline{WR}$ returns HIGH; $\overline{WR}$ returning HIGH also latches the multiplexer address inputs A0, A1 (see Figure 7). The Schmitt trigger circuit monitoring the voltage on the CLK input ends the autozero cycle when its LOW input trigger level is reached. At this point, the constant current load across the clock capacitors is removed allowing them to charge towards V_{CC} via R_{CLK}. When the voltage at the CLK input reaches the HIGH trigger level, the constant current load is replaced across C_{CLK1} and C_{CLK2}. The MSB decision is made when the LOW trigger level is reached. This cycle repeats itself 12 times to provide 12 clock pulses for the conversion cycle. The circuit arrangement of Figure 6 provides the relatively slow autozero cycle time at the beginning of a conversion while allowing the clock oscillator to speed up once the autozero cycle is complete.

EXTERNAL CLOCK OPERATION

For external clock operation R_{CLK}, C_{CLK1} and C_{CLK2} are discarded and the CLK input is driven from a 74HC compatible clock source. The mark/space ratio of the external clock can vary from 40/60 to 60/40. The AD7582 $\overline{WR}$ pulse width must now be extended to provide the minimum autozero cycle time of 10μs since this is no longer provided automatically by the AD7582. Referring to the operating waveforms of Figure 9, the minimum $\overline{WR}$ pulse width when using an external clock source is t_2 (EXT). Multiplexer address inputs A0 and A1, in addition to the $\overline{CS}$ input must now remain valid for the external $\overline{WR}$ pulse width. One approach to stretching the available μP signals is shown in the general 8-bit μP interface circuit of Figure 20. It is not necessary to synchronize the external clock source with the extended $\overline{WR}$ pulse width, the MSB decision being made on the second falling edge of the clock input after the $\overline{WR}$ input returns HIGH.

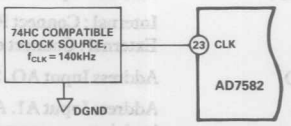


Figure 8. External Clock Operation

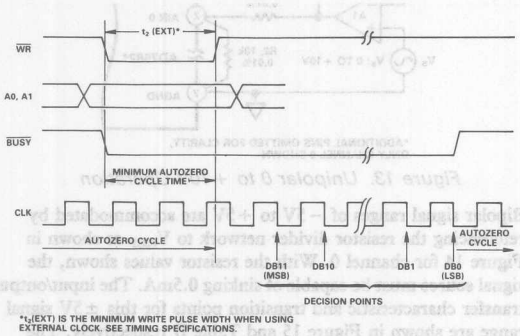


Figure 9. Operating Waveforms – External Clock

READING DATA

The 12-bit conversion data plus a converter status flag are available over an 8-bit wide data bus. Data is transferred from the AD7582 in right-justified format (i.e., the LSB is the most right-hand bit in a 16-bit word). Two READ operations are required, the Byte Select (BYSL) input determining which byte–8 least significant bits or 4 most significant bits plus status flag–is to be read first.

Since the AD7582 uses the successive approximation register (SAR) to hold conversion results (refer to Functional Diagram), it is necessary to wait until a conversion is finished before reading valid 12-bit data. Executing a READ instruction (HIGH or LOW byte) to the AD7582 while a conversion is in progress will place the existing contents of the SAR onto the data bus. Three different approaches can ensure valid 12-bit data is available for reading.

1. Insert a software delay greater than the ADC conversion time between the conversion start instruction and the data read instructions.
2. At user-defined intervals after a conversion start instruction, poll the internal converter status flag, BUSY. This signal is available on pin 10 during a HIGH byte READ instruction and is the most left-hand bit in a 16-bit right-justified word. The status bit can be shifted into a microprocessor's accumulator-carry position for testing (BUSY is HIGH during conversion).
3. Use the externally available $\overline{\text{BUSY}}$ (pin 22) signal as an interrupt to the microprocessor. This signal is LOW during a conversion and returns HIGH at conversion end.

Executing a WRITE instruction while conversion is in progress will restart the conversion.

COMPONENT SELECTION

1. Autozero Capacitor, C_{AZ}

   The autozero capacitor must be a low leakage, low dielectric absorption type such as polystyrene, polypropylene or teflon. To minimize noise connect the outside foil of C_{AZ} to AGND (pin 7), the analog system ground. C_{AZ} should be 2,200pF.

2. Clock Oscillator Components, R_{CLK}, C_{CLK1} and C_{CLK2}

   Clock pulses are generated by the action of series connected capacitors, C_{CLK1} and C_{CLK2} charging through an external resistor R_{CLK} and discharging through an internal switch. Nominal conversion time versus temperature for the recommended R_{CLK} and C_{CLK1}/C_{CLK2} combination is shown in Figure 10. Due to process variations, the actual operating frequency for this R_{CLK} and C_{CLK1}/C_{CLK2} combination can vary from device to device by up to 20%. For this reason, Analog Devices recommends using an external clock in the following situations:

   a. Applications requiring a conversion time which is within 20% of 100µs, the minimum conversion time for specified accuracy (a 140kHz clock frequency gives a 100µs conversion time).

   b. Applications which cannot accommodate conversion time differences which may occur due to unit clock frequency variations or temperature variations.

   It is possible to replace the fixed R_{CLK} resistor with a 50k potentiometer in series with a fixed 22kΩ resistor to allow individual adjustment of internal clock frequency in applications where 100µs conversion times are required. Reducing the value of R_{CLK} from 56k to 47k decreases the conversion time by typically 15µs.

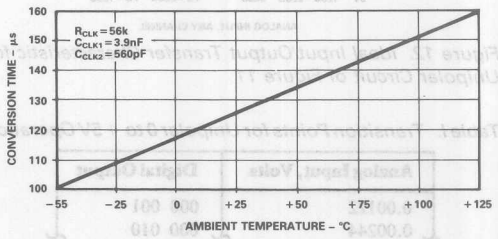


Figure 10. Typical Conversion Time vs. Temperature Using Internal Clock

APPLYING THE AD7582

The high input impedance of the analog channels, AIN0–AIN3, allows simple analog interfacing. Zero to +5V signal sources can be connected directly to the analog input channels without additional buffering for source impedances up to 5kΩ (see Figure 11). The input/output transfer characteristic and transition points for this input signal range are shown in Figure 12 and Table I respectively. The designed transition points on the AD7582 transfer characteristic occur on integer multiples of 1LSB. The output code is Natural Binary with 1LSB = (F.S.) (1/4096) = (5/4096)V = 1.22mV.

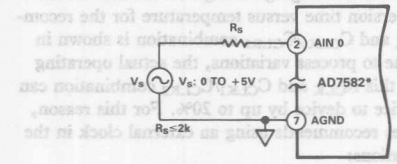


Figure 11. Unipolar 0 to +5V Operation

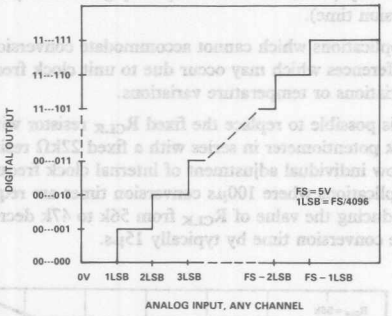


Figure 12. Ideal Input/Output Transfer Characteristic for Unipolar Circuit of Figure 11

Table I. Transition Points for Unipolar 0 to +5V Operation

Analog Input, Volts	Digital Output
0.00122	000 001
0.00244	000 010
2.49878	011 111
2.50000	100 000
2.50122	100 001
4.99756	111 110
4.99878	111 111

Signal ranges other than 0 to +5V are easily accommodated by using resistor divider networks to produce 0 to +5V signal ranges at the AD7582 input pins. Figure 13 shows a divider network on channel 0 to allow an AIN 0 signal range of 0 to +10V. The input resistors must be selected to match within 0.01% and should be the same type and from the same manufacturer so that their temperature coefficients match. Note that since the source impedance has not been included in the resistor divider ratio, it must now be as low as possible. For Figure 13 with a source impedance of 0.5Ω the maximum error across the network is approximately 0.5LSB. The LSB size is (F.S.)(1/4096) = (10/4096)V = 2.44mV.

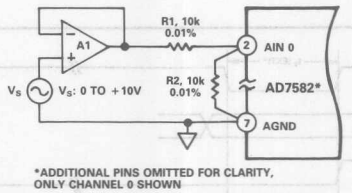


Figure 13. Unipolar 0 to +10V Operation

Bipolar signal ranges of −5V to +5V are accommodated by referencing the resistor divider network to V_{REF} as shown in Figure 14 for channel 0. With the resistor values shown, the signal source must be capable of sinking 0.5mA. The input/output transfer characteristic and transition points for this ±5V signal range are shown in Figure 15 and Table II respectively. The output code is Offset Binary with an LSB size of (F.S.)(1/4096) = (10/4096)V = 2.44mV.

With an analog input (V_S) of −1.22mV, the input offset voltage of A1 should be adjusted until the ADC output flickers between 0111 1111 1111 and 1000 0000 0000. Alternatively the −1/2LSB signal offset can be included in the signal conditioning electronics.

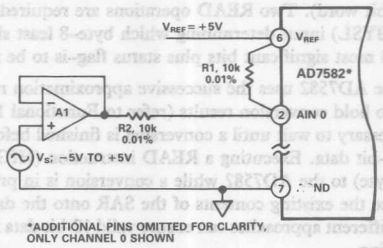


Figure 14. Bipolar −5V to +5V Operation

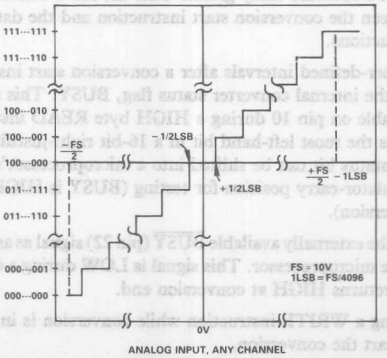


Figure 15. Ideal Input/Output Transfer Characteristic for Bipolar Circuit of Figure 14

Table II. Transition Points for Bipolar −5V to +5V Operation

Analog Input, Volts	Digital Output
−4.99878	000 001
−4.99634	000 010
−0.00122	100 000
+0.00122	100 001
+4.99389	111 110
+4.99634	111 111

Applications

Power Supply Decoupling: All power supplies to the AD7582 should be bypassed with either 10μF tantulum or electrolytic capacitors. To ensure good high frequency performance, each capacitor should be bypassed with an 0.01μF disc ceramic capacitor. All capacitors should be placed as close as possible to the AD7582.

Reference Circuit: Figure 16 shows how to configure an AD584LH to produce a reference voltage of 5.00V. R2 provides a typical adjustment range of ±75mV. The AD584LH will contribute less than 1LSB of gain error over the commercial temperature range.

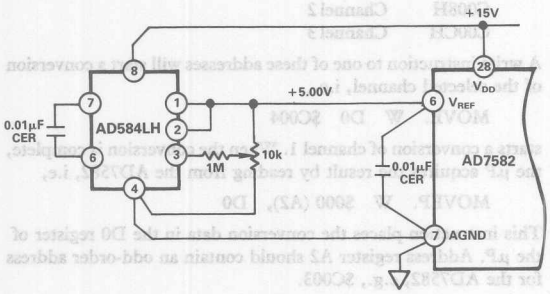


Figure 16. AD584LH as Reference Generator

Transient currents flow at the V_{REF} input during a conversion. To avoid dynamic errors place a 0.01μF disc ceramic from the V_{REF} pin to AGND.

Proper Layout: Layout for a printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or close to the autozero capacitor. The analog inputs, the reference input and the autozero input should be screened by AGND.

A single point analog ground separate from the logic system ground should be established at pin 7 (AGND) or as close as possible to the AD7582. This single point analog ground should be connected to the digital system ground, to which pin 8 (DGND) is connected, at one point only and as close to the AD7582 as possible. The autozero capacitor, bypass capacitors for the reference input and the analog supplies, AIN commons and any input signal screening should be returned to the analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible.

Noise: Input signal leads to AIN 0-3 and signal return leads from AGND (pin 7) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible, a shielded cable between source and ADC is recommended. Also since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

In applications where the AD7582 data outputs are connected to a continuously busy (and noisy) microprocessor bus it is possible to get LSB errors in conversion results. These errors are due to feedthrough from the microprocessor bus to the autozero comparator. The problem exists only for ceramic package versions of the AD7582, the electrically isolated metal lid acting like a conductor to distribute the digital noise around the package.

Grounding the lid to DGND eliminates this problem. Alternatively the AD7582 can be isolated from the microprocessor bus by means of three-state buffers.

Microprocessor Interfacing

MICROPROCESSOR INTERFACING

When the AD7582 is used with its own internal clock oscillator, microprocessor interfacing is straightforward and requires at most a few external gates (see Figures 17 through 19, 21 and 22). When the AD7582 is used with an external clock source, additional circuitry is required to extend the μP control signals (see Figure 20).

MC6800, MC6809 and 6502 MICROPROCESSORS

A typical interface to the AD7582 with any of the above microprocessors is shown in Figure 17. The decoder can be enabled high using VMA in 6800 systems or enabled low by NOR'ing ϕ_0 and ϕ_2 in 6502 systems or by NOR'ing E and Q in 6809 systems. Address lines A0, A1, and A2 of the 6800 have been tied to A0, A1 and BYSL respectively of the AD7582. Assuming the AD7582 is assigned a memory block starting at address 8000H, the input multiplexer is addressed as follows:

8000H	Channel 0
8001H	Channel 1
8002H	Channel 2
8003H	Channel 3

A write instruction to one of these addresses will start a conversion of the selected channel. To read the conversion results, it is necessary only to bring control inputs $\overline{CS}$ and $\overline{RD}$ low. The BYSL input (tied to A2 of the μP) determines whether the data high or low byte is placed onto the 8-bit data bus. A read instruction to any one of the previous channel addresses will result in the low byte of data being transferred to the μP (BYSL = Low). Similarly a read instruction to any address having A2 HIGH and within the assigned memory block, e.g., 8004H, transfers the high byte of data to the μP. The converter status flag BUSY can be polled at intervals to check whether the present conversion has finished and valid 12-bit data is available. This is accomplished by the following instructions on the 6800:

```
LDA   A   $8004      Load Flag from AD7582
ASL   A              Shift Flag into Carry
BCC       FETCH      Branch to Data Fetch
                     Subroutine if BUSY is LOW
```

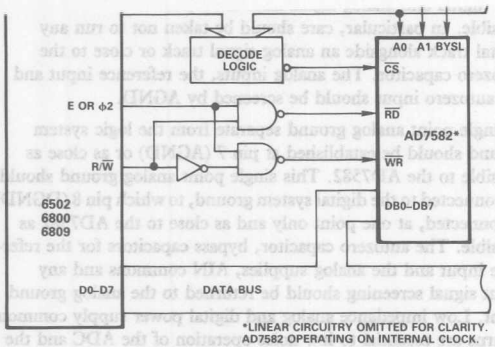


Figure 17. AD7582 – MC6800, 6809, 6502 Interface

8085A, Z80 MICROPROCESSORS

A typical interface to either of these microprocessors is shown in Figure 18. Not shown in the figure is the 8-bit latch required to demultiplex the 8085A common address/data bus. This interface uses slightly different low-level address decoding than the previous interface. Address lines A0, A1 & A2 of the µP have been tied to BYSL, A0 & A1 respectively of the AD7582. This allows the 16-bit data move instructions on both the 8085A and the Z80 to be used when reading conversion results. Assuming the AD7582 is again assigned a memory block starting at address 8000H the input multiplexer is now addressed as follows:

8000H	Channel 0
8002H	Channel 1
8004H	Channel 2
8006H	Channel 3

A write instruction to one of these addresses will start a conversion of the selected channel. The 12-bit conversion results can be read (low byte first then high byte) by a single read instruction;

On the 8085A

LHLD 8000

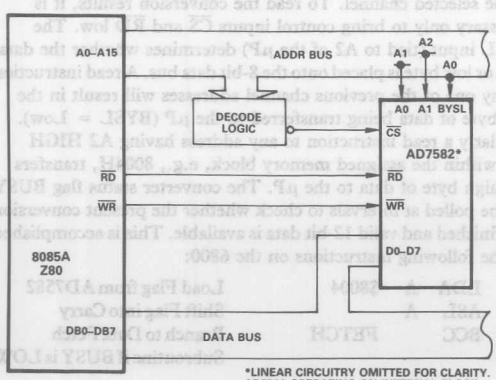


Figure 18. AD7582 – 8085A, Z80 Interface

LD BC, (8000)

moves the conversion results into register pair BC

MC68000, MC68008 MICROPROCESSOR

Figure 19 shows an AD7582–MC68000/MC68008 interface.

Address lines A1, A2 and A3 of the µP are connected to BYSL, A0 & A1 inputs respectively of the AD7582.

With the simple decoding logic shown in Figure 19, the AD7582 is decoded in a memory block from C000H to FFFFH. The input multiplexer is now addressed as follows:

C000H	Channel 0
C004H	Channel 1
C008H	Channel 2
C00CH	Channel 3

A write instruction to one of these addresses will start a conversion of the selected channel, i.e.,

MOVE. W D0 $C004

starts a conversion of channel 1. When the conversion is complete, the µP acquires the result by reading from the AD7582, i.e,

MOVEP. W $000 (A2), D0

This instruction places the conversion data in the D0 register of the µP. Address register A2 should contain an odd-order address for the AD7582, e.g., $C003.

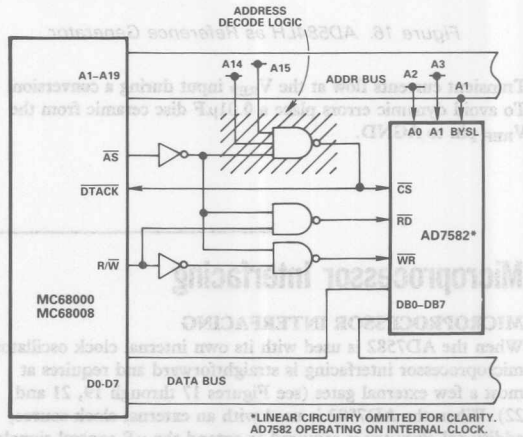


Figure 19. AD7582 – MC68000/MC68008 Interface

MICROPROCESSOR INTERFACE TO AD7582 WITH EXTERNAL CLOCK

Figure 20 shows the additional circuitry generally required to interface an 8-bit µP to the AD7582 operating from an external clock source. During a write operation, the 74121 monostable (one-shot) is triggered to latch the data (A0, A1 and $\overline{CS}$) in the 7477, a 4-bit bistable latch. The monostable timing components (not shown in Figure 20) should be chosen to provide an output pulse width corresponding to t_2 (EXT), the minimum autozero cycle time. To avoid any possibility of spurious triggering, the monostable should be enabled by a valid memory address signal. During a data read cycle, the 7477 latch is transparent and data is read normally. Note that the µP write and read cycle times are unaffected by the interface circuitry.

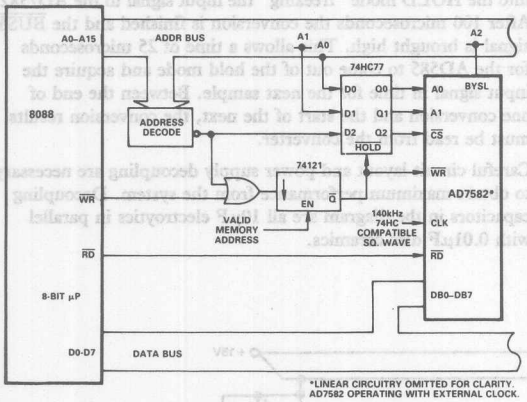


Figure 20. Interface to AD7582 Using External Clock

8088, 8086 MICROPROCESSORS

Figure 21 shows an AD7582–8088 interface.

Address lines A0, A1 and A2 are connected to BYSL, A0 and A1 inputs respectively of the AD7582. With the simple decoding shown in Figure 21 the AD7582 is decoded in a memory block from 4000H to 7FFFH. The input multiplexer is now addressed as follows:

4000H	Channel 0
4002H	Channel 1
4004H	Channel 2
4006H	Channel 3

A write instruction to one of these addresses will start a conversion of the selected channel, i.e,

MOV 4004, AX

starts a conversion of channel 2. When the conversion is finished the 8088 acquires the result by reading from the AD7582, i.e.,

MOV AX, 4000

places the conversion data in the accumulator.

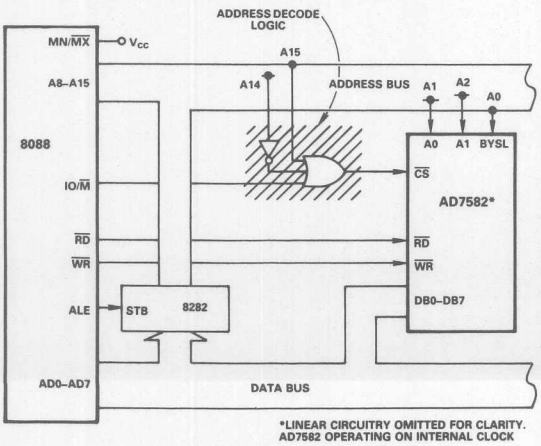


Figure 21. AD7582 – 8088 Interface

Figure 22 shows an AD7582–8086 interface. Address lines A1, A2 and A3 are connected to BYSL, A0 and A1 inputs respectively of the AD7582. The AD7582 is again decoded in a memory block from 4000H to 7FFFH. The input multiplexer is now addressed as follows:

4000H	Channel 0
4004H	Channel 1
4008H	Channel 2
400CH	Channel 3

A write instruction to one of these addresses will start a conversion of the selected channel, i.e,

MOV 4008, AX

starts a conversion of channel 2. When the conversion is finished, the 8086 acquires the result by reading from the AD7582 in two read cycles, i.e.,

MOV AL, 4000
MOV AH, 4002

places the conversion data in the accumulator.

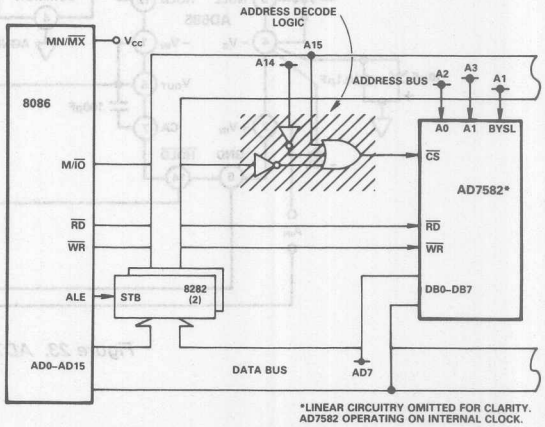


Figure 22. AD7582 – 8086 Interface

AD7582-AD585 SAMPLE-HOLD INTERFACE

Figure 23 shows an AD585 Sample-Hold Amplifier driving A_{IN1} of the AD7582. At a sampling frequency of 8kHz the maximum input signal frequency is 4kHz. The AD7582 is configured for bipolar operation to allow an input signal swing of ±5V. No clock components are shown for the AD7582 but the conversion time of the AD7582 should be adjusted for 100 microseconds. With an external hold capacitor of 100pF, the acquisition time for the sample-hold amplifier is 10 microseconds. The circuit operates from 0°C to +70°C.

To take a sample of the input, a WRITE instruction is executed to the AD7582 control inputs. The converter busy flag, $\overline{BUSY}$, is driven low indicating that a conversion is in progress. The falling edge of this $\overline{BUSY}$ signal places the sample-hold amplifier into the HOLD mode "freezing" the input signal to the AD7582. After 100 microseconds the conversion is finished and the $\overline{BUSY}$ signal is brought high. This allows a time of 25 microseconds for the AD585 to come out of the hold mode and acquire the input signal in time for the next sample. Between the end of one conversion and the start of the next, the conversion results must be read from the converter.

Careful circuit layout and power supply decoupling are necessary to obtain maximum performance from the system. Decoupling capacitors in the diagram are all 10μF electroytics in parallel with 0.01μF disc ceramics.

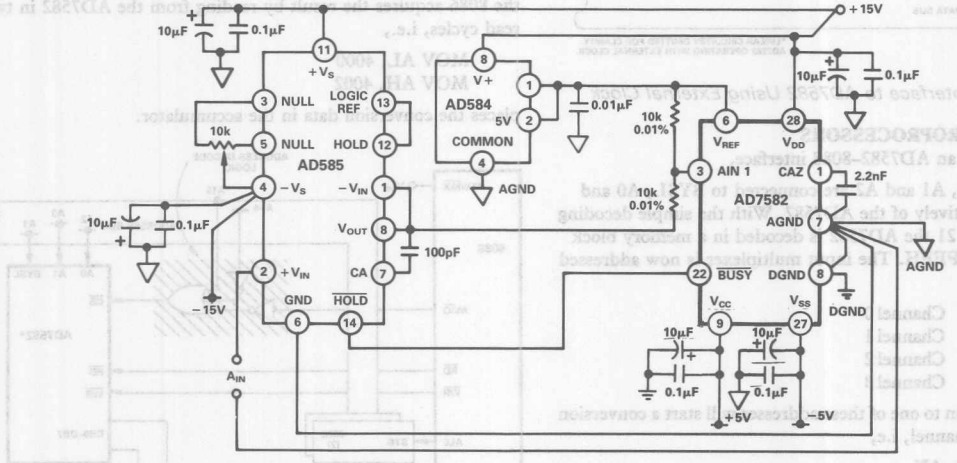


Figure 23. AD7582-AD585 Interface

LC²MOS 12-Bit 1 µs ADC

AD7586

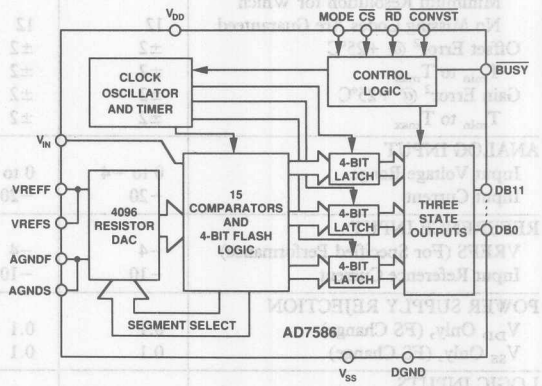
FEATURES

1 µs Conversion Time
AGND and VREF Force/Sense Connections
12-Bit Monotonic over Temperature
Low Power – 200 mW typ
Fast Bus Access Time – <57 ns

APPLICATIONS

Measurement and Control
Automatic Test Equipment
Precision Servo Control
All Data Acquisition Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7586 is a very fast 12-bit ADC that operates from ±5 V power supplies, offering high-speed performance combined with low power dissipation. The AD7586 is a triple-pass flash ADC, which uses 15 comparators in a 4-bit flash technique to achieve 12-bit accuracy in 1 µs conversion time. Each of the 4096 quantization voltage levels are realized internally with a precision resistor DAC. The use of thin-film resistor technology and on-chip force and sense amplifiers ensure 12-bit performance.

The AD7586 has a facility to force/sense the AGND and VREF inputs minimizing offset and gain errors. The precision resistor DAC with its excellent temperature drift characteristics combined with 12-bit accurate comparators provide 12-bit linearity over the entire temperature range.

The AD7586 has a high-speed digital interface with three-state data outputs. Data access and conversion start functions are controlled by $\overline{CS}$ and $\overline{RD}$ inputs, standard microprocessor signals. Conversion control can also be provided by a $\overline{CONVST}$ input for DSP applications. The data access time of less than 57 ns means that the AD7586 can interface directly to most modern microprocessors including DSP processors.

The AD7586 is fabricated in Analog Devices' Linear Compatible CMOS process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic.

PRODUCT HIGHLIGHTS

1. Fast 1 µs Conversion Time.
   Fast 1 µs conversion time makes the AD7586 suitable for a wide range of data acquisition applications.
2. Fast Microprocessor Interface.
   Standard control signals, $\overline{CS}$ and $\overline{RD}$, and fast bus access times make the AD7586 easy to interface to microprocessors
3. Low Power.
   LC²MOS fabrication process gives low power dissipation of 200 mW typically.

AD7586—SPECIFICATIONS

(V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGNDF & AGNDS are Kelvin connected to 0 V, VREFF & VREFS are Kelvin connected to −4 V, DGND = 0 V. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J, A, S Versions[1]	K, B Versions[1]	Units	Test Conditions/Comments
ACCURACY				
Resolution	12	12	Bits	
Integral Linearity @ +25°C	±2	±1.5	LSB max	
T_{min} to T_{max}	±2	±1.5	LSB max	
Differential Nonlinearity	±1	±1	LSB max	
Minimum Resolution for Which No Missing Codes Are Guaranteed	12	12	Bits	
Offset Error[2] @ +25°C	±2	±2	LSB max	Kelvin Connections Reduce Offset Error
T_{min} to T_{max}	±2	±2	LSB max	by 2 LSBs Typically
Gain Error[2] @ +25°C	±2	±2	LSB max	Kelvin Connections Reduce Gain Error
T_{min} to T_{max}	±2	±2	LSB max	by 2 LSBs Typically
ANALOG INPUT				
Input Voltage Range	0 to −4	0 to −4	Volts	
Input Current	−20	−20	μA max	V_{IN} = 0 to −4 V
REFERENCE INPUT				
VREFS (For Specified Performance)	−4	−4	Volts	±2%
Input Reference Current	−10	−10	mA max	
POWER SUPPLY REJECTION				
V_{DD} Only, (FS Change)	0.1	0.1	LSB typ	V_{SS} = −5 V, V_{DD} = +4.75 V to +5.25 V
V_{SS} Only, (FS Change)	0.1	0.1	LSB typ	V_{DD} = 5 V, V_{SS} = −4.75 V to −5.25 V
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[3]	10	10	pF max	
LOGIC OUTPUTS				
DB11–DB0, $\overline{BUSY}$				
Output High Voltage, V_{OH}	4	4	V min	I_{SOURCE} = 200 μA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0				
Floating-State Leakage Current	±10	±10	μA max	
Floating-State Output Capacitance[3]	15	15	pF max	
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	V nom	±5% for Specified Performance
I_{DD}	30	30	mA max	Typically 20 mA, $\overline{CS}$ = $\overline{RD}$ = V_{DD}
I_{SS}	−30	−30	mA max	Typically 20 mA, $\overline{CS}$ = $\overline{RD}$ = V_{DD}
Power Dissipation	200	200	mW typ	$\overline{CS}$ = $\overline{RD}$ = 5 V
	300	300	mW max	

NOTES

[1]Temperature Ranges are as follows: J/K versions 0 to +70°C; A/B versions −40°C to +85°C; S version −55°C to +125°C.

[2]Without Kelvin connections on VREF and AGND the Offset and Gain Errors are typically 4 LSBs.

[3]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V)

Parameter	Limit at T_{min}, T_{max} (J, K Versions)	Limit at T_{min}, T_{max} (A, B Versions)	Limit at T_{min}, T_{max} (S Version)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_2	35	35	40	ns max	$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay (C_L = 10 pF)
t_3	20	20	14	ns min	Data Setup Time Prior to $\overline{BUSY}$, (C_L = 20 pF)
	10	10	0	ns min	Data Setup Time Prior to $\overline{BUSY}$, (C_L = 100 pF)
t_4[2]	10	10	10	ns min	Bus Relinquish Time after $\overline{RD}$
	55	55	65	ns max	
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6	35	35	40	ns max	$\overline{CONVST}$ to $\overline{BUSY}$ Propagation Delay
t_7	75	75	90	ns min	$\overline{CONVST}$ Pulse Width
t_8[3]	57	57	70	ns max	Data Access Time after $\overline{RD}$
t_9	60	60	75	ns min	$\overline{RD}$ Pulse Width
t_{10}	0	0	0	ns min	$\overline{BUSY}$ High to $\overline{RD}$ Low, (Mode 1)
t_{11}	25	25	25	ns min	$\overline{CS}$ High Time, (Mode 0)
t_{12}	0	0	0	ns min	$\overline{CS}$ High to $\overline{CONVST}$ Low, (Mode 1)
t_{13}	0	0	0	ns min	$\overline{BUSY}$ High to $\overline{CONVST}$ Low, (Mode 1)
t_{CONV}	950	950	950	ns typ	Conversion Time (Mode 0)
	1000	1000	1000	ns max	

NOTES

[1]Timing Specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]t_4 is derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time, t_4, quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

[3]t_8 is measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{SS} to AGND[2] . . . . . +0.3 V to −7 V
AGND to DGND . . . . . −0.3 V to V_{DD} +0.3 V
V_{IN} to AGND . . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
VREFF, VREFS to AGND . . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
Digital Inputs to DGND
$\overline{CS}$, $\overline{RD}$, $\overline{CONVST}$, Mode . . . . . −0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND
DB0 to DB11, $\overline{BUSY}$ . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Commercial (J, K Versions) . . . . . 0 to +70°C
Industrial (A, B Versions) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]If V_{SS} is open circuited with V_{DD} and AGND applied, the V_{SS} pin will be pulled positive, exceeding the Absolute Maximum Ratings. If this possibility exists, a Schottky diode from V_{SS} to DGND (cathode end to GND) ensures that the Absolute Maximum Ratings will be observed.

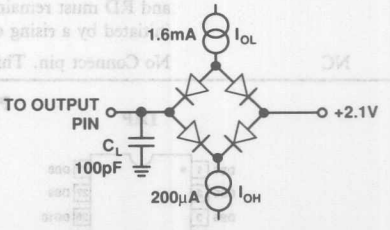


Figure 1. Load Circuit for Access and Relinquish Time

CAUTION

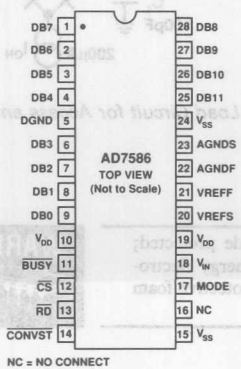
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



Number	Mnemonic	Description
POWER SUPPLY		
10 & 19	V_{DD}	Positive Power Supply, +5 V ±5%. Both V_{DD} pins must be tied together.
15 & 24	V_{SS}	Negative Power Supply, −5 V ±5%. Both V_{SS} pins must be tied together.
22	AGNDF	Analog Ground Force. The input can be used in conjunction with AGNDS to force/sense the external AGND (See Figure 3). Force/sensing the AGND minimizes offset error. In applications where offset error is not important these inputs can be tied together and connected directly to the external AGND reference.
23	AGNDS	Analog Ground Sense. This is the complementary input for AGNDF (above) to force/sense the analog ground reference. AGNDF and AGNDS are tied together internally.
5	DGND	Digital Ground.
ANALOG AND REFERENCE INPUTS		
18	V_{IN}	Analog Input. The analog input range is 0 to −4 V.
20	VREFS	Voltage Reference Sense Input. The input can be used in conjunction with VREFF to force/sense an external voltage reference (See Figure 3). Force/sensing the VREF input minimizes gain error. In applications where gain error is not important these inputs can be tied together and connected directly to an external reference.
21	VREFF	Voltage Reference Force Input. This is the complementary input for VREFS (above) to force/sense an external voltage reference. VREFF and VREFS are tied together internally.
INTERFACE		
1–4, 6–9	DB7–DB4, DB3–B0	Three-state data outputs. These outputs are controlled by $\overline{CS}$ and $\overline{RD}$. DB11 is the most significant bit, (MSB).
25–28	DB11–DB8	
11	$\overline{BUSY}$	$\overline{BUSY}$ output indicates converter status. $\overline{BUSY}$ is low during conversion.
12	$\overline{CS}$	Chip Select Input. The device is selected when this input is low.
13	$\overline{RD}$	Read Input. This active low signal, in conjunction with $\overline{CS}$ is used to enable the output data three-state drivers and initiate a conversion when the MODE input pin is tied low.
CONTROL		
14	$\overline{CONVST}$	Conversion Start Input. This input may be used to start conversion when the MODE input pin is tied high.
17	MODE	Mode Input. When this pin is low, conversion is initiated on the falling edge of $\overline{CS}$ and $\overline{RD}$. $\overline{CS}$ and $\overline{RD}$ must remain low for the duration of the conversion. When this pin is high conversion is initiated by a rising edge on the $\overline{CONVST}$ input.
16	NC	No Connect pin. This pin has no internal connections.

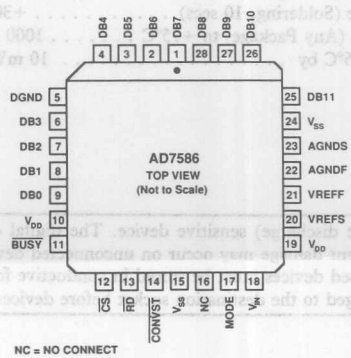
PIN CONFIGURATIONS

DIP



NC = NO CONNECT

PLCC



NC = NO CONNECT

ORDERING GUIDE

Model[1]	Temperature Range	Integral Nonlinearity	Package Option[2]
AD7586JN	0°C to +70°C	±2.0 LSB	N-28
AD7586KN	0°C to +70°C	±1.5 LSB	N-28
AD7586JP	0°C to+70°C	±2.0 LSB	P-28A
AD7586KP	0°C to+70°C	±1.5 LSB	P-28A
AD7586AQ[3]	−40°C to +85°C	±2.0 LSB	Q-28
AD7586BQ[3]	−40°C to +85°C	±1.5 LSB	Q-28
AD7586SQ[3]	−55°C to +125°C	±2.0 LSB	Q-28

NOTES
[1]Analog Devices reserves the right to ship J-Leaded Ceramic Chip Carrier packages in lieu of PLCC packages.
[2]J = J-Leaded Ceramic; N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information section.
[3]Contact your local sales office for availability.

OPERATIONAL DIAGRAM

An operational diagram for the AD7586 is shown in Figure 2. The only external component required for basic operation of the part is a −4 V reference.

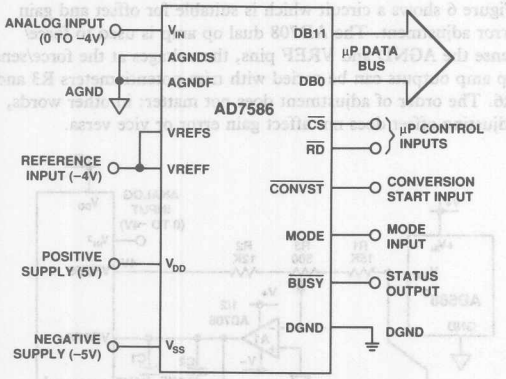


Figure 2. Operational Diagram

CONVERTER DETAILS

The AD7586 is a triple-pass flash ADC which uses 15 comparators in a 4-bit flash technique to perform the 12-bit conversion procedure. Each of the 4096 quantization levels is realized internally with a precision resistor DAC.

The fifteen comparators first compare the analog input voltage to the VREF/16 voltages of the resistor array. This determines the four most significant bits and selects 1 out of 16 voltage segments. The comparators are then switched to 15 subvoltages on that segment to determine the next four bits and select 1 out of 256 voltage segments. A further switching of the comparators to another 15 subvoltages produces the complete 12-bit conversion result. The 12 bits of data are then stored internally in a three-state output latch.

FORCE/SENSE CONNECTIONS

The AD7586 has a facility for Kelvin (force/sense) connections on the AGND and VREF pins to minimize offset and gain errors. Force/sensing these inputs eliminates error contributions from voltage or IR drops due to resistances from nonideal, internal conductors. IR drops in the AGND path cause an offset error while IR drops in the reference path cause a gain error. Typically, the use of Kelvin connections reduces the offset and gain errors by 2 LSBs.

A low op amp offset voltage is important as any offset voltage will add directly to the voltage that is being forced/sensed. Suitable op amps for this application are precision op amps such as the AD705, AD707 or the AD708 (dual op amp), all of which feature offset voltages of less than 100 µV.

REFERENCE INPUT

The AD7586 operates from a −4 V external reference. Figure 3 shows a typical reference connection circuit based on the AD586. The AD586 is a high performance voltage reference which exhibits excellent stability performance, 5 ppm/°C max. The AD586's +5 V output is scaled and inverted before being applied to the AD7586 VREF inputs. Proper decoupling on the force/sense op amp outputs is important to suppress high speed transients during the conversion procedure. Note, connecting capacitors directly to op amp outputs can cause stability problems. However, the use of large capacitors, 10 µF in Figure 3, limits the open-loop bandwidth preventing any closed-loop oscillations.

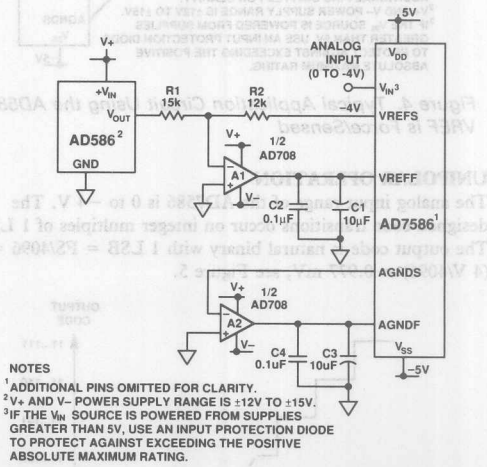


Figure 3. Typical Application Circuit Using the AD586, AGND and VREF Are Force/Sensed

Where offset and gain errors are not important, the force/sense op amps can be omitted and the force/sense pins can be tied together as shown for the AGND connection in Figure 4. However the reference circuitry will invariably use an external op amp to scale the reference input voltage to −4 V, this op amp can provide the second function of force/sensing at no extra cost. In all applications, both the AGND and the VREF pins must be driven from low impedance sources.

The AD586 is a precision voltage reference used for applications throughout this data sheet. However, other references exist which may be preferable in some applications. One example is the ZNREF040, 4 V reference, available from Plessey Semiconductor. This part is not as suitable for precision applications, its temperature drift specification is 50 ppm/°C. It does have the advantage of a smaller package size, 3-pin metal can.

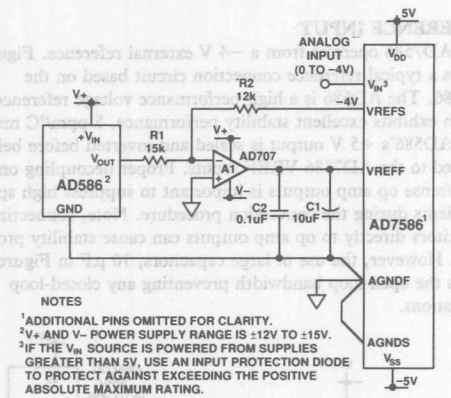


Figure 4. Typical Application Circuit Using the AD586, VREF is Force/Sensed

UNIPOLAR OPERATION

The analog input range of the AD7586 is 0 to −4 V. The designed code transitions occur on integer multiples of 1 LSB. The output code is natural binary with 1 LSB = FS/4096 = (4 V/4096) = 0.977 mV, see Figure 5.

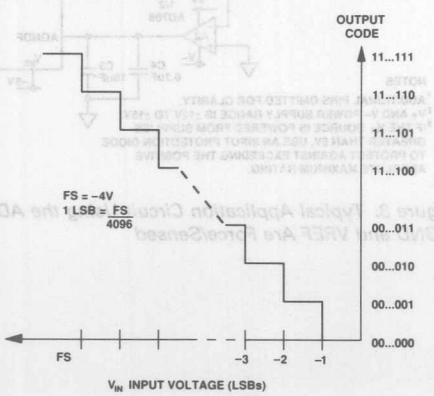


Figure 5. AD7586 Transfer Function

UNIPOLAR OFFSET AND GAIN ERROR ADJUST

Both offset and gain errors are less than 2 LSBs, when force/sense amplifiers are used for the reference and AGND pins, eliminating the need for calibrating the AD7586 in the majority of cases. However, applications requiring absolute accuracy may use the force/sense amplifiers to null any system offset or gain errors caused by signal conditioning or other external circuitry.

The overall transfer function can be calibrated as a "mid riser" type or a "mid tread" type. A mid riser type is where the code transitions occur on successive integer LSB values, the mid tread type is where the code transitions occur mid way between successive integer LSB values. The only difference between the two types is a 1/2 LSB offset, the first and last code transition voltages are shown below in Table I.

	Mid Tread	Mid Riser
First Code Transition Voltage (0000 0000 0000 to 0000 0000 0001)	−0.488 mV	−0.977 mV
Last Code Transition Voltage (1111 1111 1110 to 1111 1111 1111)	−3.9985 V	−3.9990 V

Table I. Ideal First and Last Transition Voltages for Unipolar Operation

Figure 6 shows a circuit which is suitable for offset and gain error adjustment. The AD708 dual op amp is used to force/sense the AGND and VREF pins, the voltages at the force/sense op amp outputs can be varied with trim potentiometers R3 and R6. The order of adjustment does not matter; in other words, adjusting offset does not affect gain error or vice versa.

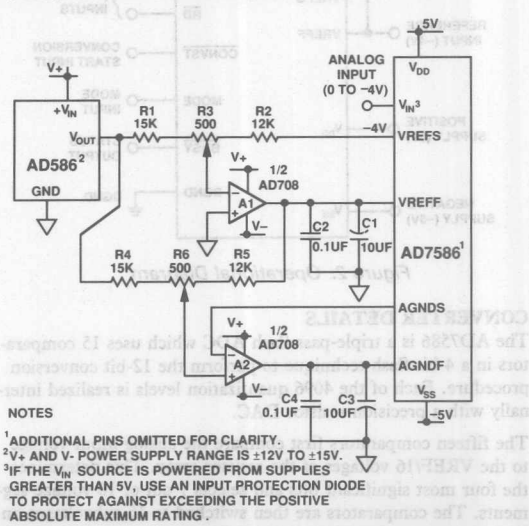


Figure 6. Unipolar Operation with Full-Scale Adjustment

Offset adjustment is achieved by adjusting the AGND force/sense voltage. To adjust the offset apply the first code transition voltage to V_{IN} (see Table I) and adjust R6 until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

Gain error can be nulled by adjusting the reference input which in turn adjusts the full-scale digital output. To adjust the full-scale output apply the last code transition voltage at V_{IN} and vary R3 until the output code flickers between 1111 1111 1110 and 1111 1111 1111.

BIPOLAR OPERATION

Figure 7 shows how bipolar operation can be achieved with the AD7586. The circuit uses an op amp to offset the analog signal by −2 V before being applied to the AD7586 analog input. The circuit has an analog input range of ±2 V with an LSB size of 0.997 mV. The output code is offset binary, see Figure 8 for the transfer function.

Signal ranges other than ±2 V are easily accommodated by using a different value of R3. For example, setting R3 equal to 30 k increases the analog input range to ±5 V. R3 should always be chosen such that the voltage range at V_{IN} covers the full dynamic range (0 to −4 V) of the ADC. All resistors should be the same type and from the same manufacturer so that their temperature coefficients match.

For ac sampling applications it is possible to substitute the op amp, A1, for a sample-and-hold amplifier SHA. Not all SHAs have both the inverting and noninverting terminals available to the user in which case the op amp is still necessary to level shift the analog input.

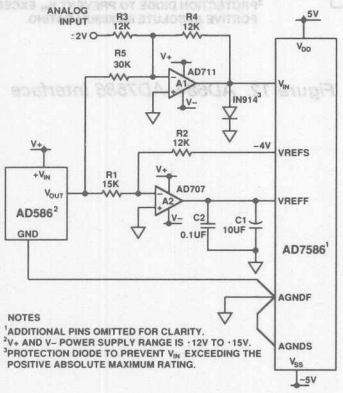


Figure 7. AD7586 Bipolar Operation

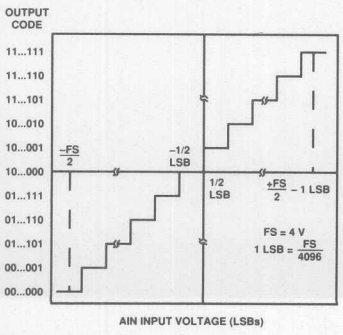


Figure 8. Ideal Input/Output Transfer Function for the Circuit of Figure 7

BIPOLAR OFFSET AND GAIN ERROR ADJUST

For applications where absolute accuracy is important then system offset and gain errors can be adjusted to zero using the force/sense amplifiers as in the unipolar case. In the case of Figure 7, one source of gain error is the resistor mismatch between R3 and R4. This error in conjunction with other gain error sources can be nulled by making either R2 or R3 variable and using the same adjustment procedure as discussed for the unipolar circuit. For offset adjustment, an AGND force/sense amplifier is needed with the same resistor biasing and trim arrangement as that shown in Figure 6 (R4, R5 and R6). Again, the adjustment procedure is the same as that discussed for Figure 6. Note, the analog input signal is level shifted by −2 V, therefore, −2 V must be subtracted from the first and last code transition voltages listed in Table I before being applied to this circuit.

TIMING AND CONTROL

Conversion start and data access are controlled by four digital inputs: $\overline{CS}$, $\overline{RD}$, $\overline{CONVST}$ and MODE. There are two basic modes of operation, Mode 0 and Mode 1 which are shown in Figures 9 to 11. Mode 0 is designed for applications where a microprocessor has complete control over conversion start and data access. Mode 1 is designed for DSP applications where a timer controls conversion start, ensuring equal sampling intervals, while data access is again controlled by a microprocessor. The AD7586 MODE input pin selects the timing mode: MODE = 0 V for Mode 0 and MODE = 5 V for Mode 1.

Mode 0 (MODE = 0 V)

For direct bus interfacing using Mode 0, the microprocessor must have a WAIT state facility. A read operation to the ADC brings $\overline{CS}$ and $\overline{RD}$ low which triggers a conversion. The AD7586 acknowledges by bringing $\overline{BUSY}$ low indicating that conversion is in progress. $\overline{BUSY}$ returns high at the end of conversion when the ADC's output latches have been updated and the conversion result is placed on the data outputs. Note the data bus is in the three-state condition for the duration of the conversion and becomes active before $\overline{BUSY}$ goes high (see t_3, Figure 9) at the end of conversion.

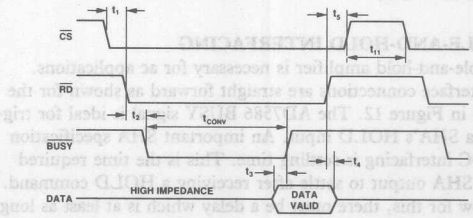


Figure 9. Mode 0 Timing Diagram (Mode = 0 V)

Mode 1 (MODE = 5 V)

In this mode conversion is started by asserting the $\overline{CONVST}$ input (see Figure 10). $\overline{BUSY}$ goes low after the falling of the $\overline{CONVST}$ input. However, the ADC conversion procedure does not start until after the rising of the $\overline{CONVST}$ pulse. $\overline{BUSY}$ returns high when conversion is complete. The total width of the $\overline{BUSY}$ pulse is equal to the $\overline{CONVST}$ pulse width plus the ADC conversion time. Note, the time t_{CONV} is typically 30 ns larger in Mode 1 than in Mode 0. Data can be read by a microprocessor any time after the rising edge of $\overline{BUSY}$. Note that pulsing $\overline{CONVST}$ low while a conversion is in progress will initiate a new conversion.

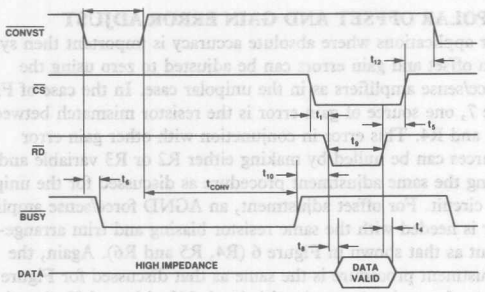


Figure 10. Mode 1 Timing Diagram (Mode = 5 V)

Figure 11 shows a variation of Mode 1 timing that is useful when external latches are used to store the conversion results. In this case, $\overline{CS}$ and $\overline{RD}$ are tied permanently low and the data bus is always active, except when $\overline{BUSY}$ is low. The data bus is in the three-state condition during the $\overline{BUSY}$ low state. The data bus then becomes active just before $\overline{BUSY}$ returns high at the end of conversion, so that $\overline{BUSY}$ can be used as a clocking signal for external latches.

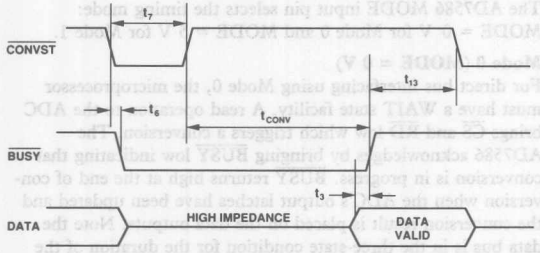


Figure 11. Mode 1 Timing Diagram, $\overline{CS}$ = $\overline{RD}$ = 0 V (Mode = 5 V)

SAMPLE-AND-HOLD INTERFACING

A sample-and-hold amplifier is necessary for ac applications. The interface connections are straight forward as shown for the AD684 in Figure 12. The AD7586 $\overline{BUSY}$ signal is ideal for triggering a SHA's HOLD input. An important SHA specification for ADC interfacing is settling time. This is the time required by the SHA output to settle after receiving a HOLD command. To allow for this, there must be a delay which is at least as long as the SHA settling time between the HOLD command and the AD7586's first flash decision. Large hold-mode settling time can be compensated for in Mode 1. The delay between the start of a conversion and the first flash decision is approximately 200 ns. In Mode 1 timing, $\overline{BUSY}$ goes low when $\overline{CONVST}$ goes low but the conversion procedure does not start until $\overline{CONVST}$ goes high. So, the $\overline{CONVST}$ pulse width can be used to compensate for any additional SHA settling time greater than 200 ns. For example, if a SHA has a settling time of 500 ns, then the $\overline{CONVST}$ pulse width should be 300 ns.

AD684 SAMPLE-AND-HOLD

The AD684 is a quad sample-and-hold (SHA) with an acquisition time of 1 μs. Figure 12 shows the SHA coupled with the calculate the overall throughput rate, the acquisition time and the settling time of the SHA along with the ADC conversion time have to be taken into account. For the single channel system shown in Figure 12, the minimum throughput time is approximately 2.5 μs. This figure allows for 1 μs each for acquisition and conversion time and 500 ns for settling time and other overheads.

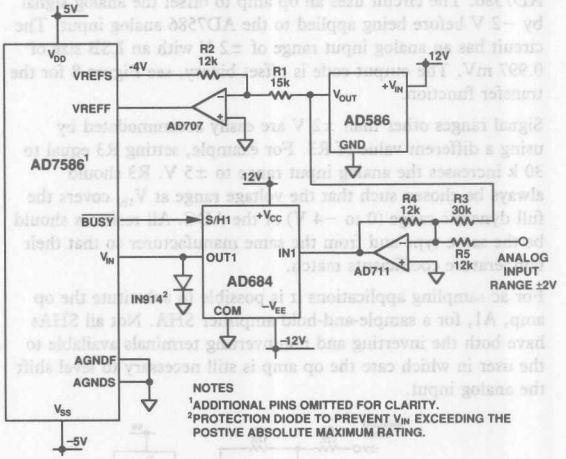


Figure 12. AD684–AD7586 Interface

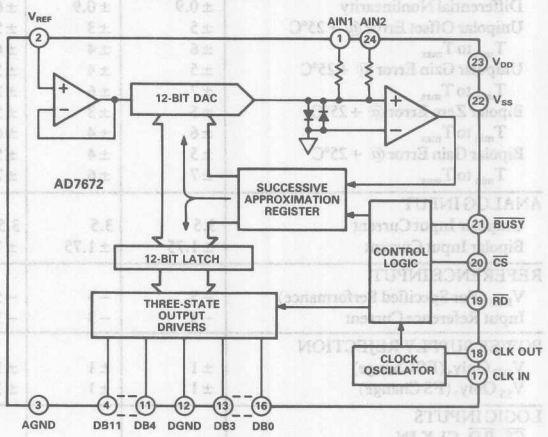
High-Speed 12-Bit ADC

AD7672

FEATURES

- 12-Bit Resolution and Accuracy
- Fast Conversion Time
  - AD7672XX03 – 3μs
  - AD7672XX05 – 5μs
  - AD7672XX10 – 10μs
- Unipolar or Bipolar Input Ranges
- Low Power: 110mW
- Fast Bus Access Times: 90ns
- Small, 0.3", 24-Pin Package and 28-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7672 is a high-speed 12-bit ADC, fabricated in an advanced, mixed technology, Linear-Compatible CMOS (LC^2MOS) process, which combines precision bipolar components with low-power, high-speed CMOS logic. The AD7672 uses an accurate high-speed DAC and comparator in an otherwise conventional successive-approximation loop to achieve conversion times as low as 3μs while dissipating only 110mW of power.

To allow maximum flexibility the AD7672 is designed for use with an external reference voltage. This allows the user to choose a reference whose performance suits the application or to drive many AD7672s from a single system reference, since the reference input of the AD7672 is buffered and draws little current. For digital signal processing applications where absolute accuracy and temperature coefficients may be unimportant, a low-cost reference can be used. For maximum precision, the AD7672 can be used with a high-accuracy reference, such as the AD588, when absolute 12-bit accuracy can be obtained over a wide temperature range.

An on-chip clock-circuit is provided which may be used with a crystal for accurate definition of conversion time. Alternatively, the clock input may be driven from an external source such as a microprocessor clock.

The AD7672 also offers flexibility in its analog input ranges, with a choice of 0 to +5V, 0 to +10V and ±5V.

The AD7672 is also designed to operate from nominal supply voltages of +5V and −12V. This makes it an ideal choice for data acquisition cards in personal computers where the negative supply is generally −12V.

The AD7672 has a high-speed digital interface with three-state data outputs and standard microprocessor control inputs (Chip Select and Read). Bus access time of only 90ns allows the AD7672 to be interfaced to most modern microprocessors.

The AD7672 is available in a variety of space-saving packages; plastic and hermetic 24-pin "skinny" DIP and 28-pin ceramic and plastic chip carrier.

PRODUCT HIGHLIGHTS

1. Fast, 3μs, 5μs and 10μs conversion speeds make the AD7672 ideal for a wide range of applications in telecommunications, sonar and radar signal processing or any high-speed data acquisition system.
2. LC^2MOS circuitry gives high precision with low power drain (110mW typ).
3. Choice of 0 to +5V, 0 to +10V or ±5V input ranges, accomplished by pin-strapping.
4. Fast, simple, digital interface has a bus access time of 90ns allowing easy connection to most microprocessors.
5. Available in space-saving 24-pin, 0.3" DIP or surface mount package.

AD7672—SPECIFICATIONS

(V_{DD} = 5V ± 5%, V_{SS} = −12V ± 10%, V_{REF} = −5V unless otherwise noted. f_{CLK}: 4MHz for AD7672XX03, 2.5MHz for AD7672XX05, 1.25MHz for AD7672XX10. All Specifications T_{min} to T_{max} unless otherwise noted. Specifications apply to Slow Memory Mode.)

Parameter	K Version[1]	L Version[1]	B Version[1]	C Version[1]	Units	Test Conditions/Comments
ACCURACY[2]						
Resolution	12	12	12	12	Bits	
Integral Nonlinearity @ +25°C	±1	±1/2	±1	±1/2	LSB max	Tested Range ±5V
T_{min} to T_{max}	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	±0.9	LSB max	No Missing Codes Guaranteed
Unipolar Offset Error @ +25°C	±5	±3	±5	±3	LSB max	Input Range: 0 to 5V or 0 to 10V
T_{min} to T_{max}	±6	±4	±6	±4	LSB max	Typical TC is 2ppm/°C
Unipolar Gain Error @ +25°C	±5	±4	±5	±4	LSB max	Input Range: 0 to 5V or 0 to 10V
T_{min} to T_{max}	±7	±6	±7	±6	LSB max	Typical TC is 2ppm/°C
Bipolar Zero Error @ +25°C	±5	±3	±5	±3	LSB max	Input Range: ±5V
T_{min} to T_{max}	±6	±4	±6	±4	LSB max	Typical TC is 2ppm/°C
Bipolar Gain Error @ +25°C	±5	±4	±5	±4	LSB max	Input Range: ±5V
T_{min} to T_{max}	±7	±6	±7	±6	LSB max	Typical TC is 2ppm/°C
ANALOG INPUT						
Unipolar Input Current	3.5	3.5	3.5	3.5	mA max	Input Ranges: 0 to 5V or 0 to 10V
Bipolar Input Current	±1.75	±1.75	±1.75	±1.75	mA max	Input Range: ±5V
REFERENCE INPUT						
V_{REF} (For Specified Performance)	−5	−5	−5	−5	Volts	±1%
Input Reference Current	−3	−3	−3	−3	μA max	
POWER SUPPLY REJECTION						
V_{DD} Only, (FS Change)	±1	±1	±1	±1	LSB typ	V_{SS} = −12V, V_{DD} = +4.75V to +5.25V
V_{SS} Only, (FS Change)	±1	±1	±1	±1	LSB typ	V_{DD} = +5V, V_{SS} = −10.8V to −13.2V
LOGIC INPUTS						
$\overline{CS}$, $\overline{RD}$, CLK IN						
V_{INL}, Input Low Voltage	+0.8	+0.8	+0.8	+0.8	V max	V_{DD} = 5V ±5%
V_{INH}, Input High Voltage	+2.4	+2.4	+2.4	+2.4	V min	
C_{IN},[3] Input Capacitance	10	10	10	10	pF max	
$\overline{CS}$, $\overline{RD}$						
I_{IN}, Input Current	±10	±10	±10	±10	μA max	V_{IN} = 0 to V_{DD}
CLK IN						
I_{IN}, Input Current	±20	±20	±20	±20	μA max	V_{IN} = 0 to V_{DD}
LOGIC OUTPUTS						
DB11–DB0, $\overline{BUSY}$, CLK OUT						
V_{OL}, Output Low Voltage	+0.4	+0.4	+0.4	+0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	+4.0	+4.0	+4.0	+4.0	V min	I_{SOURCE} = 200μA
Floating-State Leakage Current						
DB11–DB0	±10	±10	±10	±10	μA max	
Floating-State Output Capacitance[3]	15	15	15	15	pF max	
CONVERSION TIME						
AD7672XX03						Applies to K and B Grades Only
Synchronous Clock	3.125	–	3.125	–	μs max	f_{CLK} = 4MHz. See Under
Asynchronous Clock	3/3.25	–	3/3.25	–	μs min/max	Control Inputs Synchronization
AD7672XX05						
Synchronous Clock	5	5	5	5	μs max	f_{CLK} = 2.5MHz
Asynchronous Clock	4.8/5.2	4.8/5.2	4.8/5.2	4.8/5.2	μs min/max	
AD7672XX10						
Synchronous Clock	10	10	10	10	μs max	f_{CLK} = 1.25MHz
Asynchronous Clock	9.6/10.4	9.6/10.4	9.6/10.4	9.6/10.4	μs min/max	
POWER REQUIREMENTS						
V_{DD}	+5	+5	+5	+5	VNOM	±5% for Specified Performance
V_{SS}	−12	−12	−12	−12	VNOM	±10% for Specified Performance
I_{DD}[4]	7	7	7	7	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN1 = AIN2 = 5V
I_{SS}[4]	−12	−12	−12	−12	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN1 = AIN2 = 5V
Power Dissipation	110	110	110	110	mW typ	
	179	179	179	179	mW max	

NOTES

[1]Temperature range as follows: K, L Versions; 0 to +70°C.
B, C Versions; −25°C to +85°C.

[2]V_{DD} = 5V, V_{SS} = −12V, 1LSB = FS/4096

[3]Sample tested to ensure compliance.

[4]Power supply current is measured when AD7672 is inactive, i.e., $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = HIGH.

Specifications subject to change without notice.

Parameter	T Version[1]	U Version[1]	Units	Test Conditions/Comments
ACCURACY[2]				
Resolution	12	12	Bits	
Integral Nonlinearity @ +25°C	±1	±1/2	LSB max	Tested Range ±5V
T_{min} to T_{max}	±1	±3/4	LSB max	
Differential Nonlinearity	±0.9	±0.9	LSB max	No Missing Codes Guaranteed
Unipolar Offset Error @ +25°C	±5	±3	LSB max	Input Range: 0 to 5V or 0 to 10V
T_{min} to T_{max}	±6	±4	LSB max	Typical TC is 2ppm/°C
Unipolar Gain Error @ +25°C	±5	±4	LSB max	Input Range: 0 to 5V or 0 to 10V
T_{min} to T_{max}	±7	±6	LSB max	Typical TC is 2ppm/°C
Bipolar Zero Error @ +25°C	±5	±3	LSB max	Input Range: ±5V
T_{min} to T_{max}	±6	±4	LSB max	Typical TC is 2ppm/°C
Bipolar Gain Error @ +25°C	±5	±4	LSB max	Input Range: ±5V
T_{min} to T_{max}	±7	±6	LSB max	Typical TC is 2ppm/°C
ANALOG INPUT				
Unipolar Input Current	3.5	3.5	mA max	Input Ranges: 0 to 5V or 0 to 10V
Bipolar Input Current	±1.75	±1.75	mA max	Input Range: ±5V
REFERENCE INPUT				
V_{REF} (For Specified Performance)	−5	−5	Volts	±1%
Input Reference Current	−3	−3	μA max	
POWER SUPPLY REJECTION				
V_{DD} Only, (FS Change)	±1	±1	LSB typ	V_{SS} = −12V, V_{DD} = +4.75V to +5.25V
V_{SS} Only, (FS Change)	±1	±1	LSB typ	V_{DD} = +5V, V_{SS} = −10.8V to −13.2V
LOGIC INPUTS				
$\overline{CS}$, $\overline{RD}$, CLK IN				
V_{INL}, Input Low Voltage	+0.8	+0.8	V max	V_{DD} = 5V ±5%
V_{INH}, Input High Voltage	+2.4	+2.4	V min	
C_{IN},[3] Input Capacitance	10	10	pF max	
$\overline{CS}$, $\overline{RD}$				
I_{IN}, Input Current	±10	±10	μA max	V_{IN} = 0 to V_{DD}
CLK IN				
I_{IN}, Input Current	±20	±20	μA max	V_{IN} = 0 to V_{DD}
LOGIC OUTPUTS				
DB11–DB0, $\overline{BUSY}$, CLK OUT				
V_{OL}, Output Low Voltage	+0.4	+0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	+4.0	+4.0	V min	I_{SOURCE} = 200μA
Floating-State Leakage Current				
DB11–DB0	±10	±10	μA max	
Floating-State Output Capacitance[3]	15	15	pF max	
CONVERSION TIME				
AD7672XX05				
Synchronous Clock	5	5	μs max	f_{CLK} = 2.5MHz. See Under
Asynchronous Clock	4.8/5.2	4.8/5.2	μs min/max	Control Inputs Synchronization
AD7672XX10				
Synchronous Clock	10	10	μs max	f_{CLK} = 1.25MHz
Asynchronous Clock	9.6/10.4	9.6/10.4	μs min/max	
POWER REQUIREMENTS				
V_{DD}	+5	+5	VNOM	±5% for Specified Performance
V_{SS}	−12	−12	VNOM	±10% for Specified Performance
I_{DD}[4]	7	7	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN1 = AIN2 = 5V
I_{SS}[4]	−12	−12	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN1 = AIN2 = 5V
Power Dissipation	110	110	mW typ	
	179	179	mW max	

NOTES
[1]Temperature range as follows: T, U Versions; −55°C to +125°C.
[2]V_{DD} = 5V, V_{SS} = −12V, 1LSB = FS/4096
[3]Sample tested to ensure compliance.
[4]Power supply current is measured when AD7672 is inactive, i.e., $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = HIGH.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = 5V, V_{SS} = −12V)

Parameter	Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (K, L, B, C Grades)	Limit at T_{min}, T_{max} (T, U Grades)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_2	190	230	270	ns max	$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay
t_3[2]	90	110	120	ns max	Data Access Time after $\overline{RD}$, C_L = 20pF
	125	150	170	ns max	Data Access Time after $\overline{RD}$, C_L = 100pF
t_4	t_3	t_3	t_3	ns min	$\overline{RD}$ Pulse Width
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6[2]	70	90	100	ns max	Data Setup Time after $\overline{BUSY}$
t_7[3]	20	20	20	ns min	Bus Relinquish Time
	75	85	90	ns max	
t_8	200	200	200	ns min	Delay Between Successive Read Operations

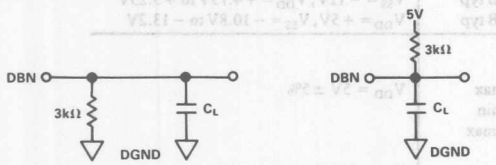
NOTES

[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.

[2]t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

[3]t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

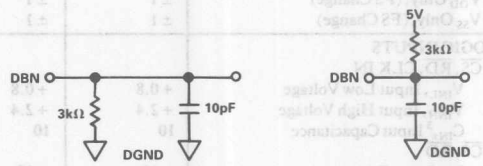
Specifications subject to change without notice.



a. High-Z to V_{OH} (t_3) and V_{OL} to V_{OH} (t_6)

b. High-Z to V_{OL} (t_3) and V_{OH} to V_{OL} (t_6)

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z

b. V_{OL} to High-Z

Figure 2. Load Circuits for Output Float Delay

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND	−0.3V to +7V
V_{SS} to DGND	+0.3V to −17V
AGND to DGND	−0.3V to V_{DD} +0.3V
AIN1, AIN2 to AGND	−15V to +15V
V_{REF} to AGND	V_{SS} −0.3V to V_{DD} +0.3V
Digital Input Voltage to DGND (CLK IN, $\overline{CS}$, $\overline{RD}$)	−0.3V to V_{DD} +0.3V
Digital Output Voltage to DGND (DB11-DB0, $\overline{BUSY}$, CLK OUT)	−0.3V to V_{DD} +0.3V
Operating Temperature Range	
K, L	0 to +70°C
B, C	−25°C to +85°C
T, U	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation (Any Package) to +75°C	1,000mW
Derates above +75°C by	10mW/°C

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



TERMINOLOGY

UNIPOLAR OFFSET ERROR
The ideal first code transition should occur when the analog input is 1/2LSB above AGND. The deviation of the actual transition from that point is termed the offset error.

BIPOLAR ZERO ERROR
The ideal midscale transition (i.e., 0111 1111 1111 to 1000 0000 0000) for the ±5V range should occur when the analog input is 1/2LSB below AGND. Bipolar zero error is the deviation of the actual transition from that point.

GAIN ERROR
The ideal difference between the first code transition and last code transition is FS − 2LSBs. The Gain error is defined as the deviation between this ideal difference and the measured difference. Ideal FS corresponds to 5V for the unipolar 0 to 5V range and 10V for both the unipolar 0 to 10V and bipolar ±5V ranges.

ORDERING GUIDE

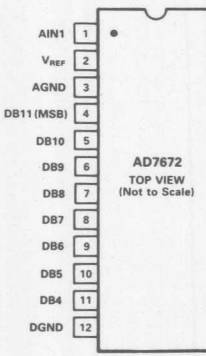
Model[1, 2]	Conversion Time	Temperature Range	Accuracy Grade	Package Option[3]
AD7672KN03	3µs	0°C to +70°C	±1LSB	N-24
AD7672BQ03	3µs	−25°C to +85°C	±1LSB	Q-24
AD7672KP03	3µs	0°C to +70°C	±1LSB	P-28A
AD7672BE03	3µs	−25°C to +85°C	±1LSB	E-28A
AD7672KN05	5µs	0°C to +70°C	±1LSB	N-24
AD7672BQ05	5µs	−25°C to +85°C	±1LSB	Q-24
AD7672TQ05	5µs	−55°C to +125°C	±1LSB	Q-24
AD7672LN05	5µs	0°C to +70°C	±1/2LSB	N-24
AD7672CQ05	5µs	−25°C to +85°C	±1/2LSB	Q-24
AD7672UQ05	5µs	−55°C to +125°C	±1/2LSB	Q-24
AD7672KP05	5µs	0°C to +70°C	±1LSB	P-28A
AD7672TE05	5µs	−55°C to +125°C	±1LSB	E-28A
AD7672LP05	5µs	0°C to +70°C	±1/2LSB	P-28A
AD7672UE05	5µs	−55°C to +125°C	±1/2LSB	E-28A
AD7672KN10	10µs	0°C to +70°C	±1LSB	N-24
AD7672BQ10	10µs	−25°C to +85°C	±1LSB	Q-24
AD7672TQ10	10µs	−55°C to +125°C	±1LSB	Q-24
AD7672LN10	10µs	0°C to +70°C	±1/2LSB	N-24
AD7672CQ10	10µs	−25°C to +85°C	±1/2LSB	Q-24
AD7672UQ10	10µs	−55°C to +125°C	±1/2LSB	Q-24
AD7672KP10	10µs	0°C to +70°C	±1LSB	P-28A
AD7672TE10	10µs	−55°C to +125°C	±1LSB	E-28A
AD7672LP10	10µs	0°C to +70°C	±1/2LSB	P-28A
AD7672UE10	10µs	−55°C to +125°C	±1/2LSB	E-28A

NOTES
[1]Analog Devices reserves the right to ship either ceramic (D-24A) or cerdip (Q-24) hermetic packages.
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact local sales office for military data sheet.
[3]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information section.

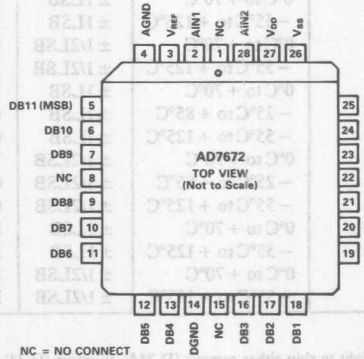
1	AIN1	Analog Input.
2	V_{REF}	Voltage Reference Input. The AD7672 is specified with $V_{REF} = -5V$.
3	AGND	Analog Ground.
4 . . . 11	DB11 . . . DB4	Three-state data outputs. They become active when $\overline{CS}$ and $\overline{RD}$ are brought low. DB11 is the most significant bit (MSB).
13 . . . 16	DB3 . . . DB0	
12	DGND	Digital Ground.
17	CLK IN	Clock Input pin. An external TTL compatible clock may be applied to this pin. Alternatively a crystal or ceramic resonator may be connected between CLK IN (Pin 17) and CLK OUT (Pin 18).
18	CLK OUT	Clock Output Pin. An inverted CLK IN signal appears at CLK OUT when an external clock is used. See CLK IN (Pin 17) description.
19	$\overline{RD}$	READ input. This active LOW signal, in conjunction with $\overline{CS}$ is used to enable the output data three-state drivers and initiate a conversion.
20	$\overline{CS}$	CHIP SELECT Input. This active LOW signal, in conjunction with $\overline{RD}$ is used to enable the output data three-state drivers and initiate a conversion.
21	$\overline{BUSY}$	$\overline{BUSY}$ output indicates converter status. $\overline{BUSY}$ is LOW during conversion.
22	V_{SS}	Negative Supply, −12V.
23	V_{DD}	Positive Supply, +5V.
24	AIN2	Analog Input.

PIN CONFIGURATIONS

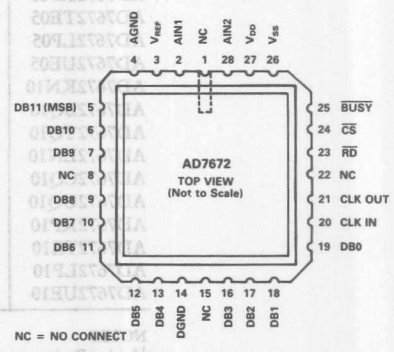
DIP



PLCC



LCCC



OPERATING FROM A NEGATIVE SUPPLY GREATER THAN −12V

The AD7672 is designed to operate with a V_{SS} input of −12V ± 10%. In applications where the negative supply is greater than −12V, then a Zener diode in series with V_{SS} can be used to reduce the supply. The Zener diode should have a dynamic impedance of not greater than 40Ω. An example is given in Figure 3. The diode has a Zener voltage of 3V, which makes it suitable for a negative supply of −15V ± 7%.

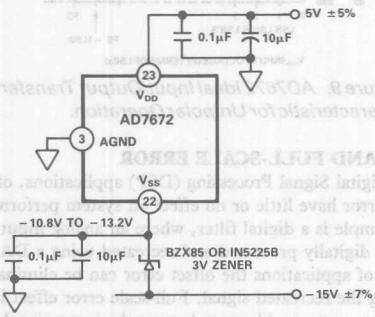


Figure 3. Operation from Nominal Power Supplies of 5V and −15V

CONVERTER DETAILS

Conversion start is controlled by the $\overline{CS}$ and $\overline{RD}$ inputs. At the start of conversion the successive approximation register (SAR) is reset and the three-state data outputs are enabled. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit DAC is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 4, the analog inputs (AIN1 & AIN2) connect to the comparator input via 5kΩ resistors. The DAC which has 2.5kΩ output impedence connects to the same comparator input. Bit decisions are made by the comparator (zero crossing detector) which checks the addition of each successive weighted bit from the DAC output against the analog inputs. The MSB decision is made 80ns (typically) after the second falling edge of CLK IN following a conversion start (see Figure 5). Similarly, the succeeding bit decisions are made approximately 80ns after a CLK IN falling edge until conversion is finished. At the end of conversion, the DAC output current balances the current from the analog inputs. The SAR contents (12-bit data word) which represent the analog input signal are loaded into a 12-bit latch.

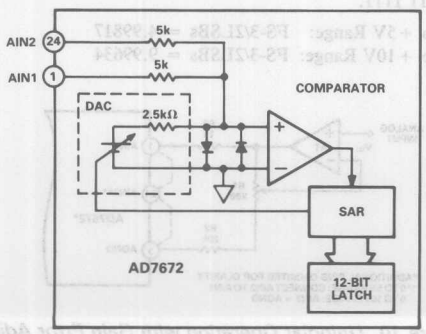


Figure 4. AD7672 AIN Input

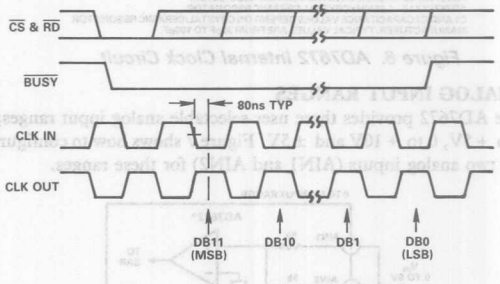


Figure 5. Operating Waveforms Using an External Clock Source for CLK IN

CONTROL INPUTS SYNCHRONIZATION

In applications where the $\overline{RD}$ control input is not synchronized with the ADC clock then conversion time can vary from 12 to 13 CLK IN periods. This is because the ADC waits for the first falling CLK IN edge after conversion start before the conversion procedure begins. Without synchronization, this delay can vary from zero to an entire clock period. If a constant conversion time is required, then the following approach may be used: when initiating a conversion, $\overline{RD}$ must go low on either the rising edge of CLK IN or the falling edge of CLK OUT. This ensures a fixed conversion time that is 12.5 times the CLK IN period.

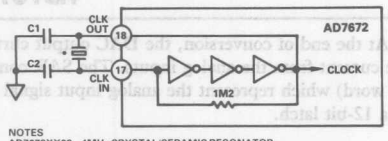
DRIVING THE ANALOG INPUTS

During conversion current from the analog inputs is modulated by the DAC output current at a rate equal to the CLK IN frequency (i.e., 4MHz when CLK IN = 4MHz). This causes voltage spikes (glitches) to appear at the analog inputs. The magnitude and settling time of these glitches depends on the open-loop output impedance and small signal bandwidth of the amplifier or sample and hold driving these inputs. These devices must have sufficient drive to ensure that the glitches have settled within one clock period. An example of a suitable op amp is the AD OP-27. The magnitude of the largest glitch when using this device to drive one of the analog inputs is typically 11mV with a 200ns settling time.

Suitable devices capable of driving the AD7672 analog inputs are the AD OP-27 and AD711 op amps and the AD585 sample-and-hold.

INTERNAL CLOCK OPERATION

Figure 6 shows the AD7672 internal clock circuit. A crystal or ceramic resonator may be connected between CLK IN (Pin 17) and CLK OUT (Pin 18) to provide a clock oscillator for the ADC timing. Alternatively the crystal/ceramic resonator may be omitted and an external clock source may be connected to CLK IN. For an external clock the mark/space ratio must be 50/50. An inverted CLK IN will appear at the CLK OUT pin as shown in the operating waveforms of Figure 5.



NOTES
AD7672XX03 – 4MHz CRYSTAL/CERAMIC RESONATOR.
AD7672XX05 – 2.5MHz CRYSTAL/CERAMIC RESONATOR.
AD7672XX10 – 1.25MHz CRYSTAL/CERAMIC RESONATOR.
C1 AND C2 CAPACITANCE VALUES DEPEND ON CRYSTAL/CERAMIC RESONATOR MANUFACTURER. TYPICAL VALUES ARE FROM 30pF TO 100pF.

Figure 6. AD7672 Internal Clock Circuit

ANALOG INPUT RANGES

The AD7672 provides three user selectable analog input ranges; 0 to +5V, 0 to +10V and ±5V. Figure 7 shows how to configure the two analog inputs (AIN1 and AIN2) for these ranges.

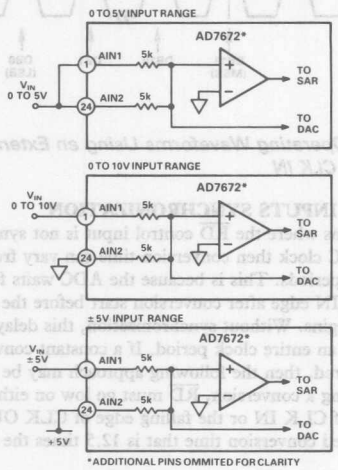
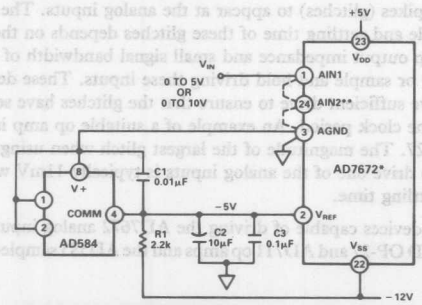


Figure 7. Analog Input Range Configurations

UNIPOLAR OPERATION

Figure 8 shows how to configure an AD584 to produce a reference voltage of −5V for unipolar operation.



*ADDITIONAL PINS OMMITED FOR CLARITY
**0-TO-5V RANGE: CONNECT AIN2 TO AIN1
0-TO-10V RANGE: AIN2 = AGND

Figure 8. Unipolar Operation Using the AD584 as a Reference

The ideal input/output characteristic is shown in Figure 9. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2LSB, 3/2LSBs . . . FS −3/2 LSBs). The output code is natural binary with 1LSB = FS/4096. FS is either +5V or +10V depending on the analog inputs configuration.

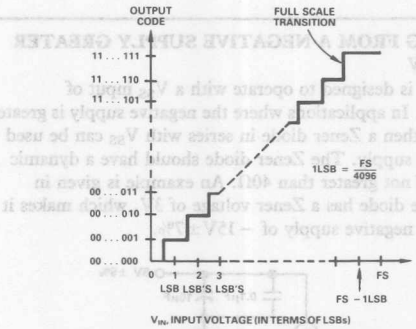


Figure 9. AD7672 Ideal Input/Output Transfer Characteristic for Unipolar Operation.

OFFSET AND FULL-SCALE ERROR

In most Digital Signal Processing (DSP) applications, offset and full-scale error have little or no effect on system performance. A typical example is a digital filter, where an analog input signal is quantized, digitally processed and recreated using a DAC. In these type of applications the offset error can be eliminated by ac coupling the recreated signal. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. An important consideration in DSP applications is Differential Nonlinearity and this is not affected by either offset or full-scale error.

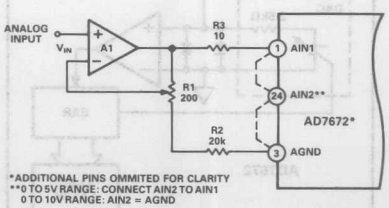
UNIPOLAR OFFSET AND FULL-SCALE ERROR ADJUSTMENT

If absolute accuracy is an application requirement then offset and full-scale error can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 10 shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset of the op amp driving the analog input (i.e., A1 in Figure 10.). For zero offset error apply a voltage equal to 1/2LSB at V_{IN} and adjust the op amp offset voltage until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

0 to +5V Range: 1/2LSB = 0.61mV
0 to +10V Range: 1/2LSB = 1.22mV

For zero full-scale error apply an analog input voltage equal to FS-3/2LSBs (last code transition) at V_{IN} and adjust R1 until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

0 to +5V Range: FS-3/2LSBs = 4.99817
0 to +10V Range: FS-3/2LSBs = 9.99634



*ADDITIONAL PINS OMMITED FOR CLARITY
**0 TO 5V RANGE: CONNECT AIN2 TO AIN1
0 TO 10V RANGE: AIN2 = AGND

Figure 10. Unipolar Operation with Gain Error Adjust

BIPOLAR OPERATION

Bipolar operation is achieved by providing a +10V span at the AIN1 input which is offset to ±5V by applying +5V at the AIN2 input. This requires two reference voltages; −5V for the V_{REF} input and +5V for the AIN2 input. Figure 11 demonstrates how to produce these voltages from an AD584 and an inverting amplifier configuration. Alternatively, a convenient solution is to use the AD588 voltage reference as in Figure 12. This device generates the required ±5V with a minimum of additional components. It also offers excellent temperature stability with voltage drifts as low as 1.5ppm/°C.

The ideal input/output transfer characteristic after offset and gain adjustment is shown in Figure 13. The LSB size is (10/4096)V = 2.44mV.

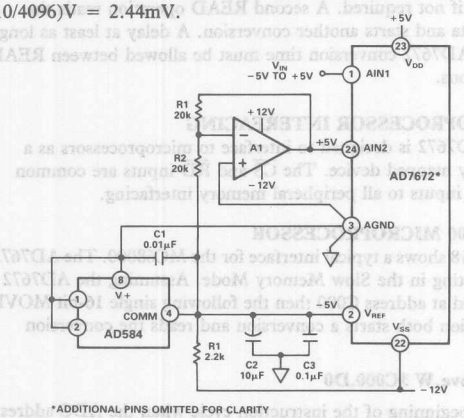


Figure 11. Bipolar Operation Using an AD584 and an AD711 Op Amp

BIPOLAR OFFSET AND GAIN ADJUSTMENT

In applications where absolute accuracy is important then offset and gain error can be adjusted to zero. Offset is adjusted by trimming the voltage at the AIN1 or the AIN2 input when the analog input is at −FS/2 +1/2LSB. This can be achieved by adjusting the offset of an external amplifier used to drive either of these analog inputs. Alternatively the AD588 voltage reference contains a balance control input which can be used to trim the offset to zero. An additional potentiometer (R2 in Figure 14) is required. The trim procedure is as follows:

Apply −4.99878V (−FS/2 + 1/2LSB) at V_{IN} and adjust R2 until the ADC ouput code flickers between 0000 0000 0000 and 0000 0000 0001.

Gain error can be adjusted at either the last positive code transition or the mid-scale transition (bipolar zero error adjust). Adjusting the positive end of the transfer function is in keeping with more conventional ADC calibration techniques where the user fixes the two end points as in the unipolar case. Bipolar zero adjustment is required in some applications (e.g., motor control) where the user must be guaranteed that the 0111 1111 1111 to 1000 0000 0000 transition occurs exactly when the analog input is 1/2LSB below AGND. The trim procedures for both cases are as follows. (See Figure 14.)

Last Code Transition Adjust

Apply a voltage of 4.99634 volts (FS/2 – 3/2LSBs) at V_{IN}. Adjust R5 until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

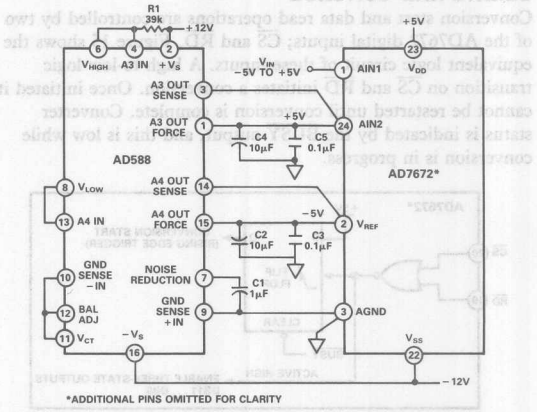


Figure 12. Bipolar Operation Using an AD588 Voltage Reference

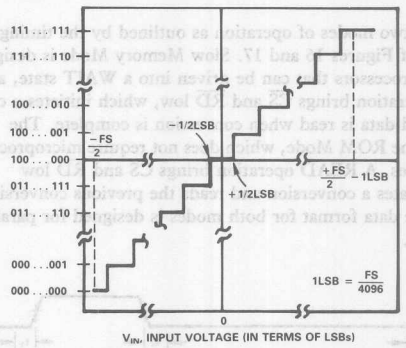


Figure 13. Ideal Input/Output Transfer Characteristic for Bipolar Operation

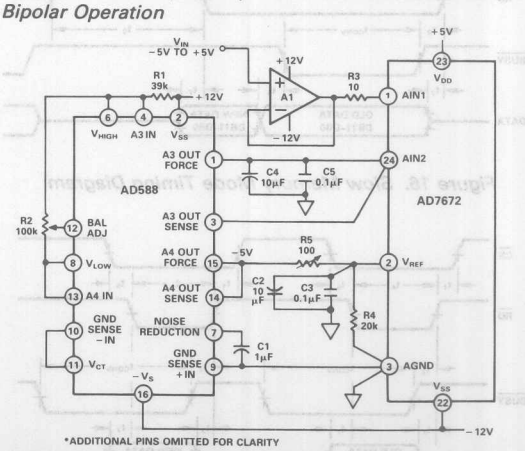


Figure 14. Bipolar Operation with Offset and Gain Error Adjust

Bipolar Zero Error Adjust

Apply a voltage of −1.22mV at V_{IN} and adjust R5 until the ADC output code flickers between 0111 1111 1111 and 1000 0000 0000.

of the AD7672 digital inputs; $\overline{CS}$ and $\overline{RD}$. Figure 15 shows the equivalent logic circuit of these inputs. A high-to-low logic transition on $\overline{CS}$ and $\overline{RD}$ initiates a conversion. Once initiated it cannot be restarted until conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output, and this is low while conversion is in progress.

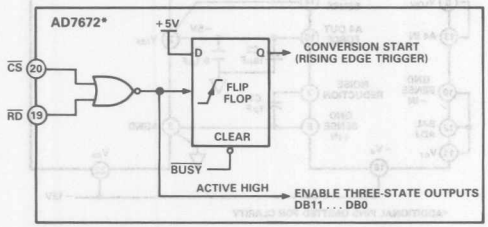


Figure 15. Internal Logic for Control Inputs $\overline{CS}$ and $\overline{RD}$

There are two modes of operation as outlined by the timing diagrams of Figures 16 and 17. Slow Memory Mode is designed for microprocessors that can be driven into a WAIT state, a READ operation brings $\overline{CS}$ and $\overline{RD}$ low, which initiates a conversion and data is read when conversion is complete. The second is the ROM Mode, which does not require microprocessor WAIT states. A READ operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and reads the previous conversion result. The data format for both modes is designed for parallel interfacing.

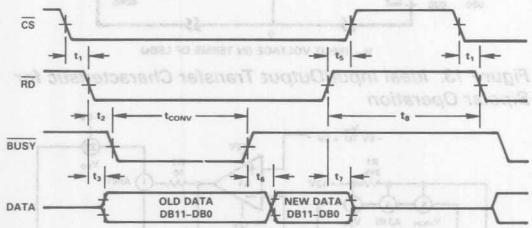


Figure 16. Slow Memory Mode Timing Diagram

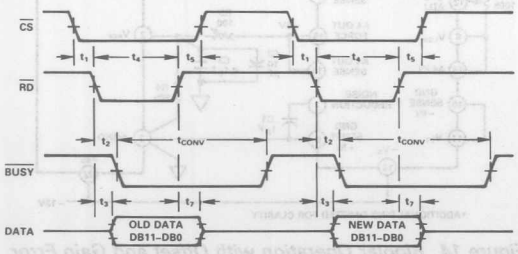


Figure 17. ROM Mode Timing Diagram

$\overline{CS}$ and $\overline{RD}$ going low triggers a conversion and the AD7672 acknowledges by taking $\overline{BUSY}$ low. Data from the previous conversion appears on the three-state data outputs. $\overline{BUSY}$ returns high at the end of conversion when the output latches have been updated and the conversion result is placed on the output data bus.

ROM MODE

The ROM Mode avoids placing a microprocessor into a wait state. A conversion is started with a READ operation and the 12-bits of data from the previous conversion are available on the data outputs while $\overline{CS}$ and $\overline{RD}$ are low. This data may be disregarded if not required. A second READ operation reads the new data and starts another conversion. A delay at least as long as the AD7672 conversion time must be allowed between READ operations.

MICROPROCESSOR INTERFACING

The AD7672 is designed to interface to microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ inputs are common control inputs to all peripheral memory interfacing.

MC68000 MICROPROCESSOR

Figure 18 shows a typical interface for the MC68000. The AD7672 is operating in the Slow Memory Mode. Assuming the AD7672 is located at address C000 then the following single 16-bit MOVE instruction both starts a conversion and reads the conversion result.

Move.W $C000,D0

At the beginning of the instruction cycle when the ADC address is selected, $\overline{BUSY}$ and $\overline{CS}$ assert $\overline{DTACK}$, so that the 68000 is forced into a WAIT state. At the end of conversion $\overline{BUSY}$ returns high and the conversion result is placed in the D0 register of the UP.

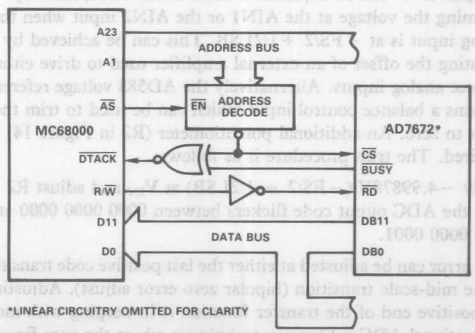


Figure 18. AD7672 –MC68000 Interface

The AD7672 is operating in the Slow Memory Mode and a two byte read is required. Not shown in the Figure is the 8-bit latch required to demultiplex the 8085A common address/data bus. The following LOAD instruction starts a conversion and reads the conversion result into the HL register pair.

For the 8085A	LHLD (B000)
For the Z-80	LDHL (B000)

This is a two byte read instruction. During the first read operation, $\overline{BUSY}$ forces the microprocessor to wait for the AD7672 conversion. At the end of conversion the low byte (DB7-DB0) is loaded into the HL register pair and the high byte (DB11-DB8) is latched into a 74HC374. No WAIT states are inserted during the second read operation when the microprocessor is reading the high data byte.

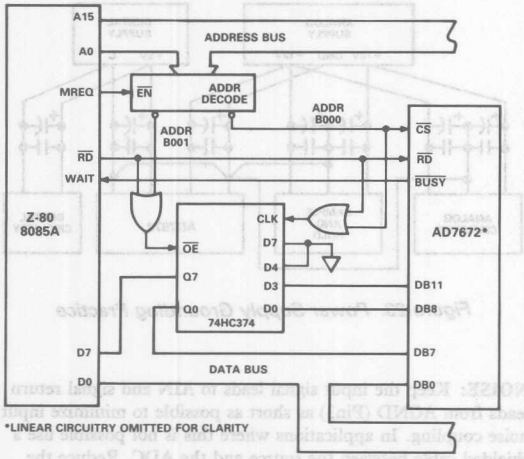


Figure 19. AD7672 – 8085A/Z80 Interface

IBM PC* COMPUTER

The −12V power supply operation of the AD7672 makes it an ideal choice for the IBM PC. A typical interface is shown in Figure 20. The AD7672 is configured in the ROM mode. Two addresses are required to read the 12-bit ADC data over the 8-bit data bus. An I/O read instruction to the ADC address (B000) starts a conversion and reads the low data byte (DB7-DB0). This data is from the previous conversion. The high byte (DB11-DB8) may be read with a similar I/O instruction to the 74HC374 latch (address B001). Alternatively the up-to-date data may be read at the end of conversion. The AD7672 $\overline{BUSY}$ may be used to interrupt the IBM PC as shown in Figure 20. The data is then read with two I/O instructions as before. Note a read instruction to the ADC should not be attempted while conversion is in progress.

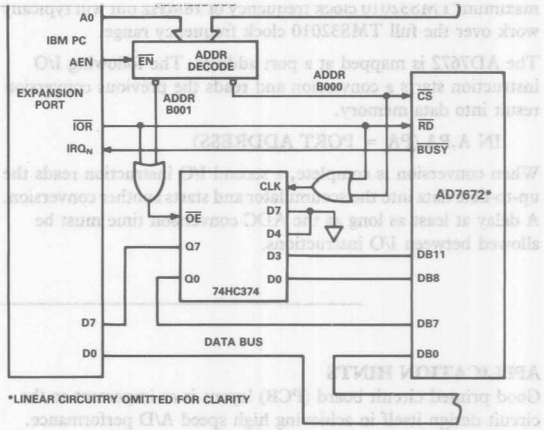


Figure 20. AD7672 – IBM PC Interface

ADSP-2100 DIGITAL SIGNAL PROCESSOR

The ADSP-2100 like other digital signal processors requires very fast data access times beyond the capabilities of the AD7672. This problem is easily overcome by inserting 74HC374 latches in the data bus as in Figure 21. Again for this interface a single instruction is sufficient to read the AD7672 conversion result.

MRO = DM (ADC ADDRESS)

This instruction initiates a conversion and reads the previous conversion result into the MRO register. $\overline{CS}$ and $\overline{RD}$ are gated so that they remain low for the duration of the conversion. Note that no WAIT states are inserted even though the AD7672 is configured for a Slow Memory mode. At the end of conversion, $\overline{BUSY}$ going high latches the new result into the 74HC374 latches. An RC delay is inserted to compensate for the data setup time after $\overline{BUSY}$ (t_6).

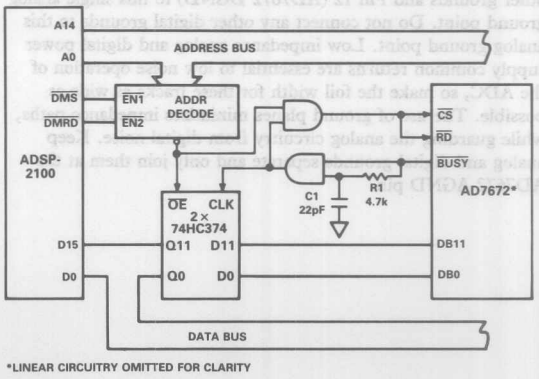


Figure 21. AD7672 – ADSP-2100 Interface

*IBM PC is a trademark of International Business Machines Corp.

TMS32010 MICROCOMPUTER

Figure 22 shows an AD7672-TMS32010 interface. The AD7672 is operating in the ROM mode. The interface is designed for a maximum TMS32010 clock frequency of 18MHz but will typically work over the full TMS32010 clock frequency range.

The AD7672 is mapped at a port address. The following I/O instruction starts a conversion and reads the previous conversion result into data memory.

IN A,PA (PA = PORT ADDRESS)

When conversion is complete, a second I/O instruction reads the up-to-date data into the accumulator and starts another conversion. A delay at least as long as the ADC conversion time must be allowed between I/O instructions.

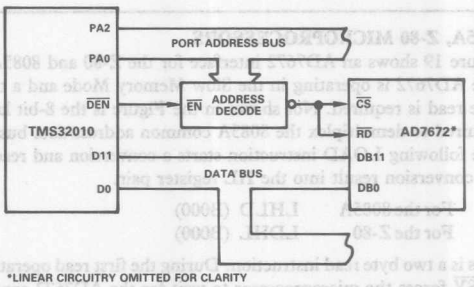


Figure 22. AD7672 – TMS32010 Interface

APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the circuit design itself in achieving high speed A/D performance. For 12-bit performance the AD7672's comparator is required to make bit decisions to an accuracy of 0.61mV. To achieve this, the designer has to be conscious of noise both in the ADC itself and the preceding analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any ADC, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground at Pin 3 (AGND) or as close as possible to the AD7672 as shown in Figure 23. Connect all other grounds and Pin 12 (AD7672 DGND) to this single analog ground point. Do not connect any other digital grounds to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths, while guarding the analog circuitry from digital noise. Keep analog and digital grounds separate and only join them at the AD7672 AGND pin.

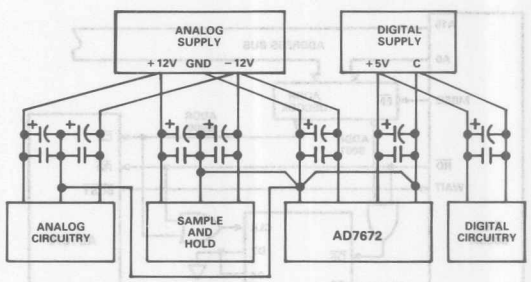


Figure 23. Power Supply Grounding Practice

NOISE: Keep the input signal leads to AIN and signal return leads from AGND (Pin3) as short as possible to minimize input noise coupling. In applications where this is not possible use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible, since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

Microprocessor applications generate noisy environments, making 12-bit performance difficult to achieve, especially when the ADC is connected to a continously active bus. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion (see Slow Memory Mode interfacing), or by using three-state buffers to isolate the AD7672 data bus.

LC²MOS 16-Bit A/D Converter

AD7701

FEATURES
- Monolithic 16-Bit ADC
- 0.0015% Linearity Error
- On-Chip Self-Calibration Circuitry
- Programmable Low Pass Filter
  - 0.1 Hz to 10 Hz Corner Frequency
- 0 to +2.5 V or ±2.5 V Analog Input Range
- 4 kSPS Output Data Rate
- Flexible Serial Interface
- Ultralow Power

APPLICATIONS
- Industrial Process Control
- Weigh Scales
- Portable Instrumentation
- Remote Data Acquisition

GENERAL DESCRIPTION

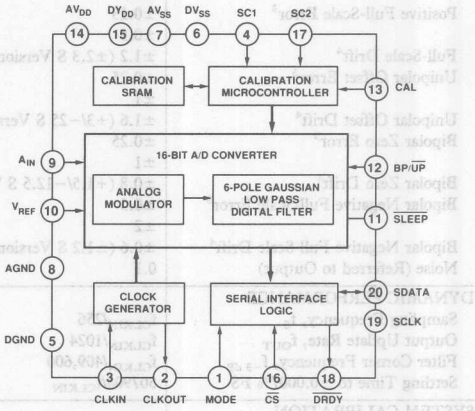
The AD7701 is a 16-bit ADC which uses a sigma delta conversion technique. The analog input is continuously sampled by an analog modulator whose mean output duty cycle is proportional to the input signal. The modulator output is processed by an on-chip digital filter with a six-pole Gaussian response, which updates the output data register with 16-bit binary words at word rates up to 4 kHz. The sampling rate, filter corner frequency and output word rate are set by a master clock input that may be supplied externally, or by a crystal-controlled on-chip clock oscillator.

The inherent linearity of the ADC is excellent, and end-point accuracy is ensured by self-calibration of zero and full-scale which may be initiated at any time. The self-calibration scheme can also be extended to null system offset and gain errors in the input channel.

The output data is accessed through a flexible serial port, which has an asynchronous mode compatible with UARTs and two synchronous modes suitable for interfacing to shift registers or the serial ports of industry-standard microcontrollers.

CMOS construction insures low power dissipation, and a power down mode reduces the idle power consumption to only 10 μW.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. The AD7701 offers 16-bit resolution coupled with outstanding 0.0015% accuracy.
2. No missing codes ensures true, usable, 16-bit dynamic range, removing the need for programmable gain and level-setting circuitry.
3. The effects of temperature drift are eliminated by on-chip self-calibration, which removes zero and gain error. External circuits can also be included in the calibration loop to remove system offsets and gain errors.
4. A flexible synchronous/asynchronous interface allows the AD7701 to interface directly to UARTs or to the serial ports of industry-standard microcontrollers.
5. Low operating power consumption and an ultralow power standby mode make the AD7701 ideal for loop-powered remote sensing applications, or battery-powered portable instruments.

AD7701—SPECIFICATIONS

(T_A = +25°C; AV_{DD} = DV_{DD} = +5 V; AV_{SS} = DV_{SS} = −5 V; V_{REF} = +2.5 V; f_{CLKIN} = 4.096 MHz; Bipolar Mode; MODE = +5 V; A_{IN} Source Resistance = 750 Ω[1] with 1 nF to AGND at A_{IN}, unless otherwise stated.)

Parameter	A, S Versions[2]	B, T Versions[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution	16	16	Bits	
Integral Nonlinearity				
T_{min} to T_{max}		±0.0007	% FSR typ	
	±0.003	±0.0015	% FSR max	
Differential Nonlinearity				
T_{min} to T_{max}	±0.125	±0.125	LSB typ	Guaranteed No Missing Codes
	±0.5	±0.5	LSB max	
Positive Full-Scale Error[3]	±0.13	±0.13	LSB typ	
	±0.5	±0.5	LSB max	
Full-Scale Drift[4]	±1.2 (±2.3 S Version)	±1.2 (±2.3 T Version)	LSB typ	
Unipolar Offset Error[3]	±0.25	±0.25	LSB typ	
	±1	±1	LSB max	
Unipolar Offset Drift[4]	±1.6 (+3/−25 S Version)	±1.6 (+3/−25 T Version)	LSB typ	
Bipolar Zero Error[3]	±0.25	±0.25	LSB typ	
	±1	±1	LSB max	
Bipolar Zero Drift[4]	±0.8 (+1.5/−12.5 S Version)	±0.8 (+1.5/−12.5 T Version)	LSB typ	
Bipolar Negative Full-Scale Error[3]	±0.5	±0.5	LSB typ	
	±2	±2	LSB max	
Bipolar Negative Full-Scale Drift[4]	±0.6 (±1.2 S Version)	±0.6 (±1.2 T Version)	LSB typ	
Noise (Referred to Output)	0.1	0.1	LSB rms typ	
DYNAMIC PERFORMANCE				
Sampling Frequency, f_S	f_{CLKIN}/256	f_{CLKIN}/256	Hz	
Output Update Rate, f_{OUT}	f_{CLKIN}/1024	f_{CLKIN}/1024	Hz	
Filter Corner Frequency, $f_{-3\ dB}$	f_{CLKIN}/409,600	f_{CLKIN}/409,600	Hz	
Settling Time to ±0.0007% FS	507904/f_{CLKIN}	507904/f_{CLKIN}	sec	For Full-Scale Input Step
SYSTEM CALIBRATION				
Positive Full-Scale Overrange	V_{REF} +0.1	V_{REF} +0.1	V max	Applies to Unipolar and Bipolar Ranges. After Calibration, If $A_{IN} > V_{REF}$, the Device Will Output All 1s If A_{IN} <0 (Unipolar) or $-V_{REF}$ (Bipolar), the Device Will Output All 0s.
Positive Full-Scale Overrange	V_{REF} +0.1	V_{REF} +0.1	V max	
Negative Full-Scale Overrange	−(V_{REF} +0.1)	−(V_{REF} +0.1)	V max	
Maximum Offset Calibration Range[5, 6]				
Unipolar Input Range	−(V_{REF} +0.1)	−(V_{REF} +0.1)	V max	
Bipolar Input Range	−0.4 V_{REF} to +0.4 V_{REF}	−0.4 V_{REF} to +0.4 V_{REF}	V max	
Input Span[7]	0.8 V_{REF}	0.8 V_{REF}	V min	
	2 V_{REF} +0.2	2 V_{REF} +0.2	V max	
ANALOG INPUT				
Unipolar Input Range	0 to +2.5	0 to +2.5	Volts	
Bipolar Input Range	±2.5	±2.5	Volts	
Input Capacitance	10	10	pF typ	
Input Bias Current[1]	1	1	nA typ	
LOGIC INPUTS				
All Inputs Except CLKIN				
V_{INL}, Input Low Voltage	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.0	2.0	V min	
CLKIN				
V_{INL}, Input Low Voltage	0.8	0.8	V max	
V_{INH}, Input High Voltage	3.5	3.5	V min	
I_{IN}, Input Current	10	10	μA max	
LOGIC OUTPUTS				
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	DV_{DD}−1	DV_{DD}−1	V min	I_{SOURCE} = 100 μA
Floating State Leakage Current	±10	±10	μA max	
Floating State Output Capacitance	9	9	pF typ	

Parameter	A, S Versions[2]	B, T Versions[2]	Units	Test Conditions/Comments
POWER REQUIREMENTS[8]				
Power Supply Voltages				
Analog Positive Supply (AV_{DD})	4.5/5.5	4.5/5.5	Vmin/Vmax	
Digital Positive Supply (DV_{DD})	4.5/AV_{DD}	4.5/AV_{DD}	Vmin/Vmax	
Analog Negative Supply (AV_{SS})	−4.5/−5.5	−4.5/−5.5	Vmin/Vmax	
Digital Negative Supply (DV_{SS})	−4.5/−5.5	−4.5/−5.5	Vmin/Vmax	
Calibration Memory Retention				
Power Supply Voltage	2.0	2.0	V min	
DC Power Supply Currents[8]				
Analog Positive Supply (AI_{DD})	3.2	3.2	mA max	Typically 2 mA
Digital Positive Supply (DI_{DD})	1.5	1.5	mA max	Typically 1 mA
Analog Negative Supply (AI_{SS})	3.2	3.2	mA max	Typically 2 mA
Digital Negative Supply (DI_{SS})	0.1	0.1	mA max	Typically 0.03 mA
Power Supply Rejection[9]				
Positive Supplies	70	70	dB typ	
Negative Supplies	75	75	dB typ	
Power Dissipation				
Normal Operation	40	40	mW max	$\overline{SLEEP}$ = Logic 1, Typically 25 mW
Standby Operation[10]	20 (40 S Version)	20 (40 T Version)	μW max	$\overline{SLEEP}$ = Logic 0, Typically 10 μW

NOTES
[1]The A_{IN} pin presents a very high impedance dynamic load which varies with clock frequency.
[2]Temperature ranges are as follows: A, B Versions; −40°C to +85°C; S, T Versions; −55°C to +125°C.
[3]Apply after calibration at the temperature of interest. Full-scale error applies for both unipolar and bipolar input ranges.
[4]Total drift over the specified temperature range since calibration at power-up at +25°C. This is guaranteed by design and/or characterization. Recalibration at any temperature will remove these errors.
[5]In unipolar mode the offset can have a negative value ($-V_{REF}$) such that the unipolar mode can mimic bipolar mode operation.
[6]The specifications for input overrange and for input span apply additional constraints on the offset calibration range.
[7]For unipolar mode, input span is the difference between full-scale and zero scale. Fir bipolar mode, input span is the difference between positive and negative full-scale points. When using less than the maximum input span, the span range may be placed anywhere within the range of $\pm(V_{REF} + 0.1)$.
[8]All digital outputs unloaded. All digital inputs at 5 V CMOS levels.
[9]Applies in 0.1 Hz to 10 Hz bandwidth. PSRR at 60 Hz will exceed 120 dB due to the digital filter.
[10]CLKIN is stopped. All digital inputs are grounded.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]
(T_A = +25°C unless otherwise noted)

DV_{DD} to AGND . . . . . −0.3 V to +6 V
DV_{DD} to AV_{DD} . . . . . −0.3 V to +0.3 V
DV_{SS} to AGND . . . . . +0.3 V to −6 V
AV_{DD} to AGND . . . . . −0.3 V to +6 V
AV_{SS} to AGND . . . . . +0.3 V to −6 V
AGND to DGND . . . . . −0.3 V to +0.3 V
Digital Input Voltage to DGND . . . −0.3 V to DV_{DD} +0.3 V
Analog Input
Voltage to AGND . . . . . AV_{SS} −0.3 V to AV_{DD} +0.3 V
Input Current to Any Pin Except Supplies[2] . . . . . ±10 mA
Operating Temperature Range
Commercial Plastic (A, B Versions) . . . . . −40°C to +85°C
Industrial Cerdip (A, B Versions) . . . . . −40°C to +85°C
Extended Cerdip (S, T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 10 mW/°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch-up.

CAUTION

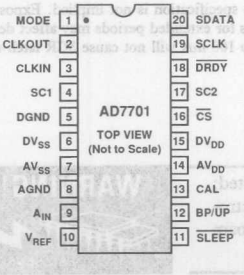
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	MODE	Selects the Serial Interface Mode. If MODE is tied to −5 V, the AD7701 will operate in the asynchronous communications (AC) mode. The SCLK pin is configured as an input, and data is transmitted in two bytes, each with one start bit and two stop bits. If MODE is tied to DGND, the synchronous external clocking (SEC) mode is selected. SCLK is configured as an input, and the output appears without formatting, the MSB coming first. If MODE is tied to +5 V, the AD7701 operates in the synchronous self-clocking (SSC) mode. SCLK is configured as an output, with a clock frequency of $f_{CLKIN}/4$ and 25% duty-cycle.
2	CLKOUT	Clock Output to generate an Internal Master Clock by connecting a crystal between CLKOUT and CLKIN. If an external clock is used, CLKOUT is not connected.
3	CLKIN	Clock Input for External Clock.
4, 17	SC1, SC2	System Calibration Pins. The state of these pins, when CAL is taken high, determines the type of calibration performed.
5	DGND	Digital Ground. Ground reference for all digital signals.
6	DV_{SS}	Digital Negative Supply, −5 V nominal.
7	AV_{SS}	Analog Negative Supply, −5 V nominal.
8	AGND	Analog Ground. Ground reference for all analog signals.
9	A_{IN}	Analog Input.
10	V_{REF}	Voltage Reference Input, +2.5 V nominal. This determines the value of positive full-scale in the unipolar mode and of both positive and negative full-scale in the bipolar mode.
11	$\overline{SLEEP}$	Sleep mode pin. When this pin is taken low, the AD7701 goes into a low-power mode with typically 10 μW power consumption.
12	BP/$\overline{UP}$	Bipolar/Unipolar Mode Pin. When this pin is low, the AD7701 is configured for a unipolar input range going from AGND to V_{REF}. When Pin 12 is high, the AD7701 is configured for a bipolar input range, $\pm V_{REF}$.
13	CAL	Calibration Mode Pin. When CAL is taken high for more than 4 cycles, the AD7701 is reset and performs a calibration cycle when CAL is brought low again. The CAL pin can also be used as a strobe to synchronize the operation of several AD7701s.
14	AV_{DD}	Analog Positive Supply, +5 V nominal.
15	DV_{DD}	Digital Positive Supply, +5 V nominal.
16	$\overline{CS}$	Chip Select Input. When $\overline{CS}$ is brought low, the AD7701 will begin to transmit serial data in a format determined by the state of the MODE pin.
18	$\overline{DRDY}$	Data Ready output. $\overline{DRDY}$ is low when valid data is available in the output register. It goes high after transmission of a word is completed. It also goes high for four clock cycles when a new data word is being loaded into the output register, to indicate that valid data is not available, irrespective of whether data transmission is complete or not.
19	SCLK	Serial Clock Input/Output. The SCLK pin in configured as an input or output, dependent on the type of serial data transmission that has been selected by the MODE pin. When configured as an output in the synchronous self-clocking mode, it has a frequency of $f_{CLKIN}/4$ and a duty cycle of 25%.
20	SDATA	Serial Data Output. The AD7701's output data is available at this pin as a 16-bit serial word. The transmission format is determined by the state of the MODE pin.

PIN CONFIGURATION



ORDERING GUIDE

Model[1]	Temperature Range	Linearity Error (%FSR)	Package Options[2]
AD7701AN	−40°C to +85°C	0.003	N-20
AD7701BN	−40°C to +85°C	0.0015	N-20
AD7701AR	−40°C to +85°C	0.003	R-20
AD7701BR	−40°C to +85°C	0.0015	R-20
AD7701AQ	−40°C to +85°C	0.003	Q-20
AD7701BQ	−40°C to +85°C	0.0015	Q-20
AD7701SQ[3]	−55°C to +125°C	0.003	Q-20
AD7701TQ[3]	−55°C to +125°C	0.0015	Q-20

NOTES
[1]To order MIL-STD-883B, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.
[3]Available to /883B processing only.

TIMING CHARACTERISTICS[1, 2]

(AV_{DD} = DV_{DD} = +5 V ± 10%; AV_{SS} = DV_{SS} = −5 V ± 10%; AGND = DGND = 0 V; f_{CLKIN} = 4.096 MHz; Input Levels: Logic 0 = 0 V, Logic 1 = DV_{DD})

Parameter	Limit at T_{min}, T_{max} (A, B Versions)	Limit at T_{min}, T_{max} (S, T Versions)	Units	Conditions/Comments
f_{CLKIN}[3, 4]	40	40	kHz min	Master Clock Frequency: Internal Gate Oscillator
	5	5	MHz max	Typically 4.096 MHz
	40	40	kHz min	Master Clock Frequency: Externally Supplied
	5	5	MHz max	
t_r[5]	50	50	ns max	Digital Output Rise Time. Typically 20 ns
t_f[5]	50	50	ns max	Digital Output Fall Time. Typically 20 ns
t_1	0	0	ns min	SC1, SC2 to CAL High Setup Time
t_2	50	50	ns min	SC1, SC2 Hold Time After CAL Goes High
t_3[6]	1000	1000	ns min	$\overline{SLEEP}$ High to CLKIN High Setup Time
SSC Mode				
t_4[7]	$3/f_{CLKIN}$	$3/f_{CLKIN}$	ns min	Data Access Time ($\overline{CS}$ Low to Data Valid)
t_5	100	100	ns max	SCLK Falling Edge to Data Valid Delay (25 ns typ)
t_6	250	250	ns min	MSB Data Setup Time. Typically 380 ns
t_7	300	300	ns max	SCLK High Pulse Width. Typically 240 ns
t_8	790	790	ns max	SCLK Low Pulse Width. Typically 730 ns
t_9[8]	$1/f_{CLKIN}$ +200	$1/f_{CLKIN}$ +200	ns max	SCLK Rising Edge to Hi-Z Delay ($1/f_{CLKIN}$ +100 ns typ)
t_{10}[8, 9]	$(4/f_{CLKIN})$ +200	$(4/f_{CLKIN})$ +200	ns max	$\overline{CS}$ High to Hi-Z Delay
SEC Mode				
f_{SCLK}	5	5	MHz	Serial Clock Input Frequency
t_{11}	50	50	ns min	SCLK Input High Pulse Width
t_{12}	180	180	ns min	SCLK Low Pulse Width
t_{13}[7, 10]	160	160	ns max	Data Access Time ($\overline{CS}$ Low to Data Valid). Typically 80 ns
t_{14}[11]	150	150	ns min	SCLK Falling Edge to Data Valid Delay. Typically 75 ns
t_{15}[8]	250	250	ns min	$\overline{CS}$ High to Hi-Z Delay
t_{16}[8]	200	200	ns min	SCLK Falling Edge to Hi-Z Delay. Typically 100 ns
AC Mode				
t_{17}	40	40	ns max	$\overline{CS}$ Setup Time. Typically 20 ns
t_{18}	180	180	ns max	Data Delay Time. Typically 90 ns
t_{19}	200	200	ns max	SCLK Falling Edge to Hi-Z Delay. Typically 100 ns

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]See Figures 1 to 5.

[3]CLKIN Duty Cycle range is 20% to 80%. CLKIN must be supplied whenever the AD7701 is not in SLEEP mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.

[4]The AD7701 is production tested with f_{CLKIN} at 4.096 MHz. It is guaranteed by characterization to operate at 200 kHz.

[5]Specified using 10% and 90% points on waveform of interest.

[6]In order to synchronize several AD7701s together using the $\overline{SLEEP}$ pin, this specification is met.

[7]t_4 and t_{13} are measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[8]t_8, t_{10}, t_{15} and t_{16} are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time quoted in the Timing Characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitance.

[9]If $\overline{CS}$ is returned high before all 16 bits are output, the SDATA and SCLK outputs will complete the current data bit and then go to high impedance.

[10]If $\overline{CS}$ is activated asynchronously to $\overline{DRDY}$, $\overline{CS}$ will not be recognized if it occurs when $\overline{DRDY}$ is high for four clock cycles. The propagation delay time may be as great as 4 CLKIN cycles plus 160 ns. To guarantee proper clocking of SDATA when using asynchronous $\overline{CS}$, the SCLK input should not be taken high sooner then 4 CLKIN cycles plus 160 ns after $\overline{CS}$ goes low.

[11]SDATA is clocked out on the falling edge of the SCLK input.

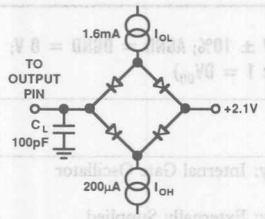
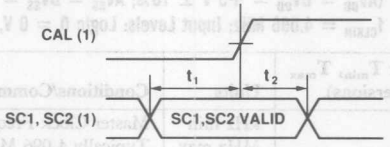
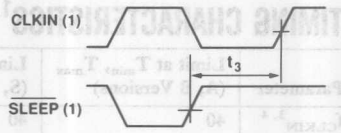


Figure 1. Load Circuit for Access Time and Bus Relinquish Time



2a. Calibration Control Timing



2b. $\overline{SLEEP}$ Mode Timing

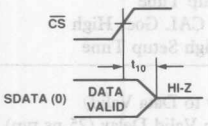


Figure 3. SSC Mode Data Hold Time

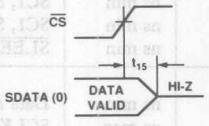


Figure 4a. SEC Mode Data Hold Time

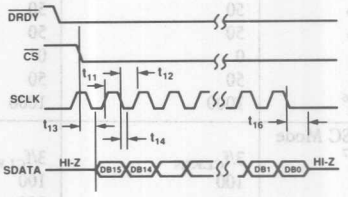


Figure 4b. SEC Mode Timing Diagram

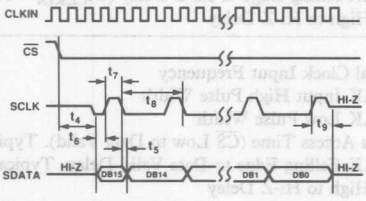


Figure 5. SSC Mode Timing Diagram

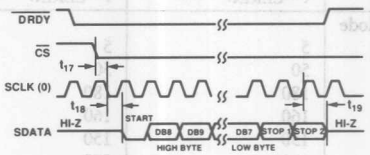


Figure 6. AC Mode Timing Diagram

TERMINOLOGY

LINEARITY ERROR
This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are Zero-Scale (not to be confused with Bipolar Zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and Full-Scale, a point 1.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

DIFFERENTIAL LINEARITY ERROR
This is the difference between any code's actual width and the ideal (1 LSB) width. Differential Linearity Error is expressed in LSBs. A differential linearity specification of ±1 LSB or less guarantees monotonicity.

POSITIVE FULL-SCALE ERROR
Positive Full-Scale Error is the deviation of the last code transition (111 . . . 110 to 111 . . . 111) from the ideal (V_{REF} −3/2 LSBs). It applies to both positive and negative analog input ranges and it is expressed in microvolts.

UNIPOLAR OFFSET ERROR
Unipolar Offset Error is the deviation of the first code transition from the ideal (AGND + 0.5 LSB) when operating in the unipolar mode. It is expressed in microvolts.

BIPOLAR ZERO ERROR
This is the deviation of the mid-scale transition (0111 . . . 111 to 1000 . . . 000) from the ideal (AGND − 0.5 LSB) when operating in the bipolar mode. It is expressed in microvolts.

BIPOLAR NEGATIVE FULL-SCALE ERROR
This is the deviation of the first code transition from the ideal ($-V_{REF}$ + 0.5 LSB), when operating in the bipolar mode. It is expressed in microvolts.

POSITIVE FULL-SCALE OVERRANGE
Positive Full-Scale Overrange is the amount of overhead available to handle input voltages greater than $+V_{REF}$ (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or overflowing the digital filter. It is expressed in millivolts.

NEGATIVE FULL-SCALE OVERRANGE
This is the amount of overhead available to handle voltages below $-V_{REF}$ without overloading the analog modulator or overflowing the digital filter. Note that the analog input will accept negative voltage peaks even in the unipolar mode. The overhead is expressed in millivolts.

In the system calibration modes (SC2 low) the AD7701 calibrates its offset with respect to the A_{IN} pin. The Offset Calibration Range specification defines the range of voltages, expressed as a percentage of V_{REF} that the AD7701 can accept and still calibrate offset accurately.

FULL-SCALE CALIBRATION RANGE

This is the range of voltages that the AD7701 can accept in the system calibration mode and still calibrate full-scale correctly.

INPUT SPAN

In system calibration schemes, two voltages applied in sequence to the AD7701's analog input define the analog input range. The input span specification defines the minimum and maximum input voltages from zero to full-scale that the AD7701 can accept and still calibrate gain accurately. The input span is expressed as a percentage of V_{REF}.

GENERAL DESCRIPTION

The AD7701 is a 16-bit A/D converter with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals such as those representing chemical, physical or biological processes. It contains a charge-balancing (sigma-delta) ADC, calibration microcontroller with on-chip static RAM, a clock oscillator and a serial communications port.

The analog input signal to the AD7701 is continuously sampled at a rate determined by the frequency of the master clock, CLKIN. A charge-balancing A/D converter (Sigma Delta Modulator) converts the sampled signal into a digital pulse train whose duty cycle contains the digital information. A six-pole Gaussian digital low-pass filter processes the output of the modulator and updates the 16-bit output register at a 4 kHz rate. The output data can be read from the serial port randomly or periodically at any rate up to 4 kHz.

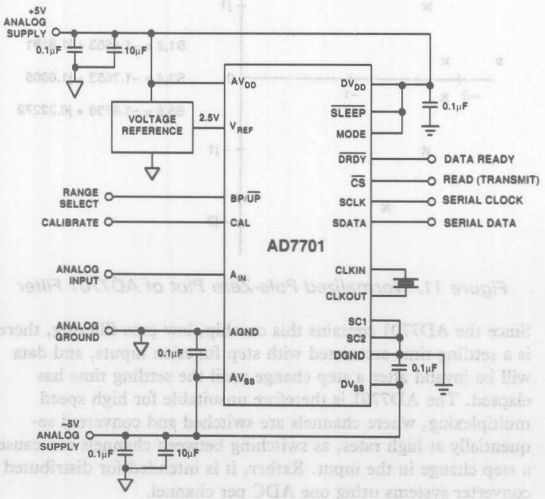


Figure 7. Typical System Connection Diagram

bration microcontroller and SRAM to store calibration parameters. A calibration cycle may be initiated at any time using the CAL control input.

Other system components may also be included in the calibration loop to remove offset and gain errors in the input channel.

For battery operation, the AD7701 also offers a standby mode that reduces idle power consumption to typically 10 μW.

THEORY OF OPERATION

The general block diagram of a sigma delta ADC is shown in Figure 8. It contains the following elements.

1. A sample-hold amplifier.
2. A differential amplifier or subtractor.
3. An analog low pass filter.
4. A 1-bit A/D converter (comparator).
5. A 1-bit DAC.
6. A digital low pass filter.

In operation, the analog signal sample is fed to the subtractor, along with the output of the 1-bit DAC. The filtered difference signal is fed to the comparator, whose output samples the difference signal at a frequency many times that of the analog signal sampling frequency (oversampling).

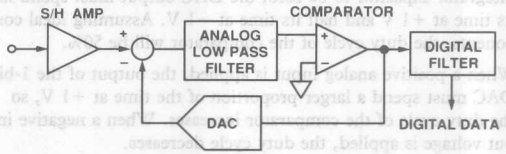


Figure 8. General Sigma Delta ADC

Oversampling is fundamental to the operation of sigma delta ADCs. Using the quantization noise formula for an ADC:

$$SNR = (6.02 \times number\ of\ bits + 1.76)\ dB$$

a 1-bit ADC or comparator yields an SNR of 7.78 dB.

The AD7701 samples the input signal at 16 kHz, which spreads the quantization noise from 0 to 8 kHz. Since the specified analog input bandwidth of the AD7701 is only 0 to 10 Hz, the noise energy in this bandwidth would be only 1/800 of the total quantization noise, even if the noise energy was spread evenly throughout the spectrum. It is reduced still further by analog filtering in the modulator loop, which shapes the quantization noise spectrum to move most of the noise energy to frequencies above 10 Hz. The SNR performance in the 0 to 10 Hz range is conditioned to the 16-bit level in this fashion.

The output of the comparator provides the digital input for the 1-bit DAC, so that the system functions as a negative feedback loop that tries to minimize the difference signal. The digital data that represents the analog input voltage is contained in the duty cycle of the pulse train appearing at the output of the comparator. It can be retrieved as a parallel binary data word using a digital filter.

lowpass filter or integrator. It also illustrates the derivation of the alternative name for these devices: Charge-Balancing ADCs.

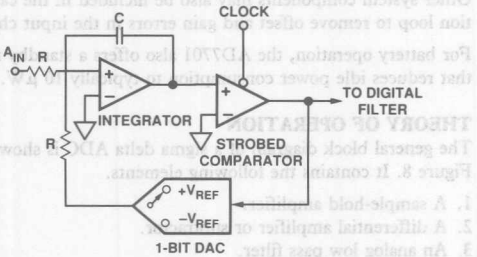


Figure 9. Basic Charge-Balancing ADC

The term charge-balancing comes from the fact that this system is a negative feedback loop that tries to keep the net charge on the integrator capacitor at zero, by balancing charge injected by the input voltage with charge injected by the 1-bit DAC. When the analog input is zero, the only contribution to the integrator output comes from the 1-bit DAC. For the net charge on the integrator capacitor to be zero, the DAC output must spend half its time at +1 V and half its time at −1 V. Assuming ideal components, the duty cycle of the comparator will be 50%.

When a positive analog input is applied, the output of the 1-bit DAC must spend a larger proportion of the time at +1 V, so the duty cycle of the comparator increases. When a negative input voltage is applied, the duty cycle decreases.

The AD7701 uses a second-order sigma delta modulator and a sophisticated digital filter that provides a rolling average of the sampled output. After power-up or if there is a step change in the input voltage, there is a settling time that must elapse before valid data is obtained.

DIGITAL FILTERING

The AD7701's digital filter behaves like a similar analog filter, with a few minor differences.

First, since digital filtering occurs after the A to D conversion process, it can remove noise injected during the conversion process. Analog filtering cannot do this.

On the other hand, analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. Digital filtering cannot do this and noise peaks riding on signals near full scale have the potential to saturate the analog modulator and digital filter, even though the average value of the signal is within limits. To alleviate this problem, the AD7701 has overrange headroom built into the sigma delta modulator and digital filter which allows overrange excursions of 100 mV. If noise signals are larger than this, consideration should be given to analog input filtering, or to reducing the gain in the input channel so that a full-scale input (2.5 V) gives only a half-scale input to the AD7701 (1.25 V). This will provide an overrange capability greater than 100% at the expense of reducing the dynamic range by 1 bit (50%).

FILTER CHARACTERISTICS

The cutoff frequency of the digital filter is $f_{CLK}/409600$. At the Gaussian response that provides 55 dB of 60 Hz rejection for a 10 Hz cutoff frequency. If the clock frequency is halved to give a 5 Hz cutoff, 60 Hz rejection is better than 90 dB. A normalized s-domain pole-zero plot of the filter is shown in Figure 11.

The response of the filter is defined by:

$$H(x)=[1 + 0.693x^2 + 0.240x^4 + 0.0555x^6 + 0.00962x^8 + 0.00133x^{10} + 0.000154x^{12}]^{-0.5}$$

where:

$x = f/f_{3\,dB}$, $f_{3\,dB} = f_{CLKIN}/409600$,

and

f is the frequency of interest.

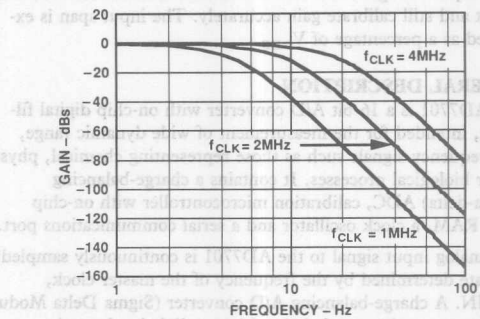


Figure 10. Frequency Response of AD7701 Filter

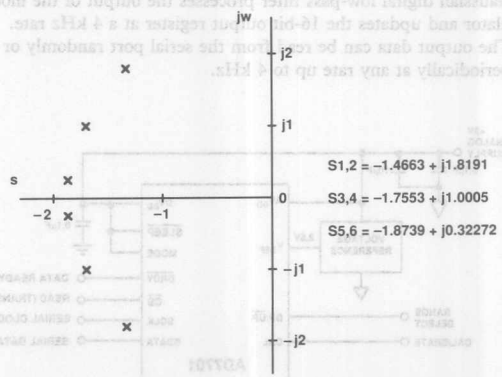


Figure 11. Normalized Pole-Zero Plot of AD7701 Filter

Since the AD7701 contains this on-chip, low pass filtering, there is a settling time associated with step function inputs, and data will be invalid after a step change until the settling time has elapsed. The AD7701 is therefore unsuitable for high speed multiplexing, where channels are switched and converted sequentially at high rates, as switching between channels can cause a step change in the input. Rather, it is intended for distributed converter systems using one ADC per channel.

However, slow multiplexing of the AD7701 is possible, provided that the settling time is allowed to elapse before data for the new channel is accessed.

The output settling of the AD7701 in response to a step input change is shown in Figure 12. The Gaussian response has fast settling with no overshoot, and the worst-case settling time to ±0.0007% (±0.5 LSB) is 125 ms with a 4.096 MHz master clock frequency.

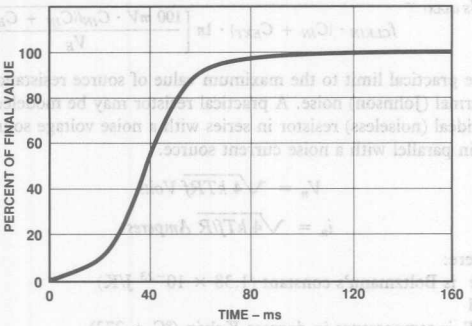


Figure 12. AD7701 Step Response

USING THE AD7701

SYSTEM DESIGN CONSIDERATIONS

The AD7701 operates differently from successive approximation ADCs or other integrating ADCs. Since it samples the signal continuously, like a tracking ADC, there is no need for a start convert command. The 16-bit output register is updated at a 4 kHz rate, and the output can be read at any time, either synchronously or asynchronously.

CLOCKING

The AD7701 requires a master clock input, which may be an external TTL/CMOS compatible clock signal applied to the CLKIN pin (CLKOUT not used). Alternatively, a crystal of the correct frequency can be connected between CLKIN and CLKOUT, when the clock circuit will function as a crystal-controlled oscillator.

The input sampling frequency, output data rate, filter characteristics and calibration time are all directly related to the master clock frequency f_{CLKIN} by the ratios given in the specification table. Therefore, the first step in system design with the AD7701 is to select a master clock frequency suitable for the bandwidth and output data rate required by the application.

ANALOG INPUT RANGES

The AD7701 performs conversion relative to an externally supplied reference voltage, which allows easy interfacing to ratiometric systems. In addition, either unipolar or bipolar input voltage range may be selected using the BP/$\overline{UP}$ input. With BP/$\overline{UP}$ tied low, the input range is unipolar and the span is 0 to $+V_{REF}$. With BP/$\overline{UP}$ tied high, the input range is bipolar and the span is $\pm V_{REF}$. In the bipolar mode both positive and negative full-scale are directly determined by V_{REF}. This offers superior tracking of positive and negative full scale and better midscale (bipolar zero) stability than bipolar schemes that simply scale and offset the input range.

The digital output coding for the unipolar range is Unipolar Binary; for the bipolar range it is Offset Binary. Bit weights for the unipolar and bipolar modes are shown in Table I. The input voltages and output codes for unipolar and bipolar ranges, using the recommended +2.5 V reference, are shown in Table II.

	Unipolar Mode			Bipolar Mode		
μV	LSBs	% FS	ppm FS	LSBs	% FS	ppm FS
10	0.26	0.0004	4	0.13	0.0002	2
19	0.5	0.0008	8	0.26	0.0004	4
38	1.00	0.0015	15	0.5	0.0008	8
76	2.00	0.0031	31	1.00	0.0015	15
153	4.00	0.0061	61	2.00	0.0031	31

Table I. Bit Weight Table (2.5 V Reference Voltage)

Unipolar Mode Input Relative to FS and AGND	Input in Volts	Bipolar Mode Input Relative to FS and AGND	Input in Volts	Output Data
$+V_{REF}$ −1.5 LSB	+2.499943	$+V_{REF}$ −1.5 LSB	+2.499886	1111 1111 1111 1111
$+V_{REF}$ −2.5 LSB	+2.499905	$+V_{REF}$ −2.5 LSB	+2.499810	1111 1111 1111 1110
$+V_{REF}$ −3.5 LSB	+2.499867	$+V_{REF}$ −3.5 LSB	+2.499733	1111 1111 1111 1101
				1111 1111 1111 1100
$+V_{REF}/2$ +0.5 LSB	+1.250019	AGND +0.5 LSB	+0.000038	1000 0000 0000 0001
$+V_{REF}/2$ −0.5 LSB	+1.249981	AGND −0.5 LSB	−0.000038	1000 0000 0000 0000
$+V_{REF}/2$ −1.5 LSB	+1.249943	AGND −1.5 LSB	−0.000114	0111 1111 1111 1111
				0111 1111 1111 1110
AGND +2.5 LSB	+0.000095	$-V_{REF}$ +2.5 LSB	−2.499810	0000 0000 0000 0011
AGND +1.5 LSB	+0.000057	$-V_{REF}$ +1.5 LSB	−2.499886	0000 0000 0000 0010
AGND +0.5 LSB	+0.000019	$-V_{REF}$ +0.5 LSB	−2.499962	0000 0000 0000 0001
				0000 0000 0000 0000

NOTES
[1]V_{REF} = +2.5 V
[2]AGND = 0 V
[3]Unipolar Mode, 1 LSB = 2.5 V/655536 = 0.000038 V
[4]Bipolar Mode, 1 LSB = 5 V/65536 = 0.000076 V
[5]Inputs are voltages at code transitions.

Table II. Output Coding

INPUT SIGNAL CONDITIONING

Reference voltages from +1 V to +3 V may be used with the AD7701, with little degradation in performance. Input ranges that cannot be accommodated by this range of reference voltages may be achieved by input signal conditioning. This may take the form of gain to accommodate a smaller signal range, or passive attenuation to reduce a larger input voltage range.

Source Resistance

If passive attenuators are used in front of the AD7701, care must be taken to ensure that the source impedance is sufficiently low. The AD7701 has an analog input with over 1 GΩ dc input resistance. In parallel with this there as a small dynamic load which varies with the clock frequency (see Figure 13). Each time the analog input is sampled, a 10 pF capacitor draws a charge packet of maximum 1 pC (10 pF × 100 mV)

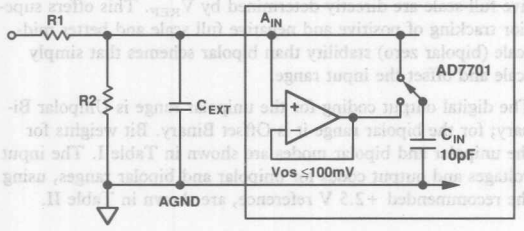


Figure 13. Equivalent Input Circuit and Input Attenuator

from the analog source with a frequency $f_{CLKIN}/256$. For a 4.096 MHz CLKIN, this yields an average current draw of 16 nA. After each sample the AD7701 allows 62 clock periods for the input voltage to settle. The equation which defines settling time is:

$$V_O = V_{IN}\,[1 - e^{-t/RC}]$$

where:

V_O is the final settled value,
V_{IN} is the value of the input signal,
R is the value of the input source resistance,
C is the 10 pF sample capacitor,
t is equal to $62/f_{CLKIN}$.

From this, the following equation can be developed which gives the maximum allowable source resistance, $R_{S(MAX)}$, for an error of V_E:

$$R_{S\,(MAX)} = \frac{62}{f_{CLKIN} \cdot (10\,pF) \cdot 1n\,(100\,mV/V_E)}$$

Provided the source resistance is less than this value, the analog input will settle within the desired error band in the requisite 62 clock periods. Insufficient settling leads to offset errors. These can be calibrated in system calibration schemes.

If a limit of 10 μV (0.25 LSB at 16 bits) is set for the maximum offset voltage, then the maximum allowable source resistance is 160 kΩ from the above equation, assuming that there is no external stray capacitance.

An RC filter may be added in front of the AD7701 to reduce high frequency noise. With an external capacitor added from A_{IN} to AGND, the following equation will specify the maximum allowable source resistance:

$$R_{S\,(MAX)} = \frac{62}{f_{CLKIN} \cdot (C_{IN} + C_{EXT}) \cdot 1n\left[\frac{100\,mV \cdot C_{IN}/(C_{IN} + C_{EXT})}{V_E}\right]}$$

The practical limit to the maximum value of source resistance is thermal (Johnson) noise. A practical resistor may be modeled as an ideal (noiseless) resistor in series with a noise voltage source or in parallel with a noise current source.

$$V_n = \sqrt{4\,kTRf}\ Volts$$

$$i_n = \sqrt{4\,kTf/R}\ Amperes$$

where:

k is Boltzmann's constant (1.38×10^{-23} J/K)
and
T is temperature in degrees Kelvin (°C + 273).

Active signal conditioning circuits such as op amps generally do not suffer from problems of high source impedance. Their open-loop output resistance is normally only tens of ohms and, in any case, most modern general purpose op amps have sufficiently fast closed-loop settling time for this not to be a problem. Offset voltage in op amps can be eliminated in a system calibration routine. With the wide dynamic range and small LSB size of the AD7701, noise can also be a problem, but the digital filter will reject most broadband noise above its cutoff frequency. However, in certain applications there may be a need for analog input filtering.

Antialias Considerations

The digital filter of the AD7701 does not provide any rejection at integer multiples of the sampling frequency ($nf_{CLKIN}/256$, where n = 1, 2, 3 . . .) .

With a 4.096 MHz master clock there are narrow (±10 Hz) bands at 16 kHz, 32 kHz, 48 kHz, etc., where noise passes unattenuated to the output.

However, due to the AD7701's high oversampling ratio of 800 (16 kHz to 20 Hz) these bands occupy only a small fraction of the spectrum, and most broadband noise is filtered.

The reduction in broadband noise is given by:

$$e_{OUT} = e_{IN}\sqrt{2f_C/f_S} = 0.035\,e_{IN}$$

where:

e_{IN} and e_{OUT} are rms noise terms referred to the input
f_C is the filter −3 dB corner frequency ($f_{CLKIN}/409600$)
and
f_S is the sampling frequency ($f_{CLKIN}/256$).

Since the ratio of f_S to f_{CLKIN} is fixed, the digital filter reduces broadband white noise by 96.5% independent of the master clock frequency.

VOLTAGE REFERENCE CONNECTIONS

The voltage applied to the V_{REF} pin defines the analog input range. The specified reference voltage is 2.5 V, but the AD7701 will operate with reference voltages from 1 V to 3 V with little degradation in performance.

The reference input presents exactly the same dynamic load as the analog input, but in the case of the reference input, source resistance and long settling time introduce gain errors rather than offset errors. Fortunately, most precision references have sufficiently low output impedance and wide enough bandwidth to settle to 10 μV within 62 clock cycles.

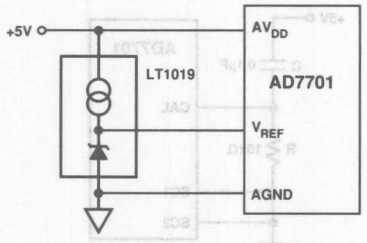


Figure 14. Typical External Reference Connections

The digital filter of the AD7701 removes noise from the reference input, just as it does with noise at the analog input, and the same limitations apply regarding lack of noise rejection at integer multiples of the sampling frequency. If reference noise is a problem, some voltage references offer noise reduction schemes using an external capacitor. Alternatively, a simple RC filter may be used, as shown in Figure 15.

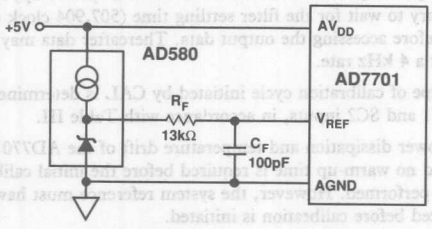


Figure 15. Filtered Reference Input

The same considerations apply to this filter as to a filter at the analog input. In this case:

$$[R_F\,(C_F + 10\,pF)] = \frac{62}{f_{CLKIN} \cdot In\left[\frac{100\,mV \cdot C_{IN}\,(C_{IN} + C_F)}{V_{FSE}}\right]}$$

where:

f_{CLKIN} is the master clock frequency

and

V_{FSE} is the maximum desired error in volts.

GROUNDING AND SUPPLY DECOUPLING

AGND is the ground reference voltage for the AD7701, and is completely independent of DGND. Any noise riding on the AGND input with respect to the system analog ground will cause conversion errors. AGND should therefore be used as the system ground and also as the ground for the analog input and the reference voltage.

The analog and digital power supplies to the AD7701 are independent and separately pinned out, to minimize coupling between analog and digital sections of the device. The digital filter will provide rejections of broadband noise on the power supplies, except at integer multiples of the sampling frequency. Therefore, the two analog supplies should be decoupled to AGND using 100 nF ceramic capacitors to provide power supply noise rejections at these frequencies. The two digital supplies should similarly be decoupled to DGND.

ACCURACY AND AUTOCALIBRATION

Sigma delta ADCs, like VFCs and other integrating ADCs, do not contain any source of nonmonotonicity and inherently offer no-missing-codes performance. The AD7701 achieves excellent linearity (±0.0007%) by the use of high quality, on-chip silicon dioxide capacitors, which have a very low capacitance/voltage coefficient.

The AD7701 offers two self-calibration modes using the on-chip calibration microcontroller and SRAM. Table III is a truth table for the calibration control inputs SC1 and SC2.

In the self-calibration mode, zero-scale is calibrated against the AGND pin and full scale is calibrated against the V_{REF} pin, to remove internal errors.

Note that in the bipolar mode the AD7701 calibrates positive full scale and midscale (bipolar zero).

In the system-calibration mode, the AD7701 calibrates its zero and full scale to voltages present on the analog input pin in two sequential steps. This allows system offsets and/or gain errors to be nulled out.

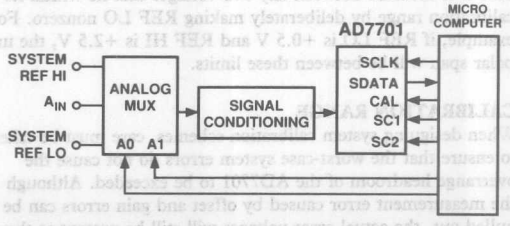


Figure 16. Typical Connections for System Calibration

A typical system calibration scheme is shown in Figure 16. In normal operation the analog signal is fed to the AD7701 via an analog multiplexer. When the system is to be calibrated, A_{IN} is first switched to the system REF LO via the multiplexer and CAL is strobed high, with SC1 and SC2 both high. A_{IN} is then switched to the system REF HI and CAL is strobed, with SC1 low and SC2 high. In this way, the effect of all error sources

CAL	SC1	SC2	CAL TYPE	ZERO REFERENCE	FS REFERENCE	SEQUENCE	CALIBRATION TIME
⎍	0	0	Self-Cal	AGND	V_{REF}	One Step	3,145,655 Clock Cycles
⎍	1	1	System Offset	A_{IN}	–	1st Step	1,052,599 Clock Cycles
⎍	0	1	System Gain	–	A_{IN}	2nd Step	1,068,813 Clock Cycles
⎍	1	0	System Offset	A_{IN}	V_{REF}	One Step	2,117,389 Clock Cycles

NOTE
$\overline{DRDY}$ remains high throughout the calibration sequence. In the Self-Cal mode, $\overline{DRDY}$ falls once the AD7701 has settled to the analog input. In all other modes $\overline{DRDY}$ falls as the device begins to settle.

Table III. Calibration Truth Table

between the multiplexer and the AD7701 is removed. Op amps and other signal conditioning circuits may be used in front of the AD7701, without worrying about their absolute gain or offset errors. Note that the absolute value of the reference supplied to the AD7701 is no longer important, provided it has adequate short-term stability between calibration cycles, as full scale is calibrated to the system reference.

If system offset errors are important but system gain errors are not, then a one step system calibration may be performed with SC1 high and SC2 low. In this case, offset is calibrated against A_{IN}, which should be connected to system REF LO during calibration, but full scale is calibrated against the AD7701's V_{REF} input.

System calibration schemes will yield better accuracy than self-calibration, even if there are no system errors. Using self-calibration, errors arise due to the mismatch in source impedances between the references during calibration (AGND and V_{REF}) and the analog input during normal operation. In system calibration, the source impedances inherently remain identical, such that the theoretical limit to system accuracy is calibration resolution. The practical limit is the noise floor of the AD7701.

Note that in system calibration, "REF LO" does not necessarily mean the system ground or zero volts. The AD7701 can be calibrated to measure between any two voltages that lie within its calibration range by deliberately making REF LO nonzero. For example, if REF LO is +0.5 V and REF HI is +2.5 V, the unipolar span will be between these limits.

CALIBRATION RANGE

When designing system calibration schemes, care must be taken to ensure that the worst-case system errors do not cause the overrange headroom of the AD7701 to be exceeded. Although the measurement error caused by offset and gain errors can be nulled out, the actual error voltages will still be present at the analog input and can cause overloading of the analog modulator or overflow of the digital filter. With a 2.5 V reference, the maximum input voltage is ($+V_{REF}$ + 100 mV), and the minimum input voltage is ($-V_{REF}$ − 100 mV).

POWER UP AND CALIBRATION

A calibration cycle must be carried out after power up to initialize the device to a consistent starting condition and correct calibration. The CAL pin must be held high for at least four clock cycles, after which calibration is initiated on the falling edge of CAL and takes a maximum of 3,145,655 clock cycles (approximately 768 ms , with a 4.096 MHz clock). See Table III.

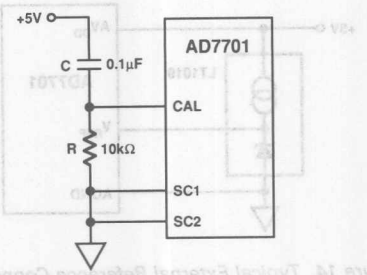


Figure 17. Power-On Reset Circuit

Figure 17 shows a simple RC circuit which will briefly pull the CAL input high as power applied. For this circuit to work the power supply must come up cleanly without oscillation, otherwise the internal circuits of the AD7701 may not all recognize the same reset transition. This can be overcome by using a Schmitt-trigger inverter between the RC combination and the CAL input to provide a clean transition. After power up, it is necessary to wait for the filter settling time (507,904 clock cycles) before accessing the output data. Thereafter data may be read at a 4 kHz rate.

The type of calibration cycle initiated by CAL is determined by the SC1 and SC2 inputs, in accordance with Table III.

The power dissipation and temperature drift of the AD7701 are low and no warm-up time is required before the initial calibration is performed. However, the system reference must have stabilized before calibration is initiated.

POWER SUPPLY SEQUENCING

The positive digital supply (DV_{DD}) must never exceed the positive analog supply (AV_{DD}) by more than 0.3 V. Power supply sequencing is therefore important. If separate analog and digital supplies are used, care must be taken to ensure that the analog supply is powered up first.

It is also important that power is applied to the AD7701 before signals at V_{REF}, A_{IN} or the logic input pins in order to avoid any possibility of latch-up. If separate supplies are used for the AD7701 and the system digital circuitry, then the AD7701 should be powered up first.

A typical scheme for powering the AD7701 from a single set of ±5 V rails is shown in the system connection diagram, Figure 7. In this circuit AV_{DD} and DV_{DD} are brought along separate tracks from the same +5 V supply. Thus, there is no possibility of the digital supply coming up before the analog supply.

GROUNDING

The AD7701 uses the analog ground connection, AGND, as the measurement reference node. It should be used as the reference node for both the analog input signal and the reference voltage at the V_{REF} pin.

The analog and digital power supplies to the AD7701 die are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled separately to their respective grounds as shown in Figure 7. The on-chip digital filtering of the AD7701 further enhances power supply rejection by attenuating noise injected into the conversion process.

SINGLE SUPPLY OPERATION

Figure 18 shows a circuit to power the AD7701 from a single +10 V supply, using an op amp to provide a half supply reference point for AGND and DGND. As the digital I/O pins ar referenced to this point, level shifting is required for external digital communications. If galvanic isolation is required in the system, level shifting and isolation can both be provided by opto-isolators.

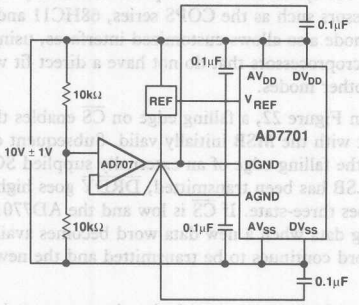


Figure 18. Single Supply Operation

SLEEP MODE

The low power standby mode is initiated by taking the $\overline{\text{SLEEP}}$ input low, which shuts down all analog and digital circuits and reduces power consumption to 10 µW. The calibration coefficients are still retained in memory, but as the converter has been quiescent, it is necessary to wait for the filter settling time (507,904 cycles) before accessing the output data.

BATTERY BACKUP OF CALIBRATION COEFFICIENTS

The calibration data stored in the AD7701's static RAM is lost whenever power is removed. In certain applications it may be desirable to protect the contents of the calibration SRAM against intermittent power loss, for example when a mains powered instrument is moved to a different location.

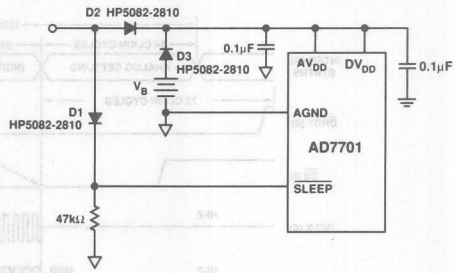


Figure 19. Battery Backup of Calibration Data

Figure 19 shows a simple battery backup circuit that maintains power to the SRAM during loss of the main +5 V supply. When power is lost, the $\overline{\text{SLEEP}}$ input goes low, reducing the power consumption to typically 10 µW, and a battery takes over from the main power supply. Note that AV_{DD} and DV_{DD} must both remain powered to retain the calibration memory. 3.6 V lithium batteries are available which can provide 1750 mA-hours before they drop below the 2 V memory-retention threshold of the AD7701. This translates to a memory-retention period of 20 years in the Sleep mode, allowing one time factory calibration of a system.

It should be noted that in this simple circuit, the supply voltage will fall below the battery voltage before it falls below the $\overline{\text{SLEEP}}$ pin threshold, and the battery will be supplying the full 4 mA operating current of the AD7701 until the supply falls below the logic 0 voltage of the $\overline{\text{SLEEP}}$ pin. This can cause excessive battery drain if power loss is frequent or the supply voltage falls slowly, for example if there are large reservoir capacitors in the system. In this case, the backup circuit should be designed so that voltage on $\overline{\text{SLEEP}}$ falls to 0.8 V before the supply voltage falls below 3.6 V.

DIGITAL INTERFACE

The AD7701's serial communications port allows easy interfacing to industry-standard microprocessors. Three different modes of operations are available, optimized for different types of interface.

SYNCHRONOUS SELF-CLOCKING MODE (SSC)

The SSC mode (MODE pin high) allows easy interfacing to serial-parallel conversion circuits in systems with parallel data communication. This mode allows interfacing to 74XX299 Universal Shift registers without any additional decoding. The SSC mode can also be used with microprocessors such as the 68HC11 and 68HC05, which allow an external device to clock their serial port.

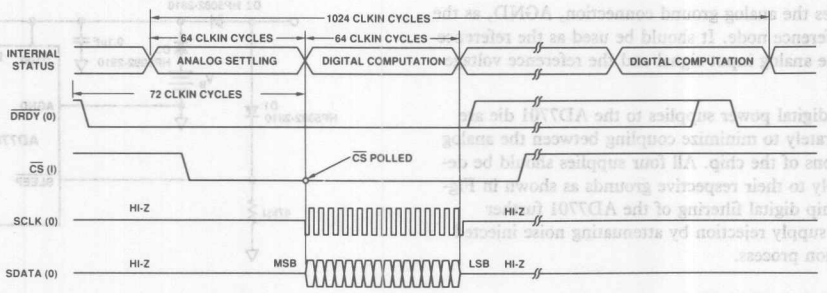


Figure 20. Timing Diagram for SSC Data Transmission Mode

Figure 20 shows the timing diagram for the SSC mode. Data is clocked out by an internally generated serial clock. The AD7701 divides each sampling interval into sixteen distinct periods. Eight periods of 64 clock pulses are for analog settling and eight periods of 64 clock pulses are for digital computation. The status of $\overline{CS}$ is polled at the beginning of each digital computation period. If it is low at any of these times then SCLK will become active and the data word currently in the output register will be transmitted, MSB first. After the LSB has been transmitted $\overline{DRDY}$ goes high and SDATA goes three-state. If $\overline{CS}$, having been brought low, is taken high again at any time during data transmission, SDATA and SCLK will go three-state after the current bit finishes. If $\overline{CS}$ is subsequently brought low, transmission will resume with the next bit during the subsequent digital computation period. If transmission has not been initiated and completed by the time the next data word is available, $\overline{DRDY}$ will go high for four clock cycles then low again as the new word is loaded into the output register.

A more detailed diagram of the data transmission in the SSC mode is shown in Figure 21. Data bits change on the falling edge of SCLK and are valid on the rising edge of SCLK.

SYNCHRONOUS EXTERNAL CLOCK MODE (SEC)

The SEC mode (MODE pin grounded) is designed for direct interface to the synchronous serial ports of industry-standard microprocessors such as the COPS series, 68HC11 and 68HC05. The SEC mode also allows customized interfaces, using I/O port pins, to microprocessors that do not have a direct fit with the AD7701's other modes.

As shown in Figure 22, a falling edge on $\overline{CS}$ enables the serial data output with the MSB initially valid. Subsequent data bits change on the falling edge of an externally supplied SCLK. After the LSB has been transmitted, $\overline{DRDY}$ goes high and SDATA goes three-state. If $\overline{CS}$ is low and the AD7701 is still transmitting data when a new data word becomes available, the old data word continues to be transmitted and the new data is lost.

If $\overline{CS}$ is taken high at any time during data transmission, SDATA will go three-state immediately. If $\overline{CS}$ returns low, the AD7701 will continue transmission with the same data bit. If transmission has not been initiated and completed by the time the next data word becomes available, and if $\overline{CS}$ is high, $\overline{DRDY}$ will return high for four clock cycles, then fall as the new word is loaded into the output register.

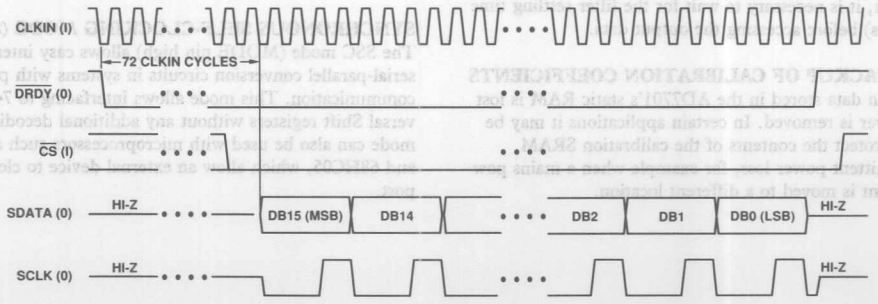


Figure 21. SSC Mode Showing Data Timing Relative to SCLK

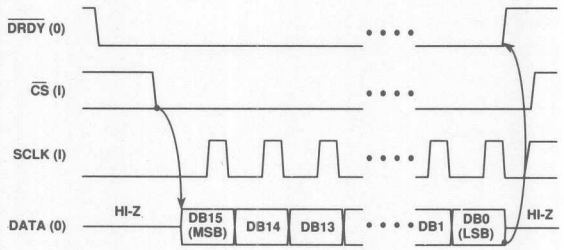


Figure 22. Timing Diagram for the SEC Mode

ASYNCHRONOUS COMMUNICATIONS (AC) MODE

The AC mode (MODE pin tied to −5 V) offers a UART-compatible interface which allows the AD7701 to transmit data asynchronously from remote locations. An external SCLK sets the baud rate and data is transmitted in two bytes in UART-compatible format. Using the AC mode, the AD7701 can be interfaced direct to microprocessors with UART interfaces, such as the 8051 and TMS70X2.

Data transmission is initiated by $\overline{CS}$ going low. If $\overline{CS}$ is low on a falling edge of SCLK, the AD7701 begins transmitting an 8-bit data byte (DB8 – DB15) with one start bit and two stop bits, as in Figure 18. The SDATA output will then go three-state. The second byte is transmitted by bringing $\overline{CS}$ low again and DB0 to DB7 are transmitted in the same format as the first byte.

UART baud rates are typically low compared to the AD7701's 4 kHz output update rate. If $\overline{CS}$ is low and data is still being transmitted when a new data word becomes available, the new data will be ignored. However, if $\overline{CS}$ has been taken high between bytes, when a new data word becomes available, the AD7701 could update the output register before the second byte is transmitted. In this case, the UART would receive the first byte of the new word instead of the second byte of the old word. When using the AC mode, care must obviously be taken to ensure that this does not occur.

DIGITAL NOISE AND OUTPUT LOADING

As mentioned earlier, the AD7701 divides its internal timing into two distinct phases, analog sampling and settling and digital computation. In the SSC mode, data is transmitted only during the digital computation periods, to minimize the effects of digital noise on analog performance. In the SEC and AC modes data transmission is externally controlled, so this automatic safeguard does not exist.

Whatever mode of operation is used, resistive and capacitive loads on digital outputs should be minimized in order to reduce crosstalk between analog and digital portions of the circuit. For this reason connection to low-power CMOS logic such as one of the 4000 series or 74C families is recommended.

It is especially important to minimize the load on SDATA in the AC mode, as transmission in this mode is inherently asynchronous. In the SEC mode the AD7701 should be synchronized to the digital system clock via CLKIN.

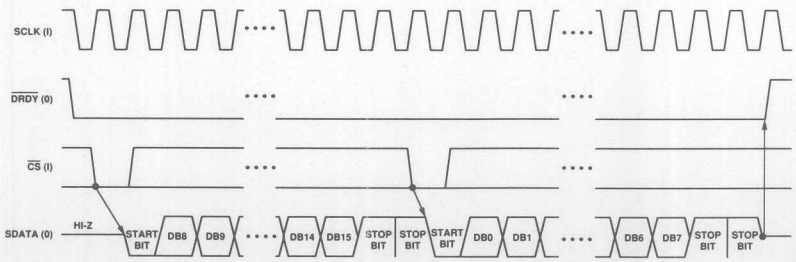


Figure 23. Timing Diagram for Asynchronous Communications Mode

LC²MOS 20-Bit A/D Converter

AD7703

FEATURES

Monolithic 20-Bit ADC
0.0003% Linearity Error
20-Bit No Missed Codes
On-Chip Self-Calibration Circuitry
Programmable Low-Pass Filter
0.1 Hz to 10 Hz Corner Frequency
0 to +2.5 V or ±2.5 V Analog Input Range
4 kSPS Output Data Rate
Flexible Serial Interface
Ultralow Power

APPLICATIONS

Industrial Process Control
Weigh Scales
Portable Instrumentation
Remote Data Acquisition

GENERAL DESCRIPTION

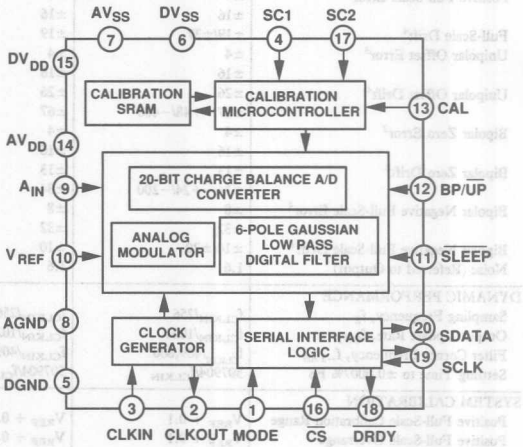
The AD7703 is a 20-bit ADC which uses a sigma delta conversion technique. The analog input is continuously sampled by an analog modulator whose mean output duty cycle is proportional to the input signal. The modulator output is processed by an on-chip digital filter with a six-pole Gaussian response, which updates the output data register with 20-bit binary words at word rates up to 4 kHz. The sampling rate, filter corner frequency and output word rate are set by a master clock input that may be supplied externally, or by an on-chip gate oscillator.

The inherent linearity of the ADC is excellent, and endpoint accuracy is ensured by self-calibration of zero and full scale which may be initiated at any time. The self-calibration scheme can also be extended to null system offset and gain errors in the input channel.

The output data is accessed through a serial port, which has two synchronous modes suitable for interfacing to shift registers or the serial ports of industry standard microcontrollers.

CMOS construction ensures low power dissipation, and a power down mode reduces the idle power consumption to only 10 μW.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. The AD7703 offers 20-bit resolution coupled with outstanding 0.0003% accuracy.
2. No missing codes ensures true, usable, 20-bit dynamic range, removing the need for programmable gain and level-setting circuitry.
3. The effects of temperature drift are eliminated by on-chip self-calibration, which removes zero and gain error. External circuits can also be included in the calibration loop to remove system offsets and gain errors.
4. A flexible synchronization allows the AD7703 to interface directly to the serial ports of industry standard microcontrollers and DSP processors.
5. Low operating power consumption and an ultralow power standby mode make the AD7703 ideal for loop powered remote sensing applications, or battery-powered portable instruments.

AD7703—SPECIFICATIONS

(T_A = +25°C; AV_{DD} = DV_{DD} = +5 V; AV_{SS} = DV_{SS} = −5 V; V_{REF} = +2.5 V; f_{CLKIN} = 4.096 MHz; BP/UP = +5 V; MODE = +5 V; A_{IN} Source Resistance = 750 Ω[1] with 1 nF to AGND at A_{IN} unless otherwise stated.)

Parameter	A/S Versions[2]	B Version[2]	C Version[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	20	20	20	Bits	
Integral Nonlinearity, T_{min} to T_{max}	±0.0015	±0.0007	±0.0003	% FSR typ	
+25°C	±0.003	±0.0015	±0.0008	% FSR max	
T_{min} to T_{max}	±0.003	±0.0015	±0.0012	% FSR max	
Differential Nonlinearity, T_{min} to T_{max}	±0.5	±0.5	±0.5	LSB typ	Guaranteed No Missing Codes
Positive Full-Scale Error[3]	±4	±4	±4	LSB typ	
	±16	±16	±16	LSB max	
Full-Scale Drift[4]	±19/±37	±19	±19	LSB typ	
Unipolar Offset Error[3]	±4	±4	±4	LSB typ	
	±16	±16	±16	LSB max	
Unipolar Offset Drift[4]	±26	±26	±26	LSB typ	Temp Range: 0 to +70°C
	±67 +48/−400	±67	±67	LSB typ	Specified Temp Range
Bipolar Zero Error[3]	±4	±4	±4	LSB typ	
	±16	±16	±16	LSB max	
Bipolar Zero Drift[4]	±13	±13	±13	LSB typ	Temp Range: 0 to +70°C
	±34 +24/−200	±34	±34	LSB typ	Specified Temp Range
Bipolar Negative Full-Scale Error[3]	±8	±8	±8	LSB typ	
	±32	±32	±32	LSB max	
Bipolar Negative Full-Scale Drift[4]	±10/±20	±10	±10	LSB typ	
Noise (Referred to Output)	1.6	1.6	1.6	LSB rms typ	
DYNAMIC PERFORMANCE					
Sampling Frequency, f_S	f_{CLKIN}/256	f_{CLKIN}/256	f_{CLKIN}/256	Hz	
Output Update Rate, f_{OUT}	f_{CLKIN}/1024	f_{CLKIN}/1024	f_{CLKIN}/1024	Hz	
Filter Corner Frequency, $f_{-3\ dB}$	f_{CLKIN}/409,600	f_{CLKIN}/409,600	f_{CLKIN}/409,600	Hz	
Settling Time to ±0.0007% FS	507904/f_{CLKIN}	507904/f_{CLKIN}	507904/f_{CLKIN}	sec	For Full-Scale Input Step
SYSTEM CALIBRATION					
Positive Full-Scale Calibration Range	V_{REF} + 0.1	V_{REF} + 0.1	V_{REF} + 0.1	V max	System Calibration Applies to
Positive Full-Scale Overrange	V_{REF} + 0.1	V_{REF} + 0.1	V_{REF} + 0.1	V max	Unipolar and Bipolar Ranges.
Negative Full-Scale Overrange	−(V_{REF} + 0.1)	−(V_{REF} + 0.1)	−(V_{REF} − + 0.1)	V max	After Calibration, if A_{IN}>V_{REF},
Maximum Offset Calibration Range[5, 6]					the Device Will Output All 1s.
Unipolar Input Range	−(V_{REF} + 0.1)	−(V_{REF} + 0.1)	−(V_{REF} + 0.1)	V max	If A_{IN}<0 (Unipolar) or −V_{REF}
Bipolar Input Range	−0.4 V_{REF} to +0.4 V_{REF}	−0.4 V_{REF} to +0.4 V_{REF}	−0.4 V_{REF} to +0.4 V_{REF}	V max	(Bipolar), the Device Will
Input Span[7]	0.8 V_{REF}	0.8 V_{REF}	0.8 V_{REF}	V min	Output all 0s
	2 V_{REF} + 0.2	2 V_{REF} + 0.2	2 V_{REF} + 0.2	V max	
ANALOG INPUT					
Unipolar Input Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Bipolar Input Range	±2.5	±2.5	±2.5	Volts	
Input Capacitance	20	20	20	pF typ	
Input Bias Current[1]	1	1	1	nA typ	
LOGIC INPUTS					
All Inputs except CLKIN					
V_{INL}, Input Low Voltage	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.0	2.0	2.0	V min	
CLKIN					
V_{INL}, Input Low Voltage	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	3.5	3.5	3.5	V min	
I_{IN}, Input Current	10	10	10	μA max	
LOGIC OUTPUTS					
V_{OL}, Output Low Voltage	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	DV_{DD}−1	DV_{DD}−1	DV_{DD}−1	V min	I_{SOURCE} = 100 μA
Floating State Leakage Current	±10	±10	±10	μA max	
Floating State Output Capacitance	9	9	9	pF typ	
POWER REQUIREMENTS[8]					
Power Supply Voltages					
Analog Positive Supply (AV_{DD})	4.5/5.5	4.5/5.5	4.5/5.5	V min/V max	For Specified Performance
Digital Positive Supply (DV_{DD})	4.5/AV_{DD}	4.5/AV_{DD}	4.5/AV_{DD}	V min/V max	
Analog Negative Supply (AV_{SS})	−4.5/−5.5	−4.5/−5.5	−4.5/−5.5	V min/V max	
Digital Negative Supply (DV_{SS})	−4.5/−5.5	−4.5/−5.5	−4.5/−5.5	V min/V max	
Calibration Memory Retention					
Power Supply Voltage	2.0	2.0	2.0	V min	

Parameter	A/S Versions[2]	B Version[2]	C Version[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE					
DC Power Supply Currents[5]					
Analog Positive Supply (AI_{DD})	3.2	3.2	3.2	mA max	Typically 2 mA
Digital Positive Supply (DI_{DD})	1.5	1.5	1.5	mA max	Typically 1 mA
Analog Negative Supply (AI_{SS})	3.2	3.2	3.2	mA max	Typically 2 mA
Digital Negative Supply (DI_{SS})	0.1	0.1	0.1	mA max	Typically 0.03 mA
Power Supply Rejection[9]					
Positive Supplies	70	70	70	dB typ	
Negative Supplies	75	75	75	dB typ	
Power Dissipation					
Normal Operation	40	40	40	mW max	$\overline{SLEEP}$ = Logic 1, Typically 25 mW
Standby Operation[10]					$\overline{SLEEP}$ = Logic 0
A, B, C	20	20	20	μW max	Typically 10 μW
S	40	40	40	μW max	

NOTES

[1]The A_{IN} pin presents a very high impedance dynamic load which varies with clock frequency. A ceramic 1 nF capacitor from the A_{IN} to AGND is necessary. Source resistance should be 750 Ω or less.

[2]Temperature Ranges are as follows: A, B, C Versions: −40°C to +85°C; S Version: −55°C to +125°C.

[3]Applies after calibration at the temperature of interest. Full-Scale Error applies for both unipolar and bipolar input ranges.

[4]Total drift over the specified temperature range after calibration at power-up at +25°C. This is guaranteed by design and/or characterization. Recalibration at any temperature will remove these errors.

[5]In unipolar mode the offset can have a negative value ($-V_{REF}$) such that the unipolar mode can mimic bipolar mode operation.

[6]The specifications for input overrange and for input span apply additional constraints on the offset calibration range.

[7]For unipolar mode, input span is the difference between full scale and zero scale. For bipolar mode, input span is the difference between positive and negative full-scale points. When using less than the maximum input span, the span range may be placed anywhere within the range of $\pm(V_{REF} + 0.1)$.

[8]All digital outputs unloaded. All digital inputs at 5 V CMOS levels.

[9]Applies in 0.1 Hz to 10 Hz bandwidth. PSRR at 60 Hz will exceed 120 dB due to the digital filter.

[10]CLKIN is stopped. All digital inputs are grounded.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

DV_{DD} to AGND . . . . . −0.3 V to +6 V
DV_{DD} to AV_{DD} . . . . . −0.3 V to +0.3 V
DV_{SS} to AGND . . . . . +0.3 V to −6 V
AV_{DD} to AGND . . . . . −0.3 V to +6 V
AV_{SS} to AGND . . . . . +0.3 V to −6 V
AGND to DGND . . . . . −0.3 V to +0.3 V
Digital Input Voltage to DGND . . . −0.3 V to DV_{DD} + 0.3 V
Analog Input Voltage to AGND
. . . . . AV_{SS} − 0.3 V to AV_{DD} + 0.3 V
Input Current to any Pin Except Supplies[1] . . . . . ±10 mA
Operating Temperature Range
Industrial (A, B, C Versions) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (DIP Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 10 mW/°C
Power Dissipation (SOIC Package) to +75°C . . . . . 250 mW
Derates above +75°C by . . . . . 15 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1]Transient currents of up to 100 mA will not cause SCR latch-up.

ORDERING GUIDE

Model	Temperature Range	Linearity Error (% FSR)	Package Option[1]
AD7703AN	−40°C to +85°C	0.003	N-20
AD7703BN	−40°C to +85°C	0.0015	N-20
AD7703CN	−40°C to +85°C	0.0012	N-20
AD7703AR	−40°C to +85°C	0.003	R-20
AD7703BR	−40°C to +85°C	0.0015	R-20
AD7703CR	−40°C to +85°C	0.0012	R-20
AD7703AQ	−40°C to +85°C	0.003	Q-20
AD7703BQ	−40°C to +85°C	0.0015	Q-20
AD7703CQ	−40°C to +85°C	0.0012	Q-20
AD7703SQ[2]	−55°C to +125°C	0.003	Q-20

NOTES

[1]N = Plastic DIP; R = SOIC; Q = Cerdip. For outline information see Package Information section.

[2]Available to /883B processing only. Contact local sales office for military data sheet.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



TIMING CHARACTERISTICS[1, 2] (AV_{DD} = DV_{DD} = +5 V ± 10%; AV_{SS} = DV_{SS} = −5 V ± 10%; AGND = DGND = 0 V; f_{CLKIN} = 4.096 MHz; Input Levels: Logic 0 = 0 V, Logic 1 = DV_{DD}; unless otherwise stated.)

Parameter	Limit at T_{min}, T_{max} (A, B, C Versions)	Limit at T_{min}, T_{max} (S Version)	Units	Conditions/Comments
f_{CLKIN}[3, 4]	40	40	kHz min	Master Clock Frequency: Internal Gate Oscillator
	5	5	MHz max	Typically 4096 kHz
	40	40	kHz min	Master Clock Frequency: Externally Supplied
	5	5	MHz max	
t_r[5]	50	50	ns max	Digital Output Rise Time. Typically 20 ns
t_f[5]	50	50	ns max	Digital Output Fall Time. Typically 20 ns
t_1	0	0	ns min	SC1, SC2 to CAL High Setup Time
t_2	50	50	ns min	SC1, SC2 Hold Time After CAL Goes High
t_3[6]	1000	1000	ns min	$\overline{SLEEP}$ High to CLKIN High Setup Time
SSC MODE				
t_4[7]	$3/f_{CLKIN}$	$3/f_{CLKIN}$	ns min	Data Access Time ($\overline{CS}$ Low to Data Valid)
t_5	100	100	ns max	SCLK Falling Edge to Data Valid Delay (25 ns typ)
t_6	250	250	ns min	MSB Data Setup Time. Typically 380 ns
t_7	300	300	ns max	SCLK High Pulse Width. Typically 240 ns
t_8	790	790	ns max	SCLK Low Pulse Width. Typically 730 ns
t_9	$1/f_{CLKIN}$ + 200	$1/f_{CLKIN}$ + 200	ns max	SCLK Rising Edge to Hi-Z Delay ($1/f_{CLKIN}$ + 100 ns typ)
t_{10}[8, 9]	$4/f_{CLKIN}$ + 200	$4/f_{CLKIN}$ + 200	ns max	$\overline{CS}$ High to Hi-Z Delay
SEC MODE				
f_{SCLK}	5	5	MHz max	Serial Clock Input Frequency
t_{11}	50	50	ns min	SCLK High Pulse Width
t_{12}	180	180	ns min	SCLK Low Pulse Width
t_{13}[7, 10]	160	160	ns max	Data Access Time ($\overline{CS}$ Low to Data Valid). Typically 80 ns
t_{14}[11]	150	150	ns min	SCLK Falling Edge to Data Valid Delay. Typically 75 ns
t_{15}[8]	250	250	ns min	$\overline{CS}$ High to Hi-Z Delay
t_{16}[8]	200	200	ns min	SCLK Falling Edge to Hi-Z Delay. Typically 100 ns

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]See Figures 1 to 6.

[3]CLKIN duty cycle range is 20% to 80%. CLKIN must be supplied whenever the AD7703 is not in SLEEP mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.

[4]The AD7703 is production tested with f_{CLKIN} at 4.096 MHz. It is guaranteed by characterization to operate at 200 kHz.

[5]Specified using 10% and 90% points on waveform of interest.

[6]In order to synchronize several AD7703s together using the $\overline{SLEEP}$ pin, this specification must be met.

[7]t_4 and t_{13} are measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[8]t_9, t_{10}, t_{15} and t_{16} are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time quoted in the Timing Characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

[9]If $\overline{CS}$ is returned high before all 20 bits are output, the SDATA and SCLK outputs will complete the current data bit and then go to high impedance.

[10]If $\overline{CS}$ is activated asynchronously to $\overline{DRDY}$, $\overline{CS}$ will not be recognized if it occurs when $\overline{DRDY}$ is high for four clock cycles. The propagation delay time may be as great as 4 CLKIN cycles plus 160 ns. To guarantee proper clocking of SDATA when using asynchronous $\overline{CS}$, The SCLK input should not be taken high sooner than 4 CLKIN cycles plus 160 ns after $\overline{CS}$ goes low.

[11]SDATA is clocked out on the falling edge of the SCLK input.

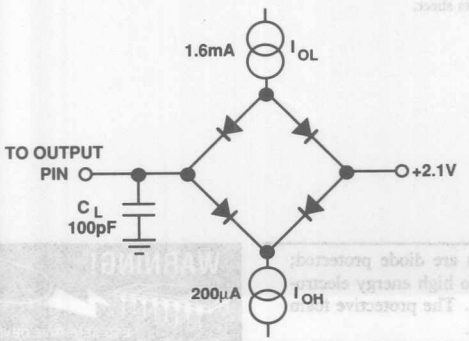


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

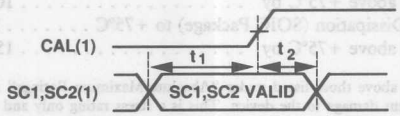


Figure 2. Calibration Control Timing

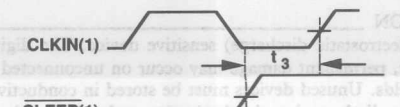


Figure 3. Sleep Mode Timing

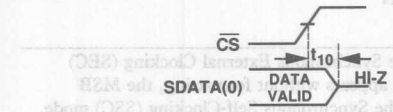


Figure 4. SSC Mode Data Hold Time

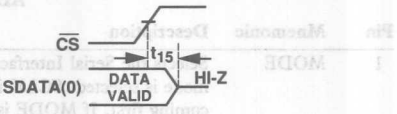


Figure 5a. SEC Mode Data Hold Time

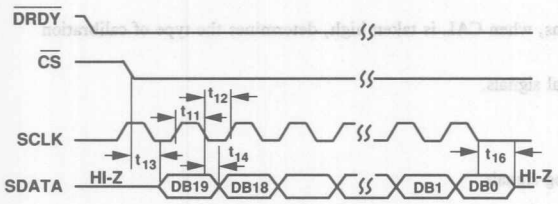


Figure 5b. SEC Mode Timing Diagram

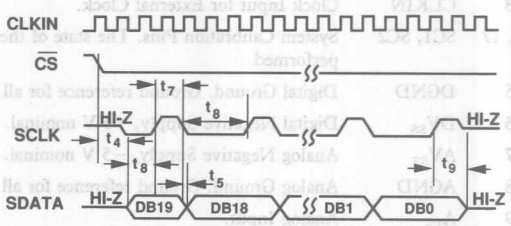


Figure 6. SSC Mode Timing Diagram

TERMINOLOGY

LINEARITY ERROR

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero-scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and full scale, a point 1.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

DIFFERENTIAL LINEARITY ERROR

This is the difference between any code's actual width and the ideal (1 LSB) width. Differential linearity error is expressed in LSBs. A differential linearity specification of ±1 LSB or less guarantees monotonicity.

POSITIVE FULL-SCALE ERROR

Positive full-scale error is the deviation of the last code transition (111 . . . 110 to 111 . . . 111) from the ideal (V_{REF} − 3/2 LSBs). It applies to both positive and negative analog input ranges.

UNIPOLAR OFFSET ERROR

Unipolar offset error is the deviation of the first code transition from the ideal (AGND + 0.5 LSB) when operating in the unipolar mode.

BIPOLAR ZERO ERROR

This is the deviation of the midscale transition (0111 . . . 111 to 1000 . . . 000) from the ideal (AGND − 0.5 LSB) when operating in the bipolar mode.

BIPOLAR NEGATIVE FULL-SCALE ERROR

This is the deviation of the first code transition from the ideal ($-V_{REF}$ + 0.5 LSB), when operating in the bipolar mode.

POSITIVE FULL-SCALE OVERRANGE

Positive full-scale overrange is the amount of overhead available to handle input voltages greater than $+V_{REF}$ (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or overflowing the digital filter.

NEGATIVE FULL-SCALE OVERRANGE

This is the amount of overhead available to handle voltages below $-V_{REF}$ without overloading the analog modulator or overflowing the digital filter. Note that the analog input will accept negative voltage peaks even in the unipolar mode.

OFFSET CALIBRATION RANGE

In the system calibration modes (SC2 Low) the AD7703 calibrates its offset with respect to the A_{IN} pin. The offset calibration range specification defines the range of voltages that the AD7701 can accept and still calibrate offset accurately.

FULL-SCALE CALIBRATION RANGE

This is the range of voltages that the AD7703 can accept in the system calibration mode and still calibrate full scale correctly.

INPUT SPAN

In system calibration schemes, two voltages applied in sequence to the AD7703's analog input define the analog input range. The input span specification defines the minimum and maximum input voltages from zero to full scale that the AD7703 can accept and still calibrate gain accurately.

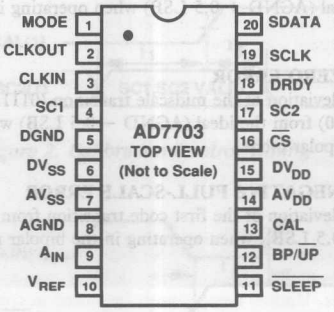
AD7703 PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	MODE	Selects the Serial Interface Mode. If MODE is tied to DGND, the Synchronous External Clocking (SEC) mode is selected. SCLK is configured as an input, and the output appears without formatting, the MSB coming first. If MODE is tied to +5 V, the AD7703 operates in the Synchronous Self-Clocking (SSC) mode. SCLK is configured as an output, with a clock frequency of $f_{CLKIN}/4$ and 25% duty cycle.
2	CLKOUT	Clock Output to generate an Internal Master Clock by connecting a crystal between CLKOUT and CLKIN. If an external clock is used, CLKOUT is left open circuit.
3	CLKIN	Clock Input for External Clock.
4, 17	SC1, SC2	System Calibration Pins. The state of these pins, when CAL is taken high, determines the type of calibration performed.
5	DGND	Digital Ground. Ground reference for all digital signals.
6	DV_{SS}	Digital Negative Supply, −5 V nominal.
7	AV_{SS}	Analog Negative Supply, −5 V nominal.
8	AGND	Analog Ground. Ground reference for all analog signals.
9	A_{IN}	Analog Input.
10	V_{REF}	Voltage Reference Input, +2.5 V nominal. This determines the value of positive full scale in the unipolar mode and of both positive and negative full-scale in the Bipolar Mode.
11	$\overline{SLEEP}$	Sleep mode pin. When this pin is taken Low, the AD7703 goes into a low-power mode with typically 10 μW power consumption.
12	BP/$\overline{UP}$	Bipolar/Unipolar mode pin. When this pin is low the AD7703 is configured for a unipolar input range of AGND to V_{REF}. When Pin 12 is High, the AD7703 is configured for a bipolar input range, $\pm V_{REF}$.
13	CAL	Calibration mode pin. When CAL is taken High for more than 4 master clock cycles, the AD7703 is reset and performs a calibration cycle when CAL is brought Low again. The CAL pin can also be used as a strobe to synchronize the operation of several AD7703s.
14	AV_{DD}	Analog Positive Supply, +5 V nominal.
15	DV_{DD}	Digital Positive Supply, +5 V nominal.
16	$\overline{CS}$	Chip Select Input. When $\overline{CS}$ is brought low, the AD7703 will begin to transmit serial data in a format determined by the state of the MODE pin.
18	$\overline{DRDY}$	Data Ready Output. $\overline{DRDY}$ is low when valid data is available in the output register. It goes High after transmission of a word is completed. It also goes High for four clock cycles when a new data word is being loaded into the output register, to indicate that valid data is not available, irrespective of whether data transmission is complete or not.
19	SCLK	Serial Clock Input/Output. The SCLK pin in configured as an input or output, dependent on the type of serial data transmission that has been selected by the MODE pin. When configured as an output in the Synchronous Self-Clocking mode, it has a frequency of $f_{CLKIN}/4$ and a duty cycle of 25%.
20	SDATA	Serial Data Output. The AD7703's output data is available at this pin as a 20-bit serial word.

	UNIPOLAR MODE			BIPOLAR MODE		
μV	LSBs	% FS	ppm FS	LSBs	% FS	ppm FS
0.596	0.25	0.0000238	0.24	0.13	0.0000119	0.12
1.192	0.5	0.0000477	0.48	0.26	0.0000238	0.24
2.384	1.00	0.0000954	0.95	0.5	0.0000477	0.48
4.768	2.00	0.0001907	1.91	1.00	0.0000954	0.95
9.537	4.00	0.0003814	3.81	2.00	0.0001907	1.91

Table I. Bit Weight Table (2.5 V Reference Voltage)

PIN CONFIGURATION



GENERAL DESCRIPTION

The AD7703 is a 20-bit A/D converter with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals such as those representing chemical, physical or biological processes. It contains a charge-balancing (sigma delta) ADC, calibration microcontroller with on-chip static RAM, a clock oscillator and a serial communications port.

The analog input signal to the AD7703 is continuously sampled at a rate determined by the frequency of the master clock, CLKIN. A charge-balancing A/D converter (sigma delta modulator) converts the sampled signal into a digital pulse train whose duty cycle contains the digital information. A six-pole Gaussian digital low pass filter processes the output of the sigma-delta modulator and updates the 20-bit output register at a 4 kHz rate. The output data can be read from the serial port randomly or periodically at any rate up to 4 kHz.

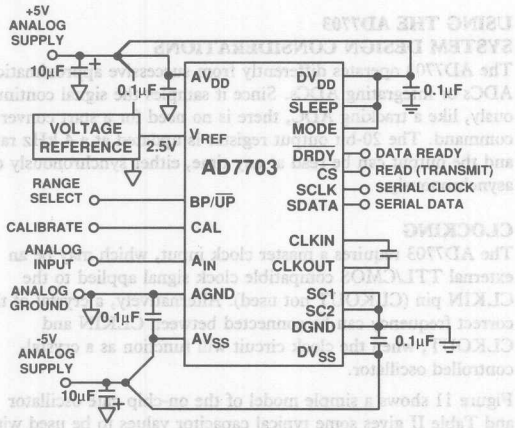


Figure 7. Typical System Connection Diagram

The AD7703 can perform self-calibration using the on-chip calibration microcontroller and SRAM to store calibration parameters. A calibration cycle may be initiated at any time using the CAL control input.

Other system components may also be included in the calibration loop to remove offset and gain errors in the input channel.

For battery operation, the AD7703 also offers a standby mode that reduces idle power consumption to typically 10 µW.

THEORY OF OPERATION

The general block diagram of a sigma-delta ADC is shown in Figure 8. It contains the following elements:

1. A sample-hold amplifier
2. A differential amplifier or subtractor
3. An analog low pass filter
4. A 1-bit A/D converter (comparator)
5. A 1-bit DAC
6. A digital low pass filter

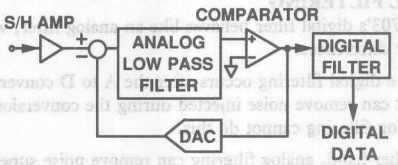


Figure 8. General Sigma Delta ADC

In operation, the sampled analog signal is fed to the subtractor, along with the output of the 1-bit DAC. The filtered difference signal is fed to the comparator, whose output samples the difference signal at a frequency many times that of the analog signal frequency (oversampling).

Oversampling is fundamental to the operation of sigma-delta ADCs. Using the quantization noise formula for an ADC:

$$SNR = (6.02 \times number\ of\ bits + 1.76)\ dB,$$

a 1-bit ADC or comparator yields an SNR of 7.78 dB.

The AD7703 samples the input signal at 16 kHz, which spreads the quantization noise from 0 to 8 kHz. Since the specified analog input bandwidth of the AD7701 is only 0 to 10 Hz, the noise energy in this bandwidth would be only 1/800 of the total quantization noise, assuming that the noise energy was spread evenly throughout the spectrum. It is reduced still further by analog filtering in the modulator loop, which shapes the quantization noise spectrum to move most of the noise energy to frequencies above 10 Hz. The SNR performance in the 0 to 10 Hz range is conditioned to the 20-bit level in this fashion.

The output of the comparator provides the digital input for the 1-bit DAC, so the system functions as a negative feedback loop which minimizes the difference signal. The digital data that represents the analog input voltage is in the duty cycle of the pulse train appearing at the output of the comparator. It can be retrieved as a parallel binary data word using a digital filter.

Sigma delta ADCs are generally described by the order of the analog low pass filter. A simple example of a first order sigma delta ADC is shown in Figure 8. This contains only a first-order low pass filter or integrator.

The AD7703 uses a second order sigma delta modulator and a digital filter that provides a rolling average of the sampled output. After power up or if there is a step change in the input voltage, there is a settling time before valid data is obtained.

The AD7703's digital filter behaves like an analog filter, with a few minor differences.

First, since digital filtering occurs after the A to D conversion process, it can remove noise injected during the conversion process. Analog filtering cannot do this.

On the other hand, analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. Digital filtering cannot do this and noise peaks riding on signals near full scale have the potential to saturate the analog modulator and digital filter, even though the average value of the signal is within limits. To alleviate this problem, the AD7703 has overrange headroom built into the sigma-delta modulator and digital filter which allows overrange excursions of 100 mV. If noise signals are larger than this, consideration should be given to analog input filtering, or to reducing the gain in the input channel so that a full-scale input (2.5 V) gives only a half-scale input to the AD7703 (1.25 V). This will provide an overrange capability greater than 100% at the expense of reducing the dynamic range by 1 bit (50%).

FILTER CHARACTERISTICS

The cutoff frequency of the digital filter is $f_{CLK}/409600$. At the maximum clock frequency of 4.096 MHz, the cutoff frequency of the filter is 10 Hz and the data update rate is 4 kHz.

Figure 9 shows the filter frequency response. This is a 6-pole Gaussian response that provides 55 dB of 60 Hz rejection for a 10 Hz cutoff frequency. If the clock frequency is halved to give a 5 Hz cutoff, 60 Hz rejection is better than 90 dB.

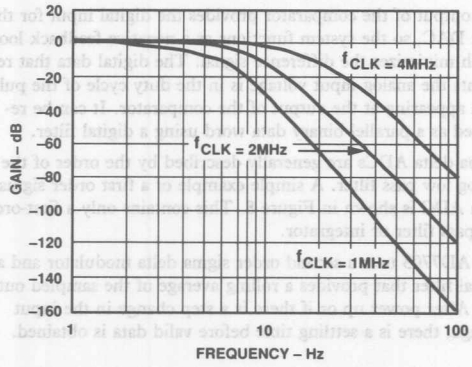


Figure 9. Frequency Response of AD7703 Filter

Since the AD7703 contains this low-pass filtering, there is a settling time associated with step function inputs, and data will be invalid after a step change until the settling time has elapsed. The AD7703 is, therefore, unsuitable for high speed multiplexing, where channels are switched and converted sequentially at high rates, as switching between channels can cause a step change in the input. However, slow multiplexing of the AD7703 is possible, provided that the settling time is allowed to elapse before data for the new channel is accessed.

The output settling of the AD7703 in response to a step input change is shown in Figure 10. The Gaussian response has fast settling with no overshoot, and the worst-case settling time to ±0.0007% is 125 ms with a 4.096 MHz master clock frequency.

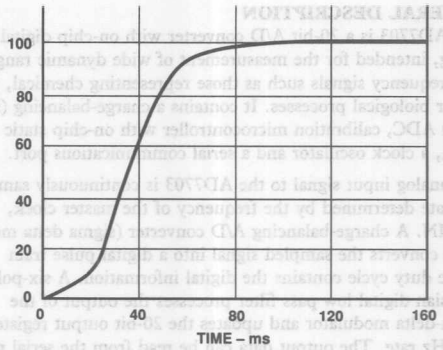


Figure 10. AD7703 Step Response

USING THE AD7703 SYSTEM DESIGN CONSIDERATIONS

The AD7703 operates differently from successive approximation ADCs or integrating ADCs. Since it samples the signal continuously, like a tracking ADC, there is no need for a start convert command. The 20-bit output register is updated at a 4 kHz rate, and the output can be read at any time, either synchronously or asynchronously.

CLOCKING

The AD7703 requires a master clock input, which may be an external TTL/CMOS compatible clock signal applied to the CLKIN pin (CLKOUT not used). Alternatively, a crystal of the correct frequency can be connected between CLKIN and CLKOUT, when the clock circuit will function as a crystal-controlled oscillator.

Figure 11 shows a simple model of the on-chip gate oscillator and Table II gives some typical capacitor values to be used with various resonators.

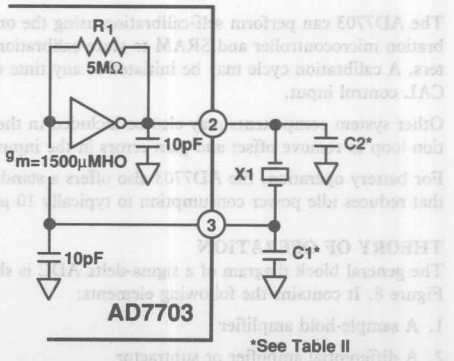


Figure 11. On-Chip Gate Oscillator

Resonators	C1	C2
Ceramic		
200 kHz	330 pF	470 pF
455 kHz	100 pF	100 pF
1.0 MHz	50 pF	50 pF
2.0 MHz	20 pF	20 pF
Crystals		
2.000 MHz	30 pF	30 pF
3.579 MHz	20 pF	20 pF
4.096 MHz	None	None

Table II. Resonator Loading Capacitors

The input sampling frequency, output data rate, filter characteristics and calibration time are all directly related to the master clock frequency f_{CLKIN} by the ratios given in the specification table under Dynamic Performance. Therefore, the first step in system design with the AD7703 is to select a master clock frequency suitable for the bandwidth and output data rate required by the application.

ANALOG INPUT RANGES

The AD7703 performs conversion relative to an externally supplied reference voltage, which allows easy interfacing to ratiometric systems. In addition, either unipolar or bipolar input voltage ranges may be selected using the BP/$\overline{UP}$ input. With BP/$\overline{UP}$ tied low, the input range is unipolar and the span is ($V_{REF} - V_{AGND}$), where V_{AGND} is the voltage at the device AGND pin. With BP/$\overline{UP}$ tied high, the input range is bipolar and the span is 2 V_{REF}. In the bipolar mode both positive and negative full scale are directly determined by V_{REF}. This offers superior tracking of positive and negative full scale and better midscale (bipolar zero) stability than bipolar schemes that simply scale and offset the input range.

The digital output coding for the unipolar range is unipolar binary and for the bipolar range it is offset binary. Bit weights for the unipolar and bipolar modes are shown in Table I.

ACCURACY

Sigma delta ADCs, like VFCs and other integrating ADCs, do not contain any source of nonmonotonicity and inherently offer no missing codes performance.

The AD7703 achieves excellent linearity by the use of high quality, on-chip silicon dioxide capacitors, which have a very low capacitance/voltage coefficient. The device also achieves low input drift through the use of chopper-stabilized techniques in its input stage. To ensure excellent performance over time and temperature, the AD7703 uses digital calibration techniques which minimize offset and gain error to typically ±4 LSBs.

AUTOCALIBRATION

The AD7703 offers both self calibration and system calibration facilities. For calibration to occur, the on-chip microcontroller must record the modulator output for two different input conditions. These are the "zero scale" and "full scale" points. In unipolar self-calibration mode, the zero scale point is V_{AGND} and the full-scale point is V_{REF}. With these readings the microcontroller can calculate the gain slope for the input to output transfer function of the converter. In unipolar mode the slope factor is determined by dividing the span between zero and full scale by 2^{20}. In bipolar mode it is determined by dividing the span by 2^{19} since the inputs applied represent only half the total codes. In both unipolar and bipolar modes the slope factor is saved and used to calculate the binary output code when an analog input is applied to the device. Table IV gives the output code size after calibration.

System calibration allows the AD7703 to compensate for system gain and offset errors. A typical circuit where this might be used is shown in Figure 12.

System calibration performs the same slope factor calculations as self calibration but uses voltage values presented by the system to the A_{IN} pin for the zero and full-scale points. There are two system calibration modes.

The first mode offers system level calibration for system offset and system gain. This is a two step operation. The zero scale point must be presented to the converter first. It must be applied to the converter before the calibration step is initiated and remain stable until the step is complete. The $\overline{DRDY}$ output from the device will signal when the step is complete by going low. After the zero scale point is calibrated the full-scale point is applied and the second calibration step is initiated. Again the voltage must remain stable throughout the calibration step.

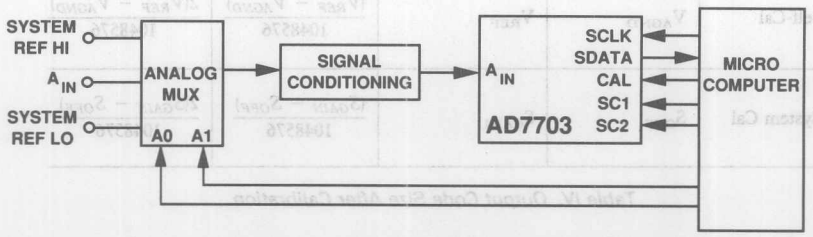


Figure 12. Typical Connections for System Calibration

The two step calibration mode offers another feature. After the sequence has been completed, additional offset calibrations can be performed by themselves to adjust the zero reference point to a new system zero reference value. This second system calibration mode uses an input voltage for the zero-scale calibration point but uses the V_{REF} value for the full-scale point.

Initiating Calibration

Table III illustrates the calibration modes available in the AD7703. Not shown in the table is the function of the BP/$\overline{UP}$ pin which determines whether the converter has been calibrated to measure bipolar or unipolar signals. A calibration step is initiated by bringing the CAL pin high for at least 4 CLKIN cycles and then bringing it low again. The states of SC1 and SC2 along with the BP/$\overline{UP}$ pin will determine the type of calibration to be performed. All three signals should be stable before the CAL pin is taken positive. The SC1 and SC2 inputs are latched when CAL goes high. The BP/$\overline{UP}$ input is not latched and therefore must remain in a fixed state throughout the calibration and measurement cycles. Any time the state of the BP/$\overline{UP}$ is changed, a new calibration cycle must be performed to enable the AD7703 to function properly in the new mode.

When a calibration step is initiated, the $\overline{DRDY}$ signal will go high and remain high until the step is finished. Table III shows the number of clock cycles each calibration requires. Once a calibration step is initiated it must finish before a new calibration step can be executed. In the two step system calibration mode, the offset calibration step must be initiated before initiating the gain calibration step.

When self-calibration is completed $\overline{DRDY}$ falls and the output port is updated with a data word that represents the analog input signal. When a system calibration step is completed, $\overline{DRDY}$ will fall and the output port will be updated with the appropriate data value (all 0s for the zero scale point and all 1s for the full-scale point). In the system calibration mode, the digital filter must settle before the output code will represent the value of the analog input signal. Tables IV and V indicate the output code size and output coding of the AD7703 in its various modes. In these tables, S_{OFF} is the measured system offset in volts and S_{GAIN} is the measured system gain at the full-scale point in volts.

Span and Offset Limits

Whenever a system calibration mode is used, there are limits on the amount of offset and span which can be accommodated. The range of input span in both the unipolar and bipolar modes has a minimum value of 0.8 V_{REF} and a maximum value of 2 (V_{REF} + 0.1 V).

The amount of offset which can be accommodated depends on whether the unipolar or bipolar mode is being used. In unipolar mode, the system calibration modes can handle a maximum offset of 0.2 V_{REF} and a minimum offset of − (V_{REF}+ 0.1 V). Thus the AD7703 in the unipolar mode can be calibrated to mimic bipolar operation.

CAL	SC1	SC2	CAL TYPE	ZERO SCALE CAL	FULL-SCALE CAL	SEQUENCE	CALIBRATION TIME
	0	0	Self-Cal	V_{AGND}	V_{REF}	One Step	3,145,655 Clock Cycles
	1	1	System Offset	A_{IN}	–	1st Step	1,052,599 Clock Cycles
	0	1	System Gain	–	A_{IN}	2nd Step	1,068,813 Clock Cycles
	1	0	System Offset	A_{IN}	V_{REF}	One Step	2,117,389 Clock Cycles

NOTE

$\overline{DRDY}$ remains high throughout the calibration sequence. In the Self-Cal mode, $\overline{DRDY}$ falls once the AD7703 has settled to the analog input. In all other modes $\overline{DRDY}$ falls as the device begins to settle.

Table III. Calibration Truth Table

			1 LSB	
CAL MODE	ZERO SCALE	GAIN FACTOR	UNIPOLAR	BIPOLAR
Self-Cal	V_{AGND}	V_{REF}	$\frac{(V_{REF} - V_{AGND})}{1048576}$	$\frac{2(V_{REF} - V_{AGND})}{1048576}$
System Cal	S_{OFF}	S_{GAIN}	$\frac{(S_{GAIN} - S_{OFF})}{1048576}$	$\frac{2(S_{GAIN} - S_{OFF})}{1048576}$

Table IV. Output Code Size After Calibration

INPUT VOLTAGE, UNIPOLAR MODE			INPUT VOLTAGE, BIPOLAR MODE	
System Cal	Self-Cal	Output Codes	Self-Cal	System-Cal
> (S_{GAIN} − 1.5 LSB)	> (V_{REF} − 1.5 LSB)	FFFFF	> (V_{REF} − 1.5 LSB)	> (S_{GAIN} − 1.5 LSB)
S_{GAIN} − 1.5 LSB	V_{REF} − 1.5 LSB	FFFFF / FFFFE	V_{REF} − 1.5 LSB	S_{GAIN} − 1.5 LSB
(S_{GAIN} − S_{OFF})/2 − 0.5 LSB	(V_{REF} − V_{AGND})/2 − 0.5 LSB	80000 / 7FFFF	V_{AGND} − 0.5 LSB	S_{OFF} − 0.5 LSB
S_{OFF} + 0.5 LSB	V_{AGND} + 0.5 LSB	00001 / 00000	−V_{REF} + 0.5 LSB	−S_{GAIN} + 2 S_{OFF} + 0.5 LSB
<(S_{OFF} + 0.5 LSB)	<(V_{AGND} + 0.5 LSB)	00000	<(−V_{REF} + 0.5 LSB)	<(−S_{GAIN} +2 S_{OFF} + 0.5 LSB)

Table V. AD7703 Output Coding

In the bipolar mode the system offset calibration range is restricted to ±0.4 V_{REF}. It should be noted that the span restrictions limit the amount of offset which can be calibrated. The span range of the converter in bipolar mode is equidistant around the voltage used for the zero scale point. When the zero-scale point is calibrated it must not cause either of the two endpoints of the bipolar transfer function to exceed the positive or the negative input overrange points (+V_{REF} + 0.1) V or −(V_{REF} + 0.1) V. If the span range is set to a minimum (0.8 V_{REF}) the offset voltage can move ±0.4 V_{REF} without causing the end points of the transfer function to exceed the overrange points. Alternatively, if the span range is set to 2 V_{REF}, the input offset cannot move more than +0.1 V or −0.1 V before an endpoint of the transfer function exceeds the input overrange limit.

POWER UP AND CALIBRATION

A calibration cycle must be carried out after power up to initialize the device to a consistent starting condition and correct calibration. The CAL pin must be held high for at least four clock cycles, after which calibration is initiated on the falling edge of CAL and takes a maximum of 3,145,655 clock cycles (approximately 768 ms with a 4.096 MHz clock). See Table III.

Figure 13 shows a simple RC circuit which will briefly pull the CAL input High as power is applied. For this circuit to work the power supply must come up cleanly without oscillation, otherwise the internal circuits of the AD7703 may not all recognize the same reset transition. This can be overcome by using a Schmitt-trigger inverter between the RC combination and the CAL input, to provide a single transition. After power up, it is necessary to wait for the filter settling time (507,904 clock cycles) before accessing the output data. Thereafter data may be read at a 4 kHz rate.

The type of calibration cycle initiated by CAL is determined by the SC1 and SC2 inputs, in accordance with Table III.

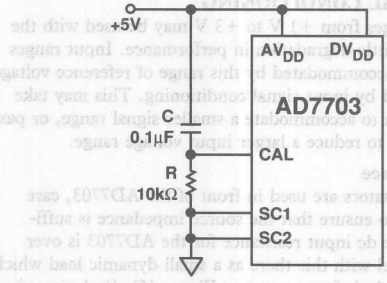


Figure 13. Power-On Reset Circuit

Drift Considerations

The AD7703 uses chopper stabilization techniques to minimize input offset drift. Charge injection in the analog switches and leakage currents at the sampling node are the primary sources of offset voltage drift in the converter. Figure 14 indicates the typical offset due to temperature changes after calibration at 25°C. Drift is relatively flat up to 75°C. Above this temperature, leakage current becomes the main source of offset drift. Since leakage current doubles approximately every 10°C, the offset drifts accordingly. The value of the voltage on the sample capacitor is updated at a rate determined by the master clock, therefore the amount of offset drift which occurs will be proportional to the elapsed time between samples. Thus, to minimize offset drift at higher temperatures, higher CLKIN rates are recommended.

Gain drift within the converter depends mainly upon the temperature tracking of the internal capacitors. It is not affected by leakage currents so that it is significantly less than offset drift. The typical gain drift of the AD7703 is less than 40 LSBs over the specified temperature range.

Measurement errors due to offset drift or gain drift can be eliminated at any time by recalibrating the converter. Using the system calibration mode can also minimize offset and gain errors in the signal conditioning circuitry. Integral and differential linearity are not significantly affected by temperature changes.

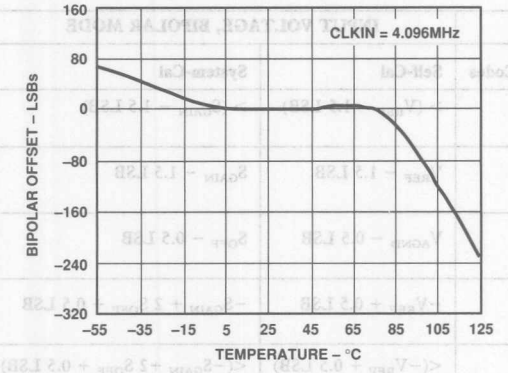


Figure 14. Typical Bipolar Offset vs. Temperature after Calibration at 25°C

INPUT SIGNAL CONDITIONING

Reference voltages from +1 V to +3 V may be used with the AD7703, with little degradation in performance. Input ranges that cannot be accommodated by this range of reference voltages may be achieved by input signal conditioning. This may take the form of gain to accommodate a smaller signal range, or passive attenuation to reduce a larger input voltage range.

Source Resistance

If passive attenuators are used in front of the AD7703, care must be taken to ensure that the source impedance is sufficiently low. The dc input resistance for the AD7703 is over 1 GΩ. In parallel with this there as a small dynamic load which varies with the clock frequency (see Figure 15). Each time the

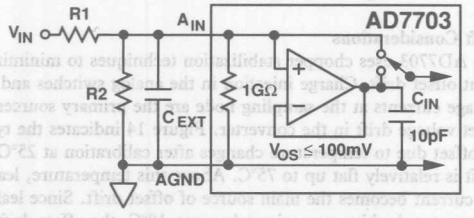


Figure 15. Equivalent Input Circuit and Input Attenuator

analog input is sampled, a 10 pF capacitor draws a charge packet of maximum 1 pC (10 pF × 100 mV) from the analog source with a frequency $f_{CLKIN}/256$. For a 4.096 MHz CLKIN, this yields an average current draw of 16 nA. After each sample the AD7703 allows 62 clock periods for the input voltage to settle. The equation which defines settling time is:

$$V_O = V_{IN}[1 - e^{-t/RC}]$$

where V_O is the final settled value, V_{IN} is the value of the input signal, R is the value of the input source resistance, C is the 10 pF sample capacitor. The value of t is equal to $62/f_{CLKIN}$. The following equation can be developed which gives the maximum allowable source resistance, $R_{S(MAX)}$, for an error of V_E.

$$R_{S(MAX)} = \frac{62}{f_{CLKIN} \cdot (10\ pF) \cdot 1\ n\ (100mV/V_E)}$$

Provided the source resistance is less than this value, the analog input will settle within the desired error band in the requisite 62 clock periods. Insufficient settling leads to offset errors. These can be calibrated in system calibration schemes.

If a limit of 600 nV (0.25 LSB at 20 bits) is set for the maximum offset voltage, then the maximum allowable source resistance is 125 kΩ from the above equation, assuming that there is no external stray capacitance.

An RC filter may be added in front of the AD7703 to reduce high frequency noise. With an external capacitor added from A_{IN} to AGND, the following equation will specify the maximum allowable source resistance:

$$R_{S(MAX)} = \frac{62}{f_{CLKIN} \cdot (C_{IN} + C_{EXT}) \cdot 1\ n \left[\frac{100\ mV \cdot \frac{C_{IN}}{(C_{IN} + C_{EXT})}}{V_E}\right]}$$

The practical limit to the maximum value of source resistance is thermal (Johnson) noise. A practical resistor may by modeled as an ideal (noiseless) resistor in series with a noise voltage source or in parallel with a noise current source.

$$V_n = \sqrt{4\ kTRf}\ Volts$$

$$i_n = \sqrt{4\ kTf/R}\ Amperes$$

where k is Boltzmann's constant (1.38×10^{-23} J/K), and T is temperature in degrees Kelvin (°C + 273).

Active signal conditioning circuits such as op amps generally do not suffer from problems of high source impedance. Their open-loop output resistance is normally only tens of ohms and, in any case, most modern general purpose op amps have sufficiently fast closed loop settling time for this not to be a problem. Offset voltage in op amps can be eliminated in a system calibration routine.

Antialias Considerations

The digital filter of the AD7703 does not provide any rejection at integer multiples of the sampling frequency ($nf_{CLKIN}/256$, where n = 1, 2, 3, . .).

With a 4.096 MHz master clock there are narrow (±10 Hz) bands at 16 kHz, 32 kHz, 48 kHz, etc., where noise passes unattenuated to the output.

However, due to the AD7703's high oversampling ratio of 800 (16 kHz to 20 Hz) these bands occupy only a small fraction of the spectrum, and most broadband noise is filtered.

The reduction in broadband noise is given by:

$$e_{out} = e_{in}\sqrt{2f_C / f_S} = 0.035\ e_{in}$$

where e_{in} and e_{out} are rms noise terms referred to the input and f_C is the filter −3 dB corner frequency ($f_{CLKIN}/409600$) and f_S is the sampling frequency ($f_{CLKIN}/256$).

Since the ratio of f_S to f_{CLKIN} is fixed, the digital filter reduces broadband white noise by 96.5% independent of the master clock frequency.

VOLTAGE REFERENCE CONNECTIONS

The voltage applied to the V_{REF} pin defines the analog input range. The specified reference voltage is 2.5 V, but the AD7703 will operate with reference voltages from 1 V to 3 V with little degradation in performance.

The reference input presents exactly the same dynamic load as the analog input, but in the case of the reference input, source resistance and long settling time introduce gain errors rather than offset errors. Fortunately, most precision references have sufficiently low output impedance and wide enough bandwidth to settle to the required accuracy within 62 clock cycles.

The digital filter of the AD7703 removes noise from the reference input, just as it does with noise at the analog input, and the same limitations apply regarding lack of noise rejection at integer multiples of the sampling frequency. Note that the reference should be chosen to minimize noise below 10 Hz. The AD7703 typically exhibits 1.6 LSB rms noise in its measurements. This specification assumes a clean reference. Many monolithic bandgap references are available which can supply the 2.5 V needed for the AD7703. However, some of these are not specified for noise especially in the 0.1 Hz to 10 Hz bandwidth. If the reference noise in this bandwidth is excessive, it can degrade the performance of the AD7703. Recommended references are the AD580 and the LT1019. Both of these 2.5 V references typically have less than 10 μV p–p noise in the 0.1 Hz to 10 Hz band.

POWER SUPPLIES AND GROUNDING

AGND is the ground reference voltage for the AD7703, and is completely independent of DGND. Any noise riding on the AGND input with respect to the system analog ground will cause conversion errors. AGND should therefore be used as the system ground and also as the ground for the analog input and the reference voltage.

The analog and digital power supplies to the AD7703 are independent and separately pinned out, to minimize coupling between analog and digital sections of the device. The digital filter will provide rejection of broadband noise on the power supplies, except at integer multiples of the sampling frequency. Therefore, the two analog supplies should be individually decoupled to AGND using 100 nF ceramic capacitors to provide power supply noise rejection at these frequencies. The two digital supplies should similarly be decoupled to DGND.

The positive digital supply (DV_{DD}) must never exceed the positive analog supply (AV_{DD}) by more than 0.3 V. Power supply sequencing is therefore important. If separate analog and digital supplies are used, care must be taken to ensure that the analog supply is powered up first.

It is also important that power is applied to the AD7703 before signals at V_{REF}, A_{IN} or the logic input pins in order to avoid any possibility of latch-up. If separate supplies are used for the AD7703 and the system digital circuitry, then the AD7703 should be powered up first.

A typical scheme for powering the AD7703 from a single set of ±5 V rails is shown Figure 7. In this circuit AV_{DD} and DV_{DD} are brought along separate tracks from the same +5 V supply. Thus, there is no possibility of the digital supply coming up before the analog supply.

SLEEP MODE

The low power standby mode is initiated by taking the $\overline{SLEEP}$ input low, which shuts down all analog and digital circuits and reduces power consumption to 10 μW. When coming out of SLEEP mode it is sometimes possible (when using a crystal to generate CLKIN, for example) to lose the calibration coefficients. Therefore, it is advisable as a safeguard to always do a calibration cycle after coming out of SLEEP mode.

BATTERY BACKUP OF CALIBRATION COEFFICIENTS

The calibration data stored in the AD7703's static RAM is lost whenever power is removed. In certain applications it may be desirable to protect the contents of the calibration SRAM against intermittent power loss, for example when a mains powered instrument is moved to a different location.

Figure 16 shows a simple battery backup circuit that maintains power to the SRAM during loss of the main +5 V supply. When power is lost, the $\overline{SLEEP}$ input goes low, reducing the power consumption to typically 10 μW, and a battery takes over from the main power supply. Note that AV_{DD} and DV_{DD} must both remain powered to retain the calibration memory. 3.6 V lithium batteries are available which can provide 1750 mA hours before they drop below the 2 V memory retention threshold of the AD7703. This translates to a memory-retention period of 20 years in the Sleep mode, allowing one time factory calibration of a system.

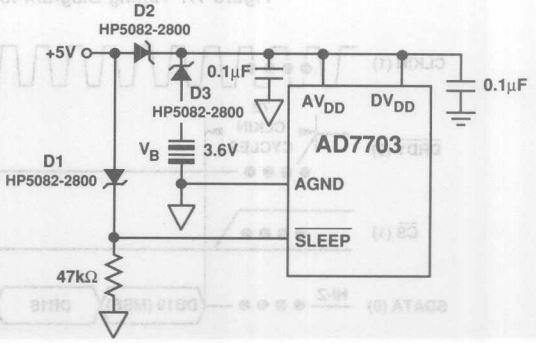


Figure 16. Battery Backup of Calibration Data

It should be noted that in this simple circuit, the supply voltage will fall below the battery voltage before it falls below the $\overline{SLEEP}$ pin threshold, and the battery will be supplying the full 2 mA operating current of the AD7703 until the supply falls below the logic 0 voltage of the $\overline{SLEEP}$ pin. This can cause excessive battery drain if power loss is frequent or the supply voltage falls slowly, for example if there are large reservoir capacitors in the system. In this case, the backup circuit should be designed so that voltage on $\overline{SLEEP}$ falls to 0.8 V before the supply voltage falls below 3.6 V.

DIGITAL INTERFACE

The AD7703's serial communications port allows easy interfacing to industry standard microprocessors. Two different modes of operation are available, optimized for different types of interface.

SYNCHRONOUS SELF-CLOCKING MODE (SSC)

The SSC mode (MODE pin high) allows easy interfacing to serial-parallel conversion circuits in systems with parallel data communication. This mode allows interfacing to 74XX299 Universal Shift registers without any additional decoding. The SSC mode can also be used with microprocessors such as the 68HC11 and 68HC05, which allow an external device to clock their serial port.

Figure 17 shows the timing diagram for the SSC mode. Data is clocked out by an internally generated serial clock. The AD7703 divides each sampling interval into sixteen distinct periods. Eight periods of 64 clock pulses are for analog settling and eight periods of 64 clock pulses are for digital computation. The status of $\overline{CS}$ is polled at the beginning of each digital computation period. If it is low at any of these times then SCLK will become active and the data word currently in the output register will be transmitted, MSB first. After the LSB has been transmitted $\overline{DRDY}$ will go high until the new data word becomes available. If $\overline{CS}$, having been brought low, is taken high again at any time during data transmission, SDATA and SCLK will go three-state after the current bit finishes. If $\overline{CS}$ is subsequently brought low, transmission will resume with the next bit during the subsequent digital computation period. If transmission has not been initiated and completed by the time the next data word is available, $\overline{DRDY}$ will go high for four clock cycles then low again as the new word is loaded into the output register.

A more detailed diagram of the data transmission in the SSC mode is shown in Figure 18. Data bits change on the falling edge of SCLK and are valid on the rising edge of SCLK.

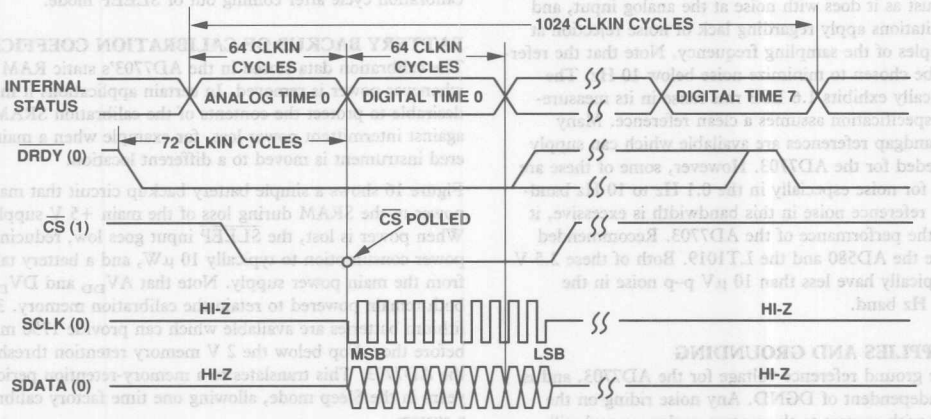


Figure 17. Timing Diagram for SSC Data Transmission Mode

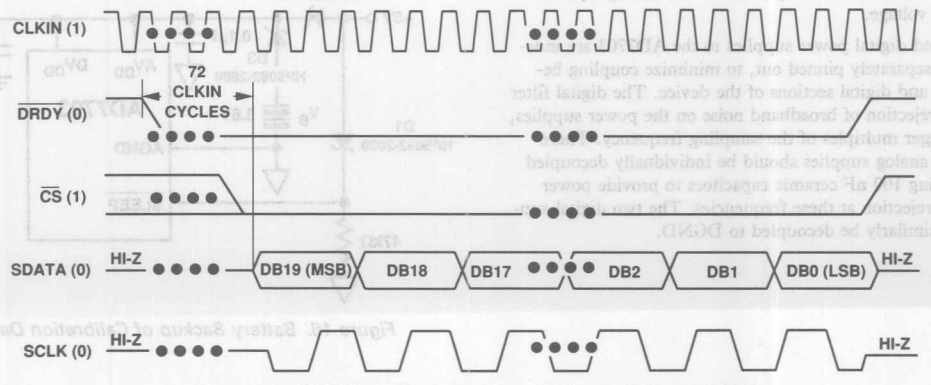


Figure 18. SSC Mode Showing Data Timing Relative to SCLK

SYNCHRONOUS EXTERNAL CLOCK MODE (SEC)

The SEC mode (MODE pin grounded) is designed for direct interface to the synchronous serial ports of industry standard microprocessors such as the 68HC11 and 68HC05. The SEC mode also allows customized interfaces, using I/O port pins, to microprocessors that do not have a direct fit with the AD7703's other mode.

As shown in Figure 19, a falling edge on $\overline{CS}$ enables the serial data output with the MSB initially valid. Subsequent data bits change on the falling edge of an externally supplied SCLK. After the LSB has been transmitted, $\overline{DRDY}$ and SDATA go three-state. If $\overline{CS}$ is low and the AD7703 is still transmitting data when a new data word becomes available, the old data word continues to be transmitted and the new data is lost.

If $\overline{CS}$ is taken high at any time during data transmission, SDATA will go three-state immediately. If $\overline{CS}$ returns low, the AD7703 will continue transmission with the same data bit. If transmission has not been initiated and completed by the time the next data word becomes available, and if $\overline{CS}$ is high, $\overline{DRDY}$ will return high for four clock cycles, then fall as the new word is loaded into the output register.

DIGITAL NOISE AND OUTPUT LOADING

As mentioned earlier, the AD7703 divides its internal timing into two distinct phases, analog sampling and settling and digital computation. In the SSC mode, data is transmitted only during the digital computation periods, to minimize the effects of digital noise on analog performance. In the SEC mode data transmission is externally controlled, so this automatic safeguard does not exist. To compensate, the AD7703 should be synchronized to the digital system clock via CLKIN when used in the SEC mode.

Whatever mode of operation is used, resistive and capacitive loads on digital outputs should be minimized in order to reduce crosstalk between analog and digital portions of the circuit. For this reason connection to low-power CMOS logic such as one of the 4000 series or 74C families is recommended.

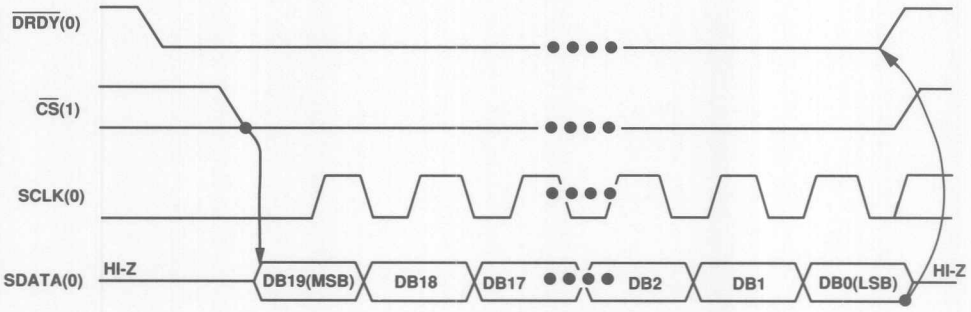
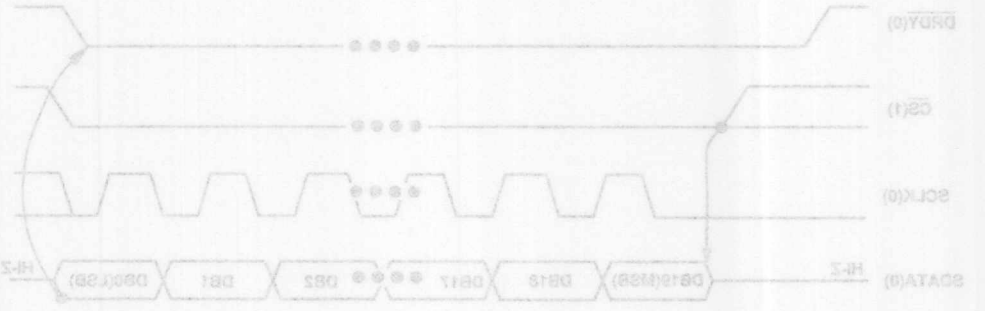


Figure 19. Timing Diagram for the SEC Mode


DRDY(0)
CS(1)
SCL(0)
SDATA(0)
HI-Z
DB15(MSB)
DB14
DB13
DB2
DB1
DB0(LSB)
HI-Z

ANALOG DEVICES

LC²MOS Signal Conditioning ADC

AD7710*

FEATURES

Charge Balancing ADC
- 21 Bits No Missing Codes
- ±0.0015% Nonlinearity

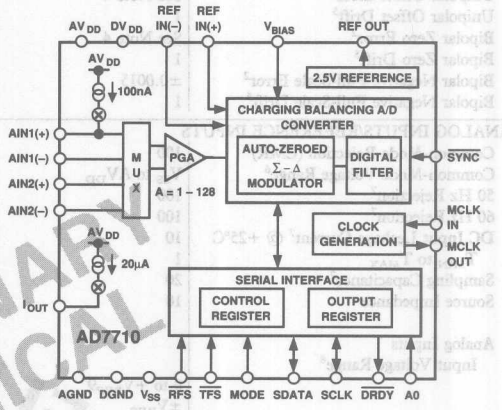
Two-Channel Programmable Gain Front End
- Gains from 1 to 128
- Differential Inputs

Low Pass Filter with Programmable Filter Cutoffs
Ability to Read/Write Calibration Coefficients
Bidirectional Microcontroller Serial Interface
Internal/External Reference Option
Single or Dual Supply Operation
Low Power (25 mW typ) with Power Down Mode (50 μW typ)

APPLICATIONS

Weigh Scales
Thermocouples
Process Control
Smart Transmitters
Chromatography

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7710 is a complete analog front end for low frequency measurement applications. The device accepts low level signals directly from a strain gage or transducer and outputs a serial digital word. It employs a sigma-delta conversion technique to realize up to 21 bits of no missing codes performance. The input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via the on-chip control register allowing adjustment of the filter cutoff and settling time.

The part features two differential analog inputs and a differential reference input. Normally, one of the channels will be used as the main channel with the second channel used as an auxiliary input to periodically measure a second voltage. It can be operated from a single supply (by tying the V_{SS} pin to AGND) provided that the input signals on the analog inputs are more positive than −30 mV. By taking the V_{SS} pin negative, the part can convert signals down to $-V_{REF}$ on its inputs. The AD7710 thus performs all signal conditioning and conversion for a single or dual channel system.

The AD7710 is ideal for use in smart, microcontroller based systems. Input channel selection, gain settings and signal polarity can be configured in software using the bidirectional serial port. The AD7710 contains self-calibration, system calibration and background calibration options and also allows the user to read and write the on-chip calibration registers.

CMOS construction ensures low power dissipation and a software programmable power down mode reduces the standby power consumption to only 50 μW typical. The part is available in a 24-pin, 0.3 inch wide, plastic and hermetic dual-in-line package (DIP) as well as a 24-lead small outline (SOIC) package.

PRODUCT HIGHLIGHTS

1. The programmable gain front end allows the AD7710 to accept input signals directly from a strain gage or transducer, removing a considerable amount of signal conditioning.
2. The AD7710 is ideal for microcontroller or DSP processor applications with an on-chip control register which allows control over filter cutoff, input gain, channel selection, signal polarity and calibration modes.
3. The AD7710 allows the user to read and write the on-chip calibration registers. This means that the microcontroller has much greater control over the calibration procedure.
4. No missing codes ensures true, usable, 21-bit dynamic range coupled with excellent ±0.0015% accuracy. The effects of temperature drift are eliminated by on-chip self-calibration, which removes zero scale and full-scale errors.

*Patent pending.

PRELIMINARY TECHNICAL DATA

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AD7710—SPECIFICATIONS

(AV_{DD} = +5 V to +10 V; DV_{DD} = +5 V; REF OUT = REF IN(+); REF IN(−) = AGND; MCLK IN = 10 MHz unless otherwise stated. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A, S Versions[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	21	Bits min	Guaranteed by Design
Output Noise	See Tables I & II		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity	±0.0015	% of FSR max	Filter Notches ≤ 60 Hz
Positive Full-Scale Error[2, 3]	See Note 4		Excluding Reference
Full-Scale Drift[5]	1	μV/°C max	Excluding Reference
Unipolar Offset Error[2]	See Note 4		
Unipolar Offset Drift[5]	1	μV/°C max	
Bipolar Zero Error[2]	See Note 4		
Bipolar Zero Drift[5]	1	μV/°C max	
Bipolar Negative Full-Scale Error[2]	±0.0015	% of FSR max	Excluding Reference; Typically ±0.0004%
Bipolar Negative Full-Scale Drift[5]	1	μV/°C max	Excluding Reference
ANALOG INPUTS/REFERENCE INPUTS			
Common-Mode Rejection (CMR)	100	dB min	At dc
Common-Mode Voltage Range[6]	V_{SS} to AV_{DD}	V min to V max	
50 Hz Rejection[7]	100	dB min	For Filter Notches of 10 Hz, 25 Hz, 50 Hz, $\pm 0.02 \times f_{NOTCH}$
60 Hz Rejection[7]	100	dB min	For Filter Notches of 10 Hz, 30 Hz, 60 Hz, $\pm 0.02 \times f_{NOTCH}$
DC Input Leakage Current[7] @ +25°C	10	pA max	
T_{MIN} to T_{MAX}	1	nA max	
Sampling Capacitance[7]	20	pF max	
Source Impedance	10	kΩ max	Maximum Allowable Output Impedance of Whatever Is Driving Either Analog Input
Analog Inputs			
Input Voltage Range[8]			For Normal Operation. Depends On Gain Selected
	0 to $+V_{REF}$[9]	max	Unipolar Input Range (B/U Bit of Control Register = 0)
	$\pm V_{REF}$	max	Bipolar Input Range (B/U Bit Of Control Register = 1)
Input Sampling Rate, f_S	See Table III		
Reference Inputs			
REF IN(+) − REF IN (−) Voltage	+2.5 to +5	V min to V max	For Specified Performance
Input Sampling Rate, f_S	$f_{CLK\ IN}/512$		
REFERENCE OUTPUT			
Output Voltage	2.5	V nom	
Initial Tolerance	±1	% max	
Drift	25	ppm/°C typ	
Line Regulation (AV_{DD})	1	mV/V max	
Load Regulation	1	mV/mA max	Maximum Load Current 1 mA
External Current	1	mA max	
V_{BIAS} INPUT			
Input Voltage Range	$AV_{DD} - 0.85 \times V_{REF}$	V max	See V_{BIAS} Input Section
	$V_{SS} + 0.85 \times V_{REF}$	V min	
LOGIC INPUTS			
Input Current	±10	μA max	
All Inputs Except MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	2.0	V min	
MCLK IN Only			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	3.5	V min	

PRELIMINARY TECHNICAL DATA

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Parameter	A, S Versions[1]	Units	Conditions/Comments
LOGIC OUTPUTS			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 100 μA
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[10]	9	pF typ	
TRANSDUCER BURN-OUT			
Current	100	nA nom	
Initial Tolerance	±10	% typ	
Drift	100	ppm/°C typ	
COMPENSATION CURRENT			
Output Current	20	μA max	
Initial Tolerance	±4	μA max	
Drift	40	ppm/°C typ	
Line Regulation (AV_{DD})	20	nA/V max	
Load Regulation	20	nA/V max	
SYSTEM CALIBRATION			
Positive Full-Scale Calibration Limit[11]	(1.05 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Negative Full-Scale Calibration Limit[11]	−(1.05 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Offset Calibration Limit[12]	−(1.05 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Input Span[12]	0.8 × V_{REF}/GAIN	V min	GAIN Is the Selected PGA Gain (Between 1 and 128)
	(2.1 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
POWER REQUIREMENTS			
Power Supply Voltages			
AV_{DD} − V_{SS} Voltage	+5 to +10	V nom	±10% for Specified Performance
DV_{DD} Voltage	+5	V nom	±10% for Specified Performance
Power Supply Currents			
AV_{DD} Current	3	mA max	
DV_{DD} Current	4	mA max	
V_{SS} Current	1.5	mA max	V_{SS} = −5 V
Power Supply Rejection[13]			Rejection w.r.t. AGND; Assumes V_{BIAS} Is Fixed
Positive Supply (AV_{DD})[14]	80	dB typ	
Negative Supply (V_{SS})	90	dB typ	
Power Dissipation			
Normal Mode	40	mW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = 0 V; Typically 25 mW
Normal Mode	45	mW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = −5 V; Typically 30 mW
Standby (Power-Down) Mode	100	μW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = 0 V or −5 V; Typically 50 μW

NOTES

[1]Temperature ranges are as follows: A Version, −40°C to +85°C; S Version −55°C to +125°C.

[2]Applies after calibration at the temperature of interest.

[3]Positive full-scale error applies to both unipolar and bipolar input ranges.

[4]These errors will be of the order of the output noise of the part as shown in Table I.

[5]Recalibration at any temperature or use of the background calibration mode will remove these drift errors. These numbers are guaranteed by design and/or characterization.

[6]This common-mode voltage range is allowed provided that the absolute value of the input voltage does not exceed AV_{DD} +30 mV and V_{SS} −30 mV.

[7]These numbers are guaranteed by design and/or characterization.

[8]The analog inputs present a very high impedance dynamic load which varies with clock frequency and input sample rate. The maximum recommended source resistance is 10 kΩ.

[9]V_{REF} = REF IN(+) − REF IN(−).

[10]Sample tested at +25°C to ensure compliance.

[11]After calibration, if the analog input exceeds positive full scale, the converter will output all 1s. If the analog input is less than negative full scale, then the device will output all 0s.

[12]These calibration and span limits apply provided the absolute voltage on the analog inputs does not exceed V_{DD} or go more negative than V_{SS} − 30 mV. The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.

[13]Measured at dc and applies in the selected passband. PSRR at 50 Hz will exceed 120 dB with filter notches of 10 Hz, 25 Hz or 50 Hz. PSRR at 60 Hz will exceed 120 dB with filter notches of 10 Hz, 30 Hz or 60 Hz.

[14]This number can be improved (to 95 dB typ) by deriving the V_{BIAS} voltage (via Zener diode or reference) from the AV_{DD} supply.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C, unless otherwise noted)

AV_{DD} to V_{SS} . . . . . −0.3 V to +12 V
AV_{DD} to AGND . . . . . −0.3 V to +12 V
AV_{DD} to DGND . . . . . −0.3 V to +12 V
DV_{DD} to AGND . . . . . −0.3 V to +6 V
DV_{DD} to DGND . . . . . −0.3 V to +6 V
V_{SS} to AGND . . . . . +0.3 V to −6 V
V_{SS} to DGND . . . . . +0.3 V to −6 V
AGND to DGND . . . . . −0.3 V to AV_{DD}+0.3 V
Analog Input Voltage to AGND . . V_{SS}−0.3 V to AV_{DD}+0.3 V
Reference Input Voltage to AGND
. . . . . V_{SS}−0.3 V to AV_{DD}+0.3 V
REF OUT to AGND . . . . . −0.3 V to AV_{DD}
Digital Input Voltage to DGND . . . . −0.3 V to DV_{DD}+0.3 V
Digital Output Voltage to DGND . . . −0.3 V to DV_{DD}+0.3 V
Operating Temperature Range
Commercial (A Version) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates Above +75°C . . . . . 6 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



TIMING CHARACTERISTICS[1, 2] (DV_{DD} = +5 V ± 10%; AV_{DD} = +5 V or +10 V ± 10% V_{SS} = 0 V or −5 V ±10%; AGND = DGND = 0 V; $f_{CLK\ IN}$ = 10 MHz; Input Logic 0 = 0 V, Logic 1 = DV_{DD} unless otherwise stated.)

Parameter	Limit at T_{MIN}, T_{MAX} (A, S Versions)	Units	Conditions/Comments
$f_{CLK\ IN}$[3, 4]	400	kHz min	Master Clock Frequency: Internal Gate Oscillator
	12	MHz max	Typically 10 MHz. 10 MHz for Specified Performance
	400	kHz min	Master Clock Frequency: Externally Supplied
	10	MHz max	
$t_{CLK\ IN\ LO}$	0.2 × $t_{CLK\ IN}$	ns min	Master Clock Input Low Time
	0.8 × $t_{CLK\ IN}$	ns max	
$t_{CLK\ IN\ HI}$	0.2 × $t_{CLK\ IN}$	ns min	Master Clock Input High Time
	0.8 × $t_{CLK\ IN}$	ns max	
t_r[5]	50	ns max	Digital Output Rise Time. Typically 20 ns
t_f[5]	50	ns max	Digital Output Fall Time. Typically 20 ns
t_1	1000	ns min	$\overline{SYNC}$ Pulse Width
Self-Clocking Mode			
t_2	4 × $t_{CLK\ IN}$	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Setup Time. $t_{CLK\ IN}$ = 1/$f_{CLK\ IN}$
t_3	4 × $t_{CLK\ IN}$	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Hold Time
t_4	2 × $t_{CLK\ IN}$	ns min	A0 to $\overline{RFS}$ Setup Time
t_5	50	ns min	A0 to $\overline{RFS}$ Hold Time
t_6	4 × $t_{CLK\ IN}$	ns max	$\overline{RFS}$ Low to SCLK Falling Edge
t_7[6]	3 × $t_{CLK\ IN}$	ns max	Data Access Time ($\overline{RFS}$ Low to Data Valid)
t_8[6]	$t_{CLK\ IN}$/2	ns min	SCLK Falling Edge to Data Valid Delay
	$t_{CLK\ IN}$/2 + 20	ns max	
t_9	$t_{CLK\ IN}$/2	ns nom	SCLK High Pulse Width
t_{10}	3 × $t_{CLK\ IN}$/2	ns nom	SCLK Low Pulse Width
t_{11}	10	ns min	$\overline{RFS}$/$\overline{TFS}$ to SCLK Falling Edge Hold Time
	$t_{CLK\ IN}$/2	ns max	
t_{12}	20	ns max	$\overline{RFS}$/$\overline{TFS}$ to SCLK Delay
t_{13}[7]	20	ns max	$\overline{RFS}$ to Data Valid Hold Time
t_{14}	2 × $t_{CLK\ IN}$	ns min	A0 to $\overline{TFS}$ Setup Time
t_{15}	50	ns min	A0 to $\overline{TFS}$ Hold Time
t_{16}	4 × $t_{CLK\ IN}$	ns max	$\overline{TFS}$ to SCLK Falling Edge Delay Time
t_{17}	4 × $t_{CLK\ IN}$	ns min	$\overline{TFS}$ to SCLK Falling Edge Hold Time
t_{18}	20	ns min	Data Valid to SCLK Setup Time
t_{19}	20	ns min	Data Valid to SCLK Hold Time

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Parameter	Limit at T_{MIN}, T_{MAX} (A, S Versions)	Units	Conditions/Comments
External Clocking Mode			
f_{SCLK}	$f_{CLK\ IN}/5$	MHz max	Serial Clock Input Frequency
t_{20}	$4 \times t_{CLK\ IN}$	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Setup Time
t_{21}	$4 \times t_{CLK\ IN}$	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Hold Time
t_{22}	$2 \times t_{CLK\ IN}$	ns min	A0 to $\overline{RFS}$ Setup Time
t_{23}	50	ns min	A0 to $\overline{RFS}$ Hold Time
t_{24}[6]	$3 \times t_{CLK\ IN}$	ns max	Data Access Time ($\overline{RFS}$ Low to Data Valid)
t_{25}[6]	$t_{CLK\ IN}/2$	ns min	SCLK Falling Edge to Data Valid Delay
	$t_{CLK\ IN}/2 + 20$	ns max	
t_{26}	$2 \times t_{CLK\ IN}$	ns min	SCLK High Pulse Width
t_{27}	$2 \times t_{CLK\ IN}$	ns min	SCLK Low Pulse Width
t_{28}	10	ns max	SCLK Falling Edge to $\overline{DRDY}$ High
t_{29}[7]	10	ns min	$\overline{DRDY}$ to Data Valid Hold Time
	20	ns max	
t_{30}	10	ns min	$\overline{RFS}$/$\overline{TFS}$ to SCLK Falling Edge Hold Time
	$t_{CLK\ IN}$	ns max	
t_{31}[7]	20	ns max	$\overline{RFS}$ to Data Valid Hold Time
t_{32}	$2 \times t_{CLK\ IN}$	ns min	A0 to $\overline{TFS}$ Setup Time
t_{33}	50	ns min	A0 to $\overline{TFS}$ Hold Time
t_{34}	10	ns max	SCLK Falling Edge to $\overline{TFS}$ Hold Time
t_{35}	20	ns min	Data Valid to SCLK Setup Time
t_{36}	20	ns min	Data Valid to SCLK Hold Time

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr= tf= 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]See Figures 8 to 11.

[3]CLK IN duty cycle range is 20% to 80%. CLK IN must be supplied whenever the AD7710 is not in STANDBY mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.

[4]The AD7710 is production tested with $f_{CLK\ IN}$ at 10 MHz. It is guaranteed by characterization to operate at 400 kHz.

[5]Specified using 10% and 90% points on waveform of interest.

[6]These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.4 V.

[7]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 100 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

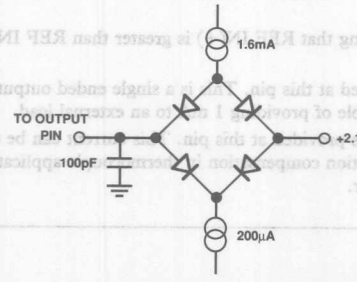
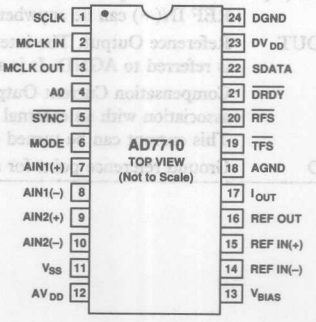


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

PIN CONFIGURATION
DIP and SOIC



PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Function
1	SCLK	Serial Clock. Logic Input/Output depending on the status of the MODE pin. When MODE is high, the device is in its self-clocking mode and the SCLK pin provides a serial clock output. This SCLK becomes active when $\overline{RFS}$ or $\overline{TFS}$ goes low and it goes high impedance when either $\overline{RFS}$ or $\overline{TFS}$ returns high or when the device has completed transmission of an output word. When MODE is low, the device is in its external clocking mode and the SCLK pin acts as an input. This input serial clock can be a continuous clock with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to the AD7710 in smaller batches of data.
2	MCLK IN	Master Clock signal for the device. This can be provided in the form of a crystal or external clock. A crystal can be tied across the MCLK IN and MCLK OUT pins. Alternatively, the MCLK IN pin can be driven with a CMOS compatible clock and MCLK OUT left unconnected. The clock input frequency is nominally 10 MHz.
3	MCLK OUT	When the master clock for the device is a crystal, the crystal is connected between MCLK IN and MCLK OUT.
4	A0	Address Input. With this input low, reading and writing to the device is to the control register. With this input high, access is to either the data register or the calibration registers.
5	$\overline{SYNC}$	Logic Input which allows for synchronization of the digital filters when using a number of AD7710s. It resets the nodes of the digital filter.
6	MODE	Logic Input. When this pin is high, the device is in its self-clocking mode; with this pin low, the device is in its external clocking mode.
7	AIN1(+)	Analog Input Channel 1. Positive input of the programmable gain differential analog input. The AIN1(+) input is connected to an output current source which can be used to check that an external transducer has burnt out or gone open circuit. This output current source can be turned on/off via the control register.
8	AIN1(−)	Analog Input Channel 1. Negative input of the programmable gain differential analog input.
9	AIN2(+)	Analog Input Channel 2. Positive input of the programmable gain differential analog input.
10	AIN2(−)	Analog Input Channel 2. Negative input of the programmable gain differential analog input.
11	V_{SS}	Analog Negative Supply, 0 V to −5 V. Tied to AGND for single supply operation. The input voltage on AIN1 or AIN2 should not go > 30 mV negative w.r.t. V_{SS} for correct operation of the device.
12	AV_{DD}	Analog Positive Supply Voltage, +5 V to +10 V.
13	V_{BIAS}	Input Bias Voltage. This input voltage should be set such that $V_{BIAS} + 0.85 \times V_{REF} < AV_{DD}$ and $V_{BIAS} - 0.85 \times V_{REF} > V_{SS}$ where V_{REF} is REF IN(+)− REF IN(−). Ideally, this should be tied halfway between AV_{DD} and V_{SS}. Thus with AV_{DD}=+5 V and V_{SS}=0 V, it can be tied to REF OUT; with AV_{DD} = +5 V and V_{SS} = −5 V, it can be tied to AGND while with AV_{DD} = +10 V, it can be tied to +5 V or to REF OUT.
14	REF IN (−)	Reference Input. The REF IN(−) can lie anywhere between AV_{DD} and V_{SS} provided REF IN(+) is greater than REF IN(−).
15	REF IN (+)	Reference Input. The reference input is differential providing that REF IN(+) is greater than REF IN(−). REF IN(+) can lie anywhere between AV_{DD} and V_{SS}.
16	REF OUT	Reference Output. The internal +2.5 V reference is provided at this pin. This is a single ended output which is referred to AGND. It is a buffered output which is capable of providing 1 mA to an external load.
17	I_{OUT}	Compensation Current Output. A 20 μA constant current is provided at this pin. This current can be used in association with an external thermistor to provide cold junction compensation in thermocouple applications. This current can be turned on or off via the control register.
18	AGND	Ground reference point for analog circuitry.

PRELIMINARY DATA SHEET

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Pin	Mnemonic	Function
19	$\overline{TFS}$	Transmit Frame Synchronization. Active low logic input used to write serial data to the device with serial data expected after the falling edge of this pulse. In the self-clocking mode, the serial clock becomes active after $\overline{TFS}$ goes low. In the self-clocking mode, $\overline{TFS}$ must go low before the first bit of the data word is written to the part.
20	$\overline{RFS}$	Receive Frame Synchronization. Active low logic input used to access serial data from the device. In the self-clocking mode, the SCLK and SDATA lines both become active after $\overline{RFS}$ goes low. In the external clocking mode, the SDATA line becomes active after $\overline{RFS}$ goes low.
21	$\overline{DRDY}$	Logic output. A falling edge indicates that a new output word is available for transmission. The $\overline{DRDY}$ pin will return high upon completion of transmission of a full output word. $\overline{DRDY}$ is also used to indicate when the AD7710 has completed its on-chip calibration sequence.
22	SDATA	Serial Data. Input /Output with serial data being written to either the control register or the calibration registers and serial data being accessed from the control register, calibration registers or the data register. During a read operation, serial data becomes active after $\overline{RFS}$ goes low. During a write operation, valid serial data is expected on the rising edges of SCLK when $\overline{TFS}$ is low.
23	DV_{DD}	Digital Supply Voltage, +5 V. DV_{DD} should never exceed AV_{DD} by more than 0.3 V. If DV_{DD} powers up before AV_{DD} or if DV_{DD} can exceed AV_{DD} by more than 0.3 V at any other time, a Schottky diode should be placed between the two pins.
24	DGND	Ground reference point for digital circuitry.

TERMINOLOGY

INTEGRAL NONLINEARITY

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and full scale, a point 0.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

POSITIVE FULL-SCALE ERROR

Positive Full-Scale Error is the deviation of the last code transition (111 . . . 110 to 111 . . . 111) from the ideal AIN(+) voltage (AIN(−) + V_{REF}/GAIN −3/2 LSBs). It applies to both unipolar and bipolar analog input ranges.

UNIPOLAR OFFSET ERROR

Unipolar Offset Error is the deviation of the first code transition from the ideal AIN(+) voltage is (AIN(−) + 0.5 LSB) when operating in the unipolar mode.

BIPOLAR ZERO ERROR

This is the deviation of the midscale transition (0111 . . . 111 to 1000 . . . 000) from the ideal AIN(+) voltage (AIN(−) −0.5 LSB) when operating in the bipolar mode.

BIPOLAR NEGATIVE FULL-SCALE ERROR

This is the deviation of the first code transition from the ideal AIN(+) voltage (AIN(−) −V_{REF}/GAIN + 0.5 LSB) when operating in the bipolar mode.

POSITIVE FULL-SCALE OVERRANGE

Positive Full-Scale Overrange is the amount of overhead available to handle input voltages on AIN(+) input greater than AIN(−) +V_{REF}/GAIN (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or overflowing the digital filter.

NEGATIVE FULL-SCALE OVERRANGE

This is the amount of overhead available to handle voltages on AIN(+) below AIN(−) −V_{REF}/GAIN without overloading the analog modulator or overflowing the digital filter. Note that the analog input will accept negative voltage peaks even in the unipolar mode provided that AIN(+) is greater than AIN(−) and greater than V_{SS}−30 mV.

OFFSET CALIBRATION RANGE

In the system calibration modes, the AD7710 calibrates its offset with respect to the analog input. The Offset Calibration Range specification defines the range of voltages that the AD7710 can accept and still calibrate offset accurately.

FULL-SCALE CALIBRATION RANGE

This is the range of voltages that the AD7710 can accept in the system calibration mode and still calibrate full scale correctly.

INPUT SPAN

In system calibration schemes, two voltages applied in sequence to the AD7710's analog input define the analog input range. The input span specification defines the minimum and maximum input voltages from zero to full scale that the AD7710 can accept and still calibrate gain accurately.

PRELIMINARY TECHNICAL DATA

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CONTROL REGISTER (24 BITS)

A write to the device with the A0 input low writes data to the control register. A read to the device with the A0 input low accesses the contents of the control register.

MD2	MD1	MD0	G2	G1	G0	CH	PD	WL	IO	BO	B/U

FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0

Operating Mode

MD2	MD1	MD0	Operating Mode
0	0	0	Normal Mode. This is the normal mode of operation of the device whereby a read to the device with A0 high accesses data from the data register. This is the default condition of these bits after the internal power on reset.
0	0	1	Activate Self-Calibration. This activates self-calibration on the channel selected by CH. This is a one-step calibration sequence, and when complete, the part returns to normal mode. The $\overline{DRDY}$ output indicates when this self-calibration is complete. For this calibration type, the zero scale calibration is done internally on AGND and the full-scale calibration is done internally on V_{REF}.
0	1	0	Activate System Calibration. This activates system calibration on the channel selected by CH. This is a two-step calibration sequence, with the zero scale calibration done first on the selected input channel and $\overline{DRDY}$ indicating when this zero scale calibration is complete. The part returns to normal mode at the end of this first step in the two-step sequence.
0	1	1	Activate System Calibration. This is the second step of the system calibration sequence with full-scale calibration being performed on the selected input channel. Once again, $\overline{DRDY}$ indicates when the full-scale calibration is complete. When this calibration is complete, the part returns to normal mode.
1	0	0	Activate System Offset Calibration. This activates system offset calibration on the channel selected by CH. This is a one-step calibration sequence and, when complete, the part returns to normal mode with $\overline{DRDY}$ indicating when this system offset calibration is complete. For this calibration type, the zero scale calibration is done on the selected input channel and the full-scale calibration is done internally on V_{REF}.
1	0	1	Activate Background Calibration. This activates background calibration on the channel selected by CH. If the background calibration mode is on, then the AD7710 provides continuous self-calibration of the reference and AGND. This calibration takes place as part of the conversion sequence, extending the conversion time and reducing the word rate by a factor of six. Its major advantage is that the user does not have to worry about recalibrating the device when there is a change in the ambient temperature. In this mode, AGND and V_{REF}, as well as the analog input voltage, are continuously monitored and the calibration registers of the device are automatically updated, if necessary.
1	1	0	Read/Write Zero Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the zero scale calibration coefficients of the channel selected by CH. A write to the device with A0 high writes data to the zero scale calibration coefficients of the channel selected by CH. The word length for reading and writing these coefficients is 24 bits, regardless of the status of the WL bit of the control register.
1	1	1	Read/Write Full-Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the full-scale calibration coefficients of the channel selected by CH. A write to the device with A0 high writes data to the full-scale calibration coefficients of the channel selected by CH. The word length for reading and writing these coefficients is 24 bits, regardless of the status of the WL bit of the control register.

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PGA Gain

G2	G1	G0	Gain	
0	0	0	1	(Default Condition After the
0	0	1	2	Internal Power-On Reset)
0	1	0	4	
0	1	1	8	
1	0	0	16	
1	0	1	32	
1	1	0	64	
1	1	1	128	

Channel Selection

CH	Channel	
0	AIN1	(Default Condition After the
1	AIN2	Internal Power-On Reset)

Power-Down

PD		
0	Normal Operation	(Default Condition After the
1	Power-Down	Internal Power-On Reset)

Word Length

WL	Output Word Length	
0	16-Bit	(Default Condition After
1	24-Bit	Internal Power-On Reset)

Output Compensation Current

IO		
0	Off	(Default Condition After
1	On	Internal Power-On Reset)

Burn Out Current

BO		
0	Off	(Default Condition After
1	On	Internal Power-On Reset)

Bipolar/Unipolar Selection (Both Inputs)

B/U		
0	Bipolar	(Default Condition After
1	Unipolar	Internal Power-On Reset)

FILTER SECTION (FS11–FS0)

The on-chip digital filter provides a $Sinc^3$ (or $(Sinx/x)^3$ filter response. The 12 bits of data programmed into these bits determine the filter cutoff frequency, the position of the first notch of the filter and the data rate for the part. In association with the gain selection, it also determines the output noise (and hence the effective resolution) of the device.

The first notch of the filter occurs at a frequency determined by the relationship: filter first notch frequency = $(f_{CLK\ IN}/512)/$ *code* where *code* is the decimal equivalent of the code in bits FS0 to FS11 and is in the range 19 to 2,000. With the nominal $f_{CLK\ IN}$ of 10 MHz, this results in a first notch frequency range from 9.76 Hz to 1.028 kHz. To ensure correct operation of the AD7710, the value of the code loaded to these bits must be within this range. Failure to do this will result in unspecified operation of the device.

Changing the filter notch frequency, as well as the selected gain, impacts resolution. Tables I and II and Figure 2 show the effect of the filter notch frequency and gain on the effective resolution of the AD7710. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 50 Hz, then a new word is available at a 50 Hz rate or every 20 ms. If the first notch is at 1 kHz, a new word is available every 1 ms.

The settling time of the filter to a full-scale step input change is worst case 4× the data rate. For example, with the first filter notch at 50 Hz, the settling time of the filter to a full-scale step input change is 80 ms max. If the first notch is at 1 kHz, the settling time of the filter to a full-scale input step is 4 ms max

The −3 dB frequency is determined by the programmed first notch frequency according to the relationship: filter −3 dB frequency = 0.262 × first notch frequency.

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Table I shows the output rms noise for some typical notch and −3 dB frequencies. The numbers given are for the bipolar input ranges with a V_{REF} of +2.5 V. The numbers in Table I are guaranteed by a combination of testing, characterization and design. The output noise from the part comes from two sources, the quantization noise from the analog-to-digital conversion process and device noise. Device noise is independent of gain and essentially flat across the frequency spectrum. Quantization noise is ratiometric to the input full-scale (and hence gain) and its frequency response is shaped by the modulator.

Looking at the table below, as the cutoff frequency increases the output noise increases because more of the quantization noise of the part comes through to the output and, hence, the output noise increases with increasing −3 dB frequencies. For the lower notch settings, the output noise is dominated by the device noise and, hence, altering the gain has little effect on the output noise. At higher notch frequencies, the quantization noise dominates the output noise and, in this case, the output noise tends to decrease with increasing gain.

Since the output noise comes from two sources, the effective resolution of the device (i.e., the ratio of the output rms noise to the input full scale) does not remain constant with increasing gain or with increasing bandwidth. Table II shows the same table as Table I except that the output is now expressed in terms of effective resolution (the magnitude of the rms noise with respect to 2 × V_{REF}/GAIN, i.e., the input full scale). It is possible to do post filtering on the device to improve the output data rate for a given −3 dB frequency and also to further reduce the output noise (see Digital Filtering section).

Table I. Output Noise vs. Gain and First Notch Frequency

First Notch of Filter and O/P Data Rate[1]	Output RMS Noise (μV) −3 dB Frequency	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
10 Hz[2]	2.62 Hz	1.7	0.84	0.60	0.42	0.42	0.42	0.42	0.42
25Hz[2]	6.55 Hz	3.4	1.7	1.2	0.60	0.60	0.60	0.60	0.60
30 Hz[2]	7.86 Hz	3.4	2.4	1.2	0.84	0.84	0.60	0.60	0.60
50 Hz[2]	13.1 Hz	9.5	4.8	2.4	1.7	1.2	0.84	0.84	0.84
60 Hz[2]	15.72 Hz	13.5	6.7	3.4	1.7	1.2	1.2	0.84	0.84
100 Hz[3]	26.2 Hz	54	27	13.5	6.7	3.4	1.7	1.7	1.2
250 Hz[3]	65.5 Hz	432	216	108	54	27	13.5	6.7	4.8
500 Hz[3]	131 Hz	2.4 × 10^3	1.2 × 10^3	610	305	153	76	38	19
1 kHz[3]	262 Hz	13.8 × 10^3	6.9 × 10^3	3.4 × 10^3	1.7 × 10^3	863	432	216	108

NOTES
[1]The default condition (after the internal power-on reset) for the first notch of filter is 60 Hz.
[2]For these filter notch frequencies, the output rms noise is primarily independent of the value of the reference voltage. Therefore, increasing the reference voltage will give an increase in the effective resolution of the device (i.e., the ratio of the rms noise to the input full scale is increased since the output rms noise remains constant as the input full-scale increases).
[3]For these filter notch frequencies, the output rms noise is proportional to the value of the reference voltage.

Table II. Effective Resolution vs. Gain and First Notch Frequency

First Notch of Filter and O/P Data Rate[1]	Effective Resolution[1] (Bits) −3 dB Frequency	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
10 Hz	2.62 Hz	21.5	21.5	21	20.5	19.5	18.5	17.5	16.5
25 Hz	6.55 Hz	20.5	20.5	20	20	19	18	17	16
30 Hz	7.86 Hz	20.5	20	20	19.5	18.5	18	17	16
50 Hz	13.1 Hz	19	19	19	18.5	18	17.5	16.5	15.5
60 Hz	15.72 Hz	18.5	18.5	18.5	18.5	18	17	16.5	15.5
100 Hz	26.2 Hz	16.5	16.5	16.5	16.5	16.5	16.5	15.5	15
250 Hz	65.5 Hz	13.5	13.5	13.5	13.5	13.5	13.5	13.5	13
500 Hz	131 Hz	11	11	11	11	11	11	11	11
1 kHz	262 Hz	8.5	8.5	8.5	8.5	8.5	8.5	8.5	8.5

NOTE
[1]Effective resolution is defined as the magnitude of the output rms noise to the input full scale (i.e., 2 × V_{REF}/GAIN). The above table applies for a V_{REF} of +2.5 V and resolution numbers are rounded to the nearest 0.5 LSB.

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Figure 2 gives similar information to that outlined in Table I. In this plot, the output rms noise is shown for the full range of available cutoff frequencies rather than for some typical cutoff frequencies as in Tables I and II. The numbers given in this plot are typical values.

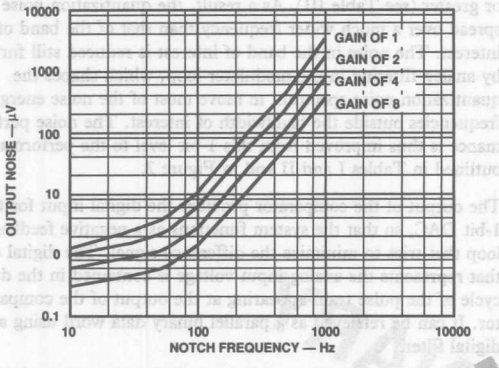


Figure 2a. Plot of Output Noise vs. Gain and Notch Frequency (Gains of 1 to 8)

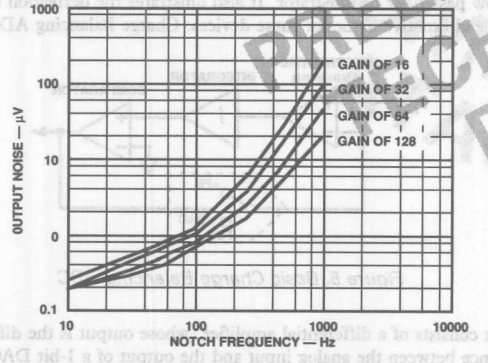


Figure 2b. Plot of Output Noise vs. Gain and Notch Frequency (Gains of 16 to 128)

CIRCUIT DESCRIPTION

The AD7710 is a sigma-delta A/D converter with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals such as those in weigh scale, industrial control or process control applications. It contains a sigma-delta (or charge balancing) ADC, a calibration microcontroller with on-chip static RAM, a clock oscillator, a digital filter and a bidirectional serial communications port.

The part contains two programmable gain differential analog input channels. The gain range is from 1 to 128 allowing the part to accept unipolar signals of between 0 to +20 mV and 0 to +2.5 V or bipolar signals in the range from ±20 mV to ±2.5 V when the reference input voltage equals +2.5 V. The input signal to the selected analog input channel is continuously sampled at a rate determined by the frequency of the master clock, CLK IN, and the selected gain (see Table III). A charge balancing A/D converter (Sigma-Delta Modulator) converts the sampled signal into a digital pulse train whose duty cycle contains the digital information. The programmable gain function on the analog input is also incorporated in this sigma-delta modulator with the input sampling frequency being modified to give the higher gains. A sinc^3 digital low pass filter processes the output of the sigma-delta modulator and updates the output register at a rate determined by the first notch frequency of this filter. The output data can be read from the serial port randomly or periodically at any rate up to the output register update rate. The first notch of this digital filter (and hence its −3 dB frequency) can be programmed via an on-chip control register. The programmable range for this first notch frequency is from 9.76 Hz to 1.028 kHz, giving a programmable range for the −3 dB frequency of 2.58 Hz to 269 Hz.

The basic connection diagram for the part is shown in Figure 3. This shows the AD7710 in the external clocking mode with both the AV_{DD} and DV_{DD} pins of the AD7710 being driven from the analog +5 V supply. Some applications will have separate supplies for both AV_{DD} and DV_{DD} and, in some of these cases, the analog supply will exceed the +5 V digital supply (see Power Supplies and Grounding section).

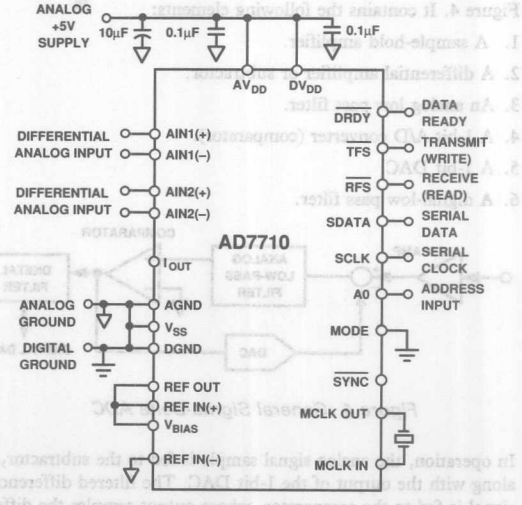


Figure 3. Basic Connection Diagram

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The AD7710 provides a number of calibration options which can be programmed via the on-chip control register. A calibration cycle may be initiated at any time by writing to this control register. The part can perform self-calibration using the on-chip calibration microcontroller and SRAM to store calibration parameters. Other system components may also be included in the calibration loop to remove offset and gain errors in the input channel using the system calibration mode. Another option is a background calibration mode where the part continuously performs self-calibration and updates the calibration coefficients. Once the part is in this mode, the user does not have to worry about issuing periodic calibration commands to the device or ask the device to recalibrate when there is a change in the ambient temperature or power supply voltage.

The AD7710 gives the user access to the on-chip calibration registers allowing the microprocessor to read the device's calibration coefficients and also to write its own calibration coefficients to the part. This gives the microprocessor much greater control over the AD7710's calibration procedure. It also means that the user can verify that the device has performed its calibration correctly by comparing the coefficients after calibration with prestored values in E^2PROM.

The AD7710 can be operated in single supply systems provided that the analog input voltage does not go more negative than 30 mV. For larger bipolar signals, a V_{SS} of −5 V is required by the part. For battery operation, the AD7710 also offers a software programmable standby mode that reduces idle power consumption to typically 50 μW.

THEORY OF OPERATION

The general block diagram of a sigma-delta ADC is shown in Figure 4. It contains the following elements:

1. A sample-hold amplifier.
2. A differential amplifier or subtractor.
3. An analog low pass filter.
4. A 1-bit A/D converter (comparator).
5. A 1-bit DAC.
6. A digital-low pass filter.

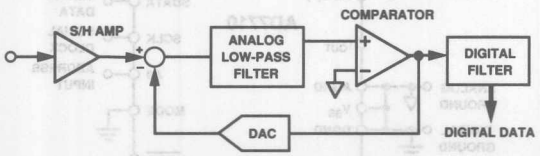


Figure 4. General Sigma-Delta ADC

In operation, the analog signal sample is fed to the subtractor, along with the output of the 1-bit DAC. The filtered difference signal is fed to the comparator, whose output samples the difference signal at a frequency many times that of the analog signal sampling frequency (oversampling).

Oversampling is fundamental to the operation of sigma-delta ADCs. Using the quantization noise formula for an ADC:

$$SNR = (6.02 \times number\ of\ bits + 1.76)\ dB,$$

a 1-bit ADC or comparator yields an SNR of 7.78 dB.

The AD7710 samples the input signal at a frequency of 20 kHz or greater (see Table III). As a result, the quantization noise is spread over a much wider frequency than that of the band of interest. The noise in the band of interest is reduced still further by analog filtering in the modulator loop, which shapes the quantization noise spectrum to move most of the noise energy to frequencies outside the bandwidth of interest. The noise performance is thus improved from this 1-bit level to the performance outlined in Tables I and II and in Figure 2.

The output of the comparator provides the digital input for the 1-bit DAC, so that the system functions as a negative feedback loop that tries to minimize the difference signal. The digital data that represents the analog input voltage is contained in the duty cycle of the pulse train appearing at the output of the comparator. It can be retrieved as a parallel binary data word using a digital filter.

Sigma-delta ADCs are generally described by the order of the analog low pass filter. A simple example of a first order sigma-delta ADC is shown in Figure 5. This contains only a first order low pass filter or integrator. It also illustrates the derivation of the alternative name for these devices: Charge Balancing ADCs.

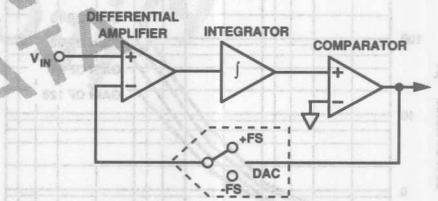


Figure 5. Basic Charge Balancing ADC

It consists of a differential amplifier (whose output is the difference between the analog input and the output of a 1-bit DAC), an integrator and a comparator. The term, charge balancing, comes from the fact that this system is a negative feedback loop that tries to keep the nett charge on the integrator capacitor at zero, by balancing charge injected by the input voltage with charge injected by the 1-bit DAC. When the analog input is zero, the only contribution to the integrator output comes from the 1-bit DAC. For the nett charge on the integrator capacitor to be zero, the DAC output must spend half its time at +FS and half its time at −FS. Assuming ideal components, the duty cycle of the comparator will be 50%.

When a positive analog input is applied, the output of the 1-bit DAC must spend a larger proportion of the time at +FS, so the duty cycle of the comparator increases. When a negative input voltage is applied, the duty cycle decreases.

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digital filter that provides a rolling average of the sampled output. After power up or if there is a step change in the input voltage, there is a settling time that must elapse before valid data is obtained.

Input Sample Rate

The modulator sample frequency for the device remains at $f_{CLK\ IN}/512$ (20 kHz @ $f_{CLK\ IN}$ = 10 MHz) regardless of the selected gain. However, gains greater than ×1 are achieved by a combination of multiple input samples per modulator cycle and a scaling of the ratio of reference capacitor to input capacitor. As a result of the multiple sampling, the input sample rate of the device varies with the selected gain (see Table III). The effective input impedance is $1/C \cdot f_S$ where C is the input sampling capacitance and f_S is the input sample rate.

Table III. Input Sampling Frequency vs. Gain

Gain	Input Sampling Frequency (f_S)
1	$f_{CLK\ IN}/512$ (20 kHz @ $f_{CLK\ IN}$ = 10 MHz)
2	$2 \times f_{CLK\ IN}/512$ (40 kHz @ $f_{CLK\ IN}$ = 10 MHz)
4	$4 \times f_{CLK\ IN}/512$ (80 kHz @ $f_{CLK\ IN}$ = 10 MHz)
8	$4 \times f_{CLK\ IN}/512$ (160 kHz @ $f_{CLK\ IN}$ = 10 MHz)
16	$4 \times f_{CLK\ IN}/512$ (160 kHz @ $f_{CLK\ IN}$ = 10 MHz)
32	$4 \times f_{CLK\ IN}/512$ (160 kHz @ $f_{CLK\ IN}$ = 10 MHz)
64	$4 \times f_{CLK\ IN}/512$ (160 kHz @ $f_{CLK\ IN}$ = 10 MHz)
128	$4 \times f_{CLK\ IN}/512$ (160 kHz @ $f_{CLK\ IN}$ = 10 MHz)

DIGITAL FILTERING

The AD7710's digital filter behaves like a similar analog filter, with a few minor differences.

First, since digital filtering occurs after the A-to-D conversion process, it can remove noise injected during the conversion process. Analog filtering cannot do this.

On the other hand, analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. Digital filtering cannot do this and noise peaks riding on signals near full scale have the potential to saturate the analog modulator and digital filter, even though the average value of the signal is within limits. To alleviate this problem, the AD7710 has overrange headroom built into the sigma-delta modulator and digital filter which allows overrange excursions of 5% above the analog input range. If noise signals are larger than this, consideration should be given to analog input filtering, or to reducing the input channel voltage so that its full scale is half that of the analog input channel full scale. This will provide an overrange capability greater than 100% at the expense of reducing the dynamic range by 1 bit (50%).

Filter Characteristics

The cutoff frequency of the digital filter is determined by the value loaded to bits FS0 to FS11 in the control register. At the maximum clock frequency of 10 MHz, the minimum cutoff frequency of the filter is 2.58 Hz while the maximum programmable cutoff frequency is 269 Hz.

quency of 2.62 Hz which corresponds to a first filter notch frequency of 10 Hz. This is a $(\sin x/x)^3$ response (also called sinc^3) that provides >100 dB of 50 Hz and 60 Hz rejection. Programming a different cutoff frequency via FS0–FS11 does not alter the profile of the filter response, it changes the frequency of the notches as outlined in the Control Register section.

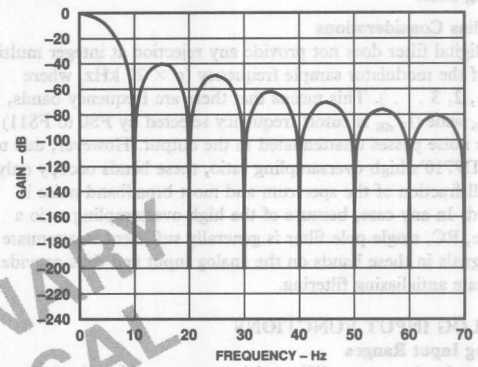


Figure 6. Frequency Response of AD7710 Filter

Post Filtering

The on-chip modulator provides samples at a 20 kHz output rate. The on-chip digital filter decimates these samples to provide data at an output rate which corresponds to the programmed first notch frequency of the filter. Since the output data rate exceeds the Nyquist criterion, the output rate for a given bandwidth will satisfy most application requirements. However, there may be some applications which require a higher data rate for a given bandwidth and noise performance. Applications which need this higher data rate will require some post filtering following the digital filter of the AD7710.

For example, if the required bandwidth is 7.86 Hz but the required update rate is 100 Hz, the data can be taken from the AD7710 at the 100 Hz rate giving a −3 dB bandwidth of 26.2 Hz. Post filtering can be applied to this to reduce the bandwidth and output noise, to the 7.86 Hz bandwidth level, while maintaining an output rate of 100 Hz.

Since the AD7710 contains this on-chip, low pass filtering, there is a settling time associated with step function inputs, and data on the output will be invalid after a step change until the settling time has elapsed. The settling time depends upon the notch frequency chosen for the filter. The output data rate equates to this filter notch frequency and the settling time of the filter to a full-scale step input is 4 times the output data period. In applications using both input channels, the settling time of the filter must be allowed to elapse before data from the second channel is accessed.

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Post filtering can also be used to reduce the output noise from the device for bandwidths below 2.62 Hz. At a gain of 128, the output rms noise is 420 nV. This is essentially device noise or white noise, and since the input is chopped, the noise has a flat frequency response. By reducing the bandwidth below 2.62 Hz, the noise in the resultant passband can be reduced. A reduction in bandwidth by a factor of 2 results in a $\sqrt{2}$ reduction in the output rms noise. This additional filtering will result in a longer settling time.

Antialias Considerations

The digital filter does not provide any rejection at integer multiples of the modulator sample frequency (n × 20 kHz, where n = 1, 2, 3 . . .). This means that there are frequency bands, $\pm f_{3\ dB}$ wide ($f_{3\ dB}$ is cutoff frequency selected by FS0 to FS11) where noise passes unattenuated to the output. However, due to the AD7710's high oversampling ratio, these bands occupy only a small fraction of the spectrum and most broadband noise is filtered. In any case, because of the high oversampling ratio a simple, RC, single pole filter is generally sufficient to attenuate the signals in these bands on the analog input and thus provide adequate antialiasing filtering.

ANALOG INPUT FUNCTIONS

Analog Input Ranges

Both analog inputs are differential, programmable gain, input channels which can handle either unipolar or bipolar input signals. The common-mode range of these inputs is from V_{SS} to AV_{DD} provided that the absolute value of the analog input voltage lies between V_{SS}−30 mV and AV_{DD}+30 mV.

The input sample rate for the part varies as per Table III and the input sampling capacitance is 15 pF typical. The effective input impedance is $1/C \cdot f_S$ and this results in a maximum allowable source impedance of whatever is driving the analog input of 10 kΩ to ensure correct charging of the sampling capacitor.

The dc input leakage current is 10 pA maximum at +25°C. This results in a dc offset voltage developed across the source impedance. However, this dc offset effect can be compensated for by a combination of the differential input capability of the part and its system calibration mode.

Burn-Out Current

The AIN1(+) input of the AD7710 contains a 100 nA current source which can be turned on/off via the control register. This current source can be used in checking that a transducer has not burnt out or gone open circuit before attempting to take measurements on that channel. If the current is turned on and allowed flow into the transducer and a measurement of the input voltage on the AIN1 input is taken, it can indicate that the transducer is not functioning correctly. For normal operation, this burn-out current is turned off by writing a 0 to the BO bit in the control register.

Output Compensation Current

The AD7710 also contains a feature which can enable the user to implement cold junction compensation in thermocouple applications. This can be achieved using the output compensation current from the I_{OUT} pin of the device. Once again, this current can be turned on/off via the control register. Writing a 1 to the IO bit of the control register enables this compensation current.

The compensation current provides a 20 μA constant current source which can be used in association with a thermistor or a diode to provide cold junction compensation. A common method of generating cold junction compensation is to use a temperature dependent current flowing through a fixed resistor to provide a voltage that is equal to the voltage developed across the cold junction at any temperature in the expected ambient range. In this case, the temperature coefficient of the compensation current is so low compared with the temperature coefficient of the thermistor that it can be considered constant with temperature. The temperature variation is then provided by the variation of the thermistor's resistance with temperature.

Bipolar/Unipolar Inputs

The two analog inputs on the AD7710 can accept either unipolar or bipolar input voltage ranges. Bipolar or unipolar options are chosen by programming the B/U bit of the control register. This programs both channels for either unipolar or bipolar operation. Programming the part for either unipolar or bipolar operation does not change any of the input signal conditioning; it simply changes the data output coding.

The input channels are differential and, as a result, the voltage to which the unipolar and bipolar signals are referenced is the voltage on the AIN(−) input. For example, if AIN(−) is +1.25 V and the AD7710 is configured for unipolar operation with a gain of 1 and a V_{REF} of +2.5 V, the input voltage range on the AIN(+) input is +1.25 V to +3.75 V. If AIN(−) is +1.25 V and the AD7710 is configured for bipolar mode with a gain of 1 and a V_{REF} of +2.5 V, the analog input range on the AIN(+) input is −1.25 V to +3.75 V.

REFERENCE INPUT/OUTPUT

The AD7710 contains a temperature compensated +2.5 V reference which has an initial tolerance of ±25 mV. This reference voltage is provided at the REF OUT pin and it can be used as the reference voltage for the part by connecting the REF OUT pin to the REF IN(+) pin. This REF OUT pin is a single-ended output, referenced to AGND, which is capable of providing up to 1 mA to an external load. In applications where REF OUT is connected directly to REF IN(+), REF IN(−) should be tied to AGND to provide the nominal +2.5 V reference for the AD7710.

The reference inputs of the AD7710, REF IN(+) and REF IN(−), provide a differential reference input capability. The common-mode range for these differential inputs is from V_{SS} to AV_{DD}. The nominal differential voltage, V_{REF} (REF IN(+) −REF IN(−)), is +2.5 V for specified operation, but the reference voltage can go to +5 V with no degradation in performance provided that the absolute value of REF IN(+) and REF IN(−) does not exceed its AV_{DD} and V_{SS} limits. REF IN(+) must always be greater than REF IN(−) for correct operation of the AD7710.

Both reference inputs provide a high impedance, dynamic load similar to the analog inputs. The maximum dc input leakage current is 10 pA (±1 μA over temperature) and source resistances will result in gain errors on the part. The reference inputs are switched capacitor inputs with the input capacitance dependent upon the selected gain. For gains of 1 to 8 the input capacitance is 20 pF; for a gain of 16 it is 10 pF; for a gain of 32 it is 5 pF; for a gain of 64 it is 2.5 pF; and for a gain of 128 it is 1.25 pF.

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The digital filter of the AD7710 removes noise from the reference input just as it does with the analog input, and the same limitations apply regarding lack of noise rejection at integer multiples of the sampling frequency. The output noise performance outlined in Tables I and II assumes a clean reference. If the reference noise in the bandwidth of interest is excessive, it can degrade the performance of the AD7710. Figure 7 shows the noise performance of the AD7710's on-board reference.

Figure 7. AD7710 Reference Output Noise

V_{BIAS} Input

The V_{BIAS} input determines at what voltage the internal analog circuitry is biased. It essentially provides the return path for analog currents flowing in the modulator and, as such, it should be driven from a low impedance point to minimize errors.

For maximum internal headroom, the V_{BIAS} voltage should be set halfway between AV_{DD} and V_{SS}. The difference between AV_{DD} and (V_{BIAS} + 0.85 × V_{REF}) determines the amount of headroom the circuit has at the upper end, while the difference between V_{SS} and (V_{BIAS} −0.85 × V_{REF}) determines the amount of headroom the circuit has at the lower end. Care should be taken in choosing a V_{BIAS} voltage to ensure that V_{BIAS} ±0.85 × V_{REF} does not exceed the AV_{DD} and V_{SS} limits. For example, with AV_{DD} = +4.75 V, V_{SS} = 0 V and V_{REF} = +2.5 V, the allowable range for the V_{BIAS} voltage is +2.125 V to +2.625 V. With AV_{DD} = +9.5 V, V_{SS} = 0 V and V_{REF} = +5 V, the range for V_{BIAS} is +4.25 V to +5.25 V. With AV_{DD} = +4.75 V, V_{SS} = −4.75 V and V_{REF} = +2.5 V, the V_{BIAS} range is −2.625 V to +2.625 V.

USING THE AD7710

SYSTEM DESIGN CONSIDERATIONS

The AD7710 operates differently from successive approximation ADCs or integrating ADCs. Since it samples the signal continuously, like a tracking ADC, there is no need for a start convert command. The output register is updated at a rate determined by the first notch of the filter and the output can be read at any time, either synchronously or asynchronously.

Clocking

The AD7710 requires a master clock input, which may be an external TTL/CMOS compatible clock signal applied to the MCLK IN pin with the MCLK OUT pin left unconnected. Alternatively, a crystal of the correct frequency can be connected between MCLK IN and MCLK OUT, in which case the clock circuit will function as a crystal controlled oscillator. For lower clock frequencies, a ceramic resonator may be used instead of the crystal. For these lower frequency oscillators, external capacitors may be required on either the ceramic resonator or on the crystal.

The input sampling frequency, the modulator sampling frequency, the −3 dB frequency, output update rate and calibration time are all directly related to the master clock frequency, $f_{CLK\ IN}$. Reducing the master clock frequency by a factor of 2 will halve the above frequencies and update rate and will double the calibration time.

The current drawn from the DV_{DD} power supply is also directly related to $f_{CLK\ IN}$. Reducing $f_{CLK\ IN}$ by a factor of 2 will halve the DV_{DD} current but will not affect the current drawn from the AV_{DD} power supply.

System Synchronization

If multiple AD7710s are operated from a common master clock, they can be synchronized to update their output registers simultaneously. A falling edge on the $\overline{SYNC}$ input resets the filter and places the AD7710 into a consistent, known state. A common signal to the AD7710s' $\overline{SYNC}$ inputs will synchronize their operation. This would normally be done after each AD7710 has performed its own calibration or has had calibration coefficients loaded to it.

ACCURACY

Sigma-delta ADCs, like VFCs and other integrating ADCs, do not contain any source of nonmonotonicity and inherently offer no missing codes performance. The AD7710 achieves excellent linearity by the use of high quality, on-chip silicon dioxide capacitors, which have a very low capacitance/voltage coefficient. The device also achieves low input drift through the use of chopper stabilized techniques in its input stage. To ensure excellent performance over time and temperature, the AD7710 uses digital calibration techniques which minimize offset and gain error.

Autocalibration

Autocalibration on the AD7710 removes offset and gain errors from the device. A calibration routine should be initiated on the device whenever there is a change in the ambient operating temperature or supply voltage. It should also be initiated if there is a change in the selected channel, gain, filter notch or bipolar/unipolar input range. However, if the AD7710 is in its background calibration mode, the above changes are all automatically taken care of (after the settling time of the filter has been allowed for).

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modulator output for two different input conditions. These are "zero scale" and "full-scale" points. With these readings, the microcontroller can calculate the gain slope for the input to output transfer function of the converter. Internally, the part works with a resolution of 33 bits to determine its conversion result of either 16 bits or 24 bits.

Self-Calibration

In the self-calibration mode with a unipolar input range, the zero scale point used in determining the calibration coefficients is AGND and the full-scale point is V_{REF}. The zero scale coefficient is determined by converting an internal AGND node. The full-scale coefficient is determined from the span between this AGND conversion and a conversion on an internal V_{REF} node. The self-calibration mode is invoked by writing the appropriate values (0, 0, 1) to the MD2, MD1 and MD0 bits of the control register. In this calibration mode, the AGND node is switched in to the modulator first and a conversion is performed; the V_{REF} node is then switched in and another conversion is performed. When the calibration sequence is complete, the calibration coefficients updated and the filter resettled to the analog input voltage, the $\overline{DRDY}$ output goes low.

For bipolar input ranges in the self-calibrating mode, the sequence is very similar to that just outlined. In this case, the two points which the AD7710 calibrates are midscale (bipolar zero) and positive full scale.

System Calibration

System calibration allows the AD7710 to compensate for system gain and offset errors as well as its own internal errors. System calibration performs the same slope factor calculations as self-calibration but uses voltage values presented by the system to the AIN inputs for the zero and full-scale points. System calibration is a two-step process. The zero scale point must be presented to the converter first. It must be applied to the converter before the calibration step is initiated and remain stable until the step is complete. System calibration is initiated by writing the appropriate values (0, 1, 0) to the MD2, MD1 and MD0 bits of the control register. The $\overline{DRDY}$ output from the device will signal when the step is complete by going low. After the zero scale point is calibrated, the full-scale point is applied and the second step of the calibration process is initiated by again writing the appropriate values (0, 1, 1) to MD2, MD1 and MD0. Again the full-scale voltage must be set up before the calibration is initiated and it must remain stable throughout the calibration step. $\overline{DRDY}$ goes low at the end of this second step to indicate that the system calibration is complete. In the unipolar mode, the system calibration is performed between the two endpoints of the transfer function; in the bipolar mode, it is performed between midscale and positive full scale.

This two-step system calibration mode offers another feature. After the sequence has been completed, additional offset calibrations can be performed by themselves to adjust the zero reference point to a new system zero reference value. This is achieved by performing the first step of the system calibration sequence (by writing 0, 1, 0 to MD2, MD1, MD0). This will adjust the zero scale or offset point but will not change the slope factor from what was set during a full system calibration sequence.

[illegible] the system is presented to the AIN input of the converter. System offset calibration is initiated by writing 1, 0, 0 to MD2, MD1, MD0. The system zero scale coefficient is determined by converting the voltage applied to the AIN input while the full-scale coefficient is determined from the span between this AIN conversion and a conversion on an internal V_{REF} node. The zero scale point should be applied to the AIN input for the duration of the calibration sequence. This is a one-step calibration sequence with $\overline{DRDY}$ going low when the sequence is completed. In the unipolar mode, the system offset calibration is performed between the two endpoints of the transfer function; in the bipolar mode, it is performed between midscale and positive full scale.

Background Calibration

The AD7710 also offers a background calibration mode where the part interleaves its calibration procedure with its normal conversion sequence. In the background calibration mode, the same nodes are used as the calibration points as are used in the self-calibration mode, i.e., AGND and V_{REF}. The background calibration mode is invoked by writing 1, 0, 1 to MD2, MD1, MD0 of the control register. When invoked, the background calibration mode reduces the output data rate of the AD7710 by a factor of six. Its advantage is that the part is continually performing calibration and automatically updating its calibration coefficients. As a result, the effects of temperature drift, supply sensitivity and time drift on zero and full-scale errors are automatically removed. When the background calibration mode is turned on, the part will remain in this mode until bits MD2, MD1 and MD0 of the control register are changed.

Table IV summarizes the calibration modes and the calibration points associated with them.

Span and Offset Limits

Whenever a system calibration mode is used, there are limits on the amount of offset and span which can be accommodated. The range of input span in both the unipolar and bipolar modes has a minimum value of $0.8 \times V_{REF}/GAIN$ and a maximum value of $2.1 \times V_{REF}/GAIN$.

The amount of offset which can be accommodated depends on whether the unipolar or bipolar mode is being used. In unipolar mode, the system calibration modes can handle a maximum offset of $0.25 \times V_{REF}/GAIN$ and a minimum offset of $-(1.05 \times V_{REF}/GAIN)$. This offset range is limited by the requirement that the positive full-scale calibration limit is $\leq 1.05 \times V_{REF}/GAIN$. Thus, the maximum offset ($0.25 \times V_{REF}/GAIN$) plus the minimum span ($0.8 \times V_{REF}/GAIN$) cannot exceed $1.05 \times V_{REF}/GAIN$.

In the bipolar mode, the system offset calibration range is restricted to $\pm 0.65 \times V_{REF}/GAIN$. The span range of the converter in bipolar mode is equidistant around the voltage used for the zero scale point. Therefore, the maximum offset $\pm(0.65 \times V_{REF}/GAIN)$ plus half the minimum span $\pm(0.4 \times V_{REF}/GAIN)$ must be less than $\pm(1.05 \times V_{REF}/GAIN)$. If the span is set to $2 \times V_{REF}/GAIN$, the offset span cannot move more than $\pm(0.05 \times V_{REF}/GAIN)$ before the endpoints of the transfer function exceed the input overrange limits $\pm(1.05 \times V_{REF}/GAIN)$.

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Cal Type	MD2, MD1, MD0	Zero Scale Cal	Full-Scale Cal	Sequence
Self-Cal	0, 0, 1	AGND	V_{REF}	One Step
System Cal	0, 1, 0	AIN		Two Step
System Cal	0, 1, 1		AIN	Two Step
System Offset Cal	1, 0, 0	AIN	V_{REF}	One Step
Background Cal	1, 0, 1	AGND	V_{REF}	One Step

POWER-UP AND CALIBRATION

On power-up, the AD7710 performs an internal reset which sets the contents of the control register to a known state. However, to ensure correct calibration for the device, a calibration routine should be performed after power-up.

The power dissipation and temperature drift of the AD7710 are low and no warm up time is required before the initial calibration is performed. However, if an external reference is being used, this reference must have stabilized before calibration is initiated.

Drift Considerations

The AD7710 uses chopper stabilization techniques to minimize input offset drift. Charge injection in the analog switches and dc leakage currents at the sampling node are the primary sources of offset voltage drift in the converter. The dc input leakage current is essentially independent of the selected gain but charge injection effects will increase with increasing gain. As a result, the offset drift numbers will be slightly larger for higher gains. Gain drift within the converter depends primarily upon the temperature tracking of the internal capacitors. It is not affected by leakage currents.

Measurement errors due to offset drift or gain drift can be eliminated at any time by recalibrating the converter or by operating the part in the background calibration mode. Using the system calibration mode can also minimize offset and gain errors in the signal conditioning circuitry. Integral and differential linearity errors are not significantly affected by temperature changes.

POWER SUPPLIES AND GROUNDING

Since the analog inputs and reference input are differential, most of the voltages in the analog modulator are common-mode voltages. V_{BIAS} provides the return path for most of the analog currents flowing in the analog modulator. As a result, the V_{BIAS} input should be driven from a low impedance to minimize errors due to charging/discharging impedances on this line. When the internal reference is used as the reference source for the part, AGND is the ground return for this reference voltage.

The analog and digital supplies to the AD7710 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The digital filter will provide rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. The digital supply (DV_{DD}) must never exceed the analog positive supply (AV_{DD}) by more than 0.3V. Power supply sequencing, therefore, is important. If separate analog and digital supplies are used, care must be taken to ensure that the analog supply is powered up first. If this cannot be ensured, or if DV_{DD} can exceed AV_{DD} at any other time, a Schottky diode should be placed between DV_{DD} and AV_{DD}.

DIGITAL INTERFACE

The AD7710's serial communications port provides a flexible arrangement to allow easy interfacing to industry standard microprocessors, microcontrollers and digital signal processors. A serial read to the AD7710 can access data from the output register, the control register or from the calibration registers. A serial write to the AD7710 can write data to the control register or the calibration registers.

Two different modes of operation are available, optimized for different types of interface where the AD7710 can act either as master in the system (it provides the serial clock) or as slave (an external serial clock can be provided to the AD7710). These two modes, labelled self clocking mode and external clocking mode, are discussed in detail in the following sections.

Self-Clocking Mode

The AD7710 is configured for its self-clocking mode by tying the MODE pin high. In this mode, the AD7710 provides the serial clock signal used for the transfer of data to and from the AD7710. This self-clocking mode can be used with processors which allow an external device to clock their serial port including most digital signal processors and microcontrollers such as the 68HC11 and 68HC05. It also allows easy interfacing to serial parallel conversion circuits in systems with parallel data communication, allowing interfacing to 74XX299 Universal Shift registers without any additional decoding. In the case of shift registers, the serial clock line should have a pull down resistor instead of the pull up resistor shown in Figure 8 and Figure 9.

Read Operation

Data can be read from either the output register, the control register or from the calibration registers. A0 determines whether the data read accesses data from the control register or from the output/calibration registers. This A0 signal must remain valid for the duration of the serial read operation. The function of the $\overline{DRDY}$ line is dependent only on the output update rate of the device and the reading of the output data register. $\overline{DRDY}$ only goes low when a new data word is available in the output data register. It is reset high when the last bit of data (either 16th bit or 24th bit) is read from the output register. If a new data word becomes available to the output register while data is being read from the output register, $\overline{DRDY}$ will not indicate this and the new data word will be lost to the user. $\overline{DRDY}$ is not affected by reading from the control register or the calibration registers.

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Data can only be accessed from the output data register when $\overline{DRDY}$ is low. If $\overline{RFS}$ goes low while $\overline{DRDY}$ is high, the SCLK and SDATA lines will not become active until $\overline{DRDY}$ goes low. When $\overline{DRDY}$ goes low, the data word will then be output by the AD7710. If $\overline{RFS}$ goes low with $\overline{DRDY}$ high, no data transfer will take place until $\overline{DRDY}$ does go low. Provided $\overline{RFS}$ stays low for long enough, $\overline{RFS}$ can in most cases be brought low at any time with the AD7710 clocking the data into the microprocessor, microcontroller or shift register when its clock and data lines become active. $\overline{DRDY}$ does not have any effect on reading data from the control register or from the calibration registers.

Figures 8a and 8b show timing diagrams for reading from the AD7710 in the self-clocking mode. Figure 8a shows a situation where all the data is read from the AD7710 in one read operation. Figure 8b shows a situation where the data is read from the AD7710 over a number of read operations. Both read operations show a read from the AD7710's output data register. A read from the control register or calibration registers is similar but in these cases the $\overline{DRDY}$ line is not related to the read function. It can go low at any stage in the read cycle without affecting the read and its status should be ignored.

Figure 8a shows a read operation to the AD7710 where $\overline{RFS}$ remains low for the duration of the data word transmission. For the timing diagram shown, it is assumed that there is a pull up resistor on the SCLK output. With $\overline{DRDY}$ low, the $\overline{RFS}$ input is brought low. $\overline{RFS}$ going low enables the serial clock of the AD7710 and also places the MSB of the word on the serial data line. All subsequent data bits are clocked out on a high to low transition of the serial clock and are valid prior to the following rising edge of this clock. The final active falling edge of SCLK clocks out the LSB and this LSB is valid prior to the final active rising edge of SCLK. Coincident with the next falling edge of SCLK, $\overline{DRDY}$ is reset high. $\overline{DRDY}$ going high turns off the SCLK and the SDATA outputs. This means that the data hold time for the LSB is slightly shorter than for all other bits.

Figure 8b shows a timing diagram for a read operation where $\overline{RFS}$ returns high during the transmission of the word and returns low again to access the rest of the data word. As before, the waveform for SCLK assumes that there is a pull up resistor on this line. Timing parameters and functions are very similar to that outlined for Figure 8a, but Figure 8b has a number of additional times to show timing relationships when $\overline{RFS}$ returns high in the middle of transferring a word.

PRELIMINARY TECHNICAL DATA

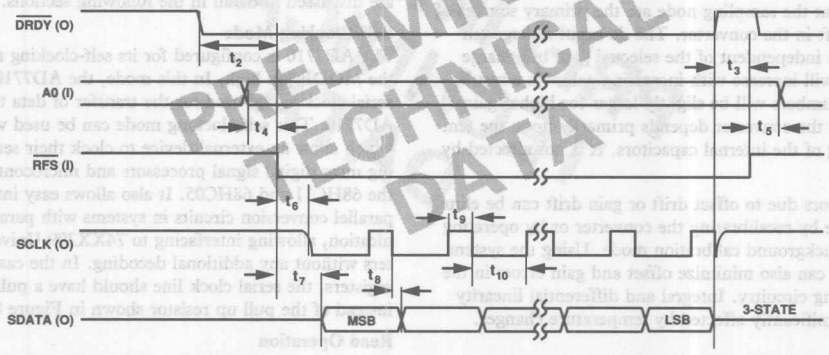


Figure 8a. Self-Clocking Mode, Output Data Read Operation

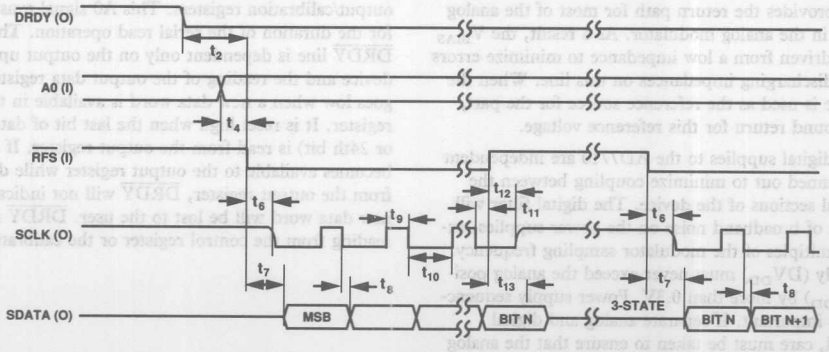


Figure 8b. Self-Clocking Mode, Output Data Read Operation ($\overline{RFS}$ Returns High During Read Operation)

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$\overline{RFS}$ should return high during a low time of SCLK. On the rising edge of $\overline{RFS}$, the SCLK and SDATA outputs are turned off. $\overline{DRDY}$ remains low and will remain low until all bits of the data word are read from the AD7710, regardless of the number of times $\overline{RFS}$ changes state during the read operation. When $\overline{RFS}$ returns low again, it turns on the SCLK output and activates the SDATA output. The first bit placed on the SDATA line after $\overline{RFS}$ goes low is the same bit as appeared on the bus when $\overline{RFS}$ went high. When the entire word is transmitted, the $\overline{DRDY}$ line will go high turning off the SDATA and SCLK lines as per Figure 8a.

Write Operation

Data can be written to either the control register or calibration registers. In either case, the write operation is not affected by the $\overline{DRDY}$ line and the write operation does not have any effect on the status of $\overline{DRDY}$.

Figure 9a shows a write operation to the AD7710 with $\overline{TFS}$ remaining low for the duration of the write operation. A0 determines whether a write operation transfers data to the control register or to the calibration registers. This A0 signal must remain valid for the duration of the serial write operation. The falling edge of $\overline{TFS}$ enables the internally generated SCLK output. The serial data to be loaded to the AD7710 must be valid on the rising edge of this SCLK signal. Data is clocked into the AD7710 on the rising edge of the SCLK signal with the MSB transferred first. On the last active rising edge of SCLK, the LSB is loaded to the AD7710. Subsequent to the next falling edge of SCLK, the SCLK output is turned off. (The timing diagram of Figure 9a assumes a pull up resistor on the SCLK line.)

Figure 9b shows a timing diagram for a write operation to the AD7710 with $\overline{TFS}$ returning high during the write operation and returning low again to write the rest of the data word. Once again, the timing diagram of Figure 9b assumes a pull up resistor on the SCLK output. Timing parameters and functions are very similar to that outlined for Figure 9a but Figure 9b has a number of additional times to show timing relationships when $\overline{TFS}$ returns high in the middle of transferring a word.

The falling edge of $\overline{TFS}$ again initiates the SCLK output and data to be loaded to the AD7710 must be valid prior to the rising edge of this SCLK signal. The rising edge of $\overline{TFS}$ turns off the SCLK output. $\overline{TFS}$ should return high during the low time of SCLK. When $\overline{TFS}$ returns low again, it turns on the SCLK output. When all data bits have been written to the device, the SCLK output is turned off as per Figure 9a.

External Clocking Mode

The AD7710 is configured for its external clocking mode by tying the MODE pin low. In this mode, SCLK of the AD7710 is configured as an input and an external serial clock must be provided to this SCLK pin. This external clocking mode is designed for direct interface to systems which provide a serial clock output which is synchronized to the serial data output, including microcontrollers such as the 80C51, 87C51, 68HC11 and 68HC05 and most digital signal processors.

PRELIMINARY TECHNICAL DATA

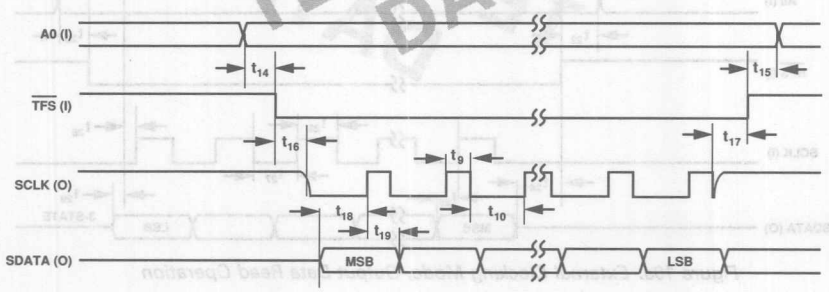


Figure 9a. Self-Clocking Mode, Control/Calibration Register Write Operation

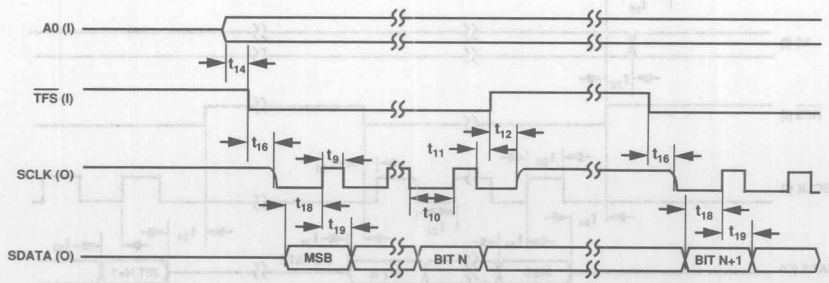


Figure 9b. Self-Clocking Mode, Control/Calibration Register Write Operation ($\overline{TFS}$ Returns High During Write Operation)

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AD7710 in the external clocking mode. Figure 10a shows a situation where all the data is read from the AD7710 in one read operation. Figure 10b shows a situation where the data is read from the AD7710 over a number of read operations.

As with the self-clocking mode, data can be read from either the output register, the control register or from the calibration registers. A0 determines whether the data read accesses data from the control register or from the output/calibration registers. This A0 signal must remain valid for the duration of the serial read operation. The function of the $\overline{\text{DRDY}}$ line is dependent only on the output update rate of the device and the reading of the output data register. $\overline{\text{DRDY}}$ only goes low when a new data word is available in the output data register. It is reset high when the last bit of data (either 16th bit or 24th bit) is read from the output register. If a new data word becomes available to the output register while data is being read from the output register, $\overline{\text{DRDY}}$ will not indicate this and the new data word will be lost to the user. $\overline{\text{DRDY}}$ is not affected by reading from the control register or the calibration register.

Data can only be accessed from the output data register when $\overline{\text{DRDY}}$ is low. If $\overline{\text{RFS}}$ goes low while $\overline{\text{DRDY}}$ is high, the SDATA line will not become active until $\overline{\text{DRDY}}$ goes low. In this external clocking mode, an external clock is applied to the SCLK input. However, with $\overline{\text{DRDY}}$ high SDATA is not active and no data is transmitted. $\overline{\text{DRDY}}$ does not have any effect on reading data from the control register or from the calibration registers.

Figure 10a shows a read operation to the AD7710 where $\overline{\text{RFS}}$ remains low for the duration of the data word transmission. With $\overline{\text{DRDY}}$ low, the $\overline{\text{RFS}}$ input is brought low. The input SCLK signal should be low between read and write operations. $\overline{\text{RFS}}$ going low places the MSB of the word to be read on the serial data line. All subsequent data bits are clocked out on a high to low transition of the serial clock and are valid prior to the following rising edge of this clock. The penultimate falling edge of SCLK clocks out the LSB and the final falling edge resets the $\overline{\text{DRDY}}$ line high. This rising edge of $\overline{\text{DRDY}}$ turns off the serial data output.

Figure 10b shows a timing diagram for a read operation where $\overline{\text{RFS}}$ returns high during the transmission of the word and returns low again to access the rest of the data word. Timing parameters and functions are very similar to that outlined for Figure 10a but Figure 10b has a number of additional times to show timing relationships when $\overline{\text{RFS}}$ returns high in the middle of transferring a word.

PRELIMINARY TECHNICAL DATA

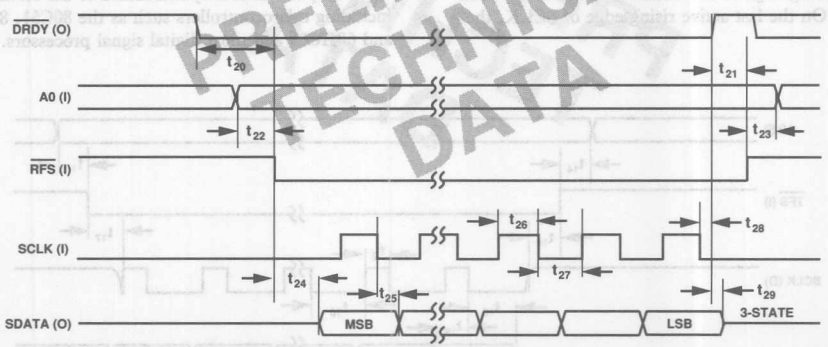


Figure 10a. External Clocking Mode, Output Data Read Operation

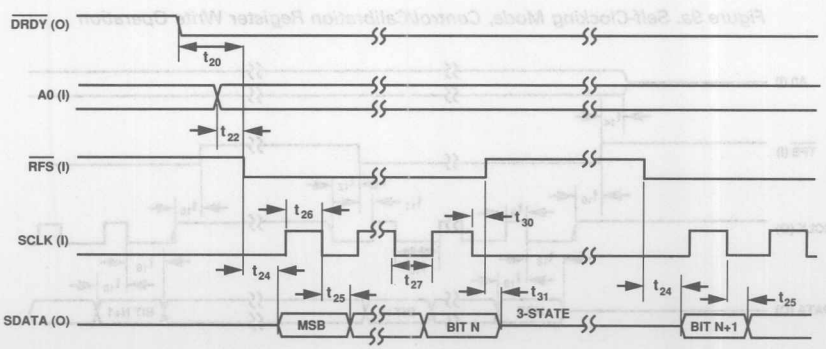


Figure 10b. External Clocking Mode, Output Data Read Operation ($\overline{\text{RFS}}$ Returns High During Read Operation)

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$\overline{RFS}$ should return high during a low time of SCLK. On the rising edge of $\overline{RFS}$, the SDATA output is turned off. $\overline{DRDY}$ remains low and will remain low until all bits of the data word are read from the AD7710, regardless of the number of times $\overline{RFS}$ changes state during the read operation. When $\overline{RFS}$ returns low again, it activates the SDATA output and places the next bit of the data word on the SDATA output. When the entire word is transmitted, the $\overline{DRDY}$ line will go high turning off the SDATA output as per Figure 10a.

Write Operation

Data can be written to either the control register or calibration registers. In either case, the write operation is not affected by the $\overline{DRDY}$ line and the write operation does not have any effect on the status of $\overline{DRDY}$.

Figure 11a shows a write operation to the AD7710 with $\overline{TFS}$ remaining low for the duration of the write operation. A0 determines whether a write operation transfers data to the control register or to the calibration registers. This A0 signal must remain valid for the duration of the serial write operation. As before, the serial clock line should be low between read and write operations. The serial data to be loaded to the AD7710 must be valid on the high level of the externally applied SCLK signal. Data is clocked into the AD7710 on the high level of this SCLK signal with the MSB transferred first. On the last active rising edge of SCLK, the LSB is loaded to the AD7710.

Figure 11b shows a timing diagram for a write operation to the AD7710 with $\overline{TFS}$ returning high during the write operation and returning low again to write the rest of the data word. Timing parameters and functions are very similar to that outlined for Figure 11a but Figure 11b has a number of additional times to show timing relationships when $\overline{TFS}$ returns high in the middle of transferring a word.

Data to be loaded to the AD7710 must be valid prior to the rising edge of the SCLK signal. $\overline{TFS}$ should return high during the low time of SCLK. After $\overline{TFS}$ returns low again, the next bit of the data word to be loaded to the AD7710 is clocked in on next high level of the SCLK input. On the last active rising edge of the SCLK input, the LSB is loaded to the AD7710.

SIMPLIFYING THE INTERFACE

In some applications, the user may not require the facility of writing to the on-chip calibration registers. In this case, the serial interface to the AD7710 can be simplified by connecting the $\overline{TFS}$ line to the A0 input of the AD7710. This means that any write to the device will load data to the control register (since A0 is low while $\overline{TFS}$ is low) and any read to the device will access data from the output data register or from the calibration registers (since A0 is high while $\overline{RFS}$ is low). It should be noted that in this arrangement the user does not have the capability of reading from the control register.

PRELIMINARY TECHNICAL DATA

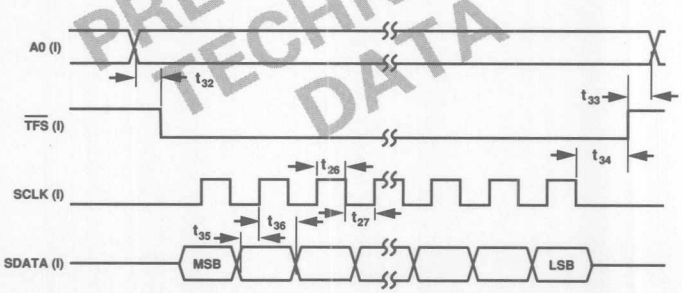


Figure 11a. External Clocking Mode, Control/Calibration Register Write Operation

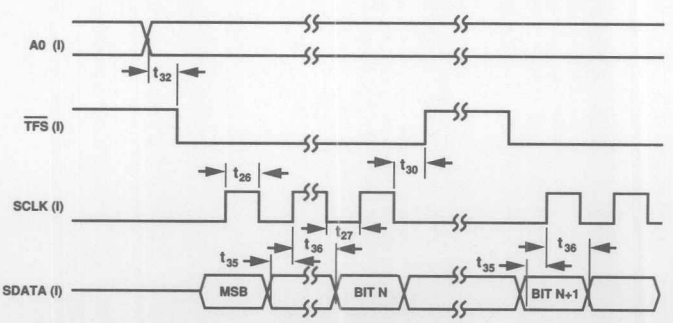
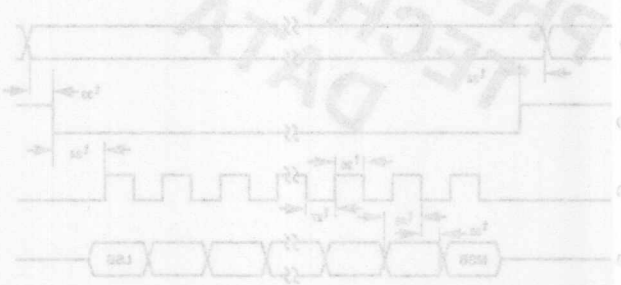


Figure 11b. External Clocking Mode, Control/Calibration Register Write Operation (TFS Returns High During Write Operation)

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LC²MOS Signal Conditioning ADC with RTD Excitation Currents

AD7711*

FEATURES

Charge Balancing ADC
- **21 Bits No Missing Codes**
- **±0.0015% Nonlinearity**

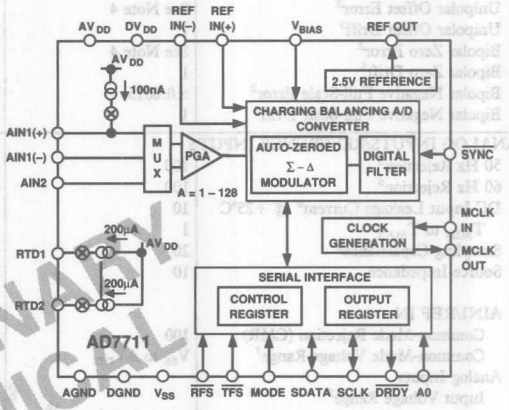
Two-Channel Programmable Gain Front End
- **Gains from 1 to 128**
- **One Differential Input**
- **One Single-Ended Input**

Low-Pass Filter with Programmable Filter Cutoffs
Ability to Read/Write Calibration Coefficients
RTD Excitation Current Sources
Bidirectional Microcontroller Serial Interface
Internal/ External Reference Option
Single or Dual Supply Operation
Low Power (25 mW typ) with Power Down Mode (50 μW typ)

APPLICATIONS

RTD Transducers
Process Control
Smart Transmitters
Portable Industrial Instruments

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD7711 is a complete analog front end for low frequency measurement applications. The device accepts low level signals directly from a transducer and outputs a serial digital word. It employs a sigma-delta conversion technique to realize up to 21 bits of no missing codes performance. The input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via the on-chip control register allowing adjustment of the filter cutoff and settling time.

The part features one differential analog input and one single ended analog input as well as a differential reference input. Normally, one of the channels will be used as the main channel with the second channel used as an auxiliary input to periodically measure a second voltage. It can be operated from a single supply (by tying the V_{SS} pin to AGND) provided that the input signals on the analog inputs are more positive than −30 mV. By taking the V_{SS} pin negative, the part can convert signals down to $-V_{REF}$ on its inputs. The part provides two current sources that can be used to provide excitation in three-wire and four-wire RTD configurations. The AD7711 thus performs all signal conditioning and conversion for a single or dual channel system.

*Patent pending.

The AD7711 is ideal for use in smart, microcontroller based systems. Gain settings, signal polarity, input channel selection and RTD current control can be configured in software using the bidirectional serial port. The AD7711 contains self-calibration, system calibration and background calibration options and also allows the user to read and to write the on-chip calibration registers.

CMOS construction ensures low power dissipation and a software programmable power down mode reduces the standby power consumption to only 50 μW typical. The part is available in a 24-pin, 0.3 inch wide, plastic and hermetic dual-in-line package (DIP) as well as a 24-lead small outline (SOIC) package.

PRODUCT HIGHLIGHTS

1. The programmable gain front end allows the AD7711 to accept input signals directly from a strain gage or transducer, removing a considerable amount of signal conditioning. On-chip current sources provide excitation for three-wire and four-wire RTD configurations.
2. No Missing Codes ensures true, usable, 21-bit dynamic range coupled with excellent ±0.0015% accuracy. The effects of temperature drift are eliminated by on-chip self-calibration, which removes zero scale and full-scale errors.
3. The AD7711 is ideal for microcontroller or DSP processor applications with an on-chip control register which allows control over filter cutoff, input gain, channel selection, signal polarity, RTD current control and calibration modes.
4. The AD7711 allows the user to read and to write the on-chip calibration registers. This means that the microcontroller has much greater control over the calibration procedure.

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Parameter	A, S Versions[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	21	Bits min	Guaranteed by Design
Output Noise	See Tables I & II		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity	±0.0015	% of FSR max	Filter Notches ≤ 60 Hz
Positive Full-Scale Error[2, 3]	See Note 4		Excluding Reference
Full-Scale Drift[5]	1	μV/°C max	Excluding Reference
Unipolar Offset Error[2]	See Note 4		
Unipolar Offset Drift[5]	1	μV/°C max	
Bipolar Zero Error[2]	See Note 4		
Bipolar Zero Drift[5]	1	μV/°C max	
Bipolar Negative Full-Scale Error[2]	±0.0015	% of FSR max	Excluding Reference; Typically ±0.0004%
Bipolar Negative Full-Scale Drift[5]	1	μV/°C max	Excluding Reference
ANALOG INPUTS/REFERENCE INPUTS			
50 Hz Rejection[6]	100	dB min	For Filter Notches of 10 Hz, 25 Hz, 50 Hz, $\pm 0.02 \times f_{NOTCH}$
60 Hz Rejection[6]	100	dB min	For Filter Notches of 10 Hz, 30 Hz, 60 Hz, $\pm 0.02 \times f_{NOTCH}$
DC Input Leakage Current[6] @ +25°C	10	pA max	
T_{MIN} to T_{MAX}	1	nA max	
Sampling Capacitance[6]	20	pF max	
Source Impedance	10	kΩ max	Maximum Allowable Output Impedance of Whatever Is Driving Either Analog Input
AIN1/REF IN			
Common-Mode Rejection (CMR)	100	dB min	At DC
Common-Mode Voltage Range[7]	V_{SS} to AV_{DD}	V min to V max	
Analog Inputs			
Input Voltage Range[8]			For Normal Operation; Depends On Gain Selected
	0 to $+V_{REF}$[9]	max	Unipolar Input Range (B/U Bit of Control Register = 0)
	$\pm V_{REF}$	max	Bipolar Input Range (B/U Bit Of Control Register = 1)
Input Sampling Rate, f_S	See Table III		
Reference Inputs			
REF IN(+) − REF IN(−) Voltage	+2.5 to +5	V min to V max	For Specified Performance
Input Sampling Rate, f_S	$f_{CLK\ IN}/512$		
REFERENCE OUTPUT			
Output Voltage	2.5	V nom	
Initial Tolerance	±1	% max	
Drift	25	ppm/°C typ	
Line Regulation (AV_{DD})	1	mV/V max	
Load Regulation	1	mV/mA max	Maximum Load Current 1 mA
External Current	1	mA max	
V_{BIAS} INPUT			
Input Voltage Range	$AV_{DD} - 0.85 \times V_{REF}$	V max	See V_{BIAS} Input Section
	$V_{SS} + 0.85 \times V_{REF}$	V min	
LOGIC INPUTS			
Input Current	±10	μA max	
All Inputs Except MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	2.0	V min	
MCLK IN Only			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	3.5	V min	

PRELIMINARY TECHNICAL DATA

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Parameter	A, S Versions[1]	Units	Conditions/Comments
LOGIC OUTPUTS			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 100 μA
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[10]	9	pF typ	
RTD EXCITATION CURRENTS (RTD1, RTD2)			
Output Current	200	μA nom	
Initial Tolerance	±20	% max	
Drift	35	ppm/°C typ	
Line Regulation (AV_{DD})	200	nA/V max	
Load Regulation	200	nA/V max	
TRANSDUCER BURN-OUT			
Current	100	nA nom	
Initial Tolerance	±10	% typ	
Drift	100	ppm/°C typ	
SYSTEM CALIBRATION			
Positive Full-Scale Calibration Limit[11]	$(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Negative Full-Scale Calibration Limit[11]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Offset Calibration Limit[12]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Input Span[12]	$0.8 \times V_{REF}/GAIN$	V min	GAIN Is the Selected PGA Gain (Between 1 and 128)
	$(2.1 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
POWER REQUIREMENTS			
Power Supply Voltages			
$AV_{DD} - V_{SS}$ Voltage	+5 to +10	V nom	±10% for Specified Performance
DV_{DD} Voltage	+5	V nom	±10% for Specified Performance
Power Supply Currents			
AV_{DD} Current	3	mA max	
DV_{DD} Current	4	mA max	
V_{SS} Current	1.5	mA max	V_{SS} = −5 V
Power Supply Rejection[13]			Rejection w.r.t. AGND. Assumes V_{BIAS} Is Fixed
Positive Supply (AV_{DD})[14]	80	dB typ	
Negative Supply (V_{SS})	90	dB typ	
Power Dissipation			
Normal Mode	40	mW max	$AV_{DD} = DV_{DD}$ = +5 V, V_{SS} = 0 V; Typically 25 mW
Normal Mode	45	mW max	$AV_{DD} = DV_{DD}$ = +5 V, V_{SS} = −5 V; Typically 30 mW
Standby (Power-Down) Mode	100	μW max	$AV_{DD} = DV_{DD}$ = +5 V, V_{SS} = 0 V or −5 V; Typically 50 μW

PRELIMINARY TECHNICAL DATA

NOTES

[1]Temperature ranges are as follows: A Version, −40°C to +85°C; S Version −55°C to +125°C.

[2]Applies after calibration at the temperature of interest.

[3]Positive full-scale error applies to both unipolar and bipolar input ranges.

[4]These errors will be of the order of the output noise of the part, as shown in Table I.

[5]Recalibration at any temperature or use of the background calibration mode will remove these drift errors. These numbers are guaranteed by design and/or characterization.

[6]These numbers are guaranteed by design and/or characterization.

[7]This common-mode voltage range is allowed provided that the absolute value of the input voltage does not exceed AV_{DD} +30 mV and V_{SS} −30 mV.

[8]The analog inputs present a very high impedance dynamic load which varies with clock frequency and input sample rate. The maximum recommended source resistance is 10 kΩ.

[9]V_{REF} = REF IN(+) − REF IN(−).

[10]Sample tested at +25°C to ensure compliance.

[11]After calibration, if the analog input exceeds positive full scale then the converter will output all 1s. If the analog input is less than negative full scale, then the device will output all 0s.

[12]These calibration and span limits apply provided that the absolute voltage on the analog inputs does not exceed V_{DD} or does not go more negative than V_{SS} − 30 mV. The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.

[13]Measured at dc and applies in the selected passband. PSRR at 50 Hz will exceed 120 dB with filter notches of 10 Hz, 25 Hz or 50 Hz. PSRR at 60 Hz will exceed 120 dB with filter notches of 10 Hz, 30 Hz or 60 Hz.

[14]This number can be improved (to 95 dB typ) by deriving the V_{BIAS} voltage (via Zener diode or reference) from the AV_{DD} supply.

Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

AV_{DD} to V_{SS} . . . . . −0.3 V to +12 V
AV_{DD} to AGND . . . . . −0.3 V to +12 V
AV_{DD} to DGND . . . . . −0.3 V to +12 V
DV_{DD} to AGND . . . . . −0.3 V to +6 V
DV_{DD} to DGND . . . . . −0.3 V to +6 V
V_{SS} to AGND . . . . . +0.3 V to −6 V
V_{SS} to DGND . . . . . +0.3 V to −6 V
AGND to DGND . . . . . −0.3 V to AV_{DD}+0.3 V
Analog Input Voltage to AGND . . V_{SS}−0.3 V to AV_{DD}+0.3 V
Reference Input Voltage to AGND
. . . . . V_{SS}−0.3 V to AV_{DD}+0.3 V
REF OUT to AGND . . . . . −0.3 V to AV_{DD}
Digital Input Voltage to DGND . . . . −0.3 V to DV_{DD}+0.3 V
Digital Output Voltage to DGND . . . −0.3 V to DV_{DD}+0.3 V
Operating Temperature Range
Commercial (A Version) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



TIMING CHARACTERISTICS[1, 2] (DV_{DD} = +5 V ± 10%; AV_{DD} = +5 V or +10 V ± 10%; V_{SS} = 0 V or −5 V ±10%; AGND = DGND = 0 V; f_{CLKIN} = 10 MHz; Input Logic 0 = 0 V, Logic 1 = DV_{DD}, unless otherwise stated.)

Parameter	Limit at T_{MIN}, T_{MAX} (A, S Versions)	Units	Conditions/Comments
$f_{CLK\ IN}$[3, 4]	400	kHz min	Master Clock Frequency: Internal Gate Oscillator
	12	MHz max	Typically 10 MHz; 10 MHz for Specified Performance
	400	kHz min	Master Clock Frequency: Externally Supplied
	10	MHz max	
$t_{CLK\ IN\ LO}$	0.2 × $t_{CLK\ IN}$	ns min	Master Clock Input Low Time
	0.8 × $t_{CLK\ IN}$	ns max	
$t_{CLK\ IN\ HI}$	0.2 × $t_{CLK\ IN}$	ns min	Master Clock Input High Time
	0.8 × $t_{CLK\ IN}$	ns max	
t_r[5]	50	ns max	Digital Output Rise Time; Typically 20 ns
t_f[5]	50	ns max	Digital Output Fall Time; Typically 20 ns
t_1	1000	ns min	$\overline{SYNC}$ Pulse Width
Self-Clocking Mode			
t_2	4 × $t_{CLK\ IN}$	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Setup Time. $t_{CLK\ IN}$ = 1/$f_{CLK\ IN}$
t_3	4 × $t_{CLK\ IN}$	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Hold Time
t_4	2 × $t_{CLK\ IN}$	ns min	A0 to $\overline{RFS}$ Setup Time
t_5	50	ns min	A0 to $\overline{RFS}$ Hold Time
t_6	4 × $t_{CLK\ IN}$	ns max	$\overline{RFS}$ Low to SCLK Falling Edge
t_7[6]	3 × $t_{CLK\ IN}$	ns max	Data Access Time ($\overline{RFS}$ Low to Data Valid)
t_8[6]	$t_{CLK\ IN}$/2	ns min	SCLK Falling Edge to Data Valid Delay
	$t_{CLK\ IN}$/2 + 20	ns max	
t_9	$t_{CLK\ IN}$/2	ns nom	SCLK High Pulse Width
t_{10}	3 × $t_{CLK\ IN}$/2	ns nom	SCLK Low Pulse Width
t_{11}	10	ns min	$\overline{RFS}$/$\overline{TFS}$ to SCLK Falling Edge Hold Time
	$t_{CLK\ IN}$/2	ns max	
t_{12}	20	ns max	$\overline{RFS}$/$\overline{TFS}$ to SCLK Delay
t_{13}[7]	20	ns max	$\overline{RFS}$ to Data Valid Hold Time
t_{14}	2 × $t_{CLK\ IN}$	ns min	A0 to $\overline{TFS}$ Setup Time
t_{15}	50	ns min	A0 to $\overline{TFS}$ Hold Time
t_{16}	4 × $t_{CLK\ IN}$	ns max	$\overline{TFS}$ to SCLK Falling Edge Delay Time
t_{17}	4 × $t_{CLK\ IN}$	ns min	$\overline{TFS}$ to SCLK Falling Edge Hold Time
t_{18}	20	ns min	Data Valid to SCLK Setup Time
t_{19}	20	ns min	Data Valid to SCLK Hold Time

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Parameter	Limit at T_{MIN}, T_{MAX} (A, S Versions)	Units	Conditions/Comments
External-Clocking Mode			
f_{SCLK}	$f_{CLK\ IN}/5$	MHz max	Serial Clock Input Frequency
t_{20}	$4 \times t_{CLK\ IN}$	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Setup Time
t_{21}	$4 \times t_{CLK\ IN}$	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Hold Time
t_{22}	$2 \times t_{CLK\ IN}$	ns min	A0 to $\overline{RFS}$ Setup Time
t_{23}	50	ns min	A0 to $\overline{RFS}$ Hold Time
t_{24}[6]	$3 \times t_{CLK\ IN}$	ns max	Data Access Time ($\overline{RFS}$ Low to Data Valid)
t_{25}[6]	$t_{CLK\ IN}/2$	ns min	SCLK Falling Edge to Data Valid Delay
	$t_{CLK\ IN}/2 + 20$	ns max	
t_{26}	$2 \times t_{CLK\ IN}$	ns min	SCLK High Pulse Width
t_{27}	$2 \times t_{CLK\ IN}$	ns min	SCLK Low Pulse Width
t_{28}	10	ns max	SCLK Falling Edge to $\overline{DRDY}$ High
t_{29}[7]	10	ns min	$\overline{DRDY}$ to Data Valid Hold Time
	20	ns max	
t_{30}	10	ns min	$\overline{RFS}$/$\overline{TFS}$ to SCLK Falling Edge Hold Time
	$t_{CLK\ IN}$	ns max	
t_{31}[7]	20	ns max	$\overline{RFS}$ to Data Valid Hold Time
t_{32}	$2 \times t_{CLK\ IN}$	ns min	A0 to $\overline{TFS}$ Setup Time
t_{33}	50	ns min	A0 to $\overline{TFS}$ Hold Time
t_{34}	10	ns max	SCLK Falling Edge to $\overline{TFS}$ Hold Time
t_{35}	20	ns min	Data Valid to SCLK Setup Time
t_{36}	20	ns min	Data Valid to SCLK Hold Time

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr= tf= 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figures 8 to 11.
[3]CLK IN Duty Cycle range is 20% to 80%. CLK IN must be supplied whenever the AD7711 is not in STANDBY mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.
[4]The AD7711 is production tested with $f_{CLK\ IN}$ at 10 MHz. It is guaranteed by characterization to operate at 400 kHz.
[5]Specified using 10% and 90% points on waveform of interest.
[6]These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.4 V.
[7]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 100 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and, as such, are independent of external bus loading capacitances.

PRELIMINARY TECHNICAL DATA

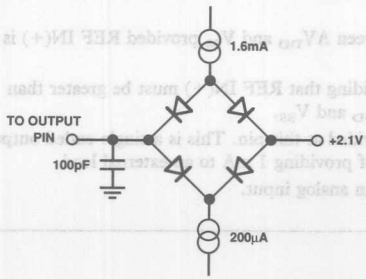
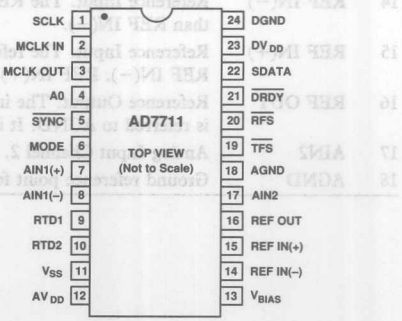


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

PIN CONFIGURATION
DIP and SOIC



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PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Function
1	SCLK	Serial Clock. Logic Input/Output depending on the status of the MODE pin. When MODE is high, the device is in its self-clocking mode and the SCLK pin provides a serial clock output. This SCLK becomes active when $\overline{RFS}$ or $\overline{TFS}$ goes low and it goes high impedance when either $\overline{RFS}$ or $\overline{TFS}$ returns high or when the device has completed transmission of an output word. When MODE is low, the device is in its external clocking mode and the SCLK pin acts as an input. This input serial clock can be a continuous clock with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to the AD7711 in smaller batches of data.
2	MCLK IN	Master Clock signal for the device. This can be provided in the form of a crystal or external clock. A crystal can be tied across the MCLK IN and MCLK OUT pins. Alternatively, the MCLK IN pin can be driven with a CMOS-compatible clock and MCLK OUT left unconnected. The clock input frequency is nominally 10 MHz.
3	MCLK OUT	When the master clock for the device is a crystal, the crystal is connected between MCLK IN and MCLK OUT.
4	A0	Address Input. With this input low, reading and writing to the device is to the control register. With this input high, access is to either the data register or the calibration registers.
5	$\overline{SYNC}$	Logic Input which allows for synchronization of the digital filters when using a number of AD7711s. It resets the nodes of the digital filter.
6	MODE	Logic Input. When this pin is high, the device is in its self-clocking mode; with this pin low, the device is in its external clocking mode.
7	AIN1(+)	Analog Input Channel 1. Positive input of the programmable gain differential analog input. The AIN1(+) input is connected to an output current source which can be used to check that an external transducer has burnt out or gone open circuit. This output current source can be turned on/off via the control register.
8	AIN1(−)	Analog Input Channel 1. Negative input of the programmable gain differential analog input.
9	RTD1	Constant Current Output. A nominal 200 μA constant current is provided at this pin, and this can be used as the excitation current for RTDs. This current can be turned on or off via the control register
10	RTD2	Constant Current Output. A nominal 200 μA constant current is provided at this pin, and this can be used as the excitation current for RTDs. This current can be turned on or off via the control register. This second current can be used to eliminate lead resistance errors in three-wire RTD configurations.
11	V_{SS}	Analog Negative Supply, 0 V to −5 V. Tied to AGND for single supply operation. The input voltage on AIN1 or AIN2 should not go > 30 mV negative w.r.t. V_{SS} for correct operation of the device.
12	AV_{DD}	Analog Positive Supply Voltage, +5 V to +10 V.
13	V_{BIAS}	Input Bias Voltage. This input voltage should be set such that $V_{BIAS} + 0.85 \times V_{REF} < AV_{DD}$ and $V_{BIAS} - 0.85 \times V_{REF} > V_{SS}$ where V_{REF} is REF IN(+)− REF IN(−). Ideally, this should be tied halfway between AV_{DD} and V_{SS}. Thus, with AV_{DD} = +5 V and V_{SS} = 0 V, it can be tied to REF OUT; with AV_{DD} = +5 V and V_{SS} = −5 V, it can be tied to AGND, while with AV_{DD} = +10 V, it can be tied to +5 V or to REF OUT.
14	REF IN(−)	Reference Input. The REF IN(−) can lie anywhere between AV_{DD} and V_{SS} provided REF IN(+) is greater than REF IN(−).
15	REF IN(+)	Reference Input. The reference input is differential providing that REF IN(+) must be greater than REF IN(−). REF IN(+) can lie anywhere between AV_{DD} and V_{SS}.
16	REF OUT	Reference Output. The internal +2.5 V reference is provided at this pin. This is a single ended output which is referred to AGND. It is a buffered output is capable of providing 1 mA to an external load.
17	AIN2	Analog Input Channel 2. Single ended programmable gain analog input.
18	AGND	Ground reference point for analog circuitry.

PRELIMINARY TECHNICAL DATA

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Pin	Mnemonic	Function
19	$\overline{TFS}$	Transmit Frame Synchronization. Active low logic input used to write serial data to the device with serial data expected after the falling edge of this pulse. In the self-clocking mode, the serial clock becomes active after $\overline{TFS}$ goes low. During a write operation to the AD7711, the SDATA line should not return to high impedance until after $\overline{TFS}$ returns high.
20	$\overline{RFS}$	Receive Frame Synchronization. Active low logic input used to access serial data from the device. In the self-clocking mode, the SCLK and SDATA lines both become active after $\overline{RFS}$ goes low. In the external clocking mode, the SDATA line becomes active after $\overline{RFS}$ goes low.
21	$\overline{DRDY}$	Logic output. A falling edge indicates that a new output word is available for transmission. The $\overline{DRDY}$ pin will return high upon completion of transmission of a full output word. $\overline{DRDY}$ is also used to indicate when the AD7711 has completed its on-chip calibration sequence.
22	SDATA	Serial Data. Input /Output with serial data being written to either the control register or the calibration registers and serial data being accessed from the control register, calibration registers or the data register. During a read operation, serial data becomes active after $\overline{RFS}$ goes low. During a write operation, valid serial data is expected on the rising edges of SCLK when $\overline{TFS}$ is low.
23	DV_{DD}	Digital Supply Voltage, +5 V. DV_{DD} should never exceed AV_{DD} by more than 0.3 V. If DV_{DD} powers up before AV_{DD}, or if DV_{DD} can exceed AV_{DD} by more than 0.3 V at any other time, a Schottky diode should be placed between the two pins.
24	DGND	Ground reference point for digital circuitry.

TERMINOLOGY

INTEGRAL NONLINEARITY

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and full scale, a point 0.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

POSITIVE FULL-SCALE ERROR

Positive full-scale error is the deviation of the last code transition (111 . . . 110 to 111 . . . 111) from the ideal input full-scale voltage. For AIN1(+), the ideal full-scale input voltage is (AIN1(−) + V_{REF}/GAIN −3/2 LSBs); for AIN2, the ideal full-scale input voltage is V_{REF}/GAIN −3/2 LSBs. It applies to both unipolar and bipolar analog input ranges.

UNIPOLAR OFFSET ERROR

Unipolar offset error is the deviation of the first code transition from the ideal input voltage. For AIN1(+), the ideal input voltage is (AIN1(−) + 0.5 LSB); for AIN2, the ideal input is 0.5 LSB when operating in the unipolar mode.

BIPOLAR ZERO ERROR

This is the deviation of the midscale transition (0111 . . . 111 to 1000 . . . 000) from the ideal input voltage. For AIN1(+), the ideal input voltage is (AIN1(−) −0.5 LSB); for AIN2, the ideal input is −0.5 LSB when operating in the bipolar mode.

BIPOLAR NEGATIVE FULL-SCALE ERROR

This is the deviation of the first code transition from the ideal input voltage. For AIN1(+), the ideal input voltage is (AIN1(−) −V_{REF}/GAIN + 0.5 LSB); for AIN2 the ideal input is −V_{REF}/GAIN + 0.5 LSB when operating in the bipolar mode.

POSITIVE FULL-SCALE OVERRANGE

Positive full-scale overrange is the amount of overhead available to handle input voltages on the AIN1(+) input greater than AIN1(−) +V_{REF}/GAIN or on the AIN2 input greater than +V_{REF}/GAIN (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or to overflowing the digital filter.

NEGATIVE FULL-SCALE OVERRANGE

This is the amount of overhead available to handle voltages on AIN1(+) below AIN1(−) −V_{REF}/GAIN or on AIN2 below −V_{REF}/GAIN without overloading the analog modulator or overflowing the digital filter. Note that the analog input will accept negative voltage peaks on AIN1(+) even in the unipolar mode provided that AIN1(+) is greater than AIN1(−) and greater than V_{SS}−30 mV.

OFFSET CALIBRATION RANGE

In the system calibration modes, the AD7711 calibrates its offset with respect to the analog input. The offset calibration range specification defines the range of voltages that the AD7711 can accept and still calibrate offset accurately.

FULL-SCALE CALIBRATION RANGE

This is the range of voltages that the AD7711 can accept in the system calibration mode and still calibrate full scale correctly.

INPUT SPAN

In system calibration schemes, two voltages applied in sequence to the AD7711's analog input define the analog input range. The input span specification defines the minimum and maximum input voltages from zero to full scale that the AD7711 can accept and still calibrate gain accurately.

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the contents of the control register.

MD2	MD1	MD0	G2	G1	G0	CH	PD	WL	RO	BO	B/U

FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0

Operating Mode

MD2	MD1	MD0	Operating Mode
0	0	0	Normal Mode. This is the normal mode of operation of the device whereby a read to the device with A0 high accesses data from the data register. This is the default condition of these bits after the internal power-on reset.
0	0	1	Activate Self-Calibration. This activates self-calibration on the channel selected by CH. This is a one-step calibration sequence, and when complete, the part returns to Normal Mode. The $\overline{DRDY}$ output indicates when this self-calibration is complete. For this calibration type, the zero scale calibration is done internally on AGND and the full-scale calibration is done internally on V_{REF}.
0	1	0	Activate System Calibration. This activates system calibration on the channel selected by CH. This is a two-step calibration sequence, with the zero scale calibration done first on the selected input channel and $\overline{DRDY}$ indicating when this zero scale calibration is complete. The part returns to Normal Mode at the end of this first step in the two-step sequence.
0	1	1	Activate System Calibration. This is the second step of the system calibration sequence with full-scale calibration being performed on the selected input channel. Once again, $\overline{DRDY}$ indicates when the full-scale calibration is complete. When this calibration is complete, the part returns to Normal Mode.
1	0	0	Activate System Offset Calibration. This activates system offset calibration on the channel selected by CH. This is a one step calibration sequence, and when complete, the part returns to Normal Mode with $\overline{DRDY}$ indicating when this system offset calibration is complete. For this calibration type, the zero scale calibration is done on the selected input channel and the full-scale calibration is done internally on V_{REF}.
1	0	1	Activate Background Calibration. This activates background calibration on the channel selected by CH. If the background calibration mode is on, then the AD7711 provides continuous self-calibration of the reference and AGND. This calibration takes place as part of the conversion sequence, extending the conversion time and reducing the word rate by a factor of six. Its major advantage is that the user does not have to worry about recalibrating the device when there is a change in the ambient temperature. In this mode, AGND and V_{REF}, as well as the analog input voltage, are continuously monitored and the calibration registers of the device are automatically updated, if necessary.
1	1	0	Read/Write Zero Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the zero scale calibration coefficients of the channel selected by CH. A write to the device with A0 high writes data to the zero scale calibration coefficients of the channel selected by CH. The word length for reading and writing these coefficients is 24 bits, regardless of the status of the WL bit of the control register.
1	1	1	Read/Write Full-Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the full-scale calibration coefficients of the channel selected by CH. A write to the device with A0 high writes data to the full-scale calibration coefficients of the channel selected by CH. The word length for reading and writing these coefficients is 24 bits, regardless of the status of the WL bit of the control register.

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PGA Gain

G2	G1	G0	Gain	
0	0	0	1	(Default Condition After the
0	0	1	2	Internal Power-On Reset)
0	1	0	4	
0	1	1	8	
1	0	0	16	
1	0	1	32	
1	1	0	64	
1	1	1	128	

Channel Selection

CH	Channel	
0	AIN1	(Default Condition After the
1	AIN2	Internal Power-On Reset)

Power-Down

PD		
0	Normal Operation	(Default Condition After the
1	Power-Down	Internal Power-On Reset)

Word Length

WL	Output Word Length	
0	16-Bit	(Default Condition After
1	24-Bit	Internal Power-On Reset)

RTD Excitation Currents

RO		
0	Off	(Default Condition After
1	On	Internal Power-On Reset)

Burn-out Current

BO		
0	Off	(Default Condition After
1	On	Internal Power-On Reset)

Bipolar/Unipolar Selection (Both Inputs)

B/U		
0	Bipolar	(Default Condition After
1	Unipolar	Internal Power-On Reset)

FILTER SECTION (FS11–FS0)

The on-chip digital filter provides a $Sinc^3$ (or $(Sinx/x)^3$ filter response. The 12 bits of data programmed into these bits determine the filter cutoff frequency, the position of the first notch of the filter and the data rate for the part. In association with the gain selection, it also determines the output noise (and hence the effective resolution) of the device.

The first notch of the filter occurs at a frequency determined by the relationship: filter first notch frequency = $(f_{CLK\ IN}/512)/code$ where *code* is the decimal equivalent of the code in bits FS0 to FS11 and is in the range 19 to 2,000. With the nominal $f_{CLK\ IN}$ of 10 MHz, this results in a first notch frequency range from 9.76 Hz to 1.028 kHz. To ensure correct operation of the AD7711, the value of the code loaded to these bits must be within this range. Failure to do this will result in unspecified operation of the device.

Changing the filter notch frequency, as well as the selected gain, impacts resolution. Tables I and II and Figure 2 show the effect of the filter notch frequency and gain on the effective resolution of the AD7711. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 50 Hz, then a new word is available at a 50 Hz rate or every 20 ms. If the first notch is at 1 kHz, a new word is available every 1 ms.

The settling time of the filter to a full-scale step input change is worst case 4× the data rate. For example, with the first filter notch at 50 Hz, the settling time of the filter to a full-scale step input change is 80 ms max. If the first notch is at 1 kHz, the settling time of the filter to a full-scale input step is 4 ms max.

The −3 dB frequency is determined by the programmed first notch frequency according to the relationship: filter −3 dB frequency = 0.262 × first notch frequency.

PRELIMINARY TECHNICAL DATA

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Table I shows the output rms noise for some typical notch and −3 dB frequencies. The numbers given are for the bipolar input ranges with a V_{REF} of +2.5 V. The numbers in Table I are guaranteed by a combination of testing, characterization and design. The output noise from the part comes from two sources: the quantization noise from the analog-to-digital conversion process and device noise. Device noise is independent of gain and is essentially flat across the frequency spectrum. Quantization noise is ratiometric to the input full-scale (and hence gain) and its frequency response is shaped by the modulator.

Looking at the table below, as the cutoff frequency increases, the output noise increases because more of the quantization noise of the part comes through to the output and, hence, the output noise increases with increasing −3 dB frequencies. For the lower notch settings, the output noise is dominated by the device noise and, hence, altering the gain has little effect on the output noise. At higher notch frequencies, the quantization noise dominates the output noise and, in this case, the output noise tends to decrease with increasing gain.

Since the output noise comes from two sources, the effective resolution of the device (i.e., the ratio of the output rms noise to the input full scale) does not remain constant with increasing gain or with increasing bandwidth. Table II shows the same table as Table I except that the output is now expressed in terms of effective resolution (the magnitude of the rms noise with respect to 2 × V_{REF}/GAIN, i.e., the input full scale). It is possible to do post filtering on the device to improve the output data rate for a given −3 dB frequency and also to further reduce the output noise (see Digital Filtering section).

Table I. Output Noise vs. Gain and First Notch Frequency

First Notch of Filter and O/P Data Rate[1]	Output RMS Noise (μV) −3 dB Frequency	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
10 Hz[2]	2.62 Hz	1.7	0.84	0.60	0.42	0.42	0.42	0.42	0.42
25Hz[2]	6.55 Hz	3.4	1.7	1.2	0.60	0.60	0.60	0.60	0.60
30 Hz[2]	7.86 Hz	3.4	2.4	1.2	0.84	0.84	0.60	0.60	0.60
50 Hz[2]	13.1 Hz	9.5	4.8	2.4	1.7	1.2	0.84	0.84	0.84
60 Hz[2]	15.72 Hz	13.5	6.7	3.4	1.7	1.2	1.2	0.84	0.84
100 Hz[3]	26.2 Hz	54	27	13.5	6.7	3.4	1.7	1.7	1.2
250 Hz[3]	65.5 Hz	432	216	108	54	27	13.5	6.7	4.8
500 Hz[3]	131 Hz	2.4×10^3	1.2×10^3	610	305	153	76	38	19
1 kHz[3]	262 Hz	13.8×10^3	6.9×10^3	3.4×10^3	1.7×10^3	863	432	216	108

NOTES
[1]The default condition (after the internal power-on reset) for the first notch of filter is 60 Hz.
[2]For these filter notch frequencies, the output rms noise is primarily independent of the value of the reference voltage. Therefore, increasing the reference voltage will give an increase in the effective resolution of the device (i.e., the ratio of the rms noise to the input full scale is increased since the output rms noise remains constant as the input full-scale increases).
[3]For these filter notch frequencies, the output rms noise is proportional to the value of the reference voltage.

Table II. Effective Resolution vs. Gain and First Notch Frequency

First Notch of Filter and O/P Data Rate	Effective Resolution[1] (Bits) −3 dB Frequency	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
10 Hz	2.62 Hz	21.5	21.5	21	20.5	19.5	18.5	17.5	16.5
25 Hz	6.55 Hz	20.5	20.5	20	20	19	18	17	16
30 Hz	7.86 Hz	20.5	20	20	19.5	18.5	18	17	16
50 Hz	13.1 Hz	19	19	19	18.5	18	17.5	16.5	15.5
60 Hz	15.72 Hz	18.5	18.5	18.5	18.5	18	17	16.5	15.5
100 Hz	26.2 Hz	16.5	16.5	16.5	16.5	16.5	16.5	15.5	15
250 Hz	65.5 Hz	13.5	13.5	13.5	13.5	13.5	13.5	13.5	13
500 Hz	131 Hz	11	11	11	11	11	11	11	11
1 kHz	262 Hz	8.5	8.5	8.5	8.5	8.5	8.5	8.5	8.5

NOTE
[1]Effective resolution is defined as the magnitude of the output rms noise to the input full scale (i.e., 2 × V_{REF}/GAIN). The above table applies for a V_{REF} of +2.5 V and resolution numbers are rounded to the nearest 0.5 LSB.

PRELIMINARY TECHNICAL DATA

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Figure 2 gives similar information to that outlined in Table I. In this plot, the output rms noise is shown for the full range of available cutoff frequencies rather than for some typical cutoff frequencies as in Tables I and II. The numbers given in this plot are typical values.

Figure 2. Plot of Output Noise vs. Gain and Notch Frequency

PRELIMINARY TECHNICAL DATA

CIRCUIT DESCRIPTION

The AD7711 is a sigma-delta A/D converter with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals such as those in RTD applications, industrial control or process control applications. It contains a sigma-delta (or charge balancing) ADC, a calibration microcontroller with on-chip static RAM, a clock oscillator, a digital filter and a bidirectional serial communications port.

The part contains two analog input channels, a programmable gain differential analog input and a programmable gain single ended input. The gain range is from 1 to 128 allowing the part to accept unipolar signals of between 0 to +20 mV and 0 V to +2.5 V or bipolar signals in the range from ±20 mV to ±2.5 V when the reference input voltage equals +2.5 V. The input signal to the selected analog input channel is continuously sampled at a rate determined by the frequency of the master clock, CLK IN, and the selected gain (see Table III). A charge balancing A/D converter (Sigma-Delta Modulator) converts the sampled signal into a digital pulse train whose duty cycle contains the digital information. The programmable gain function on the analog input is also incorporated in this sigma-delta modulator with the input sampling frequency being modified to give the higher gains. A sinc^3 digital low pass filter processes the output of the sigma-delta modulator and updates the output register at a rate determined by the first notch frequency of this filter. The output data can be read from the serial port randomly or periodically at any rate up to the output register update rate. The first notch of this digital filter (and hence its −3 dB frequency) can be programmed via an on-chip control register. The programmable range for this first notch frequency is from 9.76 Hz to 1.028 kHz, giving a programmable range for the −3 dB frequency of 2.58 Hz to 269 Hz.

The basic connection diagram for the part is shown in Figure 3. This shows the AD7711 in the external clocking mode with both the AV_{DD} and DV_{DD} pins of the AD7711 being driven from the analog +5 V supply. Some applications will have separate supplies for both AV_{DD} and DV_{DD} and, in some of these cases, the analog supply will exceed the +5 V digital supply (see Power Supplies and Grounding section).

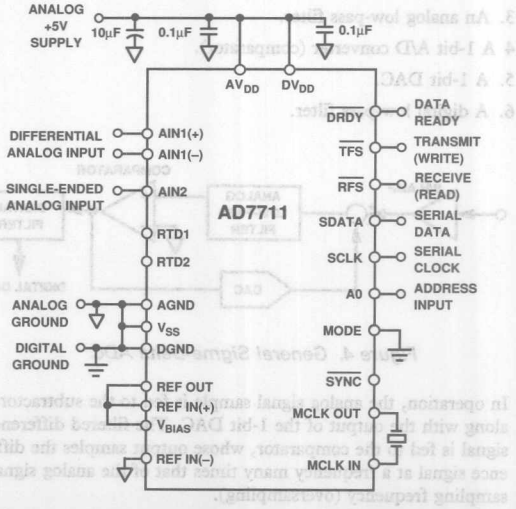


Figure 3. Basic Connection Diagram

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register. The part can perform self-calibration using the on-chip calibration microcontroller and SRAM to store calibration parameters. Other system components may also be included in the calibration loop to remove offset and gain errors in the input channel using the system calibration mode. Another option is a background calibration mode where the part continuously performs self-calibration and updates the calibration coefficients. Once the part is in this mode, the user does not have to worry about issuing periodic calibration commands to the device or asking the device to recalibrate when there is a change in the ambient temperature or power supply voltage.

The AD7711 gives the user access to the on-chip calibration registers allowing the microprocessor to read the device's calibration coefficients and also to write its own calibration coefficients to the part. This gives the microprocessor much greater control over the AD7711's calibration procedure. It also means that the user can verify that the device has performed its calibration correctly by comparing the coefficients after calibration with prestored values in E^2PROM.

The AD7711 can be operated in single supply systems provided that the analog input voltage does not go more negative than 30 mV. For larger bipolar signals, a V_{SS} of −5 V is required by the part. For battery operation, the AD7711 also offers a software programmable standby mode that reduces idle power consumption to typically 50 μW.

THEORY OF OPERATION

The general block diagram of a sigma-delta ADC is shown in Figure 4. It contains the following elements:

1. A sample hold amplifier.
2. A differential amplifier or subtractor.
3. An analog low-pass filter.
4 A 1-bit A/D converter (comparator).
5. A 1-bit DAC.
6. A digital low-pass filter.

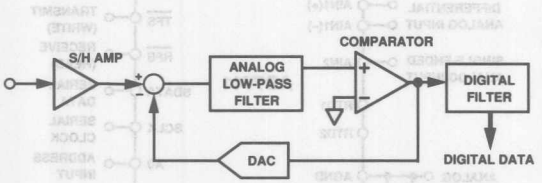


Figure 4. General Sigma-Delta ADC

In operation, the analog signal sample is fed to the subtractor, along with the output of the 1-bit DAC. The filtered difference signal is fed to the comparator, whose output samples the difference signal at a frequency many times that of the analog signal sampling frequency (oversampling).

$$SNR = (6.02 \times number\ of\ bits + 1.76)\ dB,$$

a 1-bit ADC or comparator yields an SNR of 7.78 dB.

The AD7711 samples the input signal at a frequency of 20 kHz or greater (see Table III). As a result, the quantization noise is spread over a much wider frequency than that of the band of interest. The noise in the band of interest is reduced still further by analog filtering in the modulator loop, which shapes the quantization noise spectrum to move most of the noise energy to frequencies outside the bandwidth of interest. The noise performance is thus improved from this 1-bit level to the performance outlined in Tables I and II and in Figure 2.

The output of the comparator provides the digital input for the 1–bit DAC, so that the system functions as a negative feedback loop that tries to minimize the difference signal. The digital data that represents the analog input voltage is contained in the duty cycle of the pulse train appearing at the output of the comparator. It can be retrieved as a parallel binary data word using a digital filter.

Sigma-delta ADCs are generally described by the order of the analog low pass filter. A simple example of a first order sigma-delta ADC is shown in Figure 5. This contains only a first order low pass filter or integrator. It also illustrates the derivation of the alternative name for these devices: Charge-Balancing ADCs.

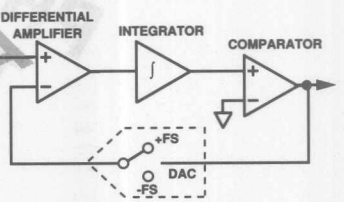


Figure 5. Basic Charge Balancing ADC

It consists of a differential amplifier (whose output is the difference between the analog input and the output of a 1-bit DAC), an integrator and a comparator. The term "charge balancing," comes from the fact that this system is a negative feedback loop that tries to keep the net charge on the integrator capacitor at zero, by balancing charge injected by the input voltage with charge injected by the 1-bit DAC. When the analog input is zero, the only contribution to the integrator output comes from the 1-bit DAC. For the net charge on the integrator capacitor to be zero, the DAC output must spend half its time at +FS and half its time at −FS. Assuming ideal components, the duty cycle of the comparator will be 50%.

When a positive analog input is applied, the output of the 1-bit DAC must spend a larger proportion of the time at +FS, so the duty cycle of the comparator increases. When a negative input voltage is applied, the duty cycle decreases.

The AD7711 uses a second-order sigma-delta modulator and a digital filter that provides a rolling average of the sampled output. After power-up, or if there is a step change in the input voltage, there is a settling time that must elapse before valid data is obtained.

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Input Sample Rate

The modulator sample frequency for the device remains at $f_{CLK\ IN}/512$ (20 kHz @ $f_{CLK\ IN}$ = 10 MHz) regardless of the selected gain. However, gains greater than ×1 are achieved by a combination of multiple input samples per modulator cycle and a scaling of the ratio of reference capacitor to input capacitor. As a result of the multiple sampling, the input sample rate of the device varies with the selected gain (see Table III). The effective input impedance is $1/C \cdot f_S$ where C is the input sampling capacitance and f_S is the input sample rate.

Table III. Input Sampling Frequency vs. Gain

Gain	Input Sampling Frequency (f_S)
1	$f_{CLK\ IN}/512$ (20 kHz @ $f_{CLK\ IN}$ = 10 MHz)
2	$2 \times f_{CLK\ IN}/512$ (40 kHz @ $f_{CLK\ IN}$ = 10 MHz)
4	$4 \times f_{CLK\ IN}/512$ (80 kHz @ $f_{CLK\ IN}$ = 10 MHz)
8	$4 \times f_{CLK\ IN}/512$ (160 kHz @ $f_{CLK\ IN}$ = 10 MHz)
16	$4 \times f_{CLK\ IN}/512$ (160 kHz @ $f_{CLK\ IN}$ = 10 MHz)
32	$4 \times f_{CLK\ IN}/512$ (160 kHz @ $f_{CLK\ IN}$ = 10 MHz)
64	$4 \times f_{CLK\ IN}/512$ (160 kHz @ $f_{CLK\ IN}$ = 10 MHz)
128	$4 \times f_{CLK\ IN}/512$ (160 kHz @ $f_{CLK\ IN}$ = 10 MHz)

DIGITAL FILTERING

The AD7711's digital filter behaves like a similar analog filter, with a few minor differences.

First, since digital filtering occurs after the A-to-D conversion process, it can remove noise injected during the conversion process. Analog filtering cannot do this.

On the other hand, analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. Digital filtering cannot do this and noise peaks riding on signals near full scale have the potential to saturate the analog modulator and digital filter, even though the average value of the signal is within limits. To alleviate this problem, the AD7711 has overrange headroom built into the sigma-delta modulator and digital filter which allows overrange excursions of 5% above the analog input range. If noise signals are larger than this, consideration should be given to analog input filtering, or to reducing the input channel voltage so that its full scale is half that of the analog input channel full scale. This will provide an overrange capability greater than 100% at the expense of reducing the dynamic range by 1 bit (50%).

Filter Characteristics

The cutoff frequency of the digital filter is determined by the value loaded to bits FS0 to FS11 in the control register. At the maximum clock frequency of 10 MHz, the minimum cutoff frequency of the filter is 2.58 Hz while the maximum programmable cutoff frequency is 269 Hz.

Figure 6 shows the filter frequency response for a cutoff frequency of 2.62 Hz which corresponds to a first filter notch frequency of 10 Hz. This is a $(\sin x/x)^3$ response (also called sinc^3) that provides >100 dB of 50 Hz and 60 Hz rejection. Programming a different cutoff frequency via FS0–FS11 does not alter the profile of the filter response; it changes the frequency of the notches as outlined in the Control Register section.

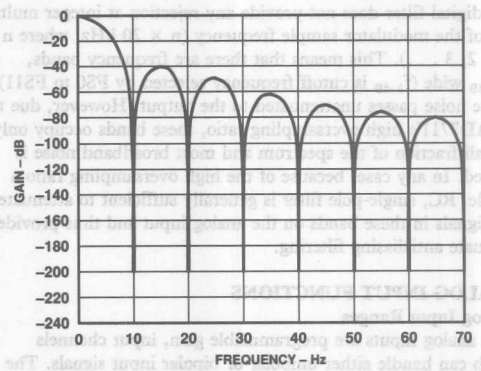


Figure 6. Frequency Response of AD7711 Filter

Since the AD7711 contains this on-chip, low pass filtering, there is a settling time associated with step function inputs, and data on the output will be invalid after a step change until the settling time has elapsed. The settling time depends upon the notch frequency chosen for the filter. The output data rate equates to this filter notch frequency and the settling time of the filter to a full-scale step input is 4 times the output data period. In applications using both input channels, the settling time of the filter must be allowed to elapse before data from the second channel is accessed.

Post Filtering

The on-chip modulator provides samples at a 20 kHz output rate. The on-chip digital filter decimates these samples to provide data at an output rate which corresponds to the programmed first notch frequency of the filter. Since the output data rate exceeds the Nyquist criterion, the output rate for a given bandwidth will satisfy most application requirements. However, there may be some applications which require a higher data rate for a given bandwidth and noise performance. Applications which need this higher data rate will require some post filtering following the digital filter of the AD7711.

For example, if the required bandwidth is 7.86 Hz but the required update rate is 100 Hz, the data can be taken from the AD7711 at the 100 Hz rate giving a −3 dB bandwidth of 26.2 Hz. Post filtering can be applied to this to reduce the bandwidth and output noise, to the 7.86 Hz bandwidth level, while maintaining an output rate of 100 Hz.

Post filtering can also be used to reduce the output noise from the device for bandwidths below 2.62 Hz. At a gain of 128, the output rms noise is 420 nV. This is essentially device noise or white noise, and since the input is chopped, the noise has a flat frequency response. By reducing the bandwidth below 2.62 Hz, the noise in the resultant passband can be reduced. A reduction in bandwidth by a factor of 2 results in a $\sqrt{2}$ reduction in the output rms noise. This additional filtering will result in a longer settling time.

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Antialias Considerations

The digital filter does not provide any rejection at integer multiples of the modulator sample frequency (n × 20 kHz, where n = 1, 2, 3 . . .). This means that there are frequency bands, $\pm f_{3\ dB}$ wide ($f_{3\ dB}$ is cutoff frequency selected by FS0 to FS11) where noise passes unattenuated to the output. However, due to the AD7711's high oversampling ratio, these bands occupy only a small fraction of the spectrum and most broadband noise is filtered. In any case, because of the high oversampling ratio a simple, RC, single-pole filter is generally sufficient to attenuate the signals in these bands on the analog input and thus provide adequate antialiasing filtering.

ANALOG INPUT FUNCTIONS

Analog Input Ranges

Both analog inputs are programmable gain, input channels which can handle either unipolar or bipolar input signals. The AIN1 channel is a differential input channel having a common-mode range from V_{SS} to AV_{DD}, provided that the absolute value of the analog input voltage lies between V_{SS} −30 mV and AV_{DD} +30 mV. The AIN2 input channel is a single-ended input that is referred to AGND.

The input sample rate for the part varies as per Table III and the input sampling capacitance is 15 pF typical. The effective input impedance is $1/C \cdot f_S$. This results in a maximum allowable source impedance of whatever is driving the analog input of 10 kΩ to ensure correct charging of the sampling capacitor.

The dc input leakage current is 10 pA maximum at +25°C. This results in a dc offset voltage developed across the source impedance. However, this dc offset effect can be compensated for by a combination of the differential input capability of the part and its system calibration mode.

Burn-Out Current

The AIN1(+) input of the AD7711 contains a 100 nA current source which can be turned on/off via the control register. This current source can be used in checking that a transducer has not burnt out or gone open circuit before attempting to take measurements on that channel. If the current is turned on and is allowed flow into the transducer and a measurement of the input voltage on the AIN1 input is taken, it can indicate that the transducer is malfunctioning. For normal operation, this burn-out current is turned off by writing a 0 to the BO bit in the control register.

RTD Excitation Currents

The AD7711 also contains two matched 200 μA constant current sources which are provided at the RTD1 and RTD2 pins of the device. These currents can be turned on/off via the control register. Writing a 1 to the RO bit of the control register enables these excitation currents.

For four-wire RTD applications, one of these excitation currents is used to provide the excitation current for the RTD, the second current source can be left unconnected. For three-wire RTD configurations, the second on-chip current source can be used to eliminate errors due to voltage drops across lead resistances.

The temperature coefficient of the RTD current sources is typically 35 ppm/°C with a typical matching between the temperature coefficients of both current sources of 5 ppm/°C. For applications where the absolute value of the temperature coefficient is too large, the following schemes can be used to remove the drift error.

The conversion result from the AD7711 is ratiometric to the V_{REF} voltage. Therefore, if the V_{REF} voltage varies with the RTD temperature coefficient, the temperature drift from the current source will be removed. For four-wire RTD applications, the reference voltage can be made ratiometric to RTD current source by using the second current with a low t.c. resistor to generate the reference voltage for the part. In this case, if a 12.5 kΩ resistor is used, the 200 μA current source generates +2.5 V across the resistor. This +2.5 V can be applied to the REF IN(+) input of the AD7711 and with the REF IN(−) input at ground it will supply a V_{REF} of 2.5 V for the part. For three-wire RTD configurations, the reference voltage for the part is generated by placing a low t.c. resistor (12.5 kΩ for 2.5 V reference) in series with one of the constant current sources. The RTD current sources can be driven to within 2 V of AV_{DD}. The reference input of the AD7711 is differential so the REF IN(+) and REF IN(−) of the AD7711 are driven from either side of the resistor. Both schemes ensure that the reference voltage for the part tracks the RTD current sources over temperature and, thereby, removes the temperature drift error.

Bipolar/Unipolar Inputs

The two analog inputs on the AD7711 can accept either unipolar or bipolar input voltage ranges. Bipolar or unipolar options are chosen by programming the B/U bit of the control register. This programs both channels for either unipolar or bipolar operation. Programming the part for either unipolar or bipolar operation does not change any of the input signal conditioning; it simply changes the data output coding.

The AIN1 input channel is differential and, as a result, the voltage to which the unipolar and bipolar signals are referenced is the voltage on the AIN1(−) input. For example, if AIN1(−) is +1.25 V and the AD7711 is configured for unipolar operation with a gain of 1 and a V_{REF} of +2.5 V, the input voltage range on the AIN1(+) input is +1.25 V to +3.75 V. If AIN1(−) is +1.25 V and the AD7711 is configured for bipolar mode with a gain of 1 and a V_{REF} of +2.5 V, the analog input range on the AIN1(+) input is −1.25 V to +3.75 V. For the AIN2 input, the input signals are referenced to AGND.

REFERENCE INPUT/OUTPUT

The AD7711 contains a temperature compensated +2.5 V reference which has an initial tolerance of ±25 mV. This reference voltage is provided at the REF OUT pin and it can be used as the reference voltage for the part by connecting the REF OUT pin to the REF IN(+) pin. This REF OUT pin is a single ended output, referenced to AGND, which is capable of providing up to 1 mA to an external load. In applications where REF OUT is connected directly to REF IN(+), REF IN(−) should be tied to AGND to provide the nominal +2.5 V reference for the AD7711.

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The reference inputs of the AD7711, REF IN(+) and REF IN(−), provide a differential reference input capability. The common-mode range for these differential inputs is from V_{SS} to AV_{DD}. The nominal differential voltage, V_{REF} (REF IN(+) −REF IN(−)), is +2.5 V for specified operation but the reference voltage can go to +5 V with no degradation in performance provided that the absolute value of REF IN(+) and REF IN(−) does not exceed its AV_{DD} and V_{SS} limits. REF IN(+) must always be greater than REF IN(−) for correct operation of the AD7711.

Both reference inputs provide a high impedance, dynamic load similar to the analog inputs. The maximum dc input leakage current is 10 pA (±1 μA over temperature) and source resistances will result in gain errors on the part. The reference inputs are switched capacitor inputs with the input capacitance dependent upon the selected gain. For gains of 1 to 8 the input capacitance is 20 pF; for a gain of 16 it is 10 pF; for a gain of 32 it is 5 pF; for a gain of 64 it is 2.5 pF; and for a gain of 128 it is 1.25 pF.

The digital filter of the AD7711 removes noise from the reference input just as it does with the analog input, and the same limitations apply regarding lack of noise rejection at integer multiples of the sampling frequency. The output noise performance outlined in Tables I and II assumes a clean reference. If the reference noise in the bandwidth of interest is excessive, it can degrade the performance of the AD7711. Figure 7 shows the noise performance of the AD7711's onboard reference.

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V_{BIAS} Input

The V_{BIAS} input determines at what voltage the internal analog circuitry is biased. It essentially provides the return path for analog currents flowing in the modulator and, as such, it should be driven from a low impedance point to minimize errors.

For maximum internal headroom, the V_{BIAS} voltage should be set halfway between AV_{DD} and V_{SS}. The difference between AV_{DD} and (V_{BIAS} + 0.85 × V_{REF}) determines the amount of headroom the circuit has at the upper end, while the difference between V_{SS} and (V_{BIAS} −0.85 × V_{REF}) determines the amount of headroom the circuit has at the lower end. Care should be taken in choosing a V_{BIAS} voltage to ensure that V_{BIAS} ±0.85 × V_{REF} does not exceed the AV_{DD} and V_{SS} limits. For example, with AV_{DD} = +4.75 V, V_{SS} = 0 V and V_{REF} = +2.5 V, the allowable range for the V_{BIAS} voltage is +2.125 V to +2.625 V. With AV_{DD} = +9.5 V, V_{SS} = 0 V and V_{REF} = +5 V, the range for V_{BIAS} is +4.25 V to +5.25 V. With AV_{DD} = +4.75 V, V_{SS} = −4.75 V and V_{REF} = +2.5 V, the V_{BIAS} range is −2.625 V to +2.625 V.

USING THE AD7711

SYSTEM DESIGN CONSIDERATIONS

The AD7711 operates differently from successive approximation ADCs or integrating ADCs. Since it samples the signal continuously, like a tracking ADC, there is no need for a start convert command. The output register is updated at a rate determined by the first notch of the filter and the output can be read at any time, either synchronously or asynchronously.

Clocking

The AD7711 requires a master clock input, which may be an external TTL/CMOS compatible clock signal applied to the MCLK IN pin with the MCLK OUT pin left unconnected. Alternatively, a crystal of the correct frequency can be connected between MCLK IN and MCLK OUT, in which case the clock circuit will function as a crystal controlled oscillator. For lower clock frequencies, a ceramic resonator may be used instead of the crystal. For these lower frequency oscillators, external capacitors may be required on either the ceramic resonator or on the crystal.

The input sampling frequency, the modulator sampling frequency, the −3 dB frequency, output update rate and calibration time are all directly related to the master clock frequency, $f_{CLK\ IN}$. Reducing the master clock frequency by a factor of 2 will halve the above frequencies and update rate and will double the calibration time.

The current drawn from the DV_{DD} power supply is also directly related to $f_{CLK\ IN}$. Reducing $f_{CLK\ IN}$ by a factor of 2 will halve the DV_{DD} current but will not affect the current drawn from the AV_{DD} power supply.

System Synchronization

If multiple AD7711s are operated from a common master clock, they can be synchronized to update their output registers simultaneously. A falling edge on the $\overline{SYNC}$ input resets the filter and places the AD7711 into a consistent, known state. A common signal to the AD7711s' $\overline{SYNC}$ inputs will synchronize their operation. This would normally be done after each AD7711 has performed its own calibration or has had calibration coefficients loaded to it.

ACCURACY

Sigma-Delta ADCs, like VFCs and other integrating ADCs, do not contain any source of nonmonotonicity and inherently offer no missing codes performance. The AD7711 achieves excellent linearity by the use of high quality, on-chip silicon dioxide capacitors, which have a very low capacitance/voltage coefficient. The device also achieves low input drift through the use of chopper stabilized techniques in its input stage. To ensure excellent performance over time and temperature, the AD7711 uses digital calibration techniques that minimize offset and gain error.

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from the device. A calibration routine should be initiated on the device whenever there is a change in the ambient operating temperature or supply voltage. It should also be initiated if there is a change in the selected channel, gain, filter notch or bipolar/unipolar input range. However, if the AD7711 is in its background calibration mode, the above changes are all automatically taken care of (after the settling time of the filter has been allowed for).

The AD7711 offers self-calibration, system calibration and background calibration facilities. For calibration to occur on the selected channel, the on-chip microcontroller must record the modulator output for two different input conditions. These are "zero-scale" and "full-scale" points. With these readings, the microcontroller can calculate the gain slope for the input to output transfer function of the converter. Internally, the part works with a resolution of 33 bits to determine its conversion result of either 16 bits or 24 bits.

Self-Calibration

In the self-calibration mode with a unipolar input range, the zero scale point used in determining the calibration coefficients is AGND and the full-scale point is V_{REF}. The zero scale coefficient is determined by converting an internal AGND node. The full-scale coefficient is determined from the span between this AGND conversion and a conversion on an internal V_{REF} node. The self-calibration mode is invoked by writing the appropriate values (0, 0, 1) to the MD2, MD1 and MD0 bits of the control register. In this calibration mode, the AGND node is switched in to the modulator first and a conversion is performed; the V_{REF} node is then switched in and another conversion is performed. When the calibration sequence is complete, the calibration coefficients updated and the filter resettled to the analog input voltage, the $\overline{DRDY}$ output goes low.

For bipolar input ranges in the self-calibrating mode, the sequence is very similar to that just outlined. In this case, the two points which the AD7711 calibrates are midscale (bipolar zero) and positive full scale.

System Calibration

System calibration allows the AD7711 to compensate for system gain and offset errors as well as its own internal errors. System calibration performs the same slope factor calculations as self-calibration but uses voltage values presented by the system to the AIN inputs for the zero and full-scale points. System calibration is a two-step process. The zero scale point must be presented to the converter first. It must be applied to the converter before the calibration step is initiated and must remain stable until the step is complete. System calibration is initiated by writing the appropriate values (0, 1, 0) to the MD2, MD1 and MD0 bits of the i.e., control register. The $\overline{DRDY}$ output from the device will signal when the step is complete by going low. After the zero-scale point is calibrated, the full-scale point is applied and the second step of the calibration process is initiated by again writing the appropriate values (0, 1, 1) to MD2, MD1 and MD0. Again the full-scale voltage must be set up before the calibration is initiated and it must remain stable throughout the calibration step. $\overline{DRDY}$ goes low at the end of this second step to indicate that the system calibration is complete. In the unipolar mode of the transfer function, it is performed between midscale and positive full scale.

This two-step system calibration mode offers another feature. After the sequence has been completed, additional offset calibrations can be performed by themselves to adjust the zero reference point to a new system zero reference value. This is achieved by performing the first step of the system calibration sequence (by writing 0, 1, 0 to MD2, MD1, MD0). This will adjust the zero scale or offset point but will not change the slope factor from what was set during a full system calibration sequence.

System Offset Calibration

System offset calibration is a variation of both the system calibration and self-calibration. In this case, the zero scale point for the system is presented to the AIN input of the converter. System offset calibration is initiated by writing 1, 0, 0 to MD2, MD1, MD0. The system zero scale coefficient is determined by converting the voltage applied to the AIN input, while the full-scale coefficient is determined from the span between this AIN conversion and a conversion on an internal V_{REF} node. The zero scale point should be applied to the AIN input for the duration of the calibration sequence. This is a one-step calibration sequence with $\overline{DRDY}$ going low when the sequence is completed. In the unipolar mode, the system offset calibration is performed between the two end points of the transfer function; in the bipolar mode, it is performed between midscale and positive full scale.

Background Calibration

The AD7711 also offers a background calibration mode where the part interleaves its calibration procedure with its normal conversion sequence. In the background calibration mode, the same nodes are used as the calibration points as are used in the self-calibration mode (i.e., AGND and V_{REF}). The background calibration mode is invoked by writing 1, 0, 1 to MD2, MD1, MD0 of the control register. When invoked, the background calibration mode reduces the output data rate of the AD7711 by a factor of six. Its advantage is that the part is continually performing calibration and automatically updating its calibration coefficients. As a result, the effects of temperature drift, supply sensitivity and time drift on zero and full scale errors are automatically removed. When the background calibration mode is turned on, the part will remain in this mode until bits MD2, MD1 and MD0 of the control register are changed.

Table IV summarizes the calibration modes and the calibration points associated with them.

Span and Offset Limits

Whenever a system calibration mode is used, there are limits on the amount of offset and span that can be accommodated. The range of input span in both the unipolar and bipolar modes has a minimum value of $0.8 \times V_{REF}/GAIN$ and a maximum value of $2.1 \times V_{REF}/GAIN$.

The amount of offset that can be accommodated depends on whether the unipolar or bipolar mode is being used. In unipolar mode, the system calibration modes can handle a maximum offset of $0.25 \times V_{REF}/GAIN$ and a minimum offset of $-(1.05 \times V_{REF}/GAIN)$. This offset range is limited by the requirement

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Table IV. Calibration Truth Table

Cal Type	MD2, MD1, MD0	Zero Scale Cal	Full-Scale Cal	Sequence
Self-Cal	0, 0, 1	AGND	V_{REF}	One Step
System Cal	0, 1, 0	AIN		Two Step
System Cal	0, 1, 1		AIN	Two Step
System Offset Cal	1, 0, 0	AIN	V_{REF}	One Step
Background Cal	1, 0, 1	AGND	V_{REF}	One Step

that the positive full-scale calibration limit is $\leq 1.05 \times V_{REF}$/GAIN. Thus, the maximum offset ($0.25 \times V_{REF}$/GAIN) plus the minimum span ($0.8 \times V_{REF}$/GAIN) cannot exceed $1.05 \times V_{REF}$/GAIN.

In the bipolar mode, the system offset calibration range is restricted to $\pm 0.65 \times V_{REF}$/GAIN. The span range of the converter in bipolar mode is equidistant around the voltage used for the zero scale point. Therefore, the maximum offset $\pm(0.65 \times V_{REF}$/GAIN) plus half the minimum span $\pm(0.4 \times V_{REF}$/GAIN) must be less than $\pm(1.05 \times V_{REF}$/GAIN). If the span is set to $2 \times V_{REF}$/GAIN, the input offset cannot move more than $\pm(0.05 \times V_{REF}$/GAIN) before the endpoints of the transfer function exceed the input overrange limits $\pm(1.05 \times V_{REF}$/GAIN).

POWER-UP AND CALIBRATION

On power-up, the AD7711 performs an internal reset which sets the contents of the control register to a known state. However, to ensure correct calibration for the device, a calibration routine should be performed after power-up.

The power dissipation and temperature drift of the AD7711 are low and no warm up time is required before the initial calibration is performed. However, if an external reference is being used, this reference must have stabilized before calibration is initiated.

Drift Considerations

The AD7711 uses chopper stabilization techniques to minimize input offset drift. Charge injection in the analog switches and dc leakage currents at the sampling node are the primary sources of offset voltage drift in the converter. The dc input leakage current is essentially independent of the selected gain but charge injection effects will increase with increasing gain. As a result, the offset drift numbers will be slightly larger for higher gains. Gain drift within the converter depends primarily upon the temperature tracking of the internal capacitors. It is not affected by leakage currents.

Measurement errors due to offset drift or gain drift can be eliminated at any time by recalibrating the converter or by operating the part in the background calibration mode. Using the system calibration mode can also minimize offset and gain errors in the signal conditioning circuitry. Integral and differential linearity errors are not significantly affected by temperature changes.

POWER SUPPLIES AND GROUNDING

Since the analog inputs and reference input are differential, most of the voltages in the analog modulator are common-mode voltages. V_{BIAS} provides the return path for most of the analog currents flowing in the analog modulator. As a result, the V_{BIAS} input should be driven from a low impedance to minimize errors due to charging/discharging impedances on this line. When the internal reference is used as the reference source for the part, AGND is the ground return for this reference voltage.

The analog and digital supplies to the AD7711 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The digital filter will provide rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. The digital supply (DV_{DD}) must never exceed the analog positive supply (AV_{DD}) by more than 0.3 V. Power supply sequencing, therefore, is important. If separate analog and digital supplies are used, care must be taken to ensure that the analog supply is powered up first. If this cannot be ensured, or if DV_{DD} can exceed AV_{DD} at any other time, a Schottky diode should be placed between DV_{DD} and AV_{DD}.

DIGITAL INTERFACE

The AD7711's serial communications port provides a flexible arrangement to allow easy interfacing to industry standard microprocessors, microcontrollers and digital signal processors. A serial read to the AD7711 can access data from the output register, the control register or from the calibration registers. A serial write to the AD7711 can write data to the control register or the calibration registers.

Two different modes of operation are available, optimized for different types of interface where the AD7711 can act either as master in the system (it provides the serial clock) or as slave (an external serial clock can be provided to the AD7711). These two modes, labelled self-clocking mode and external clocking mode, are discussed in detail in the following sections.

Self-Clocking Mode

The AD7711 is configured for its self-clocking mode by tying the MODE pin high. In this mode, the AD7711 provides the serial clock signal used for the transfer of data to and from the AD7711. This self-clocking mode can be used with processors that allow an external device to clock their serial port, including most digital signal processors and microcontrollers such as the 68HC11 and 68HC05. It also allows easy interfacing to serial parallel conversion circuits in systems with parallel data communication, allowing interfacing to 74XX299 Universal Shift registers without any additional decoding. In the case of shift registers, the serial clock line should have a pull-down resistor instead of the pull-up resistor shown in Figure 8 and Figure 9.

Read Operation

Data can be read from either the output register, the control register or the calibration registers. A0 determines whether the data read accesses data from the control register or from the output/calibration registers. This A0 signal must remain valid for

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the duration of the serial read operation. The function of the $\overline{DRDY}$ line is dependent only on the output update rate of the device and the reading of the output data register. $\overline{DRDY}$ only goes low when a new data word is available in the output data register. It is reset high when the last bit of data (either 16th bit or 24th bit) is read from the output register. If a new data word becomes available to the output register while data is being read from the output register, $\overline{DRDY}$ will not indicate this and the new data word will be lost to the user. $\overline{DRDY}$ is not affected by reading from the control register or the calibration registers.

Data can only be accessed from the output data register when $\overline{DRDY}$ is low. If $\overline{RFS}$ goes low while $\overline{DRDY}$ is high, the SCLK and SDATA lines will not become active until $\overline{DRDY}$ goes low. When $\overline{DRDY}$ goes low, the data word will then be output by the AD7711. If $\overline{RFS}$ goes low with $\overline{DRDY}$ high, no data transfer will take place until $\overline{DRDY}$ does go low. Provided $\overline{RFS}$ stays low for long enough, $\overline{RFS}$ can, in most cases, be brought low at any time with the AD7711 clocking the data into the microprocessor, microcontroller or shift register when its clock and data lines become active. $\overline{DRDY}$ does not have any effect on reading data from the control register or from the calibration registers.

Figures 8a and 8b show timing diagrams for reading from the AD7711 in the Self-Clocking mode. Figure 8a shows a situation where all the data is read from the AD7711 in one read operation. Figure 8b shows a situation where the data is read from the AD7711 over a number of read operations. Both read operations show a read from the AD7711's output data register. A read from the control register or calibration registers is similar but in these cases the $\overline{DRDY}$ line is not related to the read function. It can go low at any stage in the read cycle without affecting the read and its status should be ignored.

Figure 8a shows a read operation to the AD7711 where $\overline{RFS}$ remains low for the duration of the data word transmission. For the timing diagram shown, it is assumed that there is a pull up resistor on the SCLK output. With $\overline{DRDY}$ low, the $\overline{RFS}$ input is brought low. $\overline{RFS}$ going low enables the serial clock of the AD7711 and also places the MSB of the word on the serial data line. All subsequent data bits are clocked out on a high to low transition of the serial clock and are valid prior to the following rising edge of this clock. The final active falling edge of SCLK clocks out the LSB and this LSB is valid prior to the final active rising edge of SCLK. Coincident with the next falling edge of

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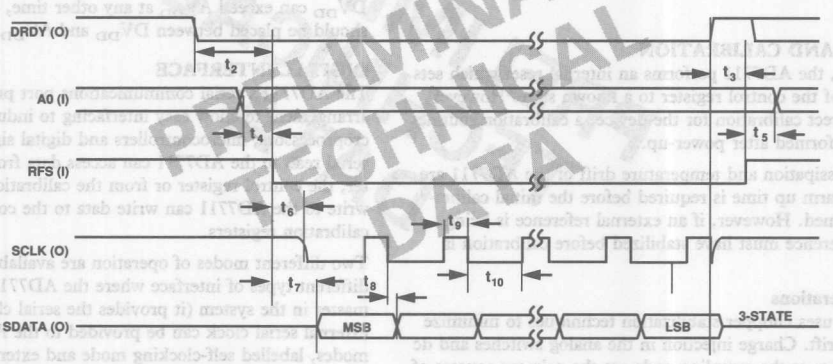


Figure 8a. Self-Clocking Mode, Output Data Read Operation

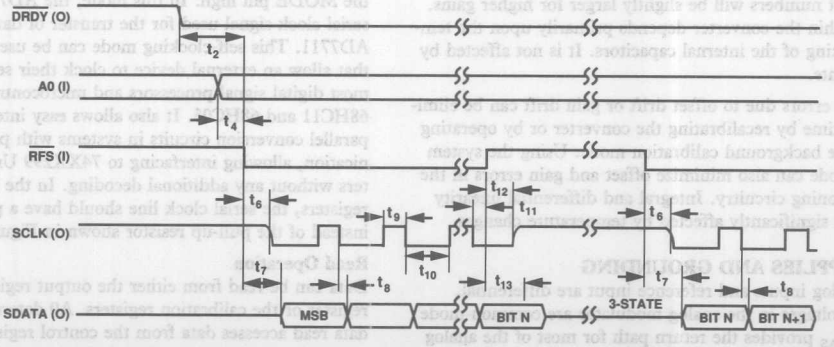


Figure 8b. Self-Clocking Mode, Output Data Read Operation ($\overline{RFS}$ Returns High During Read Operation)

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SCLK, $\overline{DRDY}$ is reset high. $\overline{DRDY}$ going high turns off the SCLK and the SDATA outputs. This means that the data hold time for the LSB is slightly shorter than for all other bits.

Figure 8b shows a timing diagram for a read operation where $\overline{RFS}$ returns high during the transmission of the word and returns low again to access the rest of the data word. As before, the waveform for SCLK assumes that there is a pull up resistor on this line. Timing parameters and functions are very similar to that outlined for Figure 8a but Figure 8b has a number of additional times to show timing relationships when $\overline{RFS}$ returns high in the middle of transferring a word.

$\overline{RFS}$ should return high during a low time of SCLK. On the rising edge of $\overline{RFS}$, the SCLK and SDATA outputs are turned off. $\overline{DRDY}$ remains low and will remain low until all bits of the data word are read from the AD7711, regardless of the number of times $\overline{RFS}$ changes state during the read operation. When $\overline{RFS}$ returns low again, it turns on the SCLK output and activates the SDATA output. The first bit placed on the SDATA line after $\overline{RFS}$ goes low is the same bit as appeared on the bus when $\overline{RFS}$ went high. When the entire word is transmitted, the $\overline{DRDY}$ line will go high turning off the SDATA and SCLK lines as per Figure 8a.

Write Operation

Data can be written to either the control register or calibration registers. In either case, the write operation is not affected by the $\overline{DRDY}$ line and the write operation does not have any effect on the status of $\overline{DRDY}$.

Figure 9a shows a write operation to the AD7711 with $\overline{TFS}$ remaining low for the duration of the write operation. A0 determines whether a write operation transfers data to the control register or to the calibration registers. This A0 signal must remain valid for the duration of the serial write operation. The falling edge of $\overline{TFS}$ enables the internally generated SCLK output. The serial data to be loaded to the AD7711 must be valid on the rising edge of this SCLK signal. Data is clocked into the AD7711 on the rising edge of the SCLK signal with the MSB transferred first. On the last active rising edge of SCLK, the LSB is loaded to the AD7711. Subsequent to the next falling edge of SCLK, the SCLK output is turned off. (The timing diagram of Figure 9a assumes a pull up resistor on the SCLK line.)

Figure 9b shows a timing diagram for a write operation to the AD7711 with $\overline{TFS}$ returning high during the write operation and returning low again to write the rest of the data word. Once again, the timing diagram of Figure 9b assumes a pull up resistor on the SCLK output. Timing parameters and functions are very similar to that outlined for Figure 9a, but Figure 9b has a number of additional times to show timing relationships when $\overline{TFS}$ returns high in the middle of transferring a word.

The falling edge of $\overline{TFS}$ again initiates the SCLK output and data to be loaded to the AD7711 must be valid prior to the rising edge of this SCLK signal. The rising edge of $\overline{TFS}$ turns off the SCLK output. $\overline{TFS}$ should return high during the low time of SCLK . When $\overline{TFS}$ returns low again, it turns on the SCLK output. When all data bits have been written to the device, the SCLK output is turned off as per Figure 9a.

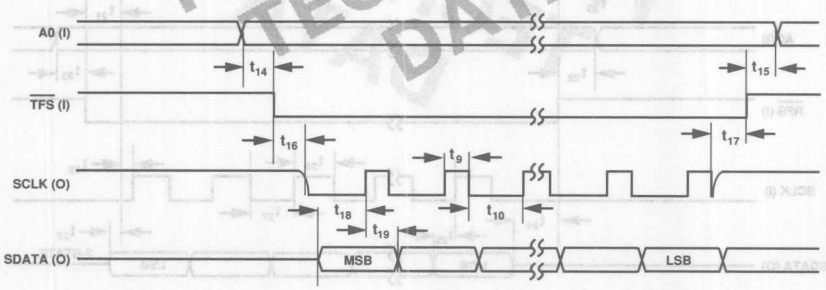


Figure 9a. Self-Clocking Mode, Control/Calibration Register Write Operation

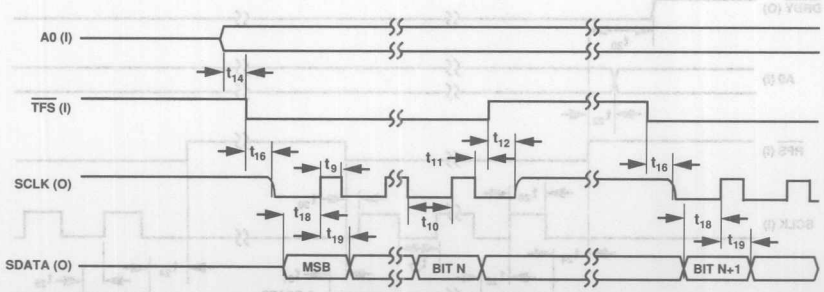


Figure 9b. Self-Clocking Mode, Control/Calibration Register Write Operation ($\overline{TFS}$ Returns High During Write Operation)

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External Clocking Mode

The AD7711 is configured for its external clocking mode by tying the MODE pin low. In this mode, SCLK of the AD7711 is configured as an input and an external serial clock must be provided to this SCLK pin. This external clocking mode is designed for direct interface to systems which provide a serial clock output that is synchronized to the serial data output, including microcontrollers such as the 80C51, 87C51, 68HC11 and 68HC05 and most digital signal processors.

Read Operation

Figures 10a and 10b show timing diagrams for reading from the AD7711 in the external clocking mode. Figure 10a shows a situation where all the data is read from the AD7711 in one read operation. Figure 10b shows a situation where the data is read from the AD7711 over a number of read operations.

As with the self-clocking mode, data can be read from either the output register, the control register or the calibration registers. A0 determines whether the data read accesses data from the control register or from the output/calibration registers. This A0 signal must remain valid for the duration of the serial read operation. The function of the $\overline{DRDY}$ line is dependent only on the output update rate of the device and the reading of the output data register. $\overline{DRDY}$ only goes low when a new data word is available in the output data register. It is reset high when the last bit of data (either 16th bit or 24th bit) is read from the output register. If a new data word becomes available to the output register while data is being read from the output register, $\overline{DRDY}$ will not indicate this and the new data word will be lost to the user. $\overline{DRDY}$ is not affected by reading from the control register or the calibration register.

Data can only be accessed from the output data register when $\overline{DRDY}$ is low. If $\overline{RFS}$ goes low while $\overline{DRDY}$ is high, the SDATA line will not become active until $\overline{DRDY}$ goes low. In this external clocking mode, an external clock is applied to the SCLK input. The receiving device (microprocessor or microcontroller) expects to see valid data on edges of this SCLK signal. However, with $\overline{DRDY}$ high SDATA is not active and no data is transmitted. $\overline{DRDY}$ does not have any effect on reading data from the control register or from the calibration registers.

Figure 10a shows a read operation to the AD7711 where $\overline{RFS}$ remains low for the duration of the data word transmission. With $\overline{DRDY}$ low, the $\overline{RFS}$ input is brought low. The input SCLK signal should be low between read and write operations. $\overline{RFS}$ going low places the MSB of the word to be read on the serial data line. All subsequent data bits are clocked out on a high to low transition of the serial clock and are valid prior to the following rising edge of this clock. The penultimate falling edge of SCLK clocks out the LSB and the final falling edge resets the $\overline{DRDY}$ line high. This rising edge of $\overline{DRDY}$ turns off the serial data output.

Figure 10b shows a timing diagram for a read operation where $\overline{RFS}$ returns high during the transmission of the word and re-

PRELIMINARY TECHNICAL DATA

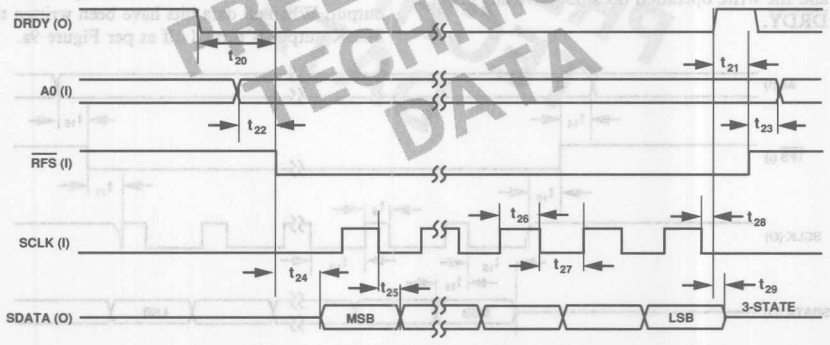


Figure 10a. External Clocking Mode, Output Data Read Operation

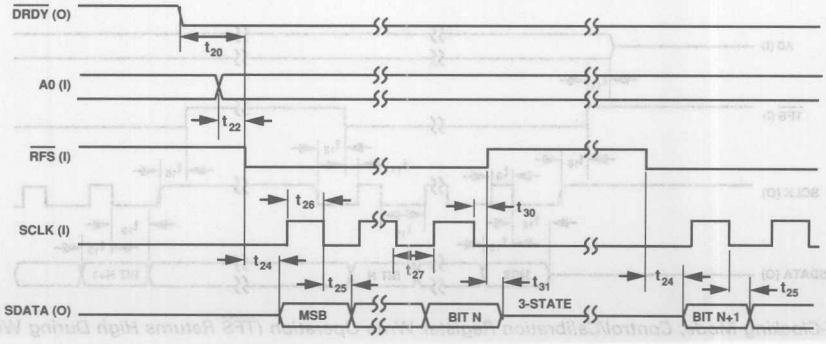


Figure 10b. External Clocking Mode, Output Data Read Operation ($\overline{RFS}$ Returns High During Read Operation)

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turns low again to access the rest of the data word. Timing parameters and functions are very similar to that outlined for Figure 10a but Figure 10b has a number of additional times to show timing relationships when $\overline{RFS}$ returns high in the middle of transferring a word.

$\overline{RFS}$ should return high during a low time of SCLK. On the rising edge of $\overline{RFS}$, the SDATA output is turned off. $\overline{DRDY}$ remains low and will remain low until all bits of the data word are read from the AD7711, regardless of the number of times $\overline{RFS}$ changes state during the read operation. When $\overline{RFS}$ returns low again, it activates the SDATA output and places the next bit of the data word on the SDATA output. When the entire word is transmitted, the $\overline{DRDY}$ line will go high turning off the SDATA output as per Figure 10a.

Write Operation

Data can be written to either the control register or calibration registers. In either case, the write operation is not affected by the $\overline{DRDY}$ line and the write operation does not have any effect on the status of $\overline{DRDY}$.

Figure 11a shows a write operation to the AD7711 with $\overline{TFS}$ remaining low for the duration of the write operation. A0 determines whether a write operation transfers data to the control register or to the calibration registers. This A0 signal must remain valid for the duration of the serial write operation. As before, the serial clock line should be low between read and write operations. The serial data to be loaded to the AD7711 must be valid on the high level of the externally applied SCLK signal. Data is clocked into the AD7711 on the high level of this SCLK signal with the MSB transferred first. On the last active rising edge of SCLK, the LSB is loaded to the AD7711.

Figure 11b shows a timing diagram for a write operation to the AD7711 with $\overline{TFS}$ returning high during the write operation and returning low again to write the rest of the data word. Timing parameters and functions are very similar to that outlined for Figure 11a, but Figure 11b has a number of additional times to show timing relationships when $\overline{TFS}$ returns high in the middle of transferring a word.

Data to be loaded to the AD7711 must be valid prior to the rising edge of the SCLK signal. $\overline{TFS}$ should return high during the low time of SCLK . After $\overline{TFS}$ returns low again, the next bit of the data word to be loaded to the AD7711 is clocked in on next high level of the SCLK input. On the last active rising edge of the SCLK input, the LSB is loaded to the AD7711 as per Figure 11a.

SIMPLIFYING THE INTERFACE

In some applications, the user may not require the facility of writing to the on-chip calibration registers. In this case, the serial interface to the AD7711 can be simplified by connecting the $\overline{TFS}$ line to the A0 input of the AD7711. This means that any write to the device will load data to the control register (since A0 is low while $\overline{TFS}$ is low) and any read to the device will access data from the output data register or from the calibration registers (since A0 is high while $\overline{RFS}$ is low). It should be noted that in this arrangement the user does not have the capability of reading from the control register.

PRELIMINARY TECHNICAL DATA

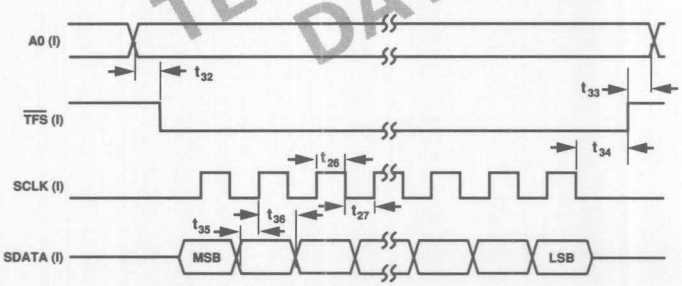


Figure 11a. External Clocking Mode, Control/Calibration Register Write Operation

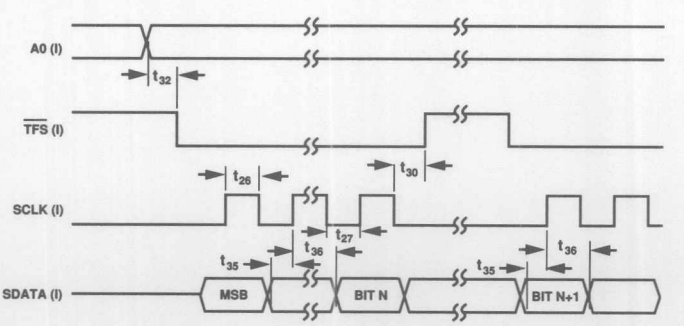
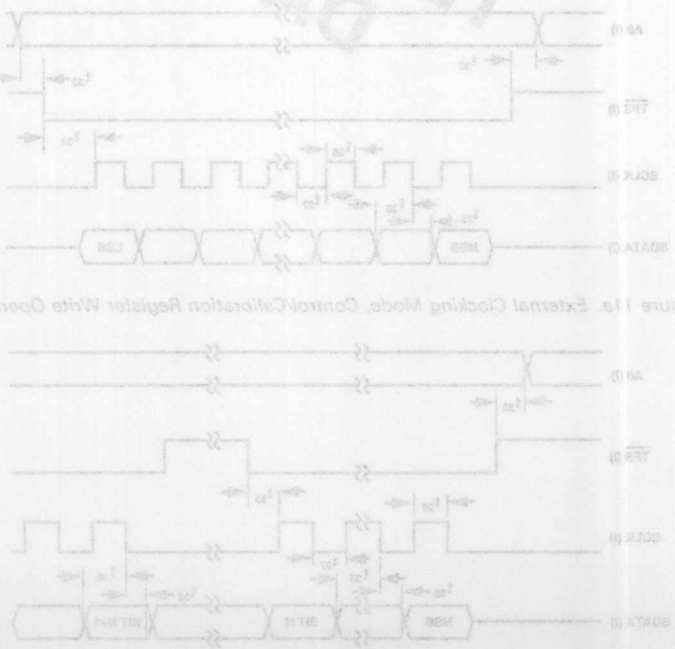


Figure 11b. External Clocking Mode, Control/Calibration Register Write Operation ($\overline{TFS}$ Returns High During Write Operation)

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AD7712*

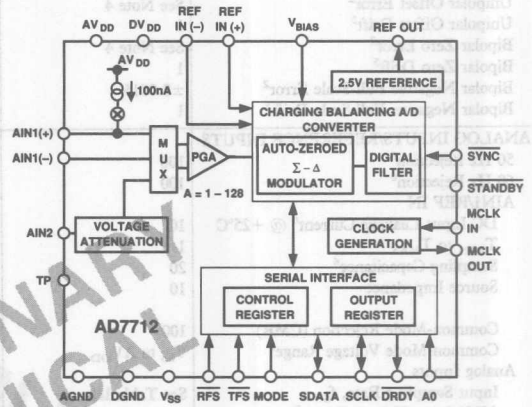
FEATURES

Charge Balancing ADC
21 Bits No Missing Codes
±0.0015% Nonlinearity
High Level and Low Level Analog Input Channels
Programmable Gain for Both Inputs
Gains from 1 to 128
Differential Input for Low Level Channel
Low-Pass Filter with Programmable Filter Cutoffs
Ability to Read/Write Calibration Coefficients
Bidirectional Microcontroller Serial Interface
Internal/ External Reference Option
Single or Dual Supply Operation
Low Power (25 mW typ) with Power-Down Mode (50 μW typ)

APPLICATIONS

Process Control
Smart Transmitters
Portable Industrial Instruments

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD7712 is a complete analog front end for low frequency measurement applications. The device has two analog input channels and accepts either low level signals directly from a transducer or high level ($\pm 4 \times V_{REF}$) signals and outputs a serial digital word. It employs a sigma-delta conversion technique to realize up to 21 bits of no missing codes performance. The low level input signal is applied to a proprietary programmable gain front end based around an analog modulator. The high-level analog input is attenuated before being applied to the same modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via the on-chip control register allowing adjustment of the filter cutoff and settling time.

Normally, one of the channels will be used as the main channel with the second channel used as an auxiliary input to periodically measure a second voltage. The part can be operated from a single supply (by tying the V_{SS} pin to AGND) provided that the input signals on the low level analog input are more positive than −30 mV. By taking the V_{SS} pin negative, the part can convert signals down to $-V_{REF}$ on this low level input. This low-level input, as well as the reference input, features differential input capability.

The AD7712 is ideal for use in smart, microcontroller based systems. Input channel selection, gain settings and signal polarity can be configured in software using the bidirectional serial port. The AD7712 also contains self-calibration, system calibration and background calibration options and also allows the user to read and to write the on-chip calibration registers.

CMOS construction ensures low power dissipation and a software programmable power-down mode reduces the standby power consumption to only 50 μW typical. The part is available in a 24-pin, 0.3 inch wide, plastic and hermetic dual-in-line package (DIP) as well as a 24-lead small outline (SOIC) package.

PRODUCT HIGHLIGHTS

1. The low level analog input channel allows the AD7712 to accept input signals directly from a strain gage or transducer, removing a considerable amount of signal conditioning. To maximize the flexibility of the part, the high level analog input accepts signals of $\pm 4 \times V_{REF}$/GAIN.
2. The AD7712 is ideal for microcontroller or DSP processor applications with an on-chip control register that allows control over filter cutoff level, input gain, channel selection, signal polarity and calibration modes.
3. The AD7712 allows the user to read and to write the on-chip calibration registers. This means that the microcontroller has much greater control over the calibration procedure.
4. No Missing Codes ensures true, usable, 21-bit dynamic range coupled with excellent ±0.0015% accuracy. The effects of temperature drift are eliminated by on-chip self-calibration, which removes zero scale and full-scale errors.

***Patent pending.**

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AD7712—SPECIFICATIONS

(AV_{DD} = +5 V to +10 V; DV_{DD} = +5 V; REF OUT = REF IN(+); REF IN(−) = AGND; MCLK IN = 10 MHz unless otherwise stated. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A, S Versions[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	21	Bits min	Guaranteed by Design
Output Noise	See Tables I & II		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity	±0.0015	% of FSR max	Filter Notches ≤ 60 Hz
Positive Full-Scale Error[2, 3]	See Note 4		Excluding Reference
Full-Scale Drift[5]	1	μV/°C max	Excluding Reference
Unipolar Offset Error[2]	See Note 4		
Unipolar Offset Drift[5]	1	μV/°C max	
Bipolar Zero Error[2]	See Note 4		
Bipolar Zero Drift[5]	1	μV/°C max	
Bipolar Negative Full-Scale Error[2]	±0.0015	% of FSR max	Excluding Reference; Typically ±0.0004%
Bipolar Negative Full-Scale Drift[5]	1	μV/°C max	Excluding Reference
ANALOG INPUTS/REFERENCE INPUTS			
50 Hz Rejection[6]	100	dB min	For Filter Notches of 10 Hz, 25 Hz, 50 Hz, $\pm 0.02 \times f_{NOTCH}$
60 Hz Rejection[6]	100	dB min	For Filter Notches of 10 Hz, 30 Hz, 60 Hz, $\pm 0.02 \times f_{NOTCH}$
AIN1/REF IN			
DC Input Leakage Current[6] @ +25°C	10	pA max	
T_{MIN} to T_{MAX}	1	nA max	
Sampling Capacitance[6]	20	pF max	
Source Impedance	10	kΩ max	Maximum Allowable Output Impedance of Whatever Is Driving Either Analog Input
Common-Mode Rejection (CMR)	100	dB min	At DC
Common-Mode Voltage Range[7]	V_{SS} to AV_{DD}	V min to V max	
Analog Inputs			
Input Sampling Rate, f_S	See Table III		
AIN1 Input Voltage Range[8]			For Normal Operation. Depends on Gain Selected
	0 to $+V_{REF}$[9]	V max	Unipolar Input Range (B/U Bit of Control Register = 0)
	$\pm V_{REF}$	V max	Bipolar Input Range (B/U Bit of Control Register = 1)
AIN2 Input Voltage Range			For Normal Operation. Depends on Gain Selected
	0 to $+4 \times V_{REF}$[9]	V max	Unipolar Input Range (B/U Bit of Control Register = 0)
	$\pm 4 \times V_{REF}$	V max	Bipolar Input Range (B/U Bit of Control Register = 1)
AIN2 dc Input Current	±300	μA max	AIN2 = ±10 V
Reference Inputs			
REF IN(+) − REF IN(−) Voltage	+2.5 to +5	V min to V max	For Specified Performance
Input Sampling Rate, f_S	$f_{CLK\ IN}/512$		
REFERENCE OUTPUT			
Output Voltage	2.5	V nom	
Initial Tolerance	±1	% max	
Drift	25	ppm/°C typ	
Line Regulation (AV_{DD})	1	mV/V max	
Load Regulation	1	mV/mA max	Maximum Load Current 1 mA
External Current	1	mA max	
V_{BIAS} INPUT			
Input Voltage Range	$AV_{DD} - 0.85 \times V_{REF}$	V max	See V_{BIAS} Input Section
	$V_{SS} + 0.85 \times V_{REF}$	V min	
LOGIC INPUTS			
Input Current	±10	μA max	
All Inputs Except MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	2.0	V min	
MCLK IN Only			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	3.5	V min	

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Parameter	A, S Versions[1]	Units	Conditions/Comments
LOGIC OUTPUTS			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 100 μA
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[10]	9	pF typ	
TRANSDUCER BURN-OUT			
Current	100	nA nom	
Initial Tolerance	±10	% typ	
Drift	100	ppm/°C typ	
SYSTEM CALIBRATION			
AIN1			
Positive Full-Scale Calibration Limit[11]	(1.05 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128).
Negative Full-Scale Calibration Limit[11]	−(1.05 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128).
Offset Calibration Limit[12, 13]	−(1.05 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128).
Input Span[12]	0.8 × V_{REF}/GAIN	V min	GAIN Is the Selected PGA Gain (Between 1 and 128).
	(2.1 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128).
AIN2			
Positive Full-Scale Calibration Limit[11]	(4.2 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128).
Negative Full-Scale Calibration Limit[11]	−(4.2 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128).
Offset Calibration Limit[13]	−(4.2 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128).
Input Span	3.2 × V_{REF}/GAIN	V min	GAIN Is the Selected PGA Gain (Between 1 and 128).
	(8.4 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128).
POWER REQUIREMENTS			
Power Supply Voltages			
AV_{DD} − V_{SS} Voltage	+5 to +10	V nom	±10% for Specified Performance
DV_{DD} Voltage	+5	V nom	±10% for Specified Performance
Power Supply Currents			
AV_{DD} Current	3	mA max	
DV_{DD} Current	4	mA max	
V_{SS} Current	1.5	mA max	V_{SS} = −5 V
Power Supply Rejection[14]			Rejection w.r.t. AGND. Assumes V_{BIAS} Is Fixed.
Positive Supply (AV_{DD})[15]	80	dB typ	
Negative Supply (V_{SS})	90	dB typ	
Power Dissipation			
Normal Mode	40	mW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = 0 V; Typically 25 mW
Normal Mode	45	mW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = −5 V; Typically 30 mW
Standby (Power-Down) Mode	100	μW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = 0 V or −5 V; Typically 50 μW

NOTES

[1]Temperature ranges are as follows: A Version, −40°C to +85°C; S Version −55°C to +125°C.

[2]Applies after calibration at the temperature of interest.

[3]Positive full-scale error applies to both unipolar and bipolar input ranges.

[4]These errors will be of the order of the output noise of the part, as shown in Table I.

[5]Recalibration at any temperature or use of the background calibration mode will remove these drift errors. These numbers are guaranteed by design and/or characterization.

[6]These numbers are guaranteed by design and/or characterization.

[7]This common-mode voltage range is allowed provided that the absolute value of the input voltage does not exceed AV_{DD} +30 mV and V_{SS} −30 mV.

[8]The AIN1 analog input presents a very high impedance dynamic load which varies with clock frequency and input sample rate. The maximum recommended source resistance is 10 kΩ.

[9]V_{REF} = REF IN(+) − REF IN(−).

[10]Sample tested at +25°C to ensure compliance.

[11]After calibration, if the analog input exceeds positive full scale, the converter will output all 1s. If the analog input is less than negative full scale, then the device will output all 0s.

[12]These calibration and span limits apply provided that the absolute voltage on the analog inputs does not exceed V_{DD} or does not go more negative than V_{SS} − 30 mV.

[13]The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.

[14]Measured at dc and applies in the selected passband. PSRR at 50 Hz will exceed 120 dB with filter notches of 10 Hz, 25 Hz or 50 Hz. PSRR at 60 Hz will exceed 120 dB with filter notches of 10 Hz, 30 Hz or 60 Hz.

[15]This number can be improved (to 95 dB typ) by deriving the V_{BIAS} voltage (via Zener diode or reference) from the AV_{DD} supply.

Specifications subject to change without notice.

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AV_{DD} to V_{SS}	−0.3 V to +12 V
AV_{DD} to AGND	−0.3 V to +12 V
AV_{DD} to DGND	−0.3 V to +12 V
DV_{DD} to AGND	−0.3 V to +6 V
DV_{DD} to DGND	−0.3 V to +6 V
V_{SS} to AGND	+0.3 V to −6 V
V_{SS} to DGND	+0.3 V to −6 V
AGND to DGND	−0.3 V to AV_{DD}+0.3 V
Analog Input Voltage to AGND	V_{SS}−0.3 V to AV_{DD}+0.3 V
Reference Input Voltage to AGND	V_{SS}−0.3 V to AV_{DD}+0.3 V
REF OUT to AGND	−0.3 V to AV_{DD}

Operating Temperature Range	
Commercial (A Version)	−40°C to +85°C
Extended (S Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C
Power Dissipation (Any Package) to +75°C	450 mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



TIMING CHARACTERISTICS[1, 2] (DV_{DD} = +5 V ± 10%; AV_{DD} = +5 V or +10 V ± 10%; V_{SS} = 0 V or −5 V ±10%; AGND = DGND = 0 V; f_{CLKIN} = 10 MHz; Input Logic 0 = 0 V, Logic 1 = DV_{DD}, unless otherwise stated.)

Parameter	Limit at T_{MIN}, T_{MAX} (A, S Versions)	Units	Conditions/Comments
$f_{CLK\ IN}$[3, 4]	400	kHz min	Master Clock Frequency: Internal Gate Oscillator
	12	MHz max	Typically 10 MHz; 10 MHz for Specified Performance
	400	kHz min	Master Clock Frequency: Externally Supplied
	10	MHz max	
$t_{CLK\ IN\ LO}$	0.2 × $t_{CLK\ IN}$	ns min	Master Clock Input Low Time
	0.8 × $t_{CLK\ IN}$	ns max	
$t_{CLK\ IN\ HI}$	0.2 × $t_{CLK\ IN}$	ns min	Master Clock Input High Time
	0.8 × $t_{CLK\ IN}$	ns max	
t_r[5]	50	ns max	Digital Output Rise Time; Typically 20 ns
t_f[5]	50	ns max	Digital Output Fall Time; Typically 20 ns
t_1	1000	ns min	$\overline{SYNC}$ Pulse Width
Self-Clocking Mode			
t_2	4 × $t_{CLK\ IN}$	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Setup Time. $t_{CLK\ IN}$ = 1/$f_{CLK\ IN}$
t_3	4 × $t_{CLK\ IN}$	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Hold Time
t_4	2 × $t_{CLK\ IN}$	ns min	A0 to $\overline{RFS}$ Setup Time
t_5	50	ns min	A0 to $\overline{RFS}$ Hold Time
t_6	4 × $t_{CLK\ IN}$	ns max	$\overline{RFS}$ Low to SCLK Falling Edge
t_7[6]	3 × $t_{CLK\ IN}$	ns max	Data Access Time ($\overline{RFS}$ Low to Data Valid)
t_8[6]	$t_{CLK\ IN}$/2	ns min	SCLK Falling Edge to Data Valid Delay
	$t_{CLK\ IN}$/2 + 20	ns max	
t_9	$t_{CLK\ IN}$/2	ns nom	SCLK High Pulse Width
t_{10}	3 × $t_{CLK\ IN}$/2	ns nom	SCLK Low Pulse Width
t_{11}	10	ns min	$\overline{RFS}$/$\overline{TFS}$ to SCLK Falling Edge Hold Time
	$t_{CLK\ IN}$/2	ns max	
t_{12}	20	ns max	$\overline{RFS}$/$\overline{TFS}$ to SCLK Delay
t_{13}[7]	20	ns max	$\overline{RFS}$ to Data Valid Hold Time
t_{14}	2 × $t_{CLK\ IN}$	ns min	A0 to $\overline{TFS}$ Setup Time
t_{15}	50	ns min	A0 to $\overline{TFS}$ Hold Time
t_{16}	4 × $t_{CLK\ IN}$	ns max	$\overline{TFS}$ to SCLK Falling Edge Delay Time
t_{17}	4 × $t_{CLK\ IN}$	ns min	$\overline{TFS}$ to SCLK Falling Edge Hold Time
t_{18}	20	ns min	Data Valid to SCLK Setup Time
t_{19}	20	ns min	Data Valid to SCLK Hold Time

PRELIMINARY TECHNICAL DATA

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Parameter	Limit at T_{MIN}, T_{MAX} (A, S Versions)	Units	Conditions/Comments
External Clocking Mode			
f_{SCLK}	$f_{CLK\ IN}/5$	MHz max	Serial Clock Input Frequency
t_{20}	$4 \times t_{CLK\ IN}$	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Setup Time
t_{21}	$4 \times t_{CLK\ IN}$	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Hold Time
t_{22}	$2 \times t_{CLK\ IN}$	ns min	A0 to $\overline{RFS}$ Setup Time
t_{23}	50	ns min	A0 to $\overline{RFS}$ Hold Time
t_{24}[6]	$3 \times t_{CLK\ IN}$	ns max	Data Access Time ($\overline{RFS}$ Low to Data Valid)
t_{25}[6]	$t_{CLK\ IN}/2$	ns min	SCLK Falling Edge to Data Valid Delay
	$t_{CLK\ IN}/2 + 20$	ns max	
t_{26}	$2 \times t_{CLK\ IN}$	ns min	SCLK High Pulse Width
t_{27}	$2 \times t_{CLK\ IN}$	ns min	SCLK Low Pulse Width
t_{28}	10	ns max	SCLK Falling Edge to $\overline{DRDY}$ High
t_{29}[7]	10	ns min	$\overline{DRDY}$ to Data Valid Hold Time
	20	ns max	
t_{30}	10	ns min	$\overline{RFS}$/$\overline{TFS}$ to SCLK Falling Edge Hold Time
	$t_{CLK\ IN}$	ns max	
t_{31}[7]	20	ns max	$\overline{RFS}$ to Data Valid Hold Time
t_{32}	$2 \times t_{CLK\ IN}$	ns min	A0 to $\overline{TFS}$ Setup Time
t_{33}	50	ns min	A0 to $\overline{TFS}$ Hold Time
t_{34}	10	ns max	SCLK Falling Edge to $\overline{TFS}$ Hold Time
t_{35}	20	ns min	Data Valid to SCLK Setup Time
t_{36}	20	ns min	Data Valid to SCLK Hold Time

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr= tf= 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]See Figures 9 to 12.

[3]CLK IN duty cycle range is 20% to 80%. CLK IN must be supplied whenever the AD7712 is not in STANDBY mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.

[4]The AD7712 is production tested with $f_{CLK\ IN}$ at 10 MHz. It is guaranteed by characterization to operate at 400 kHz.

[5]Specified using 10% and 90% points on waveform of interest.

[6]These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.4 V.

[7]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 100 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and, as such, are independent of external bus loading capacitances.

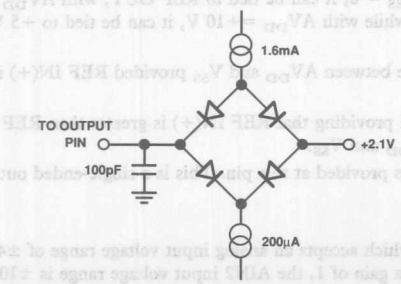
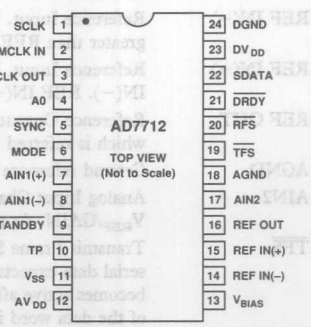


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

PIN CONFIGURATION
DIP and SOIC



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PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Function
1	SCLK	Serial Clock. Logic Input/Output depending on the status of the MODE pin. When MODE is high, the device is in its self-clocking mode and the SCLK pin provides a serial clock output. This SCLK becomes active when $\overline{RFS}$ or $\overline{TFS}$ goes low and it goes high impedance when either $\overline{RFS}$ or $\overline{TFS}$ returns high or when the device has completed transmission of an output word. When MODE is low, the device is in its external clocking mode and the SCLK pin acts as an input. This input serial clock can be a continuous clock with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to the AD7712 in smaller batches of data.
2	MCLK IN	Master Clock signal for the device. This can be provided in the form of a crystal or external clock. A crystal can be tied across the MCLK IN and MCLK OUT pins. Alternatively, the MCLK IN pin can be driven with a CMOS-compatible clock and MCLK OUT left unconnected. The clock input frequency is nominally 10 MHz.
3	MCLK OUT	When the master clock for the device is a crystal, the crystal is connected between MCLK IN and MCLK OUT.
4	A0	Address Input. With this input low, reading and writing to the device is to the control register. With this input high, access is to either the data register or the calibration registers.
5	$\overline{SYNC}$	Logic Input which allows for synchronization of the digital filters when using a number of AD7712s. It resets the nodes of the digital filter.
6	MODE	Logic Input. When this pin is high, the device is in its self-clocking mode; with this pin low, the device is in its external clocking mode.
7	AIN1(+)	Analog Input Channel 1. Positive input of the programmable gain differential analog input. The AIN1(+) input is connected to an output current source which can be used to check that an external transducer has burnt out or gone open circuit. This output current source can be turned on/off via the control register.
8	AIN1(−)	Analog Input Channel 1. Negative input of the programmable gain differential analog input.
9	$\overline{STANDBY}$	Logic Input. Taking this pin low shuts down the internal analog and digital circuitry, reducing power consumption to less than 50 μW.
10	TP	Test Pin. Used when testing the device. Do not connect anything to this pin.
11	V_{SS}	Analog Negative Supply, 0 to −5 V. Tied to AGND for single supply operation. The input voltage on AIN1 should not go > 30 mV negative w.r.t. V_{SS} for correct operation of the device.
12	AV_{DD}	Analog Positive Supply Voltage, +5 V to +10 V.
13	V_{BIAS}	Input Bias Voltage. This input voltage should be set such that $V_{BIAS} + V_{REF} < V_{DD}$ and $V_{BIAS} - V_{REF} > V_{SS}$ where V_{REF} is REF IN(+) − REF IN(−). Ideally, this should be tied halfway between AV_{DD} and V_{SS}. Thus, with AV_{DD} = +5 V and V_{SS} = 0, it can be tied to REF OUT; with AV_{DD} = +5 V and V_{SS} = −5 V, it can be tied to AGND, while with AV_{DD} = +10 V, it can be tied to +5 V or to REF OUT.
14	REF IN(−)	Reference Input. The REF IN(−) can lie anywhere between AV_{DD} and V_{SS} provided REF IN(+) is greater than REF IN(−).
15	REF IN(+)	Reference Input. The reference input is differential providing that REF IN(+) is greater than REF IN(−). REF IN(+) can lie anywhere between AV_{DD} and V_{SS}.
16	REF OUT	Reference Output. The internal +2.5 V reference is provided at this pin. This is a single-ended output which is referred to AGND.
17	AGND	Ground reference point for analog circuitry.
18	AIN2	Analog Input Channel 2. High-level analog input which accepts an analog input voltage range of ±4 × V_{REF}/GAIN. At the nominal V_{REF} of +2.5 V and a gain of 1, the AIN2 input voltage range is ±10 V.
19	$\overline{TFS}$	Transmit Frame Synchronization. Active low logic input used to write serial data to the device with serial data expected after the falling edge of this pulse. In the self-clocking mode, the serial clock becomes active after $\overline{TFS}$ goes low. In the external clocking mode, $\overline{TFS}$ must go low before the first bit of the data word is written to the part.

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Pin	Mnemonic	Function
20	$\overline{RFS}$	Receive Frame Synchronization. Active low logic input used to access serial data from the device. In the self-clocking mode, the SCLK and SDATA lines both become active after $\overline{RFS}$ goes low. In the external clocking mode, the SDATA line becomes active after $\overline{RFS}$ goes low.
21	$\overline{DRDY}$	Logic output. A falling edge indicates that a new output word is available for transmission. The $\overline{DRDY}$ pin will return high upon completion of transmission of a full output word. $\overline{DRDY}$ is also used to indicate when the AD7712 has completed its on-chip calibration sequence.
22	SDATA	Serial Data. Input/Output with serial data being written to the control register or accessed from the data registers. During a read operation, serial data becomes active after $\overline{RFS}$ goes low. During a write operation, valid serial data is expected on the rising edges of SCLK when $\overline{TFS}$ is low.
23	DV_{DD}	Digital Supply Voltage, +5 V. DV_{DD} should never exceed AV_{DD} by more than 0.3 V. If DV_{DD} powers up before AV_{DD}, or if DV_{DD} can exceed AV_{DD} by more than 0.3 V at any other time, a Schottky diode should be placed between the two pins.
24	DGND	Ground reference point for digital circuitry.

2

TERMINOLOGY

INTEGRAL NONLINEARITY

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and full scale, a point 0.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

POSITIVE FULL-SCALE ERROR

Positive full-scale error is the deviation of the last code transition (111 . . . 110 to 111 . . . 111) from the ideal input full-scale voltage. For AIN1(+), the ideal full-scale input voltage is (AIN1(−) + V_{REF}/GAIN −3/2 LSBs); for AIN2, the ideal full-scale voltage is +4 × V_{REF}/GAIN −3/2 LSBs. Positive Full-Scale Error applies to both unipolar and bipolar analog input ranges.

UNIPOLAR OFFSET ERROR

Unipolar offset error is the deviation of the first code transition from the ideal input voltage. For AIN1(+), the ideal input voltage is (AIN1(−) + 0.5 LSB); for AIN2, the ideal input is 0.5 LSB when operating in the unipolar mode.

BIPOLAR ZERO ERROR

This is the deviation of the midscale transition (0111 . . . 111 to 1000 . . . 000) from the ideal input voltage. For AIN1(+), the ideal input voltage is (AIN1(−) − 0.5 LSB); for AIN2, the ideal input voltage is −0.5 LSB when operating in the bipolar mode.

BIPOLAR NEGATIVE FULL-SCALE ERROR

This is the deviation of the first code transition from the ideal input voltage. For AIN1(+), the ideal input voltage is (AIN1(−) −V_{REF}/GAIN + 0.5 LSB); for AIN2, the ideal input voltage is (−4 × V_{REF}/GAIN+0.5 LSB) when operating in the bipolar mode.

POSITIVE FULL-SCALE OVERRANGE

Positive Full-Scale Overrange is the amount of overhead available to handle input voltages on AIN1(+) input greater than (AIN1(−) +V_{REF}/GAIN) or on AIN2 of greater than +4 × V_{REF}/GAIN (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or to overflowing the digital filter.

NEGATIVE FULL-SCALE OVERRANGE

This is the amount of overhead available to handle voltages on AIN1(+) below (AIN(−) −V_{REF}/GAIN) or on AIN2 below −4 × V_{REF}/GAIN without overloading the analog modulator or overflowing the digital filter. Note that the analog input will accept negative voltage peaks on AIN1(+) even in the unipolar mode provided that AIN1(+) is greater than AIN1(−) and greater than V_{SS} −30 mV.

OFFSET CALIBRATION RANGE

In the system calibration modes, the AD7712 calibrates its offset with respect to the analog input. The offset calibration range specification defines the range of voltages that the AD7712 can accept and still calibrate offset accurately.

FULL-SCALE CALIBRATION RANGE

This is the range of voltages that the AD7712 can accept in the system calibration mode and still calibrate full-scale correctly.

INPUT SPAN

In system calibration schemes, two voltages applied in sequence to the AD7712's analog input define the analog input range. The input span specification defines the minimum and maximum input voltages from zero to full scale that the AD7712 can accept and still calibrate gain accurately.

PRELIMINARY TECHNICAL DATA

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A write to the device with the A0 input low writes data to the control register. A read to the device with the A0 input low accesses the contents of the control register.

MD2	MD1	MD0	G2	G1	G0	CH	PD	WL	X	BO	B/U

FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0

X = Don't Care.

Operating Mode

MD2	MD1	MD0	Operating Mode
0	0	0	Normal Mode. This is the normal mode of operation of the device whereby a read to the device accesses data from the data register. This is the default condition of these bits after the internal power-on reset.
0	0	1	Activate Self-Calibration. This activates self-calibration on the channel selected by CH. This is a one-step calibration sequence, and when complete the part returns to Normal Mode. The $\overline{DRDY}$ output indicates when this self-calibration is complete. For this calibration type, the zero scale calibration is done internally on AGND and the full-scale calibration is done internally on V_{REF}.
0	1	0	Activate System Calibration. This activates system calibration on the channel selected by CH. This is a two-step calibration sequence, with the zero scale calibration done first on the selected input channel and $\overline{DRDY}$ indicating when this zero scale calibration is complete. The part returns to Normal Mode at the end of this first step in the two-step sequence.
0	1	1	Activate System Calibration. This is the second step of the system calibration sequence with full-scale calibration being performed on the selected input channel. Once again, $\overline{DRDY}$ indicates when the full-scale calibration is complete. When this calibration is complete, the part returns to Normal Mode.
1	0	0	Activate System Offset Calibration. This activates system offset calibration on the channel selected by CH. This is a one-step calibration sequence; the part returns to Normal Mode with $\overline{DRDY}$ indicating when this system offset calibration is complete. For this calibration type, the zero scale calibration is done on the selected input channel and the full-scale calibration is done internally on V_{REF}.
1	0	1	Activate Background Calibration. This activates background calibration on the channel selected by CH. If the background calibration mode is on, then the AD7712 provides continuous self-calibration of the reference and AGND. This calibration takes place as part of the conversion sequence, extending the conversion time and reducing the word rate by a factor of six. Its major advantage is that the user does not have to worry about recalibrating the device when there is a change in the ambient temperature. In this mode, AGND and V_{REF}, as well as the analog input voltage, are continuously monitored and the calibration registers of the device are automatically updated, if necessary.
1	1	0	Read/Write Zero Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the zero scale calibration coefficients of the channel selected by CH. A write to the device with A0 high writes data to the zero scale calibration coefficients of the channel selected by CH. The word length for reading and writing these coefficients is 24 bits, regardless of the status of the WL bit of the control register.
1	1	1	Read/Write Full-Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the full-scale calibration coefficients of the channel selected by CH. A write to the device with A0 high writes data to the full-scale calibration coefficients of the channel selected by CH. The word length for reading and writing these coefficients is 24 bits regardless, of the status of the WL bit of the control register.

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PGA Gain

G2	G1	G0	Gain	
0	0	0	1	(Default Condition After the
0	0	1	2	Internal Power-On Reset)
0	1	0	4	
0	1	1	8	
1	0	0	16	
1	0	1	32	
1	1	0	64	
1	1	1	128	

Channel Selection

CH	Channel		
0	AIN1	Low Level Input	(Default Condition After the
1	AIN2	High Level Input	Internal Power-On Reset)

Power-Down

PD		
0	Normal Operation	(Default Condition After the
1	Power-Down	Internal Power-On Reset)

Word Length

WL	Output Word Length	
0	16-Bit	(Default Condition After
1	24-Bit	Internal Power-On Reset)

Burn-Out Current

BO		
0	Off	(Default Condition After
1	On	Internal Power-On Reset)

Bipolar/Unipolar Selection

B/U		
0	Bipolar	(Default Condition After
1	Unipolar	Internal Power-On Reset)

Filter Selection (FS11–FS0)

The on-chip digital filter provides a $Sinc^3$ (or $(Sinx/x)^3$ filter response. The 12 bits of data programmed into these bits determine the filter cutoff frequency, the position of the first notch of the filter and the data rate for the part. In association with the gain selection, it also determines the output noise (and hence the effective resolution) of the device.

The first notch of the filter occurs at a frequency determined by the relationship: filter first notch frequency = $(f_{CLK\ IN}/512)/code$ where *code* is the decimal equivalent of the code in bits FS0 to FS11 and is in the range 19 to 2,000. With the nominal $f_{CLK\ IN}$ of 10 MHz, this results in a first notch frequency range from 9.76 Hz to 1.028 kHz. To ensure correct operation of the AD7712, the value of the code loaded to these bits must be within this range. Failure to do this will result in unspecified operation of the device.

Changing the filter notch frequency, as well as the selected gain, impacts resolution. Tables I and II and Figure 2 show the effect of the filter notch frequency and gain on the effective resolution of the AD7712. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 50 Hz, then a new word is available at a 50 Hz rate or every 20 ms. If the first notch is at 1 kHz, a new word is available every 1 ms.

The settling time of the filter to a full-scale step input change is worst case 4× the data rate. For example, with the first filter notch at 50 Hz, the settling time of the filter to a full-scale step input change is 80 ms max. If the first notch is at 1 kHz, the settling time of the filter to a full-scale input step is 4 ms max.

The −3 dB frequency is determined by the programmed first notch frequency according to the relationship: filter −3 dB frequency = 0.262 × first notch frequency.

Table I shows the output rms noise for some typical notch and −3 dB frequencies. The numbers given are for the bipolar input ranges with a V_{REF} of +2.5 V. The numbers in Table I are guaranteed by a combination of testing, characterization and design. The output noise from the part comes from two sources, the quantization noise from the analog-to-digital conversion process and device noise. Device noise is independent of gain and essentially flat across the frequency spectrum. Quantization noise is ratiometric to the input full-scale (and hence gain) and its frequency response is shaped by the modulator.

Looking at Table I, as the cutoff frequency increases, the output noise increases because more of the quantization noise of the part comes through to the output and, hence, the output noise increases with increasing −3 dB frequencies. For the lower notch settings, the output noise is dominated by the device noise and, hence, altering the gain has little effect on the output noise. At higher notch frequencies, the quantization noise dominates the output noise and, in this case, the output noise tends to decrease with increasing gain.

Since the output noise comes from two sources, the effective resolution of the device (i.e., the ratio of the output rms noise to the input full scale) does not remain constant with increasing gain or with increasing bandwidth. Table II shows the same table as Table I except that the output is now expressed in terms of effective resolution (the magnitude of the rms noise with respect to 2 × V_{REF}/GAIN, i.e., the input full scale). It is possible to do post filtering on the device to improve the output data rate for a given −3 dB frequency and also to reduce further the output noise (see Digital Filtering section).

Figure 2 gives similar information to that outlined in Table I. In this plot, the output rms noise is shown for the full range of available cutoff frequencies rather than for some typical cutoff frequencies as in Tables I and II. The numbers given in this plot are typical values.

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Table I. Output Noise vs. Gain and First Notch Frequency

First Notch of Filter and O/P Data Rate[1]	Output RMS Noise (μV)								
	−3 dB Frequency	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
10 Hz[2]	2.62 Hz	1.7	0.84	0.60	0.42	0.42	0.42	0.42	0.42
25 Hz[2]	6.55 Hz	3.4	1.7	1.2	0.60	0.60	0.60	0.60	0.60
30 Hz[2]	7.86 Hz	3.4	2.4	1.2	0.84	0.84	0.60	0.60	0.60
50 Hz[2]	13.1 Hz	9.5	4.8	2.4	1.7	1.2	0.84	0.84	0.84
60 Hz[2]	15.72 Hz	13.5	6.7	3.4	1.7	1.2	1.2	0.84	0.84
100 Hz[3]	26.2 Hz	54	27	13.5	6.7	3.4	1.7	1.7	1.2
250 Hz[3]	65.5 Hz	432	216	108	54	27	13.5	6.7	4.8
500 Hz[3]	131 Hz	2.4×10^3	1.2×10^3	610	305	153	76	38	19
1 kHz[3]	262 Hz	13.8×10^3	6.9×10^3	3.4×10^3	1.7×10^3	863	432	216	108

NOTES
[1]The default condition (after the internal power-on reset) for the first notch of filter is 60 Hz.
[2]For these filter notch frequencies, the output rms noise is primarily independent of the value of the reference voltage. Therefore, increasing the reference voltage will give an increase in the effective resolution of the device (i.e., the ratio of the rms noise to the input full scale is increased since the output rms noise remains constant as the input full-scale increases).
[3]For these filter notch frequencies, the output rms noise is proportional to the value of the reference voltage.

Table II. Effective Resolution vs. Gain and First Notch Frequency

First Notch of Filter and O/P Data Rate	Effective Resolution[1] (Bits)								
	−3 dB Frequency	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
10 Hz	2.62 Hz	21.5	21.5	21	20.5	19.5	18.5	17.5	16.5
25 Hz	6.55 Hz	20.5	20.5	20	20	19	18	17	16
30 Hz	7.86 Hz	20.5	20	20	19.5	18.5	18	17	16
50 Hz	13.1 Hz	19	19	19	18.5	18	17.5	16.5	15.5
60 Hz	15.72 Hz	18.5	18.5	18.5	18.5	18	17	16.5	15.5
100 Hz	26.2 Hz	16.5	16.5	16.5	16.5	16.5	16.5	15.5	15
250 Hz	65.5 Hz	13.5	13.5	13.5	13.5	13.5	13.5	13.5	13
500 Hz	131 Hz	11	11	11	11	11	11	11	11
1 kHz	262 Hz	8.5	8.5	8.5	8.5	8.5	8.5	8.5	8.5

NOTE
[1]Effective resolution is defined as the magnitude of the output rms noise to the input full scale (i.e., $2 \times V_{REF}$/GAIN). The above table applies for a V_{REF} of +2.5 V and resolution numbers are rounded to the nearest 0.5 LSB.

PRELIMINARY TECHNICAL DATA

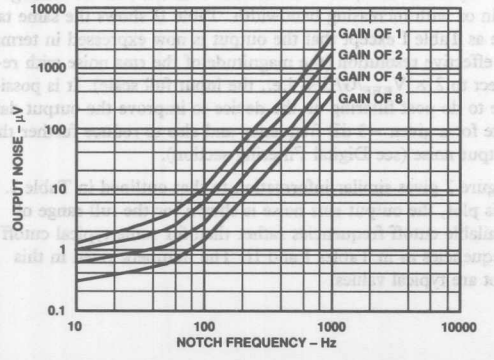


Figure 2a. Plot of Output Noise vs. Gain and Notch Frequency (Gains of 1 to 8)

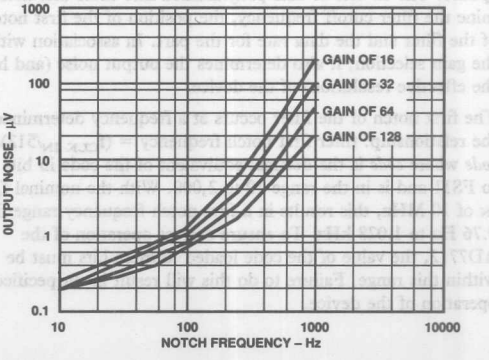


Figure 2b. Plot of Output Noise vs. Gain and Notch Frequency (Gains of 16 to 128)

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CIRCUIT DESCRIPTION

The AD7712 is a sigma-delta A/D converter with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals such as those in industrial control or process control applications. It contains a sigma-delta (or charge-balancing) ADC, a calibration microcontroller with on-chip static RAM, a clock oscillator, a digital filter and a bidirectional serial communications port.

The part contains two analog input channels, one programmable gain differential input and one programmable gain high-level single-ended input. The gain range on both inputs is from 1 to 128. For the AIN1 input, this means that the input can accept unipolar signals of between 0 to +20 mV and 0 to +2.5 V or bipolar signals in the range from ±20 mV to ±2.5 V when the reference input voltage equals +2.5 V. The input voltage range for the AIN2 input is $\pm 4 \times V_{REF}/GAIN$ and is ±10 V with the nominal reference of +2.5 V and a gain of 1. The input signal to the selected analog input channel is continuously sampled at a rate determined by the frequency of the master clock, CLK IN, and the selected gain (see Table III). A charge balancing A/D converter (Sigma-Delta Modulator) converts the sampled signal into a digital pulse train whose duty cycle contains the digital information. The programmable gain function on the analog input is also incorporated in this sigma-delta modulator with the input sampling frequency being modified to give the higher gains. A sinc^3 digital low pass filter processes the output of the sigma-delta modulator and updates the output register at a rate determined by the first notch frequency of this filter. The output data can be read from the serial port randomly or periodically at any rate up to the output register update rate. The first notch of this digital filter (and hence its −3 dB frequency) can be programmed via an on-chip control register. The programmable range for this first notch frequency is from 9.76 Hz to 1.028 kHz, giving a programmable range for the −3 dB frequency of 2.58 Hz to 269 Hz.

The basic connection diagram for the part is shown in Figure 3. This shows the AD7712 in the external clocking mode with both the AV_{DD} and DV_{DD} pins of the AD7712 being driven from the analog +5 V supply. Some applications will have separate supplies for both AV_{DD} and DV_{DD}, and in some of these cases, the analog supply will exceed the +5 V digital supply (see Power Supplies and Grounding section).

The AD7712 provides a number of calibration options which can be programmed via the on-chip control register. A calibration cycle may be initiated at any time by writing to this control register. The part can perform self-calibration using the on-chip calibration microcontroller and SRAM to store calibration parameters. Other system components may also be included in the calibration loop to remove offset and gain errors in the input channel using the system calibration mode. Another option is a background calibration mode where the part continuously performs self-calibration and updates the calibration coefficients. Once the part is in this mode, the user does not have to worry about issuing periodic calibration commands to the device or asking the device to recalibrate when there is a change in the ambient temperature or power supply voltage.

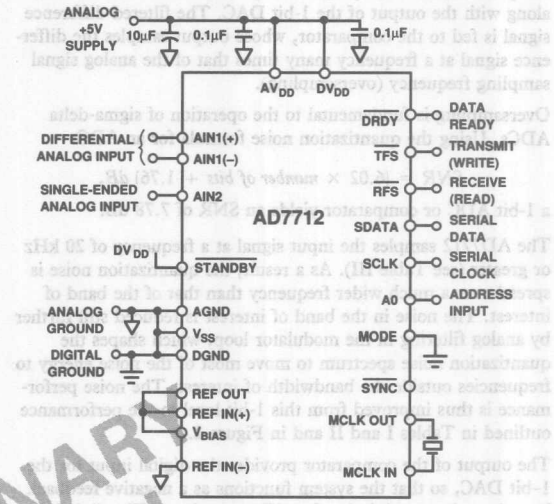


Figure 3. Basic Connection Diagram

The AD7712 gives the user access to the on-chip calibration registers allowing the microprocessor to read the device's calibration coefficients and also to write its own calibration coefficients to the part. This gives the microprocessor much greater control over the AD7712's calibration procedure. It also means that the user can verify that the device has performed its calibration correctly by comparing the coefficients after calibration with prestored values in E^{2}PROM.

The AD7712 can be operated in single supply systems provided that the analog input voltage on the AIN1 input does not go more negative than 30 mV. For larger bipolar signals on the AIN1 input, a V_{SS} of −5 V is required by the part. For battery operation, the AD7712 also offers a software programmable standby mode that reduces idle power consumption to typically 50 µW.

THEORY OF OPERATION

The general block diagram of a sigma-delta ADC is shown in Figure 4. It contains the following elements.

1. A sample-hold amplifier.
2. A differential amplifier or subtractor.
3. An analog low-pass filter.
4. A 1-bit A/D converter (comparator).
5. A 1-bit DAC.
6. A digital low-pass filter.

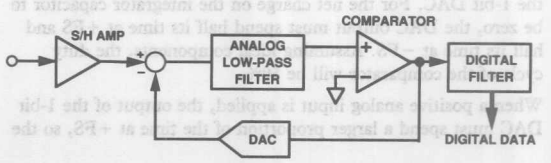


Figure 4. General Sigma-Delta ADC

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along with the output of the 1-bit DAC. The filtered difference signal is fed to the comparator, whose output samples the difference signal at a frequency many times that of the analog signal sampling frequency (oversampling).

Oversampling is fundamental to the operation of sigma-delta ADCs. Using the quantization noise formula for an ADC:

$$SNR = (6.02 \times number\ of\ bits + 1.76)\ dB,$$

a 1-bit ADC or comparator yields an SNR of 7.78 dB.

The AD7712 samples the input signal at a frequency of 20 kHz or greater (see Table III). As a result, the quantization noise is spread over a much wider frequency than that of the band of interest. The noise in the band of interest is reduced still further by analog filtering in the modulator loop, which shapes the quantization noise spectrum to move most of the noise energy to frequencies outside the bandwidth of interest. The noise performance is thus improved from this 1-bit level to the performance outlined in Tables I and II and in Figure 2.

The output of the comparator provides the digital input for the 1–bit DAC, so that the system functions as a negative feedback loop that tries to minimize the difference signal. The digital data that represents the analog input voltage is contained in the duty cycle of the pulse train appearing at the output of the comparator. It can be retrieved as a parallel binary data word using a digital filter.

Sigma-delta ADCs are generally described by the order of the analog low pass filter. A simple example of a first order sigma-delta ADC is shown in Figure 5. This contains only a first-order low pass filter or integrator. It also illustrates the derivation of the alternative name for these devices : Charge Balancing ADCs.

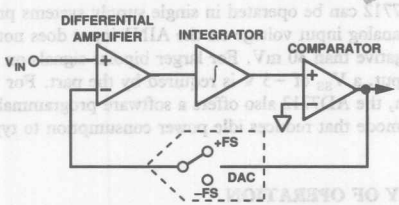


Figure 5. Basic Charge Balancing ADC

It consists of a differential amplifier (whose output is the difference between the analog input and the output of a 1-bit DAC), an integrator and a comparator. The term, "charge-balancing," comes from the fact that this system is a negative feedback loop that tries to keep the net charge on the integrator capacitor at zero by balancing charge injected by the input voltage with charge injected by the 1-bit DAC. When the analog input is zero, the only contribution to the integrator output comes from the 1-bit DAC. For the net charge on the integrator capacitor to be zero, the DAC output must spend half its time at +FS and half its time at −FS. Assuming ideal components, the duty cycle of the comparator will be 50%.

When a positive analog input is applied, the output of the 1-bit DAC must spend a larger proportion of the time at +FS, so the voltage is applied, the duty cycle decreases.

The AD7712 uses a second-order sigma-delta modulator and a digital filter that provides a rolling average of the sampled output. After power-up, or if there is a step change in the input voltage, there is a settling time that must elapse before valid data is obtained.

Input Sample Rate

The modulator sample frequency for the device remains at $f_{CLK\ IN}/512$ (20 kHz @ $f_{CLK\ IN}$ = 10 MHz) regardless of the selected gain. However, gains greater than ×1 are achieved by a combination of multiple input samples per modulator cycle and a scaling of the ratio of reference capacitor to input capacitor. As a result of the multiple sampling, the input sample rate of the device varies with the selected gain (see Table III). The effective input impedance is $1/C \cdot f_S$ where C is the input sampling capacitance and f_S is the input sample rate.

Table III. Input Sampling Frequency vs. Gain

Gain	Input Sampling Frequency (f_S)
1	$f_{CLK\ IN}/512$ (20 kHz @ $f_{CLK\ IN}$ = 10 MHz)
2	$2 \times f_{CLK\ IN}/512$ (40 kHz @ $f_{CLK\ IN}$ = 10 MHz)
4	$4 \times f_{CLK\ IN}/512$ (80 kHz @ $f_{CLK\ IN}$ = 10 MHz)
8	$4 \times f_{CLK\ IN}/512$ (160 kHz @ $f_{CLK\ IN}$ = 10 MHz)
16	$4 \times f_{CLK\ IN}/512$ (160 kHz @ $f_{CLK\ IN}$ = 10 MHz)
32	$4 \times f_{CLK\ IN}/512$ (160 kHz @ $f_{CLK\ IN}$ = 10 MHz)
64	$4 \times f_{CLK\ IN}/512$ (160 kHz @ $f_{CLK\ IN}$ = 10 MHz)
128	$4 \times f_{CLK\ IN}/512$ (160 kHz @ $f_{CLK\ IN}$ = 10 MHz)

DIGITAL FILTERING

The AD7712's digital filter behaves like a similar analog filter, with a few minor differences.

First, since digital filtering occurs after the A-to-D conversion process, it can remove noise injected during the conversion process. Analog filtering cannot do this.

On the other hand, analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. Digital filtering cannot do this and noise peaks riding on signals near full-scale have the potential to saturate the analog modulator and digital filter, even though the average value of the signal is within limits. To alleviate this problem, the AD7712 has overrange headroom built into the sigma-delta modulator and digital filter which allows overrange excursions of 5% above the analog input range. If noise signals are larger than this, consideration should be given to analog input filtering, or to reducing the input channel voltage so that its full scale is half that of the analog input channel full scale. This will provide an overrange capability greater than 100% at the expense of reducing the dynamic range by 1 bit (50%).

Filter Characteristics

The cutoff frequency of the digital filter is determined by the value loaded to bits FS0 to FS11 in the control register. At the maximum clock frequency of 10 MHz, the minimum cutoff frequency of the filter is 2.58 Hz while the maximum programmable cutoff frequency is 269Hz.

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Figure 6 shows the filter frequency response for a cutoff frequency of 2.62 Hz which corresponds to a first filter notch frequency of 10 Hz. This is a $(\sin x/x)^3$ response (also called sinc^3) that provides >100 dB of 50 Hz and 60 Hz rejection. Programming a different cutoff frequency via FS0–FS11 does not alter the profile of the filter response, it changes the frequency of the notches as outlined in the Control Register section.

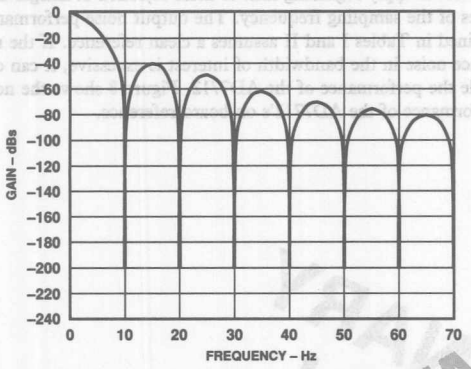


Figure 6. Frequency Response of AD7712 Filter

Since the AD7712 contains this on-chip, low pass filtering, there is a settling time associated with step function inputs and data on the output will be invalid after a step change until the settling time has elapsed. The settling time depends upon the notch frequency chosen for the filter. The output data rate equates to this filter notch frequency and the settling time of the filter to a full-scale step input is 4 times the output data period. In applications using both input channels, the settling time of the filter must be allowed to elapse before data from the second channel is accessed.

Post Filtering

The on-chip modulator provides samples at a 20 kHz output rate. The on-chip digital filter decimates these samples to provide data at an output rate which corresponds to the programmed first notch frequency of the filter. Since the output data rate exceeds the Nyquist criterion, the output rate for a given bandwidth will satisfy most application requirements. However, there may be some applications which require a higher data rate for a given bandwidth and noise performance. Applications which need this higher data rate will require some post filtering following the digital filter of the AD7712.

For example, if the required bandwidth is 7.86 Hz but the required update rate is 100 Hz, the data can be taken from the AD7712 at the 100 Hz rate giving a −3 dB bandwidth of 26.2 Hz. Post filtering can be applied to this to reduce the bandwidth and output noise, to the 7.86 Hz bandwidth level, while maintaining an output rate of 100 Hz.

Post filtering can also be used to reduce the output noise from the device for bandwidths below 2.62 Hz. At a gain of 128, the output rms noise is 420 nV. This is essentially device noise or white noise, and since the input is chopped, the noise has a flat frequency response. By reducing the bandwidth below 2.62 Hz, the noise in the resultant passband can be reduced. A reduction in bandwidth by a factor of 2 results in a $\sqrt{2}$ reduction in the output rms noise. This additional filtering will result in a longer settling time.

Antialias Considerations

The digital filter does not provide any rejection at integer multiples of the modulator sample frequency (n × 20 kHz, where n = 1, 2, 3 . . .). This means that there are frequency bands, $\pm f_{3\ dB}$ wide ($f_{3\ dB}$ is cutoff frequency selected by FS0 to FS11) where noise passes unattenuated to the output. However, due to the AD7712's high oversampling ratio, these bands occupy only a small fraction of the spectrum and most broadband noise is filtered. In any case, because of the high oversampling ratio a simple, RC, single pole filter is generally sufficient to attenuate the signals in these bands on the analog input and thus provide adequate antialiasing filtering.

ANALOG INPUT FUNCTIONS

Analog Input Ranges

The analog inputs on the AD7712 provide the user with considerable flexibility in terms of analog input voltage ranges. One of the inputs is a differential, programmable gain, input channel which can handle either unipolar or bipolar input signals. The common mode range of this input is from V_{SS} to AV_{DD} provided that the absolute value of the analog input voltage lies between V_{SS} −30 mV and AV_{DD} +30 mV. The second analog input is a single-ended, programmable gain high level input which accepts analog input ranges of 0 to $+4 \times V_{REF}/GAIN$ or $\pm 4 \times V_{REF}/GAIN$.

The input sample rate for the part varies as per Table III. For the AIN1 input, the input sampling capacitance is 15 pF typical. The effective input impedance of this AIN1 input is $1/C \cdot f_S$ and this results in a maximum allowable source impedance of whatever is driving the AIN1 analog input of 10 kΩ to ensure correct charging of the sampling capacitor. The AIN2 input is connected to a restive attenuation network and has a nominal input resistance of 44 kΩ (see Figure 7). The AIN2 input should be driven from a low impedance source.

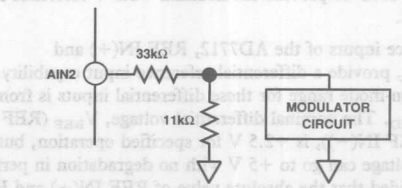


Figure 7. AIN2 Input Attenuation Circuit

The dc input leakage current on the AIN1 input is 10 pA maximum at +25°C. This results in a dc offset voltage developed across the source impedance. However, this dc offset effect can be compensated for by a combination of the differential input capability of the part and its system calibration mode. The dc input current on the AIN2 input depends on the input voltage, For the nominal input voltage range of ±10 V, the input current is ±225 μA typ.

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Burn-Out Current

The AIN1(+) input of the AD7712 contains a 100 nA current source which can be turned on/off via the control register. This current source can be used in checking that a transducer has not burnt out or gone open circuit before attempting to take measurements on that channel. If the current is turned on and is allowed flow into the transducer and a measurement of the input voltage on the AIN1 input is taken, it can indicate that the transducer is not functioning correctly. For normal operation, this burn-out current is turned off by writing a 0 to the BO bit in the control register.

Bipolar/Unipolar Inputs

The two analog inputs on the AD7712 can accept either unipolar or bipolar input voltage ranges. Bipolar or unipolar options are chosen by programming the B/U bit of the control register. This programs both channels for either unipolar or bipolar operation. Programming the part for either unipolar or bipolar operation does not change any of the input signal conditioning; it simply changes the data output coding.

The AIN1 input channel is differential and, as a result, the voltage to which the unipolar and bipolar signals are referenced is the voltage on the AIN1(−) input. For example, if AIN1(−) is +1.25 V and the AD7712 is configured for unipolar operation with a gain of 1 and a V_{REF} of +2.5 V, the input voltage range on the AIN1(+) input is +1.25 V to +3.75 V. If AIN1(−) is +1.25 V and the AD7712 is configured for bipolar mode with a gain of 1 and a V_{REF} of +2.5 V, the analog input range on the AIN1(+) input is −1.25 V to +3.75 V. For the AIN2 input, the input signals are referenced to AGND.

REFERENCE INPUT/OUTPUT

The AD7712 contains a temperature compensated +2.5 V reference which has an initial tolerance of ±25 mV. This reference voltage is provided at the REF OUT pin and it can be used as the reference voltage for the part by connecting the REF OUT pin to the REF IN(+) pin. This REF OUT pin is a single-ended output, referenced to AGND, which is capable of providing up to 1 mA to an external load. In applications where REF OUT is connected directly to REF IN(+), REF IN(−) should be tied to AGND to provide the nominal +2.5 V reference for the AD7712.

The reference inputs of the AD7712, REF IN(+) and REF IN(−), provide a differential reference input capability. The common-mode range for these differential inputs is from V_{SS} to AV_{DD}. The nominal differential voltage, V_{REF} (REF IN(+) −REF IN(−)), is +2.5 V for specified operation, but the reference voltage can go to +5 V with no degradation in performance provided that the absolute value of REF IN(+) and REF IN(−) does not exceed its AV_{DD} and V_{SS} limits. REF IN(+) must always be greater than REF IN(−) for correct operation of the AD7712.

Both reference inputs provide a high impedance, dynamic load similar to the AIN1 analog input. The maximum dc input leakage current is 10 pA (±1 μA over temperature) and source resistances will result in gain errors on the part. The reference inputs are switched capacitor inputs with the input capacitance dependent upon the selected gain. For gains of 1 to 8 the input capacitance is 20 pF; for a gain of 16 it is 10 pF; for a gain of 32 it is 5 pF; for a gain of 64 it is 2.5 pF; and for a gain of 128 it is 1.25 pF.

The digital filter of the AD7712 removes noise from the reference input just as it does with the analog input, and the same limitations apply regarding lack of noise rejection at integer multiples of the sampling frequency. The output noise performance outlined in Tables I and II assumes a clean reference. If the reference noise in the bandwidth of interest is excessive, it can degrade the performance of the AD7712. Figure 8 shows the noise performance of the AD7712's on-board reference.

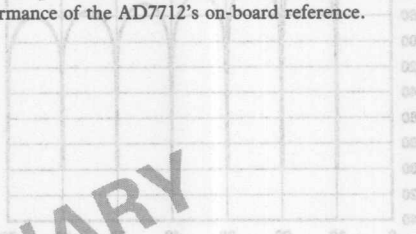


Figure 8. AD7712 Reference Output Noise

V_{BIAS} Input

The V_{BIAS} input determines at what voltage the internal analog circuitry is biased. It essentially provides the return path for analog currents flowing in the modulator and, as such, it should be driven from a low impedance point to minimize errors.

For maximum internal headroom, the V_{BIAS} voltage should be set halfway between AV_{DD} and V_{SS}. The difference between AV_{DD} and (V_{BIAS} + 0.85 × V_{REF}) determines the amount of headroom which the circuit has at the upper end while the difference between V_{SS} and (V_{BIAS} −0.85 × V_{REF}) determines the amount of headroom the circuit has at the lower end. Care should be taken in choosing a V_{BIAS} voltage to ensure that V_{BIAS} ±0.85 × V_{REF} does not exceed the AV_{DD} and V_{SS} limits. For example, with AV_{DD} = +4.75 V, V_{SS} = 0 V and V_{REF} = +2.5 V, the allowable range for the V_{BIAS} voltage is +2.125 V to +2.625 V. With AV_{DD} = +9.5 V, V_{SS} = 0 V and V_{REF} = +5 V, the range for V_{BIAS} is +4.25 V to +5.25 V. With AV_{DD} = +4.75 V, V_{SS} = −4.75 V and V_{REF} = +2.5 V, the V_{BIAS} range is −2.625 V to +2.625 V.

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USING THE AD7712

SYSTEM DESIGN CONSIDERATIONS

The AD7712 operates differently from successive approximation ADCs or integrating ADCs. Since it samples the signal continuously, like a tracking ADC, there is no need for a start convert command. The output register is updated at a rate determined by the first notch of the filter and the output can be read at any time, either synchronously or asynchronously.

Clocking

The AD7712 requires a master clock input, which may be an external TTL/CMOS compatible clock signal applied to the MCLK IN pin with the MCLK OUT pin left unconnected. Alternatively, a crystal of the correct frequency can be connected between MCLK IN and MCLK OUT, in which case the clock circuit will function as a crystal controlled oscillator. For lower clock frequencies, a ceramic resonator may be used instead of the crystal. For these lower frequency oscillators, external capacitors may be required on either the ceramic resonator or on the crystal.

The input sampling frequency, the modulator sampling frequency, the −3 dB frequency, output update rate and calibration time are all directly related to the master clock frequency, $f_{CLK\ IN}$. Reducing the master clock frequency by a factor of 2 will halve the above frequencies and update rate and will double the calibration time.

The current drawn from the DV_{DD} power supply is also directly related to $f_{CLK\ IN}$. Reducing $f_{CLK\ IN}$ by a factor of 2 will halve the DV_{DD} current but will not affect the current drawn from the AV_{DD} power supply.

System Synchronization

If multiple AD7712s are operated from a common master clock, they can be synchronized to update their output registers simultaneously. A falling edge on the $\overline{SYNC}$ input resets the filter and places the AD7712 into a consistent, known state. A common signal to the AD7712s' $\overline{SYNC}$ inputs will synchronize their operation. This would normally be done after each AD7712 has performed its own calibration or has had calibration coefficients loaded to it.

ACCURACY

Sigma-delta ADCs, like VFCs and other integrating ADCs, do not contain any source of nonmonotonicity and inherently offer no missing codes performance. The AD7712 achieves excellent linearity by the use of high quality, on-chip silicon dioxide capacitors, which have a very low capacitance/voltage coefficient. The device also achieves low input drift through the use of chopper stabilized techniques in its input stage. To ensure excellent performance over time and temperature, the AD7712 uses digital calibration techniques that minimize offset and gain error.

Autocalibration

Autocalibration on the AD7712 removes offset and gain errors from the device. A calibration routine should be initiated on the device whenever there is a change in the ambient operating temperature or supply voltage. It should also be initiated if there is a change in the selected channel, gain, filter notch or bipolar/unipolar input range. However, if the AD7712 is in its background calibration mode, the above changes are all automatically taken care of (after the settling time of the filter has been allowed for).

The AD7712 offers self-calibration, system calibration and background calibration facilities. For calibration to occur on the selected channel, the on-chip microcontroller must record the modulator output for two different input conditions. These are "zero scale" and "full-scale" points. With these readings, the microcontroller can calculate the gain slope for the input to output transfer function of the converter. Internally, the part works with a resolution of 33 bits to determine its conversion result of either 16 bits or 24 bits.

Self-Calibration

In the self-calibration mode with a unipolar input range, the zero scale point used in determining the calibration coefficients is AGND and the full-scale point is V_{REF}. The zero scale coefficient is determined by converting an internal AGND node. The full scale coefficient is determined from the span between this AGND conversion and a conversion on an internal V_{REF} node. The self-calibration mode is invoked by writing the appropriate values (0, 0, 1) to the MD2, MD1 and MD0 bits of the control register. In this calibration mode, the AGND node is switched in to the modulator first and a conversion is performed; the V_{REF} node is then switched in and another conversion is performed. When the calibration sequence is complete, the calibration coefficients updated and the filter resettled to the analog input voltage, the $\overline{DRDY}$ output goes low.

For bipolar input ranges in the self-calibrating mode, the sequence is very similar to that just outlined. In this case, the two points which the AD7712 calibrates are midscale (bipolar zero) and positive full scale.

System Calibration

System calibration allows the AD7712 to compensate for system gain and offset errors as well as its own internal errors. System calibration performs the same slope factor calculations as self-calibration but uses voltage values presented by the system to the AIN inputs for the zero and full-scale points. System calibration is a two-step process. The zero scale point must be presented to the converter first. It must be applied to the converter before the calibration step is initiated and remain stable until the step is complete. System calibration is initiated by writing the appropriate values (0, 1, 0) to the MD2, MD1 and MD0 bits of the control register. The $\overline{DRDY}$ output from the device will signal when the step is complete by going low. After the zero scale point is calibrated, the full-scale point is applied and the second step of the calibration process is initiated by again writing the appropriate values (0, 1, 1) to MD2, MD1 and MD0. Again the full-scale voltage must be set up before the calibration is initiated and it must remain stable throughout the calibration step. $\overline{DRDY}$ goes low at the end of this second step to indicate that the system calibration is complete. In the unipolar mode, the system calibration is performed between the two endpoints of the transfer function; in the bipolar mode, it is performed between midscale and positive full scale.

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This two-step system calibration mode offers another feature. After the sequence has been completed, additional offset calibrations can be performed by themselves to adjust the zero reference point to a new system zero reference value. This is achieved by performing the first step of the system calibration sequence (by writing 0, 1, 0 to MD2, MD1, MD0). This will adjust the zero scale or offset point but will not change the slope factor from what was set during a full system calibration sequence.

System Offset Calibration

System offset calibration is a variation of both the system calibration and self-calibration. In this case, the zero scale point for the system is presented to the AIN input of the converter. System offset calibration is initiated by writing 1, 0, 0 to MD2, MD1, MD0. The system zero scale coefficient is determined by converting the voltage applied to the AIN input, while the full-scale coefficient is determined from the span between this AIN conversion and a conversion on an internal V_{REF} node. The zero scale point should be applied to the AIN input for the duration of the calibration sequence. This is a one-step calibration sequence with $\overline{DRDY}$ going low when the sequence is completed. In the unipolar mode, the system offset calibration is performed between the two endpoints of the transfer function; in the bipolar mode, it is performed between midscale and positive full scale.

Background Calibration

The AD7712 also offers a background calibration mode where the part interleaves its calibration procedure with its normal conversion sequence. In the background calibration mode, the same nodes are used as the calibration points as are used in the self-calibration mode (i.e., AGND and V_{REF}). The background calibration mode is invoked by writing 1, 0, 1 to MD2, MD1, MD0 of the control register. When invoked, the background calibration mode reduces the output data rate of the AD7712 by a factor of six. Its advantage is that the part is continually performing calibration and automatically updating its calibration coefficients. As a result, the effects of temperature drift, supply sensitivity and time drift on zero and full scale errors are automatically removed. When the background calibration mode is turned on, the part will remain in this mode until bits MD2, MD1 and MD0 of the control register are changed.

Table IV summarizes the calibration modes and the calibration points associated with them.

Span and Offset Limits

Whenever a system calibration mode is used, there are limits on the amount of offset and span that can be accommodated. The range of input span in both the unipolar and bipolar modes for the AIN1 input has a minimum value of $0.8 \times V_{REF}/GAIN$ and a maximum value of $2.1 \times V_{REF}/GAIN$. For the AIN2 input, these limits are $3.2 \times V_{REF}/GAIN$ and $8.2 \times V_{REF}/GAIN$.

The amount of offset that can be accommodated depends on whether the unipolar or bipolar mode is being used. In unipolar mode, the system calibration modes can handle a maximum offset of $0.25 \times V_{REF}/GAIN$ and a minimum offset of $-(1.05 \times V_{REF}/GAIN)$ on the AIN1 input. This offset range is limited by the requirement that the positive full-scale calibration limit is $\leq 1.05 \times V_{REF}/GAIN$. Thus, the maximum offset ($0.25 \times V_{REF}/GAIN$) plus the minimum span ($0.8 \times V_{REF}/GAIN$) cannot exceed $1.05 \times V_{REF}/GAIN$. For AIN2, the maximum and minimum limits for offset are $V_{REF}/GAIN$ and $-(4.2 \times V_{REF}/GAIN)$, respectively.

In the bipolar mode, the system offset calibration range for AIN1 is restricted to $\pm 0.65 \times V_{REF}/GAIN$. The span range of the converter in bipolar mode is equidistant around the voltage used for the zero scale point. Therefore, the maximum offset $\pm(0.65 \times V_{REF}/GAIN)$ plus half the minimum span $\pm(0.4 \times V_{REF}/GAIN)$ must be less than $\pm(1.05 \times V_{REF}/GAIN)$. If the span is set to $2 \times V_{REF}/GAIN$, the input offset cannot move more than $\pm(0.05 \times V_{REF}/GAIN)$ before the endpoints of the transfer function exceed the input overrange limits $\pm(1.05 \times V_{REF}/GAIN)$. For AIN2, the system offset calibration range is $\pm 2.5 \times V_{REF}/GAIN$.

POWER-UP AND CALIBRATION

On power-up, the AD7712 performs an internal reset which sets the contents of the control register to a known state. However, to ensure correct calibration for the device, a calibration routine should be performed after power-up.

The power dissipation and temperature drift of the AD7712 are low and no warm-up time is required before the initial calibration is performed. However, if an external reference is being used, this reference must have stabilized before calibration is initiated.

Drift Considerations

The AD7712 uses chopper stabilization techniques to minimize input offset drift. Charge injection in the analog switches and dc leakage currents at the sampling node are the primary sources of offset voltage drift in the converter. The dc input leakage current is essentially independent of the selected gain but charge injection effects will increase with increasing gain. As a result, the offset drift numbers will be slightly larger for higher gains. Gain drift within the converter depends primarily upon the temperature tracking of the internal capacitors. It is not affected by leakage currents.

Table IV. Calibration Truth Table

Cal Type	MD2, MD1, MD0	Zero Scale Cal	Full-Scale Cal	Sequence
Self-Cal	0, 0, 1	AGND	V_{REF}	One Step
System Cal	0, 1, 0	AIN		Two Step
System Cal	0, 1, 1		AIN	Two Step
System Offset Cal	1, 0, 0	AIN	V_{REF}	One Step
Background Cal	1, 0, 1	AGND	V_{REF}	One Step

PRELIMINARY TECHNICAL DATA

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Measurement errors due to offset drift or gain drift can be eliminated at any time by recalibrating the converter or by operating the part in the background calibration mode. Using the system calibration mode can also minimize offset and gain errors in the signal conditioning circuitry. Integral and differential linearity errors are not significantly affected by temperature changes.

POWER SUPPLIES AND GROUNDING

Since the analog inputs and reference input are differential, most of the voltages in the analog modulator are common-mode voltages. V_{BIAS} provides the return path for most of the analog currents flowing in the analog modulator. As a result, the V_{BIAS} input should be driven from a low impedance to minimize errors due to charging/discharging impedances on this line. When the internal reference is used as the reference source for the part, AGND is the ground return for this reference voltage.

The analog and digital supplies to the AD7712 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The digital filter will provide rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. The digital supply (DV_{DD}) must never exceed the analog positive supply (AV_{DD}) by more than 0.3 V. Power supply sequencing, therefore, is important. If separate analog and digital supplies are used, care must be taken to ensure that the analog supply is powered up first. If this cannot be ensured, or if DV_{DD} can exceed AV_{DD} at any other time, a Schottky diode should be placed between DV_{DD} and AV_{DD}.

DIGITAL INTERFACE

The AD7712's serial communications port provides a flexible arrangement to allow easy interfacing to industry standard microprocessors, microcontrollers and digital signal processors. A serial read to the AD7712 can access data from the output register, the control register or from the calibration registers. A serial write to the AD7712 can write data to the control register or the calibration registers.

Two different modes of operation are available, optimized for different types of interface where the AD7712 can act either as master in the system (it provides the serial clock) or as slave (an external serial clock can be provided to the AD7712). These two modes, labelled self-clocking mode and external clocking mode, are discussed in detail in the following sections.

Self-Clocking Mode

The AD7712 is configured for its self-clocking mode by tying the MODE pin high. In this mode, the AD7712 provides the serial clock signal used for the transfer of data to and from the AD7712. This self-clocking mode can be used with processors that allow an external device to clock their serial port, including most digital signal processors and microcontrollers such as the 68HC11 and 68HC05. It also allows easy interfacing to serial parallel conversion circuits in systems with parallel data communication, allowing interfacing to 74XX299 Universal Shift registers without any additional decoding. In the case of shift registers, the serial clock line should have a pull-down resistor instead of the pull-up resistor shown in Figure 9 and Figure 10.

Read Operation

Data can be read from either the output register, the control register or the calibration registers. A0 determines whether the data read accesses data from the control register or from the output/calibration registers. This A0 signal must remain valid for the duration of the serial read operation. The function of the $\overline{DRDY}$ line is dependent only on the output update rate of the device and the reading of the output data register. $\overline{DRDY}$ only goes low when a new data word is available in the output data register. It is reset high when the last bit of data (either 16th bit or 24th bit) is read from the output register. If a new data word becomes available to the output register while data is being read from the output register, $\overline{DRDY}$ will not indicate this and the new data word will be lost to the user. $\overline{DRDY}$ is not affected by reading from the control register or the calibration registers.

Data can only be accessed from the output data register when $\overline{DRDY}$ is low. If $\overline{RFS}$ goes low while $\overline{DRDY}$ is high, the SCLK and SDATA lines will not become active until $\overline{DRDY}$ goes low. When $\overline{DRDY}$ goes low, the data word will then be output by the AD7712. If $\overline{RFS}$ goes low with $\overline{DRDY}$ high, no data transfer will take place until $\overline{DRDY}$ does go low. Provided $\overline{RFS}$ stays low for long enough, $\overline{RFS}$ can, in most cases, be brought low at any time with the AD7712 clocking the data into the microprocessor, microcontroller or shift register when its clock and data lines become active. $\overline{DRDY}$ does not have any effect on reading data from the control register or from the calibration registers.

PRELIMINARY TECHNICAL DATA

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where all the data is read from the AD7712 in one read operation. Figure 9b shows a situation where the data is read from the AD7712 over a number of read operations. Both read operations show a read from the AD7712's output data register. A read from the control register or calibration registers is similar but in these cases the $\overline{DRDY}$ line is not related to the read function. It can go low at any stage in the read cycle without affecting the read and its status should be ignored.

Figure 9a shows a read operation to the AD7712 where $\overline{RFS}$ remains low for the duration of the data word transmission. For the timing diagram shown, it is assumed that there is a pull up resistor on the SCLK output. With $\overline{DRDY}$ low, the $\overline{RFS}$ input is brought low. $\overline{RFS}$ going low enables the serial clock of the AD7712 and also places the MSB of the word on the serial data line. All subsequent data bits are clocked out on a high to low transition of the serial clock and are valid prior to the following rising edge of this clock. The final active falling edge of SCLK clocks out the LSB and this LSB is valid prior to the final active rising edge of SCLK. Coincident with the next falling edge of SCLK, $\overline{DRDY}$ is reset high. $\overline{DRDY}$ going high turns off the

Figure 9b shows a timing diagram for a read operation where $\overline{RFS}$ returns high during the transmission of the word and returns low again to access the rest of the data word. As before, the waveform for SCLK assumes that there is a pull up resistor on this line. Timing parameters and functions are very similar to that outlined for Figure 9a, but Figure 9b has a number of additional times to show timing relationships when $\overline{RFS}$ returns high in the middle of transferring a word.

$\overline{RFS}$ should return high during a low time of SCLK. On the rising edge of $\overline{RFS}$, the SCLK and SDATA outputs are turned off. $\overline{DRDY}$ remains low and will remain low until all bits of the data word are read from the AD7712, regardless of the number of times $\overline{RFS}$ changes state during the read operation. When $\overline{RFS}$ returns low again, it turns on the SCLK output and activates the SDATA output. The first bit placed on the SDATA line after $\overline{RFS}$ goes low is the same bit as appeared on the bus when $\overline{RFS}$ went high. When the entire word is transmitted, the $\overline{DRDY}$ line will go high turning off the SDATA and SCLK lines as per Figure 9a.

PRELIMINARY TECHNICAL DATA

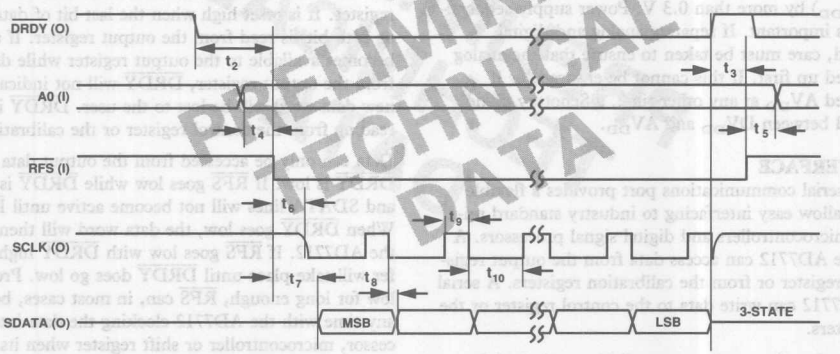


Figure 9a. Self-Clocking Mode, Output Data Read Operation

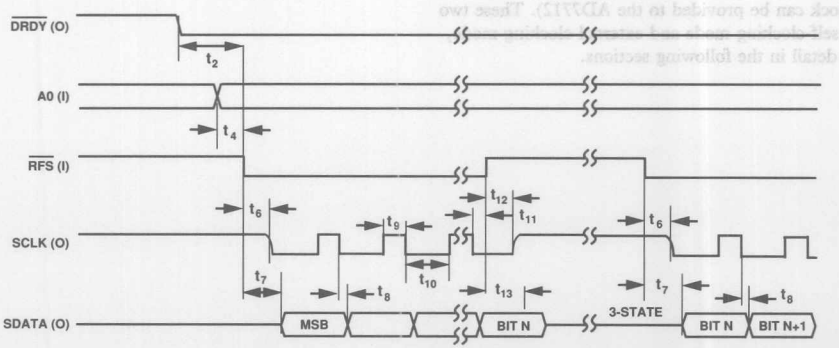


Figure 9b. Self-Clocking Mode, Output Data Read Operation ($\overline{RFS}$ Returns High During Read Operation)

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registers. In either case, the write operation is not affected by the $\overline{DRDY}$ line and the write operation does not have any effect on the status of $\overline{DRDY}$.

Figure 10a shows a write operation to the AD7712 with $\overline{TFS}$ remaining low for the duration of the write operation. A0 determines whether a write operation transfers data to the control register or to the calibration registers. This A0 signal must remain valid for the duration of the serial write operation. The falling edge of $\overline{TFS}$ enables the internally generated SCLK output. The serial data to be loaded to the AD7712 must be valid on the rising edge of this SCLK signal. Data is clocked into the AD7712 on the rising edge of the SCLK signal with the MSB transferred first. On the last active rising edge of SCLK, the LSB is loaded to the AD7712. Subsequent to the next falling edge of SCLK, the SCLK output is turned off. (The timing diagram of Figure 10a assumes a pull up resistor on the SCLK line.)

Figure 10b shows a timing diagram for a write operation to the AD7712 with $\overline{TFS}$ returning high during the write operation and returning low again to write the rest of the data word. Once

very similar to that outlined for Figure 10a but Figure 10b has a number of additional times to show timing relationships when $\overline{TFS}$ returns high in the middle of transferring a word.

The falling edge of $\overline{TFS}$ again initiates the SCLK output and data to be loaded to the AD7712 must be valid prior to the rising edge of this SCLK signal. The rising edge of $\overline{TFS}$ turns off the SCLK output. $\overline{TFS}$ should return high during the low time of SCLK. When $\overline{TFS}$ returns low again, it turns on the SCLK output. When all data bits have been written to the device, the SCLK output is turned off as per Figure 10a.

External Clocking Mode

The AD7712 is configured for its external clocking mode by tying the MODE pin low. In this mode, SCLK of the AD7712 is configured as an input and an external serial clock must be provided to this SCLK pin. This external clocking mode is designed for direct interface to systems which provide a serial clock output that is synchronized to the serial data output, including microcontrollers such as the 80C51, 87C51, 68HC11 and 68HC05 and most digital signal processors.

PRELIMINARY TECHNICAL DATA

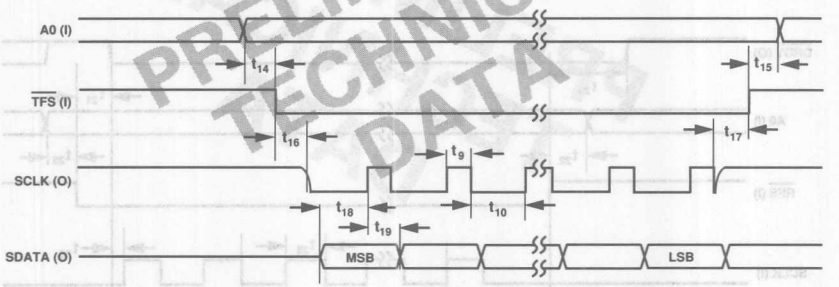


Figure 10a. Self-Clocking Mode, Control/Calibration Register Write Operation

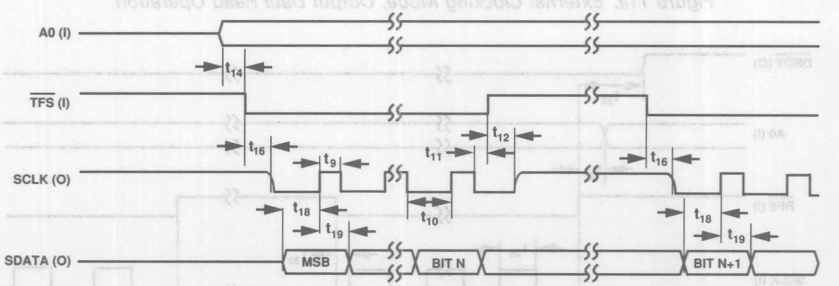


Figure 10b. Self-Clocking Mode, Control/Calibration Register Write Operation ($\overline{TFS}$ Returns High During Write Operation)

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Read Operation

Figures 11a and 11b show timing diagrams for reading from the AD7712 in the external clocking mode. Figure 11a shows a situation where all the data is read from the AD7712 in one read operation. Figure 11b shows a situation where the data is read from the AD7712 over a number of read operations.

As with the self-clocking mode, data can be read from either the output register, the control register or the calibration registers. A0 determines whether the data read accesses data from the control register or from the output/calibration registers. This A0 signal must remain valid for the duration of the serial read operation. The function of the $\overline{DRDY}$ line is dependent only on the output update rate of the device and the reading of the output data register. $\overline{DRDY}$ only goes low when a new data word is available in the output data register. It is reset high when the last bit of data (either 16th bit or 24th bit) is read from the output register. If a new data word becomes available to the output register while data is being read from the output register, $\overline{DRDY}$ will not indicate this and the new data word will be lost to the user. $\overline{DRDY}$ is not affected by reading from the control register or the calibration register.

Data can only be accessed from the output data register when $\overline{DRDY}$ is low. If $\overline{RFS}$ goes low while $\overline{DRDY}$ is high, the SDATA line will not become active until $\overline{DRDY}$ goes low. In this external clocking mode, an external clock is applied to the SCLK input. The receiving device (microprocessor or microcontroller) expects to see valid data on edges of this SCLK signal. However, with $\overline{DRDY}$ high SDATA is not active and no data is transmitted. $\overline{DRDY}$ does not have any effect on reading data from the control register or from the calibration registers.

Figure 11a shows a read operation to the AD7712 where $\overline{RFS}$ remains low for the duration of the data word transmission. With $\overline{DRDY}$ low, the $\overline{RFS}$ input is brought low. The input SCLK signal should be low between read and write operations. $\overline{RFS}$ going low places the MSB of the word to be read on the serial data line. All subsequent data bits are clocked out on a high to low transition of the serial clock and are valid prior to the following rising edge of this clock. The penultimate falling edge of SCLK clocks out the LSB and the final falling edge resets the $\overline{DRDY}$ line high. This rising edge of $\overline{DRDY}$ turns off the serial data output.

Figure 11b shows a timing diagram for a read operation where $\overline{RFS}$ returns high during the transmission of the word and returns low again to access the rest of the data word. Timing parameters and functions are very similar to that outlined for Figure 11a but Figure 11b has a number of additional times to show timing relationships when $\overline{RFS}$ returns high in the middle of transferring a word.

PRELIMINARY TECHNICAL DATA

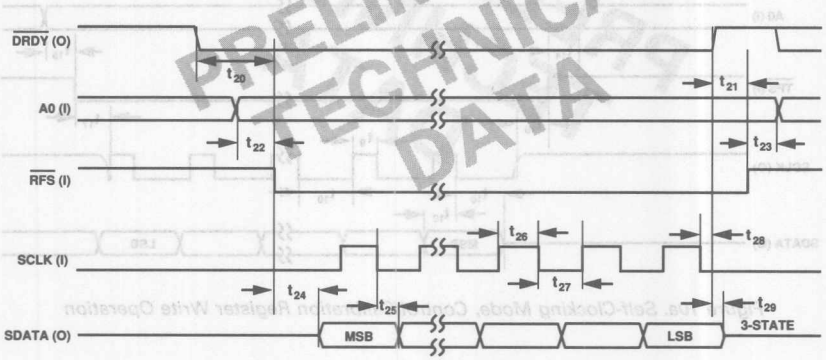


Figure 11a. External Clocking Mode, Output Data Read Operation

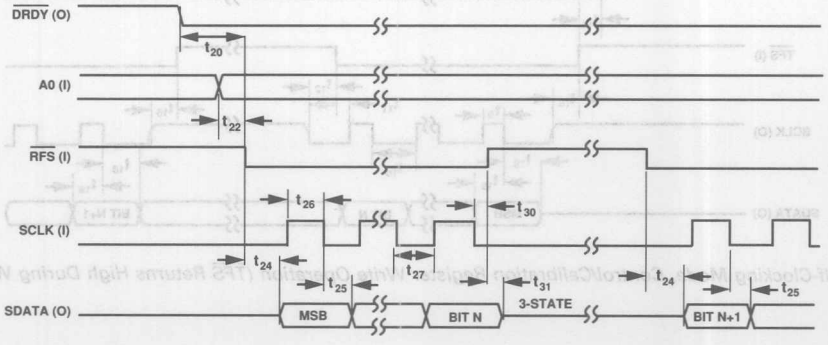


Figure 11b. External Clocking Mode, Output Data Read Operation ($\overline{RFS}$ Returns High During Read Operation)

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$\overline{RFS}$ should return high during a low time of SCLK. On the rising edge of $\overline{RFS}$, the SDATA output is turned off. $\overline{DRDY}$ remains low and will remain low until all bits of the data word are read from the AD7712, regardless of the number of times $\overline{RFS}$ changes state during the read operation. When $\overline{RFS}$ returns low again, it activates the SDATA output and places the next bit of the data word on the SDATA output. When the entire word is transmitted, the $\overline{DRDY}$ line will go high, turning off the SDATA output as per Figure 11a.

Write Operation

Data can be written to either the control register or calibration registers. In either case, the write operation is not affected by the $\overline{DRDY}$ line and the write operation does not have any effect on the status of $\overline{DRDY}$.

Figure 12a shows a write operation to the AD7712 with $\overline{TFS}$ remaining low for the duration of the write operation. A0 determines whether a write operation transfers data to the control register or to the calibration registers. This A0 signal must remain valid for the duration of the serial write operation. As before, the serial clock line should be low between read and write operations. The serial data to be loaded to the AD7712 must be valid on the high level of the externally applied SCLK signal. Data is clocked into the AD7712 on the high level of this SCLK signal with the MSB transferred first. On the last active rising edge of SCLK, the LSB is loaded to the AD7712.

Figure 12b shows a timing diagram for a write operation to the AD7712 with $\overline{TFS}$ returning high during the write operation and returning low again to write the rest of the data word. Timing parameters and functions are very similar to that outlined for Figure 12a, but Figure 12b has a number of additional times to show timing relationships when $\overline{TFS}$ returns high in the middle of transferring a word.

Data to be loaded to the AD7712 must be valid prior to the rising edge of the SCLK signal. $\overline{TFS}$ should return high during the low time of SCLK . After $\overline{TFS}$ returns low again, the next bit of the data word to be loaded to the AD7712 is clocked in on next high level of the SCLK input. On the last active rising edge of the SCLK input, the LSB is loaded to the AD7712.

SIMPLIFYING THE INTERFACE

In some applications, the user may not require the facility of writing to the on-chip calibration registers. In this case, the serial interface to the AD7712 can be simplified by connecting the $\overline{TFS}$ line to the A0 input of the AD7712. This means that any write to the device will load data to the control register (since A0 is low while $\overline{TFS}$ is low) and any read to the device will access data from the output data register or from the calibration registers (since A0 is high while $\overline{RFS}$ is low). It should be noted that in this arrangement the user does not have the capability of reading from the control register.

PRELIMINARY TECHNICAL DATA

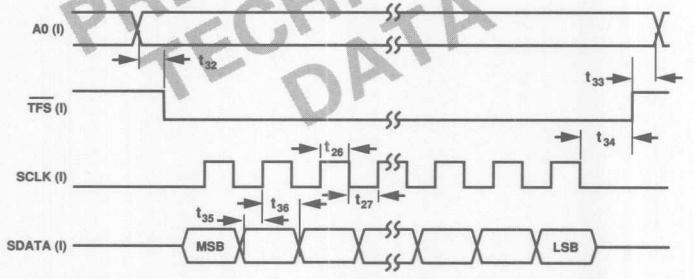


Figure 12a. External Clocking Mode, Control/Calibration Register Write Operation

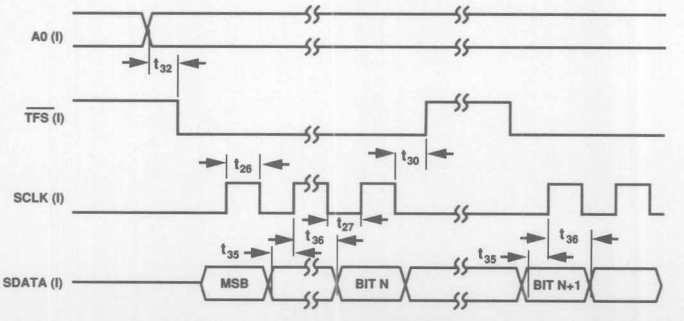


Figure 12b. External Clocking Mode, Control/Calibration Register Write Operation ($\overline{TFS}$ Returns High During Write Operation)

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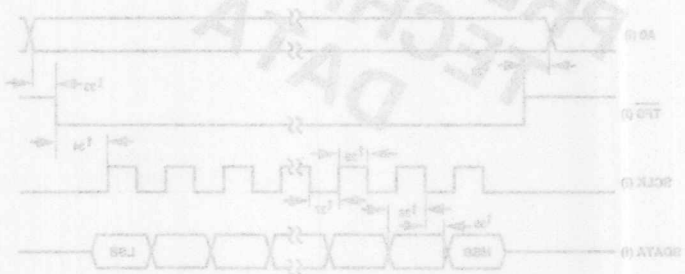


Figure 12a. External Clocking Mode, Control/Calibration Register Write Operation

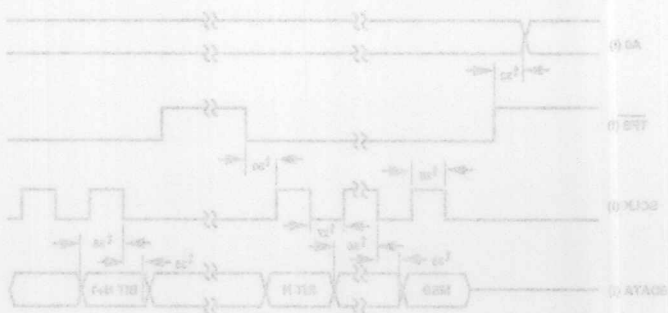


Figure 12b. External Clocking Mode, Control/Calibration Register Write Operation (TPS Returns High During Write Operation)

LC²MOS Loop-Powered Signal Conditioning ADC

AD7713*

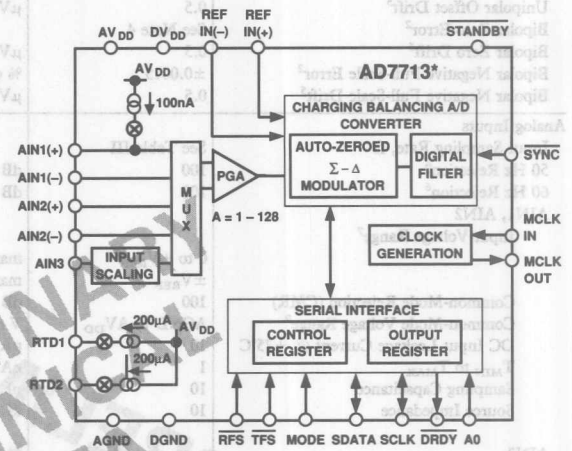
FEATURES

- Charge Balancing ADC
  - 21 Bits No Missing Codes
  - ±0.0015% Nonlinearity
- Three-Channel Programmable Gain Front End
  - Gains from 1 to 128
  - Two Differential Inputs
  - One Single Ended High Voltage Input
- Low-Pass Filter with Programmable Filter Cutoffs
- Ability to Read/Write Calibration Coefficients
- RTD Excitation Current Sources
- Bidirectional Microcontroller Serial Interface
- Single Supply Operation
- Low Power (3.5 mW typ) with Power-Down Mode (35 μW typ)

APPLICATIONS

- Loop Powered (Smart) Transmitters
- RTD Transducers
- Process Control
- Portable Industrial Instruments

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD7713 is a complete analog front end for low frequency measurement applications. The device accepts low level signals directly from a transducer or high level signals ($\pm 4 \times V_{REF}$) and outputs a serial digital word. It employs a sigma-delta conversion technique to realize up to 21 bits of no missing codes performance. The input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via the on-chip control register allowing adjustment of the filter cutoff and settling time.

The part features two differential analog inputs and one single-ended high level analog input as well as a differential reference input. It can be operated from a single supply (AV_{DD} and DV_{DD} at +5 V). The part provides two current sources which can be used to provide excitation in three-wire and four-wire RTD configurations. The AD7713 thus performs all signal conditioning and conversion for a single, dual or three-channel system.

The AD7713 is ideal for use in smart, microcontroller-based systems. Gain settings, signal polarity and RTD current control can be configured in software using the bidirectional serial port. The AD7713 contains self-calibration, system calibration and background calibration options and also allows the user to read and to write the on-chip calibration registers.

CMOS construction ensures very low power dissipation and a software programmable power-down mode reduces the standby power consumption to only 35 μW. The part is available in a 24-pin, 0.3 inch wide, plastic and hermetic dual-in-line package (DIP) as well as a 24-lead small outline (SOIC) package.

PRODUCT HIGHLIGHTS

1. The AD7713 consumes less than 1 mA in total supply current, making it ideal for use in loop-powered systems.
2. The low level programmable gain channels allow the AD7713 to accept input signals directly from a transducer, removing a considerable amount of signal conditioning. To maximize the flexibility of the part, the high level analog input accepts $\pm 4 \times V_{REF}$/GAIN signals. On-chip current sources provide excitation for three-wire and four-wire RTD configurations.
3. No Missing Codes ensures true, usable, 21-bit dynamic range coupled with excellent ±0.0015% accuracy. The effects of temperature drift are eliminated by on-chip self-calibration, which removes zero-scale and full-scale errors.
4. The AD7713 is ideal for microcontroller or DSP processor applications with an on-chip control register which allows control over filter cutoff, input gain, signal polarity and calibration modes. The AD7713 allows the user to read and to write the on-chip calibration registers.

*Patent pending.

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AD7713—SPECIFICATIONS

(AV_{DD} = +5 V to +10 V; DV_{DD} = +5 V; REF IN(+) = +2.5 V; REF IN(−) = AGND; MCLK IN = 2 MHz, unless otherwise stated. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A, S Versions[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	21	Bits min	Guaranteed by Design
Output Noise	See Tables I and II		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity	±0.0015	% of FSR max	Filter Notches ≤ 15 Hz
Positive Full-Scale Error[2, 3]	See Note 4		Excluding Reference
Full-Scale Drift[5]	0.5	μV/°C max	Excluding Reference
Unipolar Offset Error[2]	See Note 4		
Unipolar Offset Drift[5]	0.5	μV/°C max	
Bipolar Zero Error[2]	See Note 4		
Bipolar Zero Drift[5]	0.5	μV/°C max	
Bipolar Negative Full-Scale Error[2]	±0.0015	% of FSR max	Excluding Reference; Typically ±0.0004%
Bipolar Negative Full-Scale Drift[5]	0.5	μV/°C max	Excluding Reference
Analog Inputs			
Input Sampling Rate, fs	See Table III		
50 Hz Rejection[6]	100	dB min	For Filter Notches of 2, 5, 10, 25, 50 Hz, $\pm 0.02 \times f_{NOTCH}$
60 Hz Rejection[6]	100	dB min	For Filter Notches of 2, 6, 10, 30, 60 Hz, $\pm 0.02 \times f_{NOTCH}$
AIN1, AIN2			
Input Voltage Range[7]			For Normal Operation. Depends on Gain Selected.
	0 to $+V_{REF}$[8]	max	Unipolar Input Range (B/U Bit of Control Register = 0)
	$\pm V_{REF}$	max	Bipolar Input Range (B/U Bit of Control Register = 1)
Common-Mode Rejection (CMR)	100	dB min	At dc
Common-Mode Voltage Range[9]	AGND to AV_{DD}	V min to V max	
DC Input Leakage Current @ +25°C	10	pA max	
T_{MIN} to T_{MAX}	1	nA max	
Sampling Capacitance[6]	10	pF max	
Source Impedance	10	kΩ max	Maximum Allowable Output Impedance of Whatever Is Driving Either Analog Input
AIN3			
Input Voltage Range	$\pm 4 \times V_{REF}$	max	For Normal Operation; Depends on Gain Selected
REFERENCE INPUT			
REF IN(+) − REF IN(−) Voltage	+2.5 to +5	V min to V max	For Specified Performance
Input Sampling Rate, fs	$f_{CLKIN}/512$		
50 Hz Rejection[6]	100	dB min	For Filter Notches of 2, 5, 10, 25, 50 Hz, $\pm 0.02 \times f_{NOTCH}$
60 Hz Rejection[6]	100	dB min	For Filter Notches of 2, 6, 10, 30, 60 Hz, $\pm 0.02 \times f_{NOTCH}$
Common-Mode Rejection (CMR)	100	dB min	At dc
Common-Mode Voltage Range[9]	AGND to AV_{DD}	V min to V max	
DC Input Leakage Current @ +25°C	10	pA max	
T_{MIN} to T_{MAX}	1	nA max	
LOGIC INPUTS			
Input Current	±10	μA max	
All Inputs except MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	2.0	V min	
MCLK IN Only			
V_{INL}, Input Low Voltage	1.5	V max	
V_{INH}, Input High Voltage	3.5	V min	
LOGIC OUTPUTS			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 100 μA
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[10]	9	pF typ	
TRANSDUCER BURN-OUT			
Current	100	nA nom	
Initial Tolerance	±10	% typ	
Drift	100	ppm/°C typ	

PRELIMINARY TECHNICAL DATA

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Parameter	A, S Versions	Units	Conditions/Comments
RTD EXCITATION CURRENTS			(RTD1, RTD2)
Output Current	200	μA nom	
Initial Tolerance	±20	% max	
Drift	35	ppm/°C typ	
Line Regulation (AV_{DD})	200	nA/V max	
Load Regulation	200	nA/V max	
SYSTEM CALIBRATION			
AIN1, AIN2			
Positive Full-Scale Calibration Limit[11]	$(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Negative Full-Scale Calibration Limit[11]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Offset Calibration Limit[12, 13]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Input Span[12]	$0.8 \times V_{REF}/GAIN$	V min	GAIN Is the Selected PGA Gain (Between 1 and 128)
	$(2.1 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
AIN3			
Positive Full-Scale Calibration Limit[11]	$(4.2 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Negative Full-Scale Calibration Limit[11]	$-(4.2 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Offset Calibration Limit[13]	$-(4.2 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Input Span	$3.2 \times V_{REF}/GAIN$	V min	GAIN Is the Selected PGA Gain (Between 1 and 128)
	$(8.4 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
POWER REQUIREMENTS			
Power Supply Voltages			
AV_{DD} Voltage	+5 to +10	V nom	±10% for Specified Performance
DV_{DD} Voltage	+5	V nom	±10% for Specified Performance
Power Supply Currents			
AV_{DD} Current	0.5	mA max	
DV_{DD} Current	0.5	mA max	$f_{CLK\ IN}$ = 1MHz
DV_{DD} Current	1	mA max	$f_{CLK\ IN}$ = 2MHz
Power Supply Rejection[14] (AV_{DD})	90	dB typ	Rejection w.r.t. AGND
Power Dissipation			
Normal Mode	5.5	mW max	$AV_{DD} = DV_{DD}$ = +5 V, $f_{CLK\ IN}$ = 1 MHz; Typically 3.5 mW
Standby (Power-Down) Mode	50	μW max	$AV_{DD} = DV_{DD}$ = +5 V; Typically 35 μW

NOTES

[1]Temperature ranges are as follows: A Version: −40°C to +85°C; S Version: −55°C to +125°C.

[2]Applies after calibration at the temperature of interest.

[3]Positive full-scale error applies to both unipolar and bipolar input ranges.

[4]These errors will be of the order of the output noise of the part as shown in Table I.

[5]Recalibration at any temperature or use of the background calibration mode will remove these drift errors. These numbers are guaranteed by design and/or characterization.

[6]These numbers are guaranteed by design and/or characterization.

[7]The AIN1 and AIN2 analog inputs present a very high impedance dynamic load which varies with clock frequency and input sample rate. The maximum recommended source resistance is 10 kΩ.

[8]V_{REF} = REF IN(+) − REF IN(−).

[9]This common-mode voltage range is allowed provided that the absolute value of the input voltage does not exceed AV_{DD} + 30 mV and AGND − 30 mV.

[10]Sample tested at +25°C to ensure compliance.

[11]After calibration, if the analog input exceeds positive full scale, the converter will output all 1s. If the analog input is less than negative full scale, then the device will output all 0s.

[12]These calibration and span limits apply provided the absolute voltage on the analog inputs does not exceed AV_{DD} or go more negative than AGND − 30 mV.

[13]The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.

[14]Measured at dc and applies in the selected passband. PSRR at 50 Hz will exceed 120 dB with filter notches of 2, 5, 10, 25 or 50 Hz. PSRR at 60 Hz will exceed 120 dB with filter notches of 2, 6, 10, 30 or 60 Hz.

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Control Register (24-Bits)

A write to the device with A0 low writes data to the control register. A read to the device with the A0 pin low accesses the contents of the control register.

MD2	MD1	MD0	G2	G1	G0	CH1	CH0	WL	RO	BO	B/U
FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0

Operating Mode

MD2	MD1	MD0	Operating Mode
0	0	0	Normal Mode. This is the normal mode of operation of the device whereby a read to the device with A0 high accesses data from the data register. This is the default condition of these bits after the internal power-on reset.
0	0	1	Activate Self-Calibration. This activates self-calibration on the channel selected by CH0 and CH1. This is a one-step calibration sequence and when complete, the part returns to Normal Mode. For this calibration type, the zero-scale calibration is done internally on AGND and the full-scale calibration is done internally on V_{REF}.
0	1	0	Activate System Calibration. This activates system calibration on the channel selected by CH0 and CH1. This is a two-step calibration sequence, with the zero-scale calibration done first on the selected input channel and $\overline{DRDY}$ indicating when this zero-scale calibration is complete. The part returns to Normal Mode at the end of this first step in the two-step sequence.
0	1	1	Activate System Calibration. This is the second step of the system calibration sequence with full-scale calibration being performed on the selected input channel. When this calibration is complete, the part returns to Normal Mode.
1	0	0	Activate System-Offset Calibration. This activates system-offset calibration on the channel selected by CH0 and CH1. This is a one step calibration sequence and when complete the part returns to Normal Mode. For this calibration type, the zero-scale calibration is done on the selected input channel and the full-scale calibration are done internally on V_{REF}.
1	0	1	Activate Background Calibration. This activates background calibration on the channel selected by CH0 and CH1. If the background calibration mode is on, then the AD7713 provides continuous self-calibration of the reference and AGND. This calibration takes place as part of the conversion sequence, extending the conversion time and reducing the word rate by a factor of six. Its major advantage is that the user does not have to worry about recalibrating the device when there is a change in the ambient temperature. In this mode, AGND and V_{REF}, as well as the analog input voltage, are continuously monitored and the calibration registers of the device are updated, if necessary.
1	1	0	Read/Write Zero-Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the zero-scale calibration coefficients of the channel selected by CH0 and CH1. A write to the device with A0 high writes data to the zero-scale calibration coefficients of the channel selected by CH0 and CH1. The word length for reading and writing these coefficients is 24 bits, regardless of the status of the WL bit of the control register. Note, AIN2 and AIN3 share calibration coefficients.
1	1	1	Read/Write Full-Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the full-scale calibration coefficients of the channel selected by CH0 and CH1. A write to the device with A0 high writes data to the full-scale calibration coefficients of the channel selected by CH0 and CH1. The word length for reading and writing these coefficients is 24 bits, regardless of the status of the WL bit of the control register. Note, AIN2 and AIN3 share calibration coefficients.

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PGA Gain

G2	G1	G0	Gain	
0	0	0	1	(Default Condition after the internal power-on reset)
0	0	1	2	
0	1	0	4	
0	1	1	8	
1	0	0	16	
1	0	1	32	
1	1	0	64	
1	1	1	128	

Channel Selection

CH1	CH0	Channel	
0	0	AIN1	(Default Condition after the internal power-on reset)
0	1	AIN2	
1	0	AIN3	

Word Length

WL	Output Word Length	
0	16-Bit	(Default Condition after internal power-on reset)
1	24-Bit	

RTD Excitation Currents

RO		
0	Off	(Default Condition after internal power-on reset)
1	On	

Burn-out Current

BO		
0	Off	(Default Condition after internal power-on reset)
1	On	

Bipolar/Unipolar Selection (Both Inputs)

B/U		
0	Bipolar	(Default Condition after internal power-on reset)
1	Unipolar	

Filter Selection (FS11–FS0)

The on-chip digital filter provides a $Sinc^3$ (or $(Sinx/x)^3$) filter response. The 12 bits of data programmed into these bits determine the filter cutoff frequency, the position of the first notch of the filter and the data rate for the part. In association with the gain selection, it also determines the output noise (and hence the effective resolution) of the device.

The first notch of the filter occurs at a frequency determined by the relationship: filter first notch frequency = $(f_{CLKIN}/512)/$ *code* where *code* is the decimal equivalent of the code in bits FS0 to FS11 and is in the range 19 to 2,000. With the nominal $f_{CLK\ IN}$ of 2 MHz, this results in a first notch frequency range from 1.952 Hz to 205.59 Hz. To ensure correct operation of the AD7713, the value of the code loaded to these bits must be within this range. Failure to do this will result in unspecified operation of the device.

Changing the filter notch frequency, as well as the selected gain, impacts resolution. Tables I and II show the effect of the filter notch frequency and gain on the effective resolution of the AD7713. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 10 Hz, then a new word is available at a 10 Hz rate or every 100 ms. If the first notch is at 200 Hz, a new word is available every 5 ms.

The settling time of the filter to a full-scale step input change is worst case 4 × the data rate. For example, with the first filter notch at 10 Hz, the settling time of the filter to a full-scale step input change is 400 ms max. If the first notch is at 200 Hz, the settling time of the filter to a full-scale input step is 20 ms max.

The −3 dB frequency is determined by the programmed first notch frequency according to the relationship: filter −3 dB frequency = 0.262 × first notch frequency.

PRELIMINARY TECHNICAL DATA

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Table I shows the output rms noise for some typical notch and −3 dB frequencies. The numbers given are for the bipolar input ranges with a V_{REF} of +2.5 V. The numbers in Table I are guaranteed by a combination of testing, characterization and design. The output noise from the part comes from two sources: the quantization noise from the analog-to-digital conversion process, and device noise. Device noise is independent of gain and is essentially flat across the frequency spectrum. Quantization noise is ratiometric to the input full scale (and hence gain) and its frequency response is shaped by the modulator.

Looking at Table I, as the cutoff frequency increases, the output noise increases because more of the quantization noise of the part comes through to the output. Hence, the output noise increases with increasing −3 dB frequencies. For the lower notch settings, the output noise is dominated by the device noise and, hence, altering the gain has little effect on the output noise. At higher notch frequencies, the quantization noise dominates the output noise and, in this case, the output noise tends to decrease with increasing gain.

Since the output noise comes from two sources, the effective resolution of the device (i.e., the ratio of the output rms noise to the input full scale) does not remain constant with increasing gain or with increasing bandwidth. Table II shows the same table as Table I except that the output is now expressed in terms of effective resolution (the magnitude of the rms noise with respect to 2 × V_{REF}/GAIN, i.e., the input full scale). It is possible to do post filtering on the device to improve the output data rate for a given −3 dB frequency and also to further reduce the output noise (see DIGITAL FILTERING section).

Table I. Output Noise vs. Gain and First Notch Frequency

First Notch of Filter and O/P Data Rate[1]	−3 dB Frequency	OUTPUT RMS NOISE (μV) GAIN of 1	GAIN of 2	GAIN of 4	GAIN of 8	GAIN of 16	GAIN of 32	GAIN of 64	GAIN of 128
2 Hz[2]	0.52 Hz	1.7	0.84	0.60	0.42	0.42	0.42	0.42	0.42
5 Hz[2]	1.31 Hz	3.4	1.7	1.2	0.60	0.60	0.60	0.60	0.60
6 Hz[2]	1.57 Hz	3.4	2.4	1.2	0.84	0.84	0.60	0.60	0.60
10 Hz[2]	2.62 Hz	9.5	4.8	2.4	1.7	1.2	0.84	0.84	0.84
12 Hz[2]	3.14 Hz	13.5	6.7	3.4	1.7	1.2	1.2	0.84	0.84
20 Hz[3]	5.24 Hz	54	27	13.5	6.7	3.4	1.7	1.7	1.2
50 Hz[3]	13.1 Hz	432	216	108	54	27	13.5	6.7	4.8
100 Hz[3]	26.2 Hz	2.4 × 10^3	1.2 × 10^3	610	305	153	76	38	19
200 Hz[3]	52.4 Hz	13.8 × 10^3	6.9 × 10^3	3.4 × 10^3	1.7 × 10^3	863	432	216	108

NOTES
[1]The default condition (after the internal power-on reset) for the first notch of filter is 12 Hz.
[2]For these filter notch frequencies, the output rms noise is primarily independent of the value of the reference voltage. Therefore, increasing the reference voltage will give an increase in the effective resolution of the device (i.e. the ratio of the rms noise to the input full-scale is increased since the output rms noise remains constant as the input full-scale increases).
[3]For these filter notch frequencies, the output rms noise is proportional to the value of the reference voltage.

Table II. Effective Resolution vs. Gain and First Notch Frequency

First Notch of Filter and O/P Data Rate	−3 dB Frequency	EFFECTIVE RESOLUTION[1] (Bits) GAIN of 1	GAIN of 2	GAIN of 4	GAIN of 8	GAIN of 16	GAIN of 32	GAIN of 64	GAIN of 128
2 Hz	0.52 Hz	21.5	21.5	21	20.5	19.5	18.5	17.5	16.5
5 Hz	1.31 Hz	20.5	20.5	20	20	19	18	17	16
6 Hz	1.57 Hz	20.5	20	20	19.5	18.5	18	17	16
10 Hz	2.62 Hz	19	19	19	18.5	18	17.5	16.5	15.5
12 Hz	3.14 Hz	18.5	18.5	18.5	18.5	18	17	16.5	15.5
20 Hz	5.24 Hz	16.5	16.5	16.5	16.5	16.5	16.5	15.5	15
50 Hz	13.1 Hz	13.5	13.5	13.5	13.5	13.5	13.5	13.5	13
100 Hz	26.2 Hz	11	11	11	11	11	11	11	11
200 Hz	52.4 Hz	8.5	8.5	8.5	8.5	8.5	8.5	8.5	8.5

NOTE
[1]Effective Resolution is defined as the magnitude if the output rms noise to the input full-scale (i.e., 2 × V_{REF}/GAIN). The above table applies for a V_{REF} of +2.5 V and resolution numbers are rounded to the nearest 0.5 LSB.

PRELIMINARY TECHNICAL DATA

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PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Function
1	SCLK	Serial Clock. Logic input/output depending on the status of the MODE pin. When MODE is high, the device is in its self-clocking mode and the SCLK pin provides a serial clock output. This SCLK becomes active when $\overline{RFS}$ or $\overline{TFS}$ goes low and it goes high impedance when either $\overline{RFS}$ or $\overline{TFS}$ returns high or when the device has completed transmission of an output word. When MODE is low, the device is in its external clocking mode and the SCLK pin acts as an input. This input serial clock can be a continuous clock with all data being transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to the AD7713 in smaller batches of data.
2	MCLK IN	Master Clock signal for the device. This can be provided in the form of a crystal or external clock. A crystal can be tied across the MCLK IN and MCLK OUT pins. Alternatively, the MCLK IN pin can be driven with a CMOS-compatible clock and MCLK OUT left unconnected. The clock input frequency is nominally 2 MHz.
3	MCLK OUT	When the master clock for the device is a crystal, the crystal is connected between MCLK IN and MCLK OUT.
4	A0	Address Input. With this input low, reading and writing to the device is to the control register. With this input high, access is to either the data register or the calibration registers.
5	$\overline{SYNC}$	Logic Input which allows for synchronization of the digital filters when using a number of AD7713s. It resets the nodes of the digital filter.
6	MODE	Logic Input. When this pin is high, the device is in its self-clocking mode; with this pin low, the device is in its external clocking mode.
7	AIN1(+)	Analog Input Channel 1. Positive input of the programmable-gain differential analog input. The AIN1(+) input is connected to an output current source which can be used to check that an external transducer has burnt out or has gone open circuit. This output current source can be turned on/off via the control register.
8	AIN1(−)	Analog Input Channel 1. Negative input of the programmable gain differential analog input.
9	AIN2(+)	Analog Input Channel 2. Positive input of the programmable gain differential analog input.
10	AIN2(−)	Analog Input Channel 2. Negative input of the programmable gain differential analog input.
11	$\overline{STANDBY}$	Logic Input. Taking this pin low shuts down the internal analog and digital circuitry, reducing power consumption to less than 50 μW.
12	AV_{DD}	Analog Positive Supply Voltage, +5 V to +10 V.
13	RTD1	Constant Current Output. A nominal 200 μA constant current is provided at this pin and this can be used as the excitation current for RTDs. This current can be turned on or off via the control register.
14	REF IN(−)	Reference Input. The REF IN(−) can lie anywhere between AV_{DD} and AGND provided REF IN(+) is greater than REF IN(−).
15	REF IN(+)	Reference Input. The reference input is differential with the proviso that REF IN(+) must be greater than REF IN(−). REF IN(+) can lie anywhere between AV_{DD} and AGND.
16	RTD2	Constant Current Output. A nominal 200 μA constant current is provided at this pin and this can be used as the excitation current for RTDs. This current can be turned on or off via the control register. This second current can be used to eliminate lead resistance errors in three-wire RTD configurations.
17	AIN3	Analog Input Channel 3. High level analog input which accepts an analog input voltage range of $\pm 4 \times V_{REF}/GAIN$. At the nominal V_{REF} of +2.5 V and a gain of 1, the AIN3 input voltage range is ±10 V.
18	AGND	Ground Reference Point for Analog Circuitry.
19	$\overline{TFS}$	Transmit Frame Synchronization. Active low logic input used to write serial data to the device with serial data expected after the falling edge of this pulse. In the Self-Clocking mode, the serial clock becomes active after $\overline{TFS}$ goes low. In the External Clocking mode, $\overline{TFS}$ must go low before the first bit of the data word is written to the part.
20	$\overline{RFS}$	Receive Frame Synchronization. Active low logic input used to access serial data from the device. In the self-clocking mode, the SCLK and SDATA lines both become active after $\overline{RFS}$ goes low. In the external clocking mode, the SDATA line becomes active after $\overline{RFS}$ goes low.
21	$\overline{DRDY}$	Logic Output. A falling edge indicates a new output word is available for transmission. The $\overline{DRDY}$ pin will return high upon completion of transmission of a full output word. $\overline{DRDY}$ is also used to indicate when the AD7713 has completed its on-chip calibration sequence.

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Pin	Mnemonic	Function
22	SDATA	Serial Data. Input/Output with serial data being written to either the control register or the calibration registers and serial data being accessed from the control register, calibration registers or the data register. During a read operation, serial data becomes active after $\overline{RFS}$ goes low. During a write operation, valid serial data is expected on the rising edges of SCLK when $\overline{TFS}$ is low.
23	DV_{DD}	Digital Supply Voltage, +5 V. DV_{DD} should never exceed AV_{DD} by more than 0.3 V. If DV_{DD} powers up before AV_{DD} or if DV_{DD} can exceed AV_{DD} by more than 0.3 V at any other time, a Schottky diode should be placed between the two pins.
24	DGND	Ground Reference Point for Digital Circuitry.

PIN CONFIGURATION

DIP and SOIC



Table III. Input Sampling Frequency vs. Gain

Gain	Input Sampling Freq (FS)
1	$f_{CLK\ IN}$ /512 (4 kHz @ $f_{CLK\ IN}$ = 2 MHz)
2	2 × $f_{CLK\ IN}$/512 (8 kHz @ $f_{CLK\ IN}$ = 2 MHz)
4	4 × $f_{CLK\ IN}$/512 (16 kHz @ $f_{CLK\ IN}$ = 2 MHz)
8	4 × $f_{CLK\ IN}$/512 (32 kHz @ $f_{CLK\ IN}$ = 2 MHz)
16	4 × $f_{CLK\ IN}$/512 (32 kHz @ $f_{CLK\ IN}$ = 2 MHz)
32	4 × $f_{CLK\ IN}$/512 (32 kHz @ $f_{CLK\ IN}$ = 2 MHz)
64	4 × $f_{CLK\ IN}$/512 (32 kHz @ $f_{CLK\ IN}$ = 2 MHz)
128	4 × $f_{CLK\ IN}$/512 (32 kHz @ $f_{CLK\ IN}$ = 2 MHz)

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LC²MOS
High Speed 1-, 4- & 8-Channel 10-Bit ADCs
AD7776/AD7777/AD7778*

FEATURES
AD7776: Single Channel
AD7777: 4-Channel
AD7778: 8-Channel
Fast 10-Bit 1.75 μs ADC
+5 V Only
Reference Conversion Option
Fast Interface Port
Power-Down Mode

APPLICATIONS
HDD Servos
Instrumentation

GENERAL DESCRIPTION

The AD7776, AD7777 and AD7778 are a family of high speed multichannel, 10-bit ADCs primarily intended for use in R/W head positioning servos found in high density hard disc drives. They have unique input signal conditioning features which make them ideal for use in such single supply applications.

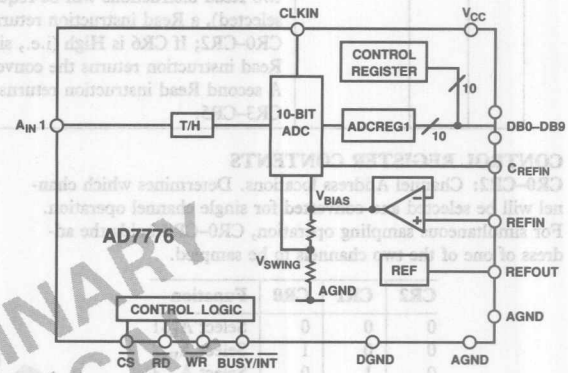
By setting a bit in a control register within both the four-channel version, AD7777, and eight-channel version, AD7778, the input channels can either be independently sampled or any two channels of choice can be simultaneously sampled. For all versions an input signal of the form $V_{BIAS} \pm V_{SWING}$ is expected. The voltage V_{BIAS} is the offset of the ADC's midpoint code from ground and is supplied either by an onboard reference available to the user (REFOUT) or by an external voltage reference applied to REFIN. The full-scale range (FSR) of the ADC is equal to $2V_{SWING}$ where V_{SWING} is nominally equal to REFIN/2. Additionally, when placed in the Calibration Mode, the value of REFIN is converted. This allows the channel offset(s) to be measured.

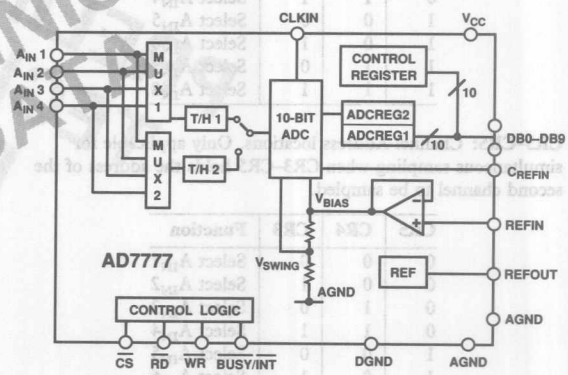
Control register loading and ADC register reading, channel select and conversion start are under the control of the μP. The two's complemented coded ADCs are easily interfaced to a standard 16-bit MPU bus via their 10-bit data port and standard microprocessor control lines.

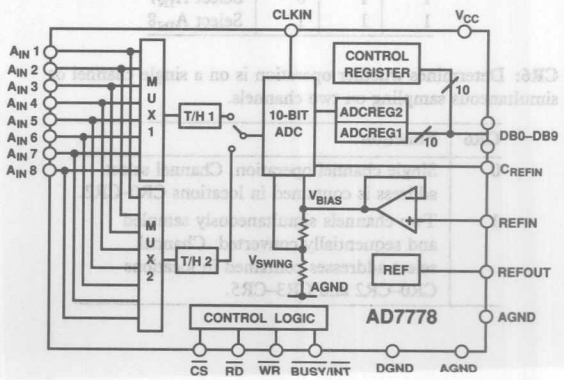
They are fabricated in linear compatible CMOS (LC²CMOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The AD7776 is available in both 24-pin DIP and 24-pin SOIC packages; the AD7777 is available in both 28-pin DIP and 28-pin SOIC packages; the AD7778 is available in a 44-pin PQFP package.

***Protected by U.S. Patent No. 4,990,916.**

FUNCTIONAL BLOCK DIAGRAMS







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CS	RD	WR	DB0–DB9	Function/Comments
1	X	X	HIGH	Data Port High Impedance
0	1	0	CR Data	Load Control Register (CR) data to Control Register and start a conversion. The contents of the Control Register are described below.
0	0	1	ADC Data	ADC data placed on data bus. Depending upon location CR6 of the Control Register, one or two Read instructions will be required: If CR6 is Low (i.e., single channel conversion selected), a Read instruction returns the conversion data for the channel previously selected by CR0–CR2; If CR6 is High (i.e., simultaneous sampling (double conversion) selected), the first Read instruction returns the conversion data for the channel previously selected by CR0–CR2. A second Read instruction returns the conversion data for the channel previously selected by CR3–CR5.

CONTROL REGISTER CONTENTS

CR0–CR2: Channel Address locations. Determines which channel will be selected and converted for single channel operation. For simultaneous sampling operation, CR0–CR2 holds the address of one of the two channels to be sampled.

CR2	CR1	CR0	Function
0	0	0	Select $A_{IN}1$
0	0	1	Select $A_{IN}2$
0	1	0	Select $A_{IN}3$
0	1	1	Select $A_{IN}4$
1	0	0	Select $A_{IN}5$
1	0	1	Select $A_{IN}6$
1	1	0	Select $A_{IN}7$
1	1	1	Select $A_{IN}8$

CR3–CR5: Channel Address locations. Only applicable for simultaneous sampling when CR3–CR5 holds the address of the second channel to be sampled.

CR5	CR4	CR3	Function
0	0	0	Select $A_{IN}1$
0	0	1	Select $A_{IN}2$
0	1	0	Select $A_{IN}3$
0	1	1	Select $A_{IN}4$
1	0	0	Select $A_{IN}5$
1	0	1	Select $A_{IN}6$
1	1	0	Select $A_{IN}7$
1	1	1	Select $A_{IN}8$

CR6: Determines whether operation is on a single channel or simultaneous sampling on two channels.

CR6	Function
0	Single channel operation. Channel select address is contained in locations CR0–CR2.
1	Two channels simultaneously sampled and sequentially converted. Channel select addresses contained in locations CR0–CR2 and CR3–CR5.

CR7: Determines whether the device is in the Normal Operating mode or in the Calibration mode:

CR7	Function
0	Normal Operating Mode
1	Calibration Mode

In the Calibration mode REFIN is internally connected as an analog input(s).

CR8: Determines whether the device is in the Normal Operating mode or in the Power-Down mode;

CR8	Function
0	Normal Operating Mode
1	Power-Down Mode

CR9: Determines whether $\overline{\text{BUSY/INT}}$ output flag goes Low and remains Low during conversion(s) or else goes Low and remains Low after the conversion(s) is (are) complete.

CR9	$\overline{\text{BUSY/INT}}$ Functionality
0	Output goes Low and remains Low during conversion(s).
1	Output goes Low and remains Low after conversion(s) is (are) complete.

PRELIMINARY TECHNICAL DATA

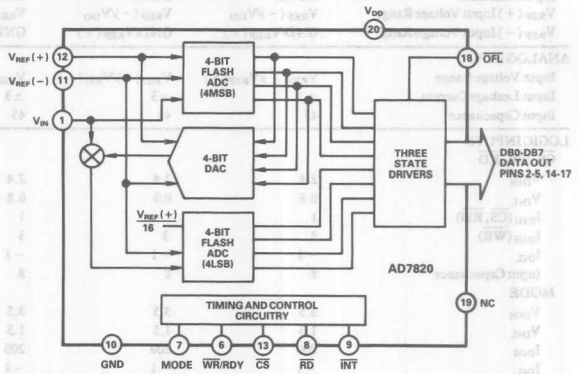
This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD7820

FEATURES

- Fast Conversion Time: 1.36μs max
- Built-In Track-and-Hold Function
- No Missed Codes
- No User Trims Required
- Single +5V Supply
- Ratiometric Operation
- No External Clock
- Extended Temperature Range Operation
- Skinny 20-Pin DIP, SOIC and 20-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7820 is a high speed, microprocessor-compatible 8-bit analog-to-digital converter which uses a half-flash conversion technique to achieve a conversion time of 1.36μs. The converter has a 0V to +5V analog input voltage range with a single +5V supply.

The half-flash technique consists of 31 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC. The input to the AD7820 is tracked and held by the input sampling circuitry, eliminating the need for an external sample-and-hold for signals with slew rates less than 100mV/μs.

The part is designed for ease of microprocessor interface with the AD7820 appearing as a memory location or I/O port without the need for external interfacing logic. All digital outputs use latched, three-state output buffer circuitry to allow direct connection to a microprocessor data bus or system input port. A non-three state overflow output is also provided to allow cascading of devices to give higher resolution.

The AD7820 is fabricated in an advanced, all ion-implanted, high speed, Linear Compatible CMOS (LC^2MOS) process and features a low maximum power dissipation of 75mW. It is available in 20-pin DIPs, SOICs and in 20-terminal surface mount packages.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time
   The half-flash conversion technique, coupled with fabrication on Analog Devices' LC^2MOS process, enables very fast conversion times. The maximum conversion time for the WR-RD mode is 1.36μs, with 1.6μs the maximum for the RD mode.
2. Total Unadjusted Error
   The AD7820 features an excellent total unadjusted error figure of less than 1/2LSB over the full operating temperature range. The part is also guaranteed to have no missing codes over the entire temperature range.
3. Built-In Track-and-Hold
   The analog input circuitry uses sampled-data comparators, which by nature have a built-in track-and-hold function. As a result, input signals with slew rates up to 100mV/μs can be converted to 8-bits without external sample-and-hold. This corresponds to a 5V peak-to-peak, 7kHz sine-wave signal.
4. Single Supply
   Operation from a single +5V supply with a positive voltage reference allows operation of the AD7820 in microprocessor systems without any additional power supplies.

AD7820—SPECIFICATIONS

(V_{DD} = +5V; V_{REF} (+) = +5V; V_{REF} (−) = GND = 0V unless otherwise stated). All specifications T_{min} to T_{max} unless otherwise specified. Specifications apply for RD Mode (Pin 7 = 0V)

Parameter	K Version[1]	L Version	B, T Versions	C, U Versions	Units	Conditions/Comments
ACCURACY						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[2]	±1	±1/2	±1	±1/2	LSB max	
Minimum Resolution for which No Missing Codes are guaranteed	8	8	8	8	Bits	
REFERENCE INPUT						
Input Resistance	1.0/4.0	1.0/4.0	1.0/4.0	1.0/4.0	kΩ min/kΩ max	
V_{REF}(+) Input Voltage Range	V_{REF}(−)/V_{DD}	V_{REF}(−)/V_{DD}	V_{REF}(−)/V_{DD}	V_{REF}(−)/V_{DD}	V min/V max	
V_{REF}(−) Input Voltage Range	GND/V_{REF}(+)	GND/V_{REF}(+)	GND/V_{REF}(+)	GND/V_{REF}(+)	V min/V max	
ANALOG INPUT						
Input Voltage Range	V_{REF}(−)/V_{REF}(+)	V_{REF}(−)/V_{REF}(+)	V_{REF}(−)/V_{REF}(+)	V_{REF}(−)/V_{REF}(+)	V min/V max	
Input Leakage Current	±3	±3	±3	±3	μA max	
Input Capacitance[3]	45	45	45	45	pF typ	
LOGIC INPUTS						
$\overline{CS}$, $\overline{WR}$, $\overline{RD}$						
V_{INH}	2.4	2.4	2.4	2.4	V min	
V_{INL}	0.8	0.8	0.8	0.8	V max	
I_{INH} ($\overline{CS}$, $\overline{RD}$)	1	1	1	1	μA max	
I_{INH} ($\overline{WR}$)	3	3	3	3	μA max	
I_{INL}	−1	−1	−1	−1	μA max	
Input Capacitance[3]	8	8	8	8	pF max	Typically 5pF
MODE						
V_{INH}	3.5	3.5	3.5	3.5	V min	
V_{INL}	1.5	1.5	1.5	1.5	V max	
I_{INH}	200	200	200	200	μA max	50 μA typ
I_{INL}	−1	−1	−1	−1	μA max	
Input Capacitance[3]	8	8	8	8	pF max	Typically 5pF
LOGIC OUTPUTS						
DB0-DB7, $\overline{OFL}$, $\overline{INT}$						
V_{OH}	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 360μA
V_{OL}	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
I_{OUT} (DB0–DB7)	±3	±3	±3	±3	μA max	Floating State Leakage
Output Capacitance[3]	8	8	8	8	pF max	Typically 5pF
RDY						
V_{OL}	0.4	0.4	0.4	0.4	V max	I_{SINK} = 2.6mA
I_{OUT}	±3	±3	±3	±3	μA max	Floating State Leakage
Output Capacitance[3]	8	8	8	8	pF max	Typically 5pF
SLEW RATE, TRACKING[3]	0.2	0.2	0.2	0.2	V/μs typ	
	0.1	0.1	0.1	0.1	V/μs max	
POWER SUPPLY						
V_{DD}	5	5	5	5	Volts	±5% for Specified Performance
I_{DD}[4]	15	15	20	20	mA max	$\overline{CS}$ = $\overline{RD}$ = 0V
Power Dissipation	40	40	40	40	mW typ	
Power Supply Sensitivity	±1/4	±1/4	±1/4	±1/4	LSB max	±1/16LSB typ V_{DD} = 5V ±5%

NOTES

[1]Temperature Ranges are as follows:
K, L Versions: −40°C to +85°C
B, C Versions: −40°C to +85°C
T, U Versions: −55°C to +125°C

[2]Total Unadjusted Error includes offset, full-scale and linearity errors.

[3]Sample tested at 25°C by Product Assurance to ensure compliance.

[4]See Typical Performance Characteristics.

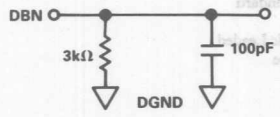
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5V; V_{REF}(+) = +5V; V_{REF}(−) = GND = 0V unless otherwise stated.)

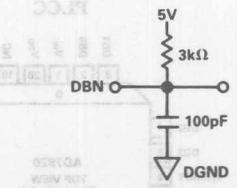
Parameter	Limit at 25°C (All Versions)	Limit at T_{min}, T_{max} (K, L, B, C Versions)	Limit at T_{min}, T_{max} (T, U Versions)	Units	Conditions/Comments
t_{CSS}	0	0	0	ns min	$\overline{CS}$ TO $\overline{RD}$/$\overline{WR}$ Setup Time
t_{CSH}	0	0	0	ns min	$\overline{CS}$ TO $\overline{RD}$/$\overline{WR}$ Hold Time
t_{RDY}[2]	70	90	100	ns max	$\overline{CS}$ to Delay. Pull-Up Resistor 5kΩ.
t_{CRD}	1.6	2.0	2.5	μs max	Conversion Time (RD Mode)
t_{ACC0}[3]	t_{CRD} + 20	t_{CRD} + 35	t_{CRD} + 50	ns max	Data Access Time (RD Mode)
t_{INTH}[2]	125	–	–	ns typ	$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)
	175	225	225	ns max	
t_{DH}[4]	60	80	100	ns max	Data Hold Time
t_P	500	600	600	ns min	Delay Time between Conversions
t_{WR}	600	600	600	ns min	Write Pulse Width
	50	50	50	μs max	
t_{RD}	600	700	700	ns min	Delay Time between $\overline{WR}$ and $\overline{RD}$ Pulses
t_{ACC1}[3]	160	225	250	ns max	Data Access Time (WR–RD Mode, see Fig. 5b)
t_{R1}	140	200	225	ns max	$\overline{RD}$ to $\overline{INT}$ Delay
t_{INTL}[2]	700	–	–	ns typ	$\overline{WR}$ to $\overline{INT}$ Delay
	1000	1400	1700	ns max	
t_{ACC2}[3]	70	90	110	ns max	Data Access Time (WR–RD Mode, see Fig. 5a)
t_{IHWR}[2]	100	130	150	ns max	$\overline{WR}$ to $\overline{INT}$ Delay (Stand-Alone Operation)
t_{ID}	50	65	75	ns max	Data Access Time after $\overline{INT}$ (Stand-Alone Operation)

NOTES
[1]Sample tested at 25°C to ensure compliance. All input control signals are specified with tr = tf = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]C_L = 50pF.
[3]Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[4]Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.

Test Circuits

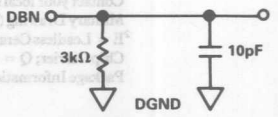


a. High-Z to V_{OH}

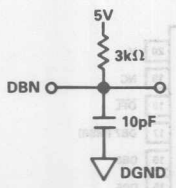


b. High-Z to V_{OL}

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High-Z



b. V_{OL} to High-Z

Figure 2. Load Circuits for Data Hold Time Test

Digital Input Voltage to GND
(Pins 6-8, 13) . . . . . −0.3V, V_{DD} +0.3V
Digital Output Voltage to GND
(Pins 2-5, 9, 14-18) . . . . . −0.3V, V_{DD} +0.3V
V_{REF} (+) to GND . . . . . V_{REF} (−), V_{DD} +0.3V
V_{REF} (−) to GND . . . . . 0V, V_{REF} (+)
V_{IN} to GND . . . . . −0.3V, V_{DD} +0.3V
Operating Temperature Range
Commercial (K, L Versions) . . . . . −40°C to +85°C
Industrial (B, C Versions) . . . . . −40°C to +85°C
Extended (T, U Versions) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C 450mW
Derates above +75°C by . . . . . 6mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



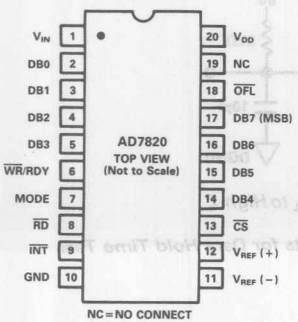
ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error (Max)	Package Option[2]
AD7820KN	−40°C to +85°C	±1LSB	N-20
AD7820LN	−40°C to +85°C	±1/2LSB	N-20
AD7820KP	−40°C to +85°C	±1LSB	P-20A
AD7820LP	−40°C to +85°C	±1/2LSB	P-20A
AD7820KR	−40°C to +85°C	±1LSB	R-20
AD7820LR	−40°C to +85°C	±1/2LSB	R-20
AD7820BQ	−40°C to +85°C	±1LSB	Q-20
AD7820CQ	−40°C to +85°C	±1/2LSB	Q-20
AD7820TQ	−55°C to +125°C	±1LSB	Q-20
AD7820UQ	−55°C to +125°C	±1/2LSB	Q-20
AD7820TE	−55°C to +125°C	±1LSB	E-20A
AD7820UE	−55°C to +125°C	±1/2LSB	E-20A

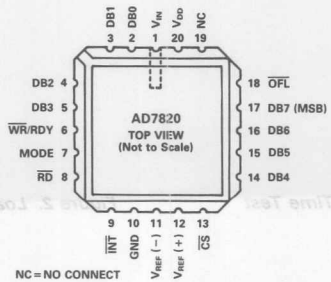
NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD), see DESC drawing #5962-88650.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

PIN CONFIGURATIONS

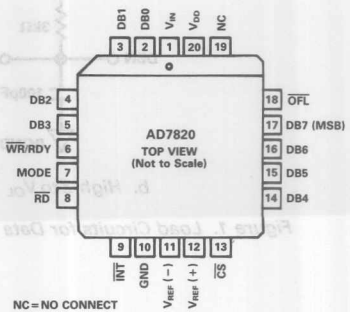
DIP, SOIC



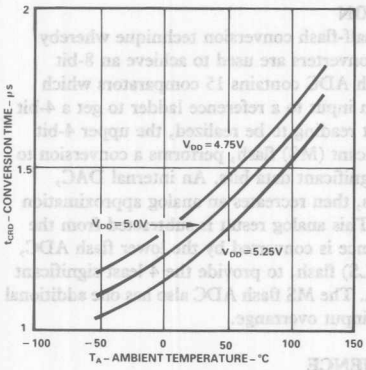
LCCC



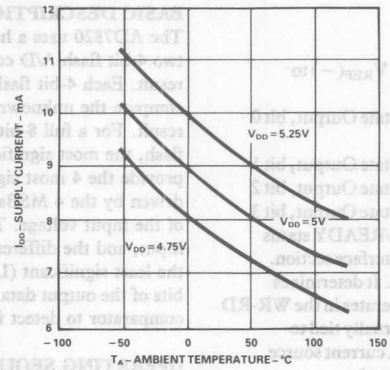
PLCC



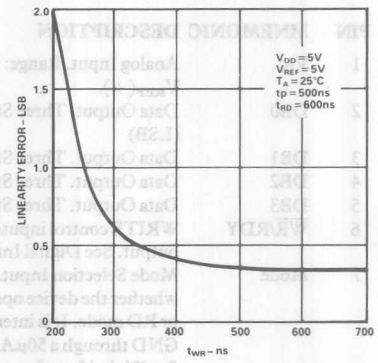
Typical Performance Characteristics—AD7820



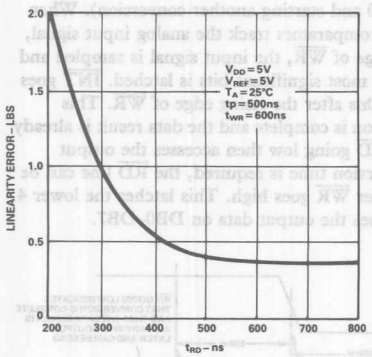
Conversion Time (RD Model) vs. Temperature



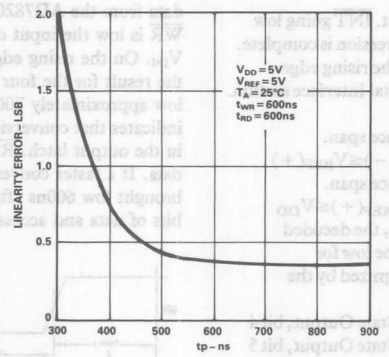
Power Supply Current vs. Temperature (not including reference ladder)



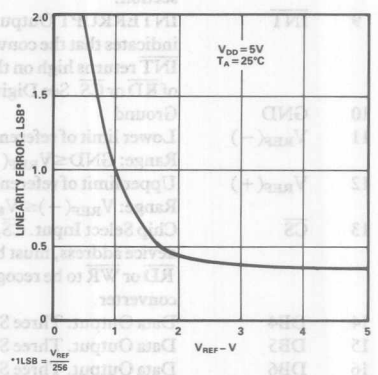
Accuracy vs. t_{WR}



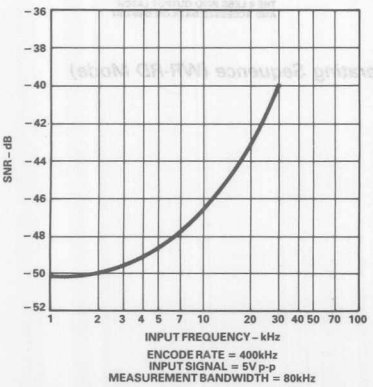
Accuracy vs. t_{RD}



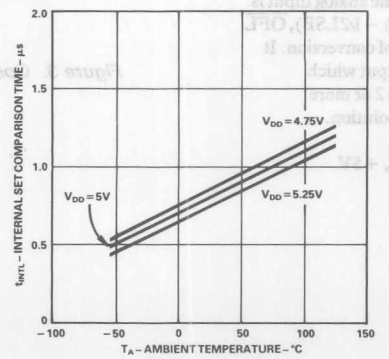
Accuracy vs. tp



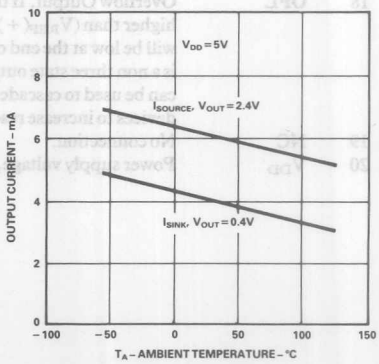
Accuracy vs V_{REF}
[V_{REF} = V_{REF}(+) – V_{REF}(–)]



Signal-Noise Ratio vs. Input Frequency



t_{INTL}, Internal Time Delay vs. Temperature



Output Current vs. Temperature

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	V_{IN}	Analog Input. Range: $V_{REF}(-)$ to $V_{REF}(+)$.
2	DB0	Data Output. Three State Output, bit 0 (LSB)
3	DB1	Data Output. Three State Output, bit 1
4	DB2	Data Output. Three State Output, bit 2
5	DB3	Data Output. Three State Output, bit 3
6	$\overline{WR}$/RDY	WRITE control input/READY status output. See Digital Interface section.
7	Mode	Mode Selection Input. It determines whether the device operates in the WR-RD or RD mode. It is internally tied to GND through a 50μA current source. See Digital Interface section.
8	$\overline{RD}$	READ Input. $\overline{RD}$ must be low to access data from the part. See Digital Interface section.
9	$\overline{INT}$	INTERRUPT Output. $\overline{INT}$ going low indicates that the conversion is complete. $\overline{INT}$ returns high on the rising edge of $\overline{RD}$ or $\overline{CS}$. See Digital Interface section.
10	GND	Ground
11	$V_{REF}(-)$	Lower limit of reference span. Range: $GND \leq V_{REF}(-) \leq V_{REF}(+)$
12	$V_{REF}(+)$	Upper limit of reference span. Range: $V_{REF}(-) \leq V_{REF}(+) \leq V_{DD}$
13	$\overline{CS}$	Chip Select Input. $\overline{CS}$, the decoded device address, must be low for $\overline{RD}$ or $\overline{WR}$ to be recognized by the converter.
14	DB4	Data Output. Three State Output, bit 4
15	DB5	Data Output. Three State Output, bit 5
16	DB6	Data Output. Three State Output, bit 6
17	DB7	Data Output. Three State Output, bit 7 (MSB)
18	$\overline{OFL}$	Overflow Output. If the analog input is higher than ($V_{REF}(+) - 1/2$LSB), $\overline{OFL}$ will be low at the end of conversion. It is a non three state output which can be used to cascade 2 or more devices to increase resolution.
19	NC	No connection.
20	V_{DD}	Power supply voltage, +5V

CIRCUIT INFORMATION

BASIC DESCRIPTION

The AD7820 uses a half-flash conversion technique whereby two 4-bit flash A/D converters are used to achieve an 8-bit result. Each 4-bit flash ADC contains 15 comparators which compare the unknown input to a reference ladder to get a 4-bit result. For a full 8-bit reading to be realized, the upper 4-bit flash, the most significant (MS) flash, performs a conversion to provide the 4 most significant data bits. An internal DAC, driven by the 4 MSBs, then recreates an analog approximation of the input voltage. This analog result is subtracted from the input, and the difference is converted by the lower flash ADC, the least significant (LS) flash, to provide the 4 least significant bits of the output data. The MS flash ADC also has one additional comparator to detect input overrange.

OPERATING SEQUENCE

The operating sequence for the AD7820 in the WR-RD mode is shown in Figure 3. A set-up time of 500ns is required prior to the falling edge of $\overline{WR}$. (This 500ns is required between reading data from the AD7820 and starting another conversion). When $\overline{WR}$ is low the input comparators track the analog input signal, V_{IN}. On the rising edge of $\overline{WR}$, the input signal is sampled and the result for the four most significant bits is latched. $\overline{INT}$ goes low approximately 700ns after the rising edge of $\overline{WR}$. This indicates that conversion is complete and the data result is already in the output latch. $\overline{RD}$ going low then accesses the output data. If a faster conversion time is required, the $\overline{RD}$ line can be brought low 600ns after $\overline{WR}$ goes high. This latches the lower 4 bits of data and accesses the output data on DB0–DB7.

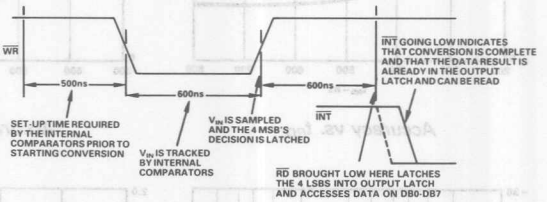


Figure 3. Operating Sequence (WR-RD Mode)

DIGITAL INTERFACE

The AD7820 has two basic interface modes which are determined by the status of the MODE pin. When this pin is low the converter is in the RD mode, with this pin high the AD7820 is set up for the WR-RD mode.

RD Mode

The timing diagram for the RD mode is shown in Figure 4. In the RD mode configuration, conversion is initiated by taking $\overline{RD}$ low. The $\overline{RD}$ line is then kept low until output data appears. It is very useful with microprocessors which can be forced into a WAIT state, with the microprocessor starting a conversion, waiting, and then reading data with a single READ instruction. In this mode, pin 6 of the AD7820 is configured as a status output, RDY. This RDY output can be used to drive the processor READY or WAIT input. It is an open drain output (no internal pull-up device) which goes low after the falling edge of $\overline{CS}$ and goes high impedance at the end of conversion. An $\overline{INT}$ line is also provided which goes low at the completion of conversion. $\overline{INT}$ returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

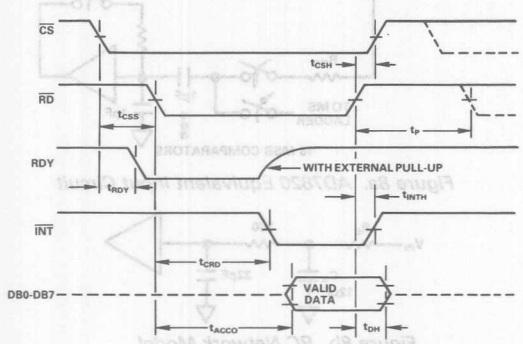


Figure 4. RD Mode

WR-RD Mode

In the WR-RD mode, pin 6 is configured as the WRITE input for the AD7820. With $\overline{CS}$ low, conversion is initiated on the falling edge of $\overline{WR}$. Two options exist for reading data from the converter.

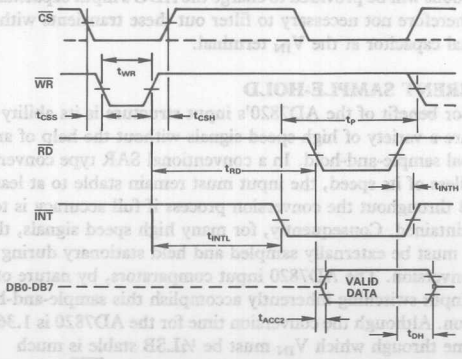


Figure 5a. WR-RD Mode ($t_{RD} > t_{INTL}$)

In the first of these options the processor waits for the $\overline{INT}$ status line to go low before reading the data (see Figure 5a). $\overline{INT}$ typically goes low 700ns after the rising edge of $\overline{WR}$. It indicates that conversion is complete and that the data result is in the output latch. With $\overline{CS}$ low, the data outputs (DB0-DB7) are activated when $\overline{RD}$ goes low. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$.

The alternative option can be used to shorten the conversion time. To achieve this, the status of the $\overline{INT}$ line is ignored and $\overline{RD}$ can be brought low 600ns after the rising edge of $\overline{WR}$. In this case $\overline{RD}$ going low transfers the data result into the output latch and activates the data outputs (DB0-DB7). $\overline{INT}$ also goes low on the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. The timing for this interface is shown in Figure 5b.

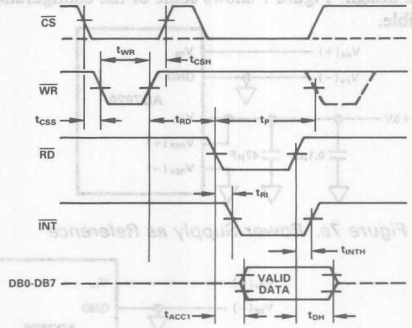


Figure 5b. WR-RD Mode ($t_{RD} < t_{INTL}$)

The AD7820 can also be used in stand-alone operation in the WR-RD mode. $\overline{CS}$ and $\overline{RD}$ are tied low and a conversion is initiated by bringing $\overline{WR}$ low. Output data is valid typically 700ns after the rising edge of $\overline{WR}$. The timing diagram for this mode is shown in Figure 6.

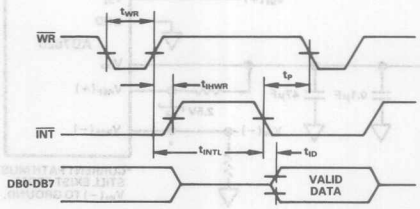


Figure 6. WR-RD Mode Stand-Alone Operation, $\overline{CS} = \overline{RD} = 0$

APPLYING THE AD7820

REFERENCE AND INPUT

The two reference inputs on the AD7820 are fully differential and define the zero to full-scale input range of the A/D converter. As a result, the span of the analog input can easily be varied since this range is equivalent to the voltage difference between $V_{IN}(+)$ and $V_{IN}(-)$. By reducing the reference span, $V_{REF}(+)-V_{REF}(-)$, to less than 5V the sensivity of the converter can be increased (i.e., if $V_{REF} = 2V$ then 1LSB = 7.8mV). The input/reference arrangement also facilitates ratiometric operation.

This reference flexibility also allows the input span to be offset from zero. The voltage at $V_{REF}(-)$ sets the input level which produces a digital output of all zeroes. Therefore, although V_{IN} is not itself differential, it will have nearly differential-input capability in most measurement applications because of the reference design. Figure 7 shows some of the configurations that are possible.

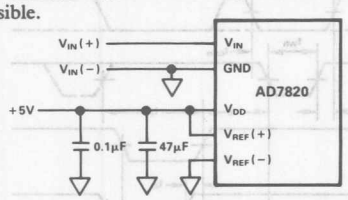


Figure 7a. Power Supply as Reference

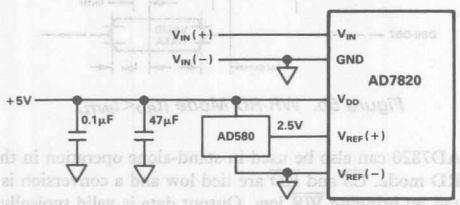


Figure 7b. External Reference 2.5V Full Scale

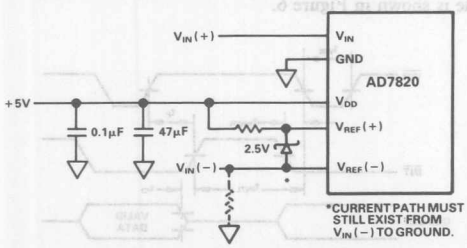


Figure 7c. Input Not Referenced to GND

INPUT CURRENT

Due to the novel conversion techniques employed by the AD7820, the analog input behaves somewhat differently than in conventional devices. The ADC's sampled-data comparators take varying amounts of input current depending on which cycle the conversion is in.

The equivalent input circuit of the AD7820 is shown in Figure 8a. When a conversion starts ($\overline{WR}$ low, WR-RD mode), all input switches close, and V_{IN} is connected to the most significant and least significant comparators. Therefore, V_{IN} is connected to thirty one 1pF input capacitors at the same time.

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 2kΩ to 5kΩ). In addition, about 12pF of input stray capacitance must be charged. For large source resistances, the analog input can be modelled as an RC network as shown in Figure 8b. As R_S increases, it takes longer for the input capacitance to charge.

In the RD mode, the time for which the input comparators track the analog input is 600ns at the start of conversion. In the WR-RD mode the input comparators track V_{IN} for the duration of the $\overline{WR}$ pulse. Since other factors cause this time to be at least 600ns, input time constants of 100ns can be accommodated without special consideration. Typical total input capacitance values of 45pF allow R_S to be 1.5kΩ without lengthening $\overline{WR}$ to give V_{IN} more time to settle.

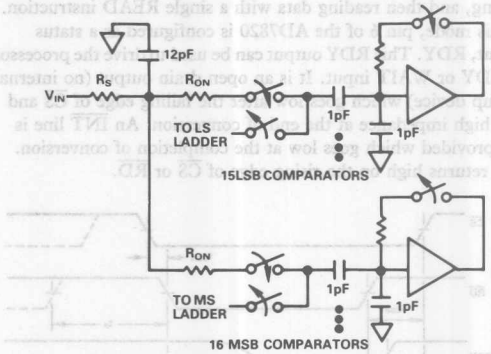


Figure 8a. AD7820 Equivalent Input Circuit

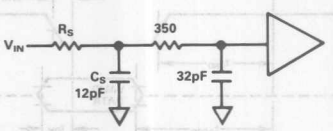


Figure 8b. RC Network Model

INPUT FILTERING

It should be made clear that transients on the analog input signal, caused by charging current flowing into V_{IN} will not normally degrade the ADC's performance. In effect, the AD7820 does not "look" at the input when these transients occur. The comparators' outputs are not latched while $\overline{WR}$ is low, so at least 600ns will be provided to charge the ADC's input capacitance. It is therefore not necessary to filter out these transients with an external capacitor at the V_{IN} terminal.

INHERENT SAMPLE-HOLD

A major benefit of the AD7820's input structure is its ability to measure a variety of high speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain stable to at least ½LSB throughout the conversion process if full accuracy is to be maintained. Consequently, for many high speed signals, this signal must be externally sampled and held stationary during the conversion. The AD7820 input comparators, by nature of their input switching inherently accomplish this sample-and-hold function. Although the conversion time for the AD7820 is 1.36µs, the time through which V_{IN} must be ½LSB stable is much smaller. The AD7820 "samples" V_{IN} only when $\overline{WR}$ is low. The value of V_{IN} approximately 100ns (internal propogation delay) after the rising edge of $\overline{WR}$ is the measured value. This value is then used in the least significant flash to generate the lower 4-bits of data.

Input signals with slew rates typically below 200mV/μs can be converted without error. However, because of the input time constants, and charge injection through the opened comparator input switches, faster signals may cause errors. Still, the AD7820's loss in accuracy for a given increase in signal slope is far less than what would be witnessed in a conventional successive approximation device. A SAR type converter with a conversion time as fast as 1μs would still not be able to measure a 5V, 1kHz sine wave without the aid of an external sample-and-hold. The AD7820 with no such help, can typically measure 5V, 10kHz waveforms.

Applications

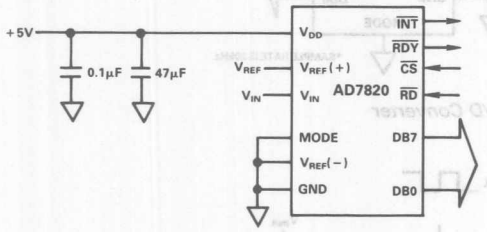


Figure 9a. 8-Bit Resolution

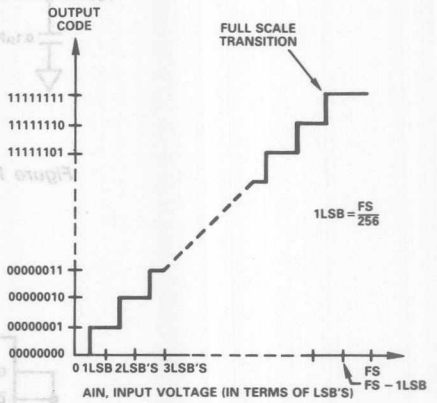


Figure 9b. Nominal Transfer Characteristic for 8-Bit Resolution Circuit

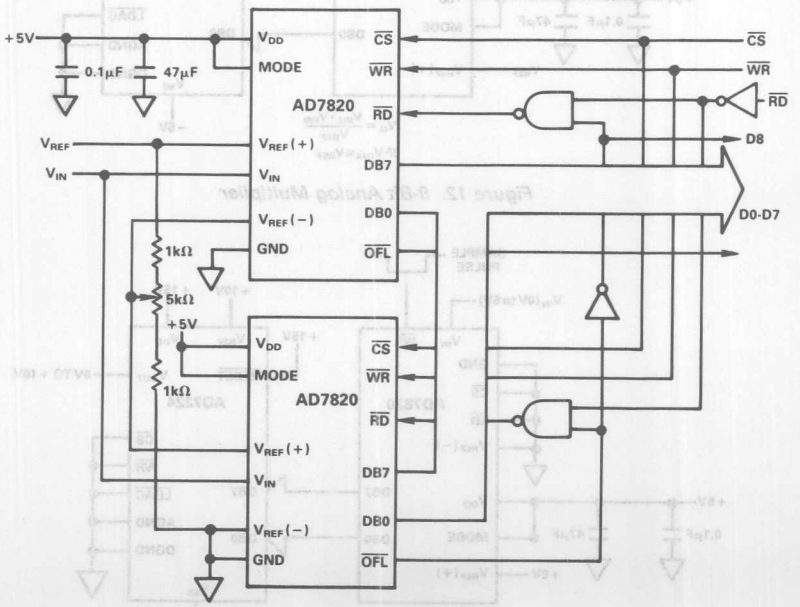


Figure 10. 9-Bit Resolution

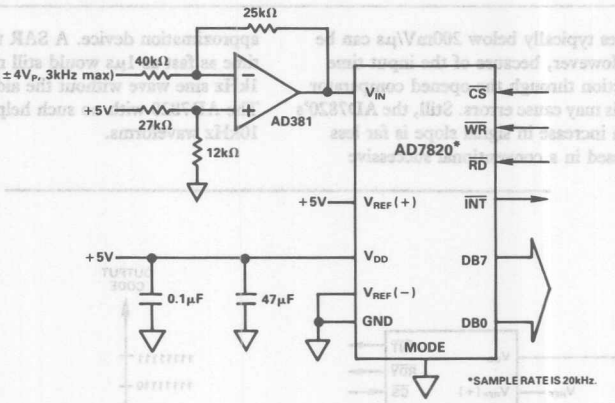


Figure 11. Telcom A/D Converter

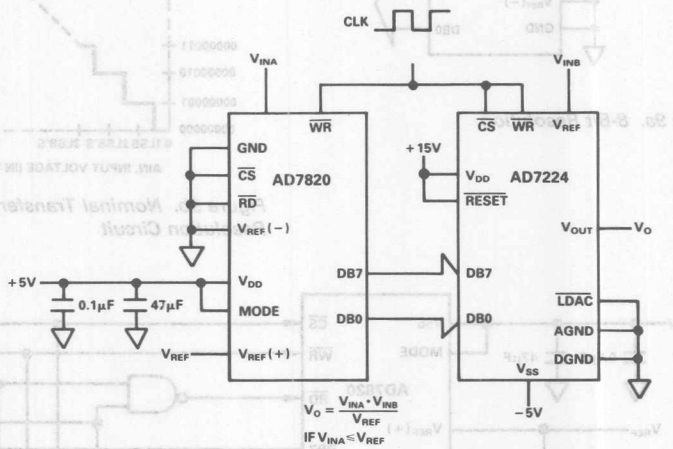


Figure 12. 8-Bit Analog Multiplier

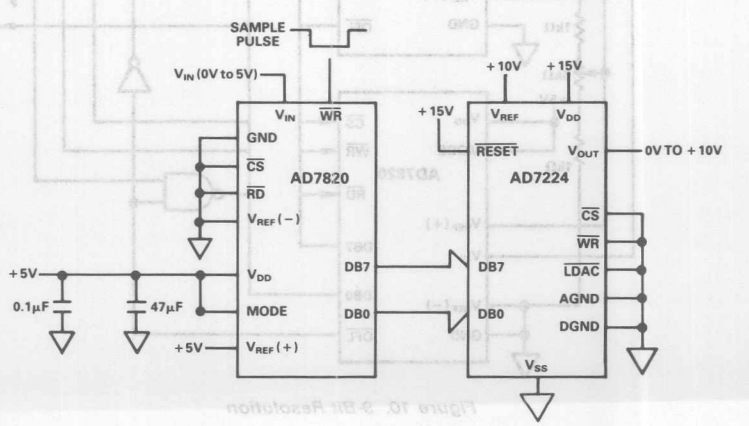


Figure 13. Fast Infinite Sample-and-Hold

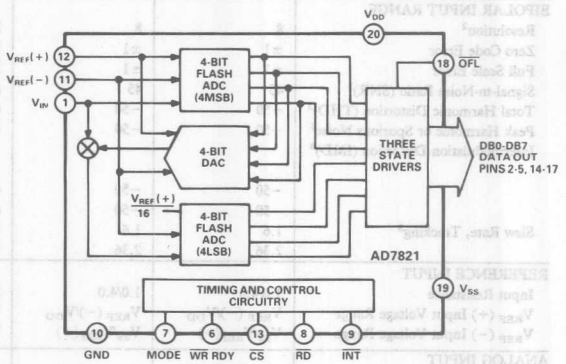
LC²MOS High Speed, µP-Compatible 8-Bit ADC with Track/Hold Function

AD7821

FEATURES

Fast Conversion Time: 660 ns max
100 kHz Track-and-Hold Function
1 MHz Sample Rate
Unipolar and Bipolar Input Ranges
Ratiometric Reference Inputs
No External Clock
Extended Temperature Range Operation
Skinny 20-Pin DIPs, SOIC and 20-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7821 is a high-speed, 8-bit, sampling, analog-to-digital converter that offers improved performance over the popular AD7820. It offers a conversion time of 660 ns (vs. 1.36 µs for the AD7820) and 100 kHz signal bandwidth (vs. 6.4 kHz). The sampling instant is better defined and occurs on the falling edge of $\overline{WR}$ or $\overline{RD}$. The provision of a V_{SS} pin (Pin 19) allows the part to operate from ±5 V supplies and to digitize bipolar input signals. Alternatively, for unipolar inputs, the V_{SS} pin can be grounded and the AD7821 will operate from a single +5 V supply, like the AD7820.

The AD7821 has a built-in track-and-hold function capable of digitizing full-scale signals up to 100 kHz max. It also uses a half-flash conversion technique that eliminates the need to generate a CLK signal for the ADC.

The AD7821 is designed with standard microprocessor control signals ($\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RDY, $\overline{INT}$) and latched, three-state data outputs capable of interfacing to high-speed data buses. An overflow output ($\overline{OFL}$) is also provided for cascading devices to achieve higher resolution.

The AD7821 is fabricated in Linear-Compatible CMOS (LC²MOS), an advanced, mixed technology process combining precision bipolar circuits with low-power CMOS logic. The part features a low power dissipation of 50 mW.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time
   The half-flash conversion technique, coupled with fabrication on Analog Devices' LC²MOS process, enables a very fast conversion time. The conversion time for the WR-RD mode is 660 ns, with 700 ns for the RD mode.
2. Built-In Track-and-Hold
   This allows input signals with slew rates up to 1.6 V/µs to be converted to 8-bits without an external track-and-hold. This corresponds to a 5 V peak-to-peak, 100 kHz sine-wave signal.
3. Total Unadjusted Error
   The AD7821 features an excellent total unadjusted error figure of less than ±1 LSB over the full operating temperature range.
4. Unipolar/Bipolar Input Ranges
   The AD7821 is specified for single supply (+5 V) operation with a unipolar full-scale range of 0 to +5 V, and for dual supply (±5 V) operation with a bipolar input range of ±2.5 V. Typical performance characteristics are given for other input ranges.
5. Dynamic Specifications for DSP Users
   In addition to the traditional ADC specifications, the AD7821 is specified for ac parameters, including signal-to-noise ratio, distortion and slew rate.

AD7821—SPECIFICATIONS

V_{DD} = +5 V ± 5%, GND = 0 V. Unipolar Input Range: V_{SS} = GND, $V_{REF}(+)$ = 5 V, $V_{REF}(-)$ = GND. Bipolar Input Range: V_{SS} = −5 V ± 5%, $V_{REF}(+)$ = 2.5 V, $V_{REF}(-)$ = −2.5 V. These test conditions apply unless otherwise stated. All specifications T_{min} to T_{max} unless otherwise stated. Specifications apply for RD Mode (Pin 7 = 0 V).

Parameter	K Version[1]	B, T Versions	Units	Comments
UNIPOLAR INPUT RANGE				
Resolution[2]	8	8	Bits	
Total Unadjusted Error[3]	±1	±1	LSB max	
Minimum Resolution for which No Missing Codes are Guaranteed	8	8	Bits	
BIPOLAR INPUT RANGE				
Resolution[2]	8	8	Bits	
Zero Code Error	±1	±1	LSB max	
Full Scale Error	±1	±1	LSB max	
Signal-to-Noise Ratio (SNR)[3]	45	45	dB min	V_{IN} = 99.85 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 500 kHz
Total Harmonic Distortion (THD)[3]	−50	−50	dB max	V_{IN} = 99.85 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 500 kHz
Peak Harmonic or Spurious Noise[3]	−50	−50	dB max	V_{IN} = 99.85 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 500 kHz
Intermodulation Distortion (IMD)[3]				fa (84.72 kHz) and fb (94.97 kHz) Full-Scale Sine Waves with $f_{SAMPLING}$ = 500 kHz
	−50	−50	dB max	Second Order Terms
	−50	−50	dB max	Third Order Terms
Slew Rate, Tracking[3]	1.6	1.6	V/μs max	
	2.36	2.36	V/μs typ	
REFERENCE INPUT				
Input Resistance	1.0/4.0	1.0/4.0	kΩ min/kΩ max	
V_{REF} (+) Input Voltage Range	V_{REF} (−)/V_{DD}	V_{REF} (−)/V_{DD}	V min/V max	
V_{REF} (−) Input Voltage Range	V_{SS}/V_{REF}(+)	V_{SS}/V_{REF}(+)	V min/V max	
ANALOG INPUT				
Input Voltage Range	V_{REF}(−)/V_{REF}(+)	V_{REF}(−)/V_{REF}(+)	V min/V max	
Input Leakage Current	±3	±3	μA max	−5 V ≤ V_{IN} ≤ +5 V
Input Capacitance	55	55	pF typ	
LOGIC INPUTS				
$\overline{CS}$, $\overline{WR}$, $\overline{RD}$				
V_{INH}	2.4	2.4	V min	
V_{INL}	0.8	0.8	V max	
I_{INH} ($\overline{CS}$, $\overline{RD}$)	1	1	μA max	
I_{INH} ($\overline{WR}$)	3	3	μA max	
I_{INL}	−1	−1	μA max	
Input Capacitance[4]	8	8	pF max	Typically 5 pF
MODE				
V_{INH}	3.5	3.5	V min	
V_{INL}	1.5	1.5	V max	
I_{INH}	200	200	μA max	50 μA typ
I_{INL}	−1	−1	μA max	
Input Capacitance[4]	8	8	pF max	Typically 5 pF
LOGIC OUTPUTS				
DB0–DB7, $\overline{OFL}$, $\overline{INT}$				
V_{OH}	4.0	4.0	V min	I_{SOURCE} = 360 μA
V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
I_{OUT} (DB0–DB7)	±3	±3	μA max	Floating State Leakage
Output Capacitance[4] (DB0–DB7)	8	8	pF max	Typically 5 pF
RDY				
V_{OL}	0.4	0.4	V max	I_{SINK} = 2.6 mA
I_{OUT}	±3	±3	μA max	Floating State Leakage
Output Capacitance[4]	8	8	pF max	Typically 5 pF
POWER SUPPLY				
I_{DD}[5]	15	20	mA max	$\overline{CS}$ = $\overline{RD}$ = 0 V
I_{SS}	100	100	μA max	$\overline{CS}$ = $\overline{RD}$ = 0 V
Power Dissipation	50	50	mW typ	
Power Supply Sensitivity	±1/4	±1/4	LSB max	±1/16 LSB typ, V_{DD} = 4.75 V to 5.25 V, (V_{REF}(+) = 4.75 V max for Unipolar Mode)

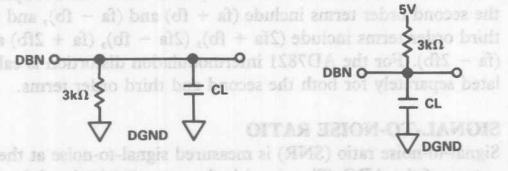
NOTES
[1]Temperature Ranges are as follows: K Version = −40°C to +85°C; B Version = −40°C to +85°C; T Version = −55°C to +125°C.
[2]1 LSB = 19.53 mV for both the unipolar (0 to +5 V) and bipolar (−2.5 V to +2.5 V) input ranges.
[3]See Terminology.
[4]Sample tested at +25°C to ensure compliance.
[5]See Typical Performance Characteristics.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5 V ± 5%, V_{SS} = 0 V or −5 V ± 5%; Unipolar or Bipolar Input Range)

Parameter	Limit at 25°C (All Versions)	Limit at T_{min}, T_{max} (K, B, Versions)	Limit at T_{min}, T_{max} (T Version)	Units	Conditions/Comments
t_{CSS}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}/\overline{WR}$ Setup Time
t_{CSH}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}/\overline{WR}$ Hold Time
t_{RDY}[2]	70	85	100	ns max	$\overline{CS}$ to RDY Delay. Pull-Up Resistor 5 kl.
t_{CRD}	700	875	975	ns max	Conversion Time (RD Mode)
t_{ACC0}[3]					Data Access Time (RD Mode)
	t_{CRD} +25	t_{CRD} +30	t_{CRD} +35	ns max	C_L = 20 pF
	t_{CRD} +50	t_{CRD} +65	t_{CRD} +75	ns max	C_L = 100 pF
t_{INTH}[2]	50	–	–	ns typ	$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)
	80	85	90	ns max	
t_{DH}[4]	15	15	15	ns min	Data Hold Time
	60	70	80	ns max	
t_P	350	425	500	ns min	Delay Time Between Conversions
t_{WR}	250	325	400	ns min	Write Pulse Width
	10	10	10	µs max	
t_{RD}	250	350	450	ns min	Delay Time between $\overline{WR}$ and $\overline{RD}$ Pulses
t_{READ1}	160	205	240	ns min	$\overline{RD}$ Pulse Width (WR–RD Mode, see Figure 12b) Determined by t_{ACC1}
t_{ACC1}[3]					Data Access Time (WR-RD Mode, see Figure 12b)
	160	205	240	ns max	C_L = 20 pF
	185	235	275	ns max	C_L = 100 pF
t_{RI}	150	185	220	ns max	$\overline{RD}$ to $\overline{INT}$ Delay
t_{INTL}[2]	380	-	-	ns typ	$\overline{WR}$ to $\overline{INT}$ Delay
	500	610	700	ns max	
t_{READ2}	65	75	85	ns min	$\overline{RD}$ Pulse Width (WR–RD Mode, see Figure 12a) Determined by t_{ACC2}
t_{ACC2}[3]					Data Access Time (WR–RD Mode, see Figure 12a)
	65	75	85	ns max	C_L = 20 pF
	90	110	130	ns max	C_L = 100 pF
t_{IHWR}[2]	80	100	120	ns max	$\overline{WR}$ to $\overline{INT}$ Delay (Stand-Alone Operation)
t_{ID}[3]					Data Access Time after $\overline{INT}$ (Stand-Alone Operation)
	30	35	40	ns max	C_L = 20 pF
	45	60	70	ns max	C_L = 100 pF

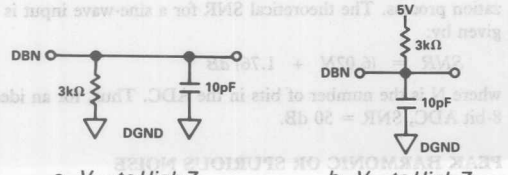
NOTES
[1]Sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[2]C_L = 50 pF.
[3]Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[4]Defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.

Test Circuits



a. High Z to V_{OH} b. High Z to V_{OL}

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High Z b. V_{OL} to High Z

Figure 2. Load Circuits for Data Hold Time Test

ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error (LSB)	Package Option[2]
AD7821KN	−40°C to +85°C	±1 max	N-20
AD7821KP	−40°C to +85°C	±1 max	P-20A
AD7821KR	−40°C to +85°C	±1 max	R-20
AD7821BQ	−40°C to +85°C	±1 max	Q-20
AD7821TQ	−55°C to +125°C	±1 max	Q-20
AD7821TE	−55°C to +125°C	±1 max	E-20A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact local sales office for military data sheet.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

Digital Input Voltage to GND
(Pins 6-8, 13). . . . . −0.3 V, V_{DD} +0.3 V
Digital Output Voltage to GND
(Pins 2-5, 9, 14-18). . . . . −0.3 V, V_{DD} +0.3 V
V_{REF} (+) to GND . . . . . V_{SS} −0.3 V, V_{DD} +0.3 V
V_{REF} (−) to GND . . . . . V_{SS} −0.3 V, V_{DD} +0.3 V
V_{IN} to GND. . . . . V_{SS} −0.3 V, V_{DD} +0.3 V
Operating Temperature Range
Commercial (K Version) . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 6 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

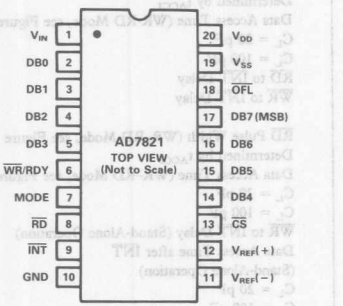
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

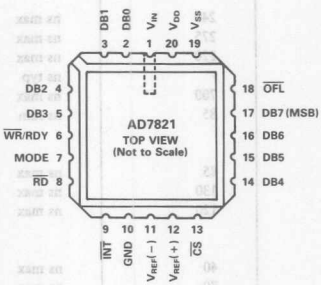


PIN CONFIGURATIONS

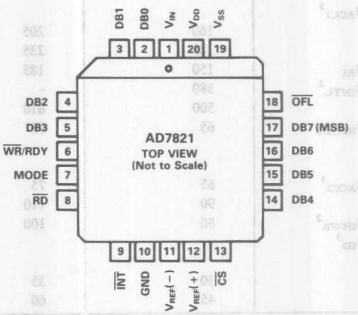
DIP AND SOIC



LCCC



PLCC



TERMINOLOGY

LEAST SIGNIFICANT BIT (LSB)

An ADC with 8-bit resolution can resolve one part in 2^8 (1/256 of full scale). For the AD7821 operating in either the unipolar or bipolar input range with 5 V full scale, one LSB is 19.53 mV.

TOTAL UNADJUSTED ERROR

This is a comprehensive specification which includes relative accuracy, offset error and full-scale error.

SLEW RATE

Slew Rate is the maximum allowable rate of change of input signal such that the digital sample values are not in error.

TOTAL HARMONIC DISTORTION

Total harmonic distortion is the ratio of the square root of the sum of the squares of the rms value of the harmonics to the rms value of the fundamental. For the AD7821, total harmonic distortion (THD) is defined as

$$20\ log\left[\frac{\sqrt{(V_2^2+V_3^2+V_5^2+V_6^2)}}{V_1}\right] dB$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, V_6, are the rms amplitudes of the individual harmonics.

INTERMODULATION DISTORTION

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mfa+nfb, where m,n = 0, 1, 2, 3,- - - -. Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms include (fa + fb) and (fa − fb), and the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb). For the AD7821 intermodulation distortion is calculated separately for both the second and third order terms.

SIGNAL-TO-NOISE RATIO

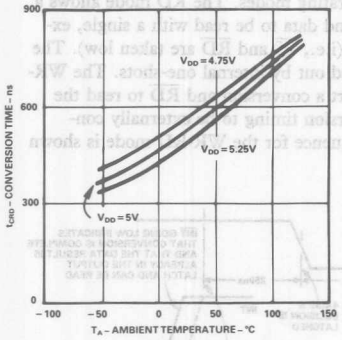
Signal-to-noise ratio (SNR) is measured signal-to-noise at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all nonfundamental signals (excluding dc) up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process. The theoretical SNR for a sine-wave input is given by:

$$SNR = (6.02N + 1.76)\ dB$$

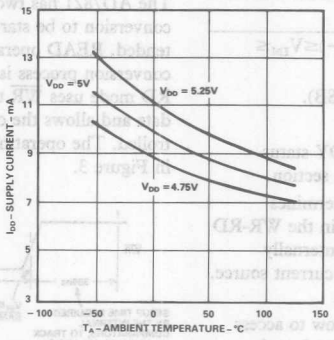
where N is the number of bits in the ADC. Thus, for an ideal 8-bit ADC, SNR = 50 dB.

PEAK HARMONIC OR SPURIOUS NOISE

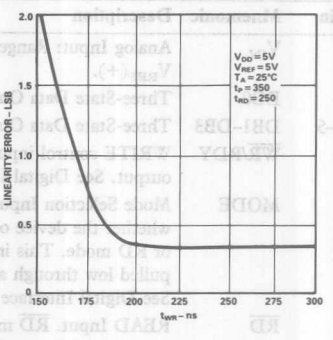
Peak harmonic or spurious noise is the rms value of the largest nonfundamental frequency (excluding dc) up to half the sampling frequency to the rms value of the fundamental.



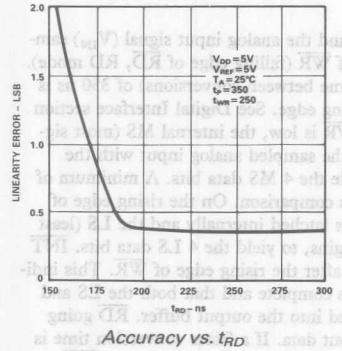
Conversion Time (RD Mode) vs. Temperature



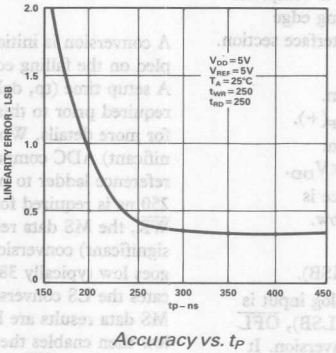
Power Supply Current vs. Temperature (Not Including Reference Ladder)



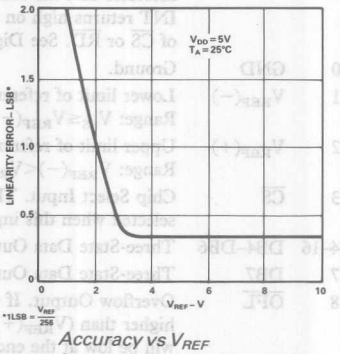
Accuracy vs. t_{WR}



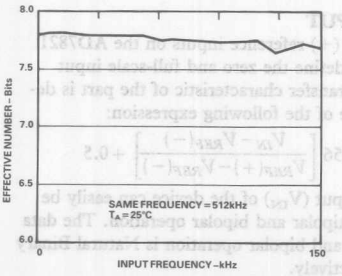
Accuracy vs. t_{RD}



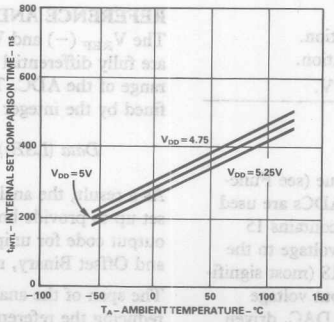
Accuracy vs. t_P



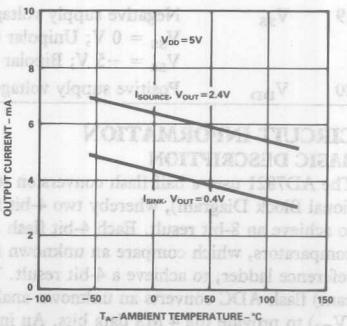
Accuracy vs V_{REF} [$V_{REF} = V_{REF}(+) - V_{REF}(-)$]



Effective Number of Bits vs. Input Signal (±2.5V) Frequency



t_{INTL}, Internal Time Delay vs. Temperature



Output Current vs. Temperature

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	V_{IN}	Analog Input: Range $V_{REF}(-) \le V_{IN} \le V_{REF}(+)$.
2	DB0	Three-State Data Output (LSB).
3–5	DB1–DB3	Three-State Data Outputs.
6	$\overline{WR}$/RDY	WRITE control input/READY status output. See Digital Interface section.
7	MODE	Mode Selection Input. It determines whether the device operates in the WR-RD or RD mode. This input is internally pulled low through a 50 μA current source. See Digital Interface section.
8	$\overline{RD}$	READ Input. $\overline{RD}$ must be low to access data from the part. See Digital Interface section.
9	$\overline{INT}$	INTERRUPT Output. $\overline{INT}$ going low indicates that the conversion is complete. $\overline{INT}$ returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$. See Digital Interface section.
10	GND	Ground.
11	$V_{REF}(-)$	Lower limit of reference span. Range: $V_{SS} \le V_{REF}(-) < V_{REF}(+)$.
12	$V_{REF}(+)$	Upper limit of reference span. Range: $V_{REF}(-) < V_{REF}(+) \le V_{DD}$.
13	$\overline{CS}$	Chip Select Input. The device is selected when this input is low.
14–16	DB4–DB6	Three-State Data Outputs.
17	DB7	Three-State Data Output (MSB).
18	$\overline{OFL}$	Overflow Output. If the analog input is higher than ($V_{REF}(+)$ −1/2 LSB), $\overline{OFL}$ will be low at the end of conversion. It is a non-three-state output which can be used to cascade 2 or more devices to increase resolution.
19	V_{SS}	Negative supply voltage. V_{SS} = 0 V; Unipolar Operation. V_{SS} = −5 V; Bipolar Operation.
20	V_{DD}	Positive supply voltage, +5 V.

CIRCUIT INFORMATION

BASIC DESCRIPTION

The AD7821 uses a half flash conversion technique (see Functional Block Diagram), whereby two 4-bit flash ADCs are used to achieve an 8-bit result. Each 4-bit flash ADC contains 15 comparators, which compare an unknown input voltage to the reference ladder, to achieve a 4-bit result. The MS (most significant) flash ADC converts an unknown analog input voltage (V_{IN}) to provide the 4 MS data bits. An internal DAC, driven by the 4 MS data bits, then recreates an analog approximation of the input voltage. The DAC output voltage is subtracted from the analog input, and the difference is converted by the LS (least significant) ADC to provide the 4 LS data bits. The MS flash ADC also has one additional comparator to detect overrange on the analog input.

OPERATING SEQUENCE

The AD7821 has two operating modes. The RD mode allows a conversion to be started and data to be read with a single, extended, READ operation (i.e., $\overline{CS}$ and $\overline{RD}$ are taken low). The conversion process is timed out by internal one-shots. The WR-RD mode uses $\overline{WR}$ to start a conversion and $\overline{RD}$ to read the data and allows the conversion timing to be externally controlled. The operating sequence for the WR-RD mode is shown in Figure 3.

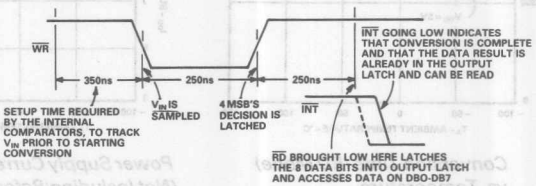


Figure 3. Operating Sequence (WR-RD Mode)

A conversion is initiated and the analog input signal (V_{IN}) sampled on the falling edge of $\overline{WR}$ (falling edge of $\overline{RD}$, RD mode). A setup time (tp, delay time between conversions) of 350 ns is required prior to this falling edge. See Digital Interface section for more details. When $\overline{WR}$ is low, the internal MS (most significant) ADC compares the sampled analog input with the reference ladder to provide the 4 MS data bits. A minimum of 250 ns is required for this comparison. On the rising edge of $\overline{WR}$, the MS data result is latched internally and the LS (least significant) conversion begins, to yield the 4 LS data bits. $\overline{INT}$ goes low typically 380 ns after the rising edge of $\overline{WR}$. This indicates the LS conversion is complete and that both the LS and MS data results are latched into the output buffer. $\overline{RD}$ going low then enables the output data. If a faster conversion time is required, the $\overline{RD}$ line can be brought low 250 ns after $\overline{WR}$ goes high. This latches both the LS and MS data bits and outputs the conversion result on DB0–DB7.

REFERENCE AND INPUT

The V_{REF} (−) and V_{REF} (+) reference inputs on the AD7821 are fully differential and define the zero and full-scale input range of the ADC. The transfer characteristic of the part is defined by the integer value of the following expression:

$$Data\ (LSBs) = 256\left[\frac{V_{IN} - V_{REF}(-)}{V_{REF}(+) - V_{REF}(-)}\right] + 0.5$$

As a result, the analog input (V_{IN}) of the device can easily be set up to provide both unipolar and bipolar operation. The data output code for unipolar and bipolar operation is Natural Binary and Offset Binary, respectively.

The span of the analog input voltage can easily be varied. By reducing the reference span, V_{REF} (+)−V_{REF} (−), to less than 5 V the sensitivity of the converter can be increased (i.e., if V_{REF} = 2 V then 1 LSB = 7.8 mV). The reference flexibility also allows the input span for unipolar operation to be offset from zero (V_{REF} (−)>GND). Additionally, the input/reference arrangement facilitates ratiometric operation.

Figures 4 and 5 show some configurations which are possible. For minimum noise a 47 μF capacitor in parallel with a 0.1 μF capacitor should be connected between the reference inputs and GND.

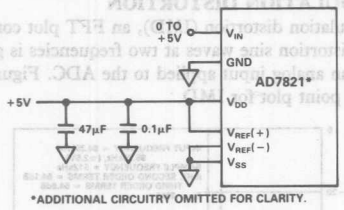


Figure 4. Power Supply as Reference. Unipolar Operation (0 to +5V)

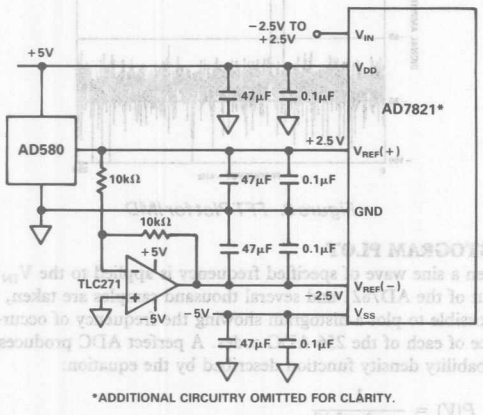


Figure 5. External Reference. Bipolar Operation (−2.5V to +2.5V)

INPUT CURRENT

The analog input of the AD7821 behaves somewhat differently to conventional A/D converters. This is due to the ADC's sampled-data comparators, which take varying amounts of input current depending on the cycle of the converter.

The equivalent input circuit of the AD7821 is shown in Figure 6. When a conversion ends (e.g., falling edge of $\overline{INT}$, WR-RD mode, $t_{RD}>t_{INTL}$) all the input switches are closed and V_{IN} is connected to the comparators of the internal LS and MS ADCs. Therefore, V_{IN} is connected to 31 one - pF input capacitors simultaneously.

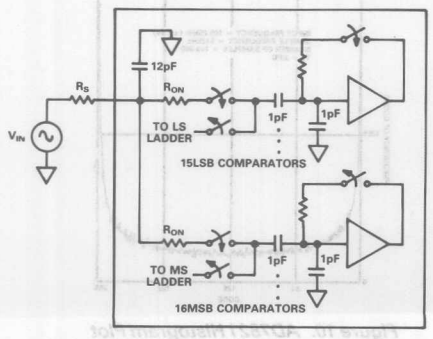


Figure 6. AD7821 Equivalent Input Circuit

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 2 kΩ to 5 kΩ). In addition, about 12 pF of input stray capacitance must be charged.

The analog input can be modeled as an equivalent RC network as shown in Figure 7. As R_S (source impedance) increases, the input capacitance takes longer to charge.

The comparators track the analog input between conversions. A minimum delay time (t_P) of 350 ns is required between conversions to allow for voltage source settling and comparator tracking time. This allows input time constants of 50 ns without settling time problems. Typical total input capacitance values of 55 pF allow R_S to be 0.9 kΩ without lengthening t_P to give V_{IN} more time to settle.

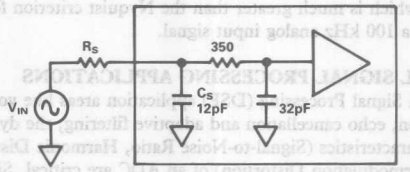


Figure 7. RC Network Model

INPUT TRANSIENTS

Transients on the analog input signal caused by charging current flowing into V_{IN} will not normally degrade the ADC's performance. In effect, the AD7821 does not "look" at the input when these transients occur. The comparators' inputs track V_{IN} and are not sampled until the falling edge of $\overline{WR}$ (WR-RD Mode) or $\overline{RD}$ (RD Mode), so at least 350 ns (t_P) is provided to charge the ADC's input capacitance. It is, therefore, not necessary to filter out these transients with an external capacitor at the V_{IN} terminal.

INHERENT TRACK-AND-HOLD

A major benefit of the AD7821's input structure is its ability to measure a variety of high-speed signals without the help of an external track-and-hold. Any ADC which does not have a built-in track-and-hold, regardless of its speed, requires the analog input to remain stable to at least 1/2 LSB for the duration of the conversion to maintain full accuracy. This requires the use of a track-and-hold whenever the input is a high-speed signal. The AD7821's sampled-data comparators, by nature of their input switching, inherently accomplish this track-and-hold function. Although the conversion time for the AD7821 is 660 ns (WR-RD mode, $t_{WR}+t_{RD}+t_{ACC1}$), the time for which V_{IN} must be stable to 1/2 LSB is much smaller. The AD7821 tracks V_{IN} between conversions only, and its value on the falling edge of $\overline{WR}$ or $\overline{RD}$ in the WR-RD or RD modes, respectively, is the measured value.

SINUSOIDAL INPUTS

The bandwidth of the built-in track-and-hold is 100 kHz max (150 kHz typ, 5 V p-p). This is limited by the analog bandwidth of the comparators and timing skew between the comparator switches. This means that the analog input frequency can be up to 100 kHz without the aid of an external track-and-hold. The Nyquist criterion requires that the sampling rate be at least twice the input frequency (i.e., ≥2×100 kHz). This requires an ideal antialiasing filter with an infinite roll-off. To ease the

problem of antialiasing filter design, the sampling rate is usually set much greater than the Nyquist criterion. The maximum sampling rate (f_{max}) for the AD7821 in the WR-RD mode, ($t_{RD} < t_{INTL}$) can be calculated as follows:

$$f_{max} = \frac{1}{t_{WR} + t_{RD} + t_{RI} + t_P}$$

$$f_{max} = \frac{1}{0.25E-6 + 0.25E-6 + 0.15E-6 + 0.35E-6}$$

t_{WR} = *Write Pulse Width*

t_{RD} = *Delay Time between* $\overline{WR}$ *and* $\overline{RD}$ *Pulses*

t_{RI} = $\overline{RD}$ *to* $\overline{INT}$ *Delay*

t_P = *Delay Time between Conversions*

This permits a maximum sampling rate for the AD7821 of 1 MHz, which is much greater than the Nyquist criterion for sampling a 100 kHz analog input signal.

DIGITAL SIGNAL PROCESSING APPLICATIONS

In Digital Signal Processing (DSP) application areas like voice recognition, echo cancellation and adaptive filtering, the dynamic characteristics (Signal-to-Noise Ratio, Harmonic Distortion, Intermodulation Distortion) of an ADC are critical. Since the AD7821 is a very fast ADC with a built-in track-and-hold function, it is specified dynamically as well as with standard dc specifications (Total Unadjusted Error, etc.).

SIGNAL-TO-NOISE RATIO AND DISTORTION

The dynamic performance of the AD7821 is evaluated by applying a very low distortion sine-wave signal to the analog input (V_{IN}) which is then sampled at a 512 kHz sampling rate. A Fast Fourier Transform (FFT) plot is then generated from which Signal-to-Noise Ratio (SNR) and harmonic distortion data are obtained.

Figure 8 shows a 2048 point FFT plot of the AD7821 with an input signal of 100.25 kHz. The SNR is 49.1 dB. It should be noted that the harmonics are taken into account when calculating the SNR. The theoretical relationship between SNR and resolution (N) is expressed by the following equation:

$$SNR = (6.02N + 1.76)\ dB \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

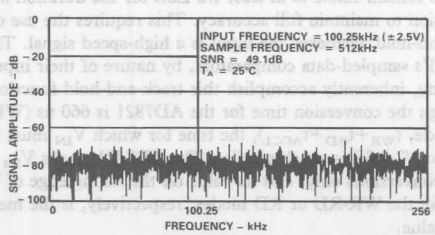


Figure 8. AD7821 FFT Plot

EFFECTIVE NUMBER OF BITS

By working backwards from Equation (1) it is possible to get a measure of ADC performance expressed in effective number of bits (N). A plot of the effective number of bits versus input frequency is given in the Typical Performance Characteristics section. The effective number of bits typically falls between 7.7 and 7.9, corresponding to SNR figures of 48.1 and 49.7 dB.

INTERMODULATION DISTORTION

For intermodulation distortion (IMD), an FFT plot consisting of very low distortion sine waves at two frequencies is generated by sampling an analog input applied to the ADC. Figure 9 shows a 2048 point plot for IMD.

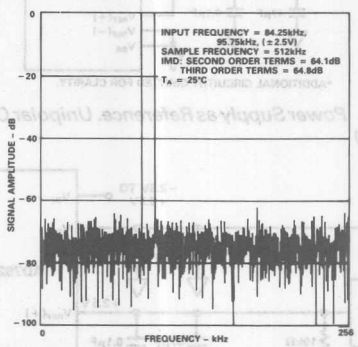


Figure 9. FFT Plot for IMD

HISTOGRAM PLOT

When a sine wave of specified frequency is applied to the V_{IN} input of the AD7821 and several thousand samples are taken, it is possible to plot a histogram showing the frequency of occurrence of each of the 256 ADC codes. A perfect ADC produces a probability density function described by the equation:

$$P(V) = \frac{1}{\pi(A^2 - V^2)^{1/2}}$$

where A is the peak amplitude of the sine wave and P(V) is the probability of occurrence at a voltage V.

If a particular step is wider than the ideal 1 LSB width, then the code associated with that step will accumulate more counts than for the code for an ideal step. Likewise, a step narrower than the ideal width will have fewer counts. Missing codes are easily seen because a missing code means zero counts for a particular code. The absence of large spikes in the plot indicates small differential nonlinearity.

Figure 10 shows a histogram plot for the AD7821, which corresponds very well with the ideal shape. The plot indicates very small differential nonlinearity and no missing codes for an input frequency of 100.25 kHz.

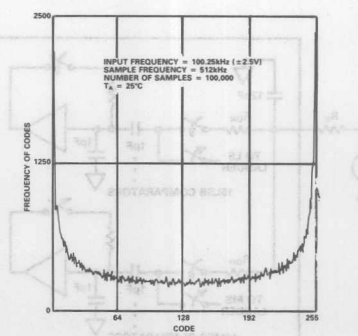


Figure 10. AD7821 Histogram Plot

In digital signal processing applications, where the AD7821 is used to sample ac signals, it is essential that the signal sampling occurs at exactly equal intervals. This minimizes errors due to sampling uncertainty or jitter. A precise timer or clock source, to start the ADC conversion process, is the best method of generating equidistant sampling intervals.

The two modes of operation given in the data sheet are suitable for DSP applications because the sampling instant of the AD7821 is well defined. V_{IN} is sampled on the falling edge of $\overline{WR}$ or $\overline{RD}$ in the WR-RD or RD modes, respectively.

DIGITAL INTERFACE

The AD7821 has two basic interface modes which are determined by the status of the MODE pin. When this pin is low, the converter is in the RD mode; with this pin high, the AD7821 is set up for the WR-RD mode.

The RD mode is designed for microprocessors that can be driven into a WAIT state. A READ operation (i.e., $\overline{CS}$ and $\overline{RD}$ are taken low) starts a conversion and data is read when the conversion is complete. The WR-RD mode does not require microprocessor WAIT states. A WRITE operation (i.e., $\overline{CS}$ and $\overline{WR}$ are taken low) initiates a conversion, and a READ operation reads the result when the conversion is complete.

RD Mode (MODE = 0)

The timing diagram for the RD mode is shown in Figure 11. This mode is intended for use with microprocessors which have a WAIT state facility, whereby a READ instruction cycle can be extended to accommodate slow memory devices. A conversion is started by taking $\overline{CS}$ and $\overline{RD}$ low (READ operation). Both $\overline{CS}$ and $\overline{RD}$ are then kept low until output data appears.

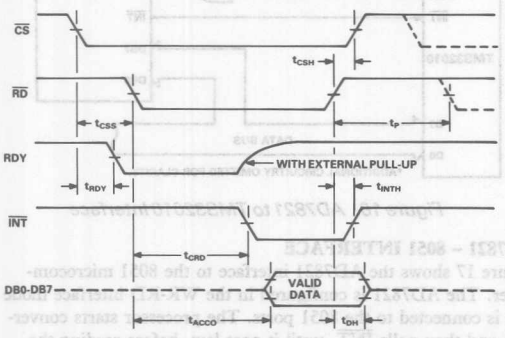


Figure 11. RD Mode

In this mode, Pin 6 of the AD7821 is configured as a status output, RDY. This RDY output can be used to drive the processor READY or WAIT input. It is an open drain output (no internal pull-up device) which goes low after the falling edge of $\overline{CS}$ and goes high impedance at the end of conversion. An $\overline{INT}$ line is also provided which goes low when a conversion is complete. $\overline{INT}$ returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

WR-RD Mode (MODE = 1)

In the WR-RD mode, Pin 6 is configured as a WRITE ($\overline{WR}$) input for the AD7821. With $\overline{CS}$ low, conversion is initiated on the falling edge of $\overline{WR}$. Two options exist for reading data from the converter.

In the first of these options the processor waits for the $\overline{INT}$ status line to go low before reading the data (see Figure 12a).

$\overline{INT}$ typically goes low within 380 ns after the rising edge of $\overline{WR}$. It indicates that conversion is complete and that the data result is in the output latch. With $\overline{CS}$ low, the data outputs (DB0–DB7) are activated when $\overline{RD}$ goes low. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$.

The alternative option can be used to shorten the conversion time. This is a method for bypassing the internal time-out circuit. The $\overline{INT}$ line is ignored and $\overline{RD}$ can be brought low

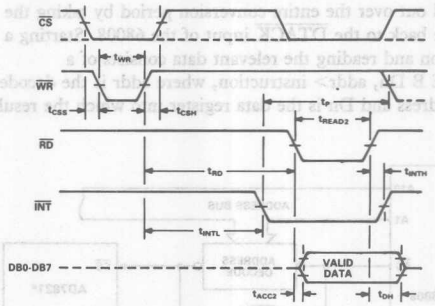


Figure 12a. WR-RD Mode ($t_{RD} > t_{INTL}$)

250 ns after the rising edge of $\overline{WR}$. In this case $\overline{RD}$ going low transfers the data result into the output latch and activates the data output (DB0–DB7). $\overline{INT}$ is driven low on the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. The timing for this interface is shown in Figure 12b.

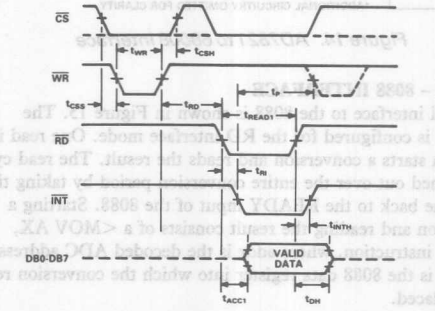


Figure 12b. WR-RD Mode ($t_{RD} < t_{INTL}$)

The AD7821 can also be used in stand-alone operation in the WR-RD mode. $\overline{CS}$ and $\overline{RD}$ are tied low, and a conversion is initiated by bringing $\overline{WR}$ low. Output data is valid 530 ns ($t_{INTL} + t_{ID}$) after the rising edge of $\overline{WR}$. The timing diagram for this mode is shown in Figure 13.

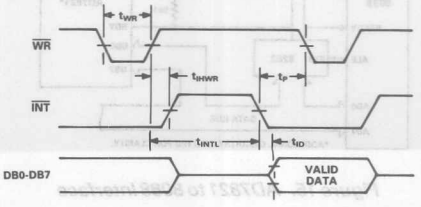


Figure 13. WR-RD Mode Stand-Alone Operation, $\overline{CS} = \overline{RD} = 0$

MICROPROCESSOR INTERFACING

The AD7821 is designed for easy interfacing to microprocessors as a memory mapped peripheral or an I/O device. This reduces to a minimum the amount of external logic required for interfacing.

AD7821 – 68008 INTERFACE

Figure 14 shows an AD7821 interface to the 68008 microprocessor. The ADC is configured for the RD interface mode. This means that one read instruction starts a conversion and reads the result when the conversion is completed. The read cycle is stretched out over the entire conversion period by taking the $\overline{INT}$ line back to the $\overline{DTACK}$ input of the 68008. Starting a conversion and reading the relevant data consists of a <MOVE B Dn, addr> instruction, where addr is the decoded ADC address and Dn is the data register into which the result is placed.

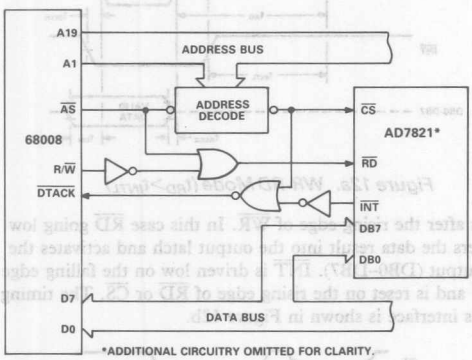


Figure 14. AD7821 to 68008 Interface

AD7821 – 8088 INTERFACE

A typical interface to the 8088 is shown in Figure 15. The AD7821 is configured for the RD interface mode. One read instruction starts a conversion and reads the result. The read cycle is stretched out over the entire conversion period by taking the RDY line back to the READY input of the 8088. Starting a conversion and reading the result consists of a <MOV AX, (addr)> instruction, where addr is the decoded ADC address and AX is the 8088 data register into which the conversion result is placed.

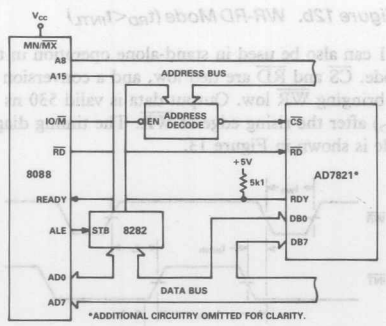


Figure 15. AD7821 to 8088 Interface

AD7821 – TMS32010 INTERFACE

A typical interface to the TMS32010 is shown in Figure 16. The AD7821 is mapped at a port address and the interface is designed for the maximum TMS32010 clock frequency of 20 MHz. In this case, the AD7821 is configured in the WR-RD interface mode. This means that a write instruction starts a conversion and a read instruction reads the result when the conversion is completed. A precise timer or clock source is used to start a conversion in applications requiring equidistant sampling intervals. The scheme used, whereby the AD7821 generates an interrupt to the TMS32010, is limited in that it does not allow the AD7821 to be sampled at its maximum rate. This is because the time between samples has to be long enough to allow the TMS32010 to service its interrupt and read data from the AD7821. Constant interruption of the TMS32010 by the AD7821, every time the ADC completes a conversion, is not a very efficient use of the processor time. To overcome these problems, some buffer memory or FIFO could be placed between the AD7821 and the TMS32010. The $\overline{INT}$ line of the AD7821 could be used to trigger a pulse which drives its $\overline{CS}$ and $\overline{RD}$ lines and places the AD7821 data into a FIFO or buffer memory. The microprocessor can then read a batch of data from the FIFO or buffer memory at some convenient time. Reading data from the AD7821, after an $\overline{INT}$ has been received, consists of <IN A, PA> instruction (PA is the decoded ADC address).

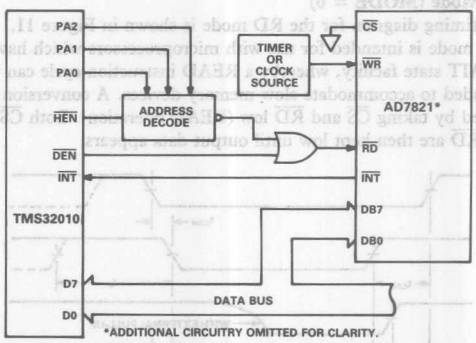


Figure 16. AD7821 to TMS32010 Interface

AD7821 – 8051 INTERFACE

Figure 17 shows the AD7821 interface to the 8051 microcomputer. The AD7821 is configured in the WR-RD interface mode and is connected to the 8051 ports. The processor starts conversion and then polls $\overline{INT}$, until it goes low, before reading the conversion result. Data is read from the AD7821 by using the <MOV A, 90H> instruction (90H is the address for Port 1).

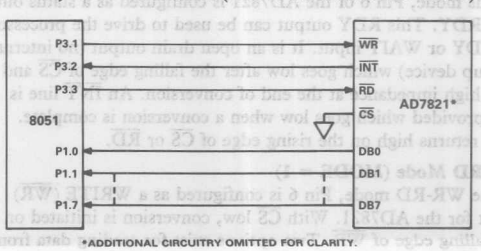


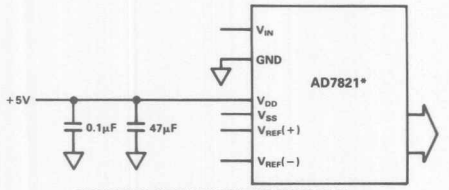
Figure 17. AD7821 to 8051 Interface

APPLYING THE AD7821

The AD7821 is specified for a unipolar input range of 0 to +5 V and a bipolar input range of −2.5 V to +2.5 V. The $V_{REF}(-)$ and $V_{REF}(+)$ voltages required for these input ranges are outlined below. See the Typical Performance Characteristics section for operation with unspecified input voltage ranges.

UNIPOLAR OPERATION

Figure 18 gives the configuration and reference voltages required for 0 to +5 V operation. The nominal transfer characteristic for this input range is shown in Figure 19. The output code is Natural Binary with 1 LSB = (5/256) V = 19.5 mV.



*ADDITIONAL CIRCUITRY OMITTED FOR CLARITY.

$V_{REF}(+)$	$V_{REF}(-)$	V_{SS}	V_{IN}	RANGE
+5V	GND	GND	UNIPOLAR	0 to +5V
+2.5V	−2.5V	−5V	BIPOLAR	−2.5V to +2.5V

Figure 18. AD7821 Unipolar/Bipolar Operation

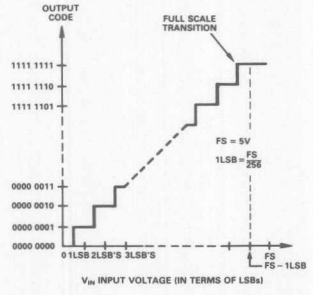


Figure 19. Nominal Transfer Characteristic for Unipolar (0 to +5 V) Operation

BIPOLAR OPERATION

Figure 18 gives the configuration and reference voltages required for −2.5 V to +2.5 V operation. The nominal transfer characteristic for this input range is shown in Figure 20. The output code is Offset Binary with 1 LSB = ([+2.5 − (−2.5)]/256)V = 19.5 mV.

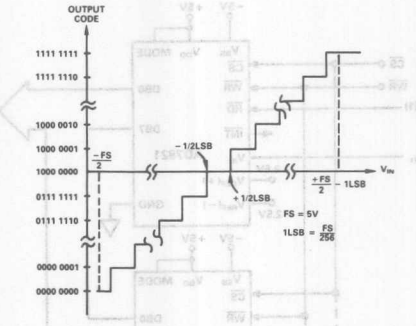


Figure 20. Nominal Transfer Characteristic for Bipolar (−2.5 V to +2.5 V) Operation

16-CHANNEL TELECOM A/D CONVERTER

The fast sampling rate (1 MHz) and bipolar operation of the AD7821 makes it useful in Telecom applications for sampling a number of input channels using a multiplexer. Figure 21 shows a circuit for such an application.

The maximum signal frequency required for acceptable quality in Telecom applications is 3 kHz. The circuit given in Figure 21 permits each of the 16-input channels to be sampled at a rate of 16 kHz maximum. The sampling rate takes account of such multiplexer parameters as t_{ON}, settling time etc. The circuit also eases the problem of the antialiasing filter design by sampling at a rate much greater than that required by the Nyquist criterion.

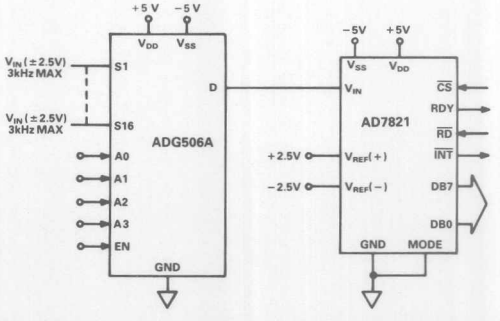


Figure 21. 16-Channel Telecom A/D Converter System

SIMULTANEOUS SAMPLING A/D CONVERTERS

The AD7821's inherent track-and-hold and well-defined sampling instant makes it useful, in such applications as sonar, where a number of input channels are required to be sampled simultaneously. Figure 22 shows a circuit for such an application.

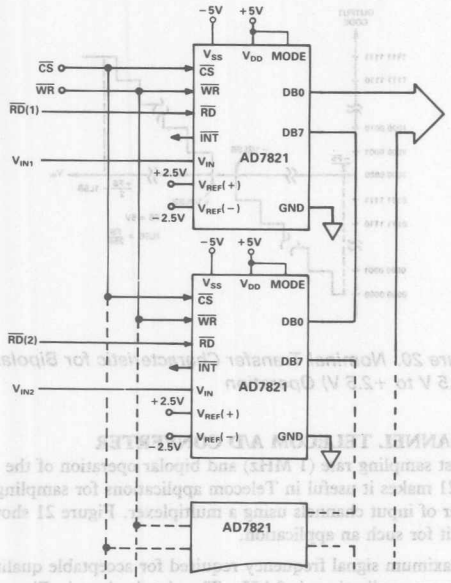


Figure 22. Simultaneous Sampling A/D Converters

The actual sampling instant, which is the instant at which V_{IN} is measured, occurs approximately 50 ns after the falling edge of $\overline{WR}$ or $\overline{RD}$ in the WR-RD or RD modes, respectively, due to internal logic delays. However, the internal logic delay and, therefore, the sampling instant can vary from device to device, but is typically within ±5 ns. This means that a maximum common input sine wave of ±2.5 V at 32 kHz, applied to any number of AD7821s in the circuit of Figure 22, will yield a maximum difference between the converter outputs of typically ±1/4 LSB.

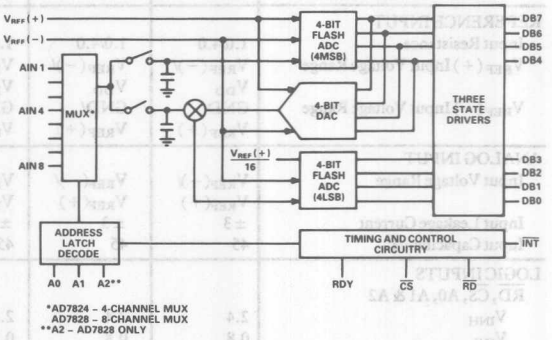
LC²MOS High Speed 4- & 8-Channel 8-Bit ADCs

AD7824/AD7828

FEATURES

4- or 8-Analog Input Channels
Built-In Track/Hold Function
10kHz Signal Handling on Each Channel
Fast Microprocessor Interface
Single +5V Supply
Low Power: 50mW
Fast Conversion Rate, 2.5μs/Channel
Tight Error Specification: 1/2LSB

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7824 and AD7828 are high-speed, multichannel, 8-bit ADCs with a choice of 4 (AD7824) or 8 (AD7828) multiplexed analog inputs. A half-flash conversion technique gives a fast conversion rate of 2.5μs per channel and the parts have a built-in track/hold function capable of digitizing full-scale signals of 10kHz (157mV/μs slew rate) on all channels. The AD7824 and AD7828 operate from a single +5V supply and have an analog input range of 0 to +5V, using an external +5V reference.

Microprocessor interfacing of the parts is simple, using standard Chip Select ($\overline{CS}$) and Read ($\overline{RD}$) signals to intitiate the conversion and read the data from the three-state data outputs. The half-flash conversion technique means that there is no need to generate a clock signal for the ADC. The AD7824 and AD7828 can be interfaced easily to most popular microprocessors.

The AD7824 and AD7828 are fabricated in an advanced, all ion-implanted, Linear-Compatible CMOS process (LC²MOS) and have low power dissipation of 40mW (typ). The AD7824 is available in a 0.3″ wide, 24-pin "skinny" DIP, while the AD7828 is available in a 0.6″ wide, 28-pin DIP and in 28-terminal surface mount packages.

PRODUCT HIGHLIGHTS

1. 4- or 8-channel input multiplexer gives cost-effective space-saving multichannel ADC system.
2. Fast conversion rate of 2.5μs/channel features a per channel sampling frequency of 100kHz for the AD7824 or 50kHz for the AD7828.
3. Built-in track-hold function allows handling of 4- or 8-channels up to 10kHz bandwidth (157mV/μs slew rate).
4. Tight total unadjusted error spec and channel-to-channel matching eliminate the need for user trims.
5. Single +5V supply simplifies system power requirements.
6. Fast, easy-to-use digital interface allows connection to most popular microprocessors with minimal external components. No clock signal is required for the ADC.

AD7824/AD7828—SPECIFICATIONS

(V_{DD} = +5V, $V_{REF}(+)$ = +5V, $V_{REF}(-)$ = GND = 0V unless otherwise stated. All specifications T_{min} to T_{max} unless otherwise specified. Specifications apply for Mode 0.)

Parameter	K Version[1]	L Version	B, T Versions	C, U Versions	Units	Conditions/Comments
ACCURACY						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[2]	±1	±1/2	±1	±1/2	LSB max	
Minimum Resolution for which No Missing Codes are guaranteed	8	8	8	8	Bits	
Channel to Channel Mismatch	±1/4	±1/4	±1/4	±1/4	LSB max	
REFERENCE INPUT						
Input Resistance	1.0/4.0	1.0/4.0	1.0/4.0	1.0/4.0	kΩ min/kΩ max	
$V_{REF}(+)$ Input Voltage Range	$V_{REF}(-)$/ V_{DD}	$V_{REF}(-)$/ V_{DD}	$V_{REF}(-)$/ V_{DD}	$V_{REF}(-)$/ V_{DD}	V min/V max	
$V_{REF}(-)$ Input Voltage Range	GND/ $V_{REF}(+)$	GND/ $V_{REF}(+)$	GND/ $V_{REF}(+)$	GND/ $V_{REF}(+)$	V min/V max	
ANALOG INPUT						
Input Voltage Range	$V_{REF}(-)$/ $V_{REF}(+)$	$V_{REF}(-)$/ $V_{REF}(+)$	$V_{REF}(-)$/ $V_{REF}(+)$	$V_{REF}(-)$/ $V_{REF}(+)$	V min/V max	
Input Leakage Current	±3	±3	±3	±3	μA max	Analog Input Any Channel
Input Capacitance[3]	45	45	45	45	pF typ	0 to +5V
LOGIC INPUTS						
$\overline{RD}$, $\overline{CS}$, A0, A1 & A2						
V_{INH}	2.4	2.4	2.4	2.4	V min	
V_{INL}	0.8	0.8	0.8	0.8	V max	
I_{INH}	1	1	1	1	μA max	
I_{INL}	−1	−1	−1	−1	μA max	
Input Capacitance[3]	8	8	8	8	pF max	Typically 5pF
LOGIC OUTPUTS						
DB0-DB7 & $\overline{INT}$						
V_{OH}	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 360μA
V_{OL}	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
I_{OUT} (DB0-DB7)	±3	±3	±3	±3	μA max	Floating State Leakage
Output Capacitance[3]	8	8	8	8	pF max	Typically 5pF
RDY						
V_{OL}[4]	0.4	0.4	0.4	0.4	V max	I_{SINK} = 2.6mA
I_{OUT}	±3	±3	±3	±3	μA max	Floating State Leakage
Output Capacitance	8	8	8	8	pF max	Typically 5pF
SLEW RATE, TRACKING[3]	0.7	0.7	0.7	0.7	V/μs typ	
	0.157	0.157	0.157	0.157	V/μs max	
POWER SUPPLY						
V_{DD}	5	5	5	5	Volts	±5% for Specified Performance
I_{DD}[5]	16	16	20	20	mA max	$\overline{CS}$ = $\overline{RD}$ = 2.4V
Power Dissipation	50	50	50	50	mW typ	
	80	80	100	100	mW max	
Power Supply Sensitivity	±1/4	±1/4	±1/4	±1/4	LSB max	±1/16LSB typ V_{DD} = 5V ±5%

NOTES

[1]Temperature Ranges are as follows:
K, L Versions; 0 to +70°C
B, C Versions; −25°C to +85°C
T, U Versions; −55°C to +125°C

[2]Total Unadjusted Error includes offset, full-scale and linearity errors.

[3]Sample tested at 25°C by Product Assurance to ensure compliance.

[4]RDY is an open drain output.

[5]See Typical Performance Characteristics.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5V; V_{REF} (+) = +5V; V_{REF} (−) = GND = 0V unless otherwise stated)

Parameter	Limit at 25°C (All Grades)	Limit at T_{min}, T_{max} (K, L, B, C Grades)	Limit at T_{min}, T_{max} (T, U Grades)	Units	Conditions/Comments
t_{CSS}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_{CSH}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_{AS}	0	0	0	ns min	Multiplexer Address Setup Time
t_{AH}	30	35	40	ns min	Multiplexer Address Hold Time
t_{RDY}[2]	40	60	60	ns max	$\overline{CS}$ to RDY Delay. Pull-Up Resistor 5kΩ.
t_{CRD}	2.0	2.4	2.8	μs max	Conversion Time, Mode 0
t_{ACC1}[3]	85	110	120	ns max	Data Access Time after $\overline{RD}$
t_{ACC2}[3]	50	60	70	ns max	Data Access Time after $\overline{INT}$, Mode 0
t_{INTH}[2]	40	65	70	ns typ	$\overline{RD}$ to $\overline{INT}$ Delay
	75	100	100	ns max	
t_{DH}[4]	60	70	70	ns max	Data Hold Time
t_P	500	500	600	ns min	Delay Time between Conversions
t_{RD}	60	80	80	ns min	Read Pulse Width, Mode 1
	600	500	400	ns max	

NOTES
[1]Sample tested at 25°C to ensure compliance. All input control signals are specified with tr = tf = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]C_L = 50pF.
[3]Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[4]Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.

Test Circuits

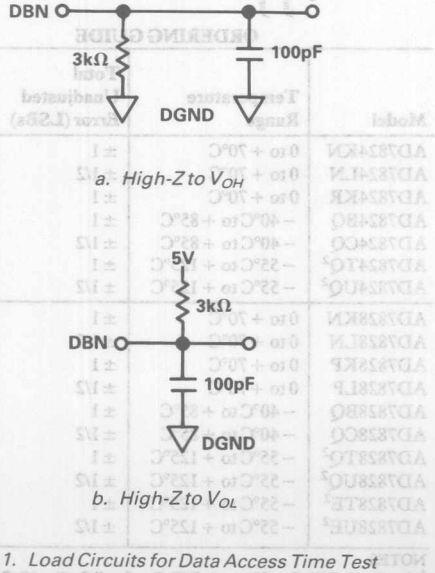


Figure 1. Load Circuits for Data Access Time Test

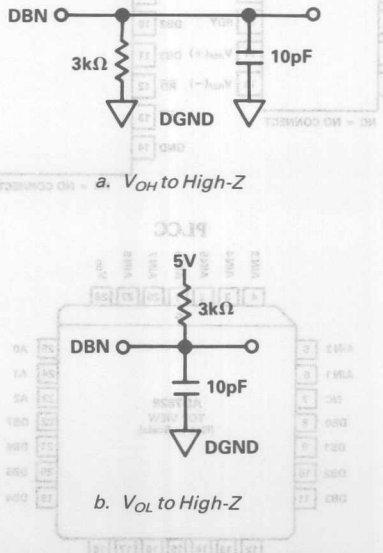


Figure 2. Load Circuits for Data Hold Time Test

V_{DD}	0V, +7V
Digital Input Voltage to GND ($\overline{RD}$, $\overline{CS}$, A0, A1 & A2)	−0.3V, V_{DD} +0.3V
Digital Output Voltage to GND (DB0, DB7, RDY & $\overline{INT}$)	−0.3V, V_{DD} +0.3V
V_{REF} (+) to GND	V_{REF} (−), V_{DD} +0.3V
V_{REF} (−) to GND	0V, V_{REF} (+)
Analog Input (Any Channel)	−0.3V, V_{DD} +0.3V
Operating Temperature Range	
Commercial (K, L Versions)	0 to +70°C
Extended (T, U Versions)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C
Power Dissipation (Any Package) to +75°C	450mW
Derates above +75°C by	6mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

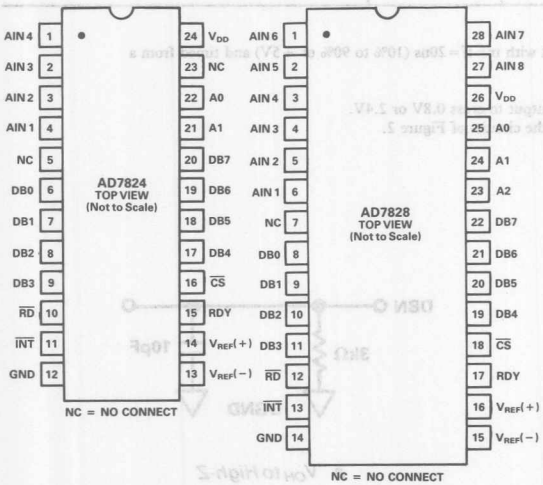
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

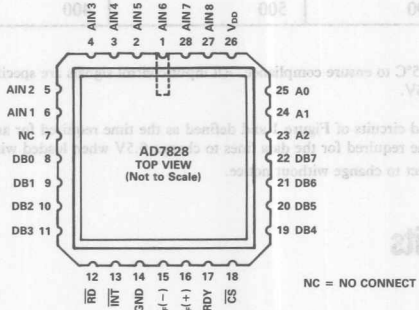


PIN CONFIGURATIONS

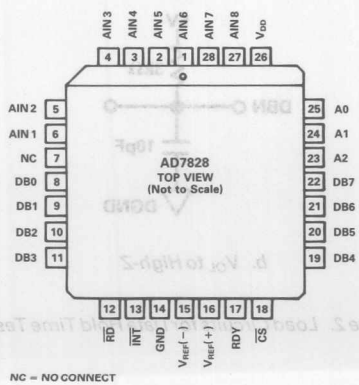
DIP



LCCC



PLCC



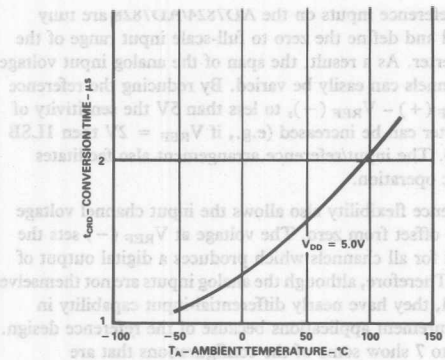
ORDERING GUIDE

Model	Temperature Range	Total Unadjusted Error (LSBs)	Package Option[1]
AD7824KN	0 to +70°C	±1	N-24
AD7824LN	0 to +70°C	±1/2	N-24
AD7824KR	0 to +70°C	±1	R-24
AD7824BQ	−40°C to +85°C	±1	Q-24
AD7824CQ	−40°C to +85°C	±1/2	Q-24
AD7824TQ[2]	−55°C to +125°C	±1	Q-24
AD7824UQ[2]	−55°C to +125°C	±1/2	Q-24
AD7828KN	0 to +70°C	±1	N-28
AD7828LN	0 to +70°C	±1/2	N-28
AD7828KP	0 to +70°C	±1	P-28A
AD7828LP	0 to +70°C	±1/2	P-28A
AD7828BQ	−40°C to +85°C	±1	Q-28
AD7828CQ	−40°C to +85°C	±1/2	Q-28
AD7828TQ[2]	−55°C to +125°C	±1	Q-28
AD7828UQ[2]	−55°C to +125°C	±1/2	Q-28
AD7828TE[2]	−55°C to +125°C	±1	E-28A
AD7828UE[2]	−55°C to +125°C	±1/2	E-28A

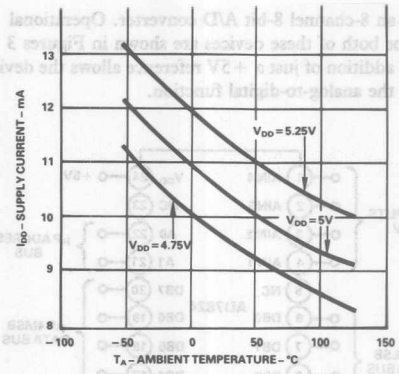
NOTES

[1]N = Plastic DIP; Q = Hermetic DIP, R = Small Outline IC; P = Plastic Leaded Chip Carrier; E = Leadless Ceramic Chip Carrier. For outline information see Package Information section.

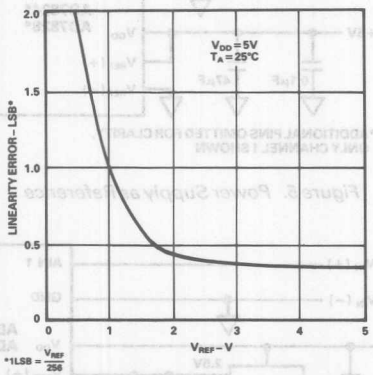
[2]Available to /883B processing only. Contact our local sales office for military data sheet. For U.S. Standard Military Drawing (SMD) see DESC Drawing #5692-88764.



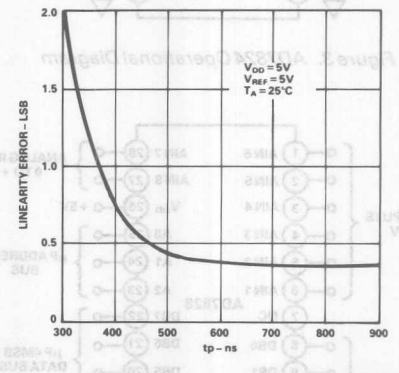
Conversion Time vs. Temperature



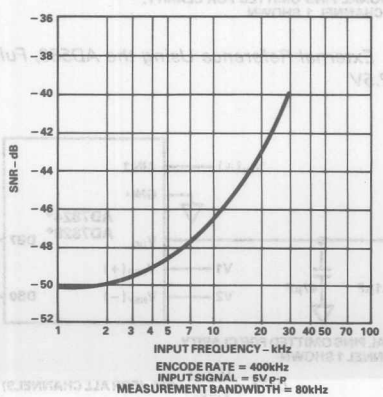
Power Supply Current vs. Temperature (not including reference ladder)



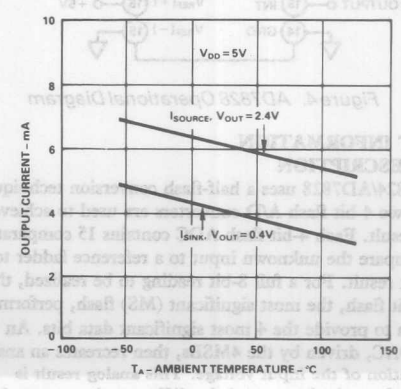
Accuracy vs. V_{REF}
[$V_{REF} = V_{REF}(+) - V_{REF}(-)$]



Accuracy vs. tp



Signal-Noise Ratio vs. Input Frequency



Output Current vs. Temperature

OPERATIONAL DIAGRAM

The AD7824 is a 4-channel 8-bit A/D converter and the AD7828 is an 8-channel 8-bit A/D converter. Operational diagrams for both of these devices are shown in Figures 3 and 4. The addition of just a +5V reference allows the devices to perform the analog-to-digital function.

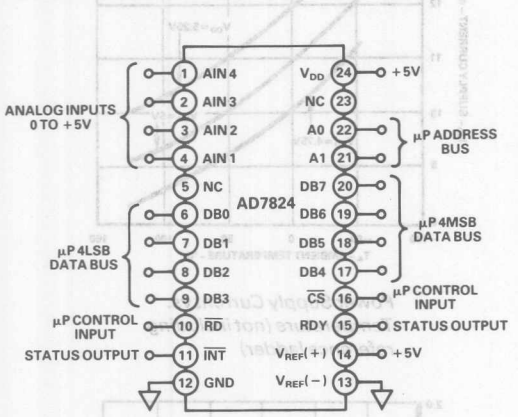


Figure 3. AD7824 Operational Diagram

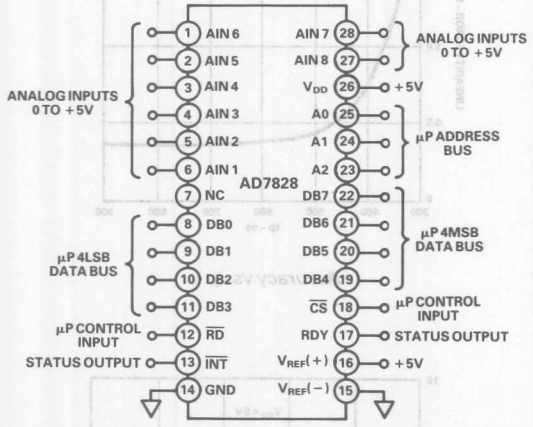


Figure 4. AD7828 Operational Diagram

CIRCUIT INFORMATION

BASIC DESCRIPTION

The AD7824/AD7828 uses a half-flash conversion technique whereby two 4-bit flash A/D converters are used to achieve an 8-bit result. Each 4-bit flash ADC contains 15 comparators which compare the unknown input to a reference ladder to get a 4-bit result. For a full 8-bit reading to be realized, the upper 4-bit flash, the most significant (MS) flash, performs a conversion to provide the 4 most significant data bits. An internal DAC, driven by the 4MSBs, then recreates an analog approximation of the input voltage. This analog result is subtracted from the input, and the difference is converted by the lower flash ADC, the least significant (LS) flash, to provide the 4 least significant bits of the output data.

APPLYING THE AD7824/AD7828

REFERENCE AND INPUT

The two reference inputs on the AD7824/AD7828 are fully differential and define the zero to full-scale input range of the A/D converter. As a result, the span of the analog input voltage for all channels can easily be varied. By reducing the reference span, $V_{REF}(+) - V_{REF}(-)$, to less than 5V the sensitivity of the converter can be increased (e.g., if V_{REF} = 2V then 1LSB = 7.8mV). The input/reference arrangement also facilitates ratiometric operation.

This reference flexibility also allows the input channel voltage span to be offset from zero. The voltage at $V_{REF}(-)$ sets the input level for all channels which produces a digital output of all zeroes. Therefore, although the analog inputs are not themselves differential, they have nearly differential-input capability in most measurement applications because of the reference design. Figures 5 to 7 show some of the configurations that are possible.

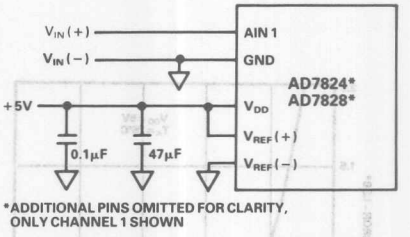


Figure 5. Power Supply as Reference

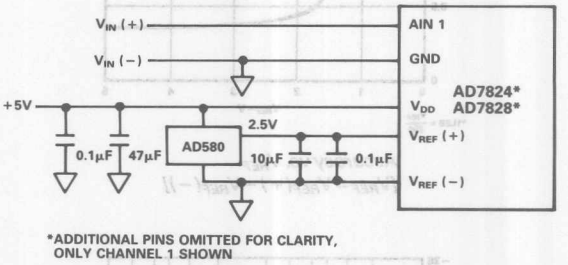


Figure 6. External Reference Using the AD580, Full-Scale Input is 2.5V

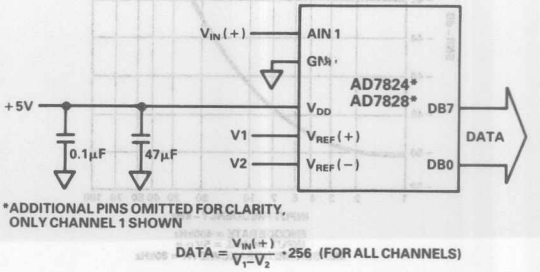


Figure 7. Input Not Referenced to GND

INPUT CURRENT

Due to the novel conversion techniques employed by the AD7824/AD7828, the analog input behaves somewhat differently than in conventional devices. The ADC's sampled-data comparators take varying amounts of input current depending on which cycle the conversion is in.

The equivalent input circuit of the AD7824/AD7828 is shown in Figure 8. When a conversion starts ($\overline{CS}$ and $\overline{RD}$ going low), all input switches close, and the selected input channel is connected to the most significant and least significant comparators. Therefore, the analog input is connected to thirty-one 1pF input capacitors at the same time.

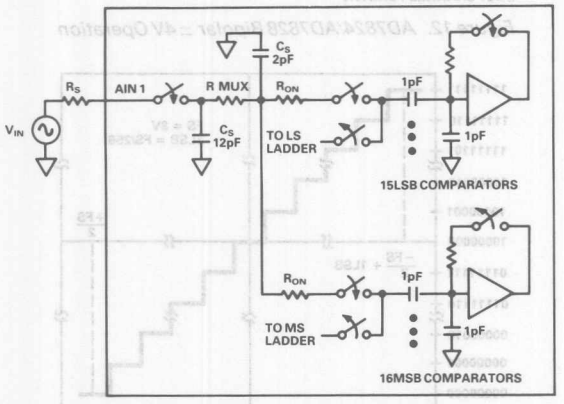


Figure 8. AD7824/AD7828 Equivalent Input Circuit

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 3k to 6k). In addition, about 14pF of input stray capacitance must be charged. The analog input for any channel can be modelled as an RC network as shown in Figure 9. As R_S increases, it takes longer for the input capacitance to charge.

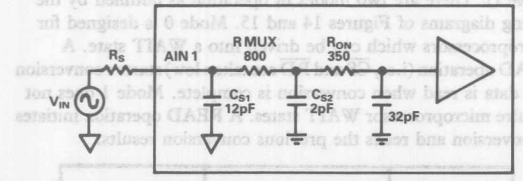


Figure 9. RC Network Model

The time for which the input comparators track the analog input is approximately 1μs at the start of conversion. Because of input transients on the analog inputs, it is recommended that a source impedence of not greater than 100 ohms be connected to the analog inputs. The output impedence of an op-amp is equal to the open loop output impedence divided by the loop gain at the frequency of interest. It is important that the amplifier driving the AD7824/AD7828 analog inputs have sufficient loop gain at the input signal frequency as to make the output impedance low.

Suitable op-amps for driving the AD7824/AD7828 are the AD544 or AD644.

INHERENT SAMPLE-HOLD

A major benefit of the AD7824's and AD7828's analog input structure is its ability to measure a variety of high-speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain stable to at least 1/2LSB throughout the conversion process if rated accuracy is to be maintained. Consequently, for many high-speed signals, this signal must be externally sampled and held stationary during the conversion. The AD7824/AD7828 input comparators, by nature of their input switching inherently accomplish this sample-and-hold function. Although the conversion time for AD7824/ AD7828 is 2μs, the time for which any selected analog input must be 1/2LSB stable is much smaller. The AD7824/AD7828 tracks the selected input channel for approximately 1μs after conversion start. The value of the analog input at that instant (1μs from conversion start) is the measured value. This value is then used in the least significant flash to generate the lower 4-bits of data.

SINUSOIDAL INPUTS

The AD7824/AD7828 can measure input signals with slew rates as high as 157mV/μs to the rated specifications. This means that the analog input frequency can be up to 10kHz without the aid of an external sample and hold. Furthermore, the AD7828 can measure eight 10kHz signals without a sample and hold. The Nyquist criterion requires that the sampling rate be twice the input frequency (i.e., 2 × 10kHz). This requires an ideal anti-aliasing filter with an infinite roll-off. To ease the problem of anti-aliasing filter design, the sampling rate is usually much greater than the Nyquist criterion. The maximum sampling rate (F_{max}) for the AD7824/AD7828 can be calculated as follows:

$$F_{max} = \frac{1}{t_{CRD} + t_p}$$

$$F_{max} = \frac{1}{2E-6+0.5E-6} = 400kHz$$

t_{CRD} = AD7824/AD7828 Conversion Time
t_P = Minimum Delay Between Conversion

This permits a maximum sampling rate of 50kHz for each of the 8 channels when using the AD7828 and 100kHz for each of the 4 channels when using the AD7824.

UNIPOLAR OPERATION

The analog input range for any channel of the AD7824/AD7828 is 0 to 5V as shown in the unipolar operational diagram of Figure 10. Figure 11 shows the designed code transitions which occur midway between successive integer LSB values (i.e., 1/2LSB, 3/2LSB, 5/2LSB, FS-3/2LSBs). The output code is Natural Binary with 1LSB = FS/256 = (5/256)V = 19.5mV.

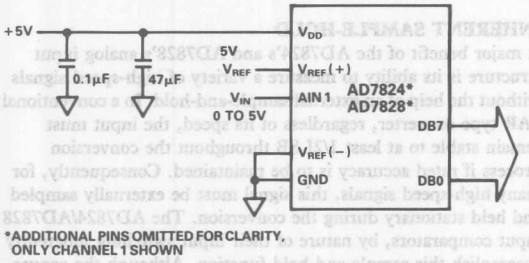


Figure 10. AD7824/AD7828 Unipolar 0 to 5V Operation

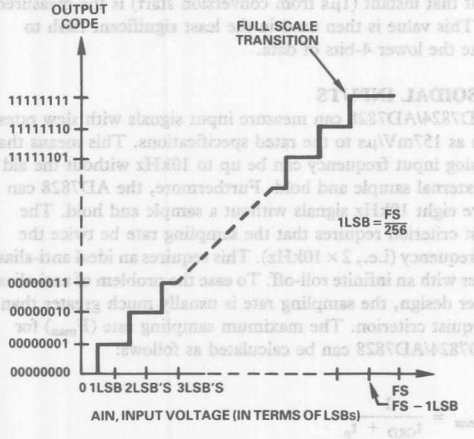


Figure 11. Ideal Input/Output Transfer Characteristic for Unipolar 0 to +5V Operation

BIPOLAR OPERATION

The circuit of Figure 12 is designed for bipolar operation. An AD544 op-amp conditions the signal input (V_{IN}) so that only positive voltages appear at AIN 1. The closed loop transfer function of the op-amp for the resistor values shown is given below:

$$AIN\ 1 = (2.5 - 0.625\ V_{IN})\ Volts$$

The analog input range is ±4V and the LSB size is 31.25mV. The output code is complementary offset binary. The ideal input/output characteristic is shown in Figure 13.

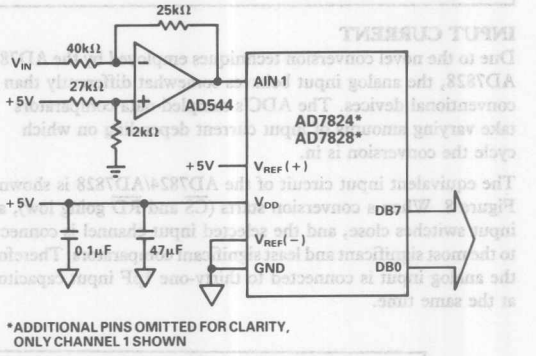


Figure 12. AD7824/AD7828 Bipolar ±4V Operation

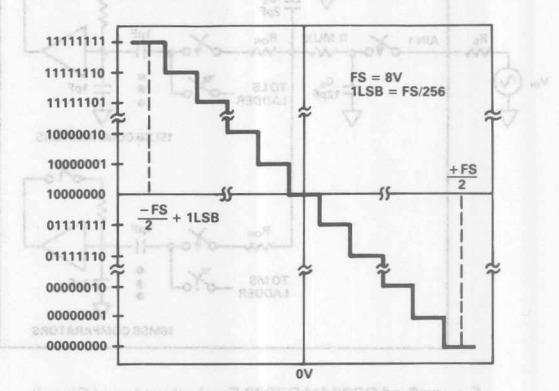


Figure 13. Ideal Input/Output Transfer Characteristic for ±4V Operation

TIMING AND CONTROL

The AD7824/AD7828 has two digital inputs for timing and control. These are Chip Select ($\overline{CS}$) and Read ($\overline{RD}$). A READ operation brings $\overline{CS}$ and $\overline{RD}$ low which starts a conversion on the channel selected by the multiplexer address inputs (see Table I). There are two modes of operation as outlined by the timing diagrams of Figures 14 and 15. Mode 0 is designed for microprocessors which can be driven into a WAIT state. A READ operation (i.e., $\overline{CS}$ and $\overline{RD}$ are taken low) starts a conversion and data is read when conversion is complete. Mode 1 does not require microprocessor WAIT states. A READ operation initiates a conversion and reads the previous conversion results.

AD7824		AD7828			CHANNEL
A1	A0	A2	A1	A0	
0	0	0	0	0	AIN 1
0	1	0	0	1	AIN 2
1	0	0	1	0	AIN 3
1	1	0	1	1	AIN 4
		1	0	0	AIN 5
		1	0	1	AIN 6
		1	1	0	AIN 7
		1	1	1	AIN 8

Table I. Truth Table for Input Channel Selection

MODE 0

Figure 14 shows the timing diagram for Mode 0 operation. This mode can only be used for microprocessors which have a WAIT state facility, whereby a READ instruction cycle can be extended to accommodate slow memory devices. A READ operation brings $\overline{CS}$ and $\overline{RD}$ low which starts a conversion. The analog multiplexer address inputs must remain valid while $\overline{CS}$ and $\overline{RD}$ are low. The data bus (DB7-DB0) remains in the three-state condition until conversion is complete. There are two converter status outputs on the AD7824/AD7828, interrupt ($\overline{INT}$) and ready (RDY) which can be used to drive the microprocessor READY/WAIT input. The RDY is an open drain output (no internal pull-up device) which goes low on the falling edge of $\overline{CS}$ and goes high impedance at the end of conversion, when the 8-bit conversion result appears on the data outputs. If the RDY status is not required, then the external pull-up resistor can be omitted and the RDY output tied to GND. The $\overline{INT}$ goes low when conversion is complete and returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

MODE 1

Mode 1 operation is designed for applications where the microprocessor is not forced into a WAIT state. A READ operation takes $\overline{CS}$ and $\overline{RD}$ low which triggers a conversion (see Figure 15). The multiplexer address inputs are latched on the rising edge of $\overline{RD}$. Data from the previous conversion is read from the three-state data outputs (DB7-DB0). This data may be disregarded if not required. Note, the RDY output (open drain output) does not provide any status information in this mode and must be connected to GND. At the end of conversion $\overline{INT}$ goes low. A second READ operation is required to access the new conversion result. This READ operation latches a new address into the multiplexer inputs and starts another conversion. $\overline{INT}$ returns high at the end of the second READ operation, when $\overline{CS}$ or $\overline{RD}$ returns high. A delay of 2.5μs must be allowed between READ operations.

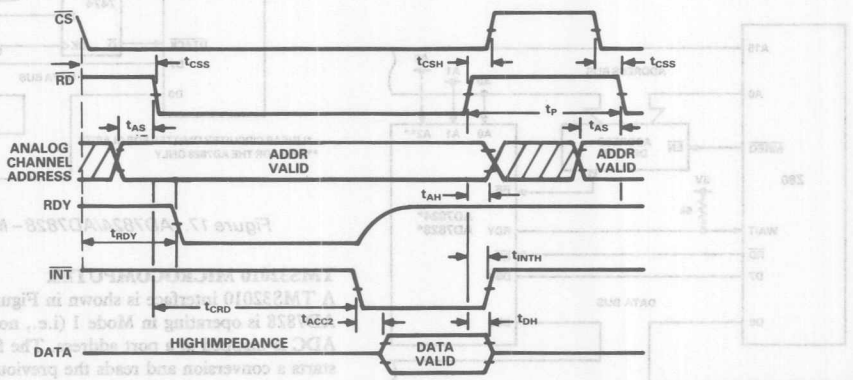


Figure 14. Mode 0 Timing Diagram

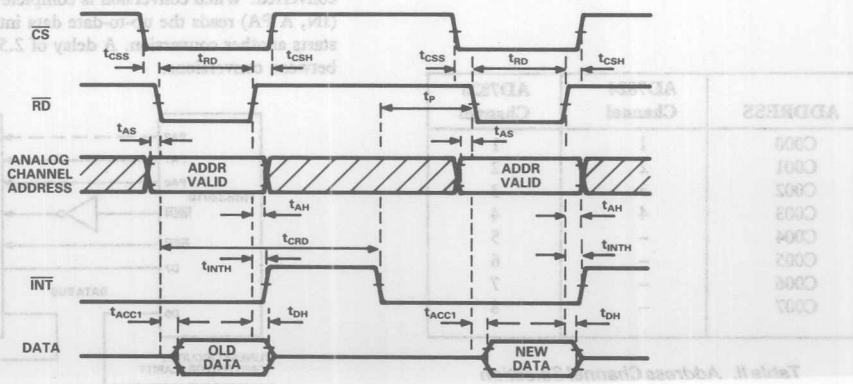


Figure 15. Mode 1 Timing Diagram

AD7824/AD7828 read operations are controlled by CS, RD and the channel address inputs. These signals are common to all memory peripheral devices.

Z80 MICROPROCESSOR

Figure 16 shows a typical AD7824/AD7828 – Z80 interface. The AD7824/AD7828 is operating in Mode 0. Assume the ADC is assigned a memory block starting at address C000. The following LOAD instruction to any of the addresses listed in Table II will start a conversion of the selected channel and read the conversion result.

LD B, (C000)

At the beginning of the instruction cycle when the ADC address is selected, RDY asserts the WAIT input, so that the Z80 is forced into a WAIT state. At the end of conversion RDY returns high and the conversion result is placed in the B register of the microprocessor.

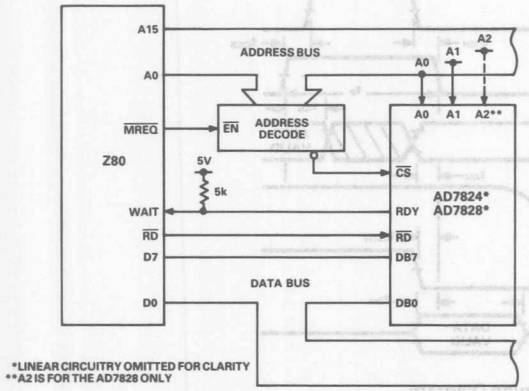


Figure 16. AD7824/AD7828 – Z80 Interface

ADDRESS	AD7824 Channel	AD7828 Channel
C000	1	1
C001	2	2
C002	3	3
C003	4	4
C004	–	5
C005	–	6
C006	–	7
C007	–	8

Table II. Address Channel Selection

block starting at address C000. A MOVE instruction to any of the addresses in Table II starts a conversion and reads the conversion result.

MOVE·B $C000,D0

Once conversion has begun, the MC68000 inserts WAIT states, until INT goes low asserting DTACK at the end of conversion. The microprocessor then places the conversion results in the D0 register.

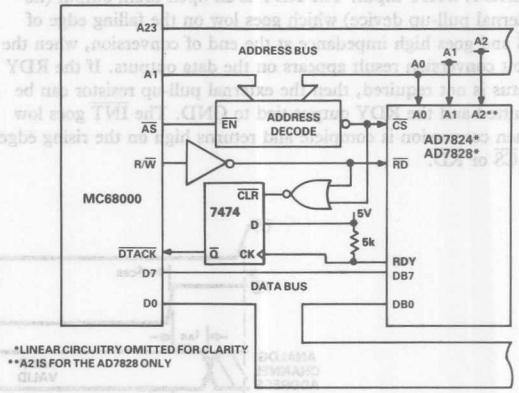


Figure 17. AD7824/AD7828 – MC68000 Interface

TMS32010 MICROCOMPUTER

A TMS32010 interface is shown in Figure 18. The AD7824/AD7828 is operating in Mode 1 (i.e., no μP WAIT states). The ADC is mapped at a port address. The following I/O instruction starts a conversion and reads the previous conversion result into the accumulator.

IN, A PA (PA = PORT ADDRESS)

The port address (000 to 111) selects the analog channel to be converted. When conversion is complete a second I/O instruction (IN, A PA) reads the up-to-date data into the accumulator and starts another conversion. A delay of 2.5μs must be allowed between conversions.

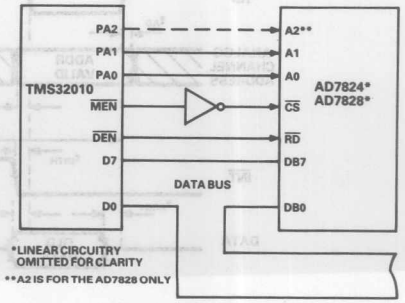


Figure 18. AD7824/AD7828 – TMS32010 Interface

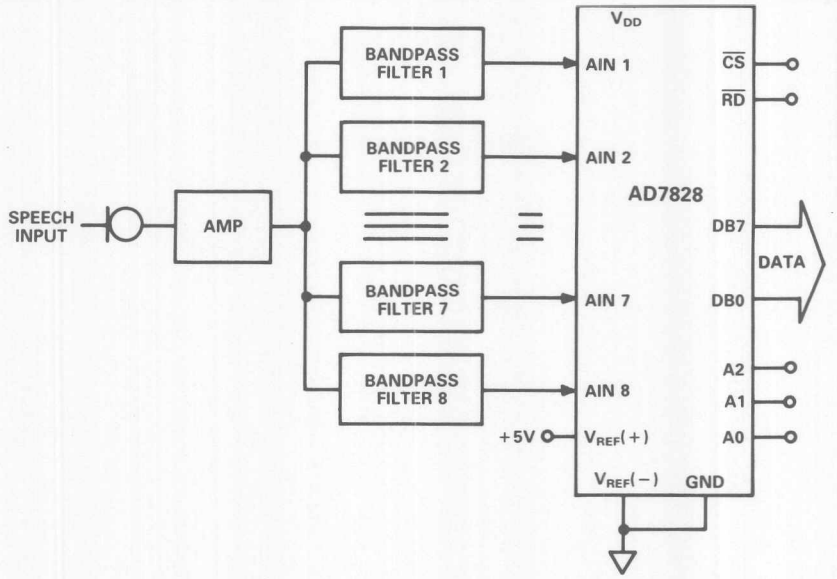


Figure 19. Speech Analysis Using Real-Time Filtering

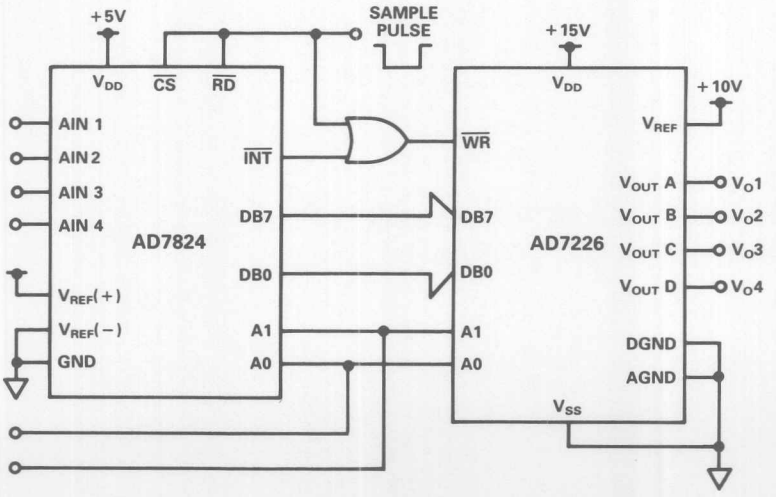
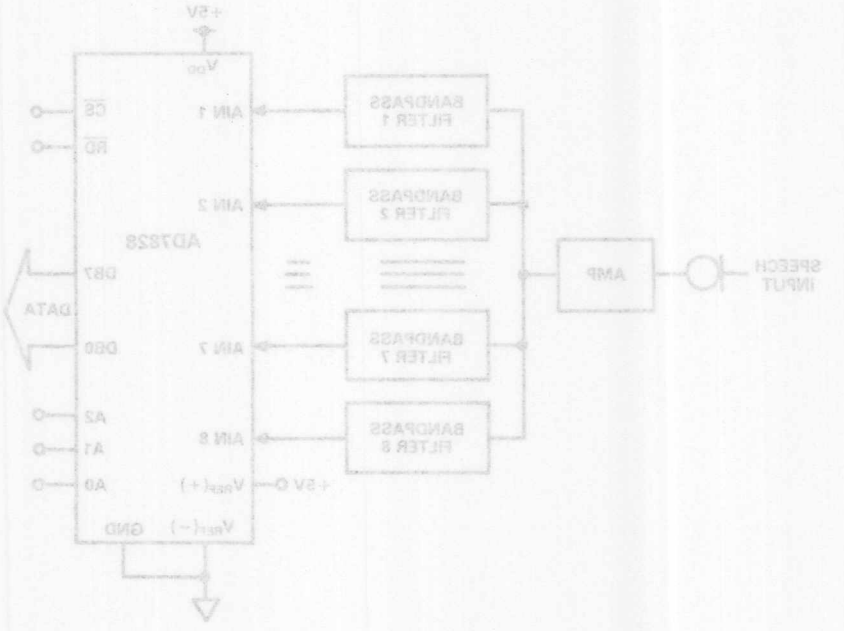
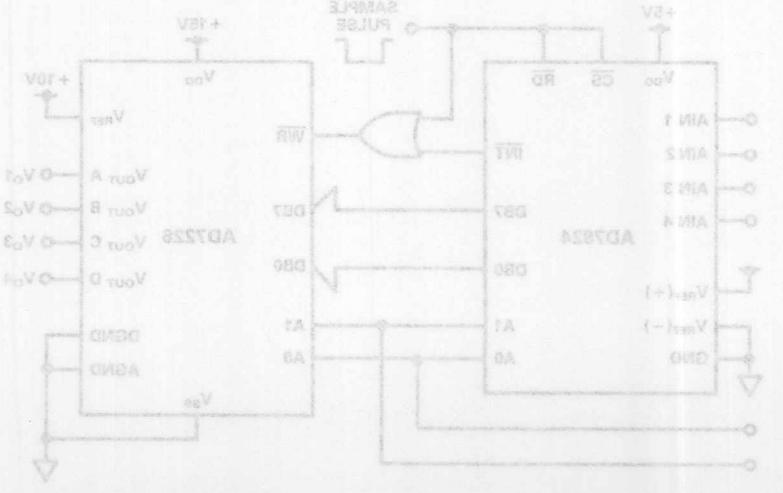


Figure 20. 4-Channel Fast Infinite Sample-and-Hold


+5V
ADT82B
BANDPASS FILTER 1
BANDPASS FILTER 2
BANDPASS FILTER 7
BANDPASS FILTER 8
AMP
SPEECH INPUT
DATA
GND


+10V
+5V
SAMPLE PULSE
ADT82B
ADT82A
GND

ANALOG DEVICES

LC²MOS Complete, 12-Bit, 100 kHz, Sampling ADCs

AD7870/AD7875/AD7876

FEATURES

Complete Monolithic 12-Bit ADC with:
- 2 μs Track/Hold Amplifier
- 8 μs A/D Converter
- On-Chip Reference
- Laser-Trimmed Clock
- Parallel, Byte and Serial Digital Interface

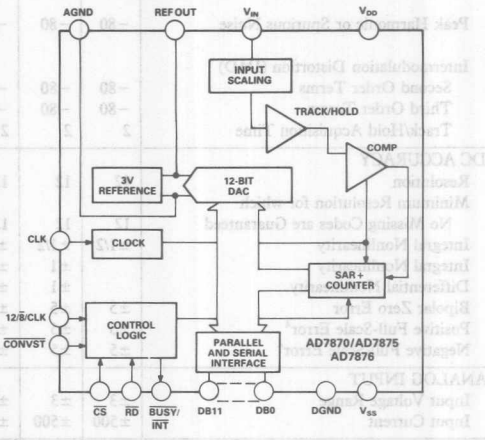
72 dB SNR at 10 kHz Input Frequency (AD7870, AD7875)

57 ns Data Access Time

Low Power −60 mW typ

Variety of Input Ranges:
- ±3 V for AD7870
- 0 to +5 V for AD7875
- ±10 V for AD7876

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7870/AD7875/AD7876 is a fast, complete, 12-bit A/D converter. It consists of a track/hold amplifier, 8 μs successive-approximation ADC, 3 V buried Zener reference and versatile interface logic. The ADC features a self-contained internal clock which is laser trimmed to guarantee accurate control of conversion time. No external clock timing components are required; the on-chip clock may be overridden by an external clock if required.

The parts offer a choice of three data output formats: a single, parallel, 12-bit word; two 8-bit bytes, or serial data. Fast bus access times and standard control inputs ensure easy interfacing to modern microprocessors and digital signal processors.

All parts operate from ±5 V power supplies. The AD7870 and AD7876 accept input signal ranges of ±3 V and ±10 V, respectively, while the AD7875 accepts a unipolar 0 to +5 V input range. The parts can convert full power signals up to 50 kHz.

The AD7870/AD7875/AD7876 feature dc accuracy specifications such as linearity, full-scale and offset error. In addition, the AD7870 and AD7875 are fully specified for dynamic performance parameters including distortion and signal-to-noise ratio.

The parts are fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low-power CMOS logic. The parts are available in a 24-pin, 0.3 inch-wide, plastic or hermetic dual-in-line package (DIP). The AD7870 and AD7875 are available in a 28-pin plastic leaded chip carrier (PLCC), while the AD7876 is available and in a 24-pin small outline (SOIC) package.

PRODUCT HIGHLIGHTS

1. Complete 12-Bit ADC on a Chip.
   The AD7870/AD7875/AD7876 provides all the functions necessary for analog-to-digital conversion and combines a 12-bit ADC with internal clock, track/hold amplifier and reference on a single chip.
2. Dynamic Specifications for DSP Users.
   The AD7870 and AD7875 are fully specified and tested for ac parameters, including signal-to-noise ratio, harmonic distortion and intermodulation distortion.
3. Fast Microprocessor Interface.
   Data access times of 57 ns make the parts compatible with modern 8- and 16-bit microprocessors and digital signal processors. Key digital timing parameters are tested and guaranteed over the full operating temperature range.

Parameter	J, A[1]	K, B[1]	L, C[1]	S[1]	T[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]							
Signal to Noise Ratio[3] (SNR)							
@ +25°C	70	70	72	69	69	dB min	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz
T_{min} to T_{max}	70	70	71	69	69	dB min	Typically 71.5 dB for 0 < V_{IN} < 50 kHz
Total Harmonic Distortion (THD)	−80	−80	−80	−78	−78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz Typically −86 dB for 0 < V_{IN} < 50 kHz
Peak Harmonic or Spurious Noise	−80	−80	−80	−78	−78	dB max	V_{IN} = 10 kHz, f_{SAMPLE} = 100 kHz Typically −86 dB for 0 < V_{IN} < 50 kHz
Intermodulation Distortion (IMD)							
Second Order Terms	−80	−80	−80	−78	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	−80	−80	−80	−78	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Track/Hold Acquisition Time	2	2	2	2	2	µs max	
DC ACCURACY							
Resolution	12	12	12	12	12	Bits	
Minimum Resolution for which							
No Missing Codes are Guaranteed	12	12	12	12	12	Bits	
Integral Nonlinearity	±1/2	±1/2	±1/4	±1/2	±1/2	LSB typ	
Integral Nonlinearity		±1	±1/2		±1	LSB max	
Differential Nonlinearity		±1	±1		±1	LSB max	
Bipolar Zero Error	±5	±5	±5	±5	±5	LSB max	
Positive Full-Scale Error[4]	±5	±5	±5	±5	±5	LSB max	
Negative Full-Scale Error[4]	±5	±5	±5	±5	±5	LSB max	
ANALOG INPUT							
Input Voltage Range	±3	±3	±3	±3	±3	Volts	
Input Current	±500	±500	±500	±500	±500	µA max	
REFERENCE OUTPUT							
REF OUT @ +25°C	2.99	2.99	2.99	2.99	2.99	V min	
	3.01	3.01	3.01	3.01	3.01	V max	
REF OUT Tempco	±60	±60	±35	±60	±35	ppm/°C max	
Reference Load Sensitivity (ΔREF OUT/ΔI)	±1	±1	±1	±1	±1	mV max	Reference Load Current Change (0-500 µA) Reference Load Should Not Be Changed During Conversion.
LOGIC INPUTS							
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	2.4	V min	V_{DD} = 5 V ±5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	0.8	V max	V_{DD} = 5 V ±5%
Input Current, I_{IN}	±10	±10	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Current (12/$\overline{8}$/CLK Input Only)	±10	±10	±10	±10	±10	µA max	V_{IN} = V_{SS} to V_{DD}
Input Capacitance, C_{IN}[5]	10	10	10	10	10	pF max	
LOGIC OUTPUTS							
Output High Voltage, V_{OH}	4.0	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 40 µA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0							
Floating-State Leakage Current	±10	±10	±10	±10	±10	µA max	
Floating-State Output Capacitance[5]	15	15	15	15	15	pF max	
CONVERSION TIME							
External Clock (f_{CLK} = 2.5 MHz)	8	8	8	8	8	µs max	
Internal Clock	7/9	7/9	7/9	7/9	7/9	µs min/µs max	
POWER REQUIREMENTS							
V_{DD}	+5	+5	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	13	13	13	13	13	mA max	Typically 8 mA
I_{SS}	6	6	6	6	6	mA max	Typically 4 mA
Power Dissipation	95	95	95	95	95	mW max	Typically 60 mW

NOTES

[1]Temperature ranges are as follows: J, K, L Versions; 0 to +70°C: A, B, C Versions; −25°C to +85°C: S, T Versions; −55°C to +125°C.

[2]V_{IN} (pk–pk) = ±3 V.

[3]SNR calculation includes distortion and noise components.

[4]Measured with respect to internal reference and includes bipolar offset error.

[5]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

Parameter	AD7875/AD7876 K, B[1]	L, C[1]	T[1]	Units	Test Conditions/Comments
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for Which No Missing Codes Are Guaranteed	12	12	12	Bits	
Integral Nonlinearity @ +25°C	±1	±1/2	±1	LSB max	
T_{min} to T_{max} (AD7875 Only)	±1	±1	±1	LSB max	
T_{min} to T_{max} (AD7876 Only)	±1	±1/2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	LSB max	
Unipolar Offset Error (AD7875 Only)	±5	±5	±5	LSB max	
Bipolar Zero Error (AD7876 Only)	±6	±2	±6	LSB max	
Full-Scale Error at +25°C[2]	±8	±8	±8	LSB max	Typical full-scale error is ±1 LSB
Full-Scale TC[2]	±60	±35	±60	ppm/°C max	Typical TC is ±20 ppm/°C
Track/Hold Acquisition Time	2	2	2	μs max	
DYNAMIC PERFORMANCE[3] (AD7875 ONLY)					
Signal-to-Noise Ratio[4] (SNR)					
@ +25°C	70	72	69	dB min	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz
T_{min} to T_{max}	70	71	69	dB min	Typically 71.5 dB for 0 <V_{IN}< 50 kHz
Total Harmonic Distortion (THD)	−80	−80	−78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz Typically −86 dB for 0 <V_{IN}< 50 kHz
Peak Harmonic or Spurious Noise	−80	−80	−78	dB max	V_{IN} = 10 kHz, f_{SAMPLE} = 100 kHz Typically −86 dB for 0 <V_{IN}< 50 kHz
Intermodulation Distortion (IMD)					
Second Order Terms	−80	−80	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	−80	−80	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
ANALOG INPUT					
AD7875 Input Voltage Range	0 to +5	0 to +5	0 to +5	Volts	
AD7875 Input Current	500	500	500	μA max	
AD7876 Input Voltage Range	±10	±10	±10	Volts	
AD7876 Input Current	±600	±600	±600	μA max	
REFERENCE OUTPUT					
REF OUT @ +25°C	2.99	2.99	2.99	V min	
	3.01	3.01	3.01	V max	
REF OUT Tempco	±60	±35	±60	ppm/°C max	Typical Tempco is ±20 ppm/°C
Reference Load Sensitivity (ΔREF OUT/ΔI)	−1	−1	−1	mV max	Reference Load Current Change (0–500 μA) Reference Load Should Not Be Changed During Conversion.
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V±5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V±5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Current (12/$\overline{8}$/CLK Input Only)	±10	±10	±10	μA max	V_{IN} = V_{SS} to V_{DD}
Input Capacitance, C_{IN}[5]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 40 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0					
Floating-State Leakage Current	10	10	10	μA max	
Floating-State Output Capacitance[5]	15	15	15	pF max	
CONVERSION TIME					
External Clock (f_{CLK} = 2.5 MHz)	8	8	8	μs max	
Internal Clock	7/9	7/9	7/9	μs min/μs max	
POWER REQUIREMENTS	As per AD7870				

NOTES

[1]Temperature ranges are as follows: AD7875: K, L Versions, 0 to +70°C; B, C Versions, −40°C to +85°C; T Version, −55°C to +125°C. AD7876: B, C Versions, −40°C to +85°C; T Version, −55°C to +125°C.

[2]Includes internal reference error and is calculated after unipolar offset error (AD7875) or bipolar zero error (AD7876) has been adjusted out. Full-scale error refers to both positive and negative full-scale error for the AD7876.

[3]Dynamic performance parameters are not tested on the AD7876 but these are typically the same as for the AD7875.

[4]SNR calculation includes distortion and noise components.

[5]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

AD7870/AD7875/AD7876

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V. See Figures 9, 10, 11 and 12.)

Parameter	Limit at T_{min}, T_{max} (J, K, L, A, B, C Versions)	Limit at T_{min}, T_{max} (S, T Versions)	Units	Conditions/Comments
t_1	50	50	ns min	$\overline{CONVST}$ Pulse Width
t_2	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time (Mode 1)
t_3	**60**	**75**	ns min	$\overline{RD}$ Pulse Width
t_4	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time (Mode 1)
t_5	70	70	ns max	$\overline{RD}$ to $\overline{INT}$ Delay
t_6[3]	**57**	**70**	ns max	Data Access Time after $\overline{RD}$
t_7[4]	5	5	ns min	Bus Relinquish Time after $\overline{RD}$
	50	**50**	ns max	
t_8	0	0	ns min	HBEN to $\overline{RD}$ Setup Time
t_9	0	0	ns min	HBEN to $\overline{RD}$ Hold Time
t_{10}	100	100	ns min	$\overline{SSTRB}$ to SCLK Falling Edge Setup Time
t_{11}[5]	370	370	ns min	SCLK Cycle Time
t_{12}[6]	135	150	ns max	SCLK to Valid Data Delay. C_L=35 pF
t_{13}	20	20	ns min	SCLK Rising Edge to $\overline{SSTRB}$
	100	100	ns max	
t_{14}	10	10	ns min	Bus Relinquish Time after SCLK
	100	100	ns max	
t_{15}	60	60	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time (Mode 2)
t_{16}	120	120	ns max	$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay
t_{17}	200	200	ns min	Data Setup Time Prior to $\overline{BUSY}$
t_{18}	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time (Mode 2)
t_{19}	0	0	ns min	HBEN to $\overline{CS}$ Setup Time
t_{20}	0	0	ns min	HBEN to $\overline{CS}$ Hold Time

NOTES

[1]Timing specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]Serial timing is measured with a 4.7 kΩ pull-up resistor on SDATA and $\overline{SSTRB}$ and a 2 kΩ pull-up on SCLK. The capacitance on all three outputs is 35 pF.

[3]t_6 is measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[4]t_7 is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.

[5]SCLK mark/space ratio (measured from a voltage level of 1.6 V) is 40/60 to 60/40.

[6]SDATA will drive higher capacitive loads but this will add to t_{12} since it increases the external RC time constant (4.7 kΩ||C_L) and hence the time to reach 2.4 V. Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{SS} to AGND . . . . . +0.3 V to −7 V
AGND to DGND . . . . . −0.3 V to V_{DD} +0.3 V
V_{IN} to AGND . . . . . −15 V to +15 V
REF OUT to AGND . . . . . 0 V to V_{DD}
Digital Inputs to DGND . . . . . −0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Commercial (J, K, L Versions – AD7870) . . . . . 0 to +70°C
Commercial (K, L Versions – AD7875) . . . . . 0 to +70°C
Industrial (A, B, C Versions – AD7870) . . . −25°C to +85°C
Industrial (B, C Versions – AD7875/AD7876) . . . . . −40°C to +85°C
Extended (S, T Versions) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

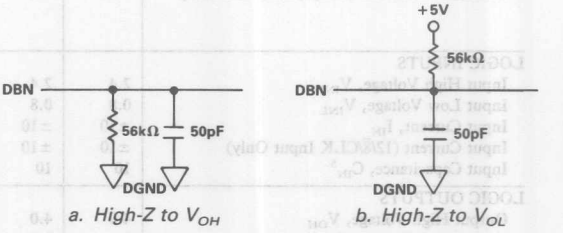


Figure 1. Load Circuits for Access Time

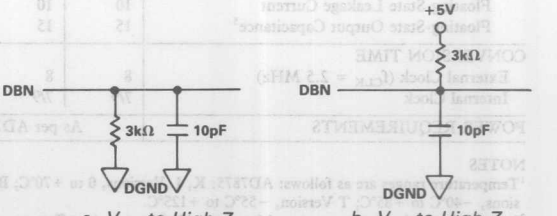


Figure 2. Load Circuits for Output Float Delay

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



AD7870 ORDERING GUIDE

Model[1, 2]	Temperature Range	V_{IN} Voltage Range (V)	SNR (dBs)	Integral Nonlinearity (LSB)	Package Option[3]
AD7870JN	0 to +70°C	±3	70 min	±1/2 typ	N-24
AD7870KN	0 to +70°C	±3	70 min	±1 max	N-24
AD7870LN	0 to +70°C	±3	72 min	±1/2 max	N-24
AD7870JP	0 to +70°C	±3	70 min	±1/2 typ	P-28A
AD7870KP	0 to +70°C	±3	70 min	±1 max	P-28A
AD7870LP	0 to +70°C	±3	72 min	±1/2 max	P-28A
AD7870AQ	−25°C to +85°C	±3	70 min	±1/2 typ	Q-24
AD7870BQ	−25°C to +85°C	±3	70 min	±1 max	Q-24
AD7870CQ	−25°C to +85°C	±3	72 min	±1/2 max	Q-24
AD7870SQ[4]	−55°C to +125°C	±3	70 min	±1/2 typ	Q-24
AD7870TQ[4]	−55°C to +125°C	±3	70 min	±1 max	Q-24

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact local sales office for military data sheet.
[2]Contact local sales office for LCCC (Leadless Ceramic Chip Carrier) availability.
[3]N = Narrow Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information section.
[4]Available to /883B processing only.

AD7875 ORDERING GUIDE

Model[1, 2]	Temperature Range	V_{IN} Voltage Range (V)	SNR (dBs)	Integral Nonlinearity (LSB)	Package Option[3]
AD7875KN	0 to +70°C	0 to +5	70 min	±1 max	N-24
AD7875LN	0 to +70°C	0 to +5	72 min	±1/2 max	N-24
AD7875KP	0 to +70°C	0 to +5	70 min	±1 max	P-28A
AD7875LP	0 to +70°C	0 to +5	72 min	±1/2 max	P-28A
AD7875BQ	−40°C to +85°C	0 to +5	70 min	±1 max	Q-24
AD7875CQ	−40°C to +85°C	0 to +5	72 min	±1/2 max	Q-24
AD7875TQ[4]	−55°C to +125°C	0 to +5	70 min	±1 max	Q-24

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact local sales office for military data sheet.
[2]Contact local sales office for LCCC (Leadless Ceramic Chip Carrier) availability.
[3]N = Narrow Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information section.
[4]Available to /883B processing only.

AD7876 ORDERING GUIDE

Model[1]	Temperature Range	V_{IN} Voltage Range (V)	Integral Nonlinearity (LSB)	Package Option[2]
AD7876BN	−40°C to +85°C	±10	±1 max	N-24
AD7876CN	−40°C to +85°C	±10	±1/2 max	N-24
AD7876BR	−40°C to +85°C	±10	±1 max	R–24
AD7876CR	−40°C to +85°C	±10	±1/2 max	R–24
AD7876BQ	−40°C to +85°C	±10	±1 max	Q-24
AD7876CQ	−40°C to +85°C	±10	±1/2 max	Q-24
AD7876TQ[3]	−55°C to +125°C	±10	±1 max	Q-24

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact local sales office for military data sheet.
[2]N = Narrow Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.
[2]Available to /883B processing only.

DIP Pin No.	Pin Mnemonic	Function
1	$\overline{RD}$	Read. Active low logic input. This input is used in conjunction with $\overline{CS}$ low to enable the data outputs.
2	$\overline{BUSY/INT}$	Busy/Interrupt, Active low logic output indicating converter status. See timing diagrams.
3	CLK	Clock input. An external TTL-compatible clock may be applied to this input pin. Alternatively, tying this pin to V_{SS} enables the internal laser-trimmed clock oscillator.
4	DB11/HBEN	Data Bit 11 (MSB)/High Byte Enable. The function of this pin is dependent on the state of the 12/$\overline{8}$/CLK input (see below). When 12-bit parallel data is selected, this pin provides the DB11 output. When byte data is selected, this pin becomes the HBEN logic input. HBEN is used for 8-bit bus interfacing. When HBEN is low, DB7/LOW to DB0/DB8 become DB7 to DB0. With HBEN high, DB7/LOW to DB0/DB8 are used for the upper byte of data (see Table I).
5	DB10/$\overline{SSTRB}$	Data Bit 10/Serial Strobe. When 12-bit parallel data is selected, this pin provides the DB10 output. $\overline{SSTRB}$ is an active low open-drain output that provides a strobe or framing pulse for serial data. An external 4.7 kΩ pull-up resistor is required on $\overline{SSTRB}$.
6	DB9/SCLK	Data Bit 9/Serial Clock. When 12-bit parallel data is selected, this pin provides the DB9 output. SCLK is the gated serial clock output derived from the internal or external ADC clock. If the 12/$\overline{8}$/CLK input is at −5 V, then SCLK runs continuously. If 12/$\overline{8}$/CLK is at 0 V, then SCLK is gated off after serial transmission is complete. SCLK is an open-drain output and requires an external 2 kΩ pull-up resistor.
7	DB8/SDATA	Data Bit 8/Serial Data. When 12-bit parallel data is selected, this pin provides the DB8 output. SDATA is an open-drain serial data output which is used with SCLK and $\overline{SSTRB}$ for serial data transfer. Serial data is valid on the falling edge of SCLK while $\overline{SSTRB}$ is low. An external 4.7 kΩ pull-up resistor is required on SDATA.
8–11	DB7/LOW–DB4/LOW	Three-state data outputs which are controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the 12/$\overline{8}$/CLK and HBEN inputs. With 12/$\overline{8}$/CLK high, they are always DB7-DB4. With 12/$\overline{8}$/CLK low or −5 V, their function is controlled by HBEN (see Table I).
12	DGND	Digital Ground. Ground reference for digital circuitry.
13–16	DB3/DB11–DB0/DB8	Three-state data outputs which are controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the 12/$\overline{8}$/CLK and HBEN inputs. With/12/$\overline{8}$/CLK high, they are always DB3-DB0. With 12/$\overline{8}$/CLK low or −5 V, their function is controlled by HBEN (see Table I).

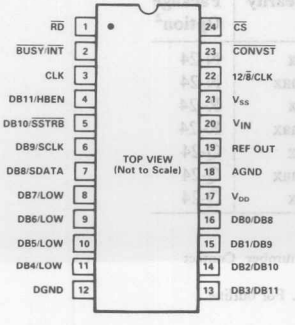
Table I. Output Data for Byte Interfacing

HBEN	DB7/LOW	DB6/LOW	DB5/LOW	DB4/LOW	DB3/DB11	DB2/DB10	DB1/DB9	DB0/DB8
HIGH	LOW	LOW	LOW	LOW	DB11 (MSB)	DB10	DB9	DB8
LOW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0 (LSB)

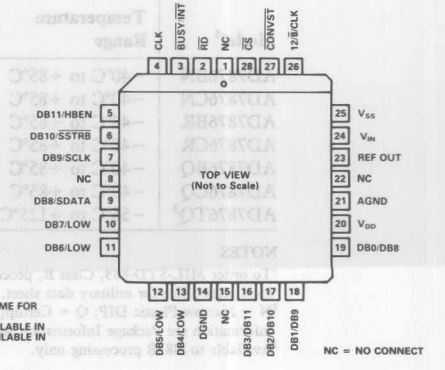
17	V_{DD}	Positive Supply, +5 V ±5%.
18	AGND	Analog Ground. Ground reference for track/hold, reference and DAC.
19	REF OUT	Voltage Reference Output. The internal 3 V reference is provided at this pin. The external load capability is 500 μA.
20	V_{IN}	Analog Input. The analog input range is ±3 V for the AD7870, ±10 V for the AD7876 and 0 to +5 V for the AD7875.
21	V_{SS}	Negative Supply, −5 V ±5%.
22	12/$\overline{8}$/CLK	Three Function Input. Defines the data format and serial clock format. With this pin at +5 V, the output data format is 12-bit parallel only. With this pin at 0 V, either byte or serial data is available and SCLK is not continuous. With this pin at −5 V, byte or serial data is again available but SCLK is now continuous.
23	$\overline{CONVST}$	Convert Start. A low to high transition on this input puts the track/hold into its hold mode and starts conversion. This input is asynchronous to the CLK input.
24	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active. With $\overline{CONVST}$ tied low, a new conversion is initiated when $\overline{CS}$ goes low.

PIN CONFIGURATIONS[1]

DIP and SOIC[2]



PLCC[2]



NC = NO CONNECT

[1]PIN CONFIGURATIONS ARE THE SAME FOR THE AD7870, AD7875 AND AD7876.
[2]THE AD7870 AND AD7875 ARE AVAILABLE IN DIP AND PLCC; THE AD7876 IS AVAILABLE IN DIP AND SOIC.

CONVERTER DETAILS

The AD7870/AD7875/AD7876 is a complete 12-bit A/D converter, requiring no external components apart from power supply decoupling capacitors. It is comprised of a 12-bit successive approximation ADC based on a fast settling voltage-output DAC, a high speed comparator and SAR, a track/hold amplifier, a 3 V buried Zener reference, a clock oscillator and control logic.

INTERNAL REFERENCE

The AD7870/AD7875/AD7876 has an on-chip temperature compensated buried Zener reference which is factory trimmed to 3 V ±10 mV. Internally it provides both the DAC reference and the dc bias required for bipolar operation (AD7870 and AD7876). The reference output is available (REF OUT) and is capable of providing up to 500 μA to an external load.

The maximum recommended capacitance on REF OUT for normal operation is 50 pF. If the reference is required for use external to the ADC, it should be decoupled with a 200 Ω resistor in series with a parallel combination of a 10 μF tantalum capacitor and a 0.1 μF ceramic capacitor. These decoupling components are required to remove voltage spikes caused by the ADC's internal operation.

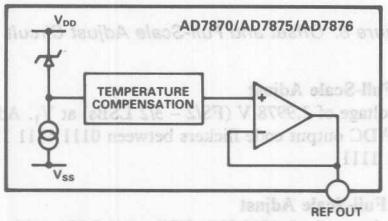


Figure 3. Reference Circuit

The reference output voltage is 3 V. For applications using the AD7875 or AD7876, a 5 V or 10 V reference may be required. Figure 4 shows how to scale the 3 V REF OUT voltage to provide either a 5 V or 10 V external reference.

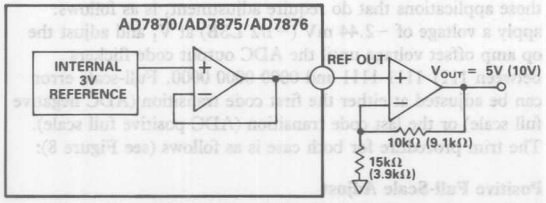


Figure 4. Generating a 5 V or 10 V Reference

TRACK-AND-HOLD AMPLIFIER

The track-and-hold amplifier on the analog input of the AD7870/AD7875/AD7876 allows the ADC to accurately convert input frequencies to 12-bit accuracy. The input bandwidth of the track/hold amplifier is much greater than the Nyquist rate of the ADC even when the ADC is operated at its maximum throughput rate. The 0.1 dB cutoff frequency occurs typically at 500 kHz. The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 2 μs. The overall throughput rate is equal to the conversion time plus the track/hold amplifier acquisition time. For a 2.5 MHz input clock the throughput rate is 10 μs max.

The operation of the track/hold is essentially transparent to the user. The track/hold amplifier goes from its tracking mode to its hold mode at the start of conversion. If the $\overline{\text{CONVST}}$ input is used to start conversion then the track to hold transition occurs on the rising edge of $\overline{\text{CONVST}}$. If $\overline{\text{CS}}$ starts conversion, this transition occurs on the falling edge of $\overline{\text{CS}}$.

2

ANALOG INPUT

The three parts differ from each other in the analog input voltage range which they can handle. The AD7870 accepts ±3 V input signals, the AD7876 accepts a ±10 V input range, while the input range for the AD7875 is 0 to +5 V.

Figure 5a shows the AD7870 analog input. The analog input range is ±3 V into an input resistance of typically 15 kΩ. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS−3/2 LSBs). The output code is 2s complement binary with 1 LSB = FS/4096 =6 V/4096 =1.46 mV. The ideal input/output transfer function is shown in Figure 6.

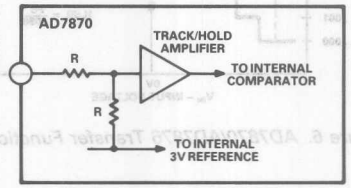


Figure 5a. AD7870 Analog Input

The AD7876 analog input structure is shown in Figure 5b. The analog input range is ±10 V into an input resistance of typically 33 kΩ. As before, the designed code transitions occur midway between successive integer LSB values. The output code is 2s complement with 1 LSB = FS/4096 = 20V/4096 = 4.88 mV. The ideal input/output transfer function is shown in Figure 6.

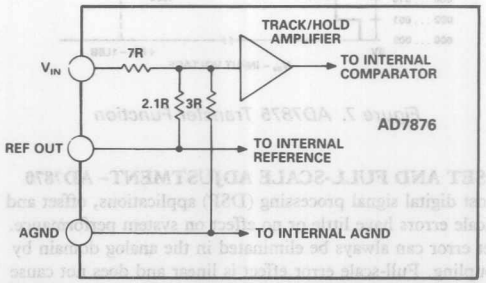


Figure 5b. AD7876 Analog Input

Figure 5c shows the analog input for the AD7875. The input range is 0 to +5 V into an input resistance of typically 25 kΩ. Once again, the designed code transitions occur midway between successive integer LSB values. The output code is

straight binary with 1 LSB = FS/4096 = 5V/4096 = 1.22 mV. The ideal input/output transfer function is shown in Figure 7.

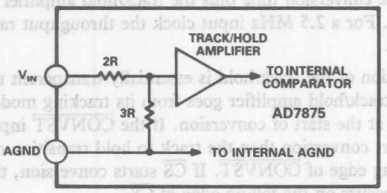


Figure 5c. AD7875 Analog Input

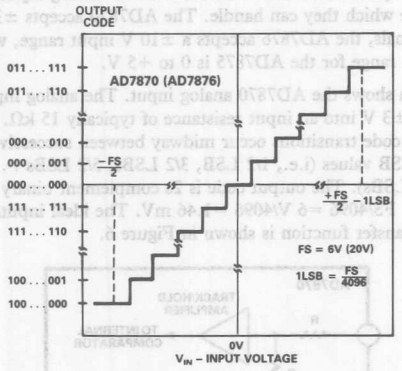


Figure 6. AD7870/AD7876 Transfer Function

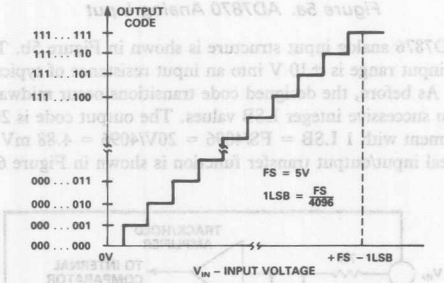


Figure 7. AD7875 Transfer Function

OFFSET AND FULL-SCALE ADJUSTMENT– AD7870

In most digital signal processing (DSP) applications, offset and full-scale errors have little or no effect on system performance. Offset error can always be eliminated in the analog domain by ac coupling. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. Some applications will require that the input signal span the full analog input dynamic range. In such applications, offset and full-scale error will have to be adjusted to zero.

Where adjustment is required, offset error must be adjusted before full-scale error. This is achieved by trimming the offset of the op amp driving the analog input of the AD7870 while the input voltage is 1/2 LSB below ground. The trim procedure is as follows: apply a voltage of −0.73 mV(−1/2 LSB) at V_1 in Figure 8 and adjust the op amp offset voltage until the ADC output code flickers between 1111 1111 1111 and 0000 0000 0000. Gain error can be adjusted at either the first code transition (ADC negative full-scale) or the last code transition (ADC positive full scale). The trim procedures for both cases are as follows (see Figure 8).

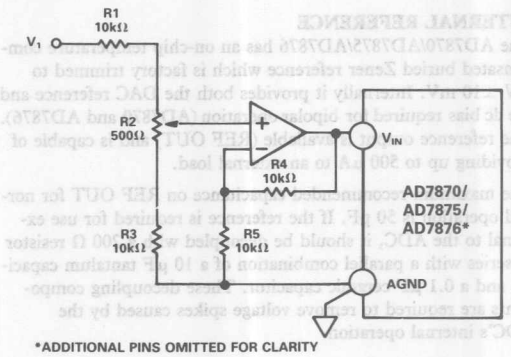


Figure 8. Offset and Full-Scale Adjust Circuit

Positive Full-Scale Adjust
Apply a voltage of 2.9978 V (FS/2 – 3/2 LSBs) at V_1. Adjust R2 until the ADC output code flickers between 0111 1111 1110 and 0111 1111 1111.

Negative Full-Scale Adjust
Apply a voltage of −2.9993 V (−FS/2 +1/2 LSB) at V_1 and adjust R2 until the ADC output code flickers between 1000 0000 0000 and 1000 0000 0001.

OFFSET AND FULL-SCALE ADJUSTMENT – AD7876

The offset and full-scale adjustment for the AD7876 is similar to that just outlined for the AD7870. The trim procedure, for those applications that do require adjustment, is as follows: apply a voltage of −2.44 mV (−1/2 LSB) at V_1 and adjust the op amp offset voltage until the ADC output code flickers between 1111 1111 1111 and 0000 0000 0000. Full-scale error can be adjusted at either the first code transition (ADC negative full scale) or the last code transition (ADC positive full scale). The trim procedure for both case is as follows (see Figure 8):

Positive Full-Scale Adjust
Apply a voltage of 9.9927 V (FS/2 − 3/2 LSBs) at V_1. Adjust R2 until the ADC output code flickers between 0111 1111 1110 and 0111 1111 1111.

Negative Full-Scale Adjust
Apply a voltage of −9.9976 V (FS/2 + 1/2 LSB) at V_1 and adjust R2 until the ADC output code flickers between 1000 0000 0000 and 1000 0000 0001.

OFFSET AND FULL-SCALE ADJUSTMENT – AD7875

Similar to the AD7870, most of the DSP applications in which the AD7875 will be used will not require offset and full-scale adjustment. For applications that do require adjustment, offset error must be adjusted before full-scale (gain) error. This is achieved by applying an input voltage of 0.61 mV (1/2 LSB) to V_1 in Figure 8 and adjusting the op amp offset voltage until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001. For full-scale adjustment, apply an input voltage of 4.9982 V (FS − 3/2 LSBs) to V_1 and adjust R2 until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

TIMING AND CONTROL

The AD7870/AD7875/AD7876 is capable of two basic operating modes. In the first mode (Mode 1), the $\overline{\text{CONVST}}$ line is used to start conversion and drive the track/hold into its hold mode. At the end of conversion the track/hold returns to its tracking mode. It is intended principally for digital signal processing and other applications where precise sampling in time is required. In these applications, it is important that the signal sampling occurs at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. For these cases, the $\overline{\text{CONVST}}$ line is driven by a timer or some precise clock source.

The second mode is achieved by hard-wiring the $\overline{\text{CONVST}}$ line low. This mode (Mode 2) is intended for use in systems where the microprocessor has total control of the ADC, both initiating the conversion and reading the data. $\overline{\text{CS}}$ starts conversion and the microprocessor will normally be driven into a WAIT state for the duration of conversion by $\overline{\text{BUSY/INT}}$.

DATA OUTPUT FORMATS

In addition to the two operating modes, the AD7870/AD7875/AD7876 also offers a choice of three data output formats, one serial and two parallel. The parallel data formats are a single, 12-bit parallel word for 16-bit data buses and a two-byte format for 8-bit data buses. The data format is controlled by the 12/$\overline{8}$/CLK input. A logic high on this pin selects the 12-bit parallel output format only. A logic low or −5 V applied to this pin allows the user access to either serial or byte formatted data. Three of the pins previously assigned to the four MSBs in parallel form are now used for serial communications while the fourth pin becomes a control input for the byte-formatted data. The three possible data output formats can be selected in either of the modes of operation.

Parallel Output Format

The two parallel formats available on the part are a 12-bit wide data word and a two-byte data word. In the first, all 12 bits of data are available at the same time on DB11 (MSB) through DB0 (LSB). In the second, two reads are required to access the data. When this data format is selected, the DB11/HBEN pin assumes the HBEN function. HBEN selects which byte of data is to be read from the ADC. When HBEN is low, the lower 8 bits of data are placed on the data bus during a read operation; with HBEN high, the upper 4 bits of the 12-bit word are placed on the data bus. These 4 bits are right justified and thereby occupy the lower nibble of data while the upper nibble contains four zeros.

Serial Output Format

Serial data is available on the AD7870/AD7875/AD7876 when the 12/$\overline{8}$/CLK input is at 0 V or −5 V and in this case the DB10/$\overline{\text{SSTRB}}$, DB9/SCLK and DB8/SDATA pins assume their serial functions. Serial data is available during conversion with a word length of 16 bits; four leading zeros, followed by the 12-bit conversion result starting with the MSB. The data is synchronized to the serial clock output (SCLK) and is framed by the serial strobe ($\overline{\text{SSTRB}}$). Data is clocked out on a low to high transition of the serial clock and is valid on the falling edge of this clock while the $\overline{\text{SSTRB}}$ output is low. $\overline{\text{SSTRB}}$ goes low within three clock cycles after $\overline{\text{CONVST}}$, and the first serial data bit (which is the first leading zero) is valid on the first falling edge of SCLK. All three serial lines are open-drain outputs and require external pull-up resistors.

The serial clock out is derived from the ADC clock source which may be internal or external. Normally, SCLK is required during the serial transmission only. In these cases, it can be shut down at the end of conversion to allow multiple ADCs to share a common serial bus. However, some serial systems (e.g., TMS32020) require a serial clock which runs continuously. Both options are available on the AD7870/AD7875/AD7876 using the 12/$\overline{8}$/CLK input. With this input at −5 V, the serial clock (SCLK) runs continuously; when 12/$\overline{8}$/CLK is at 0 V, SCLK is turned off at the end of transmission.

MODE 1 INTERFACE

Conversion is initiated by a low going pulse on the $\overline{\text{CONVST}}$ input. The rising edge of this $\overline{\text{CONVST}}$ pulse starts conversion and drives the track/hold amplifier into its hold mode. Conversion will not be initiated if the $\overline{\text{CS}}$ is low. The $\overline{\text{BUSY/INT}}$ status output assumes its $\overline{\text{INT}}$ function in this mode. $\overline{\text{INT}}$ is normally high and goes low at the end of conversion. This $\overline{\text{INT}}$ line can be used to interrupt the microprocessor. A read operation to the ADC accesses the data and the $\overline{\text{INT}}$ line is reset high on the falling edge of $\overline{\text{CS}}$ and $\overline{\text{RD}}$. The $\overline{\text{CONVST}}$ input must be high when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are brought low for the ADC to operate correctly in this mode. The $\overline{\text{CS}}$ or $\overline{\text{RD}}$ input should not be hard-wired low in this mode. Data cannot be read from the part during conversion because the on-chip latches are disabled when conversion is in progress. In applications where precise sampling is not critical, the $\overline{\text{CONVST}}$ pulse can be generated from a microprocessor $\overline{\text{WR}}$ line OR-gated with a decoded address. In some applications, depending on power supply turn-on time, the AD7870/AD7875/AD7876 may perform a conversion on power-up. In this case, the $\overline{\text{INT}}$ line will power-up low and a dummy read to the AD7870/AD7875/AD7876 will be required to reset the $\overline{\text{INT}}$ line before starting conversion.

Figure 9 shows the Mode 1 timing diagram for a 12-bit parallel data output format (12/$\overline{8}$/CLK = +5 V). A read to the ADC at the end of conversion accesses all 12 bits of data at the same time. Serial data is not available for this data output format.

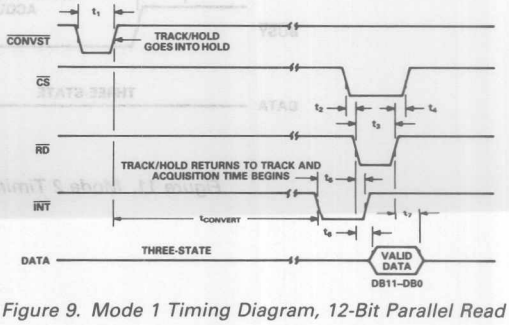


Figure 9. Mode 1 Timing Diagram, 12-Bit Parallel Read

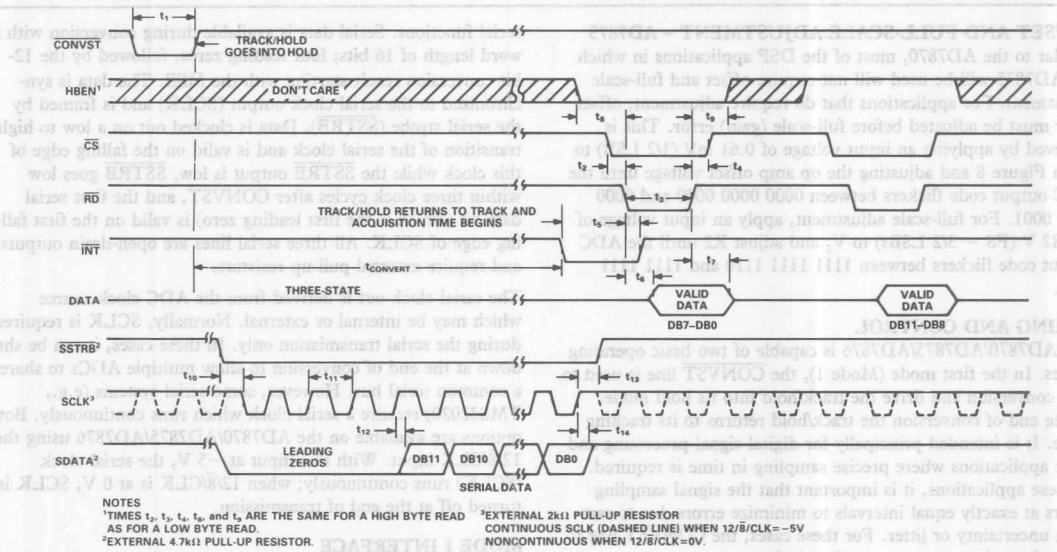


Figure 10. Mode 1 Timing Diagram, Byte or Serial Read

The Mode 1 timing diagram for byte and serial data is shown in Figure 10. $\overline{INT}$ goes low at the end of conversion and is reset high by the first falling edge of $\overline{CS}$ and $\overline{RD}$. This first read at the end of conversion can either access the low byte or high byte of data depending on the status of HBEN (Figure 10 shows low byte only for example). The diagram shows both a noncontinuously and a continuously running clock (dashed line).

MODE 2 INTERFACE

The second interface mode is achieved by hard wiring $\overline{CONVST}$ low and conversion is initiated by taking $\overline{CS}$ low while HBEN is low. The track/hold amplifier goes into the hold mode on the falling edge of $\overline{CS}$. In this mode, the $\overline{BUSY}$/$\overline{INT}$ pin assumes its $\overline{BUSY}$ function. $\overline{BUSY}$ goes low at the start of conversion, stays low during the conversion and returns high when the conversion is complete. It is normally used in parallel interfaces to drive the microprocessor into a WAIT state for the duration of conversion.

Figure 11 shows the Mode 2 timing diagram for the 12-bit parallel data output format (12/$\overline{8}$/CLK = +5 V). In this case, the ADC behaves like slow memory. The major advantage of this interface is that it allows the microprocessor to start conversion, WAIT and then read data with a single READ instruction. The user does not have to worry about servicing interrupts or ensuring that software delays are long enough to avoid reading during conversion.

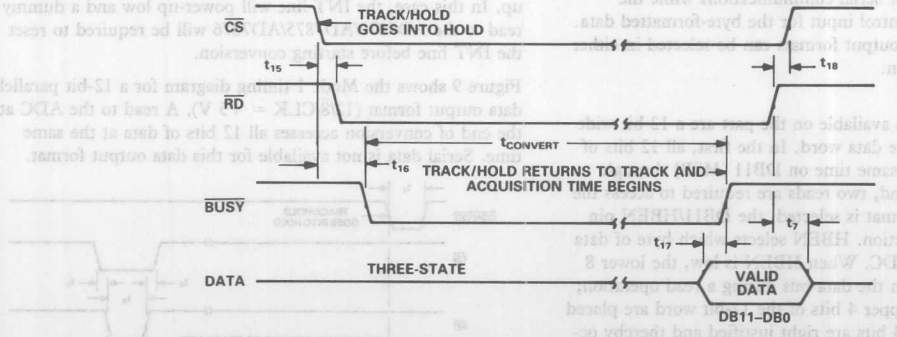


Figure 11. Mode 2 Timing Diagram, 12-Bit Parallel Read

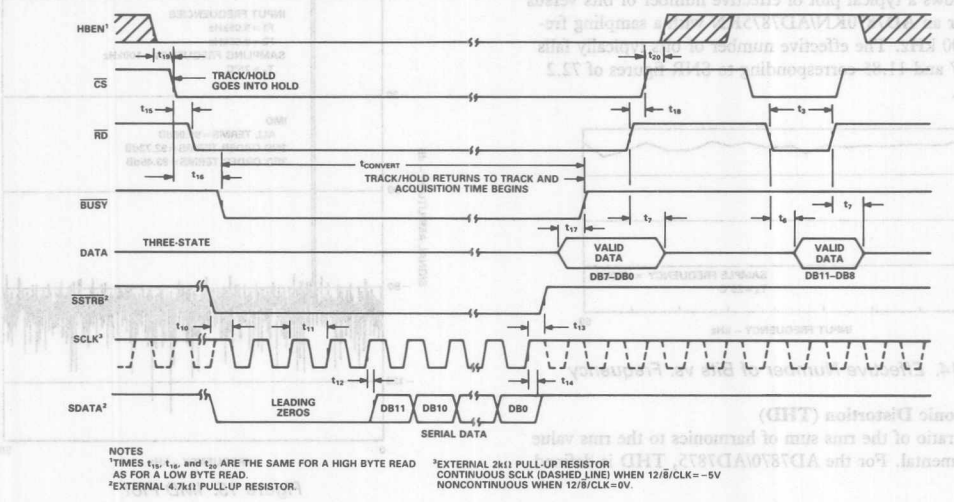


Figure 12. Mode 2 Timing Diagram, Byte or Serial Read

The Mode 2 timing diagram for byte and serial data is shown in Figure 12. For two-byte data read, the lower byte (DB0–DB7) has to be accessed first since HBEN must be low to start conversion. The ADC behaves like slow memory for this first read, but the second read to access the upper byte of data is a normal read. Operation of the serial functions is identical between Mode 1 and Mode 2. The timing diagram of Figure 12 shows both a noncontinuously and a continuously running SCLK (dashed line).

DYNAMIC SPECIFICATIONS

The AD7870 and AD7875 are specified and 100% tested for dynamic performance specifications as well as traditional dc specifications such as integral and differential nonlinearity. Although the AD7876 is not production tested for ac parameters, its dynamic performance is similar to the AD7870 and AD7875. The ac specifications are required for signal processing applications such as speech recognition, spectrum analysis and high speed modems. These applications require information on the ADC's effect on the spectral content of the input signal. Hence, the parameters for which the AD7870 and AD7875 are specified include SNR, harmonic distortion, intermodulation distortion and peak harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal-to-noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (FS/2) excluding dc. SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to noise ratio for a sine wave input is given by

$$SNR = (6.02N + 1.76)\ dB \qquad (1)$$

where N is the number of bits. Thus for an ideal 12-bit converter, SNR = 74 dB.

The output spectrum from the ADC is evaluated by applying a sine-wave signal of very low distortion to the V_{IN} input which is sampled at a 100 kHz sampling rate. A Fast Fourier Transform (FFT) plot is generated from which the SNR data can be obtained. Figure 13 shows a typical 2048 point FFT plot of the AD7870KN/AD7875KN with an input signal of 25 kHz and a sampling frequency of 100 kHz. The SNR obtained from this graph is 72.6 dB. It should be noted that the harmonics are taken into account when calculating the SNR.

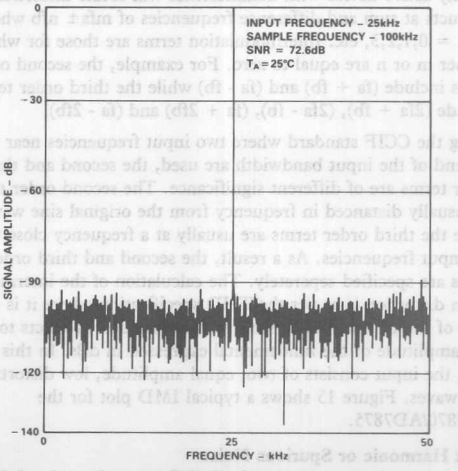


Figure 13. FFT Plot

Effective Number of Bits

The formula given in (1) relates the SNR to the number of bits. Rewriting the formula, as in (2), it is possible to get a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \qquad (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR.

quency of 100 kHz. The effective number of bits typically falls between 11.7 and 11.85 corresponding to SNR figures of 72.2 and 73.1 dB.

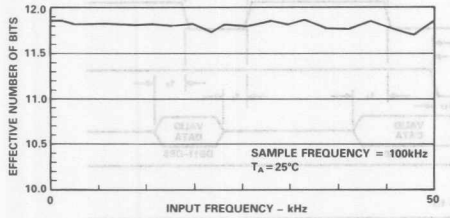


Figure 14. Effective Number of Bits vs. Frequency

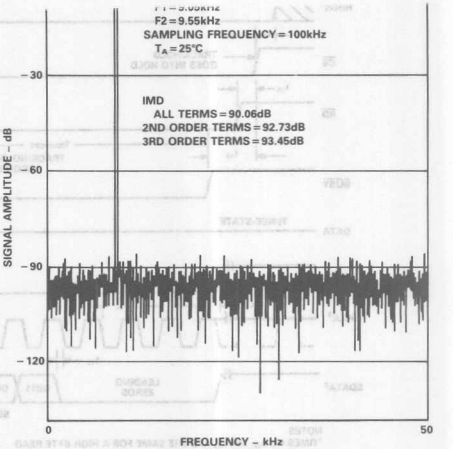


Figure 15. IMD Plot

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of harmonics to the rms value of the fundamental. For the AD7870/AD7875, THD is defined as

$$THD = 20\ log \frac{\sqrt{V_2^2+V_3^2+V_4^2+V_5^2+V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonic. The THD is also derived from the FFT plot of the ADC output spectrum.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa± nfb where m, n = 0,1,2,3, etc. Intermodulation terms are those for which neither m or n are equal to zero. For example, the second order terms include (fa + fb) and (fa - fb) while the third order terms include (2fa + fb), (2fa - fb), (fa + 2fb) and (fa - 2fb).

Using the CCIF standard where two input frequencies near the top end of the input bandwidth are used, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs. In this case, the input consists of two, equal amplitude, low distortion sine waves. Figure 15 shows a typical IMD plot for the AD7870/AD7875.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to FS/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor the peak will be a noise peak.

AC Linearity Plot

When a sine wave of specified frequency is applied to the V_{IN} input of the AD7870/AD7875 and several million samples are taken, a histogram showing the frequency of occurrence of each of the 4096 ADC codes can be generated. From this histogram data it is possible to generate an ac integral linearity plot as shown in Figure 16. This shows very good integral linearity performance from the AD7870/AD7875 at an input frequency of 25 kHz. The absence of large spikes in the plot shows good differential linearity. Simplified versions of the formulae used are outlined below.

$$INL(i) = \left[\frac{V(i) - V(o)}{V(fs) - V(o)} \cdot 4096\right] - i$$

where INL(i) is the integral linearity at code i. V(fs) and V(o) are the estimated full-scale and offset transitions and V(i) is the estimated transition for the ith code.

V(i) the estimated code transition point is derived as follows:

$$V(i) = -A \cdot Cos\ \frac{[\pi \cdot cum(i)]}{N}$$

where A is the peak signal amplitude,

N is the number of histogram samples

and $cum(i) = \sum_{n=0}^{i} V(n)$ occurrences

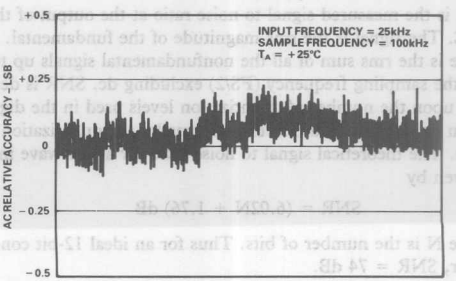


Figure 16. AC INL Plot

MICROPROCESSOR INTERFACE

The AD7870/AD7875/AD7876 has a wide variety of interfacing options. It offers two operating modes and three data-output formats. Fast data access times allow direct interfacing to most microprocessors including the DSP processors.

Parallel Read Interfacing

Figures 17 to 19 show interfaces to the ADSP-2100, TMS32010 and the TMS32020 DSP processors. The ADC is operating in Mode 1, parallel read for all three interfaces. An external timer controls conversion start asynchronously to the microprocessor. At the end of each conversion the ADC $\overline{BUSY/INT}$ interrupts the microprocessor. The conversion result is read from the ADC with the following instruction:

ADSP-2100: MR0 = DM(ADC)

TMS32010: IN D,ADC

TMS32020: IN D,ADC

MR0 = ADSP-2100 MR0 Register

D = Data Memory Address

ADC = AD7870/AD7875/AD7876 Address

Some applications may require that conversions be initiated by the microprocessor rather than an external timer. One option is to decode the $\overline{CONVST}$ signal from the address bus so that a write operation to the ADC starts a conversion. Data is read at the end of conversion as described earlier. Note, a read operation must not be attempted during conversion.

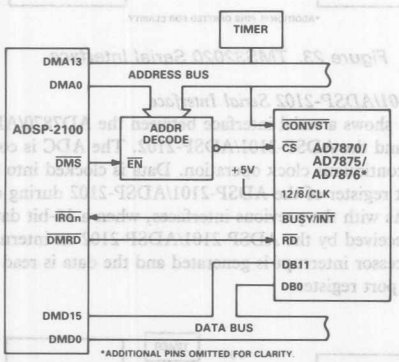


Figure 17. ADSP-2100 Parallel Interface

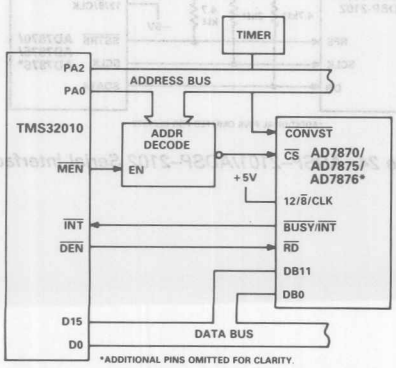


Figure 18. TMS32010 Parallel Interface

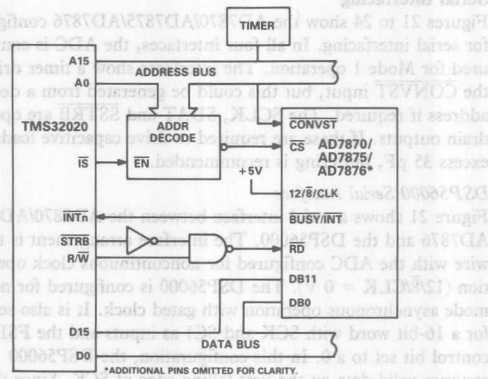


Figure 19. TMS32020 Parallel Interface

Two Byte Read Interfacing

68008 Interface

Figure 20 shows an 8-bit bus interface for the MC68008 microprocessor. For this interface, the 12/$\overline{8}$/CLK input is tied to 0 V and the DB11/HBEN pin is driven from the microprocessor least significant address bit. Conversion start control is provided by the microprocessor. In this interface example, a Move instruction from the ADC address both starts a conversion and reads the conversion result.

MOVEW ADC,DO

ADC = AD7870/AD7875/AD7876 address

D0 = 68008 D0 register

This is a two byte read instruction. During the first read operation, $\overline{BUSY}$ in conjunction with $\overline{CS}$ forces the microprocessor to WAIT for the ADC conversion. At the end of conversion the ADC low byte (DB7–DB0) is loaded into D15–D8 of the D0 register and the ADC high byte (DB15–DB7) is loaded into D7–D0 of the D0 register. The following Rotate instruction to the D0 register swaps the high and low bytes to the correct format.

R0L = 8, D0.

Note, while executing the two byte read instruction above, WAIT states are inserted during the first read operation only and not for the second.

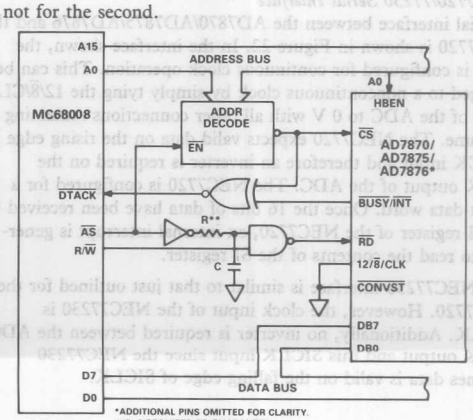


Figure 20. MC68008 Byte Interface

Serial Interfacing

Figures 21 to 24 show the AD7870/AD7875/AD7876 configured for serial interfacing. In all four interfaces, the ADC is configured for Mode 1 operation. The interfaces show a timer driving the $\overline{\text{CONVST}}$ input, but this could be generated from a decoded address if required. The SCLK, SDAT and $\overline{\text{SSTRB}}$ are open-drain outputs. If these are required to drive capacitive loads in excess 35 pF, buffering is recommended.

DSP56000 Serial Interface

Figure 21 shows a serial interface between the AD7870/AD7875/AD7876 and the DSP56000. The interface arrangement is two-wire with the ADC configured for noncontinuous clock operation (12/$\overline{8}$/CLK = 0 V). The DSP56000 is configured for normal mode asynchronous operation with gated clock. It is also set up for a 16-bit word with SCK and SC1 as inputs and the FSL control bit set to a 0. In this configuration, the DSP56000 assumes valid data on the first falling edge of SCK. Since the ADC provides valid data on this first edge, there is no need for a strobe or framing pulse for the data. SCLK and SDATA are gated off when the ADC is not performing a conversion. During conversion, data is valid on the SDATA output of the ADC and is clocked into the receive data shift register of the DSP56000. When this register has received 16 bits of data, it generates an internal interrupt on the DSP56000 to read the data from the register.

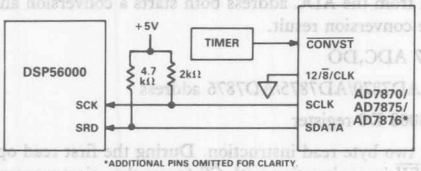


Figure 21. DSP56000 Serial Interface

The DSP56000 and AD7870/AD7875/AD7876 can also be configured for continuous clock operation (12/$\overline{8}$/CLK = −5 V). In this case, a strobe pulse is required by the DSP56000 to indicate when data is valid. The $\overline{\text{SSTRB}}$ output of the ADC is inverted and applied to the SC1 input of the DSP56000 to provide this strobe pulse. All other conditions and connections are the same as for gated clock operation.

NEC7720/77230 Serial Interface

A serial interface between the AD7870/AD7875/AD7876 and the NEC7720 is shown in Figure 22. In the interface shown, the ADC is configured for continuous clock operation. This can be changed to a noncontinuous clock by simply tying the 12/$\overline{8}$/CLK input of the ADC to 0 V with all other connections remaining the same. The NEC7720 expects valid data on the rising edge of its SCK input and therefore an inverter is required on the SCLK output of the ADC. The NEC7720 is configured for a 16-bit data word. Once the 16 bits of data have been received by the SI register of the NEC7720, an internal interrupt is generated to read the contents of the SI register.

The NEC77230 interface is similar to that just outlined for the NEC7720. However, the clock input of the NEC77230 is SICLK. Additionally, no inverter is required between the ADC SCLK output and this SICLK input since the NEC77230 assumes data is valid on the falling edge of SICLK.

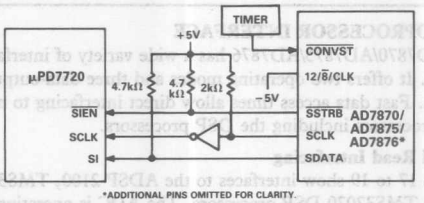


Figure 22. NEC7720 Serial Interface

TMS32020 Serial Interface

Figure 23 shows a serial interface between the AD7870/AD7875/AD7876 and the TMS32020. The AD7870/AD7875/AD7876 is configured for continuous clock operation. Note, the ADC will not interface correctly to the TMS32020 if the ADC is configured for a noncontinuous clock. Data is clocked into the data receive register (DRR) of the TMS32020 during conversion. As with the previous interfaces, when a 16-bit word is received by the TMS32020 it generates an internal interrupt to read the data from the DRR.

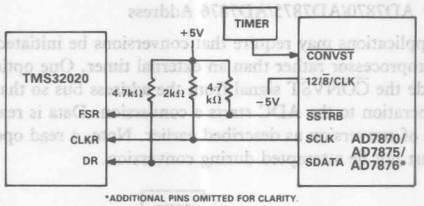


Figure 23. TMS32020 Serial Interface

ADSP-2101/ADSP-2102 Serial Interface

Figure 24 shows a serial interface between the AD7870/AD7875/AD7876 and the ADSP-2101/ADSP-2102. The ADC is configured for continuous clock operation. Data is clocked into the serial port register of the ADSP-2101/ADSP-2102 during conversion. As with the previous interfaces, when a 16-bit data word is received by the ADSP-2101/ADSP-2102 an internal microprocessor interrupt is generated and the data is read from the serial port register.

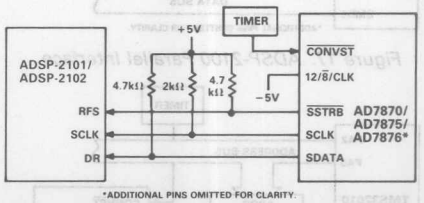
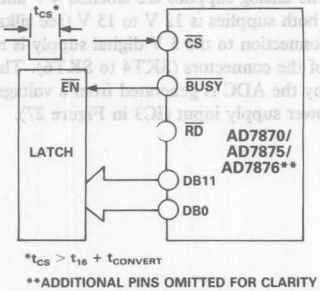


Figure 24. ADSP–2101/ADSP–2102 Serial Interface

STAND-ALONE OPERATION

The AD7870/AD7875/AD7876 can be used in its Mode 2, parallel interface mode for stand-alone operation. In this case, conversion is initiated with a pulse to the ADC $\overline{CS}$ input. This pulse must be longer than the conversion time of the ADC. The $\overline{BUSY}$ output is used to drive the $\overline{RD}$ input. Data is latched from the ADC DB0–DB11 outputs to an external latch on the rising edge of $\overline{BUSY}$.



*$t_{CS} > t_{16} + t_{CONVERT}$

**ADDITIONAL PINS OMITTED FOR CLARITY

Figure 25. Stand-Alone Operation

APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the overall circuit design itself in achieving high speed A/D performance. The designer has to be conscious of noise both in the ADC itself and in the preceding analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any ADC, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground at the AGND pin or as close as possible to the ADC. Connect all other grounds and the AD7870/AD7875/AD7876 DGND to this single analog ground point. Do not connect any other digital grounds to this analog ground point.

Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise. The circuit layout of Figures 30 and 31 have both analog and digital ground planes which are kept separated and only joined together at the AD7870/AD7875/AD7876 AGND pin.

NOISE

Keep the input signal leads to V_{IN} and signal return leads from AGND as short as possible to minimize input noise coupling. In applications where this is not possible, use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

DATA ACQUISITION BOARD

Figure 28 shows the AD7870/AD7875/AD7876 in a data acquisition circuit. The corresponding printed circuit board (PCB) layout and silkscreen are shown in Figures 29 to 31. The board layout has three interface ports: one serial and two parallel. One of the parallel ports is directly compatible with the ADSP-2100 evaluation board expansion connector.

The only additional component required for a full data acquisition system is an antialiasing filter. There is a component grid provided near the analog input on the PCB which may be used for such a filter or any other input conditioning circuitry. To facilitate this option there is a shorting plug (labelled LK1 on the PCB) on the analog input track. If this shorting plug is used, the analog input connects to the buffer amplifier driving the ADC; if this shorting plug is omitted, a wire link can be used to connect the analog input to the PCB component grid.

INTERFACE CONNECTIONS

There are two parallel connectors labeled SKT4 and SKT6 and one serial connector labeled SKT5. A shorting plug option (LK3 in Figure 28) on the ADC 12/$\overline{8}$/CLK input configures the ADC for the appropriate interface (see Pin Function Description).

SKT6 is a 96-contact (3-ROW) Eurocard connector which is directly compatible with the ADSP-2100 Evaluation Board Prototype Expansion Connector. The expansion connector on the ADSP-2100 has eight decoded chip enable outputs labeled $\overline{ECE1}$ to $\overline{ECE8}$. $\overline{ECE6}$ is used to drive the ADC $\overline{CS}$ input on the data acquisition board. To avoid selecting on board RAM sockets at the same time, LK6 on the ADSP-2100 board must be removed. In addition, the ADSP-2100 expansion connector has four interrupts labelled $\overline{EIRQ0}$ to $\overline{EIRQ3}$. The ADC $\overline{BUSY/INT}$ output connects to $\overline{EIRQ0}$. There is a single wait state generator connected to EDMACK to allow the ADC to interface to the faster versions of the ADSP-2100.

SKT4 is a 26-way (2-ROW) IDC connector. This connector contains all the signal contacts as SKT6 with the exception of EDMACK which is connected to SKT6 only. It also contains decoded R/$\overline{W}$ and $\overline{STRB}$ inputs which are necessary for TMS32020 interfacing. The SKT4 pinout is shown in Figure 26.

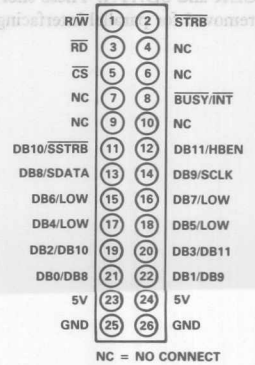


Figure 26. SKT4, IDC Connector Pinout

SKT5 is a 9 way D-type connector which is meant for serial interfacing only. An inverted DB9/SCLK output is also provided on this connector for systems which accept data on a rising clock edge. The SKT5 pinout is shown in Figure 27.

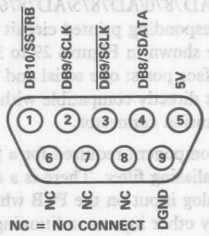


Figure 27. SKT5, D-Type Connector Pinout

SKT1, SKT2 and SKT3 are three BNC connectors which provide input connections for the analog input, the $\overline{\text{CONVST}}$ input and an external clock input. The use of an external clock source is optional, there is a shorting plug (LK2) on the ADC CLK input which must be connected to either −5 V (for the ADCs own internal clock) or to SKT3.

POWER SUPPLY CONNECTIONS

The PCB requires two analog power supplies and one 5 V digital supply . The analog supplies are labelled V+ and V−, and the range for both supplies is 12 V to 15 V (see silkscreen in Figure 29). Connection to the 5 V digital supply is made through any of the connectors (SKT4 to SKT6). The −5 V supply required by the ADC is generated from a voltage regulator on the V− power supply input (IC3 in Figure 27).

SHORTING PLUG OPTIONS

There are seven shorting plug options which must be set before using the board. These are outlined below:

LK1 Connects the analog input to a buffer amplifier. The analog input may also be connected to a component grid for signal conditioning.

LK2 Selects either the ADC internal clock or an external clock source.

LK3 Configures the ADC 12/$\overline{8}$/CLK input for the appropriate serial or parallel interface.

LK4 Connects the ADC $\overline{\text{RD}}$ input directly to the two parallel connectors or to a decoded $\overline{\text{STRB}}$ and R/$\overline{\text{W}}$ input. This shorting plug setting depends on the microprocessor e.g., the TMS32010 has a separate $\overline{\text{RD}}$ output while the TMS32020 has $\overline{\text{STRB}}$ and R/$\overline{\text{W}}$ outputs.

LK5– LK7 Connect the pull-up resistors R3, R4 and R5 to $\overline{\text{SSTRB}}$, SCLK and SDATA. These shorting plugs should be removed for parallel interfacing.

COMPONENT LIST

IC1	AD711 Op Amp
IC2	AD7870/AD7875/AD7876 Analog-to-Digital Converter
IC3	MC79L05 −5 V Regulator
IC4	74HC00 Quad NAND Gate
IC5	74HC74 Dual D-Type Flip Flop
C1, C3, C5, C7, C9, C11	10 μF Capacitors
C2, C4, C6, C8, C10, C12	0.1 μF Capacitors
R1, R2	10 kΩ Pull-Up Resistors
R3*, R5*	4.7 kΩ Pull-Up Resistors
R4*	2 kΩ Pull-Up Resistor
LK1, LK2 LK3, LK4 LK5, LK6, LK7	Shorting Plugs
SKT1, SKT2, SKT3	BNC Sockets
SKT4	26-Contact (2-Row) IDC Connector
SKT5	9-Contact D-Type Connector
SKT6	96-Contact (3-Row) Eurocard Connector

*Required for Serial Communication only.

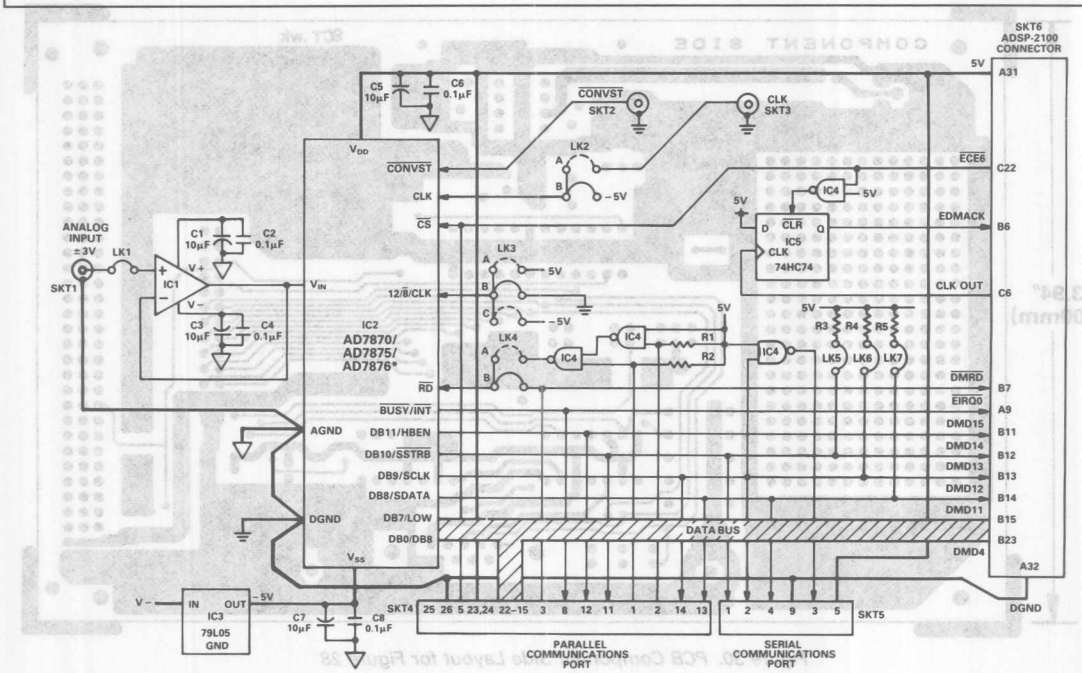


Figure 28. Data Acquisition Circuit Using the AD7870/AD7875/AD7876

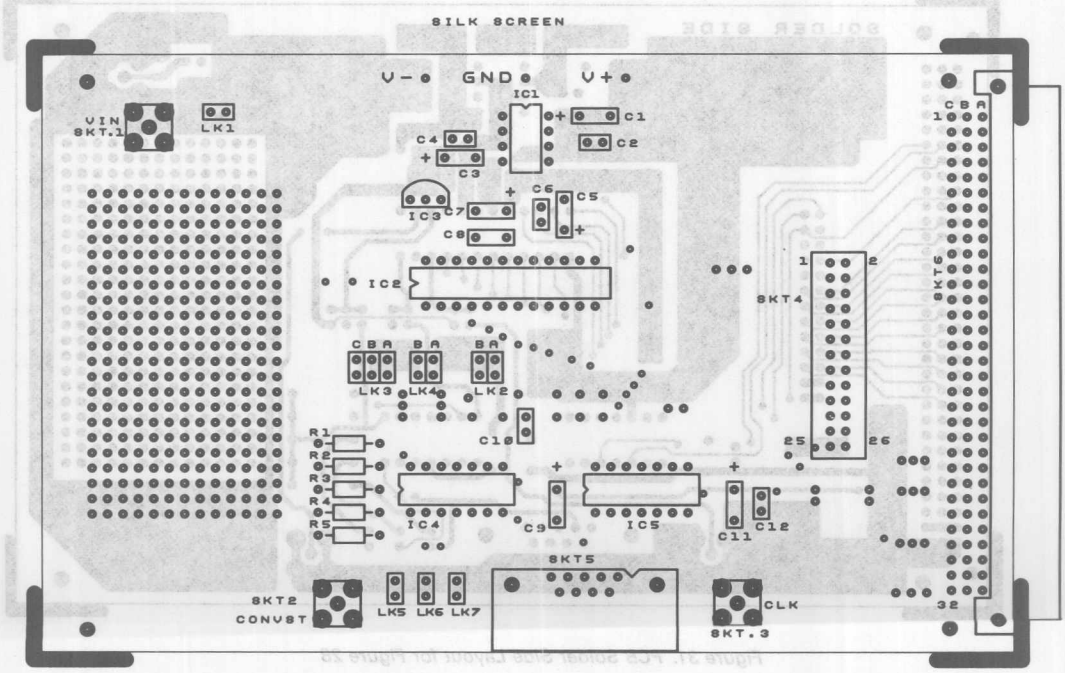


Figure 29. PCB Silkscreen for Figure 28

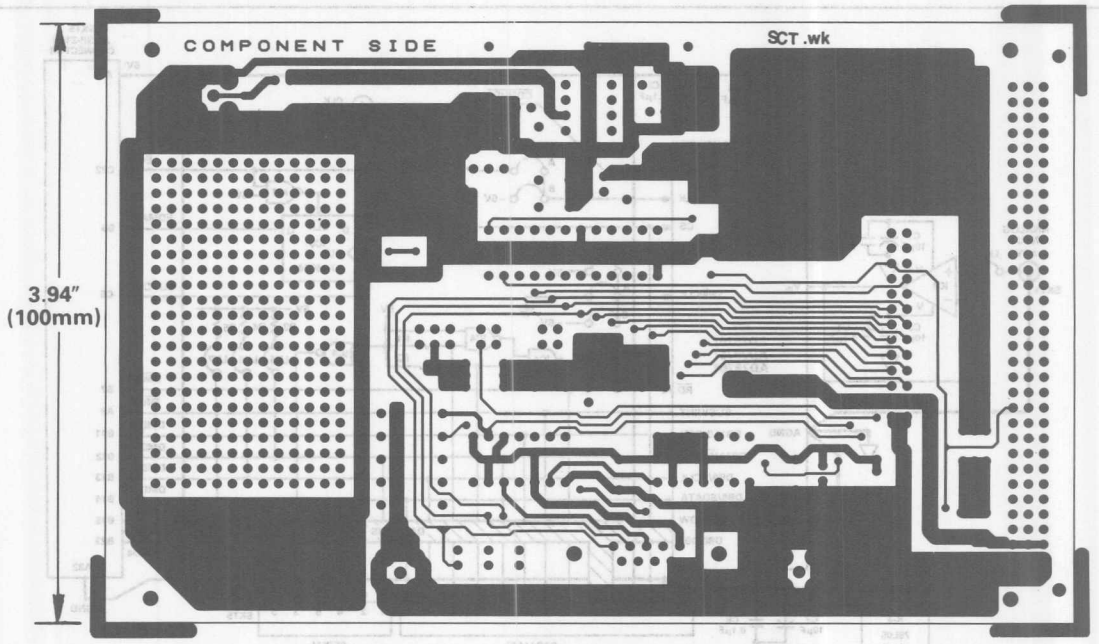


Figure 30. PCB Component Side Layout for Figure 28

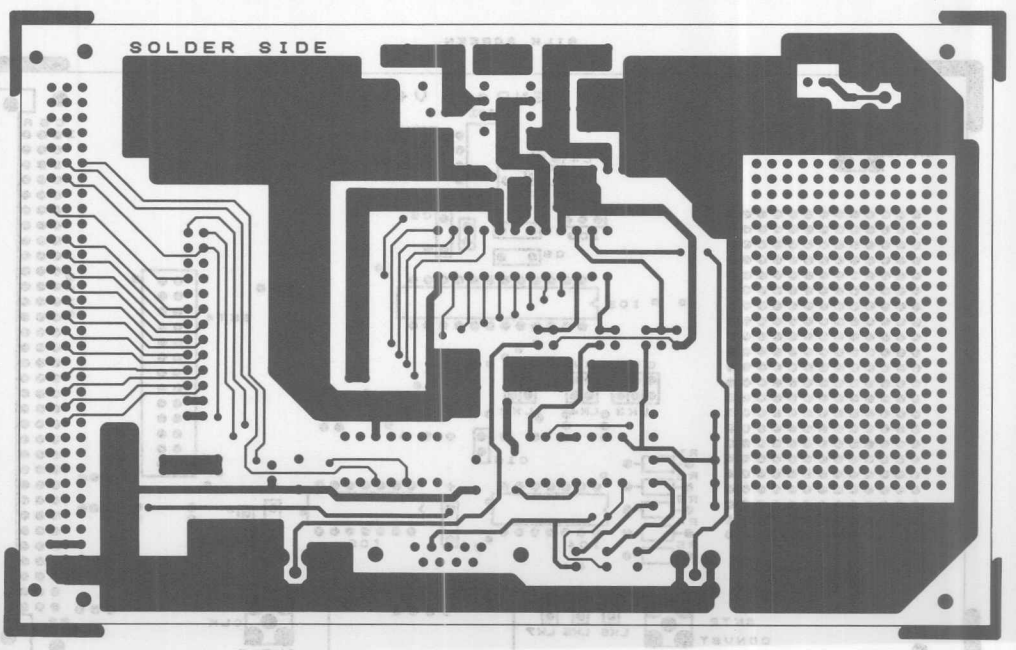


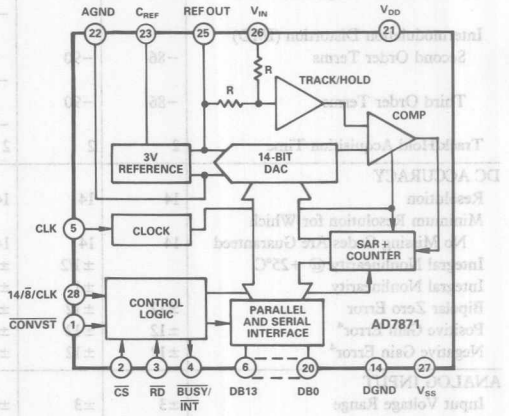
Figure 31. PCB Solder Side Layout for Figure 28

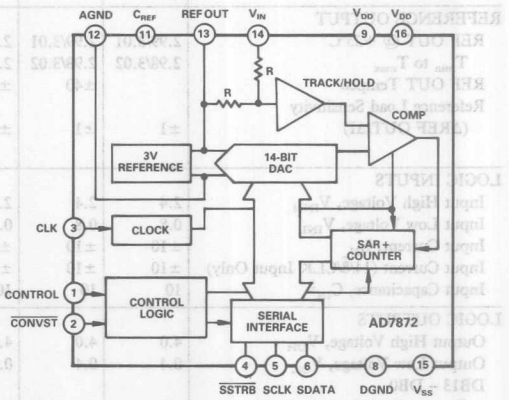
LC²MOS
Complete 14-Bit, Sampling ADCs
AD7871/AD7872

FEATURES
- Complete Monolithic 14-Bit ADC
- 2s Complement Coding
- Parallel, Byte and Serial Digital Interface
- 80 dB SNR at 10 kHz Input Frequency
- 57 ns Data Access Time
- Low Power—50 mW typ
- 83 kSPS Throughput Rate
- 16-Lead SOIC (AD7872)

APPLICATIONS
- Digital Signal Processing
- High Speed Modems
- Speech Recognition and Synthesis
- Spectrum Analysis
- DSP Servo Control

FUNCTIONAL BLOCK DIAGRAMS





GENERAL DESCRIPTION

The AD7871 and AD7872 are fast, complete, 14-bit analog-to-digital converters. They consist of a track/hold amplifier, successive-approximation ADC, 3 V buried Zener reference and versatile interface logic. The ADC features a self-contained, laser trimmed internal clock, so no external clock timing components are required. The on-chip clock may be overridden to synchronize ADC operation to the digital system for minimum noise.

The AD7871 offers a choice of three data output formats: a single, parallel, 14-bit word; two 8-bit bytes or a 14-bit serial data stream. The AD7872 is a serial output device only. The two parts are capable of interfacing to all modern microprocessors and digital signal processors.

The AD7871 and AD7872 operate from ±5 V power supplies, accept bipolar input signals of ±3 V and can convert full power signals up to 41.5 kHz.

In addition to the traditional dc accuracy specifications, the AD7871 and AD7872 are also fully specified for dynamic performance parameters including distortion and signal-to-noise ratio.

Both devices are fabricated in Analog Devices' LC²MOS mixed technology process. The AD7871 is available in 28-pin plastic DIP, hermetic DIP and PLCC packages. The AD7872 is available in 16-pin plastic and hermetic DIP packages or 16-lead SOIC.

PRODUCT HIGHLIGHTS

1. Complete 14-Bit ADC on a Chip.
2. Dynamic Specifications for DSP Users.
3. Low Power.

Parameter	J, A Versions[1]	K, B Versions[1]	T Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					
Signal to Noise Ratio[3] (SNR) @ +25°C	80	80	79	dB min	V_{IN} = 10 kHz Sine Wave
T_{min} to T_{max}	80	80	79	dB min	SNR is Typically 82 dB for $<V_{IN}<$41.5 kHz;
Total Harmonic Distortion (THD)	−86	−90		dB max	V_{IN} = 10 kHz Sine Wave
			−85	dB typ	
Peak Harmonic or Spurious Noise	−86	−90		dB max	V_{IN} = 10 kHz.
			−85	dB typ	
Intermodulation Distortion (IMD)					
Second Order Terms	−86	−90		dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
			−85	dB typ	
Third Order Terms	−86	−90		dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
			−85	dB typ	
Track/Hold Acquisition Time	2	2	2	μs max	
DC ACCURACY					
Resolution	14	14	14	Bits	
Minimum Resolution for Which					
No Missing Codes Are Guaranteed	14	14	14	Bits	
Integral Nonlinearity @ +25°C		±1/2	±1/2	LSB typ	
Integral Nonlinearity		±1	±1	LSB max	
Bipolar Zero Error	±12	±12	±12	LSB max	
Positive Gain Error[4]	±12	±12	±12	LSB max	
Negative Gain Error[4]	±12	±12	±12	LSB max	
ANALOG INPUT					
Input Voltage Range	±3	±3	±3	Volts	
Input Current	±500	±500	±500	μA max	
REFERENCE OUTPUT					
REF OUT @ +25°C	2.99/3.01	2.99/3.01	2.99/3.01	V min/V max	
T_{min} to T_{max}	2.98/3.02	2.98/3.02	2.98/3.02	V min/V max	
REF OUT Tempco		±40	±40	ppm/°C max	Typically 35 ppm
Reference Load Sensitivity					
(ΔREF OUT/ΔI)	±1	±1	±1	mV max	Reference Load Current Change (0–500 μA); Reference Load Should Not Be Changed During Conversion
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Current (14/8/CLK Input Only)	±10	±10	±10	μA max	V_{IN} = V_{SS} to V_{DD}
Input Capacitance, C_{IN}[5]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 40 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB13 – DB0					
Floating-State Leakage Current	10	10	10	μA max	
Floating-State Output Capacitance[5]	15	15	15	pF max	
CONVERSION TIME					
External Clock	10	10	10	μs max	
Internal Clock	10.5	10.5	10.5	μs max	The Internal Clock Has a Nominal Value of 2 MHz
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	13	13	13	mA max	Typically 6 mA
I_{SS}	6	6	6	mA max	Typically 4 mA
Power Dissipation	95	95	95	mW max	Typically 50 mW

NOTES

[1]Temperature ranges are as follows: J, K versions, 0°C to +70°C; A, B versions, −40°C to +85°C; T version; −55°C to +125°C.

[2]V_{IN} = ±3 V.

[3]SNR calculation includes distortion and noise components.

[4]Measured with respect to internal reference.

[5]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V. See Figures 9, 10, 11 and 12.)

Parameter	Limit at T_{min}, T_{max} (J, K, A, B Versions)	Limit at T_{min}, T_{max} (T Version)	Units	Conditions/Comments
t_1	50	50	ns min	$\overline{CONVST}$ Pulse Width
t_2	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time (Mode 1)
t_3	**60**	**75**	ns min	$\overline{RD}$ Pulse Width
t_4	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time (Mode 1)
t_5	70	70	ns min	$\overline{RD}$ to $\overline{INT}$ Delay
t_6[3]	**57**	**70**	ns max	Data Access Time after $\overline{RD}$
t_7[4]	5	5	ns min	Bus Relinquish Time after $\overline{RD}$
	50	**50**	ns max	
t_8	0	0	ns min	HBEN to $\overline{RD}$ Setup Time
t_9	0	0	ns min	HBEN to $\overline{RD}$ Hold Time
t_{10}	100	100	ns min	$\overline{SSTRB}$ to SCLK Falling Edge Setup Time
t_{11}[5]	440	440	ns min	SCLK Cycle Time
t_{12}[6]	155	155	ns max	SCLK to Valid Data Delay. C_L = 35 pF
t_{13}	140	150	ns max	SCLK Rising Edge to $\overline{SSTRB}$
	20	20	ns min	
t_{14}	4	4	ns min	Bus Relinquish Time after SCLK
	100	100	ns max	
t_{15}	60	60	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time (Mode 2)
t_{16}	120	120	ns max	$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay
t_{17}[3]	200	200	ns min	Data Setup Time Prior to $\overline{BUSY}$
t_{18}	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time (Mode 2)
t_{19}	0	0	ns min	HBEN to $\overline{CS}$ Setup Time
t_{20}	0	0	ns min	HBEN to $\overline{CS}$ Hold Time

NOTES

[1]Timing Specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]Serial timing is measured with a 4.7 kΩ pull-up resistor on SDATA and $\overline{SSTRB}$ and a 2 kΩ pull-up resistor on SCLK. The capacitance on all three outputs is 35 pF.

[3]t_6 and t_{17} are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[4]t_7 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_7, quoted in the Timing Characteristics is the true bus relinquish time of the part and is independent of bus loading.

[5]SCLK mark/space ratio (measured from a voltage level of 1.6 V) is 40/60 to 60/40.

[6]SDATA will drive higher capacitive loads, but this will add to t_{12} since it increases the external RC time constant (4.7 kΩ//C_L) and hence the time to reach 2.4 V.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{SS} to AGND . . . . . +0.3 V to −7 V
AGND to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
V_{IN} to AGND . . . . . V_{SS} − 0.3 V to V_{DD} + 0.3 V
REF OUT, C_{REF} to AGND . . . . . 0 V to V_{DD}
Digital Inputs to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
Digital Outputs to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Commercial (J, K Versions) . . . . . 0°C to +70°C
  Industrial (A, B Versions) . . . . . −40°C to +85°C
  Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 6 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

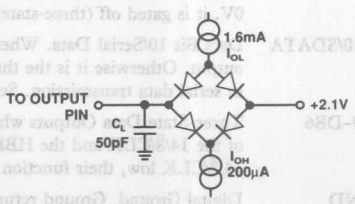


Figure 1. Load Circuit for Access Time

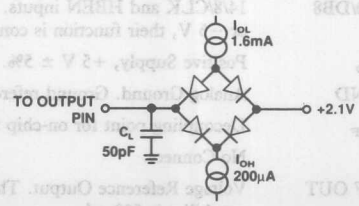


Figure 2. Load Circuit for Output Float Delay

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



AD7871 PIN FUNCTION DESCRIPTION

DIP No.	Mnemonic	Function
1	$\overline{\text{CONVST}}$	Convert Start. A low to high transition on this input puts the track/hold into the hold mode. This input is asynchronous to the CLK. $\overline{\text{CS}}$ and $\overline{\text{RD}}$ must be held high for the duration of this pulse.
2	$\overline{\text{CS}}$	Chip Select. Active low logic input. The device is selected when this input is active. With $\overline{\text{CONVST}}$ tied low, a new conversion is initiated when $\overline{\text{CS}}$ goes low.
3	$\overline{\text{RD}}$	Read. Active low logic input. This input is used in conjunction with $\overline{\text{CS}}$ low to enable the data outputs.
4	BUSY/INT	Busy/Interrupt. Logic low output indicating converter status. See timing diagrams.
5	CLK	Clock Input. An external TTL-compatible clock may be applied to this input. Alternatively, tying this pin to V_{SS} enables the internal laser-trimmed oscillator.
6	DB13/HBEN	Data Bit 13 (MSB)/High Byte Enable. The function of this pin is dependent on the state of the 14/$\overline{8}$/CLK input (see Pin 28). When 14-bit data is selected, this pin provides the DB13 output. When either byte or serial data is selected, this pin becomes the HBEN logic input. HBEN is used for 8-bit bus interfacing. When HBEN is low, DB7 to DB0 is the lower byte of data. With HBEN high, DB7 to DB0 is the upper byte of data (see Table I).

HBEN	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HIGH	LOW	LOW	DB13	DB12	DB11	DB10	DB9	DB8
LOW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Table I. Byte Output Format

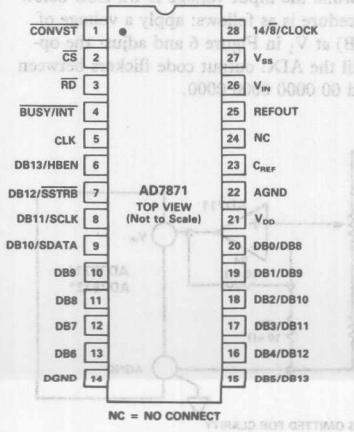
7	DB12/$\overline{\text{SSTRB}}$	Data Bit 12/Serial Strobe. When 14-bit data is selected, this pin provides the DB12 data output. Otherwise it is an active low three-state output which provides a framing pulse for serial data.
8	DB11/SCLK	Data Bit 11/Serial Clock. When 14-bit data is selected, this pin provides the DB11 data output. Otherwise SCLK is the gated serial clock output which is derived from the internal or external ADC clock. If the 14/$\overline{8}$/CLK input is held at −5 V, then the SCLK runs continuously. With 14/$\overline{8}$/CLK at 0V, it is gated off (three-state) after serial transmission is complete.
9	DB10/SDATA	Data Bit 10/Serial Data. When 14-bit parallel data is selected, this pin provides the DB10 data output. Otherwise it is the three-state serial data output used in conjunction with SCLK and $\overline{\text{SSTRB}}$ in serial data transmission. Serial data is valid on the falling edge of SCLK, when $\overline{\text{SSTRB}}$ is low.
10–13	DB9–DB6	Three-State Data Outputs which are controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$. Their function depends on the state of the 14/$\overline{8}$/CLK and the HBEN inputs. With 14/$\overline{8}$/CLK high, they are always DB9–DB6. With 14/$\overline{8}$/CLK low, their function depends on HBEN (see Table I).
14	DGND	Digital Ground. Ground return for digital circuitry.
15–20	DB5/DB13–DB0/DB8	Three-State Data Outputs which are controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$. Their function depends on the 14/$\overline{8}$/CLK and HBEN inputs. With 14/$\overline{8}$/CLK high, they are always DB5–DB0. With 14/$\overline{8}$/CLK low or −5 V, their function is controlled by HBEN (see Table I).
21	V_{DD}	Positive Supply, +5 V ± 5%.
22	AGND	Analog Ground. Ground reference for analog circuitry.
23	C_{REF}	Decoupling point for on-chip reference. Connect 10 nF between this pin and AGND.
24	NC	No Connect.
25	REF OUT	Voltage Reference Output. The internal 3 V reference is provided at this pin. The external load capability is 500 μA.
26	V_{IN}	Analog Input. The input range is ±3 V.
27	V_{SS}	Negative Supply, −5 V ± 5%.
28	14/$\overline{8}$/CLK	Three-Function Input. Defines both the parallel and serial data formats. With this pin at +5 V, the output data is 14-bit parallel only. With this pin at 0 V, both byte and serial data are available, and the SCLK is noncontinuous. With this pin at −5 V, both byte and serial data are available and the SCLK is continuous.

AD7872 PIN FUNCTION DESCRIPTION

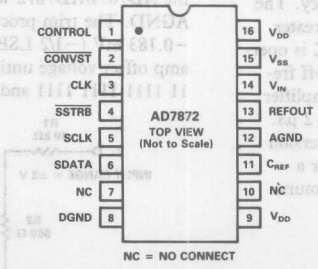
DIP No.	Mnemonic	Function
1	CONTROL	Control Input. With this pin at 0 V, the SCLK is noncontinuous. With this pin at −5 V, the SCLK is continuous.
2	$\overline{\text{CONVST}}$	Convert Start. A low to high transition on this input puts the track/hold into the hold mode. This input is asynchronous to the CLK.
3	CLK	Clock Input. An external TTL-compatible clock may be applied to this input. Alternatively, tying this pin to V_{SS}, enables the internal laser-trimmed oscillator.
4	$\overline{\text{SSTRB}}$	This is an active low three-state output which provides a framing pulse for serial data. An external 4.7 kΩ pull-up resistor is required on $\overline{\text{SSTRB}}$.
5	SCLK	Serial Clock. SCLK is the gated serial clock output which is derived from the internal or external ADC clock. If the 14/$\overline{8}$/CLK input is at −5 V, then the SCLK runs continuously. With CONTROL at 0 V, it is gated off (three-state) after serial transmission is complete. SCLK is an open-drain output and requires an external 2 kΩ pull-up resistor.
6	SDATA	Serial Data. This is the three-state serial data output used in conjunction with SCLK and $\overline{\text{SSTRB}}$ in serial data transmission. Serial data is valid on the falling edge of SCLK, when $\overline{\text{SSTRB}}$ is low. An external 4.7 kΩ pull-up resistor is required on SDATA.
7	NC	No Connect.
8	DGND	Digital Ground. Ground return for digital circuitry.
9	V_{DD}	Positive Supply for analog circuitry, +5 V ± 5%.
10	NC	No Connect.
11	C_{REF}	Decoupling point for on-chip reference. Connect 10 nF capacitor between this pin and AGND.
12	AGND	Analog Ground. Ground reference for analog circuitry.
13	REF OUT	Voltage Reference Output. The internal 3 V reference is provided at this pin. The external load capability is 500 μA.
14	V_{IN}	Analog Input. The input range is ±3 V.
15	V_{SS}	Negative Supply, −5 V ± 5%.
16	V_{DD}	Positive Supply for analog circuitry, +5 V ± 5%. Pin 16 and Pin 9 should be connected together.

PIN CONFIGURATIONS

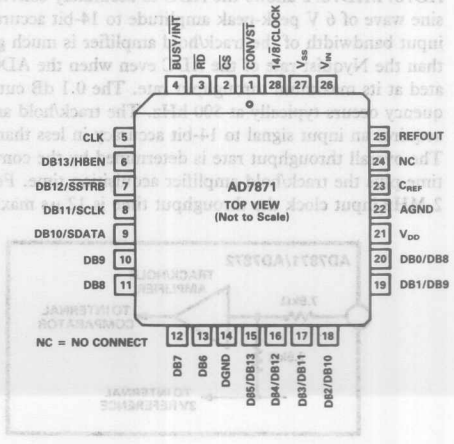
DIP



DIP, SOIC



PLCC



approximation ADC based on a fast settling voltage-output DAC, a high speed comparator and CMOS SAR, a track/hold amplifier, a 3 V buried Zener reference, a clock oscillator and control logic.

INTERNAL REFERENCE

The AD7871/AD7872 has an on-chip temperature compensated buried Zener reference which is factory trimmed to 3 V ± 10 mV. Internally it provides both the DAC reference and the dc bias required for bipolar operation. Reference noise is minimized by connecting a capacitor between C_{REF} and AGND. For specified operation this capacitor should be 10 nF. The reference output is available (REF OUT) and is capable of providing up to 500 μA to an external load.

The maximum recommended capacitance on REF OUT for normal operation is 50 pF. If the reference is required for use external to the AD7871/AD7872, it should be decoupled with a 200 Ω resistor in series with a parallel combination of a 10 μF tantalum capacitor and a 0.1 μF ceramic capacitor. These decoupling components are required to remove voltage spikes caused by the AD7871/AD7872's internal operation.

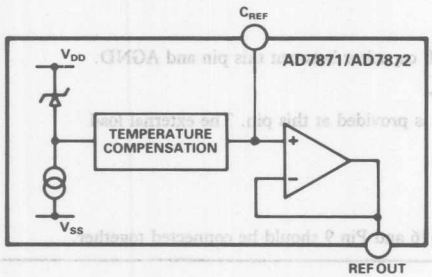


Figure 3. AD7871/AD7872 Reference Circuit

TRACK-AND-HOLD AMPLIFIER

The track-and-hold amplifier on the analog input of the AD7871/AD7872 allows the ADC to accurately convert an input sine wave of 6 V peak-peak amplitude to 14-bit accuracy. The input bandwidth of the track/hold amplifier is much greater than the Nyquist rate of the ADC even when the ADC is operated at its maximum throughput rate. The 0.1 dB cutoff frequency occurs typically at 500 kHz. The track/hold amplifier acquires an input signal to 14-bit accuracy in less than 2 μs. The overall throughput rate is determined by the conversion time plus the track/hold amplifier acquisition time. For a 2 MHz input clock the throughput time is 12 μs maximum.

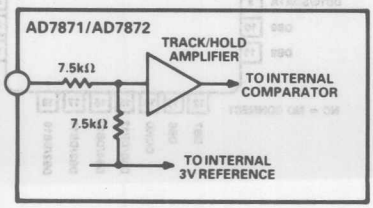


Figure 4. AD7871/AD7872 Analog Input

CONVST input is used to start conversion, then the track to hold transition occurs on the rising edge of $\overline{CONVST}$. If $\overline{CS}$ on the AD7871 starts conversion, this transition occurs on the falling edge of $\overline{CS}$.

ANALOG INPUT

Figure 4 shows the AD7871/AD7872 analog input. The analog input range is ±3 V into an input resistance of typically 15 kΩ. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS −3/2 LSBs). The output code is 2s complement binary with 1 LSB = FS/16384 = 6 V/16384 = 366 μV. The ideal input/output transfer function is shown in Figure 5.

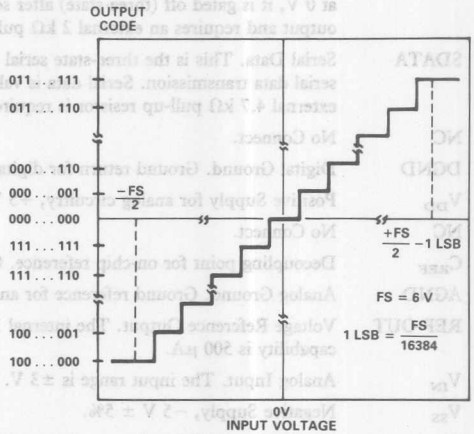


Figure 5. Bipolar Input/Output Transfer Function

BIPOLAR OFFSET AND FULL-SCALE ADJUSTMENT

When the AD7871/AD7872's offset and full-scale errors need to be adjusted, offset error must be adjusted first. This is achieved by trimming the offset of the op amp driving the analog input of the AD7871/AD7872 while the input voltage is 1/2 LSB below AGND. The trim procedure is as follows: apply a voltage of −0.183 mV (−1/2 LSB) at V_1 in Figure 6 and adjust the op-amp offset voltage until the ADC output code flickers between 11 1111 1111 1111 and 00 0000 0000 0000.

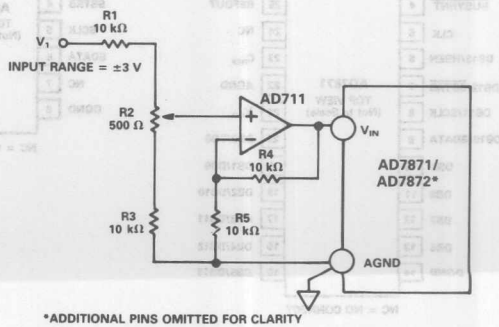


Figure 6. Bipolar Adjust Circuit

Gain error can be adjusted at either the first code transition (ADC negative full scale) or the last code transition (ADC positive full scale). The trim procedures for both cases are as follows (see Figure 6).

Positive Full-Scale Adjust

Apply a voltage of 2.9995 V (FS/2 −3/2 LSBs) at V_1 and adjust R2 until the ADC output code flickers between 01 1111 1111 1110 and 01 1111 1111 1111.

Negative Full-Scale Adjust

Apply a voltage of −2.9998 V (−FS/2+1/2 LSB) at V_1 and adjust R2 until the ADC output code flickers between 10 0000 0000 0000 and 10 0000 0000 0001.

UNIPOLAR OPERATION

A typical unipolar circuit is shown in Figure 7. The AD7871/AD7872 REF OUT is used to offset the analog input by 3 V. The analog input range is determined by the ratio of R3 to R4. The minimum range with which the circuit will work is 0 to +3 V. The resistor values are given in Figure 7 for input ranges of 0 to +5 V and 0 to +10 V. R5 and R6 are included for offset and full scale adjust only and should be omitted if adjustment is not required.

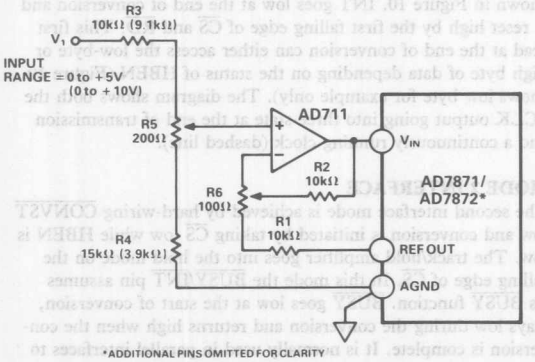


Figure 7. AD7871/AD7872 Unipolar Circuit

The ideal input/output transfer function is shown in Figure 8. The output can be converted to straight binary by inverting the MSB.

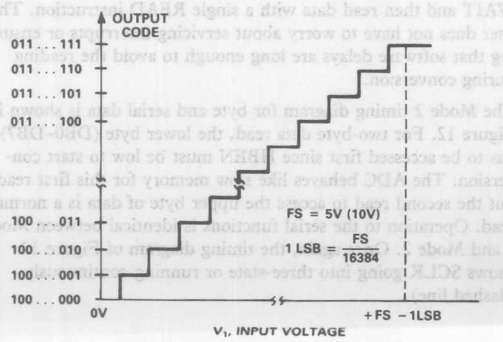


Figure 8. Unipolar Transfer Function

UNIPOLAR OFFSET AND FULL-SCALE ADJUSTMENT

When absolute accuracy is required, offset and full-scale error can be adjusted to zero. Offset must be adjusted before full-scale. This is achieved by applying an input voltage of (1/2 LSB) to V_1 and adjust R6 until the ADC output code flickers between 10 0000 0000 0000 and 10 0000 0000 0001. For full-scale adjustment apply an input voltage of (FS −3/2 LSBs) to V_1 and adjust R5 until the output code flickers between 01 1111 1111 1110 and 01 1111 1111 1111.

TIMING AND CONTROL

The conversion time for both external and internal clock can vary from 19 to 20 rising clock edges depending on the conversion start to ADC clock synchronization. If a conversion is initiated within 30 ns prior to a rising edge of the ADC clock, the conversion time will consist of 20 rising clock edges.

There are two basic operating modes for the AD7871. In the first mode (Mode 1) the $\overline{\text{CONVST}}$ line is used to start conversion and drive the track/hold into its hold mode. At the end of conversion, the track/hold returns to its tracking mode. It is intended principally for digital signal processing and other applications where precise sampling in time is required. In these applications, it is important that the signal sampling occurs at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. For these cases, the $\overline{\text{CONVST}}$ line is driven by a timer or some precise clock source.

The second mode is achieved by hard-wiring the $\overline{\text{CONVST}}$ line low. This mode (Mode 2) is intended for use in systems where the microprocessor has total control of the ADC, both initiating the conversion and reading the data. $\overline{\text{CS}}$ and $\overline{\text{RD}}$ start conversion, and the microprocessor will normally be driven into a WAIT state for the duration of conversion by $\overline{\text{BUSY/INT}}$.

The AD7872 has one operating mode only. This is Mode 1, described above, which uses $\overline{\text{CONVST}}$ to start conversion.

DATA OUTPUT FORMATS

The AD7871 offers a choice of three data output formats, one serial and two parallel. The parallel data formats include a single 14-bit parallel word for 16-bit data buses and a two-byte format for 8-bit data buses. The data format is controlled by the 14/$\overline{8}$/CLK input. A logic high on this pin selects the 14-bit parallel output format only. A logic low or −5 V applied to this pin allows the user access to either serial or byte formatted data. Three of the pins previously assigned to the four MSBs in parallel form are now used for serial communications while the fourth pin becomes a control input for the byte-formatted data. The three possible data output formats can be selected in either of the modes of operation.

The AD7872 is a serial output device only. The serial data format is exactly the same as the AD7871.

Parallel Output Format

The two parallel formats available on the AD7871 are a 14-bit wide data word and a two-byte data word. In the first, all 14 bits of data are available at the same time on DB13 (MSB) through DB0 (LSB). In the second, two reads are required to access the data. When this data format is selected, the DB13/HBEN pin assumes the HBEN function. HBEN selects which byte of data is to be read from the AD7871. When HBEN is low, the lower 8 bits of data are placed on the data bus during a read operation; with HBEN high, the upper 6 bits

of the 14-bit word are placed on the data bus. These 6 bits are right justified and thereby occupy the lower six bits of the byte while the upper two bits are zeros.

Serial Output Format

Serial data is available on the AD7871 when the 14/$\overline{8}$/CLK input is at 0 V or −5 V and in this case the DB12/$\overline{\text{SSTRB}}$, DB11/SCLK and DB10/SDATA pins assume their serial functions. The AD7872 is a serial output device only. The serial function on both devices is identical. Serial data is available during conversion with a word length of 16 bits; 2 leading zeros, followed by the 14-bit conversion result starting with the MSB. The data is synchronized to the serial clock output (SCLK) and is framed by the serial strobe ($\overline{\text{SSTRB}}$). Data is clocked out on a low to high transition of the serial clock and is valid on the falling edge of this clock while the $\overline{\text{SSTRB}}$ output is low. $\overline{\text{SSTRB}}$ goes low at the start of conversion and the first serial data bit (which is the first leading zero) is valid on the first falling edge of SCLK. All the serial lines are open-drain outputs and require external pull-up resistors.

The serial clock out is derived from the ADC master clock source which may be internal or external. Normally, SCLK is required during the serial transmission only. In these cases it can be shut down (i.e., placed into three-state) at the end of conversion to allow multiple ADCs to share a common serial bus. However, some serial systems (e.g., TMS32020) require a serial clock which runs continuously. Both options are available on the AD7871 and AD7872. With the 14/$\overline{8}$/CLK input on the AD7871 at −5 V, the serial clock (SCLK) runs continuously; when 14/$\overline{8}$/CLK is at 0 V, SCLK goes into three-state at the end of transmission. The CONTROL pin on the AD7872 performs the same function. When this is at 0 V, SCLK is noncontinuous and when it is at −5 V, SCLK is continuous.

The SCLK, SDATA and $\overline{\text{SSTRB}}$ lines are open-drain outputs. If these are required to drive capacitive loads in excess of 35 pF, buffering is recommended.

MODE 1 INTERFACE

Conversion is initiated by a low going pulse on the $\overline{\text{CONVST}}$ input. The rising edge of this $\overline{\text{CONVST}}$ pulse starts conversion and drives the track/hold amplifier into its hold mode. The $\overline{\text{BUSY}}$/$\overline{\text{INT}}$ status output assumes its $\overline{\text{INT}}$ function in this mode. $\overline{\text{INT}}$ is normally high and goes low at the end of conversion. This $\overline{\text{INT}}$ line can be used to interrupt the microprocessor. A read operation to the AD7871 accesses the data and the $\overline{\text{INT}}$ line is reset high on the falling edge of $\overline{\text{CS}}$ and $\overline{\text{RD}}$. The $\overline{\text{CONVST}}$ input must be high when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are brought low for the AD7871 to operate correctly in this mode. It is important, especially in systems where the conversion start ($\overline{\text{CONVST}}$) pulse is asynchronous to the microprocessor, to ensure that a parallel or byte data read is not attempted during a conversion. Trying to read data during a conversion can cause errors to the conversion in progress. Avoid pulsing the $\overline{\text{CONVST}}$ line a second time before conversion end since it can cause errors in the conversion result. In applications where precise sampling is not critical, the $\overline{\text{CONVST}}$ pulse can be generated from microprocessor $\overline{\text{WR}}$ line OR-gated with the AD7871 $\overline{\text{CS}}$ input. In some applications, depending on power supply turn-on time, the AD7871/AD7872 may perform a conversion on power-up. In this case, the $\overline{\text{INT}}$ line on the AD7871 will power up low, and a dummy read to the device will be required to reset the $\overline{\text{INT}}$ line before starting conversion.

Figure 9 shows the Mode 1 timing diagram for a 14-bit parallel data output format (14/$\overline{8}$/CLK = +5 V). A read to the AD7871 at the end of conversion accesses all 14 bits of data at the same time. Serial data is not available for this data output format.

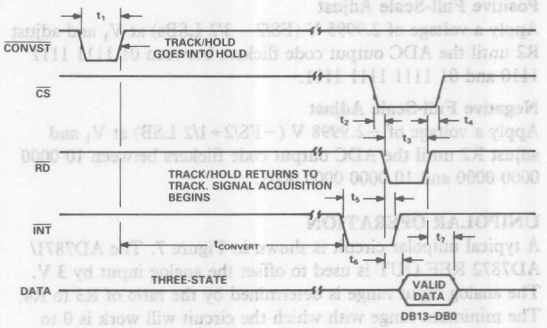


Figure 9. Mode 1 Timing Diagram, 14-Bit Parallel Read

The Mode 1 function timing diagram for byte and serial data is shown in Figure 10. $\overline{\text{INT}}$ goes low at the end of conversion and is reset high by the first falling edge of $\overline{\text{CS}}$ and $\overline{\text{RD}}$. This first read at the end of conversion can either access the low-byte or high byte of data depending on the status of HBEN (Figure 10 shows low byte for example only). The diagram shows both the SCLK output going into three-state at the end of transmission and a continuously running clock (dashed line).

MODE 2 INTERFACE

The second interface mode is achieved by hard-wiring $\overline{\text{CONVST}}$ low and conversion is initiated by taking $\overline{\text{CS}}$ low while HBEN is low. The track/hold amplifier goes into the hold mode on the falling edge of $\overline{\text{CS}}$. In this mode the $\overline{\text{BUSY}}$/$\overline{\text{INT}}$ pin assumes its $\overline{\text{BUSY}}$ function. $\overline{\text{BUSY}}$ goes low at the start of conversion, stays low during the conversion and returns high when the conversion is complete. It is normally used in parallel interfaces to drive the microprocessor into a WAIT state for the duration of conversion.

Figure 11 shows the Mode 2 timing diagram for the 14-bit parallel data output format (14/$\overline{8}$/CLK = +5 V). In this case the ADC behaves like slow memory. The major advantage of this interface is that it allows the microprocessor to start conversion, WAIT and then read data with a single READ instruction. The user does not have to worry about servicing interrupts or ensuring that software delays are long enough to avoid the reading during conversion.

The Mode 2 timing diagram for byte and serial data is shown in Figure 12. For two-byte data read, the lower byte (DB0–DB7) has to be accessed first since HBEN must be low to start conversion. The ADC behaves like slow memory for this first read, but the second read to access the upper byte of data is a normal read. Operation to the serial functions is identical between Mode 1 and Mode 2. Once again, the timing diagram of Figure 12 shows SCLK going into three-state or running continuously (dashed line).

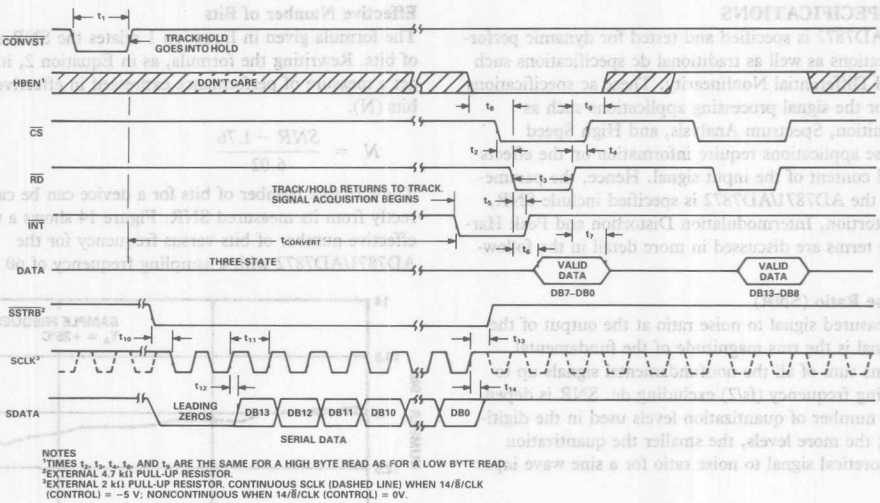


Figure 10. Mode 1 Timing Diagram, Byte or Serial Read

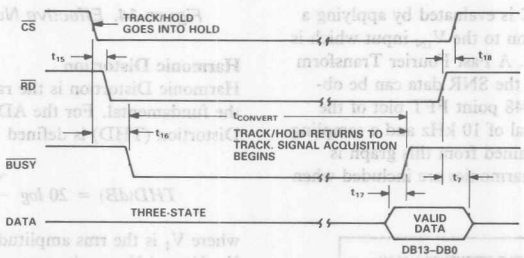


Figure 11. Mode 2 Timing Diagram, 14-Bit Parallel Read

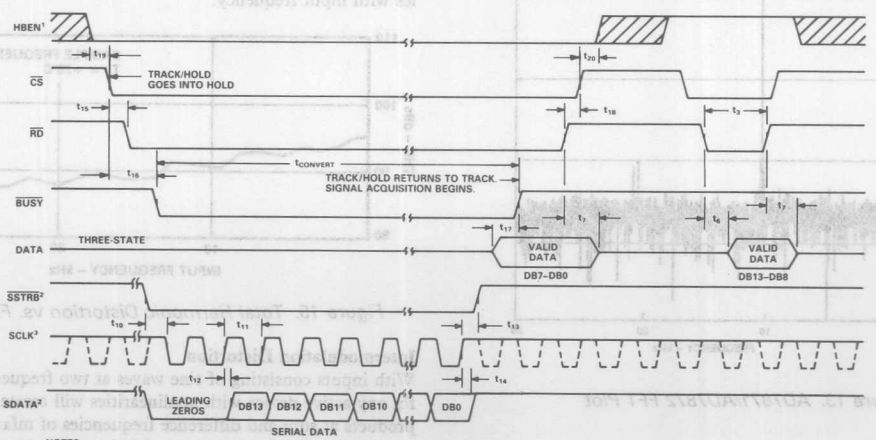


Figure 12. Mode 2 Timing Diagram, Byte or Serial Read

DYNAMIC SPECIFICATIONS

The AD7871/AD7872 is specified and tested for dynamic performance specifications as well as traditional dc specifications such as Integral and Differential Nonlinearity. These ac specifications are required for the signal processing applications such as Speech Recognition, Spectrum Analysis, and High Speed Modems. These applications require information on the effects on the spectral content of the input signal. Hence, the parameters for which the AD7871/AD7872 is specified include SNR, Harmonic Distortion, Intermodulation Distortion and Peak Harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal to noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (fs/2) excluding dc. SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to noise ratio for a sine wave input is given by:

$$SNR(dB) = (6.02N + 1.76) \quad (1)$$

where N is the number of bits in the ADC. Thus for an ideal 14-bit converter, SNR = 86 dB.

The output spectrum from the ADC is evaluated by applying a sine wave signal of very low distortion to the V_{IN} input which is sampled at an 83 kHz sampling rate. A Fast Fourier Transform (FFT) plot is generated from which the SNR data can be obtained. Figure 13 shows a typical 2048 point FFT plot of the AD7871/AD7872 with an input signal of 10 kHz and a sampling frequency of 83 kHz. The SNR obtained from this graph is 80 dB. It should be noted that the harmonics are included when calculating the SNR.

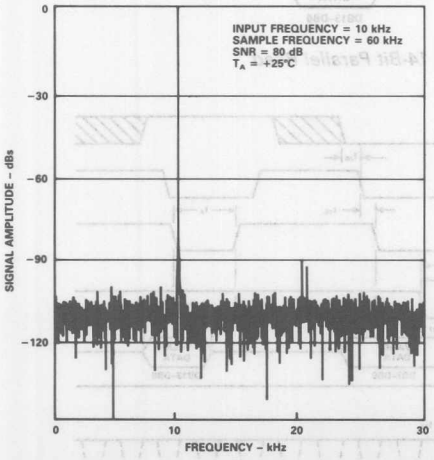


Figure 13. AD7871/AD7872 FFT Plot

Effective Number of Bits

The formula given in Equation 1 relates the SNR to the number of bits. Rewriting the formula, as in Equation 2, it is possible to get a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \quad (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR. Figure 14 shows a typical plot of effective number of bits versus frequency for the AD7871/AD7872 with a sampling frequency of 60 kHz.

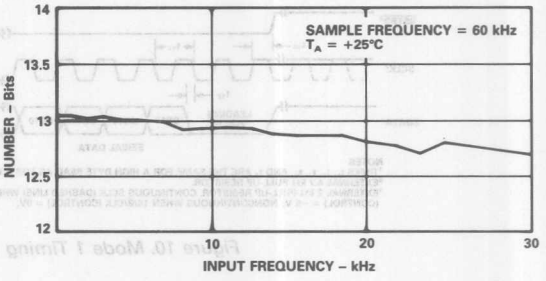


Figure 14. Effective Number of Bits vs. Frequency

Harmonic Distortion

Harmonic Distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7871/AD7872, Total Harmonic Distortion (THD) is defined as

$$THD(dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonic. The THD is also derived from the FFT plot of the ADC output spectrum. Figure 15 shows how the THD varies with input frequency.

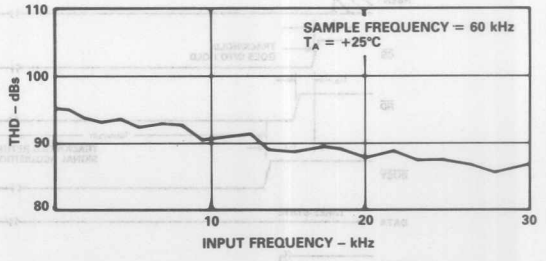


Figure 15. Total Harmonic Distortion vs. Frequency

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa±nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m or n are equal to zero. For example, the second order terms include (fa+fb) and (fa−fb), while the third order terms include (2fa+fb), (2fa−fb), (fa+2fb) and (fa−2fb).

Using the CCIF standard where two input frequencies near the top end of the input bandwidth are used, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs. In this case, the input consists of two, equal amplitude, low distortion sine waves. Figure 16 shows a typical IMD plot for the AD7871/AD7872.

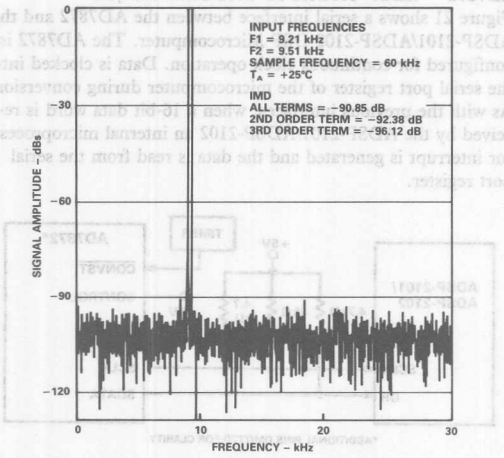


Figure 16. AD7871/AD7872 IMD Plot

Peak Harmonic or Spurious Noise

Peak Harmonic or Spurious Noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to fs/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor peak will be a noise peak.

MICROPROCESSOR INTERFACE

The AD7871 and AD7872 have a wide variety of interfacing options. The AD7871 offers two operating modes and three data-output formats, while the AD7872 is a dedicated serial output device. The fast data access times on the parallel modes of the AD7871 allow interfacing to the very fast DSPs. The serial mode on both the AD7871 and AD7872 is compatible with the serial port structures on all the popular DSPs.

Parallel Read Interfacing

Figures 17 and 18 show interfaces to the ADSP-2100 and the TMS32020/C25 DSP processors. The AD7871 is operating in Mode 1, parallel read for both interfaces. An external timer controls conversion start asynchronously to the microprocessor. At the end of each conversion the ADC $\overline{\text{BUSY/INT}}$ interrupts the microprocessor and the conversion result is read from the ADC with the following instruction:

ADSP-2100 MR0 = DM(ADC)

TMS32020/C25: IN D,ADC

MR0 = ADSP-2100 MR0 Register

D = Data Memory Address

ADC = AD7871 Address

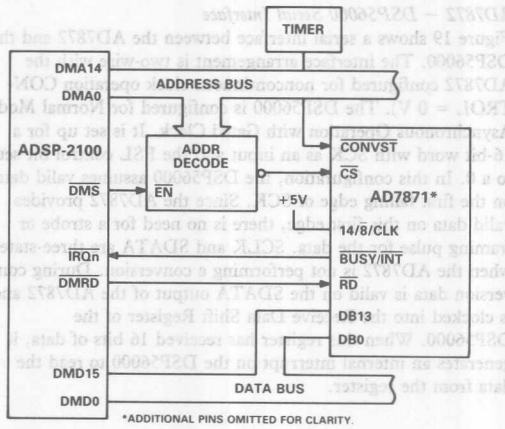


Figure 17. AD7871 to ADSP-2100 Parallel Interface

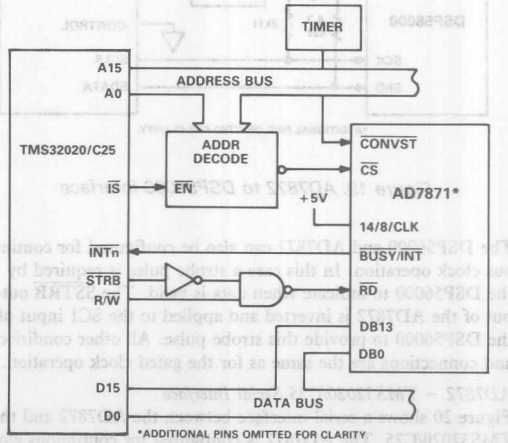


Figure 18. AD7871 to TMS32020/C25 Interface

Some applications may require that conversions be initiated by the microprocessor rather than an external timer. One option is to decode the AD7871 $\overline{\text{CONVST}}$ from the address bus so that a write operation to the ADC starts a conversion. Data is read at the end of conversion as described earlier. Note, a read operation must not be attempted during conversion.

face. The diagrams that follow show the AD7872 interfaces only but the AD7871 could just as easily be used in these circuits. Figures 19, 20 and 21 show the AD7872 connected to three popular DSPs. In all three interfaces, $\overline{\text{CONVST}}$ is used to start conversion since this does not activate the parallel bus. Thus, the microprocessor can continue to use its parallel bus regardless of the state of the AD7872. The interfaces show a timer driving the $\overline{\text{CONVST}}$ input but this could be generated from a decoded address if required.

AD7872 – DSP56000 Serial Interface

Figure 19 shows a serial interface between the AD7872 and the DSP56000. The interface arrangement is two-wire with the AD7872 configured for noncontinuous clock operation CONTROL = 0 V). The DSP56000 is configured for Normal Mode Asynchronous Operation with Gated Clock. It is set up for a 16-bit word with SCK as an input and the FSL control bit set to a 0. In this configuration, the DSP56000 assumes valid data on the first falling edge of SCK. Since the AD7872 provides valid data on this first edge, there is no need for a strobe or framing pulse for the data. SCLK and SDATA are three-stated when the AD7872 is not performing a conversion. During conversion data is valid on the SDATA output of the AD7872 and is clocked into the Receive Data Shift Register of the DSP56000. When this register has received 16 bits of data, it generates an internal interrupt on the DSP56000 to read the data from the register.

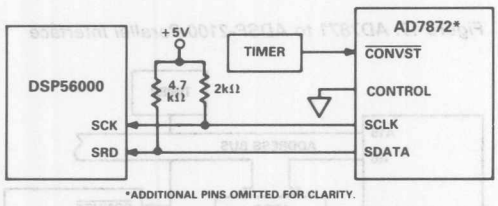


Figure 19. AD7872 to DSP56000 Interface

The DSP56000 and AD7872 can also be configured for continuous clock operation. In this case a strobe pulse is required by the DSP56000 to indicate when data is valid. The $\overline{\text{SSTRB}}$ output of the AD7872 is inverted and applied to the SC1 input of the DSP56000 to provide this strobe pulse. All other conditions and connections are the same as for the gated clock operation.

AD7872 – TMS32020/C25 Serial Interface

Figure 20 shows a serial interface between the AD7872 and the TMS32020/C25. The AD7872 is configured for continuous clock operation. Note, the ADC will not interface correctly to the TMS32020/C25 if it is configured for a noncontinuous clock. Data is clocked into the Data Receive Register (DRR) of the TMS32020/C25 during conversion. As with the previous interfaces, when a 16-bit word is received by the DSP it generates an internal interrupt to read the data from the DRR.

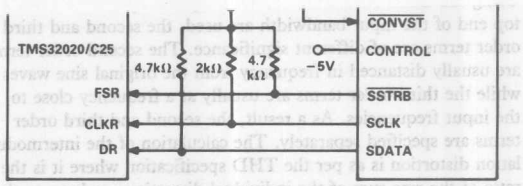


Figure 20. AD7872 to TMS32020/C25 Interface

AD7872 – ADSP-2101/ADSP-2102 Serial Interface

Figure 21 shows a serial interface between the AD7872 and the ADSP-2101/ADSP-2102 DSP Microcomputer. The AD7872 is configured for continuous clock operation. Data is clocked into the serial port register of the microcomputer during conversion. As with the previous interfaces, when a 16-bit data word is received by the ADSP-2101/ADSP-2102 an internal microprocessor interrupt is generated and the data is read from the serial port register.

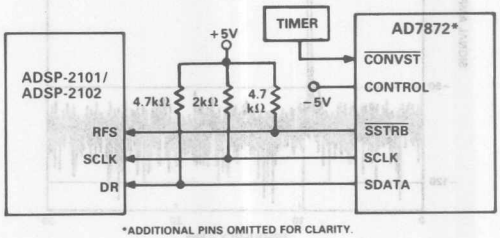


Figure 21. AD7872 to ADSP-2101/ADSP-2101 Serial Interface

STAND-ALONE OPERATION

The AD7871 can be used in its Mode 2, parallel mode for stand-alone operation. In this case, conversion is initiated with a pulse to the $\overline{\text{CS}}$ input. This pulse must be longer than the conversion time of the ADC. The $\overline{\text{BUSY}}$ output is used to drive the $\overline{\text{RD}}$ input. Data is latched from the AD7871 DB0–DB11 outputs to an external latch on the rising edge of $\overline{\text{BUSY}}$.

APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the circuit design itself in achieving high speed A/D performance. The AD7871/AD7872 is required to make bit decisions on an LSB size of 366 μV. Thus, the designer has to be conscious of noise both in the ADC itself and in the preceding analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any ADC, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run a digital track alongside an analog signal track. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground at the AD7871/AD7872 AGND pin or as close as possible to the AD7871/AD7872. Connect all other grounds and the AD7871/AD7872 DGND to this single analog ground point. Do not connect any other digital grounds to this analog ground point.

Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise. The circuit layout of Figures 26 and 27 have both analog and digital ground planes which are kept separated and only joined together at the AD7871/AD7872 AGND pin.

NOISE

Keep the input signal leads to V_{IN} and signal return leads from AGND as short as possible to minimize input noise coupling. In applications where this is not possible, use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

DATA ACQUISITION BOARD

Figure 24 shows the AD7871/AD7872 in a data acquisition circuit. The corresponding printed circuit board (PCB) layout has three interface ports: one serial and two parallel. Note that the AD7871/AD7872 serial lines are buffered by a 74HC244. This allows long lines with large capacitive loads to be driven. One of the parallel ports is directly compatible with the ADSP-2100 evaluation board expansion connector.

The only additional component required for a full data acquisition system is an anti-aliasing filter. There is a component grid provided near the analog input on the PCB which may be used for such a filter or any other input conditioning circuitry. To facilitate this option, there is a shorting plug (labelled LK1 on the PCB) on the analog input track. If this shorting plug is used, the analog input connects to the buffer amplifier driving the AD7871/AD7872; if this shorting plug is omitted, a wire link can be used to connect the analog input to the PCB component grid.

INTERFACE CONNECTIONS

There are two parallel connectors labeled SKT4 and SKT6 and one serial connector labeled SKT5. A shorting plug option (LK3 in Figure 24) configures the ADC for the appropriate interface.

SKT6 is a 96-contact (3-row) Eurocard connector which is directly compatible with the ADSP-2100 Evaluation Board Prototype Expansion Connector. The expansion connector on the ADSP-2100 has eight decoded chip enable outputs labeled ECE1 to ECE8. ECE6 is used to drive the AD7871 $\overline{CS}$ input on the board. To avoid selecting the on-board RAM sockets at the same time, LK6 on the ADSP-2100 board must be removed. In addition, the ADSP-2100 expansion connector has four interrupts labelled EIRQ0 to EIRQ3. The AD7871 $\overline{BUSY/INT}$ output connects to EIRQ0. There is a single wait state generator connected to EDMACK to allow the AD7871 to interface to the faster versions of the ADSP-2100.

SKT4 is a 26-way (2-row) IDC connector. This contains the same signal contacts as SKT6 except for EDMACK which is connected to SKT6 only. It also contains decoded R/$\overline{W}$ and $\overline{STRB}$ inputs which are necessary for TMS32020 interfacing.

SKT5 is a 5-way D-type connector which is meant for serial interfacing only. An inverted DB11/SCLK output is also provided on this connector for systems which accept data on a rising clock edge.

SKT1, SKT2 and SKT3 are three BNC connectors which provide connections for the analog input, the $\overline{CONVST}$ input and an external clock.

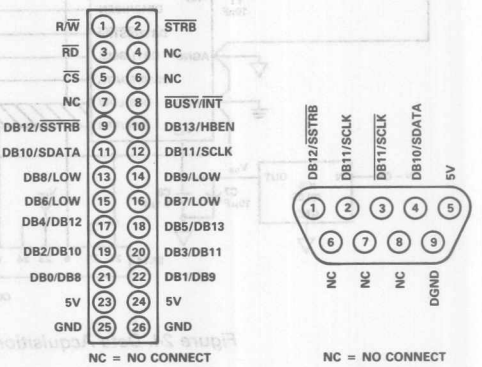


Figure 22. SKT4 Pinout *Figure 23. SKT5 Pinout*

POWER SUPPLY CONNECTIONS

The PCB requires two analog power supplies and one 5 V logic supply. The analog supplies are labelled V+ and V−, and the range for both supplies is 12 V to 15 V. Connection to the 5 V digital supply is made through any of the connectors SKT4 to SKT6. The ±5 V supply required by the AD7871 and AD7872 is generated from voltage regulators on the V+ and V− power supplies input (IC6 and IC7 in Figure 24).

SHORTING PLUG OPTIONS

There are seven shorting plug options which must be set before using the board. These are outlined below:

LK1 Connects the analog input to a buffer amplifier. The analog input may also be connected to a component grid for signal conditioning.
LK2 Selects either the AD7871/AD7872 internal clock or an external clock source.
LK3 Configures the AD7871 14/$\overline{8}$/CLK input for the appropriate serial or parallel interface.
LK4 Connects the AD7871 $\overline{RD}$ input directly to the two parallel connectors or to a decoded $\overline{STRB}$ and R/$\overline{W}$ input.
LK5 Connects the pull-up resistor R3 to $\overline{SSTRB}$.
LK6 Connects the pull-up resistor R4 to SCLK.
LK7 Connects the pull-up resistor R5 to SDATA.

Note that LK5 to LK7 should be removed for parallel interfacing.

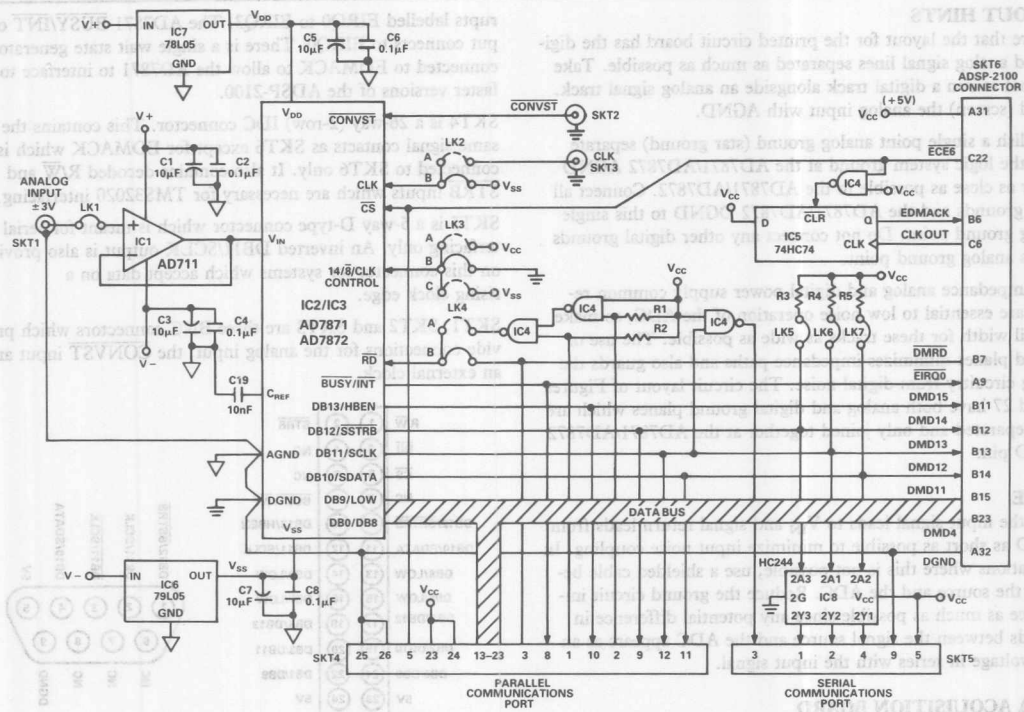


Figure 24. Data Acquisition Circuit Using the AD7871/AD7872

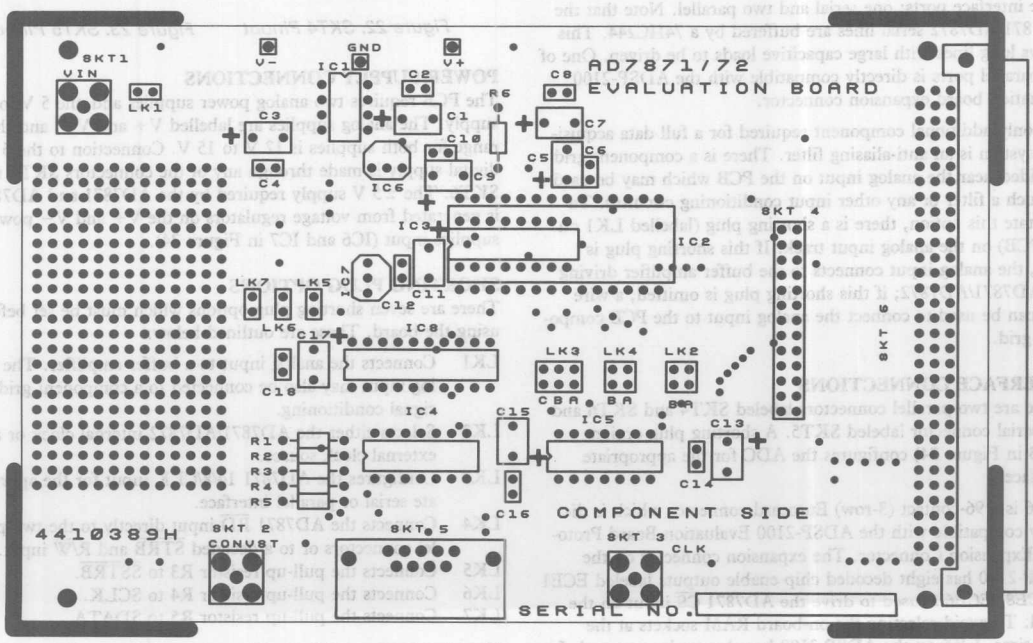


Figure 25. PCB Silkscreen for Figure 24

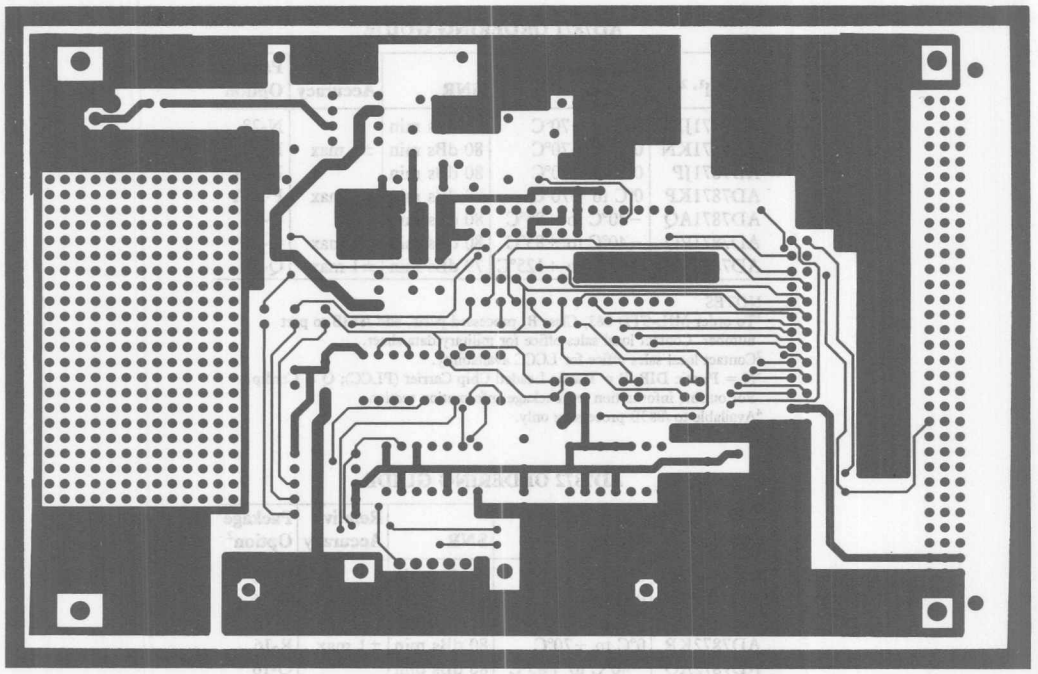


Figure 26. PCB Component Side Layout for Figure 24

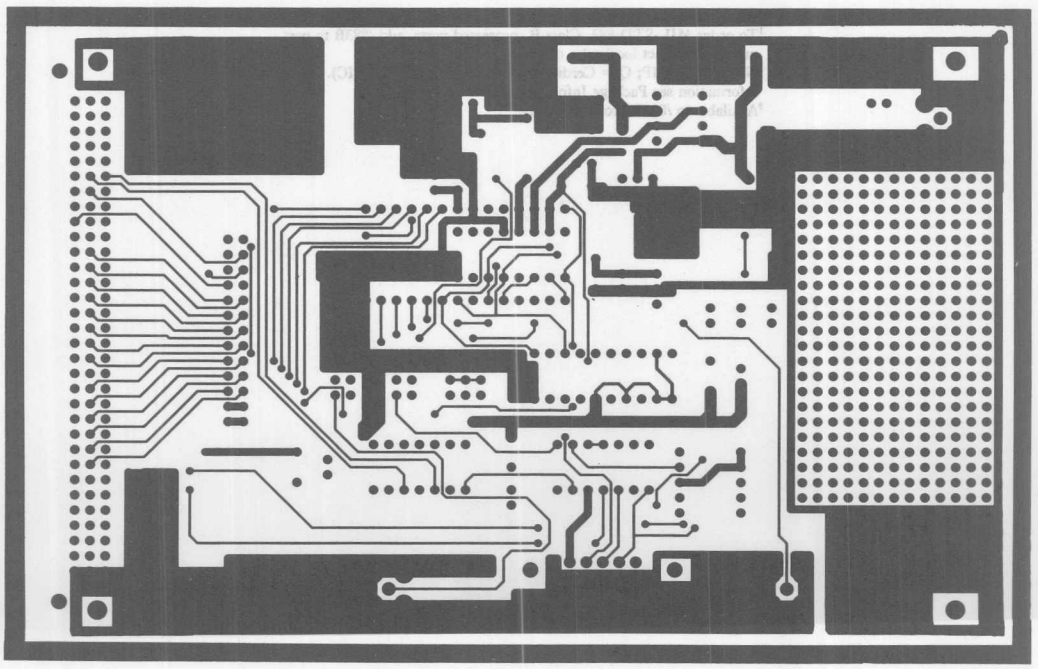


Figure 27. PCB Solder Side Layout for Figure 24

AD7871 ORDERING GUIDE

Model[1, 2]	Temperature Range	SNR	Relative Accuracy	Package Option[3]
AD7871JN	0°C to +70°C	80 dBs min		N-28
AD7871KN	0°C to +70°C	80 dBs min	±1 max	N-28
AD7871JP	0°C to +70°C	80 dBs min		P-28A
AD7871KP	0°C to +70°C	80 dBs min	±1 max	P-28A
AD7871AQ	−40°C to +85°C	80 dBs min		Q-28
AD7871BQ	−40°C to +85°C	80 dBs min	±1 max	Q-28
AD7871TQ[4]	−55°C to +125°C	79 dBs min	±1 max	Q-28

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact local sales office for military data sheet.
[2]Contact local sales office for LCCC availability.
[3]N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information section.
[4]Available to /883B processing only.

AD7872 ORDERING GUIDE

Model[1]	Temperature Range	SNR	Relative Accuracy	Package Option[2]
AD7872JN	0°C to +70°C	80 dBs min		N-16
AD7872KN	0°C to +70°C	80 dBs min	±1 max	N-16
AD7872JR	0°C to +70°C	80 dBs min		R-16
AD7872KR	0°C to +70°C	80 dBs min	±1 max	R-16
AD7872AQ	−40°C to +85°C	80 dBs min		Q-16
AD7872BQ	−40°C to +85°C	80 dBs min	±1 max	Q-16
AD7872TQ[3]	−55°C to +125°C	79 dBs min	±1 max	Q-16

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact local sales office for military data sheet.
[2]N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.
[3]Available to /883B processing only.

LC²MOS 4-Channel, 12-Bit Simultaneous Sampling Data Acquisition System

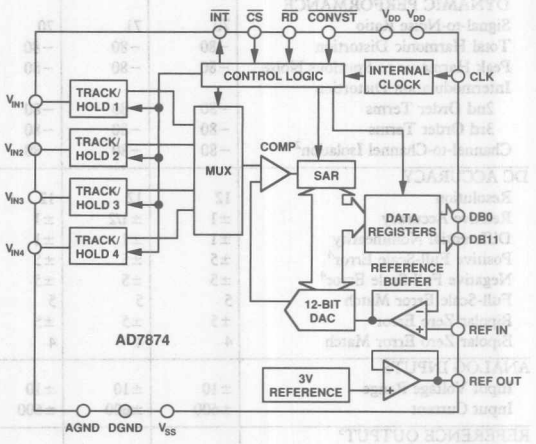
AD7874

2

FEATURES
- Four On-Chip Track/Hold Amplifiers
- Simultaneous Sampling of 4 Channels
- Fast 12-Bit ADC with 8 μs Conversion Time/Channel
- 29 kHz Sample Rate for All Four Channels
- On-Chip Reference
- ±10 V Input Range
- ±5 V Supplies

APPLICATIONS
- Sonar
- Motor Controllers
- Adaptive Filters
- Digital Signal Processing

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7874 is a four-channel simultaneous sampling, 12-bit data acquisition system. The part contains a high speed 12-bit ADC, on-chip reference, on-chip clock and four track/hold amplifiers. This latter feature allows the four input channels to be sampled simultaneously, thus preserving the relative phase information of the four input channels, which is not possible if all four channels share a single track/hold amplifier. This makes the AD7874 ideal for applications such as phased-array sonar and ac motor controllers where the relative phase information is important.

The aperture delay of the four track/hold amplifiers is small and specified with minimum and maximum limits. This allows several AD7874s to sample multiple input channels simultaneously without incurring phase errors between signals connected to several devices. A reference output/reference input facility also allows several AD7874s to be driven from the same reference source.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7874 is also fully specified for dynamic performance parameters including distortion and signal-to-noise ratio.

The AD7874 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low-power CMOS logic. The part is available in a 28-pin, 0.6" wide, plastic or hermetic dual-in-line package (DIP), in a 28-terminal leadless ceramic chip carrier (LCCC) and in a 28-pin SOIC.

PRODUCT HIGHLIGHTS

1. Simultaneous Sampling of Four Input Channels.
   Four input channels, each with its own track/hold amplifier, allow simultaneous sampling of input signals. Track/hold acquisition time is 2 μs, and the conversion time per channel is 8 μs, allowing 29 kHz sample rate for all four channels.
2. Tight Aperture Delay Matching.
   The aperture delay for each channel is small and the aperture delay matching between the four channels is less than 4 ns. Additionally, the aperture delay specification has upper and lower limits allowing multiple AD7874s to sample more than four channels.
3. Fast Microprocessor Interface.
   The high speed digital interface of the AD7874 allows direct connection to all modern 16-bit microprocessors and digital signal processors.

AD7874—SPECIFICATIONS

(V_{DD} = +5 V, V_{SS} = −5 V, AGND = DGND = 0 V, REF IN = +3 V, f_{CLK} = 2.5 MHz external. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	A Version	B Version	S Version	Units	Test Conditions/Comments
SAMPLE-AND-HOLD					
Acquisition Time[2] to 0.01%	2	2	2	μs max	
Droop Rate[2, 3]	1	1	2	mV/ms max	
−3 dB Small Signal Bandwidth[3]	500	500	500	kHz typ	V_{IN} = 500 mV p–p
Aperture Delay[2]	0	0	0	ns min	
	40	40	40	ns max	
Aperture Jitter[2, 3]	200	200	200	ps typ	
Aperture Delay Matching[2]	4	4	4	ns max	
SAMPLE-AND-HOLD AND ADC DYNAMIC PERFORMANCE					
Signal-to-Noise Ratio	70	71	70	dB min	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 29 kHz
Total Harmonic Distortion	−80	−80	−80	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 29 kHz
Peak Harmonic or Spurious Noise	−80	−80	−80	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 29 kHz
Intermodulation Distortion					fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 29 kHz
2nd Order Terms	−80	−80	−80	dB max	
3rd Order Terms	−80	−80	−80	dB max	
Channel-to-Channel Isolation[2]	−80	−80	−80	dB max	
DC ACCURACY					
Resolution	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	LSB max	No Missing Codes Guaranteed
Positive Full-Scale Error[4]	±5	±5	±5	LSB max	Any Channel
Negative Full-Scale Error[4]	±5	±5	±5	LSB max	Any Channel
Full-Scale Error Match	5	5	5	LSB max	Between Channels
Bipolar Zero Error	±5	±5	±5	LSB max	Any Channel
Bipolar Zero Error Match	4	4	4	LSB max	Between Channels
ANALOG INPUTS					
Input Voltage Range	±10	±10	±10	Volts	
Input Current	±600	±600	±600	μA max	
REFERENCE OUTPUT[5]					
REF OUT	3	3	3	V nom	
REF OUT Error @ +25°C	±0.33	±0.33	±0.33	% max	
T_{min} to T_{max}	±1	±1	±1	% max	
REF OUT Temperature Coefficient	±35	±35	±35	ppm/°C typ	
Reference Load Change	±1	±1	±2	mV max	Reference Load Current Change (0–500 μA)
					Reference Load Should Not Be Changed During Conversion
REFERENCE INPUT					
Input Voltage Range	2.85/3.15	2.85/3.15	2.85/3.15	V min/V max	3 V ± 5%
Input Current	±1	±1	±1	μA max	
Input Capacitance[3]	10	10	10	pF max	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ±5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ±5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[3]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	V_{DD} = 5 V ±5%; I_{SOURCE} = 40 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	V_{DD} = 5 V ±5%; I_{SINK} = 1.6 mA
DB0–DB11					
Floating-State Leakage Current	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Floating-State Output Capacitance	10	10	10	pF max	
Output Coding	2s COMPLEMENT				
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	18	18	18	mA max	$\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = +5 V; Typically 12 mA
I_{SS}	12	12	12	mA max	$\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = +5 V; Typically 8 mA
Power Dissipation	150	150	150	mW max	$\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = +5 V; Typically 100 mW

NOTES

[1]Temperature ranges are as follows: A, B Versions: −40°C to +85°C; S Version: −55°C to +125°C.

[2]See Terminology.

[3]Sample tested @ +25°C to ensure compliance.

[4]Measured with respect to the REF IN voltage and includes bipolar offset error.

[5]For capacitive loads greater than 50 pF a series resistor is required.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V, f_{CLK} = 2.5 MHz external unless otherwise stated.)

Parameter	A, B Versions	S Version	Units	Conditions/Comments
t_1	50	50	ns min	$\overline{CONVST}$ Pulse Width
t_2	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_3	**60**	**70**	ns min	$\overline{RD}$ Pulse Width
t_4	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_5	60	60	ns max	$\overline{RD}$ to $\overline{INT}$ Delay
t_6[2]	**57**	**70**	ns max	Data Access Time after $\overline{RD}$
t_7[3]	5	5	ns min	Bus Relinquish Time after $\overline{RD}$
	45	**50**	ns max	
t_8	130	150	ns min	Delay Time between Reads
t_{CONV}	31	31	µs min	$\overline{CONVST}$ to $\overline{INT}$, External Clock
	32.5	32.5	µs max	$\overline{CONVST}$ to $\overline{INT}$, External Clock
	31	31	µs min	$\overline{CONVST}$ to $\overline{INT}$, Internal Clock
	35	35	µs max	$\overline{CONVST}$ to $\overline{INT}$, Internal Clock
t_{CLK}	10	10	µs max	Minimum Input Clock Period

NOTES

[1]Timing Specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[2]t_6 is measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[3]t_7 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_7, quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

Specifications subject to change without notice.

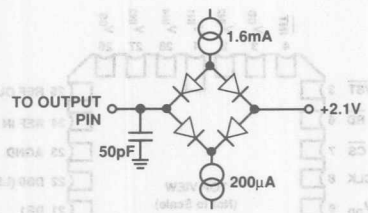


Figure 1. Load Circuit for Access Time

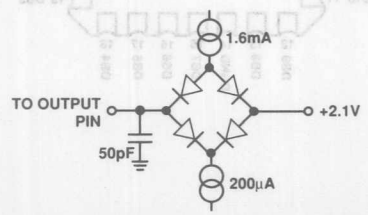


Figure 2. Load Circuit for Bus Relinquish Time

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	−0.3 V to +7 V
V_{DD} to DGND	−0.3 V to +7 V
V_{SS} to AGND	+0.3 V to −7 V
AGND to DGND	−0.3 V to V_{DD}+0.3 V
V_{IN} to AGND	−15 V to +15 V
REF OUT to AGND	0 V to V_{DD}
Digital Inputs to DGND	−0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND	−0.3 V to V_{DD} +0.3 V
Operating Temperature Range	
Commercial (A, B Versions)	−40°C to +85°C
Extended (S Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C
Power Dissipation (Any Package) to +75°C	1,000 mW
Derates above +75°C by	10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



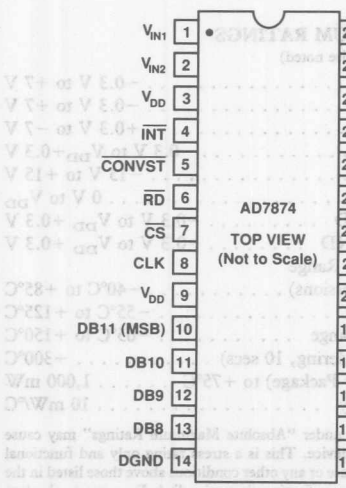
ORDERING GUIDE

Model[1]	Temperature Range	SNR (dBs)	Relative Accuracy (LSB)	Package Option[2]
AD7874AN	−40°C to +85°C	70 min	±1 max	N-28
AD7874BN	−40°C to +85°C	72 min	±1/2 max	N-28
AD7874AR	−40°C to +85°C	70 min	±1 max	R-28
AD7874BR	−40°C to +85°C	72 min	±1/2 max	R-28
AD7874AQ	−40°C to +85°C	70 min	±1 max	Q-28
AD7874BQ	−40°C to +85°C	72 min	±1/2 max	Q-28
AD7874SQ[3]	−55°C to +125°C	70 min	±1 max	Q-28
AD7874SE[3]	−55°C to +125°C	70 min	±1 max	E-28A

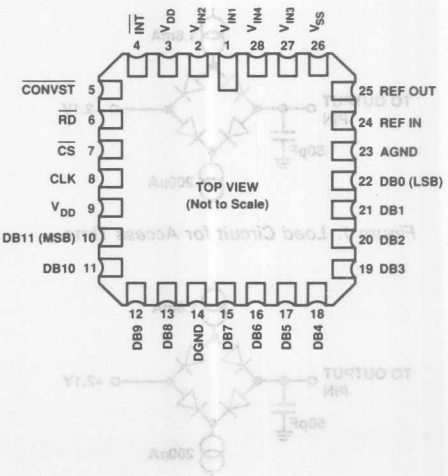
NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact our local sales office for military data sheet and availability.
[2]E = Leaded Ceramic Chip Carrier; N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.
[3]Available to /883B processing only.

PIN CONFIGURATIONS

DIP and SOIC



LCCC



PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	V_{IN1}	Analog Input Channel 1. This is the first of the four input channels to be converted in a conversion cycle. Analog input voltage range is ±10 V.
2	V_{IN2}	Analog Input Channel 2. Analog input voltage range is ±10 V.
3	V_{DD}	Positive supply voltage, +5 V ± 5%. This pin should be decoupled to AGND.
4	$\overline{INT}$	Interrupt. Active low logic output indicating converter status. See Figure 7.
5	$\overline{CONVST}$	Convert Start. Logic Input. A low to high transition on this input puts the track/hold into its hold mode and starts conversion. The four channels are converted sequentially, Channel 1 to Channel 4. The $\overline{CONVST}$ input is asynchronous to CLK and independent of $\overline{CS}$ and $\overline{RD}$.
6	$\overline{RD}$	Read. Active low logic input. This input is used in conjunction with $\overline{CS}$ low to enable the data outputs. Four successive reads after a conversion will read the data from the four channels in the sequence, Channel 1, 2, 3, 4.
7	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active.
8	CLK	Clock Input. An external TTL-compatible clock may be applied to this input pin. Alternatively, tying this pin to V_{SS} enables the internal laser trimmed clock oscillator.
9	V_{DD}	Positive Supply Voltage, +5 V ± 5%. Same as Pin 3; both pins must be tied together at the package. This pin should be decoupled to DGND.
10	DB11	Data Bit 11 (MSB). Three-state TTL output. Output coding is 2s complement.
11–13	DB10–DB8	Data Bit 10 to Data Bit 8. Three-state TTL outputs.
14	DGND	Digital Ground. Ground reference for digital circuitry.
15–21	DB7–DB1	Data Bit 7 to Data Bit 1. Three-state TTL outputs.
22	DB0	Data Bit 0 (LSB). Three-state TTL output.
23	AGND	Analog Ground. Ground reference for track/hold, reference and DAC.
24	REF IN	Voltage Reference Input. The reference voltage for the part is applied to this pin. It is internally buffered, requiring an input current of only ±1 μA. The nominal reference voltage for correct operation of the AD7874 is 3 V.
25	REF OUT	Voltage Reference Output. The internal 3 V analog reference is provided at this pin. To operate the AD7874 with internal reference, REF OUT is connected to REF IN. The external load capability of the reference is 500 μA.
26	V_{SS}	Negative Supply Voltage, −5 V ± 5%.
27	V_{IN3}	Analog Input Channel 3. Analog input voltage range is ±10 V.
28	V_{IN4}	Analog Input Channel 4. Analog input voltage range is ±10 V.

TERMINOLOGY

ACQUISITION TIME
Acquisition Time is the time required for the output of the track/hold amplifiers to reach their final values, within ±1/2 LSB, after the falling edge of $\overline{INT}$ (the point at which the track/holds return to track mode). This includes switch delay time, slewing time and settling time for a full-scale voltage change.

APERTURE DELAY
Aperture Delay is defined as the time required by the internal switches to disconnect the hold capacitors from the inputs. This produces an effective delay in sample timing. It is measured by applying a step input and adjusting the $\overline{CONVST}$ input position until the output code follows the step input change.

APERTURE DELAY MATCHING
Aperture Delay Matching is the maximum deviation in aperture delays across the four on-chip track/hold amplifiers.

APERTURE JITTER
Aperture Jitter is the uncertainty in aperture delay caused by internal noise and variation of switching thresholds with signal level.

DROOP RATE
Droop Rate is the change in the held analog voltage resulting from leakage currents.

CHANNEL-TO-CHANNEL ISOLATION
Channel-to-Channel Isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 1 kHz signal to the other three inputs. The figure given is the worst case across all four channels.

SNR, THD, IMD
See DYNAMIC SPECIFICATIONS section.

CONVERTER DETAILS

The AD7874 is a complete 12-bit, 4-channel data acquisition system. It is comprised of a 12-bit successive approximation ADC, four high speed track/hold circuits, a four-channel analog multiplexer and a 3 V Zener reference. The ADC uses a successive-approximation technique and is based on a fast-settling, voltage-switching DAC, a high speed comparator, a fast CMOS SAR and high speed logic.

Conversion is initiated on the rising edge of $\overline{\text{CONVST}}$. All four input track/holds go from track to hold on this edge. Conversion is first performed on the Channel 1 input voltage, then Channel 2 is converted and so on. The four results are stored in on-chip registers. When all four conversions have been completed, $\overline{\text{INT}}$ goes low indicating that data can be read from these locations. The conversion sequence takes either 78 or 79 rising clock edges depending on the synchronization of $\overline{\text{CONVST}}$ with CLK. Internal delays and reset times bring the total conversion time from $\overline{\text{CONVST}}$ going high to $\overline{\text{INT}}$ going low to 32.5 μs maximum for a 2.5 MHz external clock. The AD7874 uses an implicit addressing scheme whereby four successive reads to the same memory location access the four data words sequentially. The first read accesses Channel 1 data, the second read accesses Channel 2 data and so on. Individual data registers cannot be accessed independently.

INTERNAL REFERENCE

The AD7874 has an on-chip temperature compensated buried Zener reference which is factory trimmed to 3 V ±10 mV (see Figure 3). The reference voltage is provided at the REF OUT pin. This reference can be used to provide both the reference voltage for the ADC and the bipolar bias circuitry. This is achieved by connecting REF OUT to REF IN.

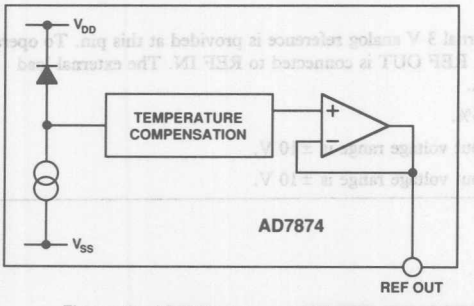


Figure 3. AD7874 Internal Reference

The reference can also be used as a reference for other components and is capable of providing up to 500 μA to an external load. In systems using several AD7874s, using the REF OUT of one device to provide the REF IN for the other devices ensures good full-scale tracking between all the AD7874s. Because the AD7874 REF IN is buffered, each AD7874 presents a high impedance to the reference so one AD7874 REF OUT can drive several AD7874 REF INs.

The maximum recommended capacitance on REF OUT for normal operation is 50 pF. If the reference is required for other system uses, it should be decoupled to AGND with a 200 Ω resistor in series with a parallel combination of a 10 μF tantalum capacitor and a 0.1 μF ceramic capacitor.

EXTERNAL REFERENCE

In some applications, the user may require a system reference or some other external reference to drive the AD7874 reference input. Figure 4 shows how the AD586 5 V reference can be used to provide the 3 V reference required by the AD7874 REF IN.

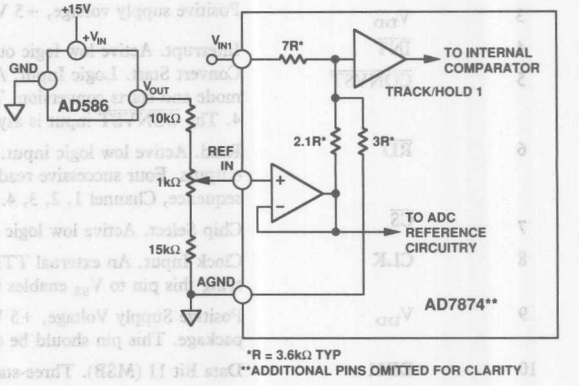


Figure 4. AD586 Driving AD7874 REF IN

TRACK-AND-HOLD AMPLIFIER

The track-and-hold amplifier on each analog input of the AD7874 allows the ADC to accurately convert an input sine wave of 20 V p–p amplitude to 12-bit accuracy. The input bandwidth of the track/hold amplifier is greater than the Nyquist rate of the ADC even when the ADC is operated at its maximum throughput rate. The small signal 3 dB cutoff frequency occurs typically at 500 kHz.

The four track/hold amplifiers sample their respective input channels simultaneously. The aperture delay of the track/hold circuits is small and, more importantly, is well matched across the four track/holds on one device and also well matched from device to device. This allows the relative phase information between different input channels to be accurately preserved. It also allows multiple AD7874s to sample more than four channels simultaneously.

The operation of the track/hold amplifiers is essentially transparent to the user. Once conversion is initiated, the four channels are automatically converted and there is no need to select which channel is to be digitized.

ANALOG INPUT

The analog input of Channel 1 of the AD7874 is as shown in Figure 4. The analog input range is ±10 V into an input resistance of typically 30 kΩ. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs, . . . FS − 3/2 LSBs). The output code is 2s complement binary with 1 LSB = FS/4096 = 20 V/4096 = 4.88 mV. The ideal input/output transfer function is shown in Figure 5.

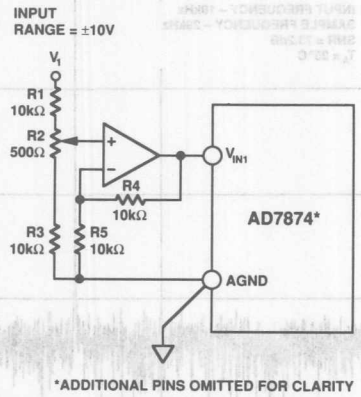


Figure 5. Input/Output Transfer Function

OFFSET AND FULL-SCALE ADJUSTMENT

In most Digital Signal Processing (DSP) applications, offset and full-scale errors have little or no effect on system performance. Offset error can always be eliminated in the analog domain by ac coupling. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. Invariably, some applications will require that the input signal span the full analog input dynamic range. In such applications, offset and full-scale error will have to be adjusted to zero.

Figure 6 shows a circuit which can be used to adjust the offset and full-scale errors on the AD7874 (Channel 1 is shown for example purposes only). Where adjustment is required, offset error must be adjusted before full-scale error. This is achieved by trimming the offset of the op amp driving the analog input of the AD7874 while the input voltage is a 1/2 LSB below analog ground. The trim procedure is as follows: apply a voltage of −2.44 mV (−1/2 LSB) at V_1 in Figure 6 and adjust the op amp offset voltage until the ADC output code flickers between 1111 1111 1111 and 0000 0000 0000.

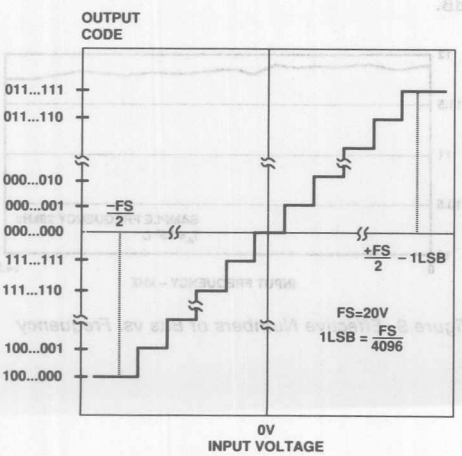


Figure 6. AD7874 Full-Scale Adjust Circuit

Gain error can be adjusted at either the first code transition (ADC negative full scale) or the last code transition (ADC positive full scale). The trim procedures for both cases are as follows:

Positive Full-Scale Adjust
Apply a voltage of +9.9927 V (FS/2 − 3/2 LSBs) at V_1. Adjust R2 until the ADC output code flickers between 0111 1111 1110 and 0111 1111 1111.

Negative Full-Scale Adjust
Apply a voltage of −9.9976 V (−FS + 1/2 LSB) at V_1 and adjust R2 until the ADC output code flickers between 1000 0000 0000 and 1000 0000 0001.

An alternative scheme for adjusting full-scale error in systems which use an external reference is to adjust the voltage at the REF IN pin until the full-scale error for any of the channels is adjusted out. The good full-scale matching of the channels will ensure small full-scale errors on the other channels.

TIMING AND CONTROL

Conversion is initiated on the AD7874 by asserting the $\overline{\text{CONVST}}$ input. This $\overline{\text{CONVST}}$ input is an asynchronous input which is independent of the ADC clock. This is essential for applications where precise sampling in time is important. In these applications, the signal sampling must occur at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. In these cases, the $\overline{\text{CONVST}}$ input is driven from a timer or precise clock source. Once conversion is started, $\overline{\text{CONVST}}$ should not be asserted again until conversion is complete on all four channels.

In applications where precise time interval sampling is not critical, the $\overline{\text{CONVST}}$ pulse can be generated from a microprocessor WRITE or READ line gated with a decoded address (different to the AD7874 $\overline{\text{CS}}$ address). $\overline{\text{CONVST}}$ should not be derived from a decoded address alone because very short $\overline{\text{CONVST}}$ pulses (which may occur in some microprocessor systems as the address bus is changing at the start of an instruction cycle) could initiate a conversion.

All four track/hold amplifiers go from track to hold on the rising edge of the $\overline{\text{CONVST}}$ pulse. The four track/hold amplifiers remain in their hold mode while all four channels are converted. The rising edge of $\overline{\text{CONVST}}$ also initiates a conversion on the Channel 1 input voltage (V_{IN1}). When conversion is complete on Channel 1, its result is stored in Data Register 1, one of four on-chip registers used to store the conversion results. When the result from the first conversion is stored, conversion is initiated on the voltage held by track/hold 2. When conversion has been completed on the voltage held by track/hold 4 and its result is stored in Data Register 4, $\overline{\text{INT}}$ goes low to indicate that the conversion process is complete.

The sequence in which the channel conversions takes place is automatically taken care of by the AD7874. This means that the user does not have to provide address lines to the AD7874 or worry about selecting which channel is to be digitized.

Reading data from the device consists of four read operations to the same microprocessor address. Addressing of the four on-chip data registers is again automatically taken care of by the AD7874. The first read operation to the AD7874 after conversion always accesses data from Data Register 1 (i.e., the conversion result from the V_{IN1} input). $\overline{\text{INT}}$ is reset high on the falling edge of $\overline{\text{RD}}$ during this first read operation. The second read always

CONVST. A read operation to the AD7874 should not be attempted during conversion. The timing diagram for the AD7874 conversion sequence is shown in Figure 7.

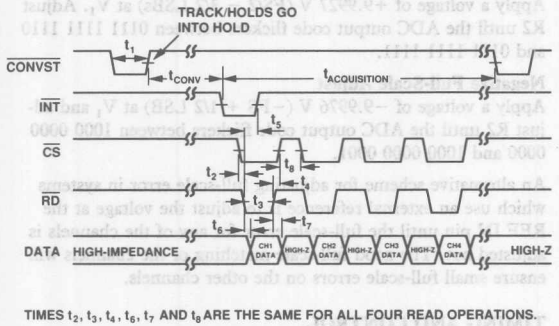


Figure 7. AD7874 Timing Diagram

AD7874 DYNAMIC SPECIFICATIONS

The AD7874 is specified and 100% tested for dynamic performance specifications as well as traditional dc specifications such as Integral and Differential Nonlinearity. These ac specifications are required for the signal processing applications such as phased array sonar, adaptive filters and spectrum analysis. These applications require information on the ADC's effect on the spectral content of the input signal. Hence, the parameters for which the AD7874 is specified include SNR, harmonic distortion, intermodulation distortion and peak harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal to noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (fs/2) excluding dc. SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to noise ratio for a sine wave input is given by

$$SNR = (6.02N + 1.76)\ dB \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

where N is the number of bits.

Thus for an ideal 12-bit converter, SNR = 74 dB.

The output spectrum from the ADC is evaluated by applying a sine wave signal of very low distortion to the V_{IN} input which is sampled at a 29 kHz sampling rate. A Fast Fourier Transform (FFT) plot is generated from which the SNR data can be obtained. Figure 8 shows a typical 2048 point FFT plot of the AD7874BN with an input signal of 10 kHz and a sampling frequency of 29 kHz. The SNR obtained from this graph is 73.2 dB. It should be noted that the harmonics are taken into account when calculating the SNR.

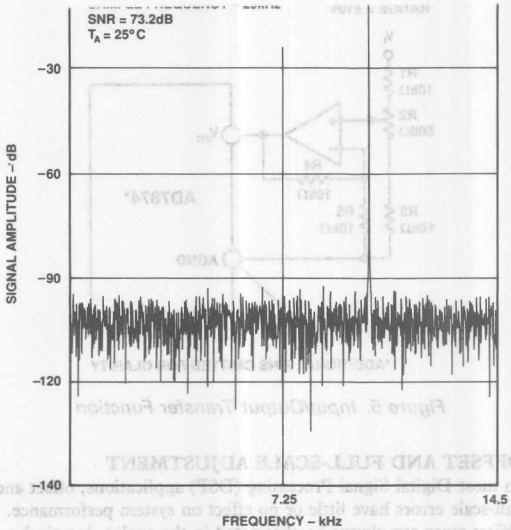


Figure 8. AD7874 FFT Plot

Effective Number of Bits

The formula given in Equation 1 relates the SNR to the number of bits. Rewriting the formula, as in Equation 2, it is possible to get a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR.

Figure 9 shows a typical plot of effective number of bits versus frequency for an AD7874BN with a sampling frequency of 29 kHz. The effective number of bits typically falls between 11.75 and 11.87 corresponding to SNR figures of 72.5 dB and 73.2 dB.

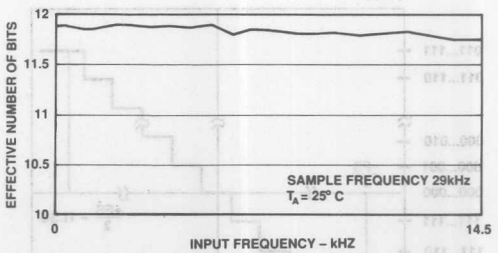


Figure 9. Effective Numbers of Bits vs. Frequency

Total Harmonic Distortion (THD)

Total Harmonic Distortion (THD) is the ratio of the rms sum of harmonics to the rms value of the fundamental. For the AD7874, THD is defined as

$$THD = 20\ log\ \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonic. The THD is also derived from the FFT plot of the ADC output spectrum.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3 . . ., etc. Intermodulation terms are those for which neither m or n are equal to zero. For example, the second order terms include (fa + fb) and (fa − fb) while the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb).

Using the CCIF standard where two input frequencies near the top end of the input bandwidth are used, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs. In this case, the input consists of two, equal amplitude, low distortion sine waves. Figure 10 shows a typical IMD plot for the AD7874.

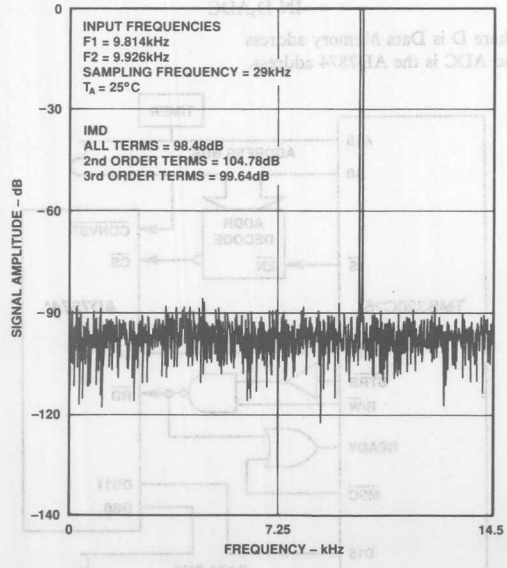


Figure 10. AD7874 IMD Plot

Peak Harmonic or Spurious Noise

Peak Harmonic or Spurious Noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to fs/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor the peak will be a noise peak.

AC Linearity Plot

When a sine wave of specified frequency is applied to the V_{IN} input of the AD7874 and several million samples are taken, a histogram showing the frequency of occurrence of each of the 4096 ADC codes can be generated. From this histogram data it is possible to generate an ac integral linearity plot as shown in Figure 11. This shows very good integral linearity performance from the AD7874 at an input frequency of 10 kHz. The absence of large spikes in the plot shows good differential linearity. Simplified versions of the formulae used are outlined below.

$$INL(i) = \left[\frac{(V(i) - V(o)) \cdot 4096}{V(fs) - V(o)}\right] - i$$

where INL(i) is the integral linearity at code i. V(fs) and V(o) are the estimated full-scale and offset transitions, and V(i) is the estimated transition for the ith code.

V(i), the estimated code transition point is derived as follows:

$$V(i) = -A \cdot Cos\ \frac{[\pi \cdot cum\ (i)]}{N}$$

where A is the peak signal amplitude, N is the number of histogram samples

$$\text{and cum (i)} = \sum_{n=0}^{i} \text{V(n) occurrences}$$

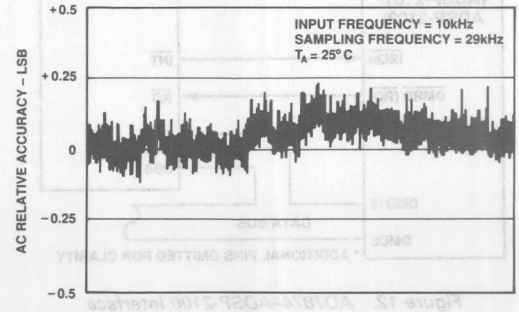


Figure 11. AD7874 AC INL Plot

MICROPROCESSOR INTERFACING

The AD7874 high speed bus timing allows direct interfacing to DSP processors as well as modern 16-bit microprocessors. Suitable microprocessor interfaces are shown in Figures 12 through 16.

AD7874–ADSP-2100 Interface

Figure 12 shows an interface between the AD7874 and the ADSP-2100. Conversion is initiated using a timer which allows very accurate control of the sampling instant on all four channels. The AD7874 $\overline{INT}$ line provides an interrupt to the ADSP-2100 when conversion is completed on all four channels. The four conversion results can then be read from the AD7874 using four successive reads to the same memory address. The following instruction reads one of the four results (this instruction is repeated four times to read all four results in sequence):

MR0 = DM(ADC)

where MR0 is the ADSP-2100 MR0 register and ADC is the AD7874 address.

AD7874–ADSP-2101/ADSP-2102 Interface

The interface outlined in Figure 12 also forms the basis for an interface between the AD7874 and the ADSP-2101/ADSP-2102. The READ line of the ADSP-2101/ADSP-2102 is labeled $\overline{RD}$. In this interface, the $\overline{RD}$ pulse width of the processor can be programmed using the Data Memory Wait State Control Register. The instruction used to read one of the four results is as outlined for the ADSP-2100.

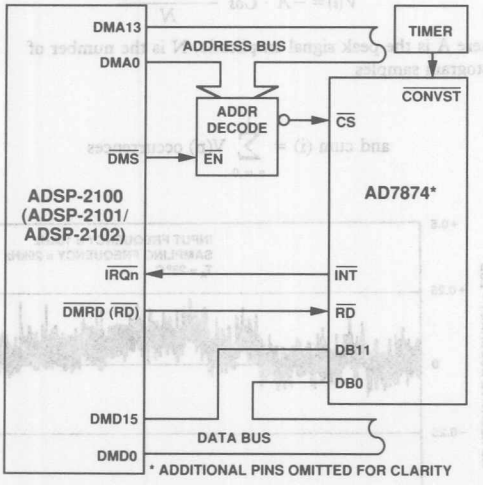


Figure 12. AD7874–ADSP-2100 Interface

AD7874–TMS32010 Interface

An interface between the AD7874 and the TMS32010 is shown in Figure 13. Once again the conversion is initiated using an external timer and the TMS32010 is interrupted when all four conversions have been completed. The following instruction is used to read the conversion results from the AD7874:

IN D,ADC

where D is Data Memory address and ADC is the AD7874 address.

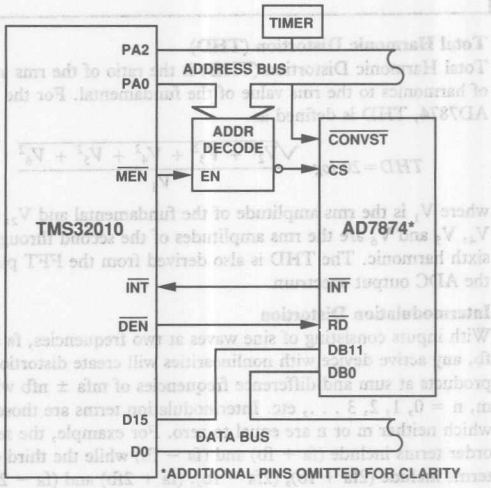


Figure 13. AD7874–TMS32010 Interface

AD7874–TMS320C25 Interface

Figure 14 shows an interface between the AD7874 and the TMS320C25. As with the two previous interfaces, conversion is initiated with a timer and the processor is interrupted when the conversion sequence is completed. The TMS320C25 does not have a separate $\overline{RD}$ output to drive the AD7874 $\overline{RD}$ input directly. This has to be generated from the processor $\overline{STRB}$ and R/$\overline{W}$ outputs with the addition of some logic gates. The $\overline{RD}$ signal is OR-gated with the $\overline{MSC}$ signal to provide the one WAIT state required in the read cycle for correct interface timing. Conversion results are read from the AD7874 using the following instruction:

IN D,ADC

where D is Data Memory address and ADC is the AD7874 address.

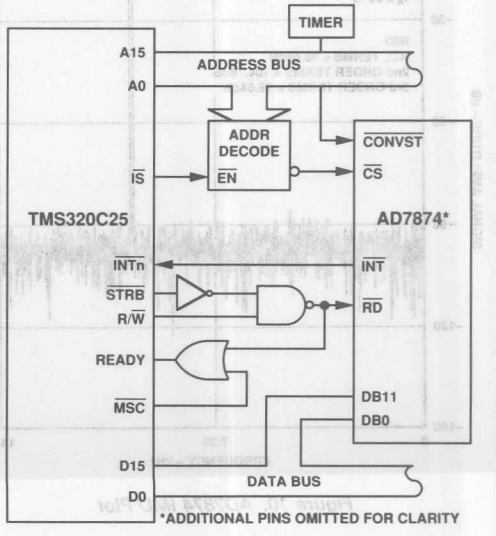


Figure 14. AD7874–TMS320C25 Interface

Some applications may require that the conversion is initiated by the microprocessor rather than an external timer. One option is to decode the AD7874 $\overline{CONVST}$ from the address bus so that a write operation starts a conversion. Data is read at the end of the conversion sequence as before. Figure 16 shows an example of initiating conversion using this method. Note that for all interfaces, a read operation should not be attempted during conversion.

AD7874–MC68000 Interface

An interface between the AD7874 and the MC68000 is shown in Figure 15. As before, conversion is initiated using an external timer. The AD7874 $\overline{INT}$ line can be used to interrupt the processor or, alternatively, software delays can ensure that conversion has been completed before a read to the AD7874 is attempted. Because of the nature of its interrupts, the 68000 requires additional logic (not shown in Figure 15) to allow it to be interrupted correctly. For further information on 68000 interrupts, consult the 68000 users manual.

The MC68000 $\overline{AS}$ and R/$\overline{W}$ outputs are used to generate a separate $\overline{RD}$ input signal for the AD7874. $\overline{CS}$ is used to drive the 68000 $\overline{DTACK}$ input to allow the processor to execute a normal read operation to the AD7874. The conversion results are read using the following 68000 instruction:

MOVE.W ADC,D0

where D0 is the 68000 D0 register
and ADC is the AD7874 address.

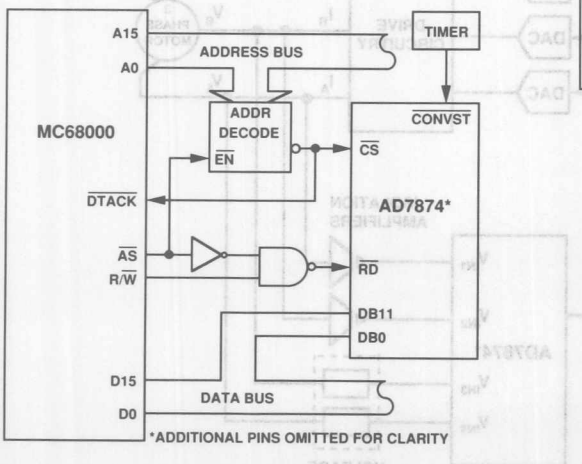


Figure 15. AD7874–MC68000 Interface

AD7874–8086 Interface

Figure 16 shows an interface between the AD7874 and the 8086 microprocessor. Unlike the previous interface examples, the microprocessor initiates conversion. This is achieved by gating the 8086 $\overline{WR}$ signal with a decoded address output (different to the AD7874 $\overline{CS}$ address). The AD7874 $\overline{INT}$ line is used to interrupt the microprocessor when the conversion sequence is completed. Data is read from the AD7874 using the following instruction:

MOV AX,ADC

where AX is the 8086 accumulator
and ADC is the AD7874 address.

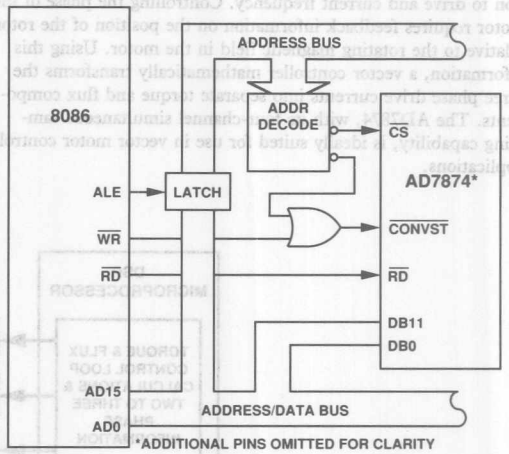


Figure 16. AD7874–8086 Interface

APPLICATIONS

Vector Motor Control

The current drawn by a motor can be split into two components: one produces torque and the other produces magnetic flux. For optimal performance of the motor, these two components should be controlled independently. In conventional methods of controlling a three-phase motor, the current (or voltage) supplied to the motor and the frequency of the drive are the basic control variables. However, both the torque and flux are functions of current (or voltage) and frequency. This coupling effect can reduce the performance of the motor because, for example, if the torque is increased by increasing the frequency, the flux tends to decrease.

Vector control of an ac motor involves controlling phase in addition to drive and current frequency. Controlling the phase of the motor requires feedback information on the position of the rotor relative to the rotating magnetic field in the motor. Using this information, a vector controller mathematically transforms the three phase drive currents into separate torque and flux components. The AD7874, with its four-channel simultaneous sampling capability, is ideally suited for use in vector motor control applications.

A block diagram of a vector motor control application using the AD7874 is shown in Figure 17. The position of the field is derived by determining the current in each phase of the motor. Only two phase currents need to be measured because the third can be calculated if two phases are known. Channel 1 and Channel 2 of the AD7874 are used to digitize this information. Simultaneous sampling is critical to maintain the relative phase information between the two channels. A current sensing isolation amplifier, transformer or Hall effect sensor is used between the motor and the AD7874. Rotor information is obtained by measuring the voltage from two of the inputs to the motor. Channel 3 and Channel 4 of the AD7874 are used to obtain this information. Once again the relative phase of the two channels is important. A DSP microprocessor is used to perform the mathematical transformations and control loop calculations on the information fed back by the AD7874.

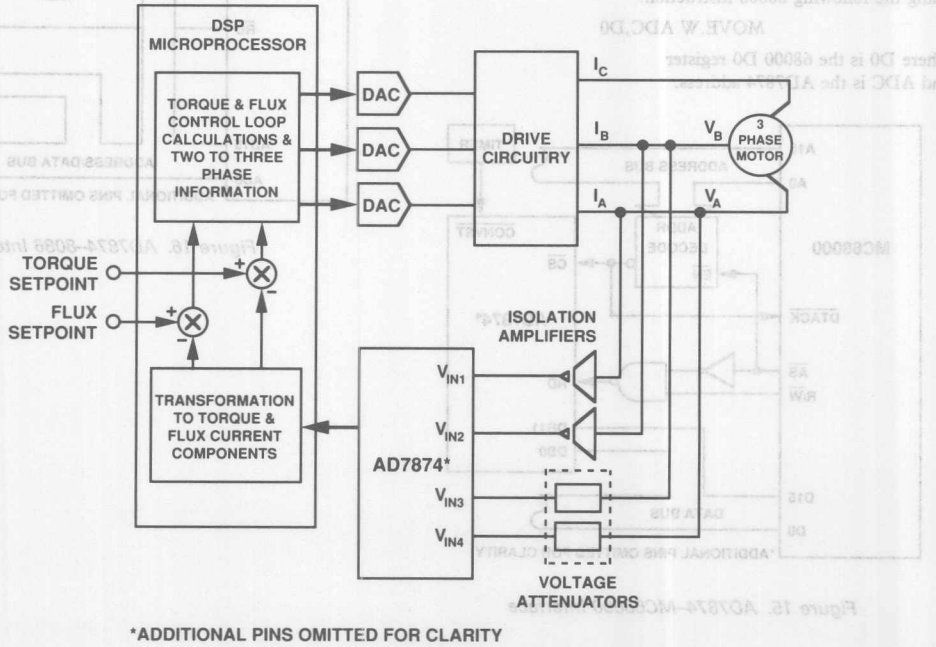


Figure 17. Vector Motor Control Using the AD7874

MULTIPLE AD7874s

Figure 18 shows a system where a number of AD7874s can be configured to handle multiple input channels. This type of configuration is common in applications such as sonar, radar, etc. The AD7874 is specified with maximum and minimum limits on aperture delay. This means that the user knows the maximum difference in the sampling instant between all channels. This allows the user to maintain relative phase information between the different channels.

A common read signal from the microprocessor drives the $\overline{RD}$ input of all AD7874s. Each AD7874 is designated a unique address selected by the address decoder. The reference output of AD7874 number 1 is used to drive the reference input of all other AD7874s in the circuit shown in Figure 18. One REF OUT pin can drive several AD7874 REF IN pins. Alternatively, an external or system reference can be used to drive all REF IN inputs. A common reference ensures good full-scale tracking between all channels.

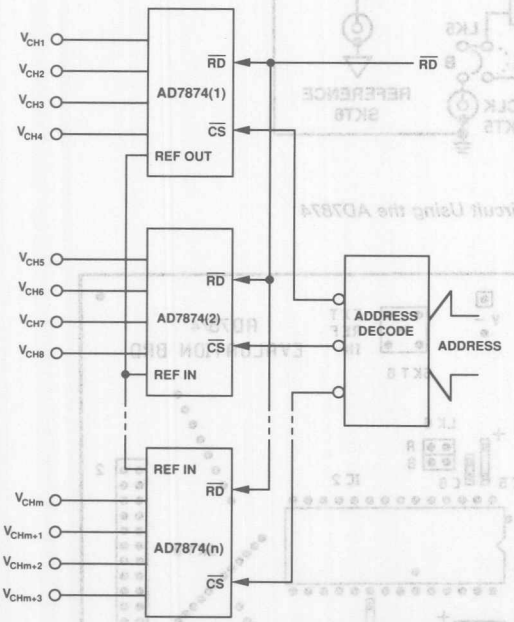


Figure 18. Multiple AD7874s in Multichannel System

DATA ACQUISITION BOARD

Figure 20 shows the AD7874 in a data acquisition circuit. The corresponding printed circuit board (PCB) layout and silkscreen are shown in Figures 21 to 23. A 26-contact IDC connector provides for a microprocessor connection to the board.

A component grid is provided near the analog inputs on the PCB which may be used to provide antialiasing filters for the analog input channels or to provide signal conditioning circuitry. To facilitate this option, four shorting plugs (labeled LK1 to LK4 on the PCB) are provided on the analog inputs, one plug per input. If the shorting plug for a particular channel is used, the input signal connects to the buffer amplifier driving the analog input of the ADC. If the shorting plug is omitted, a wire link can be used to connect the input signal to the PCB component grid.

Microprocessor connections to the board are made via a 26-contact IDC connector, SKT8, the pinout for which is shown in Figure 19. This connector contains all data, control and status signals of the AD7874 (with the exception of the CLK input and the $\overline{CONVST}$ input which are provided via SKT5 and SKT7, respectively). It also contains decoded R/$\overline{W}$ and $\overline{STRB}$ inputs which are necessary for TMS32020 interfacing (and also for 68000 interfacing although pin labels on the 68000 are different). Note that the AD7874 $\overline{CS}$ input must be decoded prior to the AD7874 evaluation board.

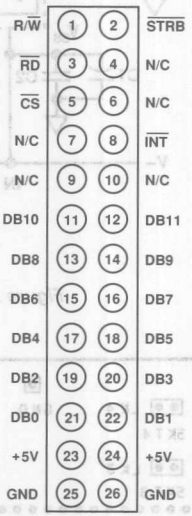


Figure 19. SKT8, IDC Connector Pinout

SKT1, SKT2, SKT3 and SKT4 provide the inputs for V_{IN1}, V_{IN2}, V_{IN3}, V_{IN4} respectively. Assuming LK1 to LK4 are in place, these input signals are fed to four buffer amplifiers, IC1, before being applied to the AD7874. The use of an external clock source is optional; there is a shorting plug (LK5) on the AD7874 CLK input which must be connected to either −5 V (for the ADCs own internal clock) or to SKT5. SKT6 and SKT7 provide the reference and $\overline{CONVST}$ inputs respectively. Shorting plug LK6 provides the option of using the external reference or the ADCs own internal reference.

POWER SUPPLY CONNECTIONS

The PCB requires two analog power supplies and one 5 V digital supply. The analog supplies are labeled V+ and V− and the range for both supplies is 12 V to 15 V (see silkscreen in Figure 23). Connection to the 5 V digital supply is made via SKT8. The +5 V supply and the −5 V supply required by the AD7874 are generated from voltage regulators (IC3 and IC4) on the V+ and V− supplies.

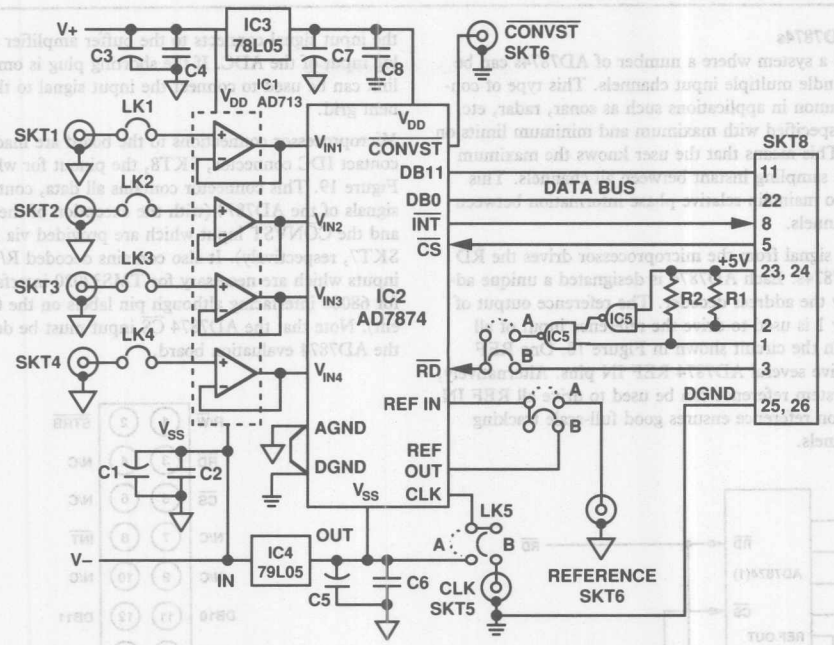


Figure 20. Data Acquisition Circuit Using the AD7874

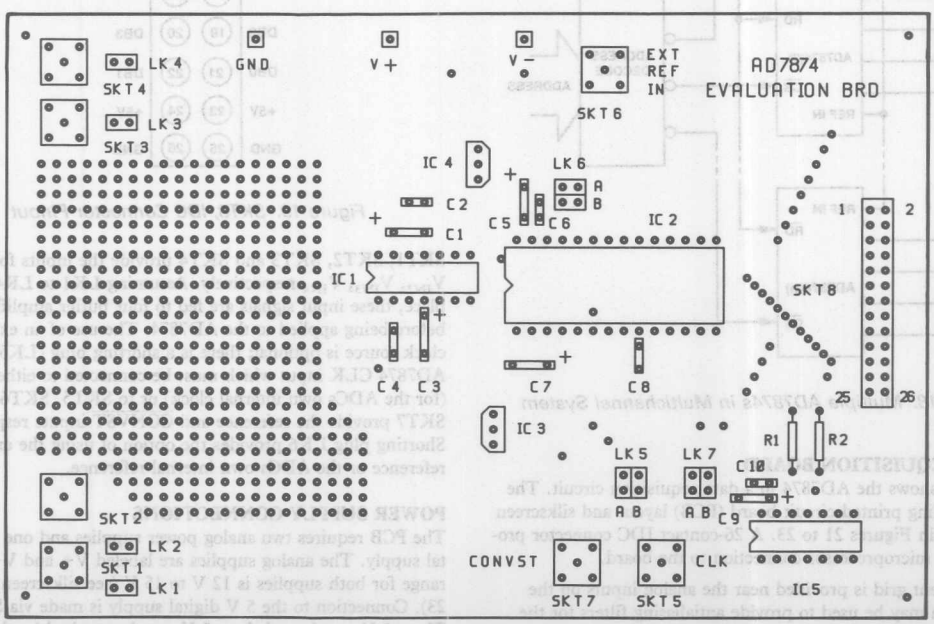


Figure 21. PCB Silkscreen for Figure 20

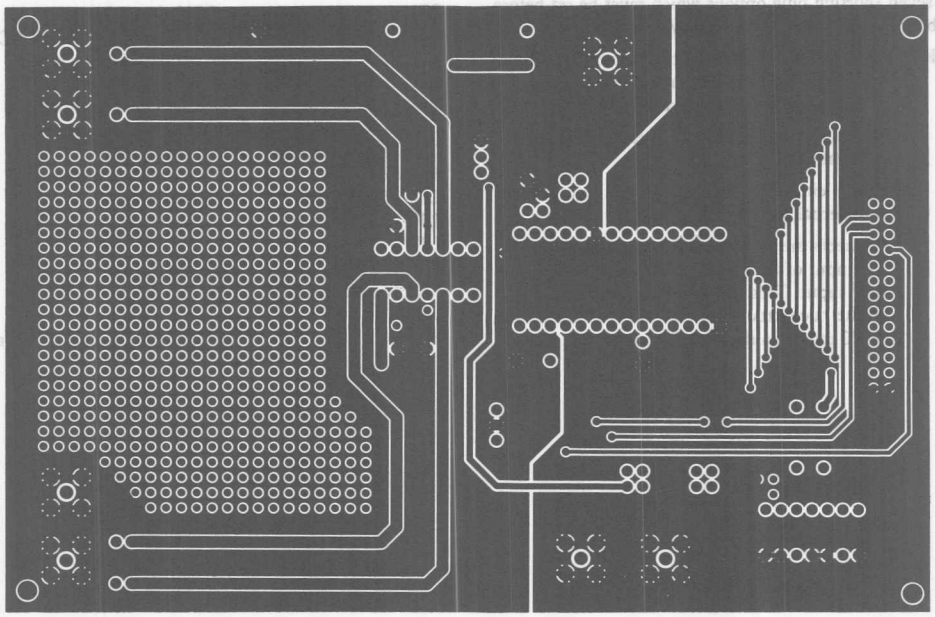


Figure 22. PCB Component Side Layout for the Circuit of Figure 20

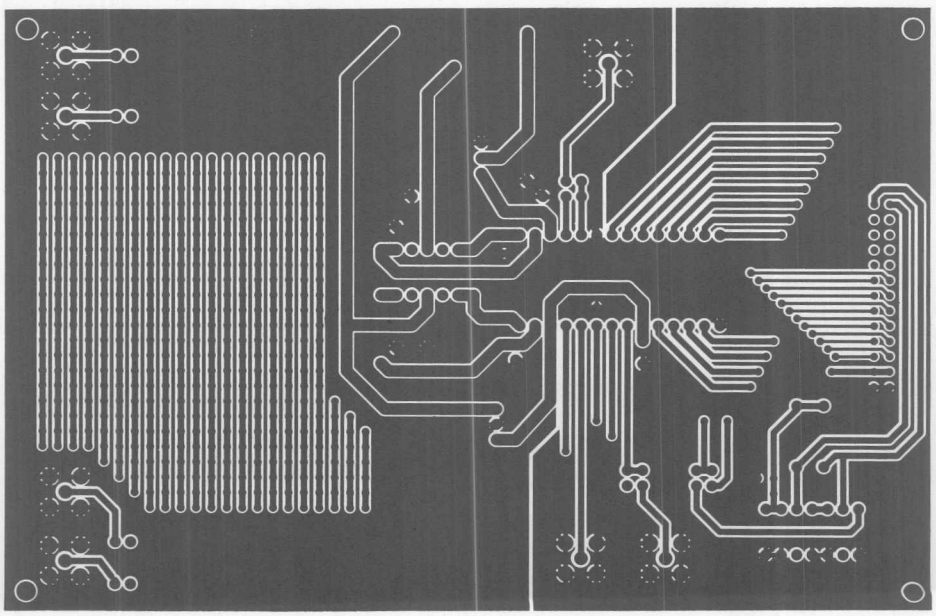


Figure 23. PCB Solder Side Layout for the Circuit of Figure 20

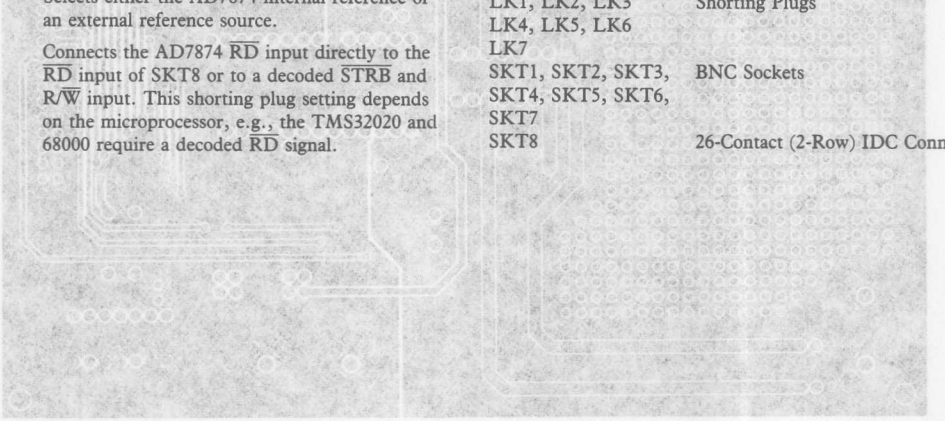
SHORTING PLUG OPTIONS

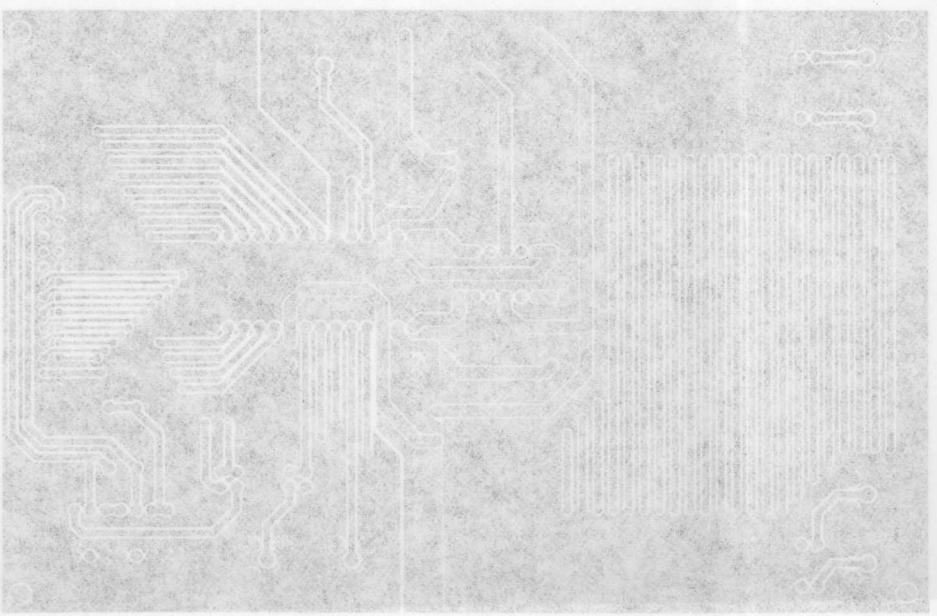
There are seven shorting plug options which must be set before using the board. These are outlined below:

LK1 – LK4	Connects the analog inputs to the buffer amplifiers. The analog inputs may also be connected to a component grid for signal conditioning.
LK5	Selects either the AD7874 internal clock or an external clock source.
LK6	Selects either the AD7874 internal reference or an external reference source.
LK7	Connects the AD7874 $\overline{RD}$ input directly to the $\overline{RD}$ input of SKT8 or to a decoded $\overline{STRB}$ and R/$\overline{W}$ input. This shorting plug setting depends on the microprocessor, e.g., the TMS32020 and 68000 require a decoded $\overline{RD}$ signal.

COMPONENT LIST

IC1	AD713 Quad Op Amp
IC2	AD7874 Analog-to-Digital Converter
IC3	MC78L05 +5 V Regulator
IC4	MC79L05 −5 V Regulator
IC5	74HC00 Quad NAND Gate
C1, C3, C5, C7, C9	10 μF Capacitors
C2, C4, C6, C8, C10	0.1 μF Capacitors
R1, R2	10 kΩ Pull-Up Resistors
LK1, LK2, LK3	Shorting Plugs
LK4, LK5, LK6	
LK7	
SKT1, SKT2, SKT3,	BNC Sockets
SKT4, SKT5, SKT6,	
SKT7	
SKT8	26-Contact (2-Row) IDC Connector





LC²MOS Complete 12-Bit 100 kHz Sampling ADC with DSP Interface

AD7878

2

FEATURES

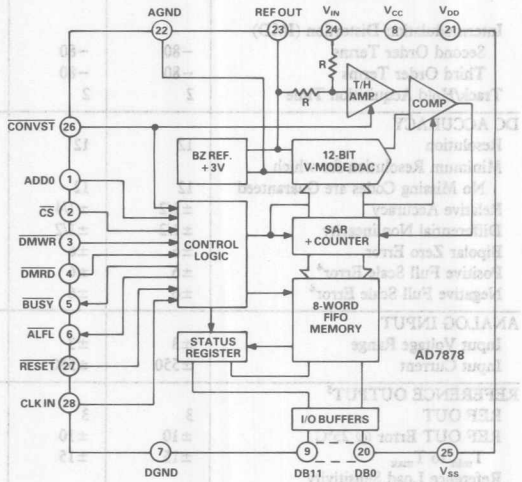
Complete ADC with DSP Interface, Comprising:
- **Track/Hold Amplifier with 2 µs Acquisition Time**
- **7 µs A/D Converter**
- **3 V Zener Reference**
- **8-Word FIFO and Interface Logic**

72 dB SNR at 10 kHz Input Frequency
Interfaces to High Speed DSP Processors, e.g., ADSP-2100, TMS32010, TMS32020
41 ns max Data Access Time
Low Power, 60 mW typ

APPLICATIONS

Digital Signal Processing
Speech Recognition and Synthesis
Spectrum Analysis
High Speed Modems
DSP Servo Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7878 is a fast, complete 12-bit A/D converter with a versatile DSP interface consisting of an 8-word, first-in, first-out (FIFO) memory and associated control logic.

The FIFO memory allows up to eight samples to be digitized before the microprocessor is required to service the A/D converter. The eight words can then be read out of the FIFO at maximum microprocessor speed. A fast data access time of 41 ns allows direct interfacing to DSP processors and high speed 16-bit microprocessors.

An on-chip status/control register allows the user to program the effective length of the FIFO and contains the FIFO out of range, FIFO empty and FIFO word count information.

The analog input of the AD7878 has a bipolar range of ±3 V. The AD7878 can convert full power signals up to 50 kHz and is fully specified for dynamic parameters such as signal-to-noise ratio and harmonic distortion.

The AD7878 is fabricated in Linear Compatible CMOS (LC^2MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in four package styles, 28-pin plastic and hermetic dual-in-line package (DIP), leadless ceramic chip carrier (LCCC) or plastic leaded chip carrier (PLCC).

PRODUCT HIGHLIGHTS

1. Complete A/D Function with DSP Interface
   The AD7878 provides the complete function for digitizing ac signals to 12-bit accuracy. The part features an on-chip track/hold, on-chip reference and 12-bit A/D converter. The additional feature of an 8-word FIFO reduces the high software overheads associated with servicing interrupts in DSP processors.
2. Dynamic Specifications for DSP Users
   The AD7878 is fully specified and tested for ac parameters, including signal-to-noise ratio, harmonic distortion and intermodulation distortion. Key digital timing parameters are also tested and specified over the full operating temperature range.
3. Fast Microprocessor Interface
   Data access time of 41 ns is the fastest ever achieved in a monolithic A/D converter and makes the AD7878 compatible with all modern 16-bit microprocessors and digital signal processors.

Parameter	J, A Versions[1]	K, L, B Versions	S Version	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					
Signal-to-Noise Ratio (SNR)[3] @ 25°C	70	72	70	dB min	V_{IN} = 10 kHz Sine Wave , f_{SAMPLE} = 100 kHz
T_{min} to T_{max}	70	71	70	dB min	Typically 71.5 dB for 0<V_{IN}<50 kHz
Total Harmonic Distortion (THD)	−80	−80	−78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz Typically −86 dB for 0<V_{IN}<50 kHz
Peak Harmonic or Spurious Noise	−80	−80	−78	dB max	V_{IN} = 10 kHz, f_{SAMPLE} = 100 kHz Typically −86 dB for 0<V_{IN}<50 kHz
Intermodulation Distortion (IMD)					
Second Order Terms	−80	−80	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	−80	−80	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Track/Hold Acquisition Time	2	2	2	µs max	See Throughput Rate Section.
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for which					
No Missing Codes are Guaranteed	12	12	12	Bits	
Relative Accuracy	±1/2	±1/4	±1/2	LSB typ	
Differential Nonlinearity	±1/2	±1/2	±1/2	LSB typ	
Bipolar Zero Error	±6	±6	±6	LSB max	
Positive Full Scale Error[4]	±6	±6	±6	LSB max	
Negative Full Scale Error[4]	±6	±6	±6	LSB max	
ANALOG INPUT					
Input Voltage Range	±3	±3	±3	Volts	
Input Current	±550	±550	±550	µA max	
REFERENCE OUTPUT[5]					
REF OUT	3	3	3	V nom	
REF OUT Error @ 25°C	±10	±10	±10	mV max	
T_{min} to T_{max}	±15	±15	±15	mV max	
Reference Load Sensitivity (ΔREF OUT/ΔI)	±1	±1	±1	mV max	Reference Load Current Change (0–500 µA). Reference Load Should Not Be Changed During Conversion.
LOGIC INPUTS					
Input High Voltage, V_{INH}	+2.4	+2.4	+2.4	V min	V_{CC} = +5 V ± 5%
Input Low Voltage, V_{INL}	+0.8	+0.8	+0.8	V max	V_{CC} = +5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	µA max	V_{IN} = 0 to V_{CC}
Input Capacitance, C_{IN}[6]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	+2.7	+2.7	+2.7	V min	I_{SOURCE} = 40 µA
Output Low Voltage, V_{OL}	+0.4	+0.4	+0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0					
Floating State Leakage Current	±10	±10	±10	±10	µA max
Floating State Output Capacitance[6]	15	15	15	15	pF max
CONVERSION TIME					
	7/7.125	7/7.125	7/7.125	µs min/µs max	Assuming No External Read/Write Operations
	7/9.250	7/9.250	7/9.250	µs min/µs max	Assuming 17 External Read/Write Operations See Internal Comparator Timing Section
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{CC}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	13	13	13	mA max	$\overline{CS}$ = $\overline{DMWR}$ = $\overline{DMRD}$ = 5 V
I_{CC}	100	100	100	µA max	$\overline{CS}$ = $\overline{DMWR}$ = $\overline{DMRD}$ = 5 V
I_{SS}	6	6	6	mA max	$\overline{CS}$ = $\overline{DMWR}$ = $\overline{DMRD}$ = 5 V
Power Dissipation	95.5	95.5	95.5	mW max	Typically 60 mW

NOTES

[1]Temperature range as follows: J, K, L versions: 0 to +70°C; A, B versions: −25°C to +85°C; S version: −55°C to +125°C.

[2]V_{IN} = ±3 V. See Dynamic Specifications section.

[3]SNR calculation includes distortion and noise components.

[4]Measured with respect to the Internal Reference.

[5]For Capacitive Loads greater than 50 pF a series resistor is required (see Internal Reference section).

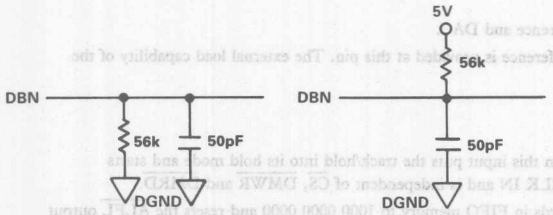
[6]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = 5 V ± 5%, V_{CC} = 5 V ± 5%, V_{SS} = −5 V ± 5%)

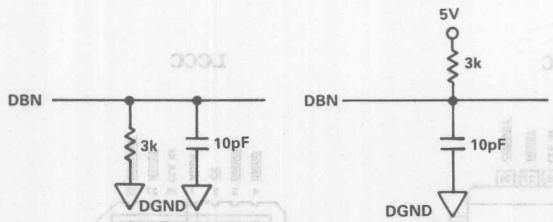
Parameter	Limit at T_{min}, T_{max} (L Grade)	Limit at T_{min}, T_{max} (J, K, A, B Grades)	Limit at T_{min}, T_{max} (S Grade)	Units	Conditions/Comments
t_1	65	65	75	ns max	CLK IN to BUSY Low Propagation Delay
t_2	65	65	75	ns max	CLK IN to BUSY High Propagation Delay
t_3	2 CLK IN cycles	2 CLK IN cycles	2 CLK IN cycles	min	CONVST Pulse Width
t_4	0	0	0	ns min	CS to DMRD/REGISTER ENABLE Setup Time
t_5	0	0	0	ns min	CS to DMRD/REGISTER ENABLE Hold Time
t_6	**45**	**60**	**60**	ns min	DMRD Pulse Width
	50	50	50	µs max	
t_7	**16**	**16**	**16**	ns min	ADD0 to DMRD/REGISTER ENABLE Setup Time
t_8	0	0	0	ns min	ADD0 to DMRD/REGISTER ENABLE Hold Time
t_9[2]	**41**	**57**	**57**	ns min	Data Access Time after DMRD
t_{10}[3]	5	5	5	ns min	Bus Relinquish Time
	45	**45**	**45**	ns max	
t_{11}	**42**	**42**	**55**	ns min	REGISTER ENABLE Pulse Width
	50	50	50	µs max	
t_{12}	**20**	**20**	**30**	ns min	Data Valid to REGISTER ENABLE Setup Time
t_{13}	10	10	10	ns min	Data Hold Time after REGISTER ENABLE
t_{14}[2]	41	57	57	ns min	Data Access Time after BUSY
t_{RESET}	2 CLK IN cycles	2 CLK IN cycles	2 CLK IN cycles	min	RESET Pulse Width

NOTES
[1]Timing Specifications in **bold** print are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]t_9 and t_{14} are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[3]t_{10} is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.



a. High-Z to V_{OH} *b. High-Z to V_{OL}*

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 2. Load Circuits for Output Float Delay

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} to DGND . . . . . −0.3 V to +7 V
V_{CC} to DGND . . . . . −0.3 V to +7 V
V_{SS} to DGND . . . . . +0.3 V to −7 V
V_{DD} to V_{CC} . . . . . −0.3 V to +0.3 V
AGND to DGND . . . . . −0.3 V to V_{DD} +0.3 V
V_{IN} to AGND . . . . . −15 V to +15 V
REF OUT to AGND . . . . . 0 to V_{DD}
Digital Inputs to DGND
CLK IN, DMWR, DMRD, RESET, CS, CONVST, ADD0 . . . . . −0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND
ALFL, BUSY . . . . . −0.3 V to V_{DD} +0.3 V
Data Pins
DB11–DB0 . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
J, K, L Versions . . . . . 0 to +70°C
A, B Versions . . . . . −25°C to +85°C
S Version . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

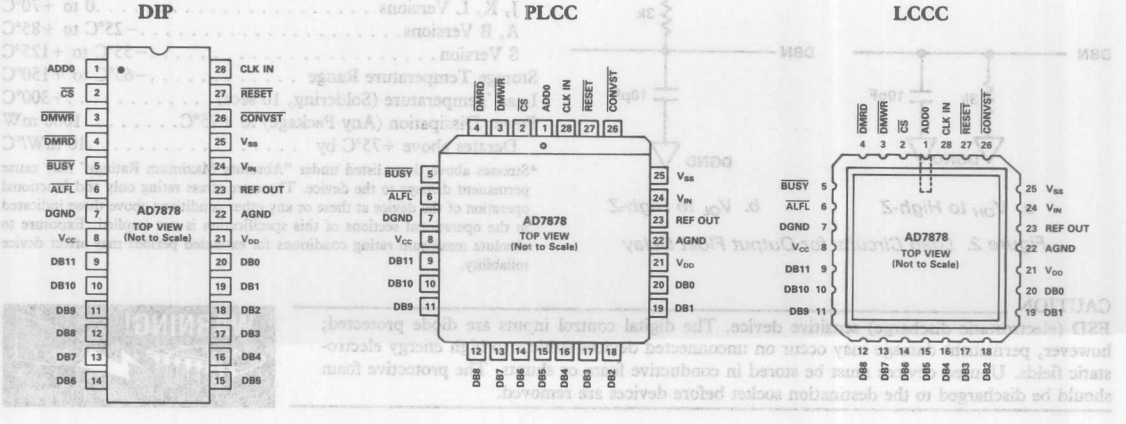
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



PIN FUNCTION DESCRIPTION

Pin Number	Pin Mnemonic	Function
1	ADD0	Address Input. This control input determines whether the word placed on the output data bus during a read operation is a data word from the FIFO RAM or the contents of the status/control register. A logic low accesses the data word from Location 0 of the FIFO while a logic high selects the contents of the register (see Status/Control Register section).
2	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active.
3	$\overline{DMWR}$	Data Memory Write. Active low logic input. $\overline{DMWR}$ is used in conjunction with $\overline{CS}$ low and ADD0 high to write data to the status/control register. Corresponds to $\overline{DMWR}$ (ADSP-2100), R/$\overline{W}$ (MC68000, TMS32020), $\overline{WE}$ (TMS32010).
4	$\overline{DMRD}$	Data Memory READ. Active low logic input. $\overline{DMRD}$ is used in conjunction with $\overline{CS}$ low to enable the three-state output buffers. Corresponds directly to $\overline{DMRD}$ (ADSP-2100), $\overline{DEN}$ (TMS32010).
5	$\overline{BUSY}$	Active low logic output. This output goes low when the ADC receives a $\overline{CONVST}$ pulse and remains low until the track/hold has gone into its hold mode. The three-state drivers of the AD7878 can be disabled while the $\overline{BUSY}$ signal is low (see Extended READ/WRITE section). This is achieved by writing a logic 0 to DB5 ($\overline{DISO}$) of the status/control register. Writing a logic 1 to DB5 of the status/control register allows data to be accessed from the AD7878 while $\overline{BUSY}$ is low.
6	$\overline{ALFL}$	FIFO Almost Full. A logic low indicates that the word count (i.e., number of conversion results) in the FIFO memory has reached the programmed word count in the status/control register. $\overline{ALFL}$ is updated at the end of each conversion. The $\overline{ALFL}$ output is reset to a logic high when a word is read from the FIFO memory and the word count is less than the preprogrammed word count. It can also be set high by writing a logic 1 to DB7 ($\overline{ENAF}$) of the status/control register.
7	DGND	Digital Ground. Ground reference for digital circuitry.
8	V_{CC}	Digital supply voltage, +5 V ±5%. Positive supply voltage for digital circuitry.
9	DB11	Data Bit 11 (MSB). Three-state TTL output. Coding for the data words in FIFO RAM is 2s complement.
10–15	DB10–DB5	Data Bit 10 to Data Bit 5. Three-state TTL input/outputs.
16–19	DB4–DB1	Data Bit 4 to Data Bit 1. Three-state TTL outputs.
20	DB0	Data Bit 0 (LSB). Three-state TTL output.
21	V_{DD}	Analog positive supply voltage, +5 V ±5%.
22	AGND	Analog Ground. Ground reference for track/hold, reference and DAC.
23	REF OUT	Voltage Reference Output. The internal 3 V analog reference is provided at this pin. The external load capability of the reference is 500 μA.
24	V_{IN}	Analog Input. Analog input range is ±3 V.
25	V_{SS}	Analog negative supply voltage, −5 V ±5%.
26	$\overline{CONVST}$	Convert Start. Logic input. A low to high transition on this input puts the track/hold into its hold mode and starts conversion. The $\overline{CONVST}$ input is asynchronous to CLK IN and is independent of $\overline{CS}$, $\overline{DMWR}$ and $\overline{DMRD}$.
27	$\overline{RESET}$	Reset. Active low logic input. A logic low sets the words in FIFO memory to 1000 0000 0000 and resets the $\overline{ALFL}$ output and status/control register.
28	CLK IN	Clock Input. TTL-compatible logic input. Used as the clock source for the A/D converter. The mark-space ratio of this clock can vary from 35/65 to 65/35.

PIN CONFIGURATIONS



ORDERING GUIDE

Model[1, 2]	Temperature Range	Signal-to-Noise Ratio	Data Access Time	Package Options[3]
AD7878JN	0°C to +70°C	70 dB	57 ns	N-28
AD7878AQ	−25°C to +85°C	70 dB	57 ns	Q-28
AD7878SQ	−55°C to +125°C	70 dB	57 ns	Q-28
AD7878KN	0°C to +70°C	72 dB	57 ns	N-28
AD7878BQ	−25°C to +85°C	72 dB	57 ns	Q-28
AD7878LN	0°C to +70°C	72 dB	41 ns	N-28
AD7878SE[4]	−55°C to +125°C	70 dB	57 ns	E-28A
AD7878JP	0°C to +70°C	70 dB	57 ns	P-28A
AD7878KP	0°C to +70°C	72 dB	57 ns	P-28A
AD7878LP	0°C to +70°C	72 dB	41 ns	P-28A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact our local sales office for military data sheet.
[2]Analog Devices reserves the right to ship either ceramic (D-28) packages or cerdip (Q-28) hermetic packages.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier, Q = Cerdip. For outline information see Package Information section.
[4]Available to /883B processing only.

STATUS/CONTROL REGISTER

The status/control register serves the dual function of providing control and monitoring the status of the FIFO memory. This register is directly accessible through the data bus (DB11–DB0) with a read or write operation while ADD0 is high. A write operation to the status/control register provides control for the $\overline{ALFL}$ output, bus interface and FIFO counter reset. This is normally done on power-up initialization. The FIFO memory address pointer is incremented after each conversion and compared with a preprogrammed count in the status/control register. When this preprogrammed count is reached, the $\overline{ALFL}$ output is asserted if the $\overline{ENAF}$ control bit is set to zero. This $\overline{ALFL}$ can be used to interrupt the microprocessor after any predetermined number of conversions (between 1 and 8). The status of the address pointer along with sample overrange and $\overline{ALFL}$ status can be accessed at any time by reading the status/control register. Note, reading the status/control register does not cause any internal data movement in the FIFO memory. Status information for a particular word should be read from the status register before the data word is read from the FIFO memory.

STATUS/CONTROL REGISTER FUNCTION DESCRIPTION

DB11 ($\overline{ALFL}$)

Almost Full Flag, Read only. This is the same as Pin 6 ($\overline{ALFL}$ output) status. A logic low indicates that the word count in the FIFO memory has reached the preprogrammed count in bit locations DB10–DB8. $\overline{ALFL}$ is updated at the end of conversion.

DB10–DB8 (AFC2–AFC0)

Almost Full Word Count, Read/Write. The count value determines the number of words in the FIFO memory which will cause $\overline{ALFL}$ to be set. When the FIFO word count equals the programmed count in these three bits, then both the $\overline{ALFL}$ output and DB11 of the status register are set to a logic low. For example, when a code of 011 is written to these bits, $\overline{ALFL}$ is set when Location 0 through Location 3 of the FIFO memory contains valid data. AFC2 is the most significant bit of the word count. The count value can be read back if required.

DB7 ($\overline{ENAF}$)

Enable Almost Full, Read/Write. Writing a 1 to this bit disables the $\overline{ALFL}$ output and status register bit DB11.

DB6 (FOVR/RESET)

FIFO Overrun/RESET, Read/Write. Reading a 1 from this bit indicates that at least one sample has been discarded because the FIFO memory is full. When the FIFO is full (i.e., contains eight words) any further conversion results will be lost. Writing a 1 to this bit causes a system RESET as per the $\overline{RESET}$ input (Pin 27).

DB5 (FOOR/$\overline{DISO}$)

FIFO Out of RANGE/Disable Outputs, Read/Write. Reading a 1 from this bit indicates that at least one sample in the FIFO memory is out of range. Writing a 0 to this bit prevents the data bus from becoming active while $\overline{BUSY}$ is low, regardless of the state of $\overline{CS}$ and $\overline{DMRD}$.

DB4 (FEMP)

FIFO Empty, Read Only. Reading a 1 indicates that there are no samples in the FIFO memory. When the FIFO is empty the internal ripple-down effects of the FIFO are disabled and further reads will continue to access the last valid data word in Location 0.

DB3 (SOOR)

Sample out of Range, Read Only. Reading a 1 indicates that the next sample to be read is out of range, i.e., the sample in Location 0 of the FIFO.

DB2–DB0 (FCN2–FCN0)

FIFO Word Count, Read Only. The value read from these bits indicates the number of samples in the FIFO memory. For example, reading 011 from these bits indicates that Location 0 through Location 3 contains valid data. Note, reading all 0s indicates that there is either one word or no word in the FIFO memory; in this case the FIFO Empty determines if there is no word in memory. FCN2 is the most significant bit.

Table I. Status/Control Bit Function Description

BIT LOCATION	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
STATUS INFORMATION (READ)	$\overline{ALFL}$	AFC2	AFC1	AFC0	$\overline{ENAF}$	FOVR	FOOR	FEMP	SOOR	FCN2	FCN1	FCN0
CONTROL FUNCTION (WRITE)	X	AFC2	AFC1	AFC0	$\overline{ENAF}$	RESET	$\overline{DISO}$	X	X	X	X	X
RESET STATUS	1	0	0	0	0	0	0	1	0	0	0	0

X =DON'T CARE

memory locations. Each word in memory contains 13 bits of information - 12 bits of data from the conversion result and one additional bit which contains information as to whether the 12-bit result is out of range or not. A block diagram of the AD7878 FIFO architecture is shown in Figure 3.

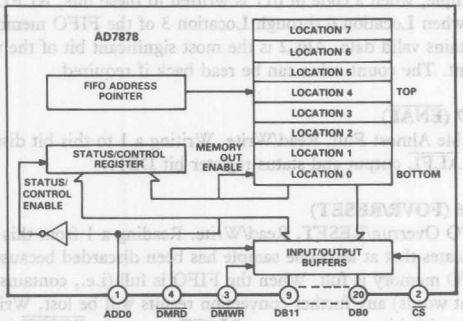


Figure 3. Internal FIFO Architecture

The conversion result is gathered in the successive approximation register (SAR) during conversion. At the end of conversion this result is transferred to the FIFO memory. The FIFO address pointer always points to the top of memory, which is the uppermost location containing valid data. The pointer is incremented after each conversion. A read operation from the FIFO memory accesses data from the bottom of the FIFO, Location 0. On completion of the read operation, each data word moves down one location and the address pointer is decremented by one. Therefore, each conversion result from the SAR enters at the top of memory, propagates down with successive reads until it reaches Location 0 from where it can be accessed by a microprocessor read operation.

The transfer of information from the SAR to the FIFO occurs in synchronization with the AD7878 input clock (CLK IN). The propagation of data words down the FIFO is also synchronous with this clock. As a result, a read operation to obtain data from the FIFO must also be synchronous with CLK IN to avoid Read/Write conflicts in the FIFO (i.e., reading from FIFO Location 0 while it is being updated). This requires that the microprocessor clock and the AD7878 CLK IN are derived from the same source.

INTERNAL COMPARATOR TIMING

The ADC clock, which is applied to CLK IN, controls the successive approximation A/D conversion process. This clock is internally divided by four to yield a bit trial cycle time of 500 ns latched by the rising edge of an internal comparator strobe signal. There are 12 bit decisions, as in a normal successive approximation routine, and one extra decision that checks if the input sample is out of range. In a normal successive approximation A/D converter, reading data from the device during conversion can upset the conversion in progress. This is due to on-chip transients, generated by charging or discharging the data bus, concurrent with a bit decision. The scheme outlined below and shown in Figure 4 describes how the AD7878 overcomes this problem.

The internal comparator strobe on the AD7878 is gated with both $\overline{\text{DMRD}}$ and $\overline{\text{DMWR}}$ so that if a read or write operation occurs when a bit decision is about to be made, the bit decision point is deferred by one CLK IN cycle. In other words, if $\overline{\text{DMRD}}$ or $\overline{\text{DMWR}}$ goes low (with $\overline{\text{CS}}$ low) at any time during the CLK IN low-time immediately prior to the comparator strobing edge (t_{LOW} of Figure 4), the bit trial is suspended for a clock cycle. This makes sure that the bit decision is latched at a time when the AD7878 is not attempting to charge or discharge the data bus, thereby ensuring that no spurious transients occur internally near a bit decision point.

The decision point slippage mechanism is shown in Figure 4 for the MSB decision. Normally, the MSB decision occurs 25 ns after the fourth rising CLK IN edge after $\overline{\text{CONVST}}$ goes high. However, in the timing diagram of Figure 4, $\overline{\text{CS}}$ and $\overline{\text{DMRD}}$ or $\overline{\text{DMWR}}$ are low in the time period t_{LOW} prior to the MSB decision point on the fourth rising edge. This causes the internal comparator strobe to be slipped to the fifth rising clock edge. The AD7878 will again check during a period t_{LOW} prior to this fifth rising clock edge; and if the $\overline{\text{CS}}$ and $\overline{\text{DMRD}}$ or $\overline{\text{DMWR}}$ are still low, the bit decision point will be slipped a further clock cycle.

The conversion time for the ADC normally consists of the 13-bit trials described above and one extra internal clock cycle during which data is written from the SAR to the FIFO. For an 8 MHz input clock this results in a conversion time of 7 μs. However, the software routine servicing the AD7878 has the potential to read 16 times from the device during conversion – 8 reads from the FIFO and 8 reads from the status/control register. It also has the potential to write once to the status/control register. If these 17 (16 read plus 1 write) operations all occur during t_{LOW} time periods, the conversion time will slip by 17 CLK IN cycles. Therefore, if read or write operations can occur during t_{LOW} periods, it means that the conversion time for the ADC can vary from 7 μs to 9.12 μs (assuming 8 MHz CLK IN). This calculation assumes that there is a slippage of one CLK IN cycle for each read or write operation.

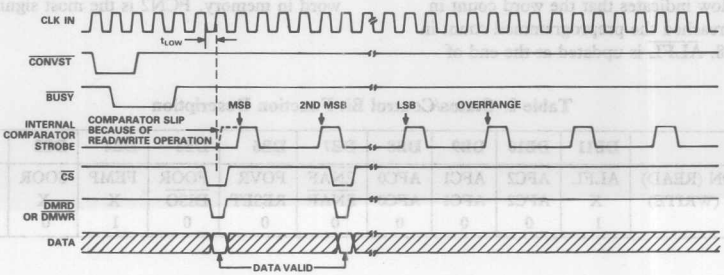


Figure 4. Operational Timing Diagram

INITIATING A CONVERSION

Conversion is initiated on the AD7878 by asserting the $\overline{\text{CONVST}}$ input. This $\overline{\text{CONVST}}$ input is an asynchronous input independent of either the ADC or DSP clocks. This is essential for applications where precise sampling in time is important. In these applications the signal sampling must occur at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. In these cases the $\overline{\text{CONVST}}$ input is driven from a timer or some precise clock source. On receipt of a $\overline{\text{CONVST}}$ pulse, the AD7878 acknowledges by taking the $\overline{\text{BUSY}}$ output low. This $\overline{\text{BUSY}}$ output can be used to ensure no bus activity while the track/hold goes from track to hold mode (see Extended Read-/Write section). The $\overline{\text{CONVST}}$ input must stay low for at least two CLK IN periods. The track/hold amplifier switches from the track to hold mode on the rising edge of $\overline{\text{CONVST}}$ and conversion is also initiated at this point. The $\overline{\text{BUSY}}$ output returns high after the $\overline{\text{CONVST}}$ input goes high and the ADC begins its successive approximation routine. Once conversion has been initiated another conversion start should not be attempted until the full conversion cycle has been completed. Figure 5 shows the timing diagram for the conversion start.

In applications where precise sampling is not critical, the $\overline{\text{CONVST}}$ pulse can be generated from a microprocessor $\overline{\text{WR}}$ or $\overline{\text{RD}}$ line gated with a decoded address (different to the AD7878 $\overline{\text{CS}}$ address). Note that the $\overline{\text{CONVST}}$ pulse width must be a minimum of two AD7878 CLK IN cycles.

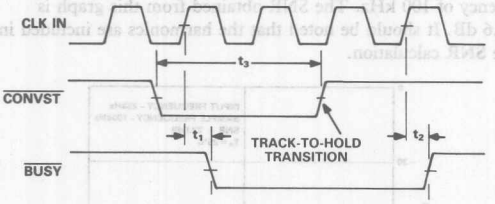


Figure 5. Conversion Start Timing Diagram

READ/WRITE OPERATIONS

The AD7878 read/write operations consist of reading from the FIFO memory and reading and writing from the status/control register. These operations are controlled by the $\overline{\text{CS}}$, $\overline{\text{DMRD}}$, $\overline{\text{DMWR}}$ and ADD0 logic inputs. A description of these operations is given in the following sections. In addition to the basic read/write operations there is an extended read/write operation. This can occur if a read/write operation occurs during a $\overline{\text{CONVST}}$ pulse. This extended read/write is intended for use with microprocessors that can be driven into a WAIT state, and the scheme is recommended for applications where an external timer controls the $\overline{\text{CONVST}}$ input asynchronously to the microprocessor read/write operations.

Basic Read Operation

Figure 6 shows the timing diagram for a basic read operation on the AD7878. $\overline{\text{CS}}$ and $\overline{\text{DMRD}}$ going low accesses data from either the status/control register or the FIFO memory. A read operation with ADD0 low accesses data from the FIFO while a read with ADD0 high accesses data from the status/control register.

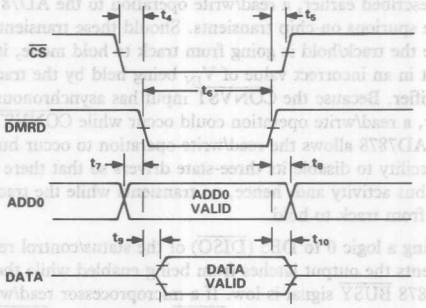


Figure 6. Basic Read Operation

Basic Write Operation

A basic write operation to the AD7878 status/control register consists of bringing $\overline{\text{CS}}$ and $\overline{\text{DMWR}}$ low with ADD0 high. Internally these signals are gated with CLK IN to provide an internal REGISTER ENABLE signal (see Figure 7). The pulse width of this REGISTER ENABLE signal is effectively the overlap between the CLK IN low time and the $\overline{\text{DMWR}}$ pulse. This may result in shorter write pulse widths, data setup times and data hold times than those given by the microprocessor. The timing on the AD7878 timing diagram of Figure 8 is therefore given with respect to the internal REGISTER ENABLE signal rather than the $\overline{\text{DMWR}}$ signal.

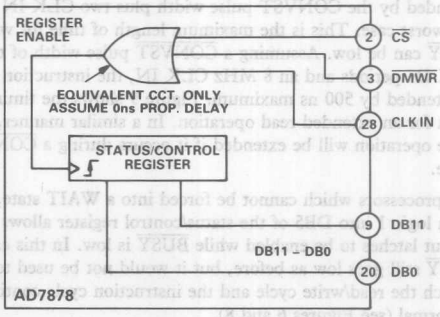


Figure 7. $\overline{\text{DMWR}}$ Internal Logic

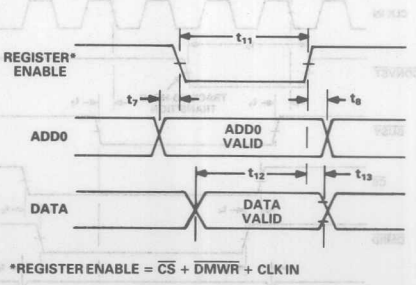


Figure 8. Basic Write Operation

Extended Read/Write Operation

As described earlier, a read/write operation to the AD7878 can cause spurious on-chip transients. Should these transients occur while the track/hold is going from track to hold mode, it may result in an incorrect value of V_{IN} being held by the track/hold amplifier. Because the $\overline{CONVST}$ input has asynchronous capability, a read/write operation could occur while $\overline{CONVST}$ is low. The AD7878 allows the read/write operation to occur but has the facility to disable its three-state drivers so that there is no data bus activity and, hence, no transients while the track/hold goes from track to hold.

Writing a logic 0 to DB5 ($\overline{DISO}$) of the status/control register prevents the output latches from being enabled while the AD7878 $\overline{BUSY}$ signal is low. If a microprocessor read/write operation can occur during the $\overline{BUSY}$ low time, the $\overline{BUSY}$ should be gated with $\overline{CS}$ of the AD7878 and this gated signal used to stretch the instruction cycle using DMACK (ADSP-2100), READY (TMS32020) or $\overline{DTACK}$ (68000).

When $\overline{CONVST}$ goes low, the AD7878 acknowledges it by bringing $\overline{BUSY}$ low on the next rising edge of CLK IN. With a logic 0 in DB5, the AD7878 data bus cannot now be enabled. If a read/write operation now occurs, the $\overline{BUSY}$ and $\overline{CS}$ gated signal drives the microprocessor into a WAIT state, thereby extending the read/write operation. $\overline{BUSY}$ goes high on the second rising edge of CLK IN after $\overline{CONVST}$ goes high. The AD7878 data outputs are now enabled and the microprocessor is released from its WAIT state, allowing it to complete its read/write operation to the AD7878.

The microprocessor cycle time for the read/write operation is extended by the $\overline{CONVST}$ pulse width plus two CLK IN periods worst case. This is the maximum length of time for which $\overline{BUSY}$ can be low. Assuming a $\overline{CONVST}$ pulse width of two CLK IN periods and an 8 MHz CLK IN, the instruction cycle is extended by 500 ns maximum. Figure 9 shows the timing diagram for an extended read operation. In a similar manner, a write operation will be extended if it occurs during a $\overline{CONVST}$ pulse.

For processors which cannot be forced into a WAIT state, writing a logic 1 into DB5 of the status/control register allows the output latches to be enabled while $\overline{BUSY}$ is low. In this case $\overline{BUSY}$ still goes low as before, but it would not be used to stretch the read/write cycle and the instruction cycle continues as normal (see Figures 6 and 8).

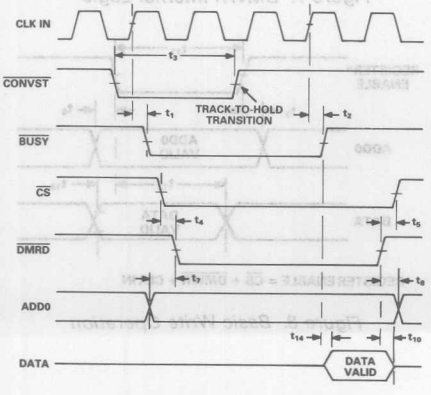


Figure 9. Extended Read Operation

AD7878 DYNAMIC SPECIFICATIONS

The AD7878 is specified and 100% tested for dynamic performance specifications rather than for traditional dc specifications such as Integral and Differential Nonlinearity. These ac specifications provide information on the AD7878's effect on the spectral content of the input signal. Hence, the parameters for which the AD7878 is specified include SNR, Harmonic Distortion, Intermodulation Distortion and Peak Harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal-to-noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals (excluding dc) up to half the sampling frequency (fs/2). SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-noise ratio for a sine wave input is given by

$$SNR = (6.02\,N + 1.76)\,dB \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

where N is the number of bits. Thus for an ideal 12-bit converter, SNR = 74 dB.

The output spectrum from the ADC is evaluated by applying a sine-wave signal of very low distortion to the V_{IN} input, which is sampled at a 100 kHz sampling rate. A Fast Fourier Transform (FFT) plot is generated from which the SNR data can be obtained. Figure 10 shows a typical 2048 point FFT plot of the AD7878KN with an input signal of 25 kHz and a sampling frequency of 100 kHz. The SNR obtained from this graph is 72.6 dB. It should be noted that the harmonics are included in the SNR calculation.

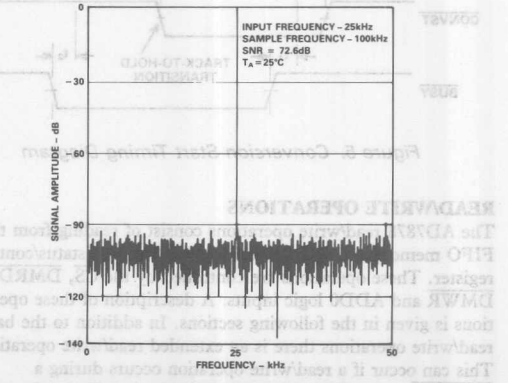


Figure 10. AD7878 FFT Plot

Effective Number of Bits

The formula given in (1) relates the SNR to the number of bits. Rewriting the formula, as in (2), it is possible to get a measure of performance expressed in effective number of bits (N). The effective number of bits for a device can be calculated directly from its measured SNR.

$$N = \frac{SNR - 1.76}{6.02} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

Figure 11 shows a typical plot of effective number of bits versus frequency for an AD7878KN with a sampling frequency of 100 kHz. The effective number of bits typically falls between 11.7 and 11.85 corresponding to SNR figures of 72.2 and 73.1 dB.

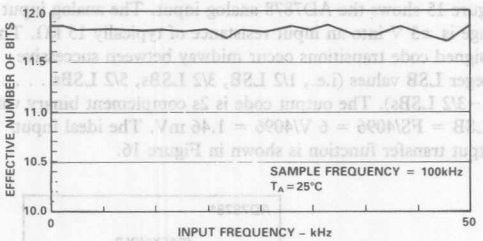


Figure 11. Effective Number of Bits vs. Frequency

Harmonic Distortion

Harmonic Distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7878, Total Harmonic Distortion (THD) is defined as:

$$THD = 20\ Log \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second to the sixth harmonic. The THD is also derived from the FFT plot of the ADC output spectrum.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa±nfb where m, n = 0,1,2,3 . . . . , etc. Intermodulation terms are those for which neither m nor n is equal to zero. For example, the second order terms include (fa+fb) and (fa−fb) while the third order terms include (2fa+fb), (2fa−fb), (fa+2fb) and (fa−2fb).

Using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Intermodulation distortion is calculated using an FFT algorithm but, in this case, the input consists of two equal amplitude, low distortion sine waves. Figure 12 shows a typical IMD plot for the AD7878.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to fs/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor the largest peak will be a noise peak.

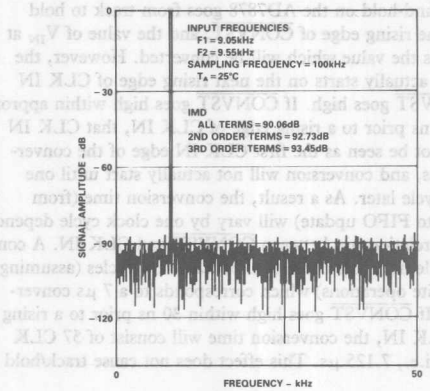


Figure 12. AD7878 IMD Plot

Histogram Plot

When a sine wave of a specified frequency is applied to the V_{IN} input of the AD7878 and several million samples are taken, it is possible to plot a histogram showing the frequency of occurrence of each of the 4096 ADC codes. If a particular step is wider than the ideal 1 LSB width, then the code associated with that step will accumulate more counts than for the code for an ideal step. Likewise, a step narrower than ideal will have fewer counts. Missing codes are easily seen in the histogram plot because a missing code means zero counts for a particular code. Large spikes in the plot indicate large differential nonlinearity.

Figure 13 shows a histogram plot for the AD7878KN with a sampling frequency of 100 kHz and an input frequency of 25 kHz. For a sine-wave input, a perfect ADC would produce a cusp probability density function described by the equation:

$$p\ (V) = \frac{1}{\pi\sqrt{(A^2 - V^2)}}$$

where A is the peak amplitude of the sine wave and p (V) is the probability of occurrence at a voltage V. The histogram plot of Figure 13 corresponds very well with this cusp shape. The absence of large spikes in this plot indicates small dynamic differential nonlinearity (the largest spike in the plot represents less than 1/4 LSB of DNL error). The AD7878 has no missing codes under these conditions since no code records zero counts.

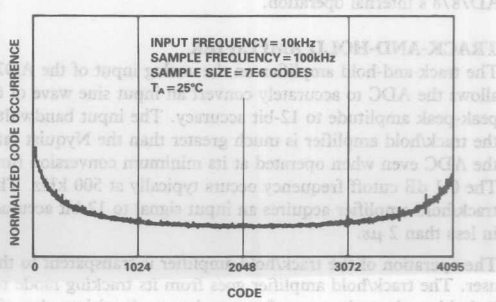


Figure 13. AD7878 Histogram Plot

mode on the rising edge of $\overline{\text{CONVST}}$, and the value of V_{IN} at this point is the value which will be converted. However, the conversion actually starts on the next rising edge of CLK IN after $\overline{\text{CONVST}}$ goes high. If $\overline{\text{CONVST}}$ goes high within approximately 30 ns prior to a rising edge of CLK IN, that CLK IN edge will not be seen as the first CLK IN edge of the conversion process, and conversion will not actually start until one CLK IN cycle later. As a result, the conversion time (from $\overline{\text{CONVST}}$ to FIFO update) will vary by one clock cycle depending on the relationship between $\overline{\text{CONVST}}$ and CLK IN. A conversion cycle normally consists of 56 CLK IN cycles (assuming no read/write operations) which corresponds to a 7 μs conversion time. If $\overline{\text{CONVST}}$ goes high within 30 ns prior to a rising edge of CLK IN, the conversion time will consist of 57 CLK IN cycles, i.e., 7.125 μs. This effect does not cause track/hold jitter.

INTERNAL REFERENCE

The AD7878 has an on-chip temperature compensated buried Zener reference (see Figure 14) that is factory trimmed to 3 V ±1%. Internally, it provides both the DAC reference and the dc bias required for bipolar operation. The reference output is available (REF OUT) and is capable of providing up to 500 μA to an external load.

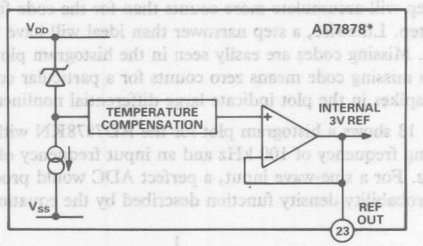


Figure 14. AD7878 Reference Circuit

The maximum recommended capacitance on REF OUT for normal operation is 50 pF. If the reference is required for use external to the AD7878, then it should be decoupled with a 200 Ω resistor in series with a parallel combination of a 10 μF tantalum capacitor and a 0.1 μF ceramic capacitor. These decoupling components are required to remove voltage spikes caused by the AD7878's internal operation.

TRACK-AND-HOLD AMPLIFIER

The track-and-hold amplifier on the analog input of the AD7878 allows the ADC to accurately convert an input sine wave of 6 V peak-peak amplitude to 12-bit accuracy. The input bandwidth of the track/hold amplifier is much greater than the Nyquist rate of the ADC even when operated at its minimum conversion time. The 0.1 dB cutoff frequency occurs typically at 500 kHz. The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 2 μs.

The operation of the track/hold amplifier is transparent to the user. The track/hold amplifier goes from its tracking mode to its hold mode at the start of conversion on the rising edge of $\overline{\text{CONVST}}$ and returns to track mode at the end of conversion.

range is ±3 V into an input resistance of typically 15 kΩ. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . . FS−3/2 LSBs). The output code is 2s complement binary with 1 LSB = FS/4096 = 6 V/4096 = 1.46 mV. The ideal input/output transfer function is shown in Figure 16.

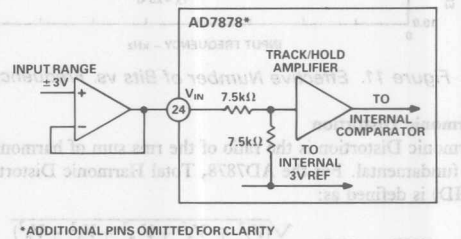


Figure 15. AD7878 Analog Input

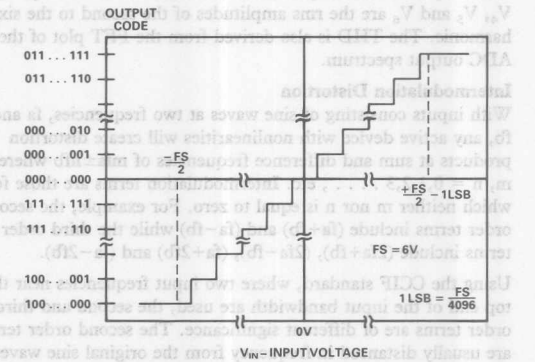


Figure 16. Input/Output Transfer Function

OFFSET AND FULL-SCALE ADJUSTMENT

In most Digital Signal Processing (DSP) applications offset and full-scale error have little or no effect on system performance. Offset error can always be eliminated in the analog domain by ac coupling. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. Some applications may require that the input signal span the full analog input dynamic range and, accordingly, offset and full-scale error will have to be adjusted to zero.

Where adjustment is required, offset must be adjusted before full-scale error. This is achieved by trimming the offset of the op amp driving the analog input of the AD7878 while the input voltage is 1/2 LSB below ground. The trim procedure is as follows: apply a voltage of −0.73 mV (−1/2 LSB) at V_1 and adjust the op amp offset voltage until the ADC output code flickers between 1111 1111 1111 and 0000 0000 0000.

Gain error can be adjusted at either the first code transition (ADC negative full scale) or the last code transition (ADC positive full scale). The trim procedures for both cases are as follows:

Positive Full-Scale Adjust

Apply a voltage of 2.9978 V (FS/2 − 3/2 LSBs) at V_1. Adjust

R2 until the ADC output code flickers between 0111 1111 1110 and 0111 1111 1111.

Negative Full-Scale Adjust

Apply a voltage of −2.9993 V (−FS/2 + 1/2 LSB) at V_1 and adjust R2 until the ADC output code flickers between 1000 0000 0000 and 1000 0000 0001.

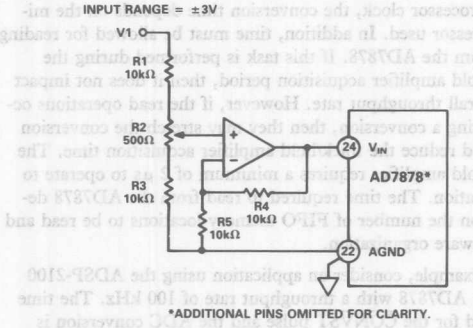


Figure 17. AD7878 Full-Scale Adjust Circuit

MICROPROCESSOR INTERFACING

The AD7878 high speed bus timing allows direct interfacing to DSP processors. Due to the complexity of the AD7878 internal logic, only synchronous interfacing is allowed. This means that the ADC clock must be the same as, or a derivative of, the processor clock. Suitable processor interfaces are shown in Figures 18 to 21.

AD7878–ADSP-2100/TMS32010/TMS32020

All three interfaces use an external timer for conversion control, allowing the ADC to sample the analog input asynchronously to the microprocessor. The AD7878 $\overline{ALFL}$ output interrupts the processor when the FIFO preprogrammed word count is reached. The processor then reads the conversion results from the AD7878 internal FIFO memory.

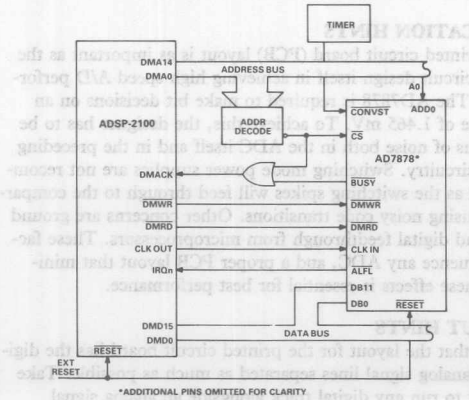


Figure 18. AD7878–ADSP-2100 Interface

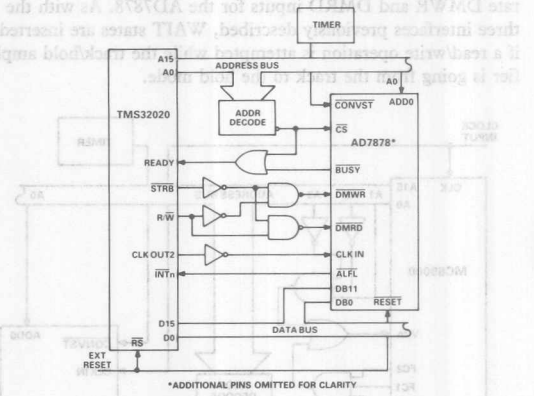


Figure 19. AD7878 – TMS32020 Interface

The interfaces to the ADSP-2100 and the TMS32020 gate the AD7878 $\overline{CS}$ and the $\overline{BUSY}$ to provide a signal which drives the processor into a wait state if a read/write operation to the ADC is attempted while the ADC track/hold amplifier is going from the track to the hold mode. This avoids digital feedthrough to the analog circuitry. The TMS32020 does not have separate $\overline{RD}$ and $\overline{WR}$ outputs to drive the AD7878 $\overline{DMWR}$ and $\overline{DMRD}$ inputs. These are generated from the processor $\overline{STRB}$ and R/$\overline{W}$ outputs with the addition of some logic gates.

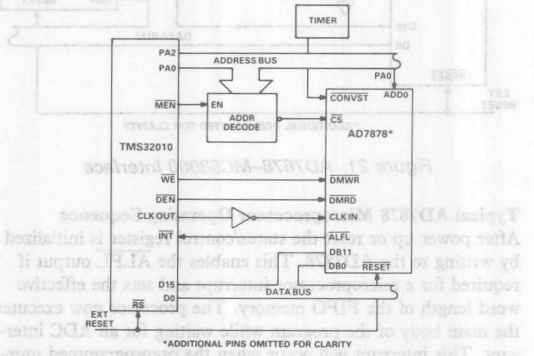


Figure 20. AD7878 – TMS32010 Interface

AD7878–MC68000

This interface also uses an external timer for conversion control as described for the previous three interfaces. It is discussed separately because it needs extra logic due to the nature of its interrupts. The MC68000 has eight levels of external interrupt. When interrupting this processor one of these levels (0 to 7) has to be encoded onto the $\overline{IPL2}$–$\overline{IPL0}$ inputs. This is achieved with a 74148 encoder in Figure 21, (interrupt Level 1 is taken for example purposes only). The MC68000 places this interrupt level on address bits A3 to A1 at the start of the interrupt service routine. Additional logic is used to decode this interrupt level on the address bus and the FC2–FC0 outputs to generate a $\overline{VPA}$ signal for the MC68000. This results in an autovectored interrupt, the start address for the service routine must be loaded into the appropriate auto vector location during initialization. For further information on the 68000 interrupts consult the 68000 user's manual.

The MC68000 $\overline{AS}$ and R/$\overline{W}$ outputs are used to generate separate $\overline{DMWR}$ and $\overline{DMRD}$ inputs for the AD7878. As with the three interfaces previously described, WAIT states are inserted if a read/write operation is attempted while the track/hold amplifier is going from the track to the hold mode.

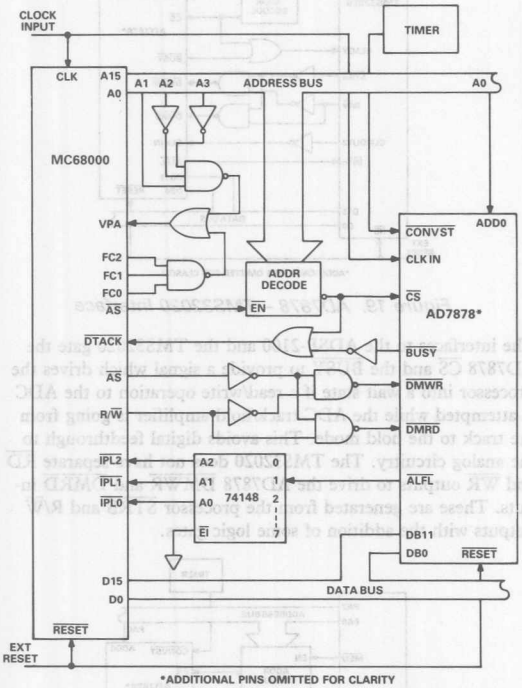


Figure 21. AD7878–MC68000 Interface

Typical AD7878 Microprocessor Operating Sequence

After power up or reset the status/control register is initialized by writing to the AD7878. This enables the $\overline{ALFL}$ output if required for a microprocessor interrupt and sets the effective word length of the FIFO memory. The processor now executes the main body of the program while waiting for an ADC interrupt. This interrupt will occur when the preprogrammed number of samples are collected in the FIFO memory. The interrupt service routine first interrogates DB5(FOOR) of the status/control register to determine if any sample in the FIFO memory is out of range. If all data samples are valid, then the program proceeds to read the FIFO memory. If, on the other hand, at least one sample is out of range, then an overrange routine is called.

There are many actions that can be taken by the out of range routine, the selection of which is application dependent. One option is to ignore all the current samples residing in the FIFO memory, reinitialize the status/control register and return to the main body of the program. Another option is to check the individual out of range status of each word in the FIFO memory and to discard the invalid ones. The underrange or overrange status of each word can also be determined and the analog input adjusted accordingly before returning to the main program.

Note there is no need to check the out of range status if the analog input is always assured to be within range.

THROUGHPUT RATE

The AD7878 has a maximum specified throughput rate (sample rate) of 100 kHz. This is a worst-case test condition and specifications apply for reduced sampling rates, provided that the Nyquist criterion is obeyed. The throughput rate must take into account ADC $\overline{CONVST}$ pulse width, ADC conversion time and the track/hold amplifier acquisition time. The time required for each of these tasks is shown in Table II for a selection of DSP processors. Since the ADC clock has to be synchronized to the microprocessor clock, the conversion time depends on the microprocessor used. In addition, time must be allowed for reading data from the AD7878. If this task is performed during the track/hold amplifier acquisition period, then it does not impact the overall throughput rate. However, if the read operations occur during a conversion, then they may stretch the conversion time and reduce the track/hold amplifier acquisition time. The track/hold amplifier requires a minimum of 2 μs to operate to specification. The time required to read from the AD7878 depends on the number of FIFO memory locations to be read and the software organization.

As an example, consider an application using the ADSP-2100 and the AD7878 with a throughput rate of 100 kHz. The time required for the $\overline{CONVST}$ pulse and the ADC conversion is 7.375 μs. This leaves 2.625 μs for the track/hold acquisition time and for reading the ADC (both operations occurring in parallel). The ADSP-2100, when operating from a 32 MHz clock, has an instruction cycle of 125 ns and an interrupt response time of 500 ns. This allows adequate time to perform 16 read operations within the time budget allowed.

Table II. AD7878 Throughput Rate

	$\overline{CONVST}$ Pulse Width	Conversion Time	T/H Acquisition Time
Number of Clock Cycles	2 min	57 max	Non-Applicable
ADSP-2100[1]	250 ns min	7.125 μs max	2 μs min
TMS32010[2]	400 ns min	11.14 μs max	2 μs min
TMS32020[2]	400 ns min	11.14 μs max	2 μs min

NOTES
[1]ADSP-2100 Clock Freq. = 32 MHz.
[2]TMS320XX Clock Freq. = 20 MHz.

APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the overall circuit design itself in achieving high speed A/D performance. The AD7878 is required to make bit decisions on an LSB size of 1.465 mV. To achieve this, the designer has to be conscious of noise both in the ADC itself and in the preceding analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through to the comparator, causing noisy code transitions. Other concerns are ground loops and digital feedthrough from microprocessors. These factors influence any ADC, and a proper PCB layout that minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground at Pin 22 (AGND) or as close as possible to the AD7878, as shown in Figure 22. Connect all other grounds and Pin 7 (AD7878 DGND) to this single analog ground point. Do not connect any other digital grounds to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise. The circuit layouts of Figures 25 and 26 have both analog and digital ground planes, which are kept separated and only joined together at the AD7878 AGND pin.

NOISE

Keep the input signal leads to V_{IN} and signal return leads from AGND (Pin 22) as short as possible to minimize input noise coupling. In applications where this is not possible, use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

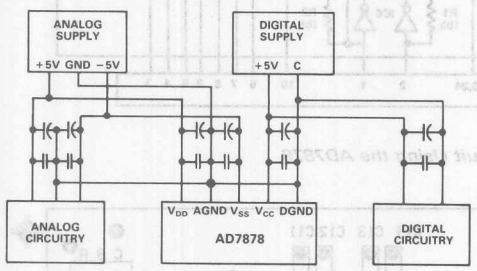


Figure 22. Power Supply Grounding Practice

DATA ACQUISITION BOARD

Figure 23 shows the AD7878 in a data acquisition circuit that will interface directly to either the ADSP-2100, TMS32010 or the TMS32020. The corresponding printed circuit board (PCB) layout and silkscreen are shown in Figures 24 to 26.

The only additional component required for a full data acquisition system is an antialiasing filter. There is a component grid provided near the analog input on the PCB which may be used for such a filter or any other conditioning circuitry. To facilitate this option, a wire link (labelled LK1 on the PCB) is required on the analog input track. This link connects the input signal to either the component grid or directly to the buffer amplifier driving the AD7878 analog input.

Microprocessor connections to the PCB can be made by either of two ways:

1. 96-contact (3 ROW) Eurocard connector.
2. 26-contact (2 ROW) IDC connector.

The 96-contact Eurocard connector is directly compatible with the ADSP-2100 Evaluation Board Prototype Expansion Connector. The expansion connector on the ADSP-2100 has eight decoded chip enable outputs labelled $\overline{ECE8}$ to $\overline{ECE1}$. $\overline{ECE6}$ is used to drive the AD7878 $\overline{CS}$ input on the data acquisition board. To avoid selecting onboard RAM sockets at the same time, LK6 on the ADSP-2100 board must be removed. In addition, the expansion connector on the ADSP-2100 has four interrupts labelled $\overline{EIRQ3}$ to $\overline{EIRQ0}$. The AD7878 $\overline{ALFL}$ output connects to $\overline{EIRQ0}$. The AD7878 and ADSP-2100 data lines are aligned for left justified data transfer.

The 26-way IDC connector contains all the necessary contacts for both the TMS32010 and TMS32020. There are two switches on the data acquisition board that must be set to enable the appropriate interface configuration (see Table III). The interface connections for the TMS32010/32020 and IDC signal contact numbers are shown in Table IV and Figure 23. Note the AD7878 $\overline{CS}$ input must be decoded from the address bus prior to the AD7878 evaluation board for the TMS320XX interfaces.

Connections to the analog input (V_{IN}) and the $\overline{CONVST}$ input are made via two BNC sockets labelled SKT1 and SKT2 on the silk-screen. If the $\overline{CONVST}$ input is derived from either the microprocessor or ADC clock, the effects of clock noise coupling will be reduced.

Table III. AD7878 PCB Switch Settings

SWITCH SETTING		
Microprocessor	**SW1**	**SW2**
ADSP-2100	A	A
TMS32010	B	A
TMS32020	B	B

POWER SUPPLY CONNECTIONS

The PCB requires two analog supplies and one 5 V digital supply. Connections to the analog supplies are made directly to the PCB as shown on the silk screen in Figure 24. The connections are labelled V+ and V− and the range for both of these supplies is 12 V to 15 V. Connection to the 5 V digital supply is made through either of the two microprocessor connectors. The +5 V and −5 V analog power supplies required by the AD7878 are generated from two voltage regulators on the V+ and V− power supply inputs (IC3 and IC4 in Figure 23).

COMPONENT LIST

IC1	AD711 Op Amp
IC2	AD7878 Analog-to-Digital Converter
IC3	MC78L05 5 V Regulator
IC4	MC79L05 −5 V Regulator
IC5*	74HC00 Quad NAND Gate
IC6*	74HC04 Hex Inverter
IC7	74HC02 Quad NOR Gate
SW1	Single Pole Double Throw
SW2	Double Pole Double Throw
LK1	Wire Link for Analog Input
C1, C3, C5, C7, C9 C11, C13, C15	10 μF Capacitors
C2, C4, C6, C8, C10 C12, C14, C16	0.1 μF Capacitors
R1*, R2*	10 kΩ Resistors
SKT1, SKT2	BNC Sockets
SKT3	26-Contact (2 Row) IDC Connector
SKT4	96-Contact (3 Row) Eurocard Connector

*Not required for ADSP-2100 Interface

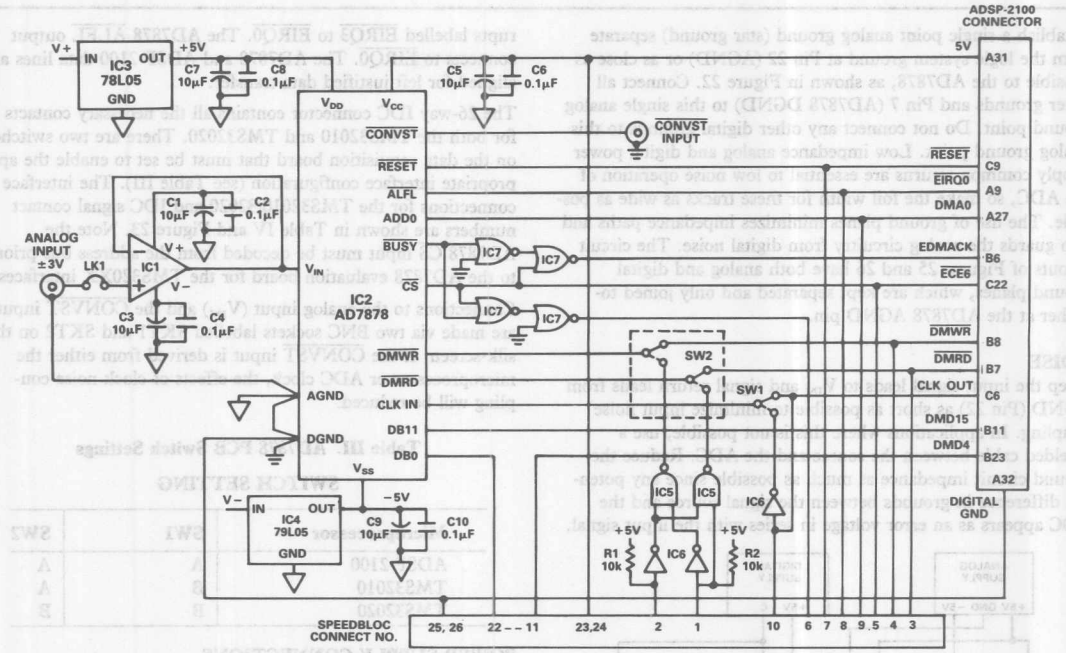


Figure 23. Data Acquisition Circuit Using the AD7878

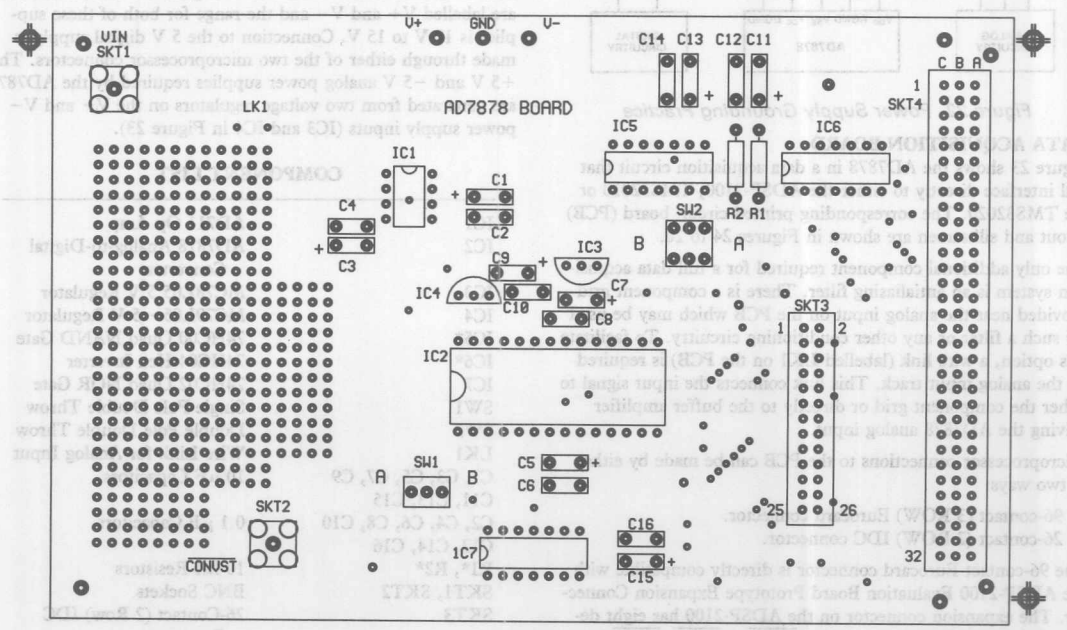


Figure 24. PCB Silkscreen for Figure 23

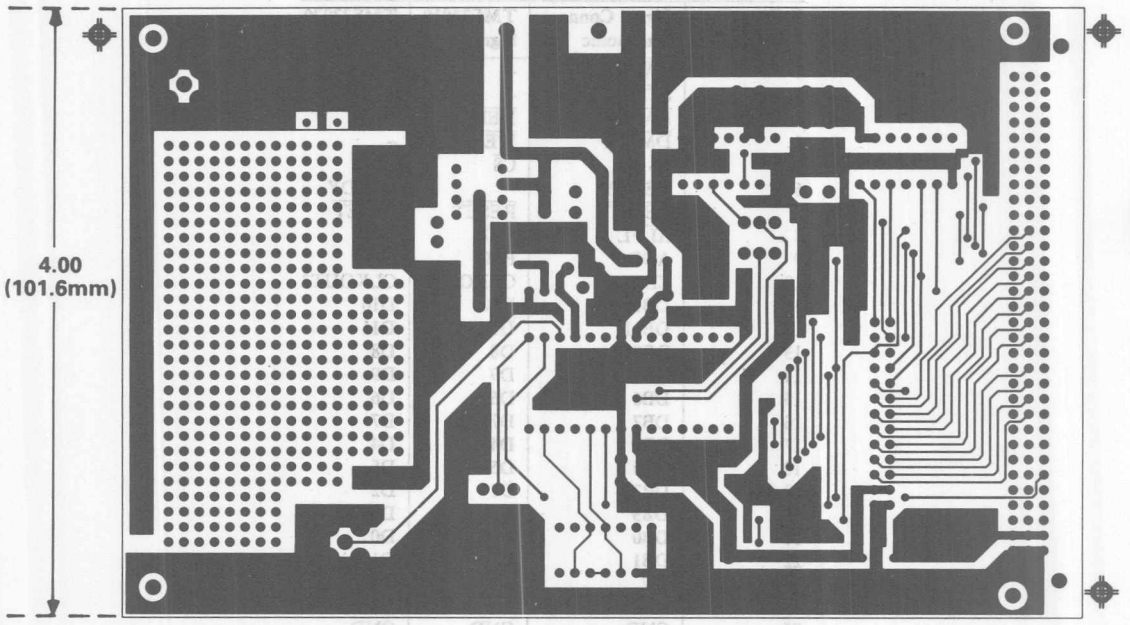


Figure 25. PCB Component Side Layout for Figure 23

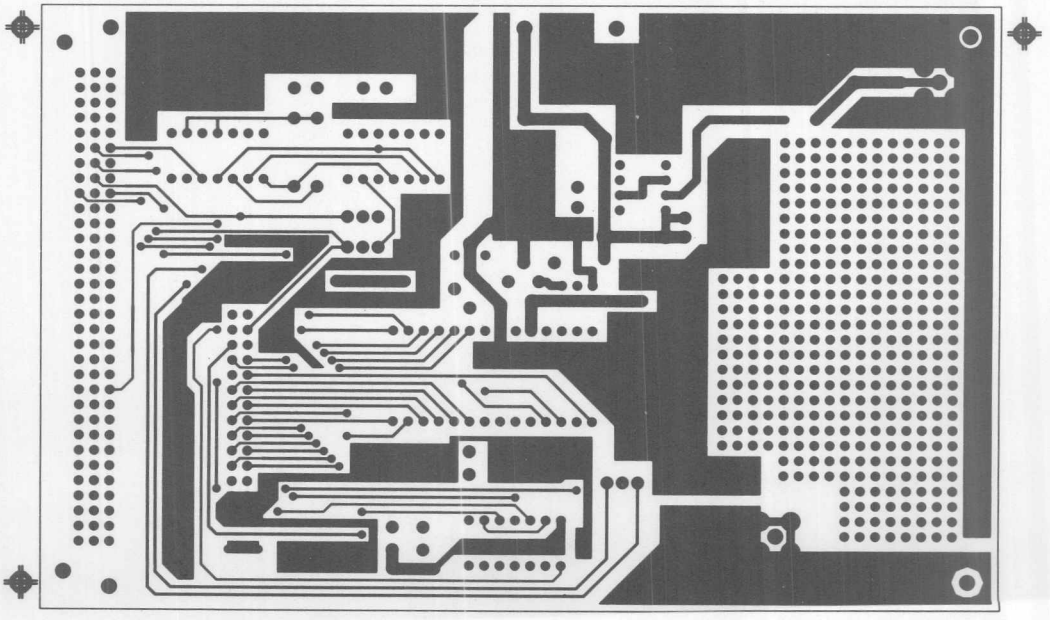
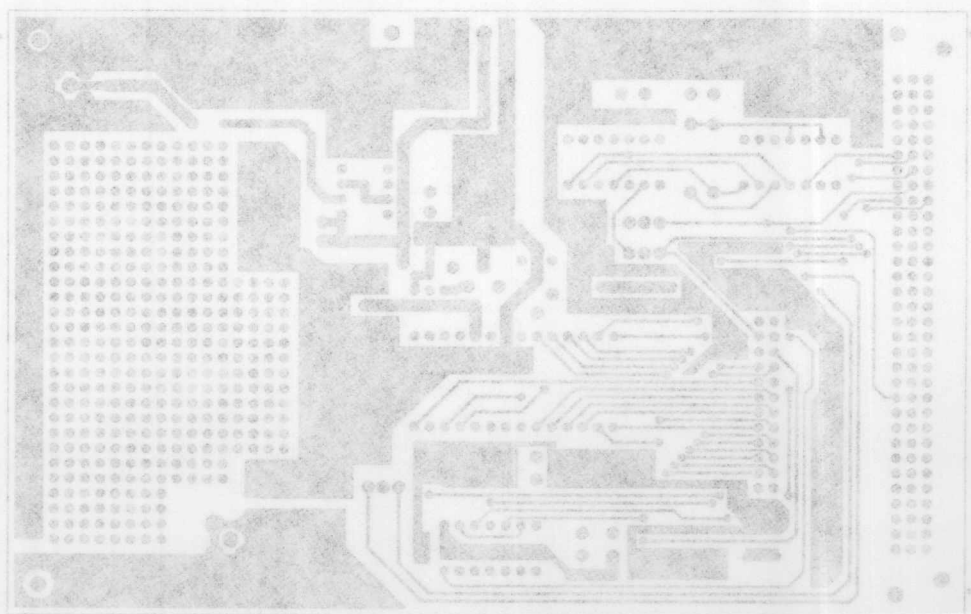


Figure 26. PCB Solder Side Layout for Figure 23

Table IV. TMS32010/TMS32020 Interface Connections

IDC Contact No.	Signal Connect Mnemonic	TMS32010 Signal	TMS32020 Signal
1	R/$\overline{W}$	–	R/$\overline{W}$
2	$\overline{STRB}$	–	$\overline{STRB}$
3	$\overline{DMRD}$	$\overline{DEN}$	–
4	$\overline{DMWR}$	$\overline{WE}$	–
5	$\overline{CS}$	$\overline{CS}$	$\overline{CS}$
6	READY	–	READY
7	$\overline{RESET}$	$\overline{RESET}$	$\overline{RESET}$
8	$\overline{ALFL}$	$\overline{INT}$	$\overline{INT}$
9	ADD0	PA0	A0
10	CLK	CLKOUT	CLKOUT2
11	DB10	D10	D10
12	DB11	D11	D11
13	DB8	D8	D8
14	DB9	D9	D9
15	DB6	D6	D6
16	DB7	D7	D7
17	DB4	D4	D4
18	DB5	D5	D5
19	DB2	D2	D2
20	DB3	D3	D3
21	DB0	D0	D0
22	DB1	D1	D1
23	5 V	5 V	5 V
24	5 V	5 V	5 V
25	GND	GND	GND
26	GND	GND	GND



LC²MOS, Single +5 V Supply, Low Power, 12-Bit Sampling ADC

AD7880

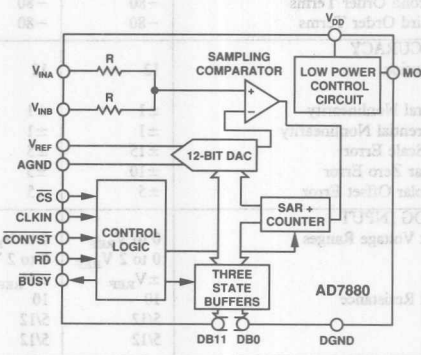
FEATURES

12-Bit Monolithic A/D Converter
66 kHz Throughput Rate
12 μs Conversion Time
3 μs On-Chip Track/Hold Amplifier
Low Power
Power Save Mode: 2 mW typ
Normal Operation: 25 mW typ
70 dB SNR
Fast Data Access Time: 57 ns
Small 24-Lead SOIC and 0.3" DIP Packages

APPLICATIONS

Battery Powered Portable Systems
Digital Signal Processing
Speech Recognition and Synthesis
High Speed Modems
Control and Instrumentation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7880 is a high speed, low power, 12-bit A/D converter which operates from a single +5 V supply. It consists of a 3 μs track/hold amplifier, a 12 μs successive-approximation ADC, versatile interface logic and a multiple-input-range circuit. The part also includes a power save feature.

An internal resistor network allows the part to accept both unipolar and bipolar input signals while operating from a single +5 V supply. Fast bus access times and standard control inputs ensure easy interfacing to modern microprocessors and digital signal processors.

The AD7880 features a total throughput time of 15 μs and can convert full power signals up to 33 kHz with a sampling frequency of 66 kHz.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7880 is also fully specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The AD7880 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin, 0.3 inch-wide, plastic or hermetic dual-in-line package (DIP) as well as a small 24-lead SOIC package.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time.
   12 μs conversion time and 3 μs acquisition time allow for large input signal bandwidth. This performance is ideally suited for applications in areas such as telecommunications, audio, sonar and radar signal processing.
2. Low Power Consumption.
   2 mW power consumption in the power-down mode makes the part ideally suited for portable, hand held, battery powered applications.
3. Multiple Input Ranges.
   The part features three user-determined input ranges, 0 to +5 V, 0 to 10 V and ±5 V. These unipolar and bipolar ranges are achieved with a 5 V only power supply.

AD7880—SPECIFICATIONS

(V_{DD} = +5 V ± 5%, V_{REF} = V_{DD}, AGND = DGND = 0 V, f_{CLKIN} = 2.5 MHz, MODE = V_{DD} unless otherwise noted. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	B Version[1]	C Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]				
Signal-to-Noise Ratio[3] (SNR)	70	70	dB min	Typically SNR Is 72 dB V_{IN} = 1 kHz Sine Wave, f_{SAMPLE} = 66 kHz
Total Harmonic Distortion (THD)	−80	−80	dB typ	V_{IN} = 1 kHz Sine Wave, f_{SAMPLE} = 66 kHz
Peak Harmonic or Spurious Noise	−80	−80	dB typ	V_{IN} = 1 kHz, f_{SAMPLE} = 66 kHz
Intermodulation Distortion (IMD)				
Second Order Terms	−80	−80	dB typ	fa = 0.983 kHz, fb = 1.05 kHz, f_{SAMPLE} = 66 kHz
Third Order Terms	−80	−80	dB typ	fa = 0.983 kHz, fb = 1.05 kHz, f_{SAMPLE} = 66 kHz
DC ACCURACY				
Resolution	12	12	Bits	All DC ACCURACY Specifications Apply for the Three Analog Input Ranges
Integral Nonlinearity	±1	±1	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
Full-Scale Error	±15	±5	LSB max	
Bipolar Zero Error	±10	±5	LSB max	
Unipolar Offset Error	±5	±5	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	Volts	See Figure 5
	0 to 2 V_{REF}	0 to 2 V_{REF}	Volts	See Figure 6
	±V_{REF}	±V_{REF}	Volts	See Figure 7
Input Resistance	10	10	MΩ min	0 to V_{REF} Range
	5/12	5/12	kΩ min/max	8 kΩ typical: 0 to 2V_{REF} Range
	5/12	5/12	kΩ min/max	8 kΩ typical: ±V_{REF} Range
REFERENCE INPUT				
V_{REF} (For Specified Performance)	5	5	V	±5%: Normally V_{REF} = V_{DD} (See Reference Input Section)
I_{REF}	1.5	1.5	mA max	
Nominal Reference Range	2.5/V_{DD}	2.5/V_{DD}	V min/max	See Figure 3 for Degradation in Performance Down to 2.5 V
LOGIC INPUTS				
$\overline{CONVST}$, $\overline{RD}$, $\overline{CS}$, CLKIN				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current, I_{IN}	±10	±10	μA max	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
MODE INPUT				
Input High Voltage, V_{INH}	4	4	V min	
Input Low Voltage, V_{INL}	1	1	V max	
Input Current, I_{IN}	±125	±125	μA max	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
LOGIC OUTPUTS				
DB11–DB0, $\overline{BUSY}$				
Output High Voltage, V_{OH}	4.0	4.0	V min	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0				
Floating-State Leakage Current	±10	±10	μA max	
Floating-State Output Capacitance[4]	10	10	pF max	
CONVERSION				
Conversion Time	12	12	μs max	f_{CLKIN} = 2.5 MHz
Track/Hold Acquisition Time	3	3	μs max	
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
I_{DD}				
Normal Power Mode @ +25°C	7.5	7.5	mA max	Typically 4 mA; MODE = V_{DD}
T_{min} to T_{max}	10	10	mA max	Typically 5 mA; MODE = V_{DD}
Power Save Mode @ +25°C	750	750	μA max	Logic Inputs @ 0 V or V_{DD}; MODE = 0 V
T_{min} to T_{max}	1	1	mA max	Logic Inputs @ 0 V or V_{DD}; MODE = 0 V
Power Dissipation				
Normal Power Mode @ +25°C	37.5	37.5	mW max	V_{DD} = 5 V: Typically 20 mW; MODE = V_{DD}
T_{min} to T_{max}	50	50	mW max	V_{DD} = 5 V: Typically 25 mW; MODE = V_{DD}
Power Save Mode @ +25°C	3.75	3.75	mW max	V_{DD} = 5 V: Typically 2 mW; MODE = 0 V
T_{min} to T_{max}	5	5	mW max	V_{DD} = 5 V: Typically 2.5 mW; MODE = 0 V

NOTES

[1]Temperature Ranges are as follows: B/C Versions, −40°C to +85°C.

[2]V_{IN} = 0 to V_{REF}.

[3]SNR calculation includes distortion and noise components.

[4]Sample tested @25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5 V ± 5%, V_{REF} = V_{DD}, AGND = DGND = 0 V)

Parameter	Limit at 25°C (All Versions)	Limit at T_{min}, T_{max} (All Versions)	Units	Conditions/Comments
t_1	50	50	ns min	$\overline{CONVST}$ Pulse Width
t_2	130	130	ns min	$\overline{CONVST}$ to $\overline{BUSY}$ Falling Edge
t_3	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Setup Time
t_4	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_5	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6	60	75	ns min	$\overline{RD}$ Pulse Width
t_7[2]	57	70	ns max	Data Access Time after $\overline{RD}$
t_8[3]	5	5	ns min	Bus Relinquish Time after $\overline{RD}$
	50	50	ns max	

NOTES

[1]Timing specifications in **bold** print are 100% production tested. All other times are sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]t_7 is measured with the load circuit of Figure 2 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[3]t_8 is derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

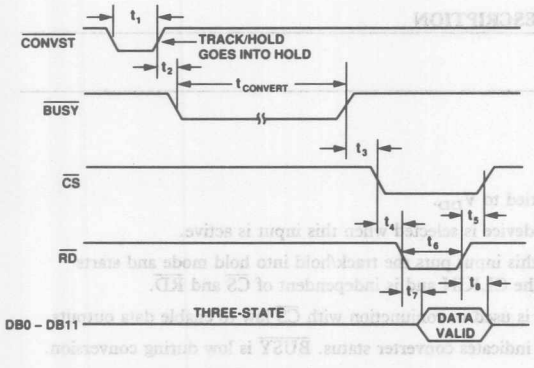


Figure 1. Timing Diagram

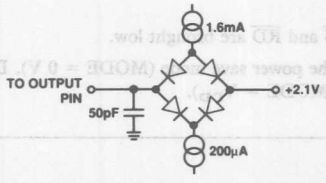


Figure 2. Load Circuit for Access and Relinquish Time

Table I. AD7880 Truth Table

$\overline{CS}$	$\overline{CONVST}$	$\overline{RD}$	Function
1	1	X	Not Selected
1	↓	1	Start Conversion ↓
0	1	0	Enable ADC Data
0	1	1	Data Bus Three Stated

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{DD} to DGND . . . . . −0.3 V to +7 V
AGND to DGND . . . . . −0.3 V to V_{DD} +0.3 V
V_{INA}, V_{INB} to AGND (Fig 5) . . . . . −0.3 V to V_{DD} +0.3 V
V_{INA} to AGND (Fig 6) . . . . . −0.6 V to 2 V_{DD} +0.6 V
V_{INA} to AGND(Fig 7) . . . . . $-V_{DD}$−0.3 V to V_{DD}+0.3 V
V_{REF} to AGND . . . . . 0.3 V to V_{DD}
Digital Inputs to DGND . . . . . −0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Industrial (B, C Versions) . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

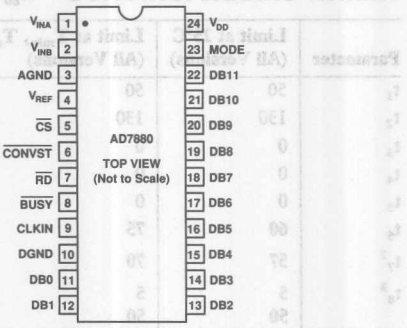


ORDERING GUIDE

Model	Temperature Range	Full-Scale Error (LSBs)	Bipolar Zero Error (LSBs)	Package Option*
AD7880BN	−40°C to +85°C	±15	±10	N-24
AD7880BQ	−40°C to +85°C	±15	±10	Q-24
AD7880CN	−40°C to +85°C	±5	±5	N-24
AD7880CQ	−40°C to +85°C	±5	±5	Q-24
AD7880BR	−40°C to +85°C	±15	±10	R-24
AD7880CR	−40°C to +85°C	±5	±5	R-24

*N = Plastic DIP; Q = Cerdip; R = SOIC (Small Outline Integrated Circuit). For outline information see Package Information section.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTION

Pin No.	Pin Mnemonic	Function
1	V_{INA}	Analog Input.
2	V_{INB}	Analog Input.
3	AGND	Analog Ground.
4	V_{REF}	Voltage Reference Input. This is normally tied to V_{DD}.
5	$\overline{CS}$	Chip Select. Active Low Logic input. The device is selected when this input is active.
6	$\overline{CONVST}$	Convert Start. A low to high transition on this input puts the track/hold into hold mode and starts conversion. This input is asynchronous to the CLKIN and is independent of $\overline{CS}$ and $\overline{RD}$.
7	$\overline{RD}$	Read. Active Low Logic Input. This input is used in conjunction with $\overline{CS}$ low to enable data outputs.
8	$\overline{BUSY}$	Active Low Logic Output. This status line indicates converter status. $\overline{BUSY}$ is low during conversion.
9	CLKIN	Clock Input. TTL-compatible logic input. Used as the clock source for the A/D converter. The mark/space ratio of the clock can vary from 40/60 to 60/40.
10	DGND	Digital Ground.
11 . . . 22	DB0–DB11	Three-State Data Outputs. These become active when $\overline{CS}$ and $\overline{RD}$ are brought low.
23	MODE	MODE Input. This input is used to put the device into the power save mode (MODE = 0 V). During normal operation, the MODE input will be a logic high (MODE = V_{DD}).
24	V_{DD}	Power Supply. This is nominally +5 V.

CIRCUIT INFORMATION

The AD7880 is a +5 V single supply 12-bit A/D converter. The part requires no external components apart from a 2.5 MHz external clock and power supply decoupling capacitors. It contains a 12-bit successive approximation ADC based on a fast-settling voltage-output DAC, a high speed comparator and SAR, as well as the necessary control logic. The charge balancing comparator used in the AD7880 provides the user with an inherent track-and-hold function. The ADC is specified to work with sampling rates up to 66 kHz.

CONVERTER DETAILS

The AD7880 conversion cycle is initiated on the rising edge of the $\overline{CONVST}$ pulse, as shown in the timing diagram of Figure 1. The rising edge of the $\overline{CONVST}$ pulse places the track/hold amplifier into "HOLD" mode. The conversion cycle then takes between 26 and 28 clock periods. The maximum specified conversion time is 12 μs. This corresponds to a conversion cycle time of 28 clock periods with a CLKIN frequency of 2.5 MHz and also includes internal propagation delays. During conversion the $\overline{BUSY}$ output will remain low, and the output databus drivers will be three-stated. When a conversion is completed, the $\overline{BUSY}$ output will go to a high level, and the result of the conversion can be read by bringing $\overline{CS}$ and $\overline{RD}$ low.

The track/hold amplifier acquires a 12-bit input signal in 3 μs. The overall throughput time for the AD7880 is equal to the conversion time plus the track/hold acquisition time. For a 2.5 MHz input clock the throughput time is 15 μs.

REFERENCE INPUT

For specified performance, it is recommended that the reference input be tied to V_{DD}. The part, however, will operate with a reference down to 2.5 V though with reduced performance specifications. Figure 3 shows a graph of signal-to-noise ratio (SNR) versus V_{REF}.

V_{REF} must not be allowed to go above V_{DD} by more than 100 mV.

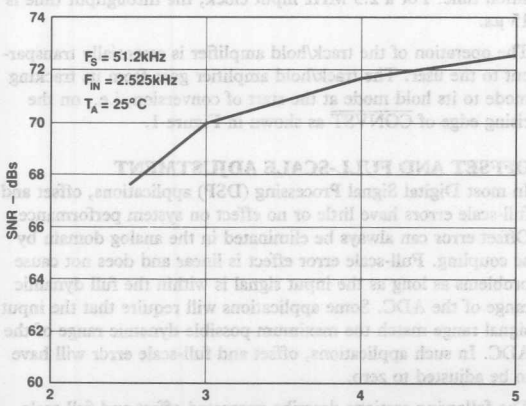


Figure 3. SNR Versus V_{REF}

ANALOG INPUT

The AD7880 has two analog input pins, V_{INA} and V_{INB}. Figure 4 shows the input circuitry to the ADC sampling comparator. The on-board attenuator network, made up of equal resistors, allows for various input ranges.

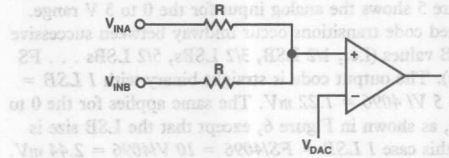


Figure 4. AD7880 Input Circuit

The AD7880 accommodates three separate input ranges, 0 to V_{REF}, 0 to 2 V_{REF} and $\pm V_{REF}$. The input configurations corresponding to these ranges are shown in Figures 5, 6 and 7.

With $V_{REF} = V_{DD}$ and using a nominal V_{DD} of +5 V, the input ranges are 0 to 5 V, 0 to 10 V and ±5 V, as shown in Table II.

Table II. Analog Input Ranges

Analog Input Range	V_{REF}	Input Connections		Connection Diagram
		V_{INA}	V_{INB}	
0 V to +5 V	V_{DD}	V_{IN}	V_{IN}	Figure 5
0 V to +10 V	V_{DD}	V_{IN}	AGND	Figure 6
±5 V	V_{DD}	V_{IN}	V_{REF}	Figure 7

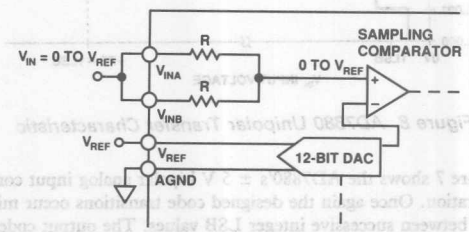


Figure 5. 0 to V_{REF} Unipolar Input Configuration

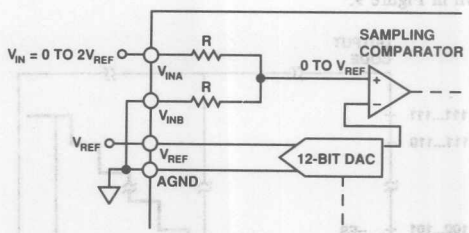


Figure 6. 0 to 2 V_{REF} Unipolar Input Configuration

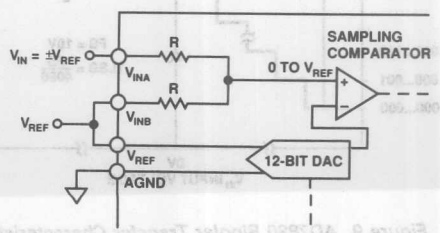


Figure 7. ±V_{REF} Bipolar Input Configuration

The AD7880 has two unipolar input ranges, 0 to 5 V and 0 to 10 V. Figure 5 shows the analog input for the 0 to 5 V range. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS −3/2 LSBs). The output code is straight binary with *1 LSB = FS/4096 = 5 V/ 4096 = 1.22 mV*. The same applies for the 0 to 10 V range, as shown in Figure 6, except that the LSB size is bigger. In this case *1 LSB = FS/4096 = 10 V/4096 = 2.44 mV*. The ideal input/output transfer characteristic for both these unipolar ranges is shown in Figure 8.

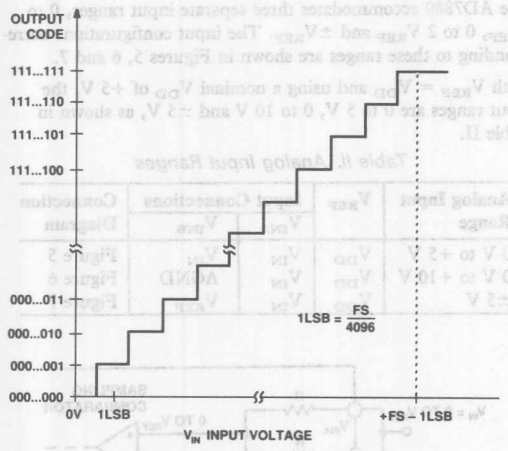


Figure 8. AD7880 Unipolar Transfer Characteristic

Figure 7 shows the AD7880's ± 5 V bipolar analog input configuration. Once again the designed code transitions occur midway between successive integer LSB values. The output code is straight binary with *1 LSB = FS/4096 = 10 V/4096 = 2.44 mV*. The ideal bipolar input/output transfer characteristic is shown in Figure 9.

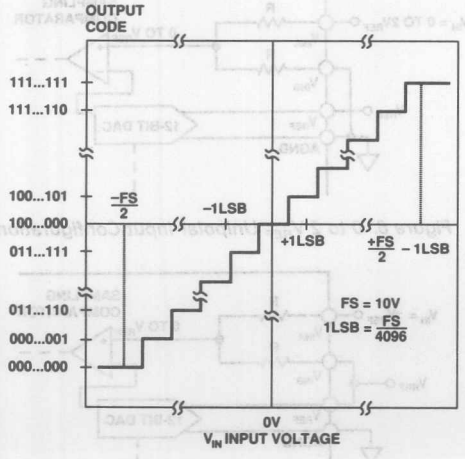


Figure 9. AD7880 Bipolar Transfer Characteristic

CLOCK INPUT

The AD7880 is specified to operate with a 2.5 MHz clock connected to the CLKIN input pin. This pin may be driven directly by CMOS or TTL buffers. The mark/space ratio on the clock can vary from 40/60 to 60/40. As the clock frequency is slowed down, it can result in slightly degraded accuracy performance. This is due to leakage effects on the hold capacitor in the internal track-and-hold amplifier. Figure 10 is a typical plot of accuracy versus clock frequency for the ADC.

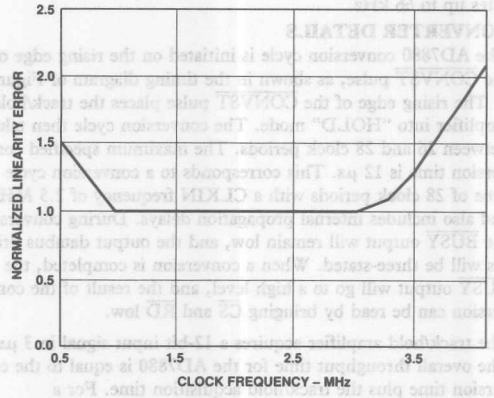


Figure 10. Normalized Linearity Error vs. Clock Frequency

TRACK/HOLD AMPLIFIER

The charge balanced comparator used in the AD7880 for the A/D conversion provides the user with an inherent track/hold function. The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 3 μs. The overall throughput time is equal to the conversion time plus the track/hold amplifier acquisition time. For a 2.5 MHz input clock, the throughput time is 15 μs.

The operation of the track/hold amplifier is essentially transparent to the user. The track/hold amplifier goes from its tracking mode to its hold mode at the start of conversion, i.e., on the rising edge of $\overline{\text{CONVST}}$ as shown in Figure 1.

OFFSET AND FULL-SCALE ADJUSTMENT

In most Digital Signal Processing (DSP) applications, offset and full-scale errors have little or no effect on system performance. Offset error can always be eliminated in the analog domain by ac coupling. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. Some applications will require that the input signal range match the maximum possible dynamic range of the ADC. In such applications, offset and full-scale error will have to be adjusted to zero.

The following sections describe suggested offset and full-scale adjustment techniques which rely on adjusting the inherent offset of the op amp driving the input to the ADC as well as tweaking an additional external potentiometer as shown in Figure 11.

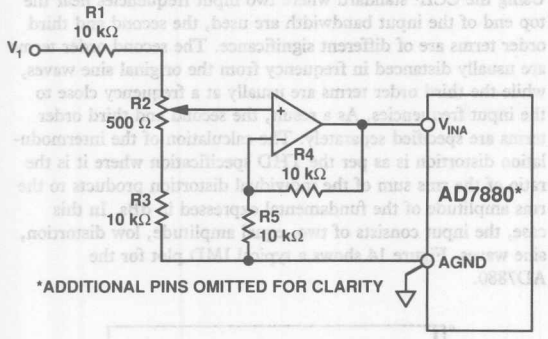


Figure 11. Offset and Full-Scale Adjust Circuit

Unipolar Adjustments

In the case of the 0 to 5 V unipolar input configuration, unipolar offset error must be adjusted before full-scale error. Adjustment is achieved by trimming the offset of the op amp driving the analog input of the AD7880. This is done by applying an input voltage of 0.61 mV (1/2 LSB) to V_1 in Figure 11 and adjusting the op amp offset voltage until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001. For full-scale adjustment, an input voltage of 4.9982 V (FS−3/2 LSBs) is applied to V_1 and R2 is adjusted until the output code flickers between 1111 1111 1110 and 111 1111 1111.

The same procedure is required for the 0 to 10 V input configuration of Figure 6. An input voltage of 1.22 mV (1/2 LSB) is applied to V_1 in Figure 11 and the op amp's offset voltage is adjusted until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001. For full-scale adjustment, an input voltage of 9.9963 V (FS−3/2 LSBs) is applied to V_1 and R2 is adjusted until the output code flickers between 1111 1111 1110 and 111 1111 1111.

Bipolar Adjustments

Bipolar zero and full-scale errors for the bipolar input configuration of Figure 7 are adjusted in a similar fashion to the unipolar case. Again, bipolar zero error must be adjusted before full-scale error. Bipolar zero error adjustment is achieved by trimming the offset of the op amp driving the analog input of the AD7880 while the input voltage is 1/2 LSB below ground. This is done by applying an input voltage of −1.22 mV (1/2 LSB) to V_1 in Figure 11 and adjusting the op amp offset voltage until the ADC output code flickers between 0111 1111 1111 and 1000 0000 0000. For full-scale adjustment, an input voltage of 4.9982 V(FS/2-3/2 LSBs) is applied to V1 and R2 is adjusted until the output code flickers between 1111 1111 1110 and 1111 1111 1111.

DYNAMIC SPECIFICATIONS

The AD7880 is specified and tested for dynamic performance specifications as well as traditional dc specifications such as integral and differential nonlinearity. The ac specifications are required for signal processing applications such as speech recognition, spectrum analysis and high speed modems. These applications require information on the ADC's effect on the spectral content of the input signal. Hence, the parameters for which the AD7880 is specified include SNR, harmonic distortion, intermodulation distortion and peak harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal-to-noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (FS/2) excluding dc. SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to noise ratio for a sine wave input is given by:

$$SNR = (6.02\ N + 1.76)\ dB \qquad (1)$$

where N is the number of bits.

Thus for an ideal 12-bit converter, SNR = 74 dB.

The output spectrum from the ADC is evaluated by applying a sine wave signal of very low distortion to the V_{IN} input which is sampled at a 66 kHz sampling rate. A Fast Fourier Transform (FFT) plot is generated from which the SNR data can be obtained. Figure 12 shows a typical 2048 point FFT plot of the AD7880 with an input signal of 2.5 kHz and a sampling frequency of 61 kHz. The SNR obtained from this graph is 73 dB. It should be noted that the harmonics are taken into account when calculating the SNR.

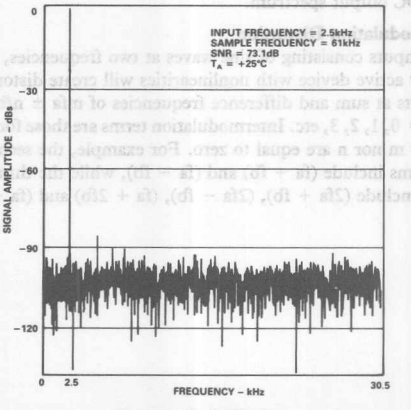


Figure 12. FFT Plot

Effective Number of Bits

The formula given in Equation 1 relates the SNR to the number of bits. Rewriting the formula, as in Equation 2, it is possible to get a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \qquad (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR.

Figure 13 shows a plot of effective number of bits versus input frequency for an AD7880 with a sampling frequency of 61 kHz. The effective number of bits typically remains better than 11.5 for frequencies up to 12 kHz.

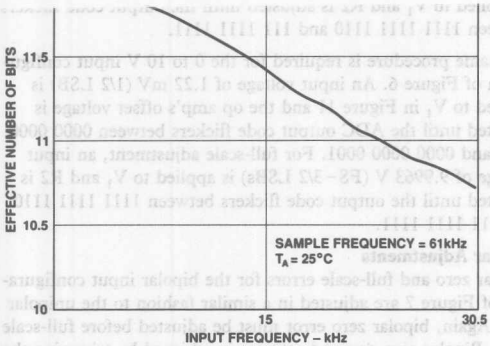


Figure 13. Effective Number of Bits vs. Frequency

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of harmonics to the rms value of the fundamental. For the AD7880, THD is defined as:

$$THD = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1} \quad (3)$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonic. The THD is also derived from the FFT plot of the ADC output spectrum.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa − fb), while the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb).

top end of the input bandwidth are used, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs. In this case, the input consists of two, equal amplitude, low distortion, sine waves. Figure 14 shows a typical IMD plot for the AD7880.

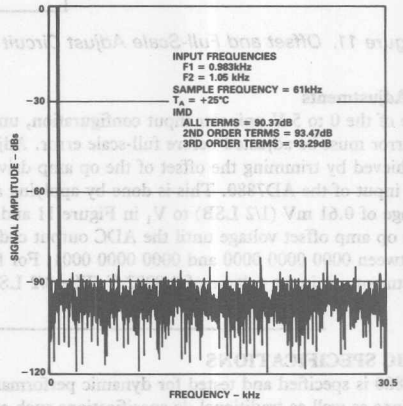


Figure 14. IMD Plot

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to FS/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor the peak will be a noise peak.

MICROPROCESSOR INTERFACING

The AD7880 high speed bus timing allows direct interfacing to real time digital signal processors, DSPs, as well as modern high speed, 16-bit microprocessors. Suitable microprocessor interfaces are shown in Figures 15 through 20.

AD7880–ADSP-2100 Interface

Figure 15 shows an interface between the AD7880 and the ADSP-2100. Conversion is initiated using a timer to drive the $\overline{\text{CONVST}}$ input asynchronously to the microprocessor. This allows very accurate control of the sampling instant. When conversion is complete, the AD7880 $\overline{\text{BUSY}}$ line goes high. An inverter on this $\overline{\text{BUSY}}$ output drives the $\overline{\text{IRQ}}$ line low thus providing an interrupt to the ADSP-2100 when conversion is completed. The conversion result is then read from the AD7880 into the ADSP-2100 with the following instruction:

MR0 = DM(ADC)

where *MR0* is the ADSP-2100 MR0 Register and
ADC is the AD7880 address.

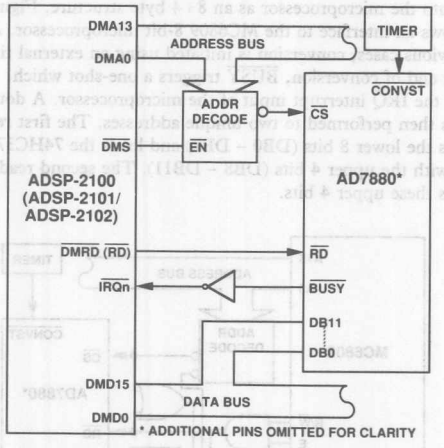


Figure 15. AD7880–ADSP-2100 (ADSP-2101/ADSP-2102) Interface

AD7880–ADSP-2101/ADSP-2102 Interface

The interface outlined in Figure 15 also forms the basis for an interface between the AD7880 and the ADSP-2101/ADSP-2102. The READ line of the ADSP-2101/ADSP-2102 is labeled $\overline{\text{RD}}$. In this interface, the $\overline{\text{RD}}$ pulse width of the processor can be programmed using the Data Memory Wait State Control Register. The instruction used to read a conversion result is as outlined for the ADSP-2100.

AD7880-TMS32010 Interface

An interface between the AD7880 and the TMS32010 is shown in Figure 16. Once again the conversion is initiated using an external timer and the TMS32010 is interrupted when conversion is completed. The following instruction is used to read the conversion result from the AD7880:

IN D,ADC

where *D* is Data Memory Address and
ADC is the AD7880 address.

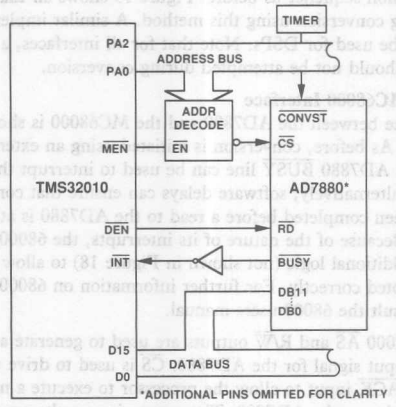


Figure 16. AD7880–TMS32010 Interface

AD7880–TMS320C25 Interface

Figure 17 shows an interface between the AD7880 and the TMS320C25. As with the two previous interfaces, conversion is initiated with a timer, and the processor is interrupted when the conversion sequence is completed. The TMS320C25 does not have a separate $\overline{\text{RD}}$ output to drive the AD7880 $\overline{\text{RD}}$ input directly. This has to be generated from the processor $\overline{\text{STRB}}$ and R/$\overline{\text{W}}$ outputs with the addition of some logic gates. The $\overline{\text{RD}}$ signal is OR-gated with the $\overline{\text{MSC}}$ signal to provide the one WAIT state required in the read cycle for correct interface timing. Conversion results are read from the AD7880 using the following instruction:

IN D,ADC

where *D* is Data Memory Address and
ADC is the AD7880 address.

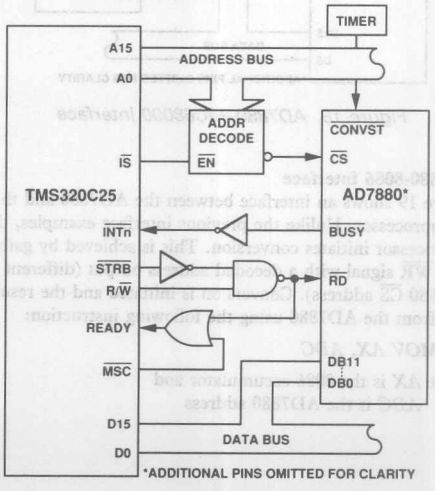


Figure 17. AD7880–TMS320C25 Interface

Some applications may require that the conversion be initiated by the microprocessor rather than an external timer. One option is to decode the AD7880 $\overline{\text{CONVST}}$ from the address bus so that

a write operation starts a conversion. Data is read at the end of the conversion sequence as before. Figure 19 shows an example of initiating conversion using this method. A similar implementation can be used for DSPs. Note that for all interfaces, a read operation should not be attempted during conversion.

AD7880–MC68000 Interface

An interface between the AD7880 and the MC68000 is shown in Figure 18. As before, conversion is initiated using an external timer. The AD7880 $\overline{BUSY}$ line can be used to interrupt the processor or, alternatively, software delays can ensure that conversion has been completed before a read to the AD7880 is attempted. Because of the nature of its interrupts, the 68000 requires additional logic (not shown in Figure 18) to allow it to be interrupted correctly. For further information on 68000 interrupts, consult the 68000 users manual.

The MC68000 $\overline{AS}$ and R/$\overline{W}$ outputs are used to generate a separate $\overline{RD}$ input signal for the AD7880. $\overline{CS}$ is used to drive the 68000 $\overline{DTACK}$ input to allow the processor to execute a normal read operation to the AD7880. The conversion results are read using the following 68000 instruction:

MOVE.W ADC, D0

where *D0* is the 68000 D0 register and
ADC is the AD7880 address

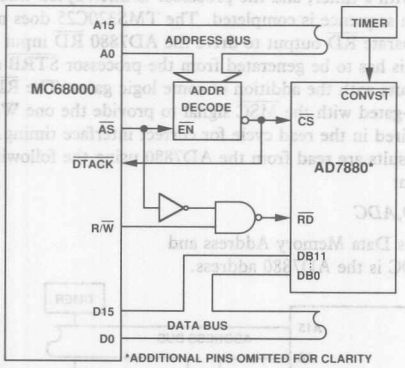


Figure 18. AD7880–MC68000 Interface

AD7880-8086 Interface

Figure 19 shows an interface between the AD7880 and the 8086 microprocessor. Unlike the previous interface examples, the microprocessor initiates conversion. This is achieved by gating the 8086 $\overline{WR}$ signal with a decoded address output (different to the AD7880 $\overline{CS}$ address). Conversion is initiated and the result is read from the AD7880 using the following instruction:

MOV AX, ADC

where *AX* is the 8086 accumulator and
ADC is the AD7880 address

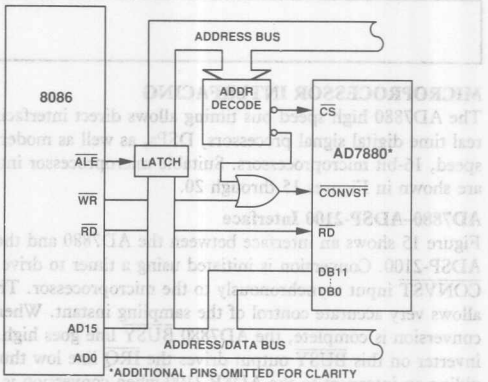


Figure 19. AD7880–8086 Interface

AD7880-6809 Interface

The AD7880 can also interface quite easily with 8-bit microprocessors. The 12-bit parallel data output from the AD7880 can be read into the microprocessor as an 8+4 byte structure. Figure 20 shows an interface to the MC6809 8-bit microprocessor. As in previous cases, conversion is initiated using an external timer. At the end of conversion, $\overline{BUSY}$ triggers a one-shot which drives the $\overline{IRQ}$ interrupt input of the microprocessor. A double read is then performed to two unique addresses. The first read fetches the lower 8 bits (DB0 – DB7) and loads the 74HC374 latch with the upper 4 bits (DB8 – DB11). The second read fetches these upper 4 bits.

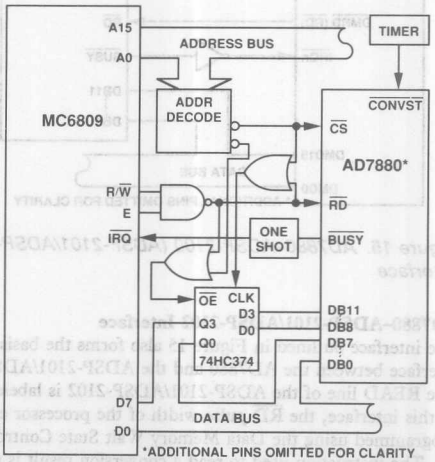


Figure 20. AD7880–6809 Interface

Good printed circuit board (PCB) layout is as important as the circuit design itself in achieving high speed A/D performance. The AD7880's comparator is required to make bit decisions on an LSB size of 1.22 mV. To achieve this, the designer must be conscious of noise both in the ADC itself and in the preceding analog circuitry. Switching mode power supplies are not recommended, as the switching spikes will feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any ADC, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run digital tracks alongside analog signal tracks. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground at the AD7880 AGND pin or as the AD7880 DGND to this single analog ground point. Do not connect any other digital grounds to this analog ground point.

Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise. The circuit layout of Figures 26 and 27 have both analog and digital ground planes which are kept separated and only joined together at the AD7880 AGND pin.

NOISE

Keep the input signal leads to V_{IN} and signal return leads from AGND as short as possible to minimize input noise coupling. In applications where this is not possible, use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

ANALOG INPUT BUFFERING

To achieve specified performance, it is recommended that the analog input (V_{INA}, V_{INB}) be driven from a low impedance source. This necessitates the use of an input buffer amplifier. The choice of op amp will be a function of the particular application and the desired analog input range. The data acquisition circuit, described in this data sheet allows for various op amp configurations. Figure 21 shows the analog input buffer circuit.

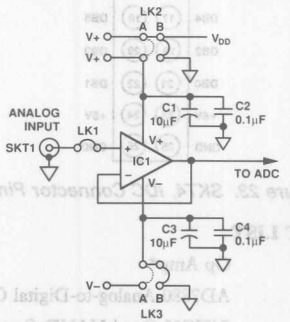


Figure 21. Analog Input Buffering

The options available to drive the supply of the op amp are:

Single +5 V (derived from PCB 5 V supply)

Dual Supply (externally supplied to V+ and V−)
±5 V, ±12 V or ±15 V

The simplest configuration is the 0 to 5 V range of Figure 5. A single supply 5 V op amp is recommended for such an implementation. This will allow for operation of the AD7880 in the 0 to 5 V unipolar range without supplying an external supply to V+ and V−. The 5 V supply is derived from the systems +5 V V_{DD} supply.

When it is required to drive the AD7880 with the 0 to 10 V input range, an external supply must be connected to V+ (see Figure 21).

In bipolar operation, positive and negative supplies must be connected to V+ and V−.

The AD711 is a general purpose op amp which could be used to drive the analog input of the AD7880.

POWER-DOWN CONTROL (MODE INPUT)

The AD7880 is designed for systems which need to have minimum power consumption. This includes such applications as hand held, portable battery powered systems and remote monitoring systems. As well as consuming minimum power under normal operating conditions, typically 20 mW, the AD7880 can be put into a power-down or sleep mode when not required to convert signals. When in this power-down mode, the AD7880 consumes approximately 2 mW of power.

The AD7880 is powered down by bringing the MODE input pin to a Logic Low in conjunction with keeping the $\overline{RD}$ input control High. The AD7880 will remain in the power-down mode until MODE is brought to a Logic High again. The MODE input should be driven with CD4000 or HCMOS logic levels.

It is recommended that one "dummy" conversion be implemented before reading conversion data from the AD7880 after it has been in the power-down mode. This is required to reset all internal logic and control circuitry. In a remote monitoring system where, say, 10 conversions are required to be taken with a sampling interval of 1 second, an additional 11th conversion must be carried out. Figure 22 gives a plot of power consump-

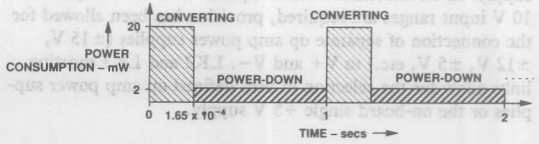


Figure 22. Power Consumption for Normal Operation and Power-Down Operation vs. Time

tion as a function of time for such operation. The total conversion time for each cycle is 11 × 15 μs (where 15 μs is the time taken for a single conversion) corresponding to 1.65×10^{-4} secs. Hence:

$$\text{Average Power} = \text{Power}_{\text{CONVERTING}} + \text{Power}_{\text{POWER-DOWN}}$$
$$= \{20\text{ mW} \times (1.65 \times 10^{-4})/(10)\} + \{2\text{ mW} \times (9.9998)/(10)\}$$
$$= 2.029\text{ mW}$$

AD7880 DATA ACQUISITION LAYOUT

Figure 24 shows the AD7880 in a data acquisition circuit. The corresponding printed circuit board (PCB) layout and silkscreen are shown in Figures 25 to 27.

The only additional component required for a full data acquisition system is an antialiasing filter. There is a component grid provided near the analog input on the PCB which may be used for such a filter or any other input conditioning circuitry. To facilitate this option there is a shorting link (labeled LK1 on the PCB) on the analog input track. With LK1 in place, the analog input connects to the buffer amplifier driving the AD7880. With LK1 removed, a wire link is needed to connect the analog input to the PCB component grid.

INTERFACE CONNECTIONS

The data acquisition board contains a parallel connection port labeled SKT4. This is a 26-contact IDC Connector and provides for direct microprocessor connection to the board. This connector, the pinout of which is shown in Figure 23, contains all data, control and status signals of the AD7880 (with the exception of the $\overline{\text{CONVST}}$ and the CLKIN inputs both of which are provided via SKT2 and SKT3 respectively). It also contains decoded R/$\overline{\text{W}}$ and $\overline{\text{STRB}}$ inputs which are necessary for interfacing to many microprocessors including the TMS320C25 and the Motorola 68000 series. Link LK7 selects $\overline{\text{RD}}$ directly or alternatively, the decoded version. Note that the AD7880 $\overline{\text{CS}}$ input must be decoded prior to the AD7880 evaluation board.

SKT1, SKT2 and SKT3 are three sub-miniature connectors (SMC) which provide input connections for the analog input, the $\overline{\text{CONVST}}$ input and the CLKIN input. Three different input ranges can be accepted by the AD7880 each of which is configured by selecting shorting plug options A, B or C of LK4. Position A corresponds to the 0 to 5 V unipolar configuration of Figure 5, position B corresponds to the bipolar ±5 V configuration of Figure 7 and position C allows for a 0 to +10 V unipolar range as shown in Figure 6.

POWER SUPPLY CONNECTIONS

The PCB requires a single +5 V power supply (labeled V_{DD}). Good decoupling allows this supply to drive the AD7880 V_{DD} which also drives the V_{REF} input as well as the op amp power supply. In circumstances where bipolar ±5 V or a unipolar 0 to 10 V input ranges are required, provision has been allowed for the connection of separate op amp power supplies (±15 V, ±12 V, ±5 V, etc.) to V+ and V−. LK2 and LK3 shorting links allow for the selection of user defined op amp power supplies or the on-board single +5 V supply.

LINK OPTIONS

There are seven link options which must be set before using the board. These are outlined below:

LK1	Connects the analog input to a buffer amplifier. The analog input may also be connected to a component grid for signal conditioning.
LK2, LK3	Allows for various op amp power supplies to be used to drive the input buffer of the AD7880. External supplies may be connected to V+ and V−. Alternatively, the AD7880's +5 V system supply and AGND can be selected to drive a single supply op amp.
LK4	Configures the various analog input ranges, 0 to 5 V, 0 to 10 V or ±5 V.
LK5	Selects reference input to V_{REF} of AD7880. Normally connected to V_{DD}. An external reference could also be wired in.
LK6	Selects power-down or sleep mode. The shorting plug is connected to V_{DD} for normal operation.
LK7	Connects the AD7880 $\overline{\text{RD}}$ input directly to the $\overline{\text{RD}}$ input of SKT4 or to a decoded $\overline{\text{STRB}}$ and R/$\overline{\text{W}}$ input. This shorting plug setting depends on the microprocessor, e.g., the TMS320C25 requires a decoded $\overline{\text{RD}}$ signal.

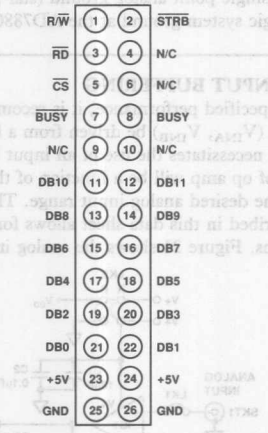


Figure 23. SKT4, IDC Connector Pinout

COMPONENT LIST

IC1	Op Amp*
IC2	AD7880 Analog-to-Digital Converter
IC3	74HC00 Quad NAND Gate
C1, C3, C5	10 μF Capacitors
C2, C4, C6, C7	0.1 μF Capacitors
R1, R2	10 kΩ Pull-up Resistors
LK1, LK2, LK3 LK4, LK5, LK6 LK7	Shorting Links
SKT1, SKT2, SKT3	Sub-Miniature Connectors Vendor No: Sealectro 50-051-0000 (Socket) Sealectro 50-007-0000 (Plug)
SKT4	26-Contact (2 Row) IDC Connector

NOTE
*See ANALOG INPUT BUFFERING section.

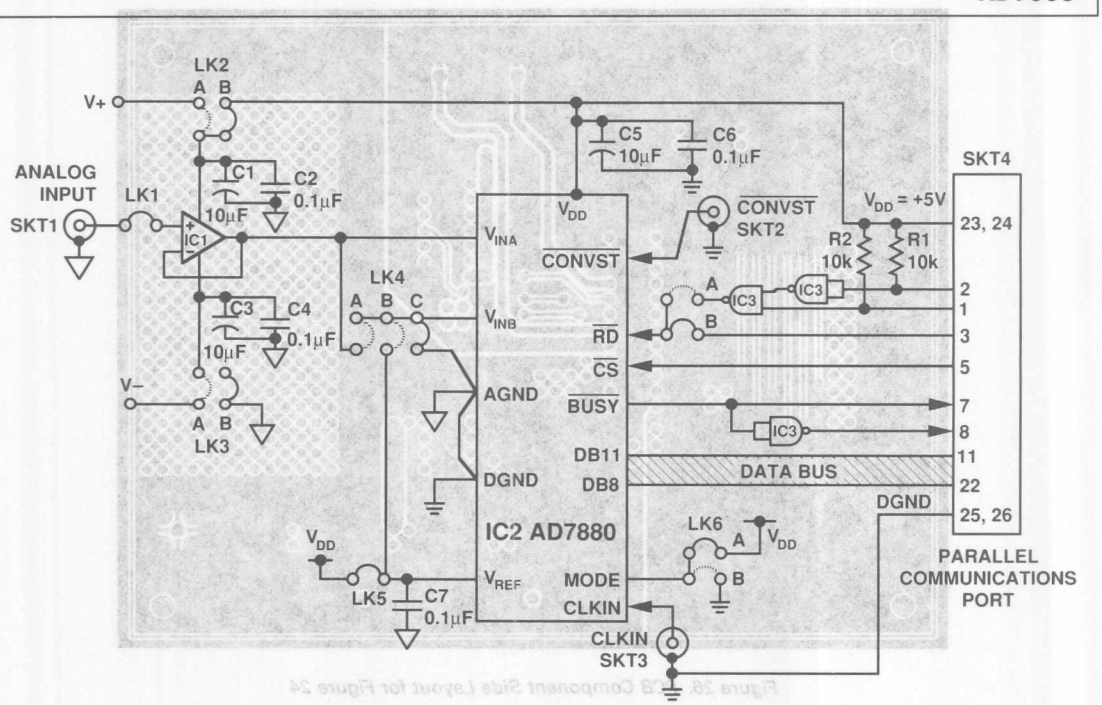


Figure 24. Data Acquisition Circuit Using the AD7880

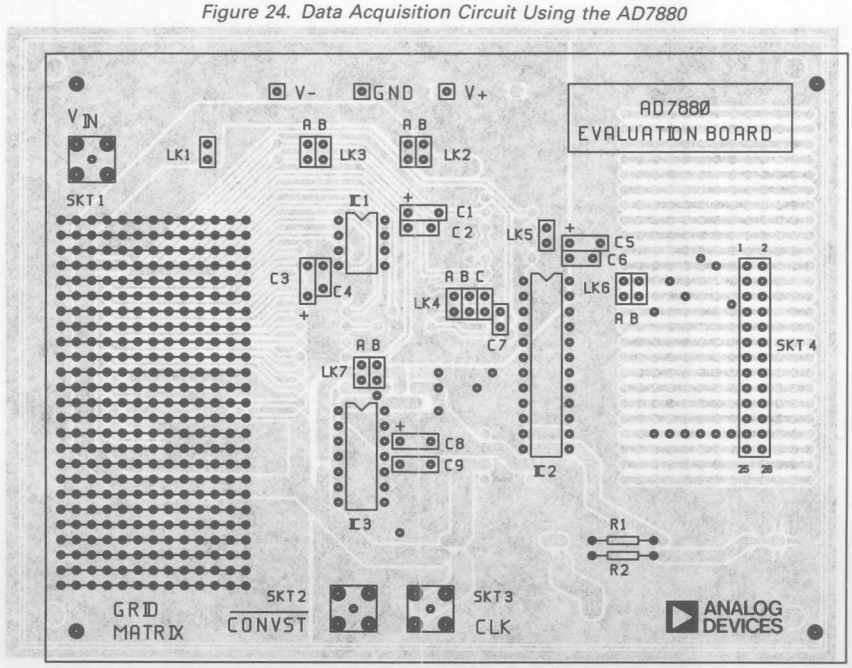


Figure 25. PCB Silkscreen for Figure 24

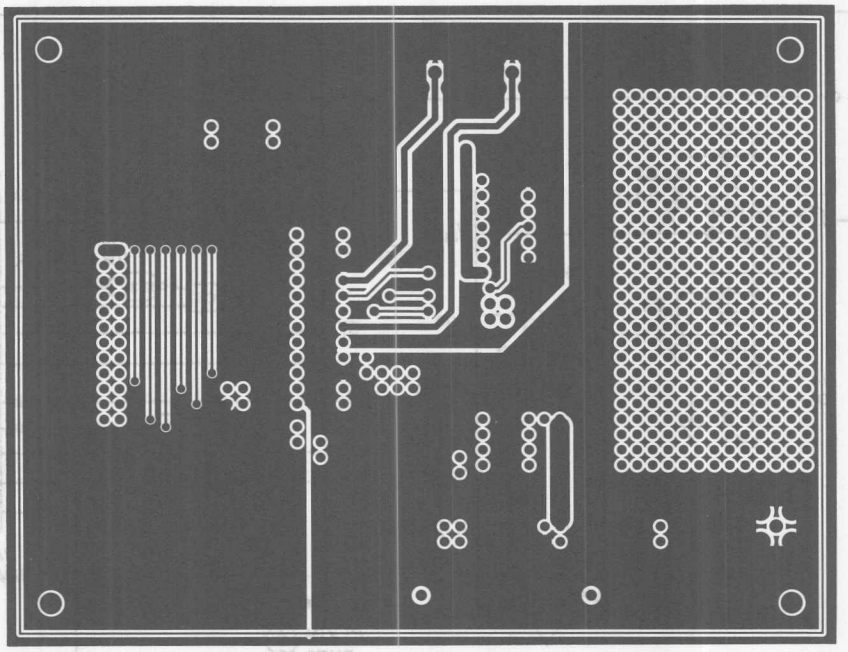


Figure 26. PCB Component Side Layout for Figure 24

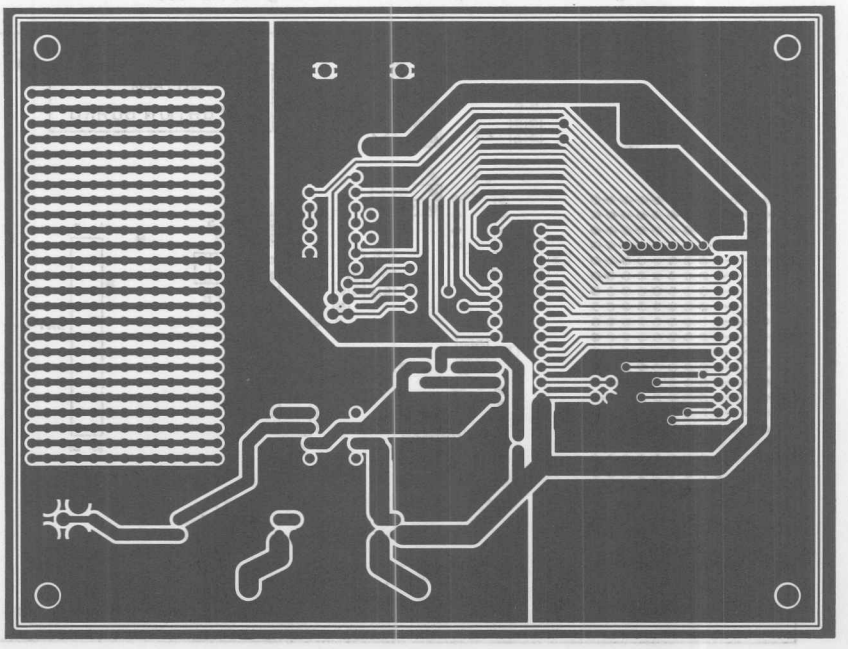


Figure 27. PCB Solder Side Layout for Figure 24

ANALOG DEVICES

LC²MOS
16-Bit, High Speed Sampling ADCs
AD7884/AD7885

FEATURES
Monolithic Construction
Fast Conversion: 5.3 µs
High Throughput: 166 kSPS
Low Power: 250 mW

APPLICATIONS
Automatic Test Equipment
Medical Instrumentation
Industrial Control
Data Acquisition Systems
Robotics

GENERAL DESCRIPTION

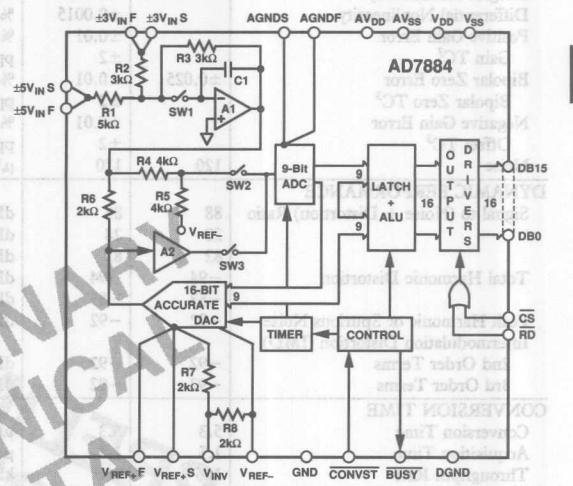
The AD7884/AD7885 is a 16-bit monolithic analog-to-digital converter with internal sample-and-hold and a conversion time of 5.3 µsec. The maximum throughput rate is 166 kSPS. It uses a two pass flash architecture to achieve this speed. Two input ranges are available: ±5 V and ±3 V. Conversion is initiated by the $\overline{\text{CONVST}}$ signal. The result can be read into a microprocessor using the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs on the device. The AD7884 has a 16-bit parallel reading structure while the AD7885 has a byte reading structure. The conversion result is in 2s complement code.

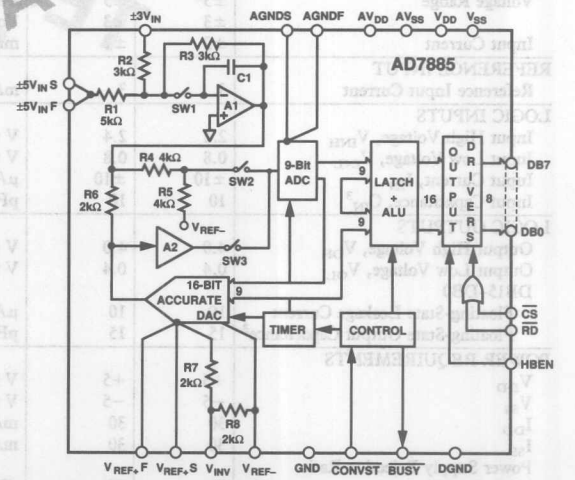
The AD7884/AD7885 has its own internal oscillator which controls conversion. It runs from ±5 V supplies and needs a V_{REF+} of +3 V.

The AD7884 is available in 40-pin plastic and cerdip packages and in a 44-pin PLCC package.

The AD7885 is available in 28-pin plastic and cerdip packages and in a 28-pin PLCC package.

FUNCTIONAL BLOCK DIAGRAMS





PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

DC ACCURACY				
Resolution	16	16	Bits	
Minimum Resolution for Which				
No Missing Codes Are Guaranteed	16	16	Bits	
Integral Nonlinearity		±0.003	% FSR max	
Differential Nonlinearity		±0.0015	% FSR max	
Positive Gain Error		±0.01	% FSR max	
Gain TC[3]		±2	ppm FSR/°C typ	
Bipolar Zero Error	±0.025	±0.01	% FSR max	
Bipolar Zero TC[3]		±2	ppm FSR/°C typ	
Negative Gain Error		±0.01	% FSR max	
Offset TC[3]		±2	ppm FSR/°C typ	
Noise	120	120	μV rms typ	78 μV rms typical in ±3 V Input Range
DYNAMIC PERFORMANCE				
Signal to (Noise + Distortion) Ratio	88	88	dB min	Input Signal: ±5 V, 1 kHz Sine Wave
	28	28	dB min	Input Signal: ±5 mV, 1 kHz Sine Wave
	82	82	dB min	Input Signal: ±5 V, 25 kHz Sine Wave
Total Harmonic Distortion	−94	−94	dB max	Input Signal: ±5 V, 1 kHz Sine Wave
	−83	−83	dB max	Input Signal: ±5 V, 25 kHz Sine Wave
Peak Harmonic or Spurious Noise	−92	−92	dB max	Input Signal: ±5 V, 25 kHz Sine Wave
Intermodulation Distortion (IMD)				
2nd Order Terms	−92	−92	dB max	f_A = 24.5 kHz, f_B = 25 kHz, f_{SAMPLE} = 166 kHz
3rd Order Terms	−92	−92	dB max	f_A = 24.5 kHz, f_B = 25 kHz, f_{SAMPLE} = 166 kHz
CONVERSION TIME				
Conversion Time	5.3	5.3	μs max	
Acquisition Time	1.5	1.5	μs max	
Throughput Rate	166	166	kSPS max	There is an overlap between conversion and acquisition.
ANALOG INPUT				
Voltage Range	±5	±5	Volts	
	±3	±3	Volts	
Input Current	±2	±2	mA max	
REFERENCE INPUT				
Reference Input Current	3	3	mA max	V_{REF} + S = +3 V
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V± 5%
Input Current, I_{IN}	±10	±10	μA max	Input Level = 0 V to V_{DD}
Input Capacitance, C_{IN}[3]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	4.0	4.0	V min	I_{SOURCE} = 40 μA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB15–DB0				
Floating-State Leakage Current	10	10	μA max	
Floating-State Output Capacitance[3]	15	15	pF max	
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	V nom	±5% for Specified Performance
I_{DD}	30	30	mA max	Typically 25 mA
I_{SS}	30	30	mA max	Typically 25 mA
Power Supply Rejection Ratio				
$\Delta Gain/\Delta V_{DD}$	86	86	dB typ	
$\Delta Gain/\Delta V_{SS}$	86	86	dB typ	
Power Dissipation	300	300	mW max	Typically 250 mW

NOTES
[1]Temperature Ranges are as follows: A, B Versions: −40°C to +85°C; T Version: −55°C to +125°C.
[2]V_{IN} = ±5 V.
[3]Sample tested to ensure compliance.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = GND = 0 V. See Figures 2, 3, 4 and 5.)

Parameter	Limit at +25°C (All Versions)	Limit at T_{MIN}, T_{MAX} (A, B Versions)	Limit at T_{MIN}, T_{MAX} (T Version)	Units	Conditions/Comments
t_1	50	50	50	ns min	$\overline{CONVST}$ Pulse Width
t_2	100	100	100	ns min	$\overline{CONVST}$ to $\overline{BUSY}$ Low Delay
t_3	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_4	60	60	75	ns min	$\overline{RD}$ Pulse Width
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6[2]	57	57	70	ns max	Data Access Time after $\overline{RD}$
t_7[3]	5	5	5	ns min	Bus Relinquish Time after $\overline{RD}$
	50	50	50	ns max	
t_8	40	40	40	ns min	New Data Valid before Rising Edge of $\overline{BUSY}$
t_9	0	0	0	ns min	HBEN to $\overline{RD}$ Setup Time
t_{10}	0	0	0	ns min	HBEN to $\overline{RD}$ Hold Time
t_{11}	60	60	75	ns min	HBEN Low Pulse Duration
t_{12}	60	60	75	ns min	HBEN High Pulse Duration
t_{13}	40	40	40	ns max	Propagation Delay from HBEN Falling to Data Valid
t_{14}	40	40	40	ns max	Propagation Delay from HBEN Rising to Data Valid

NOTES

[1]Timing specifications in **bold** print are 100% production tested. All other times are sample tested at +5°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]t_6 is measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[3]t_7 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time, t_7, quoted in the Timing Characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Linearity Error (% FSR)	SNR (dB)	Package Option*
AD7884AN	−40°C to +85°C		88	N-40
AD7884BN	−40°C to +85°C	±0.003	88	N-40
AD7884AP	−40°C to +85°C		88	P-44
AD7884BP	−40°C to +85°C	±0.003	88	P-44
AD7884TQ	−55°C to +125°C	±0.003	88	Q-40
AD7885AN	−40°C to +85°C		88	N-28
AD7885BN	−40°C to +85°C	±0.003	88	N-28
AD7885AP	−40°C to +85°C		88	P-28
AD7885BP	−40°C to +85°C	±0.003	88	P-28
AD7885TQ	−55°C to +125°C	±0.003	88	Q-28

*N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip.
For outline information see Package Information section.

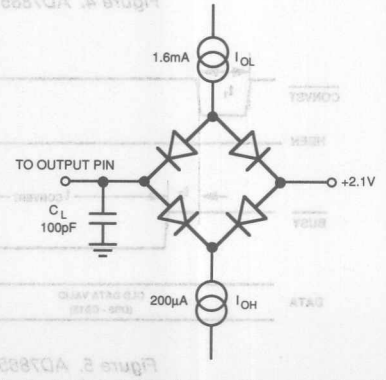


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

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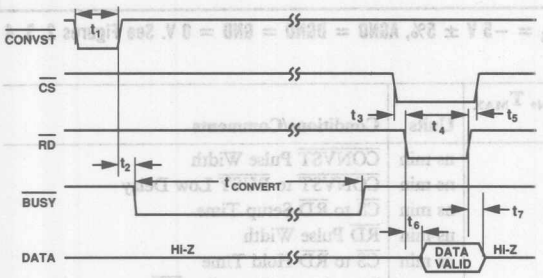


Figure 2. AD7884 Timing Diagram, Using $\overline{CS}$ and $\overline{RD}$

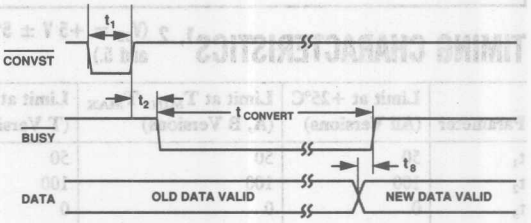
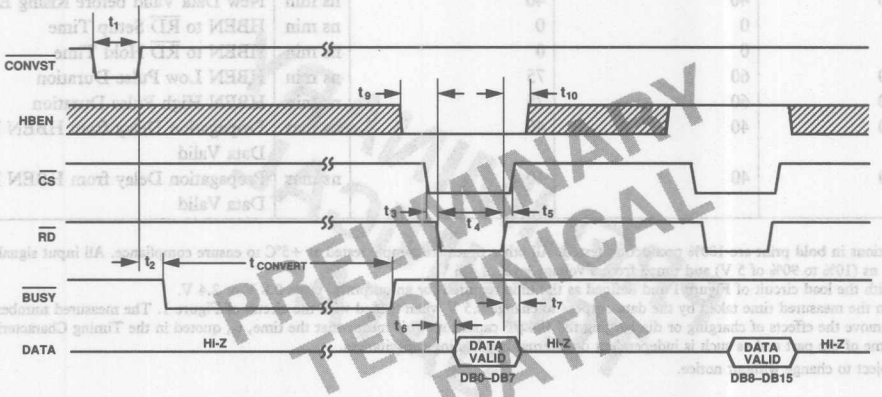


Figure 3. AD7884 Timing Diagram, with $\overline{CS}$ and $\overline{RD}$ Permanently Low



PRELIMINARY TECHNICAL DATA

Figure 4. AD7885 Timing Diagram, Using $\overline{CS}$ and $\overline{RD}$

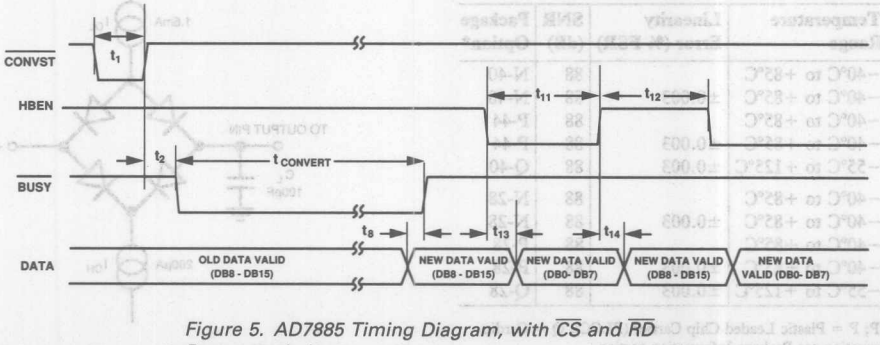


Figure 5. AD7885 Timing Diagram, with $\overline{CS}$ and $\overline{RD}$ Permanently Low

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ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{SS} to AGND . . . . . +0.3 V to −7 V
AGND Pins to DGND . . . . . −0.3 V to V_{DD} +0.3 V
GND to DGND . . . . . −0.3 V to V_{DD} +0.3 V
$V_{IN}S$, $V_{IN}F$ to AGND . . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
V_{REF+} to AGND . . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
V_{REF-} to AGND . . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
V_{INV} to AGND . . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
Digital Inputs to DGND . . . . . −0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND . . . . . −0.3 V to V_{DD} +0.3 V

Operating Temperature Range
Commercial Plastic (A, B Versions) . . . . . −40°C to +85°C
Industrial Cerdip (A, B Versions) . . . . . −40°C to +85°C
Extended Cerdip (T Versions) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

CAUTION

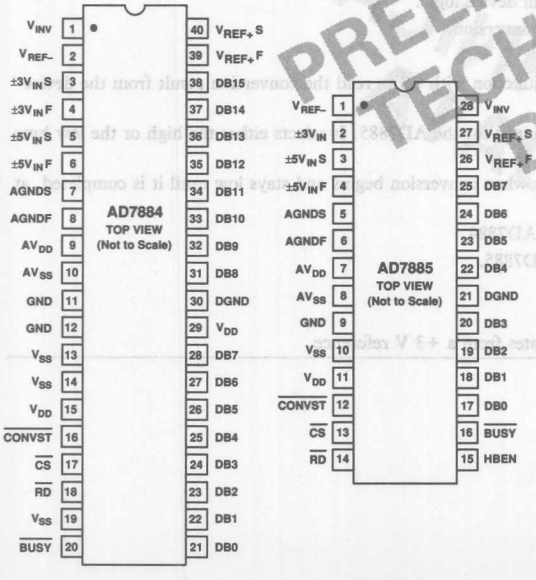
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



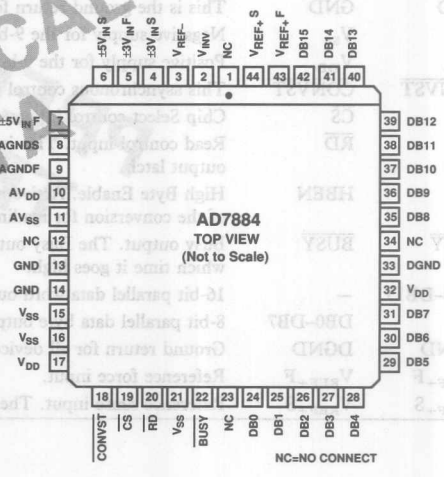
PRELIMINARY TECHNICAL DATA

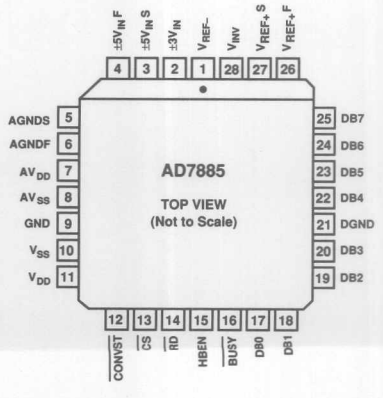
PIN CONFIGURATIONS

DIP



PLCC





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PIN FUNCTION DESCRIPTION

AD7884 Pin	AD7885 Pin	Description
V_{INV}	V_{INV}	This pin is connected to the inverting terminal of an op amp, as in Figure 6 and allows the inversion of the supplied +3 V reference.
V_{REF-}	V_{REF-}	This is the negative reference input and it can be obtained by using an external amplifier to invert the positive reference input. In this case, the amplifier output is connected to V_{REF-}. See Figure 6.
$\pm 3V_{IN}S$	—	This is the analog input sense pin for the ±3 volt analog input range on the AD7884.
$\pm 3V_{IN}F$	—	This is the analog input force pin for the ±3 volt analog input range on the AD7884. When using this input range, the ± 5 $V_{IN}F$ and ± 5 $V_{IN}S$ pins should be tied to AGND.
—	$\pm 3V_{IN}$	This is the analog input pin for the ±3 volt analog input range on the AD7885. When using this input range, the ± 5 $V_{IN}F$ and ± 5 $V_{IN}S$ pins should be tied to AGND.
$\pm 5V_{IN}S$	$\pm 5V_{IN}S$	This is the analog input sense pin for the ±5 volt analog input range on both the AD7884 and the AD7885.
$\pm 5V_{IN}F$	$\pm 5V_{IN}F$	This is the analog input force pin for the ±5 volt analog input range on both the AD7884 and AD7885. When using this input range, the ± 3 $V_{IN}F$ and ± 3 $V_{IN}S$ pins should be tied to AGND.
AGNDS	AGNDS	This is the ground return sense pin for the 9-bit ADC and the on-chip residue amplifier.
AGNDF	AGNDF	This is the ground return force pin for the 9-bit ADC and the on-chip residue amplifier.
AV_{DD}	AV_{DD}	Positive analog power rail for the sample-and-hold amplifier and the residue amplifier.
AV_{SS}	AV_{SS}	Negative analog power rail for the sample-and-hold amplifier and the residue amplifier.
GND	GND	This is the ground return for sample-and-hold section.
V_{SS}	V_{SS}	Negative supply for the 9-bit ADC.
V_{DD}	V_{DD}	Positive supply for the 9-bit ADC and all device logic.
$\overline{CONVST}$	$\overline{CONVST}$	This asynchronous control input starts conversion.
$\overline{CS}$	$\overline{CS}$	Chip Select control input.
$\overline{RD}$	$\overline{RD}$	Read control input. This is used in conjunction with $\overline{CS}$ to read the conversion result from the device output latch.
—	HBEN	High Byte Enable. Active high control input for the AD7885. It selects either the high or the low byte of the conversion for reading.
$\overline{BUSY}$	$\overline{BUSY}$	Busy output. The Busy output goes low when conversion begins and stays low until it is completed, at which time it goes high.
DB0–DB15	—	16-bit parallel data word output on the AD7884.
—	DB0–DB7	8-bit parallel data byte output on the AD7885.
DGND	DGND	Ground return for all device logic.
$V_{REF+}F$	$V_{REF+}F$	Reference force input.
$V_{REF+}S$	$V_{REF+}S$	Reference sense input. The device operates from a +3 V reference.

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TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Bipolar Zero Error
This is the deviation of the midscale transition (all 0s to all 1s) from the ideal (AGND).

Positive Gain Error
This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal ($+V_{REF+}$ S − 1 LSB).

Negative Gain Error
This is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal ($-V_{REF+}$S + 1 LSB)

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$Signal\ to\ (Noise + Distortion) = (6.02N + 1.76)\ dB$$

Thus for a 16-bit converter, this is 98 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7884/AD7885, it is defined as:

$$THD\ (dB) = 20\ log\ \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m or n are equal to zero. For example, the second order terms include (fa + fb) and (fa − fb), while the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb).

The AD7884/AD7885 is tested using the CCIFF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Power Supply Rejection Ratio
This is the ratio, in dBs, of the change in positive gain error to the change in V_{DD} or V_{SS}. It is a dc measurement.

OPERATIONAL DIAGRAM

An operational diagram for the AD7884/AD7885 is shown in Figure 6. It is set up for an analog input range of ±5 V. If a ±3 V input range is required, A1 should drive ±3 V_{IN}S and ±3 V_{IN}F with ±5 V_{IN}S, ±5 V_{IN}F being tied to system AGND.

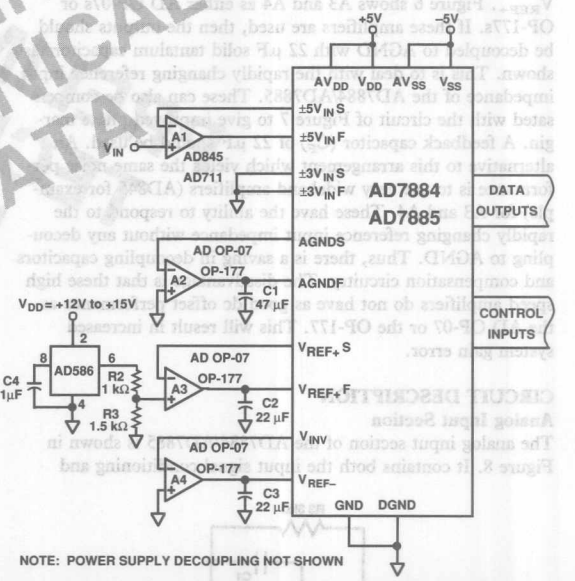


Figure 6. AD7884/AD7885 Operational Diagram

The chosen input buffer amplifier (A1) should have low noise and distortion and fast settling time for high bandwidth applications. Both the AD711 and the AD845 are suitable amplifiers.

A2 is the force, sense amplifier for AGND. The AGNDS pin should be at zero potential. Therefore, the amplifier must have a very low input offset voltage and good noise performance. For these reasons, either the AD OP-07 or OP-177 is recommended. The output of A2 is decoupled with a 47 µF solid tantalum capacitor to AGND to deal with the fast current transients on the

PRELIMINARY TECHNICAL DATA

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If the user wishes to improve the phase margin, the circuit given in Figure 7 may be used. A feedback capacitor (R_F) of 47 μF should be used. This circuit compensates for the load capacitor by adding a low frequency zero and ensures an adequate phase margin.

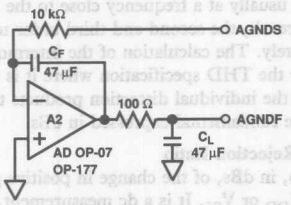


Figure 7. Compensation Circuit for A2

The required +3 V reference is derived from the AD586. The +5 V output is divided down to +3 V by R2 and R3 before being buffered by A3. A4 is a unity gain inverter which provides the −3 V negative reference. The gain setting resistors are on-chip and are factory trimmed to ensure precise tracking of V_{REF+}. Figure 6 shows A3 and A4 as either AD OP-07s or OP-177s. If these amplifiers are used, then the outputs should be decoupled to AGND with 22 μF solid tantalum capacitors as shown. This is to deal with the rapidly changing reference input impedance of the AD7884/AD7885. These can also be compensated with the circuit of Figure 7 to give improved phase margin. A feedback capacitor (C_F) of 22 μF should be used. An alternative to this arrangement which yields the same noise performance is to use very wideband amplifiers (AD845 for example) for A3 and A4. These have the ability to respond to the rapidly changing reference input impedance without any decoupling to AGND. Thus, there is a saving in decoupling capacitors and compensation circuitry. The disadvantage is that these high speed amplifiers do not have as good dc offset performance as the AD OP-07 or the OP-177. This will result in increased system gain error.

CIRCUIT DESCRIPTION

Analog Input Section

The analog input section of the AD7884/AD7885 is shown in Figure 8. It contains both the input signal conditioning and

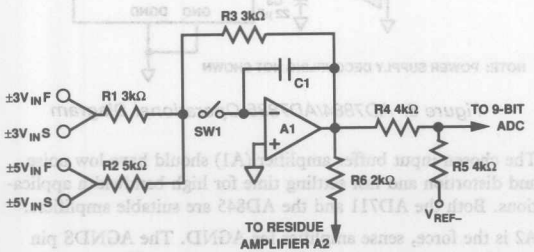


Figure 8. AD7884/AD7885 Analog Input Section

inputs are tied to 0 V, the input section has a gain of −0.6 and transforms an input signal of ±5 volts to the required ±3 volts. When the ±5 $V_{IN}S$ and ±5 $V_{IN}F$ inputs are grounded, the input section has a gain of −1 and so the analog input range is now ±3 volts. Resistors R4 and R5, at the amplifier output, further condition the ±3 volts signal to be 0 to −3 volts. This is the required input for the 9-bit A/D converter section.

With SW1 closed, the output of A1 follows the input (the sample-and-hold is in the track mode). On the rising edge of the $\overline{\text{CONVST}}$ pulse, SW1 goes open circuit, and capacitor C1 holds the voltage on the output of A1. The sample-and-hold is now in the hold mode. The aperture delay time for the sample-and-hold is nominally 50 ns.

A/D Converter Section

The AD7884/AD7885 uses a two-pass flash technique in order to achieve the required speed and resolution. When the $\overline{\text{CONVST}}$ control input goes from low to high, the sample-and-hold amplifier goes into the hold mode and a 0 V to −3 V signal is presented to the input of the 9-bit ADC. The first phase of conversion generates the 9 MSBs of the 16-bit result and transfers these to the latch and ALU combination. They are also fed back to the 9 MSBs of the 16-bit DAC. The 7 LSBs of the DAC are permanently loaded with 0s. The DAC output is subtracted from the analog input with the result being amplified and offset in the Residue Amplifier Section. The signal at the output of A2 is proportional to the error between the first phase result and the actual analog input signal and is digitized in the second conversion phase. This second phase begins when the 16-bit DAC and the Residue Error Amplifier have both settled. First, SW2 is turned off and SW3 is turned on. The 9-bit result is transferred to the output latch and ALU. An error correction algorithm now compensates for the offset inserted in the Residue Amplifier Section and errors introduced in the first pass conversion and combines both results to give the 16-bit answer.

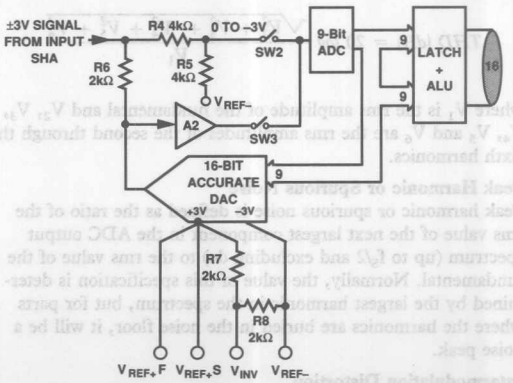
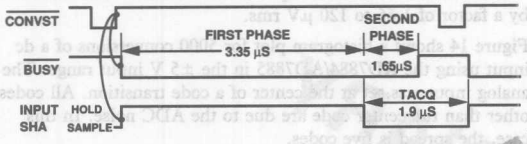


Figure 9. A/D Converter Section

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Timing and Control Section

Figure 10 shows the timing and control sequence for the AD7884/AD7885. When the part receives a $\overline{\text{CONVST}}$ pulse, the conversion begins. The input sample-and-hold goes into the hold mode 50 ns after the rising edge of $\overline{\text{CONVST}}$ and $\overline{\text{BUSY}}$ goes low. This is the first phase of conversion and takes 3.35 μs to complete. The second phase of conversion begins when SW2 is turned off and SW3 turned on. The Residue Amplifier and SHA section (A2 in Figure 9) goes into hold mode at this point and allows the input sample-and-hold to go back into sample mode. Thus, while the second phase of conversion is ongoing, the input sample-and-hold is also acquiring the input signal for the next conversion. This overlap between conversion and acquisition allows throughput rates of 166 kSPS to be achieved.



FIRST PHASE OF CONVERSION
1ST 9-BIT CONVERSION
DAC SETTLING TIME
RESIDUE AMPLIFIER
SETTLING TIME

SECOND PHASE OF CONVERSION
2ND 9-BIT CONVERSION
ERROR CORRECTION
OUTPUT LATCH UPDATE

Figure 10. Timing and Control Sequence

PRELIMINARY TECHNICAL DATA

USING THE AD7884/AD7885

Analog Input Ranges

The AD7884/AD7885 can be set up to have either a ±3 volts analog input range or a ±5 volts analog input range. Figures 11 and 12 show the necessary corrections for each of these. The output code is 2s complement and the ideal code table for both input ranges is shown in Table I.

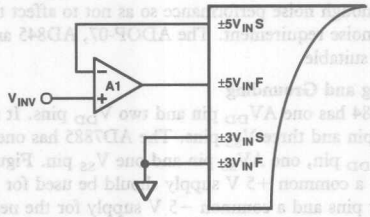


Figure 11. ±5 V Input Range Connections

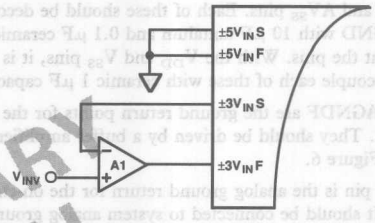


Figure 12. ±3 V Input Range Connections

Reference Considerations

The AD7884/AD7885 operates from a ±3 volt reference. This can be derived simply from any single +5 volt reference as shown in Figure 6.

The critical performance specification for a reference in a 16-bit application is noise. The reference pk-pk noise should be insignificant in comparison to the ADC noise. The AD7884/AD7885 has a typical rms noise of 120 μV. For example a reasonable target would be to keep the total rms noise less than 125 μV. To do this the reference noise needs to be less than 35 μV rms. Using a crest factor of 3.3 this corresponds to a pk-pk noise of 230 μV. Both the AD586 and the AD REF-02 noise is lower than this, making both suitable.

Table I. Ideal Output Code Table for the AD7884/AD7885

Analog Input			Digital Output
In Terms of FSR[2]	±3 V Range[3]	±5 V Range[4]	Code Transition[1]
+FSR/2 − 1 LSB	2.999908	4.999847	011 . . . 111 to 011 . . . 110
+FSR/2 − 2 LSBs	2.999817	4.999695	011 . . . 110 to 011 . . . 101
+FSR/2 − 3 LSBs	2.999726	4.999543	011 . . . 101 to 011 . . . 100
AGND + 1 LSB	0.000092	0.000153	000 . . . 001 to 000 . . . 000
AGND	0.000000	0.000000	000 . . . 000 to 111 . . . 111
AGND − 1 LSB	−0.000092	−0.000153	111 . . . 111 to 111 . . . 110
−(FSR/2 − 3 LSBs)	−2.999726	−4.999543	100 . . . 011 to 100 . . . 010
−(FSR/2 − 2 LSBs)	−2.999817	−4.999695	100 . . . 010 to 100 . . . 001
−(FSR/2 − 1 LSB)	−2.999908	−4.999847	100 . . . 001 to 100 . . . 000

NOTES
[1]This table applies for $V_{REF+}S$ = +3 V.
[2]FSR (Full-Scale Range) is 6 volts for the ±3 V input range and 10 volts for the ±5 V input range.
[3]1 LSB on the ±3 V range is FSR/2^{16} and is equal to 91.5 μV.
[4]1 LSB on the ±5 V range is FSR/2^{16} and is equal to 152.6 μV.

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The buffer amplifier used to drive the device V_{REF+} should have low enough noise performance so as not to affect the overall system noise requirement. The ADOP-07, AD845 and OP-177 are all suitable.

Decoupling and Grounding

The AD7884 has one AV_{DD} pin and two V_{DD} pins. It also has one AV_{SS} pin and three V_{SS} pins. The AD7885 has one AV_{DD} pin, one V_{DD} pin, one AV_{SS} pin and one V_{SS} pin. Figure 6 shows how a common +5 V supply should be used for the positive supply pins and a common −5 V supply for the negative supply pins.

For decoupling purposes, the critical pins on both devices are the AV_{DD} and AV_{SS} pins. Each of these should be decoupled to system AGND with 10 μF tantalum and 0.1 μF ceramic capacitors right at the pins. With the V_{DD} and V_{SS} pins, it is sufficient to decouple each of these with ceramic 1 μF capacitors.

AGNDS, AGNDF are the ground return points for the on-chip 9-bit ADC. They should be driven by a buffer amplifier as shown in Figure 6.

The GND pin is the analog ground return for the on-chip linear circuitry. It should be connected to system analog ground.

The DGND pin is the ground return for the on-chip digital circuitry. It should be connected to the ground terminal of the V_{DD} and V_{SS} supplies. If a common analog supply is used for AV_{DD} and V_{DD} then DGND should be connected to the common ground point.

Power Supply Sequencing

If the AD7884/AD7885 is being powered from separate analog and digital supplies, then care should be taken with power supply sequencing. AV_{DD} should always come up before V_{DD} and AV_{SS} should always come up before V_{SS}. If this cannot be guaranteed, Schottky diodes (HP5082-2810 or equivalent) should be used to ensure that V_{DD} never exceeds AV_{DD} by more than 0.3 V and that V_{SS} never goes below AV_{SS} by more than 0.3 V.

AD7884/AD7885 PERFORMANCE

Linearity

The linearity of the AD7884/AD7885 is determined by the on-chip 16-bit D/A converter. This is a segmented DAC which is laser trimmed for 16-bit DNL performance to ensure that there are no missing codes in the ADC transfer function. Figure 13 shows a typical INL plot for the AD7884/AD7885.

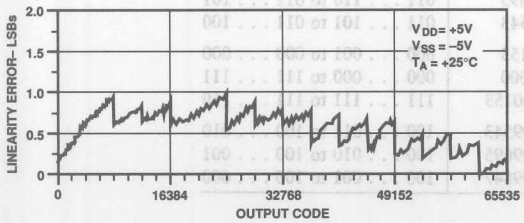


Figure 13. AD7884/AD7885 Typical Linearity Performance

Noise

In an A/D converter, noise exhibits itself as code uncertainty in dc applications and as the noise floor (in an FFT, for example) in ac applications.

In a sampling A/D converter like the AD7884/AD7885, all information about the analog input appears in the baseband from dc to 1/2 the sampling frequency. An antialiasing filter will remove unwanted signals above fs/2 in the input signal but the converter wideband noise will alias into the baseband. In the AD7884/AD7885, this noise is made up of sample-and-hold noise and a/d converter noise. The sample-and-hold section contributes 51 μV rms and the ADC section contributes 59 μV rms. These add up to a total rms noise of 78 μV. This is the input referred noise in the ±3 V analog input range. When operating in the ±5 V input range, the input gain is reduced to −0.6. This means that the input referred noise is now increased by a factor of 1.66 to 120 μV rms.

Figure 14 shows a histogram plot for 5000 conversions of a dc input using the AD7884/AD7885 in the ±5 V input range. The analog input was set at the center of a code transition. All codes other than the center code are due to the ADC noise. In this case, the spread is five codes.

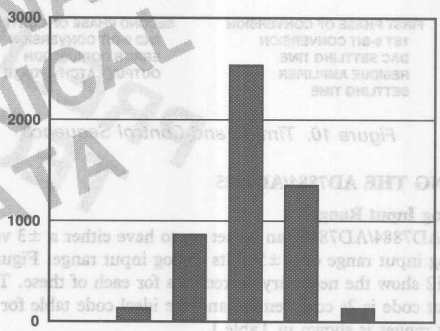


Figure 14. Histogram of 5000 Conversions of a DC Input

If the noise in the converter is too high for an application, it can be reduced by oversampling and digital filtering. This involves sampling the input at higher than the required word rate and then averaging to arrive at the final result. The very fast conversion time of the AD7884/AD7885 makes it very suitable for oversampling. For example, if the required input bandwidth is 50 kHz, the AD7884/AD7885 could be oversampled by a factor of 2. This yields a 3 dB improvement in the effective SNR performance. The noise performance in the ±5 volt input range is now effectively 85 μV rms and the resultant spread of codes for 2500 conversions will be four. This is shown in Figure 15.

PRELIMINARY TECHNICAL DATA

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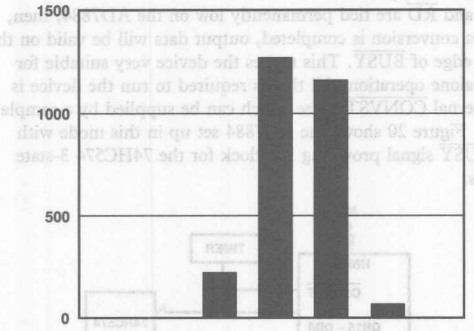


Figure 15. Histogram of 2500 Conversions of a DC Input Using a ×2 Oversampling Ratio

Dynamic Performance

With a combined conversion and acquisition time of 6 µs, the AD7884/AD7885 is ideal for wide bandwidth signal processing applications. Signal to (Noise + Distortion), Total Harmonic Distortion, Peak Harmonic or Spurious Noise and Intermodulation Distortion are all specified. Figure 16 shows a typical FFT plot of a 1.8 kHz, ±5 V input after being digitized by the AD7884/AD7885.

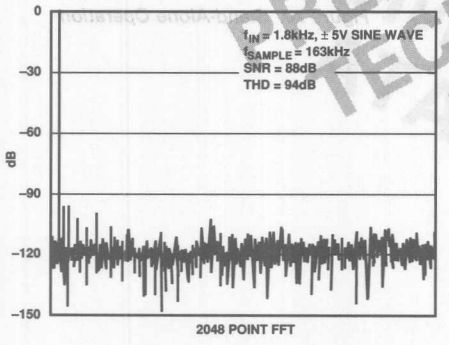


Figure 16. AD7884/AD7885 FFT Plot

MICROPROCESSOR INTERFACING

The AD7884/AD7885 is designed on a high speed process which results in very fast interfacing timing. The AD7884 has a full 16-bit parallel bus and the AD7885 has an 8-bit wide bus.

AD7884–MC68000 Interface

Figure 17 shows a general interface diagram for the MC68000, 16-bit microprocessor to the AD7884. In Figure 17, conversion is initiated by bringing $\overline{CSA}$ low (i.e., writing to the appropriate address). This allows the processor to maintain control over the complete conversion process. In some cases it may be more desirable to control conversion independent from the processor. This can be done by using an external sampling timer.

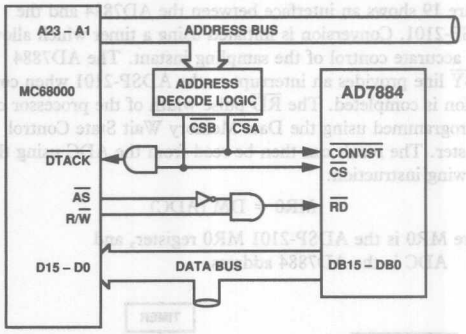


Figure 17. AD7884 to MC68000 Interface

Once conversion has been started, the processor must wait until it is completed before reading the result. There are two ways of ensuring this. The first way is to simply use a software delay to wait for 6.5 µs before bringing $\overline{CS}$ and $\overline{RD}$ low to read the data. The second way is to use the $\overline{BUSY}$ output of the AD7884 to generate an interrupt in the MC68000. Because of the nature of its interrupts, the MC68000 requires additional logic (not shown in Figure 17) to allow it to be interrupted correctly. For full information on this, consult the MC68000 User's Manual.

AD7885 to 8088 Interface

The AD7885, with its byte (8 + 8) data format, is ideal for use with the 8088 microprocessor. Figure 18 is the interface diagram. Conversion is started by enabling $\overline{CSA}$. At the end of conversion, data is read into the processor. The read instructions are:

```
MOV AX, C001    Read 8 MSBs of data
MOV AX, C000    Read 8 LSBs of data
```

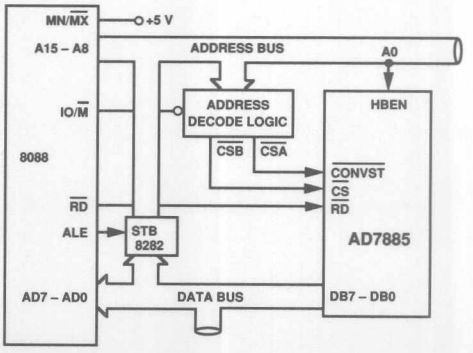


Figure 18. AD7885 to 8088 Interface

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AD7884 to ADSP-2101 Interface

Figure 19 shows an interface between the AD7884 and the ADSP-2101. Conversion is initiated using a timer which allows very accurate control of the sampling instant. The AD7884 $\overline{BUSY}$ line provides an interrupt to the ADSP-2101 when conversion is completed. The $\overline{RD}$ pulse width of the processor can be programmed using the Data Memory Wait State Control Register. The result can then be read from the ADC using the following instruction:

MR0 = DM (ADC)

where MR0 is the ADSP-2101 MR0 register, and
ADC is the AD7884 address.

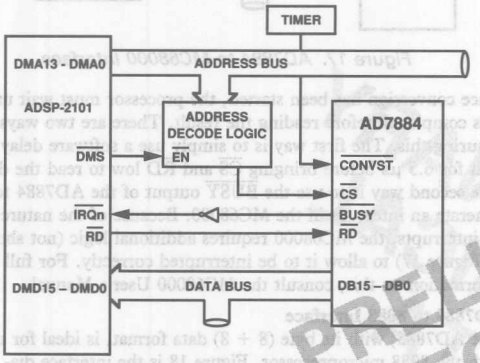


Figure 19. AD7884 to ADSP-2101 Interface

Stand-Alone Operation

If $\overline{CS}$ and $\overline{RD}$ are tied permanently low on the AD7884, then, when a conversion is completed, output data will be valid on the rising edge of $\overline{BUSY}$. This makes the device very suitable for stand-alone operation. All that is required to run the device is an external $\overline{CONVST}$ pulse which can be supplied by a sample timer. Figure 20 shows the AD7884 set up in this mode with the $\overline{BUSY}$ signal providing the clock for the 74HC574 3-state latches.

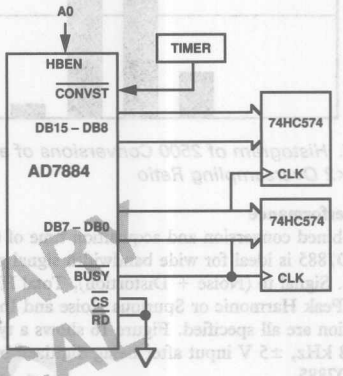


Figure 20. Stand-Alone Operation

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ANALOG DEVICES

LC²MOS 12-Bit, 750 kHz, Sampling ADC

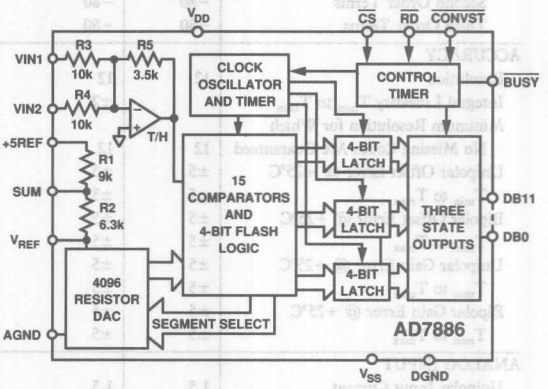
AD7886

2

FEATURES
- 750 kHz Throughput Rate
- 1 μs Conversion Time
- 12-Bit No Missed Codes Over Temperature
- 67 dB SNR at 100 kHz Input Frequency
- Low Power—250 mW typ
- Fast Bus Access Time—57 ns max

APPLICATIONS
- Digital Signal Processing
- Speech Recognition and Synthesis
- Spectrum Analysis
- DSP Servo Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7886 is 12-bit ADC with a sample-and-hold amplifier offering high speed performance combined with low power dissipation. The AD7886 is a triple pass flash ADC, which uses 15 comparators in a 4-bit flash technique to achieve 12-bit accuracy in 1 μs conversion time. An on-chip clock oscillator provides the appropriate timing for each of the three conversion stages eliminating the need for any external clocks. Acquisition time of the sample-and-hold amplifier is less than 333 ns giving a resulting throughput rate of 750 kHz.

The AD7886 operates from ±5 V power supplies. Pin-strappable inputs offer a choice of three analog input ranges; 0 to 5 V, 0 to 10 V or ±5 V.

In addition to the traditional dc accuracy specifications such as linearity, offset and full-scale errors, the AD7886 is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio at a sampling frequency of 750 kHz.

The AD7886 has a high speed digital interface with three-state data outputs. Conversion control is provided by a $\overline{\text{CONVST}}$ input. Data access is controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs, standard microprocessor signals. The data access time of less than 57 ns means that the AD7886 can interface directly to most modern microprocessors including DSP processors.

The AD7886 is fabricated in Analog Devices' Linear Compatible CMOS process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic.

The AD7886 is available in both a 28-pin DIP and in a 28-pin leaded chip carrier.

PRODUCT HIGHLIGHTS

1. Fast 1.333 μs Throughput Time.
   Fast 1.333 μs throughput time makes the AD7886 suitable for a wide range of data acquisition applications.
2. Dynamic Specifications for DSP Users.
   The AD7886 is specified for ac parameters, including signal-to-noise ratio, harmonic distortion and intermodulation distortion. Key digital timing parameters are also tested and guaranteed over the full operating temperature range.
3. Fast Microprocessor Interface.
   Standard control signals, $\overline{\text{CS}}$ and $\overline{\text{RD}}$, and fast bus access times make the AD7886 easy to interface to microprocessors.
4. Low Power.
   LC²MOS fabrication process gives low power dissipation of 250 mW.

DYNAMIC PERFORMANCE					
Signal-to-Noise Ratio[3] (SNR)	65	67	65	dB min	VIN = 100 kHz Sine Wave, f_{SAMPLE} = 750 kHz
Total Harmonic Distortion (THD)	−75	−75	−75	dB typ	VIN = 100 kHz Sine Wave, f_{SAMPLE} = 750 kHz
Peak Harmonic or Spurious Noise	−77	−77	−77	dB typ	VIN = 100 kHz Sine Wave, f_{SAMPLE} = 750 kHz
Intermodulation Distortion (IMD)					
Second Order Terms	−80	−80	−80	dB typ	f_a = 96 kHz, f_b = 103 kHz, f_{SAMPLE} = 750 kHz
Third Order Terms	−80	−80	−80	dB typ	
ACCURACY					
Resolution	12	12	12	Bits	
Integral Linearity T_{min} to T_{max}		±2	±2	LSB max	
Minimum Resolution for Which					
No Missing Codes Are Guaranteed	12	12	12	Bits	
Unipolar Offset Error @ +25°C	±5	±5	±5	LSB max	Input Range: 0 to 5 V or 0 to 10 V
T_{min} to T_{max}	±5	±5	±5	LSB max	
Bipolar Offset Error @ +25°C	±5	±5	±5	LSB max	Input Range: ±5 V
T_{min} to T_{max}	±5	±5	±5	LSB max	
Unipolar Gain Error @ +25°C	±5	±5	±5	LSB max	Input Range: 0 to 5 V or 0 to 10 V
T_{min} to T_{max}	±5	±5	±5	LSB max	
Bipolar Gain Error @ +25°C	±5	±5	±5	LSB max	Input Range: ±5 V
T_{min} to T_{max}	±5	±5	±5	LSB max	
ANALOG INPUT					
Unipolar Input Current	1.5	1.5	1.5	mA max	Input Ranges: 0 to 5 V or 0 to 10 V
Bipolar Input Current	±0.75	±0.75	±0.75	mA max	Input Range: ±5 V
REFERENCE INPUT					
V_{REF}	−3.5	−3.5	−3.5	Volts	±2% For Specified Performance
Input Reference Current	−10	−10	−10	mA max	
R1, Resistance	9	9	9	kΩ nom	±25%
R2, Resistance	6.3	6.3	6.3	kΩ nom	±25%
R2/R1 Ratio	0.7	0.7	0.7	nom	±0.1%
POWER SUPPLY REJECTION					
V_{DD} Only, (FS Change)	0.5	0.5	0.5	LSB typ	V_{SS} = −5 V, V_{DD} = +4.75 V to +5.25 V
V_{SS} Only, (FS Change)	0.5	0.5	0.5	LSB typ	V_{DD} = +5 V, V_{SS} = −4.75 V to −5.25 V
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	10	pF max	
LOGIC OUTPUTS					
DB11–DB0, $\overline{BUSY}$					
Output High Voltage, V_{OH}	4	4	4	V min	I_{SOURCE} = 200 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0					
Floating-State Leakage Current	±10	±10	±10	μA max	
Floating-State Output Capacitance[4]	15	15	15	pF max	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	35	35	35	mA max	Typically 25 mA, $\overline{CONVST}$ = $\overline{CS}$ = $\overline{RD}$ = V_{DD}
I_{SS}	−35	−35	−35	mA max	Typically 25 mA, $\overline{CONVST}$ = $\overline{CS}$ = $\overline{RD}$ = V_{DD}
Power Dissipation	250	250	250	mW typ	$\overline{CONVST}$ = $\overline{CS}$ = $\overline{RD}$ = V_{DD}
	350	350	350	mW max	

NOTES
[1]Temperature ranges are as follows: J, K Versions: 0°C to +70°C; B Version: −40°C to +85°C; T Version: −55°C to +125°C.
[2]Applies to all three input ranges, VIN = 0 to FS, pk-to-pk V.
[3]SNR calculation includes distortion and noise components.
[4]Sample tested @+25°C to ensure compliance.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V)

Parameter	Limit at T_{min}, T_{max} (J, K Versions)	Limit at T_{min}, T_{max} (B Version)	Limit at T_{min}, T_{max} (T Version)	Units	Conditions/Comments
t_1	50	50	50	ns min	$\overline{CONVST}$ Pulse Width
	1	1	1	µs max	
t_2	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_3	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_4	**60**	**60**	75	ns min	$\overline{RD}$ Pulse Width
t_5	100	100	100	ns max	$\overline{CONVST}$ to $\overline{BUSY}$ Propagation Delay, (C_L = 10 pF)
t_6[2]	57	57	70	ns max	Data Access Time After $\overline{RD}$
t_7[3]	**10**	**10**	**10**	ns min	Bus Relinquish Time After $\overline{RD}$
	50	**50**	**60**	ns max	
t_8	20	20	14	ns min	Data Setup Time Prior to $\overline{BUSY}$, (C_L = 20 pF)
	10	10	0	ns min	Data Setup Time Prior to $\overline{BUSY}$, (C_L = 100 pF)
t_9[3]	10	10	10	ns min	Bus Relinquish Time After $\overline{CONVST}$
	100	100	100	ns max	
t_{10}	0	0	0	ns min	$\overline{CS}$ High to $\overline{CONVST}$ Low
t_{11}	0	0	0	ns min	$\overline{BUSY}$ High to $\overline{RD}$ Low
t_{12}	250	250	250	ns typ	$\overline{BUSY}$ High to $\overline{CONVST}$ Low, SHA Acquisition Time
t_{13}	1.333	1.333	1.333	µs min	Sampling Interval
t_{CONV}	950	950	950	ns typ	Conversion Time
	1000	**1000**	**1000**	ns max	

NOTES

[1]Timing specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]t_6 is measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[3]t_7 and t_9 are derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the load capacitor, C_L. This means that the times, t_7 and t_9, quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

Specifications subject to change without notice.

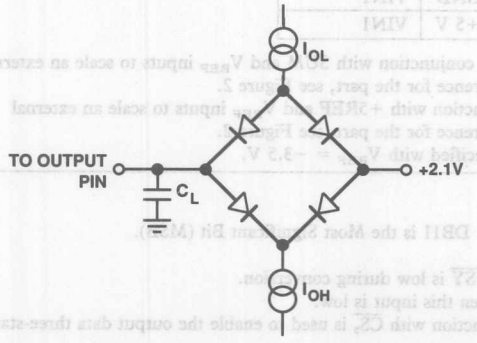


Figure 1. Load Circuit for Bus Access and Relinquish Time

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{SS} to AGND . . . . . +0.3 V to −7 V
AGND to DGND . . . . . −0.3 V to V_{DD} +0.3 V
VIN1, VIN2, SUM, +5REF to AGND . . . . −15 V to +15 V
V_{REF} to AGND . . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
Digital Inputs to DGND
$\overline{CS}$, $\overline{RD}$, $\overline{CONVST}$ . . . . . −0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND
DB0 to DB11, $\overline{BUSY}$ . . . . . −0.3 V to V_{DD} +0.3V
Operating Temperature Range
Commercial (J, K Versions) . . . . . 0°C to +70°C
Industrial (B Version) . . . . . −40°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]If V_{SS} is open circuited with V_{DD} and AGND applied, the V_{SS} pin will be pulled positive, exceeding the Absolute Maximum Ratings. If this possibility exists, a Schottky diode from V_{SS} to DGND (cathode end to GND) ensures that the Absolute Maximum Ratings will be observed.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



ORDERING GUIDE

Model[1, 2]	Temperature Range	SNR (dBs)	Integral Nonlinearity (LSBs)	Package Option[3]
AD7886JD	0°C to +70°C	65		D-28
AD7886KD	0°C to +70°C	67	±2.0	D-28
AD7886JP	0°C to +70°C	65		P-28A[2]
AD7886KP	0°C to +70°C	67	±2.0	P-28A[2]
AD7886BD	−40°C to +85°C	67	±2.0	D-28
AD7886TD	−55°C to +125°C	65	±2.0	D-28

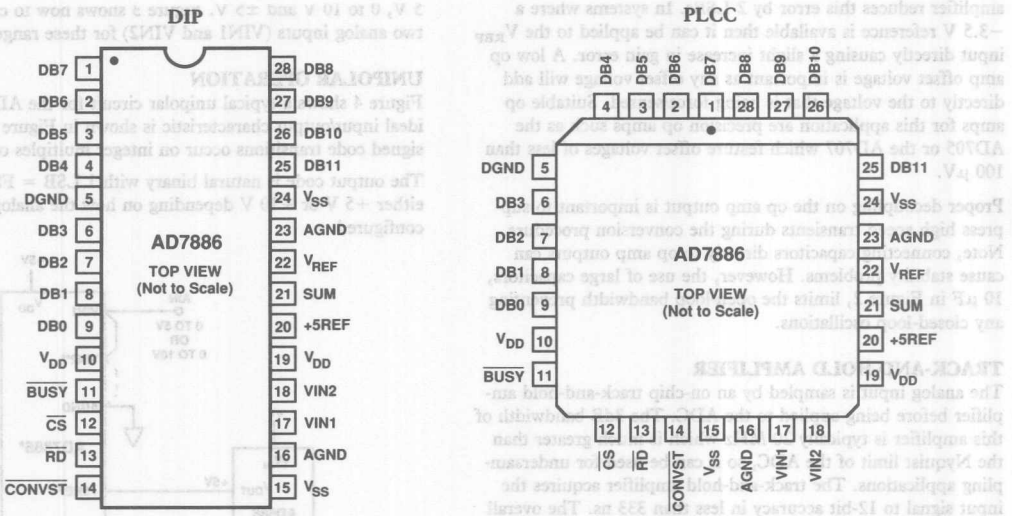
NOTES
[1]Contact your sales office for availability of AD7886BD and AD7886TD.
[2]Analog Devices reserves the right to ship J-Leaded Ceramic Chip Carrier (JLCCC) in lieu of PLCC packages.
[3]D = Ceramic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

PIN FUNCTION DESCRIPTION

DIP Pin Number	Mnemonic	Description
Power Supply		
10 & 19	V_{DD}	Positive Power Supply, +5 V ± 5%. Both V_{DD} pins must be tied together.
15 & 24	V_{SS}	Negative Power Supply, −5 V ± 5%. Both V_{SS} pins must be tied together.
16 & 23	AGND	Analog Ground. Both AGND pins must be tied together.
5	DGND	Digital Ground.
Analog and Reference Inputs		
17 & 18	VIN	Analog Inputs, VIN1 and VIN2. The part can be pin strapped for any one of three analog input ranges;

Range	Pin Strap	Signal Input
0 to 5 V	Connect VIN2 to VIN1	VIN1 & VIN2
0 to 10 V	Connect VIN2 to GND	VIN1
±5 V	Connect VIN2 to +5 V	VIN1

20	+5REF	+5 V Reference input. This input is used in conjunction with SUM and V_{REF} inputs to scale an external +5 V reference to −3.5 V, the required reference for the part, see Figure 2.
21	SUM	Summing Point. This input is used in conjunction with +5REF and V_{REF} inputs to scale an external +5 V reference to −3.5 V, the required reference for the part, see Figure 2.
22	V_{REF}	Voltage Reference Input. The AD7886 is specified with V_{REF} = −3.5 V.
Interface and Control		
1–4,	DB7–DB4	Three-state data outputs.
6–9,	DB3–DB0	These outputs are controlled by $\overline{CS}$ and $\overline{RD}$. DB11 is the Most Significant Bit (MSB).
25–28	DB11–DB8	
11	$\overline{BUSY}$	$\overline{BUSY}$ Output indicates converter status. $\overline{BUSY}$ is low during conversion.
12	$\overline{CS}$	Chip Select Input. The device is selected when this input is low.
13	$\overline{RD}$	Read Input. This active low signal, in conjunction with $\overline{CS}$, is used to enable the output data three-state drivers.
14	$\overline{CONVST}$	Conversion Start Input. This input is used to start conversion.



TERMINOLOGY

Unipolar Offset Error

The ideal first code transition should occur when the analog input is 1 LSB above AGND. The deviation of the actual transition from that point is termed the offset error.

Bipolar Zero Error

The ideal midscale transition (i.e., 0111 1111 1111 to 1000 0000 0000 for the ±5 V range should occur when the analog input is at zero volts. Bipolar zero error is the deviation of the actual transition from that point.

Gain Error

In the unipolar mode, gain error is measured with respect to the first and last code transition points. The ideal difference between these points if FS−2 LSBs. For bipolar applications, the gain error is measured from the midscale transition to both the first and last code transitions. The ideal difference in this case is FS/2−1 LSB. The gain error is defined as the deviation between the ideal difference, given above, and the measured difference. For the bipolar case, there are two gain errors, the figure in the specification page represents the worst case. Ideal FS depends on the +5REF input; for the 0 to 5 V input, ideal FS = +5REF and for the 0 to 10 V and ±5 V ranges, ideal FS = 2 × +5REF.

CONVERTER DETAILS

The AD7886 is a triple-pass flash ADC which uses 15 comparators in a 4-bit flash technique to perform the 12-bit conversion procedure. Each of the 4096 quantization levels is realized internally with a precision resistor DAC.

The fifteen comparators first compare the analog input voltage to the $V_{REF}/16$ voltages of the resistor array. This determines the four most significant bits and selects 1 out of 16 voltage segments. The comparators are then switched to 15 subvoltages on that segment to determine the next four bits and select 1 out of 256 voltage segments. A further switching of the comparators to another 15 subvoltages produces the complete 12-bit conversion result. The 12 bits of data are then stored internally in a three-state output latch.

REFERENCE INPUT

The AD7886 operates from a −3.5 V reference which must be provided at the V_{REF} input. Two on-chip resistors for use with an external amplifier can be used for deriving −3.5 V from standard 5 V references. Figure 2 shows an example with the AD586 which a is a high performance voltage reference which exhibits excellent stability performance, 5 ppm/°C max. The external amplifier serves a second function of force/sensing the V_{REF} input. Force/sensing minimizes error contributions from

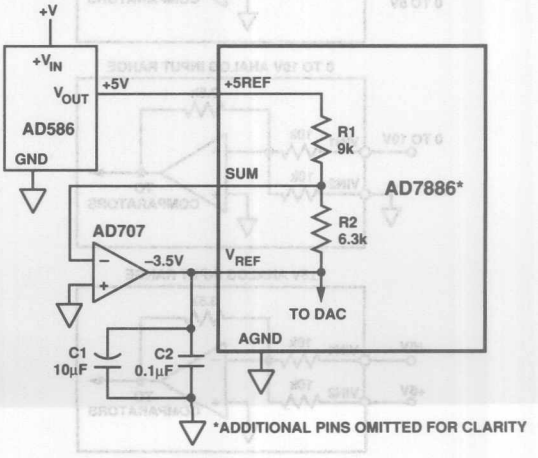


Figure 2. Typical Reference Circuitry

voltage or IR drops along the internal conductors. IR drops in the reference path cause a gain error, and typically the external amplifier reduces this error by 2 LSBs. In systems where a −3.5 V reference is available then it can be applied to the V_{REF} input directly causing a slight increase in gain error. A low op amp offset voltage is important as any offset voltage will add directly to the voltage that is being force/sensed. Suitable op amps for this application are precision op amps such as the AD705 or the AD707 which feature offset voltages of less than 100 μV.

Proper decoupling on the op amp output is important to suppress high speed transients during the conversion procedure. Note, connecting capacitors directly to op amp outputs can cause stability problems. However, the use of large capacitors, 10 μF in Figure 2, limits the open-loop bandwidth preventing any closed-loop oscillations.

TRACK-AND-HOLD AMPLIFIER

The analog input is sampled by an on-chip track-and-hold amplifier before being applied to the ADC. The 3dB bandwidth of this amplifier is typically 20 MHz which is much greater than the Nyquist limit of the ADC, so it can be used for undersampling applications. The track-and-hold amplifier acquires the input signal to 12-bit accuracy in less than 333 ns. The overall throughput time is equal to the conversion time plus the track/hold amplifier acquisition time which is 1.333 μs for the AD7886.

The operation of the track/hold amplifier is essentially transparent to the user. The track-to-hold transition occurs at the start of conversion on the falling edge of $\overline{\text{CONVST}}$. The conversion procedure does not start until the rising edge of $\overline{\text{CONVST}}$. The width of the $\overline{\text{CONVST}}$ pulse low time determines the track-to-hold settling time. The track/hold reverts back to the track mode at the end of conversion when $\overline{\text{BUSY}}$ has returned high.

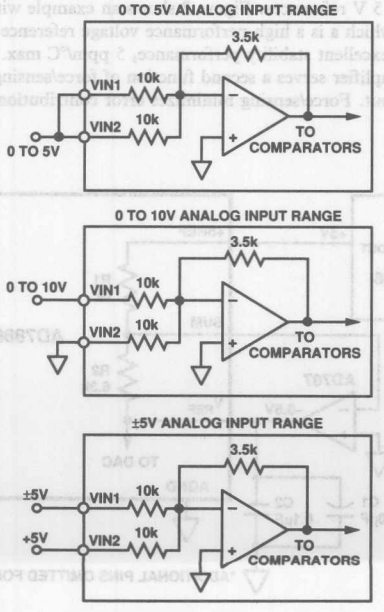


Figure 3. Analog Input Range Configurations

ANALOG INPUT RANGES

The AD7886 has three user selectable analog input ranges: 0 to 5 V, 0 to 10 V and ±5 V. Figure 3 shows how to configure the two analog inputs (VIN1 and VIN2) for these ranges.

UNIPOLAR OPERATION

Figure 4 shows a typical unipolar circuit for the AD7886. The ideal input/output characteristic is shown in Figure 5. The designed code transitions occur on integer multiples of 1 LSB.

The output code is natural binary with 1 LSB = FS/4096. FS is either +5 V or +10 V depending on how the analog inputs are configured.

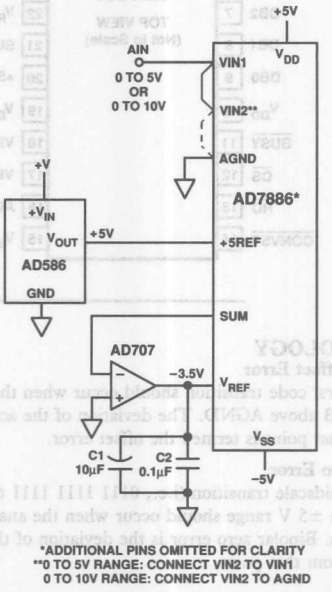


Figure 4. Unipolar Operation

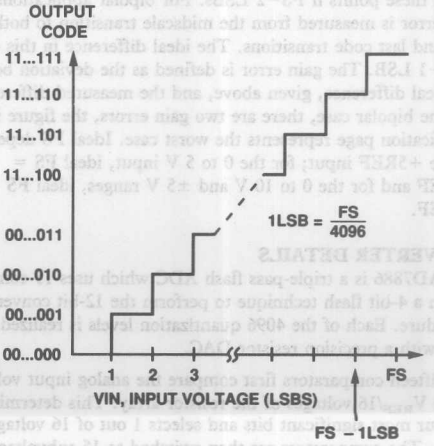


Figure 5. Ideal Input/Output Transfer Characteristic for Unipolar Operation

OFFSET AND GAIN ADJUSTMENT

In most digital signal processing (DSP) applications, offset and full-scale errors have little or no effect on system performance. Offset error can usually be eliminated in the analog domain by ac coupling. Full-scale errors do not cause problems as long as the input signal is within the full dynamic range of the ADC. For applications which require that the input signal range match the full analog input dynamic range of the ADC, offset and full-scale errors have to be adjusted to zero.

UNIPOLAR OFFSET AND GAIN ERROR ADJUSTMENT

If absolute accuracy is an application requirement, then offset and gain can be adjusted to zero. Offset error must be adjusted before gain error. Zero offset is achieved by adjusting the offset of the op amp driving the analog input (i.e., A1 in Figure 6). For zero offset error apply a voltage of 1 LSB to AIN and adjust the op amp offset until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

0 to 5 V Range: 1 LSB = 1.22 mV
0 to 10 V Range: 1 LSB = 2.44 mV

For zero gain error apply an analog input voltage equal to FS−1 LSB (last code transition) at AIN and adjust R3 until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

0 to 5 V Range: FS−1 LSB = 4.99878 V
0 to 10 V Range: FS−1 LSB = 9.99756 V

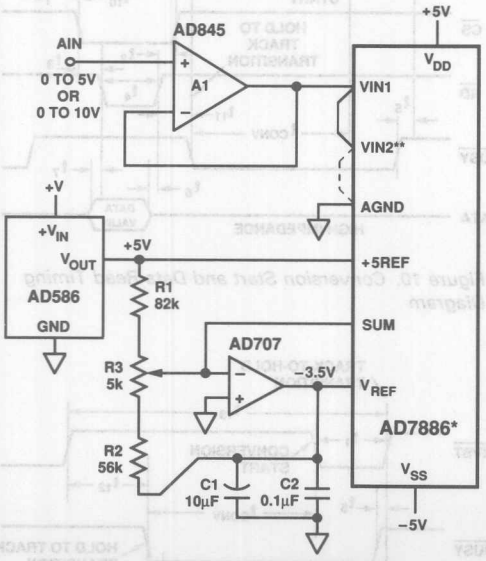


Figure 6. Unipolar Operation with Gain Error Adjust

BIPOLAR OPERATION

Bipolar operation is achieved by providing a +10 V span on the VIN1 input while offsetting the VIN2 input by +5 V. A typical circuit is shown in Figure 7. The output code is offset binary. The ideal input/output transfer characteristic is shown in Figure 8. The LSB size is (10/4096) V = 2.44 mV.

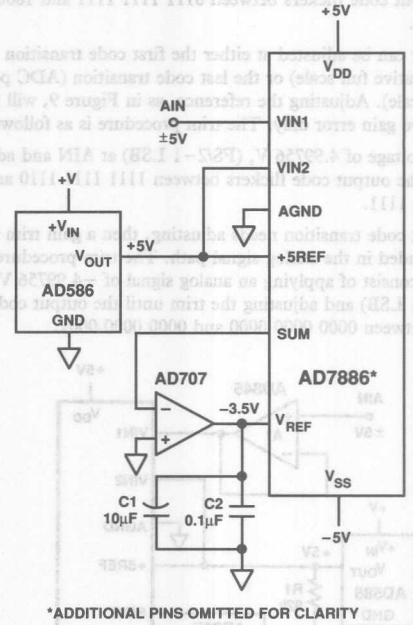


Figure 7. Bipolar Operation

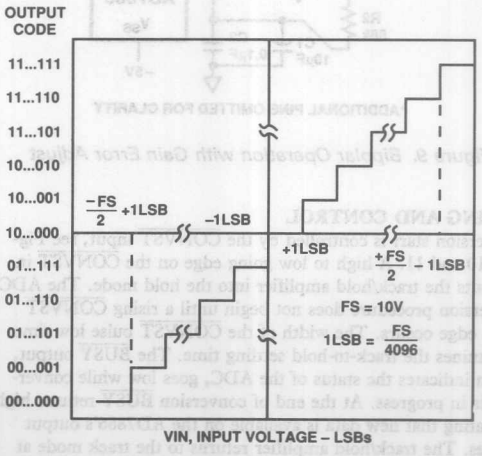


Figure 8. Ideal Input/Output Characteristics for Bipolar Operation

BIPOLAR OFFSET AND GAIN ADJUSTMENT

In applications where absolute accuracy is important then offset and gain error can be adjusted to zero. Offset is adjusted by trimming the voltage at the VIN1 or VIN2 input when the analog input is at zero volts. This can be achieved by adjusting the offset of an external amplifier used to drive either of these inputs, see A1 in Figure 9. The trim procedure is as follows:

Apply zero volts at AIN and adjust the offset of A1 until the ADC output code flickers between 0111 1111 1111 and 1000 0000 0000.

Gain error can be adjusted at either the first code transition (ADC negative full scale) or the last code transition (ADC positive full scale). Adjusting the reference, as in Figure 9, will trim the positive gain error only. The trim procedure is as follows:

Apply a voltage of 4.99756 V, (FS/2−1 LSB) at AIN and adjust R3 until the output code flickers between 1111 1111 1110 and 1111 1111 1111.

If the first code transition needs adjusting, then a gain trim has to be included in the analog signal path. The trim procedure will then consist of applying an analog signal of −4.99756 V, (−FS/2+1 LSB) and adjusting the trim until the output code flickers between 0000 0000 0000 and 0000 0000 0001.

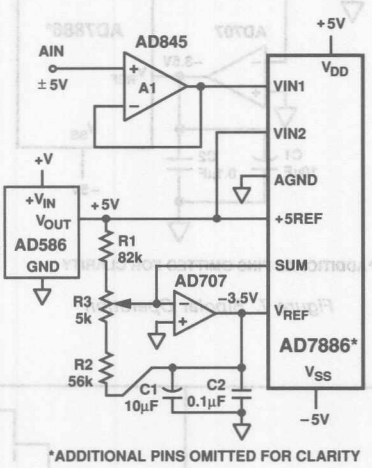


Figure 9. Bipolar Operation with Gain Error Adjust

TIMING AND CONTROL

Conversion start is controlled by the $\overline{\text{CONVST}}$ input, see Figures 10 and 11. A high to low going edge on the $\overline{\text{CONVST}}$ input puts the track/hold amplifier into the hold mode. The ADC conversion procedure does not begin until a rising $\overline{\text{CONVST}}$ pulse edge occurs. The width of the $\overline{\text{CONVST}}$ pulse low time determines the track-to-hold settling time. The $\overline{\text{BUSY}}$ output, which indicates the status of the ADC, goes low while conversion is in progress. At the end of conversion $\overline{\text{BUSY}}$ returns high indicating that new data is available on the AD7886's output latches. The track/hold amplifier returns to the track mode at the end of conversion and remains there until the next $\overline{\text{CONVST}}$ pulse. Conversion starts must not be attempted while conversion is in progress as this will cause erroneous results.

Data read operations are controlled by the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs. These digital inputs, when low, enable the AD7886's three-state output latches. Note, these latches cannot be enabled during conversion. In applications where $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are tied permanently low, as in Figure 11, the data bus will go into the three-state condition at the start of conversion and return to its active state when conversion is complete. Tying $\overline{\text{CS}}$ and $\overline{\text{RD}}$ permanently low is useful when external latches are used to store the conversion results. The data bus becomes active before $\overline{\text{BUSY}}$ returns high at the end of conversion, so that $\overline{\text{BUSY}}$ can be used as a clocking signal for the external latches.

A typical DSP application would have a timer connected to the $\overline{\text{CONVST}}$ input for precise sampling intervals. $\overline{\text{BUSY}}$ would be connected to the interrupt of a microprocessor which would be asserted at the end of every conversion. The microprocessor would then assert the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs and read the data from the ADC. For applications where both data reading and conversion control need to be managed by a microprocessor, then a $\overline{\text{CONVST}}$ pulse can be decoded from the address bus. One decoding possibility is that a write instruction to the ADC address starts a conversion and a read instruction reads the conversion result.

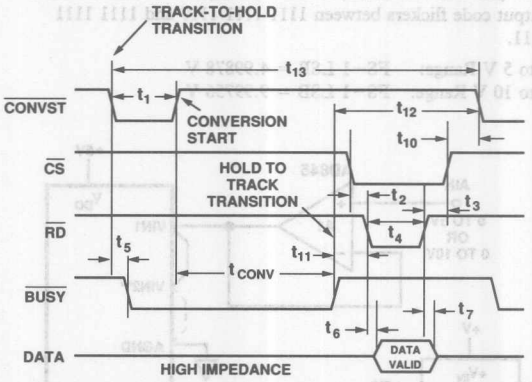


Figure 10. Conversion Start and Data Read Timing Diagram

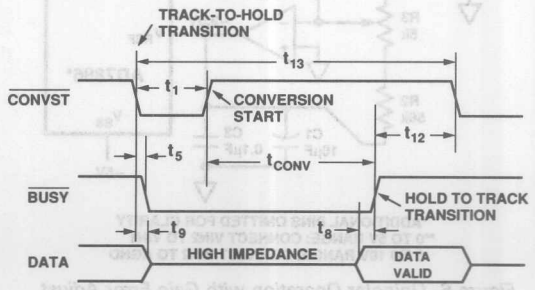


Figure 11. Conversion Start and Data Read Timing Diagram, ($\overline{CS}$ = $\overline{RD}$ = 0 V)

AD7886 DYNAMIC SPECIFICATIONS

The AD7886 is specified for dynamic performance specifications as well as traditional dc specifications such as integral and differential nonlinearity. These ac specifications are required for the signal processing applications such as speech recognition, spectrum analysis, and high speed modems. These applications require information on the ADC's effect on the spectral content of the input signal. Hence, the parameters for which the AD7886 is specified include SNR, harmonic distortion, intermodulation distortion and peak harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal-to-noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (FS/2) excluding dc. SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to noise ratio for a sine wave input is given by

$$SNR = (6.02N + 1.76)\ dB \quad (1)$$

where N is the number of bits. Thus for an ideal 12-bit converter, SNR = 74dB.

The output spectrum from the ADC is evaluated by applying a sine wave signal of very low distortion to the VIN input which is sampled at a 750 kHz sampling rate. A Fast Fourier Transform (FFT) plot is generated from which the SNR data can be obtained. Figure 12 shows a typical 2048 point FFT plot with an input signal of 100 kHz and a sampling frequency of 750 kHz. The SNR obtained from this graph is 68 dB. It should be noted that the harmonics are taken into account when calculating the SNR.

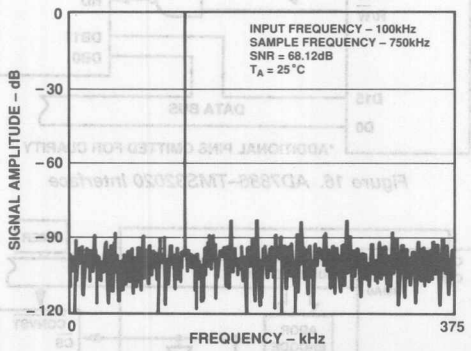


Figure 12. AD7886 FFT Plot

Effective Number of Bits

The formula given in Equation 1 relates the SNR to the number of bits. Rewriting the formula, as in Equation 2, it is possible to get a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \quad (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR.

Figure 13 shows a typical plot of effective number of bits versus frequency for a sampling frequency of 750 kHz. Input frequency range for this particular graph was limited by the test equipment to FS/4. The effective number of bits typically falls between 10.9 and 11.2 corresponding to SNR figures of 67.38 dB and 69.18 dB.

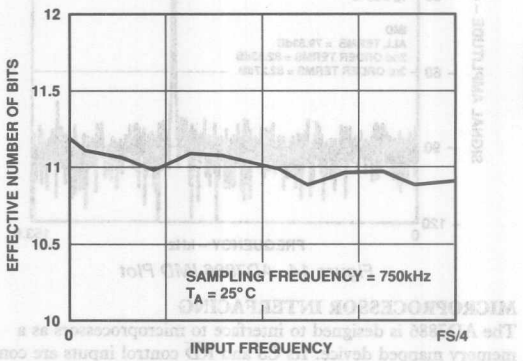


Figure 13. Effective Number of Bits vs. Frequency

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7886, THD is defined as

$$THD = 20\ log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1} \quad (3)$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through to the sixth harmonic. The THD is also derived from the FFT plot of the ADC output spectrum.

Intermodulation Distortion (IMD)

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa± nfb where m,n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m or n are equal to zero. For example, the second order terms include (fa + fb) and (fa − fb) while the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb).

Using the CCIF standard where two input frequencies near the top end of the input bandwidth are used, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs. In this case, the input consists of two, equal amplitude, low distortion sine waves. Figure 14 shows a typical IMD plot for the AD7886.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to FS/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification will be

parts where the harmonics are buried in the noise floor the peak will be a noise peak.

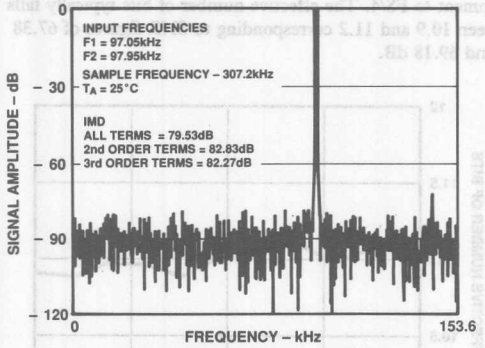


Figure 14. AD7886 IMD Plot

MICROPROCESSOR INTERFACING

The AD7886 is designed to interface to microprocessors as a memory mapped device. Its $\overline{CS}$ and $\overline{RD}$ control inputs are common to all memory peripheral interfacing. Figures 15 to 21 demonstrate typical interfaces for the AD7886.

AD7886–TMS320C10/TMS32020

Figures 15 and 16 show typical interfaces for the TMS320C10 and the TMS32020 DSP processors. An external timer controls conversion start to the processor. At the end of each conversion the ADC's $\overline{BUSY}$ output interrupts the microprocessor. The conversion result can then be read from the ADC with the following instruction:

IN D,ADC (ADC = ADC address)

AD7886– ADSP-2100/TMS320C25/DSP56000

Some of the faster DSP processors have data access times which are outside the capabilities of the AD7886. Interfacing to such processors requires the use of either a single WAIT state or external latches. Examples are shown in Figures 17, 18 and 19.

The use of a single WAIT state for the TMS320C25 and the ADSP-2100 interfaces extends the read instruction to the ADC by one processor CLK OUT cycle. In the DSP56000 example the ADC's data is first clocked into 74HC374 latches before being read by the processor. The AD7886's $\overline{CS}$ and $\overline{RD}$ inputs are tied permanently low, and the rising edge of $\overline{BUSY}$ updates the latches at the end of conversion. Both methods of overcoming the very fast data access time required by these processors are interchangeable, i.e., a WAIT state can be used for the DSP56000 eliminating the need for latches or vice versa for the other two interfaces.

For all three interfaces, an external timer controls conversion start, the processor is interrupted at the end of each conversion by the ADC's $\overline{BUSY}$ output. The following instruction then reads data from the ADC:

ADSP-2100 – MR = DM(ADC)
TMS320C25 – IN D,ADC
DSP56000 – MOVEP Y:ADC,XO

Assuming the ADC is memory mapped into the top 64 locations in Y memory space.
(ADC = ADC address)

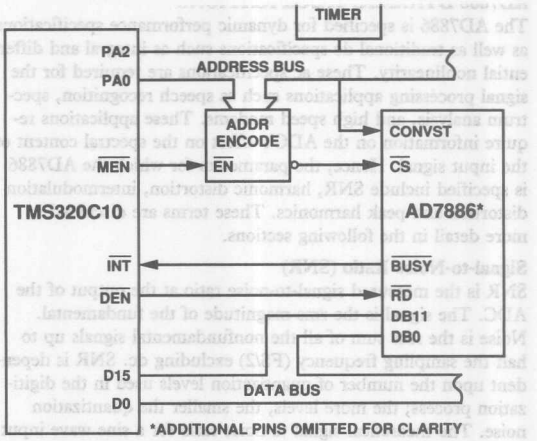


Figure 15. AD7886–TMS320C10 Interface

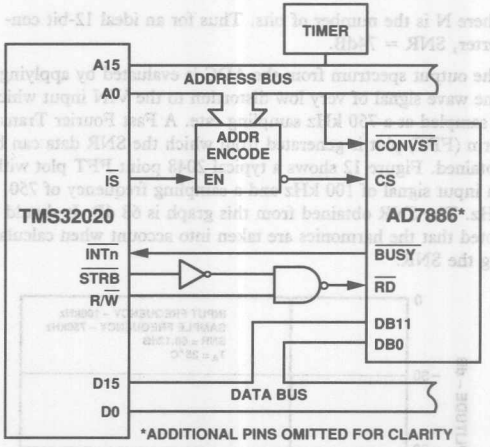


Figure 16. AD7886–TMS32020 Interface

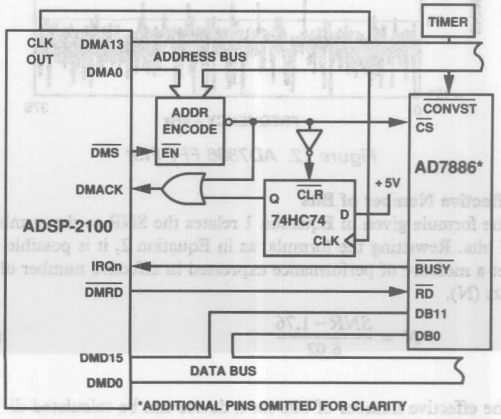


Figure 17. AD7886–ADSP-2100 Interface

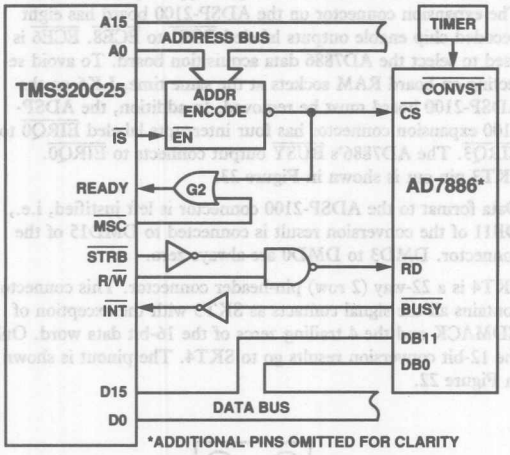


Figure 18. AD7886–TMS320C25 Interface

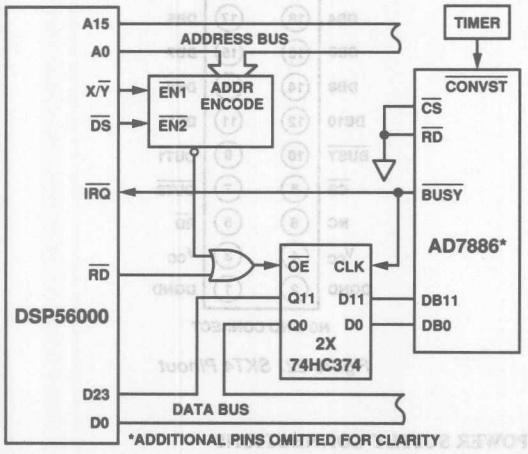


Figure 19. AD7886–DSP56000 Interface

AD7886–MC68000

Applications that require conversions to be initiated by the microprocessor rather than an external timer may decode a $\overline{\text{CONVST}}$ signal from the address bus. An example is given in Figure 20 with the MC68000 processor. A write instruction starts conversion while a read instruction reads the data when conversion is complete. A delay at least as long as the ADC conversion time must allowed between initiating a conversion and reading the ADC data into the processor. In Figure 20, $\overline{\text{BUSY}}$ is used to drive the processor into a WAIT state if the processor attempts to read data before conversion is complete.

Conversion is initiated with a write instruction to the ADC:

Move.W D0,ADC (ADC = ADC address)

Data is transferred to the processor with a read instruction, $\overline{\text{BUSY}}$ will force the processor to WAIT for the end of conversion if a conversion is in progress.

Move.W ADC,DO (ADC = ADC address)

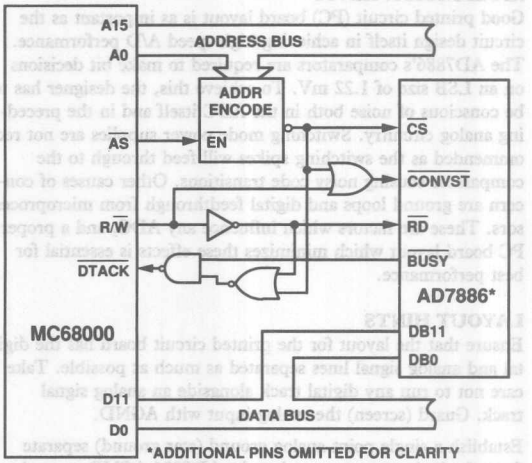


Figure 20. AD7886–MC68000 Interface

AD7886–Z-80/8085A

For 8-bit processors an external latch is required to store 4-bits of the conversion result (4 LSBs in Figure 21). The data is then read in two bytes: one read from the ADC and a second from the latch.

Figure 21 shows a typical interface that is suitable for the Z-80 or the 8085A. Not shown in the Figure is the 8-bit latch needed to demultiplex the 8085A common address/data bus. The following LOAD instruction reads the conversion result into the HL register pair.

For the 8085A – LHLD (ADC) (ADC = ADC address)
For the Z-80–LDHL (ADC) (ADC = ADC address)

This is a two byte read instruction. The first byte to be read has to be the high byte (DB11 to DB4). At the end of the first read operation, the rising edge of $\overline{\text{CS}}$ and $\overline{\text{RD}}$ clocks the 4 LSBs into 74HC374 latches. The second byte (4 LSBs) is then read from these latches.

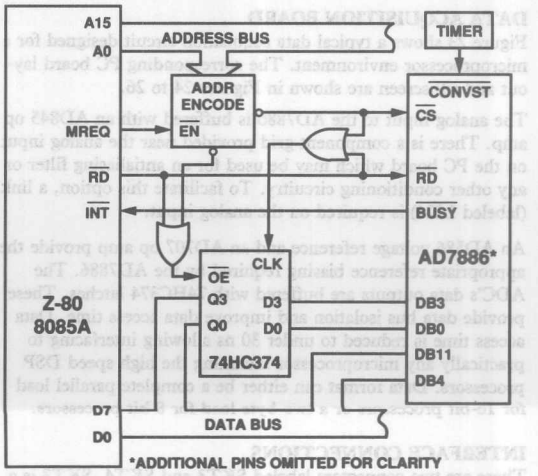


Figure 21. AD7886–Z-80/8085A Interface

APPLICATION HINTS

Good printed circuit (PC) board layout is as important as the circuit design itself in achieving high speed A/D performance. The AD7886's comparators are required to make bit decisions on an LSB size of 1.22 mV. To achieve this, the designer has to be conscious of noise both in the ADC itself and in the preceding analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any ADC, and a proper PC board layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground at the AD7886 AGND or as close as possible to the AD7886. Connect all other grounds and the AD7886 DGND to this single analog ground point. Do not connect any other digital grounds to this analog ground point.

Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise. The circuit layout of Figures 25 and 26 have both analog and digital ground planes which are kept separated and only joined together at the AD7886 AGND.

NOISE

Keep the input signal leads to VIN and signal return leads from AGND as short as possible to minimize input noise coupling. In applications where this is not possible, use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

DATA ACQUISITION BOARD

Figure 23 shows a typical data acquisition circuit designed for a microprocessor environment. The corresponding PC board layout and silkscreen are shown in Figures 24 to 26.

The analog input to the AD7886 is buffered with an AD845 op amp. There is a component grid provided near the analog input on the PC board which may be used for an antialiasing filter or any other conditioning circuitry. To facilitate this option, a link (labeled LK4) is required on the analog input.

An AD586 voltage reference and an AD707 op amp provide the appropriate reference biasing required by the AD7886. The ADC's data outputs are buffered with 74HC374 latches. These provide data bus isolation and improve data access time. Data access time is reduced to under 30 ns allowing interfacing to practically any microprocessor including the high speed DSP processors. Data format can either be a complete parallel load for 16-bit processors or a two-byte load for 8-bit processors.

INTERFACE CONNECTIONS

There are two connectors labeled SKT3 and SKT4. SKT3 is a 96-contact (3-row) connector which is directly compatible with the ADSP-2100 evaluation board prototype expansion connector. The expansion connector on the ADSP-2100 board has eight decoded chip enable outputs labeled $\overline{\text{ECE1}}$ to $\overline{\text{ECE8}}$. $\overline{\text{ECE6}}$ is used to select the AD7886 data acquisition board. To avoid selecting on-board RAM sockets at the same time, LK6 on the ADSP-2100 board must be removed. In addition, the ADSP-2100 expansion connector has four interrupts labeled $\overline{\text{EIRQ0}}$ to $\overline{\text{EIRQ3}}$. The AD7886's $\overline{\text{BUSY}}$ output connects to $\overline{\text{EIRQ0}}$. SKT3 pin out is shown in Figure 23.

Data format to the ADSP-2100 connector is left justified, i.e., DB11 of the conversion result is connected to DMD15 of the connector. DMD3 to DMD0 are always zero.

SKT4 is a 22-way (2 row) pin-header connector. This connector contains all the signal contacts as SKT3 with the exception of EDMACK and the 4 trailing zeros of the 16-bit data word. Only the 12-bit conversion results go to SKT4. The pinout is shown in Figure 22.

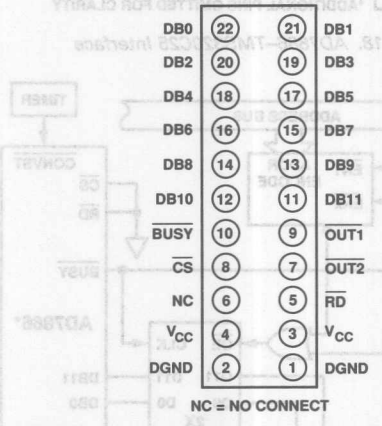


Figure 22. SKT4 Pinout

POWER SUPPLY CONNECTIONS

The PC board requires two analog power supplies and one 5 V digital supply. Connections to the analog supply are made directly to the PC board as shown on the silkscreen in Figure 24. The connections are labeled V+ and V−, and the range for both of these supplies is 12 V to 15 V. Connection to the 5 V digital supply is made through either of the two connectors (SKT3 or SKT4). The ±5 V analog supplies required by the AD7886 are generated from voltage regulators on the V− and V+ power supplies.

LINK OPTIONS

There are five link options, labeled LK1 to LK5 which must be set before using the board.

LK1 Input Range Select

The AD7886 can accommodate three possible analog input ranges: 0 to 5 V, 0 to 10 V and ±5 V. The link options are as follows:

0 to 5 V	Use Link C
0 to 10 V	Use Link B
±5 V	Use Link A

LK2 and LK3 Control Input Options

The evaluation board includes two latches to increase the data access time when interfacing to the faster DSP machines. If these latches are not required, they may be removed and the data digital paths shorted out, i.e., latch inputs Dx shorted to outputs Qx using wire links in the latch sockets. When using the latches, the AD7886 control inputs, $\overline{CS}$ and $\overline{RD}$, must be tied low via links 2 and 3. The latches are updated by the rising edge of the $\overline{BUSY}$ signal at the end of every conversion. Data is then read by asserting the latch output enable signals. The alternative is to remove the latches and assert the ADC's control inputs from either of the connectors, SKT3 or SKT4, as outlined in the data sheet.

Latches Included	Latches Removed
Insert Link 2	Remove Link 2
Insert Link 3	Remove Link 3

LK4 Analog Input Option

LK4 connects the analog input to a component grid or to a buffer amplifier which drives the ADC input.

LK5

Data format can be 16-bits parallel or two bytes for 8-bit processors. There are two data enable controls for the 74HC374 latches, labeled $\overline{OUT1}$ and $\overline{OUT2}$. $\overline{OUT1}$ enables the 8 MSBs (IC8), and $\overline{OUT2}$ enables the 4 LSBs (IC9). Link options are: for 16-bit format, include LK5 and for a two byte read format, remove LK5.

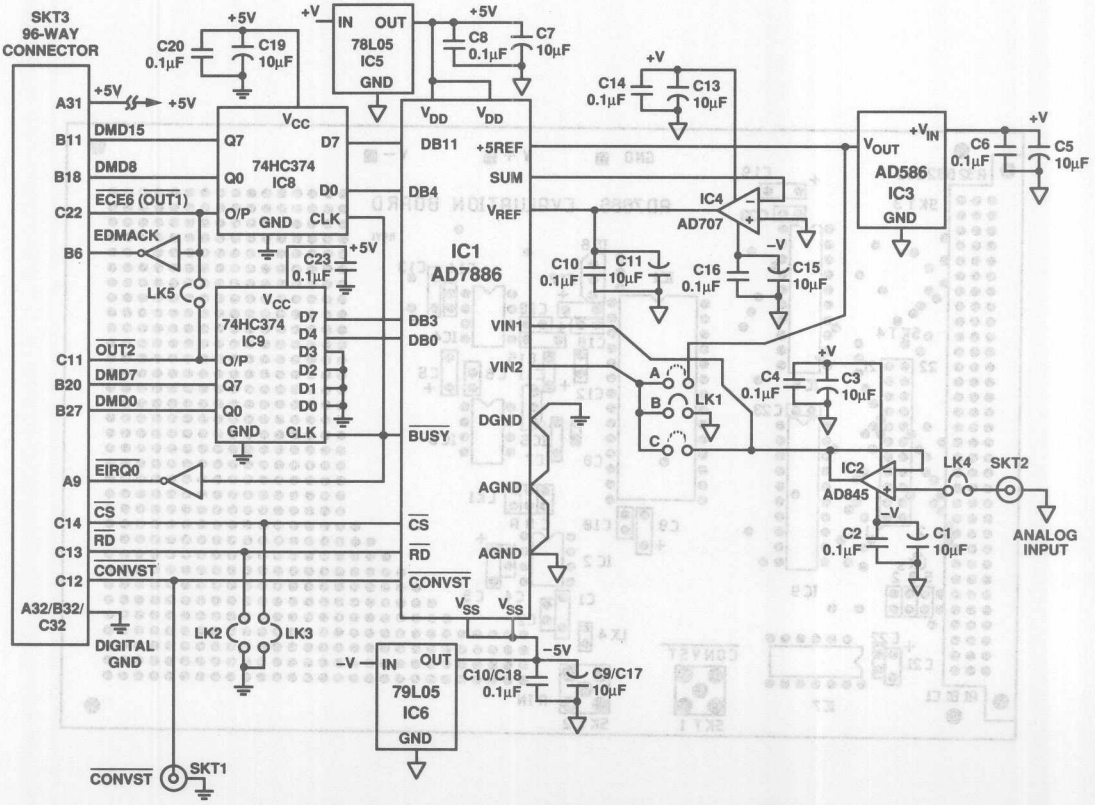


Figure 23. Data Acquisition Circuit Using the AD7886

COMPONENT LIST

IC1	AD7886, 12-Bit Sampling ADC
IC2	AD845, Op Amp
IC3	AD586, Precision Voltage Reference
IC4	AD707, Op Amp
IC5	MC78L05, +5 V Regulator
IC6	MC79L05, −5 V Regulator
IC7	74HC04, Hex Inverter
IC8. IC9	74HC374, Octal Latches with Three-State Outputs
C1, C3, C5, C7, C9, C11, C13, C15 C17, C19, C21	10 μF Capacitors
C2, C4, C6, C8, C10, C12, C14, C16, C18, C20, C22, C23	0.1 μF Capacitors
SKT1, SKT2	BNC Sockets
SKT3	96-Contact (3 Row) Eurocard Connector
SKT4	22-Way (2 Row) Pin Header and Socket

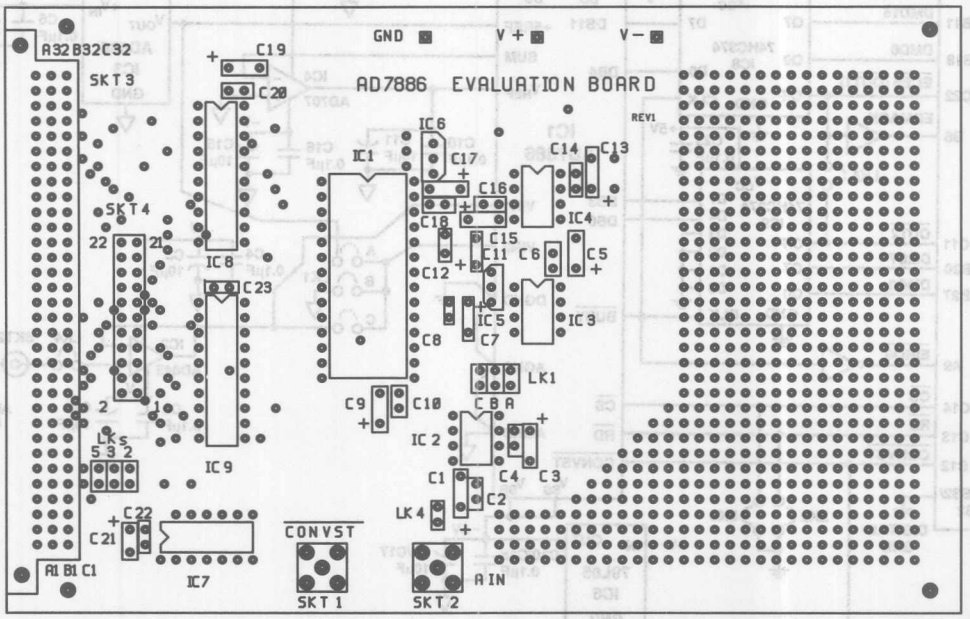


Figure 24. PC Board Silkscreen for Figure 23

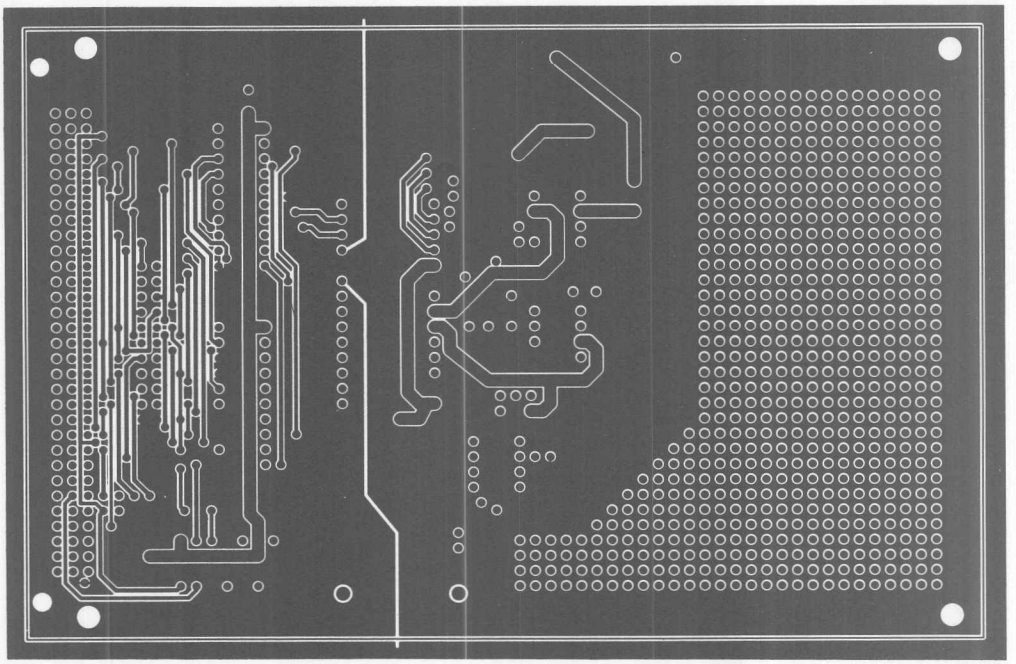


Figure 25. PC Board Component Side Layout for Figure 23

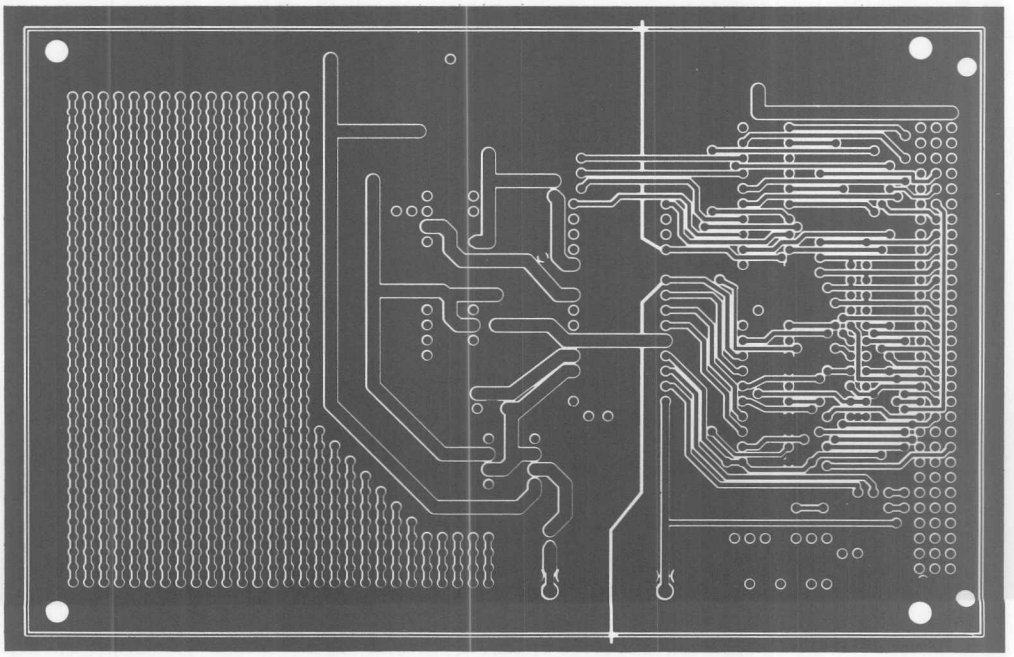
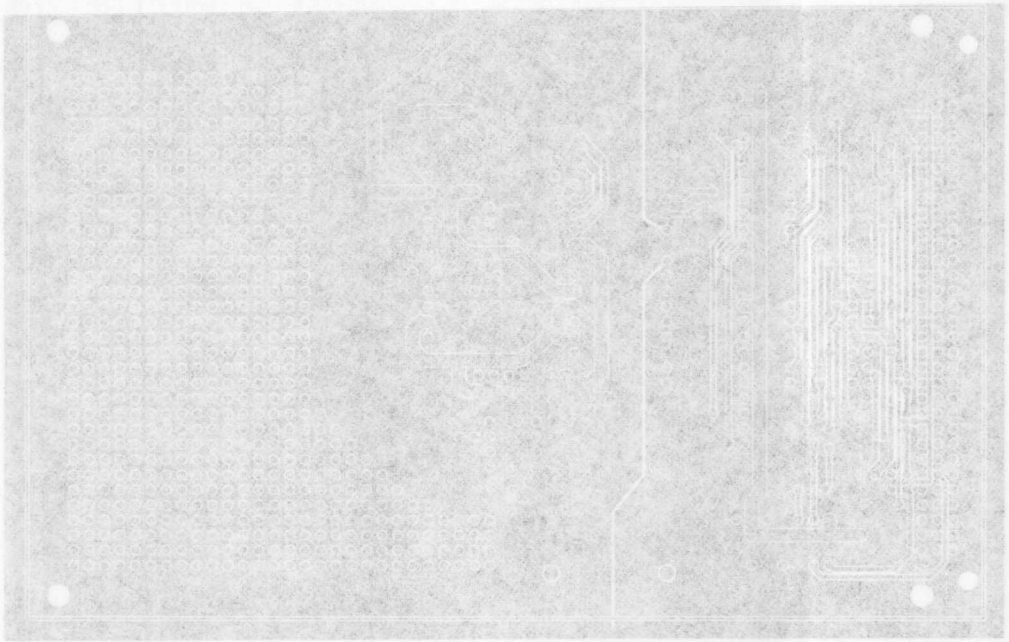
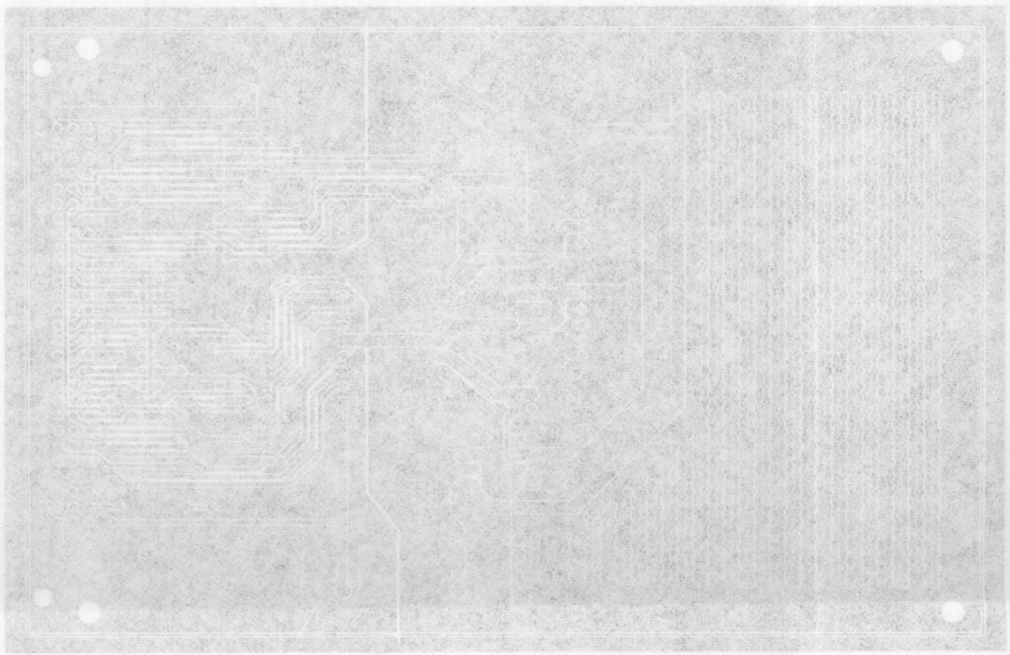


Figure 26. PC Board Solder Side Layout for Figure 23





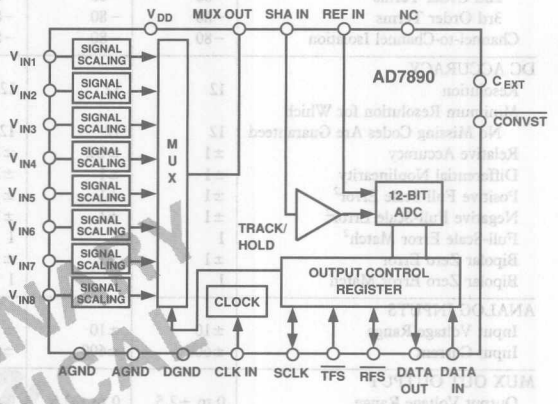
LC²MOS 8-Channel, 12-Bit Serial, Data Acquisition System

AD7890

FEATURES

- Fast 12-Bit ADC with 10 μs Conversion Time
- Eight Single-Ended Analog Input Channels
- ±10 V Input Range
- Allows Separate Access to Multiplexer and ADC
- On-Chip Track/Hold Amplifier
- High Speed, Flexible, Serial Interface
- Single Supply Operation
- Low Power, 50 mW max in Normal Operation
- Power-Down Mode

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7890 is an eight-channel 12-bit data acquisition system. The part contains an input multiplexer, an on-chip track/hold amplifier, a high speed 12-bit ADC and a high speed serial interface. The part operates from a single +5 V supply and accepts an analog input range of ±10 V.

The multiplexer on the part is independently accessible. This allows the user to insert an antialiasing filter, if required, between the multiplexer and the ADC. This means that one antialiasing filter can be used for all eight channels. Connection of an external capacitor allows the user to adjust the time given to the multiplexer settling to include any external delays in this antialiasing filter.

Output data from the AD7890 is provided via a high speed bidirectional serial interface port. The part contains an on-chip control register, allowing control of channel selection, conversion start, power-down, etc., via the serial port. Versatile, high speed logic ensures easy interfacing to serial ports on microcontrollers and digital signal processors.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7890 is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

Power dissipation in normal mode is low at 30 mW typ, and the part can be placed in a standby (power-down) mode if it is not required to performed conversions. The AD7890 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin, 0.3" wide, plastic or hermetic dual-in-line package or in a 24-pin small outline package (SOIC).

PRODUCT HIGHLIGHTS

1. Complete 12-Bit Data Acquisition System on a Chip
   The AD7890 is a complete monolithic ADC combining an eight-channel multiplexer, 12-bit ADC and a track/hold amplifier on a single chip.
2. Separate Access to Multiplexer and ADC
   The AD7890 provides access to the output of the multiplexer allowing the user to insert an antialiasing filter between the multiplexer and the ADC. This allows one antialiasing filter for eight channels—a considerable saving over the eight antialiasing filters required if the multiplexer was internally connected to the ADC.
3. High Speed Serial Interface
   The part provides a high speed serial interface for easy connection to serial ports of microcontrollers and DSP processors. An on-chip control register is programmed via this bidirectional serial port.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD7890—SPECIFICATIONS

(V_{DD} = +5 V, AGND = DGND = 0 V, REF IN = +2.5 V, f_{CLKIN} = 2.5 MHz external, MUX OUT connected to SHA IN. All specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	A Version[1]	B Version	S Version	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE					Any Channel
Signal-to-Noise Ratio @ +25°C	70	72	70	dB min	f_{IN} =10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
T_{MIN} to T_{MAX}	70	70	70	dB min	
Total Harmonic Distortion	−80	−80	−80	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
Peak Harmonic or Spurious Noise	−81	−81	−81	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
Intermodulation Distortion					fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 83 kHz
2nd Order Terms	−80	−80	−80	dB typ	
3rd Order Terms	−80	−80	−80	dB typ	
Channel-to-Channel Isolation	−80	−80	−80	dB max	f_{IN} = 1 kHz Sine Wave
DC ACCURACY					Any Channel
Resolution	12	12	12	Bits	
Minimum Resolution for Which No Missing Codes Are Guaranteed	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	LSB max	
Positive Full-Scale Error[2]	±1	±1	±1	LSB max	
Negative Full-Scale Error[2]	±1	±1	±1	LSB max	
Full-Scale Error Match[2]	1	1	1	LSB max	
Bipolar Zero Error	±1	±1	±1	LSB max	
Bipolar Zero Error Match	1	1	1	LSB max	
ANALOG INPUTS					
Input Voltage Range	±10	±10	±10	Volts	
Input Current	±600	±600	±600	μA max	
MUX OUT OUTPUT					
Output Voltage Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Output Resistance	2.9/4.2	2.9/4.2	2.9/4.2	kΩ min/ kΩ max	
SHA IN INPUT					
Input Voltage Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Input Current	50	50	50	nA max	
REFERENCE INPUT					
Input Voltage Range	2.375/2.625	2.375/2.625	2.375/2.625	V min/V max	2.5 V ± 5%
Input Current	4	4	4	mA max	Varies with ADC Code
Input Capacitance[3]	10	10	10	pF max	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[3]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 40 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
Serial Data Output Coding	2s COMPLEMENT				
CONVERSION RATE					
Conversion Time	10	10	10	μs max	$f_{CLK\ IN}$ = 2.5 MHz, MUX OUT Connected to SHA IN
Track/Hold Acquisition Time	2	2	2	μs max	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
I_{DD} (Normal Mode)	10	10	10	mA max	
I_{DD} (Standby Mode)	500	500	500	μA max	Logic Inputs = 0 V or V_{DD}
Power Dissipation (Normal Mode)	50	50	50	mW max	Typically 30 mW
Power Dissipation (Standby Mode)	2.5	2.5	2.5	mW max	Typically 1 mW

NOTES

[1]Temperature ranges are as follows: A, B Versions: −40°C to +85°C; S Version: −55°C to +125°C.

[2]Measured with respect to 4 × REF IN voltage and is calculated after the bipolar zero error has been adjusted out.

[3]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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PIN FUNCTION DESCRIPTION

Pin Mnemonic	Description
V_{IN1}–V_{IN8}	Analog Input Channels. These input channels provide eight single-ended inputs. The analog input range on each channel is ±10 V. The channel to be converted is selected using the A0, A1 and A2 bits in the control register. The multiplexer has guaranteed break-before-make operation.
MUX OUT	Multiplexer Output. The output of the multiplexer appears at this pin. The output voltage range from this output is 0 to +2.5 V for a ±10 V analog input to the selected channel. The output impedance of this output is nominally 3.5 kΩ. If no external antialiasing filter is required, MUX OUT should be connected to SHA IN.
SHA IN	Track/Hold Input. The input to the on-chip track/hold is applied to this pin. It is a high impedance input, and the input voltage range is 0 V to +2.5 V.
REF IN	Voltage Reference Input. The reference voltage for the part is applied to this pin. The input impedance of this reference input varies with the analog input voltage and REF IN should, therefore, be driven from a low impedance source. The nominal reference voltage for correct operation of the AD7890 is +2.5 V.
V_{DD}	Positive supply voltage, +5 V ± 5%.
AGND	Analog Ground. Ground reference for track/hold, comparator and DAC.
DGND	Digital Ground. Ground reference for digital circuitry.
SCLK	Serial Clock Input. In the external clocking (slave) mode (see DIGITAL INTERFACE section) this is an externally applied serial clock which is used to load serial data to the control register and to access data from the output register. In the self-clocking (master) mode, the internal serial clock, which is derived from the clock input (CLK IN), appears on this pin. Once again, it is used to load serial data to the control register and to access data from the output register.
$\overline{TFS}$	Transmit Frame Synchronization Pulse. Active low logic input with serial data expected after the falling edge of this signal.
DATA IN	Serial Data Input. Serial data to be loaded to the control register is provided at this input. The first six bits of serial data are loaded to the control register on the first six falling edges of SCLK after $\overline{TFS}$ goes low. Serial data on subsequent SCLK edges is ignored while $\overline{TFS}$ remains low.
$\overline{RFS}$	Receive Frame Synchronization Pulse. In the external clocking mode, this pin is an active low logic input with $\overline{RFS}$ provided externally as a strobe or framing pulse to access serial data from the output register. In the self-clocking mode, it is an active low output which is internally generated and provides a strobe or framing pulse for serial data from the output register. For applications which require that data be transmitted and received at the same time, $\overline{RFS}$ and $\overline{TFS}$ should be connected together.
DATA OUT	Serial Data Output. Sixteen bits of serial data are provided with one leading zero, preceeding the three address bits of the Control register and the 12-bits of conversion data. Serial data is valid on the falling edge of SCLK for sixteen edges after $\overline{RFS}$ goes low. Output coding from the ADC is 2s complement.
$\overline{CONVST}$	Convert Start. Edge-triggered logic input. A low to high transition on this input puts the track/hold into hold and initiates conversion provided that the internal one-shot has timed out (see Control Register section). If the internal pulse is active when the $\overline{CONVST}$ goes high, the track/hold will not go into hold until the pulse times out. If the internal pulse has timed out when $\overline{CONVST}$ goes high, the rising edge of $\overline{CONVST}$ drives the track/hold into hold and initiates conversion.
CLK IN	Clock Input. An external TTL-compatible clock is applied to this input pin to provide the clock source for the conversion sequence. In the self-clocking serial mode, the SCLK output is derived from this CLK IN pin.
C_{EXT}	External Capacitor. An external capacitor is connected to this pin to determine the length of the internal one-shot pulse (see $\overline{CONVST}$ input and Control Register section). Larger capacitances on this pin extend the pulse to allow for settling-time delays through an external antialiasing filter or signal conditioning circuitry.
NC	No Connect. Do not connect anything to this pin.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

A2	A1	A0	CONV	SC/EC	STBY

A2 Address Input. This input is the most significant address input for multiplexer channel selection.

A1 Address Input. This is the 2nd most significant address input for multiplexer channel selection.

A0 Address Input. Least significant address input for multiplexer channel selection. When the address is written to the control register, an internal one-shot is initiated, the pulse width of which is determined by the value of capacitance on the C_{EXT} pin. When this pulse is active, it ensures the conversion process cannot be activated. This allows an external antialiasing filter (the output of which appears at SHA IN) to settle before the track/hold goes into hold and conversion is initiated. When this pulse times out, the track/hold goes into hold and conversion is initiated.

CONV Conversion Start. Writing a 1 to this bit initiates a conversion in a similar manner to the $\overline{\text{CONVST}}$ input. Continuous conversion starts do not take place when there is a 1 in this location. The internal one-shot and the conversion process are initiated on the next clock edge after a 1 is written to this bit. With a 1 in this bit, the hardware conversion start, i.e., the $\overline{\text{CONVST}}$ input, is disabled. Writing a 0 to this bit enables the hardware $\overline{\text{CONVST}}$ input.

SC/EC Master/Slave Selection. Writing a 0 to this bit puts the AD7890 into its self-clocking (master) mode where the SCLK and $\overline{\text{RFS}}$ pins are outputs and the AD7890 effectively acts as a master in a serial system. This self-clocking mode is useful for connection to shift registers and the serial ports of DSP processors. Writing a 1 to this bit puts the AD7890 serial interface into its external clocking (slave) mode where the SCLK and $\overline{\text{RFS}}$ pins are both inputs and the AD7890 effectively acts as a slave to a microprocessor in a serial system. This external clocking mode is useful for connection to the serial port of microcontrollers such as the 8XC51 and the 68HCXX and for connection to the serial ports of DSP processors. The AD7890 powers up in its external clocking mode.

STBY Standby Mode Input. Writing a 1 to this bit places the device in its standby or power-down mode. Writing a 0 to this bit places the device in its normal operating mode.

PRELIMINARY TECHNICAL DATA

CIRCUIT DESCRIPTION

The AD7890 is an eight-channel, 12-bit serial data acquisition system. It provides the user with signal scaling, multiplexer, track/hold, A/D converter and versatile serial logic functions on a single chip. The signal scaling allows the part to handle ±10 V input signals while operating from a single +5 V supply. The part requires an external +2.5 V external reference.

Unlike other single chip solutions, the AD7890 provides the user with separate access to the multiplexer and the A/D converter. This means that the flexibility of separate multiplexer and ADC solutions is not sacrificed with the one-chip solution. With access to the multiplexer output, the user can implement external signal conditioning between the multiplexer and the track/hold. It means that one antialiasing filter can be used to on the output of the multiplexer to provide the antialiasing function for all eight channels. The extra settling time introduced into the circuit by the external circuitry can be allowed for by the AD7890 by connecting a single capacitor to the C_{EXT} pin. If no external signal conditioning is required, the multiplexer output (MUX OUT) can simply be connected directly to the track/hold input (SHA IN).

A serial write to the control register selects the input channel to be converted. When the three address bits are written to the control register, an internal pulse is initiated. This disables the track/hold from going into hold and also disables conversion from being initiated. The duration of the internal pulse allows for the settling time of the on-chip multiplexer. By connecting different values of capacitor for the C_{EXT} pin, this internal pulse can be stretched to cater for the settling time of external components between the MUX OUT and SHA IN pins.

Once the pulse has been timed out, conversion can be initiated on the A/D converter. The conversion can be initiated by pulsing the $\overline{\text{CONVST}}$ input or by writing to the CONV bit of the Control Register. If the conversion start command is coincident with the multiplexer write or occurs while the internal pulse is active, the track/hold will not go into hold and conversion will not be initiated until the internal pulse has timed out.

The AD7890 provides separate channel select and conversion start control. This allows the user to optimize the throughput rate of the system. Once the track/hold has gone into hold mode the input channel can be updated and the input voltage can settle to the new value while the present conversion is in progress.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

DIGITAL INTERFACE

The AD7890's serial communications port provides a flexible arrangement to allow easy interfacing to industry standard microprocessors, microcontrollers and digital signal processors. A serial read to the AD7890 accesses data from the output register via the DATA OUT line. A serial write to the AD7890 writes data to the Control Register via the DATA IN line.

Two different modes of operation are available, optimized for different types of interface where the AD7890 can either act as master in the system (it provides the serial clock and data framing signal) or act as slave (an external serial clock and framing signal can be provided to the AD7890). These two modes, labelled self-clocking mode and external clocking mode, are discussed in detail in the following sections. Note, the AD7890 powers up in its external clocking mode. A Logic 0 must be written to the SC/EC bit of the control register to place the part in its self-clocking mode.

Self-Clocking Mode

The AD7890 is configured for its self-clocking mode by writing a 0 to the SC/EC bit of the control register. In this mode, the AD7890 provides the serial clock signal and the serial data framing signal used for the transfer of data from the AD7890. This self-clocking mode can be used with processors which allow an external device to clock their serial port including most digital signal processors.

Read Operation

Figure 1 shows a timing diagram for reading from the AD7890 in the self-clocking mode. At the end of conversion, $\overline{RFS}$ goes low and the serial clock (SCLK) and serial data (DATA OUT) outputs become active. Sixteen bits of data are transmitted with one leading zero, followed by the three address bits of the Control Register, followed by the 12 bit conversion result starting with the MSB. Serial data is clocked out of the device on the rising edge of SCLK and is valid on the falling edge of SCLK. The $\overline{RFS}$ output remains low for the duration of the sixteen clock cycles. When $\overline{RFS}$ returns high, the serial clock and serial data outputs are disabled.

Write Operation

Figure 2 shows a write operation to the Control Register of the AD7890. The $\overline{TFS}$ input goes low to indicate to the part that a serial write is about to occur. $\overline{TFS}$ going low initiates the SCLK output, and this is used to clock data out of the processors serial port and into the Control Register of the AD7890. The AD7890 Control Register requires only six bits of data. These are loaded on the first six clock cycles of the serial clock with data on all subsequent clock cycles being ignored. Serial data to be written to the AD7890 must be valid on the falling edge of SCLK.

PRELIMINARY TECHNICAL DATA

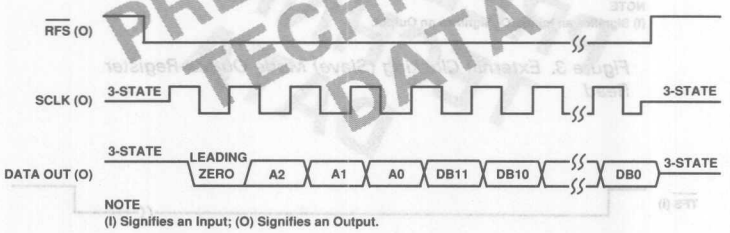


Figure 1. Self-Clock (Master) Mode Output Register Read

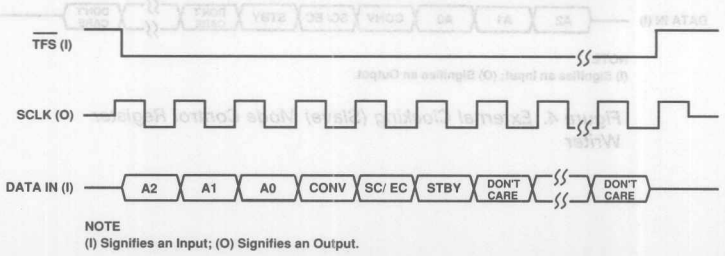


Figure 2. Self-Clocking (Master) Mode Control Register Write

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

External Clocking Mode

The AD7890 is configured for its external clocking mode by writing a 1 to the SC/EC bit of the Control Register. In this mode, SCLK and $\overline{RFS}$ of the AD7890 are configured as inputs. This external-clocking mode is designed for direct interface to systems which provide a serial clock output which is synchronized to the serial data output including microcontrollers such as the 80C51, 87C51, 68HC11 and 68HC05 and most digital signal processors.

Read Operation

Figure 3 shows the timing diagram for reading from the AD7890 in the external clocking mode. $\overline{RFS}$ goes low to access data from the AD7890. The serial clock input does not have to be continuous. The serial data can be accessed in a number of bytes. However, $\overline{RFS}$ must remain low for the duration of the data transfer operation. Once again, sixteen bits of data are transmitted with one leading zero, followed by the three address bits in the Control Register, followed by the 12-bit conversion result starting with the MSB. Serial data is clocked out of the device on the rising edge of SCLK and is valid on the falling edge of SCLK. If a serial read from the output register is in progress when conversion is complete, the updating of the output register is deferred until the serial data read is complete.

Write Operation

Figure 4 shows a write operation to the Control Register of the AD7890. As with the self-clocking mode, the $\overline{TFS}$ input goes low to indicate to the part that a serial write is about to occur. The AD7890 control register requires only six bits of data. These are loaded on the first six clock cycles of the serial clock with data on all subsequent clock cycles being ignored. Serial data to be written to the AD7890 must be valid on the falling edge of SCLK.

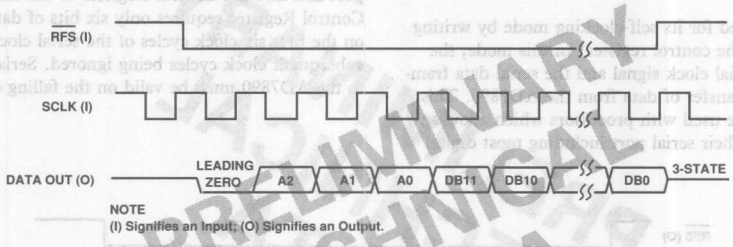


Figure 3. External Clocking (Slave) Mode Output Register Read

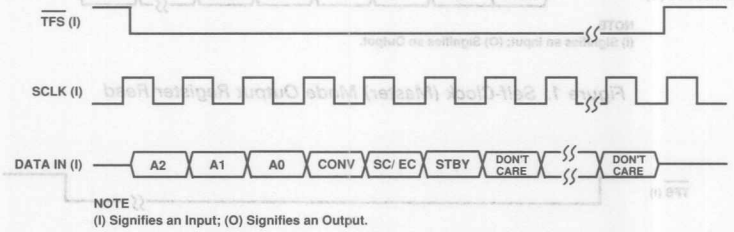


Figure 4. External Clocking (Slave) Mode Control Register Writer

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

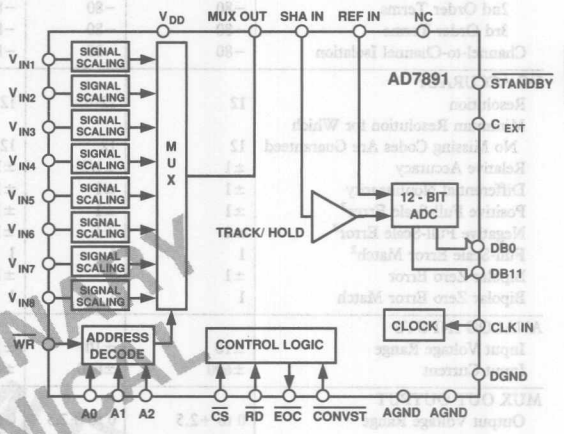
LC²MOS 8-Channel, 12-Bit Parallel Data Acquisition System

AD7891

FEATURES

- Fast 12-Bit ADC with 10 μs Conversion Time
- Eight Single-Ended Analog Input Channels
- ±10 V Input Range
- Allows Separate Access to Multiplexer and ADC
- On-Chip Track/Hold Amplifier
- High Speed Parallel Interface
- Single Supply Operation
- Low Power, 50 mW max in Normal Operation
- Power-Down Mode

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7891 is an 8-channel 12-bit data acquisition system with a parallel interface structure. The part contains an input multiplexer, an on-chip track/hold amplifier, a high speed 12-bit ADC and a high speed parallel interface. The part operates from a single +5 V supply and accepts an analog input range of ±10 V.

The multiplexer on the part is independently accessible. This allows the user to insert an antialiasing filter, if required, between the multiplexer and the ADC. This means that one antialiasing filter can be used for all eight channels. Connection of an external capacitor allows the user to adjust the time given to the multiplexer settling to include any external delays in this antialiasing filter.

The AD7891 has standard control inputs and fast data access times which ensure easy interfacing to modern microprocessors and digital signal processors.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the part is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

Power dissipation in normal mode is low at 30 mW typ, while in the standby mode this is reduced to 1 mW typ. The AD7891 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 44-pin plastic quad flat-pack (PQFP) and a 44-lead ceramic quad flat pack (CERQUAD).

PRODUCT HIGHLIGHTS

1. Complete 12-Bit Data Acquisition System on a Chip
   The AD7891 is a complete monolithic ADC combining an 8-channel multiplexer, 12-bit ADC and a track/hold amplifier on a single chip.
2. Separate Access to Multiplexer and ADC
   The AD7891 provides access to the output of the multiplexer allowing the user to insert an antialiasing filter between the multiplexer and the ADC. This allows one antialiasing filter for eight channels—a considerable saving over the eight antialiasing filters required if the multiplexer were internally connected to the ADC.
3. Fast Microprocessor Interface
   The part offers a high speed, parallel interface for easy connection to microprocessors, 16-bit microcontrollers and digital signal processors.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	A Version[1]	B Version	S Version	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE					Any Channel
Signal-to-Noise Ratio @ +25°C	70	72	70	dB min	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
T_{MIN} to T_{MAX}	70	70	70	dB min	
Total Harmonic Distortion	−80	−80	−80	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
Peak Harmonic or Spurious Noise	−81	−81	−81	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
Intermodulation Distortion					fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 83 kHz
2nd Order Terms	−80	−80	−80	dB typ	
3rd Order Terms	−80	−80	−80	dB typ	
Channel-to-Channel Isolation	−80	−80	−80	dB max	f_{IN} = 1 kHz Sine Wave
DC ACCURACY					Any Channel
Resolution	12	12	12	Bits	
Minimum Resolution for Which No Missing Codes Are Guaranteed	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	LSB max	
Positive Full-Scale Error[2]	±1	±1	±1	LSB max	
Negative Full-Scale Error[2]	±1	±1	±1	LSB max	
Full-Scale Error Match[2]	1	1	1	LSB max	
Bipolar Zero Error	±1	±1	±1	LSB max	
Bipolar Zero Error Match	1	1	1	LSB max	
ANALOG INPUTS					
Input Voltage Range	±10	±10	±10	Volts	
Input Current	±600	±600	±600	µA max	
MUX OUT OUTPUT					
Output Voltage Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Output Resistance	2.9/4.2	2.9/4.2	2.9/4.2	kΩ min/ kΩ max	
SHA IN INPUT					
Input Voltage Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Input Current	50	50	50	nA max	
REFERENCE INPUT					
Input Voltage Range	2.375/2.625	2.375/2.625	2.375/2.625	V min/V max	2.5 V ± 5%
Input Current	4	4	4	mA max	Varies with ADC Code
Input Capacitance[3]	10	10	10	pF max	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[3]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 40 µA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0					
Output Coding	2s Complement				
Floating-State Leakage Current	±10	±10	±10	µA max	
Floating-State Capacitance[3]	15	15	15	pF max	
CONVERSION RATE					
Conversion Time	10	10	10	µs max	$f_{CLK\ IN}$ = 2.5 MHz, MUX OUT Connected to SHA IN
Track/Hold Acquisition Time	2	2	2	µs max	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
I_{DD} (Normal Mode)	10	10	10	mA max	
I_{DD} (Standby Mode)	500	500	500	µA max	Logic Inputs = 0 V or V_{DD}
Power Dissipation (Normal Mode)	50	50	50	mW max	Typically 30 mW
Power Dissipation (Standby Mode)	2.5	2.5	2.5	mW max	Typically 1 mW

NOTES

[1]Temperature ranges are as follows: A, B Versions: −40°C to +85°C; S Version: −55°C to +125°C.

[2]Measured with respect to 4 × REF IN voltage and is calculated after the bipolar zero error has been adjusted out.

[3]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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PIN FUNCTION DESCRIPTION

Pin Mnemonic	Description
V_{IN1}–V_{IN8}	Analog Input Channels. These input channels provide eight single-ended inputs. The analog input range for each channel is ±10 V. The channel to be converted is selected by the A2, A1 and A0 inputs. The multiplexer has guaranteed break-before-make operation.
MUX OUT	Multiplexer Output. The output of the multiplexer appears at this pin. The output voltage range from this output is 0 to +2.5 V for a ±10 V analog input to the selected channel. The output impedance of this output is nominally 3.5 kΩ. If no external antialiasing filter is required, MUX OUT should be connected to SHA IN.
SHA IN	Track/Hold Input. The input to the on-chip track/hold is applied to this pin. It is a high impedance input and the input voltage range is 0 V to +2.5 V.
REF IN	Voltage Reference Input. The reference voltage for the part is applied to this pin. The input impedance of this reference input varies with the analog input voltage and REF IN should, therefore, be driven from a low impedance source. The nominal reference voltage for correct operation of the AD7891 is +2.5 V.
V_{DD}	Positive Supply Voltage, +5 V ±5%.
AGND	Analog Ground. Ground reference for track/hold, comparator and DAC.
DGND	Digital Ground. Ground reference for digital circuitry.
A0	Address Input. Least significant address input for multiplexer channel selection.
A1	Address Input. This is the 2nd most significant address input for multiplexer channel selection.
A2	Address Input. This input is the most significant address input for multiplexer channel selection.
$\overline{WR}$	Write Input. Edge-triggered, active low, logic input which latches the multiplexer address. The rising edge of this input also initiates an internal one-shot, the pulse width of which is determined by the value of capacitance on the C_{EXT} pin. When this pulse is active, it ensures the conversion process cannot be activated. This allows an external antialiasing filter (the output of which is applied to SHA IN) to settle before the track/hold goes into hold and conversion is initiated. If the $\overline{CONVST}$ input goes high , either coincident with the $\overline{WR}$ input or during the internal pulse active time, the track/hold will not go from track to hold and conversion will not be initiated until the internal pulse times out. When this pulse times out, the track/hold then goes into hold and conversion is initiated. If the pulse has timed out prior to $\overline{CONVST}$ going high, the rising edge of $\overline{CONVST}$ will put the track/hold into hold and initiate conversion.
$\overline{CONVST}$	Convert Start. Edge-triggered logic input. A low to high transition on this input puts the track/hold into hold and initiates conversion, provided that the internal one-shot has timed out (see $\overline{WR}$ input). If the internal pulse is active when the $\overline{CONVST}$ goes high, the track/hold will not go into hold until the internal pulse times out. If the internal pulse has timed out when $\overline{CONVST}$ goes high, the rising edge of $\overline{CONVST}$ drives the track/hold into hold and initiates conversion.
$\overline{CS}$	Chip Select. Active low logic input which is used in conjunction with $\overline{RD}$ to enable the data outputs.
$\overline{RD}$	Read. Active low logic input which is used in conjunction with $\overline{CS}$ low to enable the data outputs.
EOC	End-of-Conversion. Active low logic output indicating converter status. The end of conversion is signified by a low-going pulse on this line. The duration of this EOC pulse is nominally 500 ns.
CLK IN	Clock Input. An external TTL-compatible clock may be applied to this input pin to provide the clock source for the conversion sequence.
C_{EXT}	External Capacitor. An external capacitor is connected to this pin to determine the length of the internal one-shot pulse (see $\overline{WR}$ input). Larger capacitances on this pin extend the pulse to allow for settling-time delays through the external antialiasing filter.
$\overline{STANDBY}$	Standby Mode Input. TTL-compatible input which is used to put the device into the power save or standby mode. The STANDBY input is high for normal operation and low for standby operation.
DB0–DB11	Data Bit 0 (LSB) to Data Bit 11 (MSB). Three-state TTL-compatible outputs. Output data coding from the AD7891 is 2s complement.
NC	No Connect. Do not connect anything to this pin.

PRELIMINARY DATA

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CIRCUIT DESCRIPTION

The AD7891 is an 8-channel, 12-bit parallel data acquisition system. It provides the user with signal scaling, multiplexer, track/hold, A/D converter and high speed parallel interface logic functions on a single chip. The signal scaling allows the part to handle ±10 V input signals while operating from a single +5 V supply. The part requires an external +2.5 V external reference.

Unlike other single chip solutions, the AD7891 provides the user with separate access to the multiplexer and the A/D converter. This means that the flexibility of separate multiplexer and ADC solutions is not sacrificed with the one chip solution. With access to the multiplexer output, the user can implement external signal conditioning between the multiplexer and the track/hold. It means that one antialiasing filter can be used on the output of the multiplexer to provide the antialiasing function for all eight channels. The extra settling time introduced into the circuit by the external circuitry can be allowed for by the AD7891 by connecting a single capacitor to the C_{EXT} pin. If no external signal conditioning is required, the multiplexer output (MUX OUT) can simply be connected directly to the track/hold input (SHA IN).

A write to the multiplexer address inputs (A0, A1, A2) selects the input channel to be converted. When the three address bits are written to the part, an internal pulse is initiated. This disables the track/hold from going into hold and also disables conversion from being initiated. The duration of the internal pulse allows for the settling time of the on-chip multiplexer. By connecting different values of capacitor for the C_{EXT} pin, this internal pulse can be stretched to cater for the settling-time of external components between the MUX OUT and SHA IN pins.

Once the pulse has been timed out, conversion can be initiated on the A/D converter. The conversion is initiated by pulsing the $\overline{CONVST}$ input. If the conversion start command is coincident with the multiplexer write or occurs while the internal pulse is active, the track/hold will not go into hold and conversion will not be initiated until the internal pulse has timed out.

The AD7891 provides separate channel select and conversion start control. This allows the user to optimize the throughput rate of the system. Once the track/hold has gone into hold mode, the input channel can be updated and the input voltage can settle to the new value while the present conversion is in progress.

INTERFACE INFORMATION

Figure 1 shows a timing diagram illustrating the operational sequence of the AD7891. The multiplexer address is written to the AD7891 on the rising edge of the $\overline{WR}$ input. The on-chip track/hold goes into hold mode on the rising edge of $\overline{CONVST}$, and conversion is also initiated at this point. When conversion is complete, the end of conversion line ($\overline{EOC}$) pulses low to indicate that new data is available in the AD7891's output register. This $\overline{EOC}$ line can be used to drive an edge-triggered interrupt of a microprocessor. $\overline{CS}$ and $\overline{RD}$ going low accesses the 12-bit conversion result. In stand-alone systems, the $\overline{EOC}$ pulse can be applied to the $\overline{CS}$ and $\overline{RD}$ inputs to latch data out of the AD7891 and into an external latch or gate array.

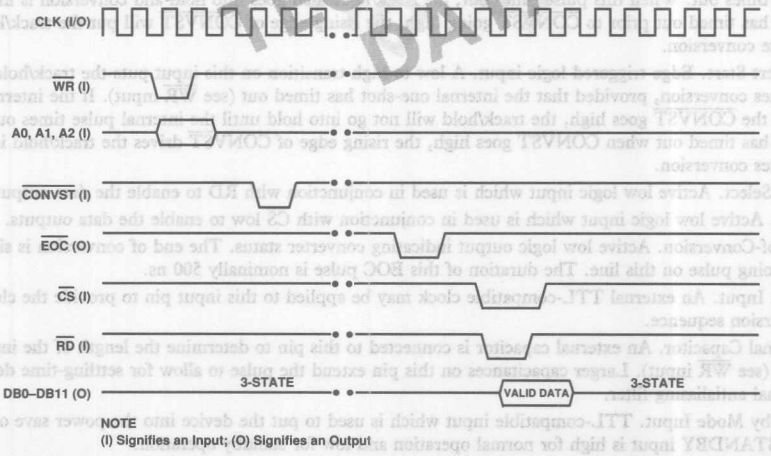


Figure 1. AD7891 Timing Diagram

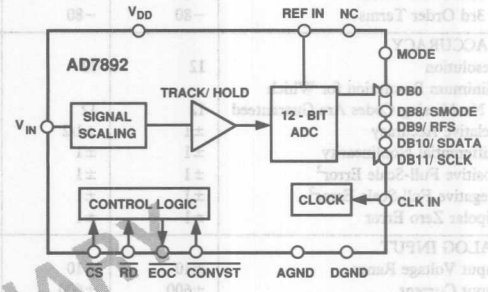
This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

LC²MOS
Single Supply, 12-Bit, 5.5 µs ADC
AD7892

FEATURES

Fast 12-Bit ADC with 5.5 µs Conversion Time
Single Supply Operation
On-Chip Track/Hold Amplifier
±10 V Input Range
High Speed Serial and Parallel Interface
Low Power, 50 mW

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD7892 is a high speed, low power, 12-bit A/D converter which operates from a single +5 V supply. The part contains a 5.5 µs successive approximation ADC, an on-chip track/hold amplifier and on-chip versatile interface structures which allow both serial and parallel connection to a microprocessor. The part accepts an analog input range of ±10 V.

The AD7892 offers a choice of two data output formats: a single, parallel, 12-bit word or serial data. Fast bus access times and standard control inputs ensure easy parallel interface to microprocessors and digital signal processors. A high speed flexible serial interface allows direct connection to shift registers and to the serial ports of microcontrollers and digital signal processors.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the part is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The part operates from a single +5 V supply and accepts ±10 V input signals. Power dissipation for the part is low at 30 mW typical.

The AD7892 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. It is available in a 24-pin, 0.3" wide, plastic or hermetic dual-in-line package or in a 24-pin small outline package (SOIC).

PRODUCT HIGHLIGHTS

1. Fast Conversion Time
   The AD7892 features a conversion time of 5.5 µs and a track/hold acquisition time of 1.5 µs. This allows a throughput rate in excess of 140 kHz and an input bandwidth in excess of 70 kHz.
2. Single Supply Operation
   The AD7892 operates from a single +5 V supply and consumes only 30 mW making it ideal for low power and portable applications.
3. Fast, Versatile Microprocessor Interface
   The part offers a high speed, flexible interface arrangement with parallel and serial interfaces for easy connection to microprocessors, microcontrollers and digital signal processors.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Signal-to-Noise Ratio @ +25°C	70	72	70	dB min	f_{IN} =10 kHz Sine Wave, f_{SAMPLE} = 140 kHz
T_{MIN} to T_{MAX}	70	70	70	dB min	
Total Harmonic Distortion	−80	−80	−80	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 140 kHz
Peak Harmonic or Spurious Noise	−81	−81	−81	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 140 kHz
Intermodulation Distortion					fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 140 kHz
2nd Order Terms	−80	−80	−80	dB max	
3rd Order Terms	−80	−80	−80	dB max	
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for Which					
No Missing Codes Are Guaranteed	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	LSB max	
Positive Full-Scale Error[2]	±1	±1	±1	LSB max	
Negative Full-Scale Error[2]	±1	±1	±1	LSB max	
Bipolar Zero Error	±1	±1	±1	LSB max	
ANALOG INPUT					
Input Voltage Range	±10	±10	±10	Volts	
Input Current	±600	±600	±600	μA max	
REFERENCE INPUT					
Input Voltage Range	2.375/2.625	2.375/2.625	2.375/2.625	V min/V max	2.5 V ± 5%
Input Current	700	700	700	μA max	Varies with Analog Input Voltage
Input Capacitance[3]	10	10	10	pF max	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[3]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 40 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0					
Floating-State Leakage Current	±10	±10	±10	μA max	
Floating-State Capacitance[3]	15	15	15	pF max	
CONVERSION RATE					
Conversion Time	5.5	5.5	5.5	μs max	$f_{CLK\ IN}$ = 2.5 MHz
Track/Hold Acquisition Time	1.5	1.5	1.5	μs max	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
I_{DD}	10	10	10	mA max	
Power Dissipation	50	50	50	mW max	Typically 30 mW

NOTES

[1]Temperature ranges are as follows: A, B Versions: −40°C to +85°C; S Version: −55°C to +125°C.

[2]Measured with respect to 4 × REFIN voltage and is calculated after the bipolar zero error has been adjusted out.

[3]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Pin Mnemonic	Description
V_{IN}	Analog Input. The analog input range is ±10 V.
REFIN	Voltage Reference Input. The reference voltage for the part is applied to this pin. The input impedance of this reference input varies with the analog input voltage and REFIN should, therefore, be driven from a low impedance source. The nominal reference voltage for correct operation of the AD7892 is +2.5 V.
V_{DD}	Positive Supply Voltage, +5 V ±5%.
AGND	Analog Ground. Ground reference for track/hold, comparator and DAC.
DGND	Digital Ground. Ground reference for digital circuitry.
$\overline{CONVST}$	Convert Start. Logic Input. A low to high transition on this input puts the track/hold into its hold mode and starts conversion.
$\overline{CS}$	Chip Select. Active low logic input which is used in conjunction with $\overline{RD}$ to enable the data outputs.
$\overline{RD}$	Read. Active low logic input which is used in conjunction with $\overline{CS}$ low to enable the data outputs.
EOC	End-of-Conversion. Active low logic output indicating converter status. The end of conversion is signified by a low going pulse on this line. The duration of this EOC pulse is nominally 500 ns.
CLK	Clock Input. The external TTL-compatible clock is applied to this input pin to provide the clock source for the conversion sequence.
MODE	Mode. Control input which determines the interface mode for the AD7892. With this pin at a logic low, the device is in its serial interface mode; with this pin at a logic high, the device is in its parallel interface mode.
DB0-DB7	Data Bit 0 (LSB) to Data Bit 7. Three-state TTL-compatible outputs. Output coding is 2s complement. These outputs should be left unconnected when the device is in its serial mode.
DB8/SMODE	Data Bit 8/Serial Mode. When the device is in its parallel mode, this pin is Data Bit 8, a three-state TTL-compatible output. When the device is in its serial mode, this becomes a control input which determines whether the part operates in its External Clocking (slave) or Self-Clocking (master) serial mode. With SMODE at a logic high, the part is in its Self-Clocking serial mode with $\overline{RFS}$ and SCLK as outputs. This Self-Clocking mode is useful for connection to shift registers or to the serial ports of DSP processors. With SMODE at a logic low, the part is in its External Clocking serial mode with SCLK and $\overline{RFS}$ as inputs. This External Clocking mode is useful for connection to the serial port of microcontrollers such as the 8XC51 and the 68HCXX and for connection to the serial port of DSP processors.
DB9/$\overline{RFS}$	Data Bit 9/Receive Frame Synchronization. When the device is in its parallel mode, this pin is Data Bit 9, a three-state TTL-compatible output. When the device is in its serial mode, this becomes the receive frame synchronization pulse which can be either an input or an output depending on the status of SMODE. With SMODE at a logic high, the part is in its Self-Clocking mode and $\overline{RFS}$ is internally generated by the device and is provided as an output to frame the valid serial data. With SMODE at a logic low, the part is in its External Clocking serial mode with $\overline{RFS}$ provided externally to obtain serial data from the AD7892.
DB10/SDATA	Data Bit 10/Serial Data. When the device is in its parallel mode, this pin is Data Bit 10, a three-state TTL-compatible output. When the device is in its serial mode, this becomes the serial data output line. Sixteen bits of serial data are provided with four leading zeros preceding the 12-bits of valid data. Serial data is valid on the falling edge of SCLK for sixteen edges after $\overline{RFS}$ goes low. Output coding is 2s complement.
DB11/SCLK	Data Bit 11/Serial Clock. When the device is in its parallel mode, this pin is Data Bit 11(MSB), a three-state TTL-compatible output. When the device is in its serial mode, this becomes the serial clock pin which is an input or an output depending on the status of SMODE. With SMODE at a logic high, SCLK is generated internally from the CLK input and is provided as an output. With SMODE at a logic low, SCLK is an input and an external serial clock must be provided at this pin to obtain serial data from the AD7892. Regardless of the status of SMODE, serial data is valid on the falling edge of SCLK for sixteen edges after $\overline{RFS}$ goes low.
NC	No Connect. Do not connect anything to this pin.

PRELIMINARY TECHNICAL DATA

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CIRCUIT DESCRIPTION

The AD7892 is a fast, 12-bit single supply A/D converter. It provides the user with signal scaling, track/hold, A/D converter and versatile interface logic functions on a single chip. The signal scaling allows the part to handle ±10 V input signals while operating from a single +5 V supply. The part requires an external +2.5 V external reference.

Conversion is initiated on the AD7892 by pulsing the $\overline{\text{CONVST}}$ input. On the rising edge of $\overline{\text{CONVST}}$, the on-chip track/hold goes from track to hold mode and the conversion sequence is started. Conversion time for the AD7892 is 5.5 μs and the track/hold acquisition time is 1.5 μs. This allows the part to operate at throughput rates up to 140 kHz, while the input track/hold can handle input bandwidths in excess of the Nyquist criterion of 70 kHz.

INTERFACING

The part provides three interface options, one parallel and two serial. The parallel interface mode is selected by tying the MODE input to a logic high. The serial modes are selected by tying this pin to a logic low. With the MODE pin low, the DB8/SMODE, DB9/$\overline{\text{RFS}}$, DB10/SDATA and DB11/SCLK pins all assume their serial mode functions. SMODE becomes a logic input which selects whether the AD7892 operates in its Self-Clocking serial mode or in its External-Clocking serial mode. The three interface modes are discussed in the following sections.

Parallel Interface Mode

Figure 1 shows a timing diagram illustrating the operational sequence of the AD7892. The on-chip track/hold goes into hold mode on the rising edge of $\overline{\text{CONVST}}$ and conversion is also initiated at this point. When conversion is complete, the end of conversion line (EOC) pulses low to indicate that new data is available in the AD7892's output register. This EOC line can be used to drive an edge-triggered interrupt of a microprocessor. $\overline{\text{CS}}$ and $\overline{\text{RD}}$ going low accesses the 12-bit conversion result. In stand-alone systems, the EOC pulse can be applied to the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs to latch data out of the AD7892 and into an external latch or gate array.

PRELIMINARY TECHNICAL DATA

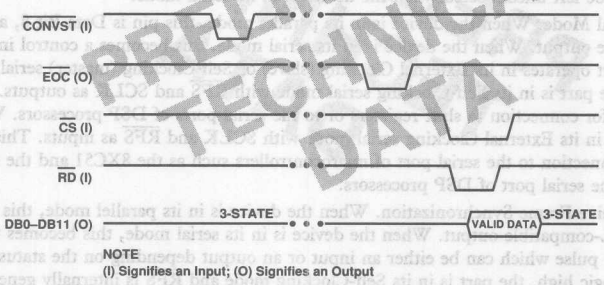


Figure 1. Parallel Mode Timing Diagram

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SERIAL INTERFACE

The AD7892 is configured for serial mode interfacing by tying the MODE input low. The AD7892's serial communications port provides a flexible arrangement to allow easy interfacing to industry-standard microprocessors, microcontrollers and digital signal processors. It provides for a three-wire, serial link between the AD7892 and the microprocessor. Two different modes of operation are available, optimized for different types of interface where the AD7892 can act either as master in the system (it provides the serial clock and data framing signal) or acts as slave (an external serial clock and framing signal can be provided to the AD7892). These two modes, labelled Self-Clocking mode and External Clocking mode, are discussed in detail in the following sections.

Self-Clocking Mode

The AD7892 is configured for its self-clocking mode by tying the SMODE input high. In this mode, the AD7892 provides the serial clock signal and the serial data framing signal used for the transfer of data from the AD7892. This self-clocking mode can be used with processors which allow an external device to clock their serial port including most digital signal processors.

Figure 2 shows a timing diagram for reading from the AD7892 in the self-clocking mode. At the end of conversion, $\overline{RFS}$ goes low and the serial clock (SCLK) and serial data (SDATA) outputs become active. Sixteen bits of data are transmitted with four leading zeros followed by the 12 bit conversion result starting with the MSB. Serial data is clocked out of the device on the rising edge of SCLK and is valid on the falling edge of SCLK. The $\overline{RFS}$ output remains low for the duration of the 16 clock cycles. When $\overline{RFS}$ returns high, the serial clock and serial data outputs are disabled.

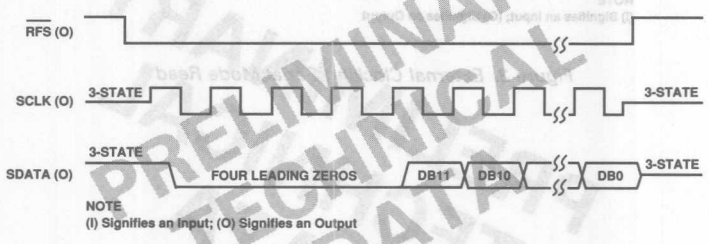


Figure 2. Self-Clocking Serial Mode Read

PRELIMINARY TECHNICAL DATA

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External-Clocking Mode

The AD7892 is configured for its external-clocking mode by tying the SMODE input to a logic low. In this mode, SCLK and $\overline{RFS}$ of the AD7892 are configured as inputs. This external-clocking mode is designed for direct interface to systems which provide a serial clock output which is synchronized to the serial data output including microcontrollers such as the 80C51, 87C51, 68HC11 and 68HC05 and most digital signal processors.

Figure 3 shows the timing diagram for reading from the AD7892 in the external-clocking mode. $\overline{RFS}$ goes low to access data from the AD7892. The serial clock input does not have to be continuous. The serial data can be accessed in a number of bytes. However, $\overline{RFS}$ must remain low for the duration of the data transfer operation. Once again, 16 bits of data are transmitted with 4 leading zeros followed by the 12 bit conversion result starting with the MSB. Serial data is clocked out of the device on the rising edge of SCLK and is valid on the falling edge of SCLK. If a serial read from the output register is in progress when conversion is complete, the updating of the output register is deferred until the serial data read is complete.

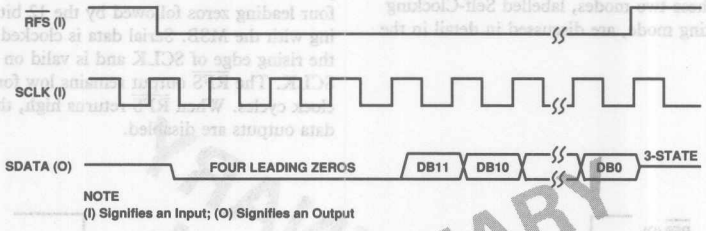


Figure 3. External Clocking Serial Mode Read

PRELIMINARY TECHNICAL DATA

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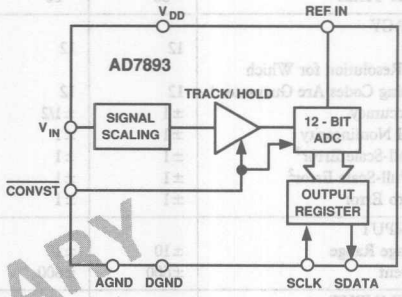
LC²MOS 12-Bit, Serial 5.5 µs, ADC in 8-Pin Package

AD7893

FEATURES

Fast 12-Bit ADC with 5.5 µs Conversion Time
8-Pin Mini-DIP and SOIC
Single Supply Operation
High Speed, Easy-to-Use, Serial Interface
On-Chip Track/Hold Amplifier
±10 V Input Range
Low Power, 50 mW max

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD7893 is a fast, 12-bit ADC which operates from a single +5 V supply and is housed in a small 8-pin mini-DIP and 8-pin SOIC. The part contains a 5.5 µs successive approximation A/D converter, an on-chip track/hold amplifier, an on-chip clock and a high speed serial interface.

Output data from the AD7893 is provided via a high speed, serial interface port. This two-wire serial interface has a serial clock input and a serial data output with the external serial clock accessing the serial data from the part.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7893 is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The part accepts an analog input range of ±10 V and operates from a single +5 V supply consuming only 30 mW.

The AD7893 is fabricated in Analog Devices' linear compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a small, 8-pin, 0.3″ wide, plastic or hermetic dual-in-line package (mini-DIP) and in an 8-pin, small-outline IC (SOIC).

PRODUCT HIGHLIGHTS

1. Fast, 12-Bit ADC in 8-Pin Package
   The AD7893 contains a 5.5 µs ADC, a track/hold amplifier, control logic and a high speed serial interface, all in an 8-pin DIP. This offers considerable space saving over alternative solutions.
2. Low Power, Single Supply Operation
   The AD7893 operates from a single +5 V supply and consumes only 30 mW. This low power, single supply operation makes it ideal for battery-powered or portable applications.
3. High Speed Serial Interface
   The part provides high speed serial data and serial clock lines allowing for an easy, two-wire serial interface arrangement.

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DYNAMIC PERFORMANCE					
Signal-to-Noise Ratio @ +25°C	70	72	70	dB min	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 140 kHz
T_{MIN} to T_{MAX}	70	70	70	dB min	
Total Harmonic Distortion	−80	−80	−80	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 140 kHz
Peak Harmonic or Spurious Noise	−81	−81	−81	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 140 kHz
Intermodulation Distortion					fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 140 kHz
2nd Order Terms	−80	−80	−80	dB max	
3rd Order Terms	−80	−80	−80	dB max	
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for Which					
No Missing Codes Are Guaranteed	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	LSB max	
Positive Full-Scale Error[2]	±1	±1	±1	LSB max	
Negative Full-Scale Error[2]	±1	±1	±1	LSB max	
Bipolar Zero Error	±1	±1	±1	LSB max	
ANALOG INPUT					
Input Voltage Range	±10	±10	±10	Volts	
Input Current	±600	±600	±600	μA max	
REFERENCE INPUT					
Input Voltage Range	2.375/2.625	2.375/2.625	2.375/2.625	V min/V max	2.5 V ± 5%
Input Current	700	700	700	μA max	Varies with Analog Input Voltage
Input Capacitance[3]	10	10	10	pF max	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[3]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 40 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
CONVERSION RATE					
Conversion Time	5.5	5.5	5.5	μs max	
Track/Hold Acquisition Time	1.5	1.5	1.5	μs max	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
I_{DD}	10	10	10	mA max	
Power Dissipation	50	50	50	mW max	Typically 30 mW

NOTES

[1]Temperature ranges are as follows: A, B Versions: −40°C to +85°C; S Version: −55°C to +125°C.

[2]Measured with respect to 4 × REFIN voltage and is calculated after the bipolar zero error has been adjusted out.

[3]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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PIN FUNCTION DESCRIPTION

Pin Mnemonic	Description
V_{IN}	Analog Input. The analog input range is ±10 V.
REF IN	Voltage Reference Input. The reference voltage for the part is applied to this pin. The input impedance of this reference input varies with the analog input voltage and REFIN should, therefore, be driven from a low impedance source. The nominal reference voltage for correct operation of the AD7893 is +2.5 V.
V_{DD}	Positive Supply Voltage, +5 V ±5%.
AGND	Analog Ground. Ground reference for track/hold, comparator and DAC.
DGND	Digital Ground. Ground reference for digital circuitry.
SCLK	Serial Clock Input. An external serial clock is applied to this input to obtain serial data from the AD7893. A new serial data bit is clocked out on the rising edge of this serial clock and data is valid on the falling edge. The serial clock input should be taken low at the end of the serial data transmission.
SDATA	Serial Data Output. Serial data from the AD7893 is provided at this output. The serial data is clocked out by the rising edge of SCLK and is valid on the falling edge of SCLK. Sixteen bits of serial data are provided with four leading zeros followed by the 12-bits of conversion data. The last bit of serial data clocked out in a read cycle (on the sixteenth rising edge of SCLK) will remain on the SDATA line until the next serial data word is accessed.
$\overline{\text{CONVST}}$	Convert Start. Edge-triggered logic input. A low to high transition on this input puts the track/hold into its hold mode and starts conversion.

CIRCUIT DESCRIPTION

The AD7893 is a fast, 12-bit single supply A/D converter. It provides the user with signal scaling, track/hold, A/D converter and serial interface logic functions on a single chip. The signal scaling allows the part to handle ±10 V input signals while operating from a single +5 V supply. The AD7893 consumes only 30 mW typical making it ideal for battery-powered applications.

The part requires an external +2.5 V external reference. This reference input should be driven from a low impedance source as the input current to the REFIN pin varies with the analog input voltage.

A major advantage of the AD7893 is that it provides all of the above functions in an 8-pin package, either 8-pin mini-DIP or SOIC. This offers the user considerable spacing saving advantages over alternative solutions.

Conversion is initiated on the AD7893 by pulsing the $\overline{\text{CONVST}}$ input. On the rising edge of $\overline{\text{CONVST}}$, the on-chip track/hold goes from track-to-hold mode and the conversion sequence starts. Conversion time for the AD7893 is 5.5 μs and the track/hold acquisition time is 1.5 μs. This allows the part to operate at throughput rates up to 140 kHz, while the input track/hold can handle input bandwidths in excess of the Nyquist criterion of 70 kHz.

PRELIMINARY TECHNICAL DATA

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Serial Interface

The serial interface to the AD7893 consists of just two wires, a serial clock input (SCLK) and the serial data output (SDATA). This allows for an easy-to-use interface to most microcontrollers, DSP processors and shift registers.

Figure 1 shows the timing diagram for a read operation to the AD7893. The serial clock input (SCLK) provides the clock source for the serial interface. Serial data is clocked out from the SDATA line on the rising edge of this clock and is valid on the falling edge of SCLK. Sixteen clock pulses must be provided to the part to access to full conversion result. The AD7893 provides four leading zeros followed by the 12-bit conversion result starting with the MSB (DB11). The last data bit to be clocked out on the final rising clock edge is the LSB (DB0). This bit will remain on the SDATA line until the next serial data read is performed to the AD7893. After this last bit has been clocked out, the SCLK input should return low and remain low until the next serial data read operation.

The serial clock input does not have to be continuous during the serial read operation. The 16 bits of data (4 leading zeros and 12-bit conversion result) can be read from the AD7893 in a number of bytes. However, the SCLK input must remain low between the two bytes.

If a serial read from the output register is in progress when conversion is complete, the updating of the output register is deferred until the serial read is completed.

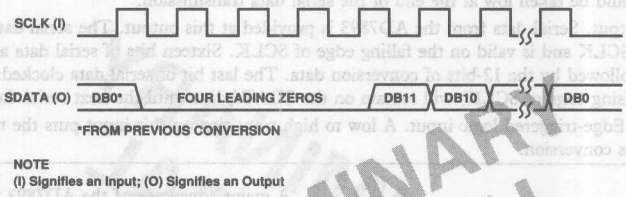


Figure 1. Data Read Operation

PRELIMINARY TECHNICAL DATA

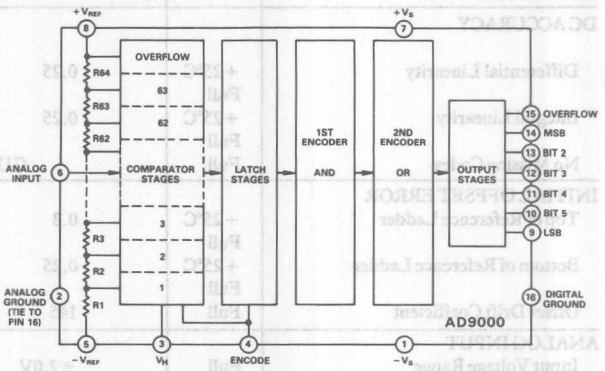
This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD9000

FEATURES
77MSPS Encode Rate
Bipolar Input Range
Low Error Rate
Overflow Bit
MIL-STD-883 Compliant Versions Available

APPLICATIONS
QAM Telecommunications
Electronic Warfare (ECM, ECCM, ESM)
Radar Guidance Digitizers

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9000 is a 6-bit, high speed, analog-to-digital converter with ECL compatible outputs and a bipolar input stage. The AD9000 is fabricated in a high-performance bipolar process which allows encode rates up to 77MSPS.

The AD9000 employs the standard flash converter architecture based on 64 individual comparators which simultaneously determine the precise analog signal level. The comparators are followed by two stages of decoding logic, allowing the AD9000 to operate with a very low error rate. The low 35pF input capacitance of the AD9000 greatly simplifies the analog driver stage. Also incorporated into the AD9000 design is an overflow output bit as well as a hysteresis control pin to modify comparator sensitivity.

The AD9000 is offered as both an commercial temperature range device 0 to +70°C, and as an extended temperature range device −55°C to +125°C. Both versions are available packaged in a 16-pin ceramic DIP. The extended temperature range device is also available in a 28-pin ceramic LCC package. The extended temperature range versions are offered as fully compliant MIL-STD-883 Class B devices.

ELECTRICAL CHARACTERISTICS (Supply Voltages = −5.2V and +5.0V; Differential Reference Voltage = 2.0V unless otherwise stated)

Parameter	Temp	Commercial 0 to +70°C AD9000JD Min	Typ	Max	Military −55°C to +125°C AD9000SD/SE Min	Typ	Max	Units
RESOLUTION		6			6			Bits
DC ACCURACY								
Differential Linearity	+25°C		0.25	0.5		0.25	0.5	LSB
	Full			1.0			1.0	LSB
Integral Linearity	+25°C		0.25	0.5		0.25	0.5	LSB
	Full			1.0			1.0	LSB
No Missing Codes	Full		GUARANTEED			GUARANTEED		
INITIAL OFFSET ERROR								
Top of Reference Ladder	+25°C		0.3	7/8		0.3	7/8	LSB
	Full			1.5			1.5	LSB
Bottom of Reference Ladder	+25°C		0.25	7/8		0.25	7/8	LSB
	Full			1.5			1.5	LSB
Offset Drift Coefficient	Full		145			145		µV/°C
ANALOG INPUT								
Input Voltage Range	Full		±2.0V			±2.0V		V
Input Bias Current (Sampling)[1]	Full			800			800	µA
Input Bias Current (Latched)[1]	Full			20			20	µA
Input Resistance	+25°C		3.0			3.0		kΩ
Input Capacitance	+25°C		35	50		35	50	pF
Full Power Bandwidth[2]	+25°C		20			20		MHz
REFERENCE INPUT[3,4]								
Reference Ladder Resistance	+25°C	80		200	80		200	Ω
Ladder Temperature Coefficient			0.275			0.275		Ω/°C
Reference Input Bandwidth	+25°C		20			20		MHz
DYNAMIC PERFORMANCE[5]								
Conversion Rate	+25°C	50	70		75	77		MHz
Conversion Time (+1 Clock)	+25°C			20			13.3	ns
Aperture Delay (t_D)	+25°C		2			2		ns
Aperture Uncertainty (Jitter)	+25°C		25			25		ps
Output Propagation Delay (t_{PD})[6]	+25°C	8		12	8		12	ns
Output Hold Time (t_{OH})[7]	+25°C	8		14	8		14	ns
Transient Response[8]	+25°C		13			13		ns
Overvoltage Recovery Time[9]	+25°C		11			11		ns
Output Rise Time[10]	+25°C			5.0			4.5	ns
Output Fall Time[10]	+25°C			5.0			4.5	ns
Output Time Skew	+25°C		0.4			0.4		ns
ENCODE INPUT								
Logic "1" Voltage	Full	−1.1			−1.1			V
Logic "0" Voltage	Full			−1.5			−1.5	V
Logic "1" Current	Full			100			100	µA
Logic "0" Current	Full			100			100	µA
Input Capacitance	+25°C		2.5	5.0		2.5	5.0	pF
ENCODE Pulse Width High (t_{PWH})	+25°C	6.6			6.6			ns
ENCODE Pulse Width Low (t_{PWL})	+25°C	6.6			6.6			ns

ELECTRICAL CHARACTERISTICS (Continued)

Parameter	Temp	Commercial 0 to +70°C AD9000JD Min	Typ	Max	Military −55°C to +125°C AD9000SD/SE Min	Typ	Max	Units
AC LINEARITY[11]								
Dynamic Linearity[12]	+25°C		0.5			0.5		LSB
In-Band Harmonics								
(DC to 1MHz)	+25°C		44			44		dBc
(1MHz to 5MHz)	+25°C		42			42		dBc
(5MHz to 8MHz)	+25°C		38			38		dBc
Signal to Noise Ratio[13]	+25°C	31	33		31	33		dB
Signal to Noise Ratio[14]	+25°C	40	42		40	42		dB
Two Tone Intermodulation Rejection[15]	+25°C		46			46		dBc
Noise Power Ratio (NPR)[16]	+25°C		30			30		dBc
DIGITAL OUTPUTS[5]								
Logic "1" Voltage	Full	−1.1			−1.1			V
Logic "0" Voltage	Full			−1.5			−1.5	V
POWER SUPPLY[17]								
Positive Supply Current (+5.0V)	+25°C		60	70		60	70	mA
	Full			75			75	mA
Negative Supply Current (−5.2V)	+25°C		68	80		68	80	mA
	Full			85			85	mA
Nominal Power Dissipation	+25°C		675			675		mW
Reference Ladder Dissipation	+25°C		20			20		mW

NOTES
[1]$A_{IN} = +V_{REF}$.
[2]Determined by 3dB reduction in reconstructed output at 75MSPS.
[3]Under normal operating conditions, the analog input voltages should not exceed nominal ±2V operating range, nor the supply voltages ($+V_S$ and $-V_S$), whichever is smaller.
[4]Under normal operating conditions the differential reference voltage may range from ±0.5V to ±2V; $+V_{REF} \geq -V_{REF}$.
[5]Output terminated with 100Ω resistors to −2.0V.
[6]Measured from the leading edge of ENCODE to data out on Bit 1 (MSB).
[7]Measured from the trailing edge of ENCODE to data out on Bit 1 (MSB).
[8]For full-scale step input, 6-bit accuracy is attained in specified time.
[9]Recovers to 6-bit accuracy in specified time, after 150% full-scale input overvoltage.
[10]Measured on Bit 1 (MSB) only.
[11]Measured at 50MSPS encode rate.
[12]Analog input frequency = 15MHz.
[13]RMS signal to RMS noise, with 540kHz analog input signal.
[14]Peak-to-peak signal to rms noise, with 540kHz analog input signal.
[15]$f_1 = 9.3$MHz; $f_2 = 7.6$MHz; Encode = 42MHz.
[16]DC to 8.2MHz noise bandwidth with 3.886MHz slot.
[17]Supply voltage should remain stable within ±5% for normal operation.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage	−0.3V to +6V
Negative Supply Voltage	−6.0V to +0.3V
Analog-to-Digital Ground Voltage Differential	0.5
Analog Input Voltages (A_{IN}, $+V_{REF}$, $-V_{REF}$)[2]	±3V
Differential Reference Voltage ($+V_{REF}$ to $-V_{REF}$)[3]	6V
ENCODE Input Voltage	$-V_S$ to 0V
HYSTERESIS Control Voltage	0V to +3.0V
Digital Output Current	20mA
Power Dissipation (+25°C Free Air)[4]	745mW
Operating Temperature Range	
AD9000JD	0 to +70°C
AD9000SD/SE	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+175°C
Lead Soldering Temperature (10sec)	+300°C

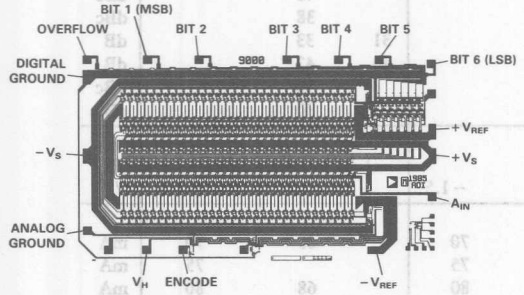
NOTES
[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Under normal operating conditions, the analog input voltages should not exceed nominal ±2V operating range, nor the supply voltages ($+V_S$ and $-V_S$), whichever is smaller.
[3]Under normal operating conditions the differential reference voltage may range from ±0.5V to ±2V; $+V_{REF} \geq -V_{REF}$.
[4]Typical thermal impedances . . .
16-Pin Ceramic $\theta_{ja} = 67°C/W$; $\theta_{jc} = 7°C/W$
28-Pin LCC $\theta_{ja} = 62°C/W$; $\theta_{jc} = 14°C/W$

ORDERING GUIDE

Model[1]	Temperature Range	Description	Package Option[2]
AD9000JD	0 to +70°C	16-Pin DIP, Industrial	D-16
AD9000SD	−55°C to +125°C	16-Pin DIP	D-16
AD9000SE	−55°C to +125°C	28-Pin LCC	E-28A

NOTES
[1]MIL-STD-883 versions available, contact factory.
[2]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier. For outline information see Package Information section.

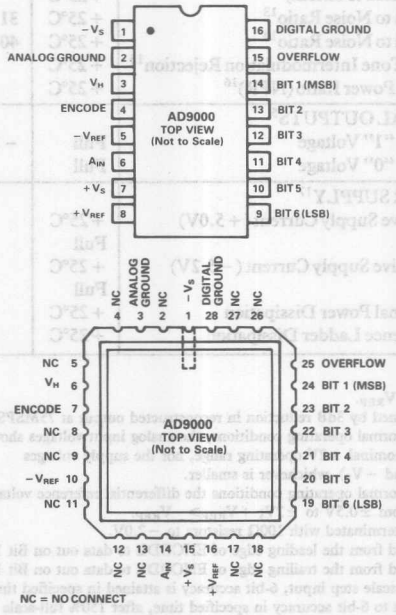
DIE LAYOUT



MECHANICAL INFORMATION

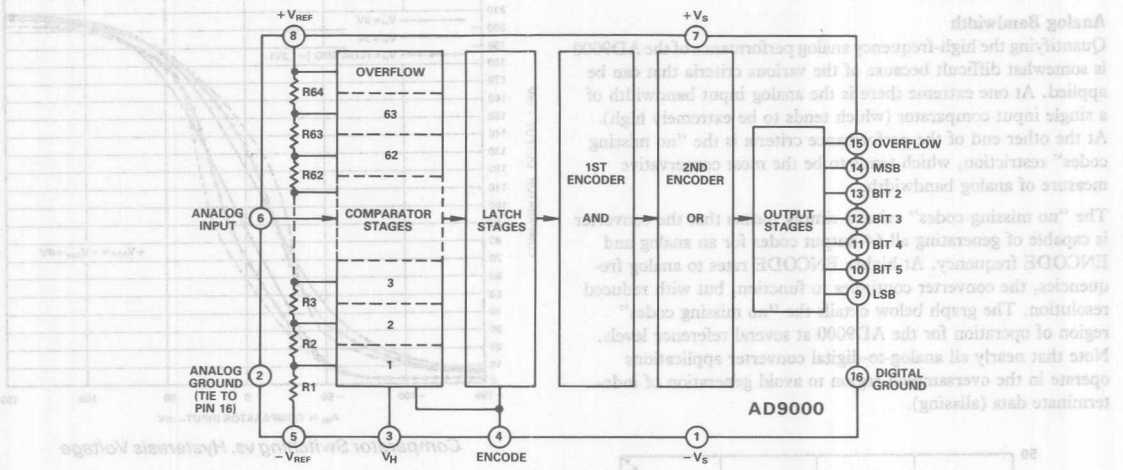
Die Dimensions	129 × 217 × 15 (±2) mils
Pad Dimensions	4 × 4 mils
Metalization	10,000Å Aluminum
Backing	None
Substrate Potential	−VS
Passivation	10,000Å Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil Aluminum; Ultrasonic Bonding or 1mil Gold; Gold Ball Bonding

PIN DESIGNATIONS

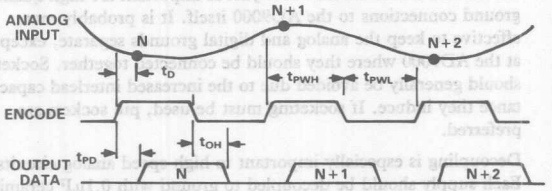


FUNCTIONAL DESCRIPTION

PIN NAME	DESCRIPTION
−VS	Negative supply terminal, nominally −5.2V.
ANALOG GROUND	Analog ground return. All grounds should be connected together near the the AD9000.
VHYSTERESIS	The hysteresis control voltage varies the comparator hysteresis from 15mV to 50mV, for a change of 0V to +3V at the hysteresis control pin.
ENCODE	The ENCODE pin controls the conversion cycle. Encode is rising edge sensitive and should be driven with a 50% duty-cycle waveform under normal conditions.
−VREF	The most negative reference voltage for the internal resistor ladder.
ANALOG INPUT	Analog input pin.
+VS	Positive supply terminal, nominally +5.0V.
+VREF	Most positive reference voltage of the internal resistor ladder.
BIT 6 (LSB)	One of six digital outputs. BIT 6 (LSB) is the least-significant-bit of the digital output.
BIT 5 – BIT 2	One of six digital outputs.
BIT 1 (MSB)	One of six digital outputs. BIT1 (MSB) is the most-significant-bit of the digital output.
OVERFLOW	Overflow data output. Logic high indicates an input overvoltage ($A_{IN} \geq +V_{REF}$).
DIGITAL GROUND	Digital ground return. All grounds should be connected together near the AD9000.

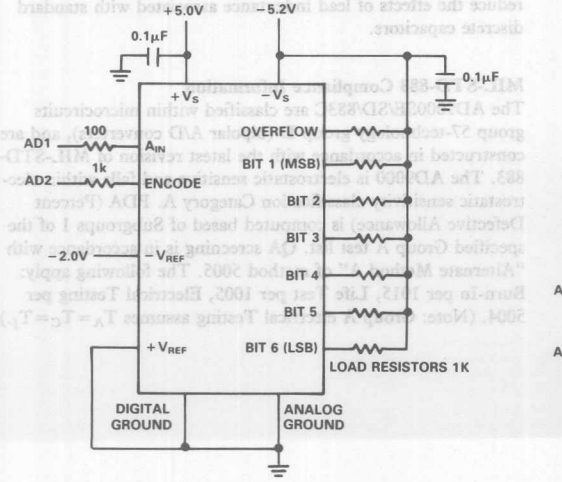


AD9000 Functional Block Diagram

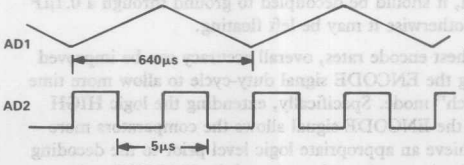


t_D	APERTURE DELAY
t_{PD}	OUTPUT PROPAGATION DELAY
t_{OH}	MINIMUM OUTPUT HOLD TIME
t_{PWH}	MINIMUM ENCODE PULSE WIDTH HIGH
t_{PWL}	MINIMUM ENCODE PULSE WIDTH LOW

System Timing Diagram



ALL RESISTORS ±5%
ALL CAPACITORS ±20%
ALL SUPPLY VOLTAGES ±5%
OPTION #1: (STATIC) ADI = 0.0V, AD2 = LOGIC HIGH
OPTION #2: (DYNAMIC) SEE WAVEFORMS



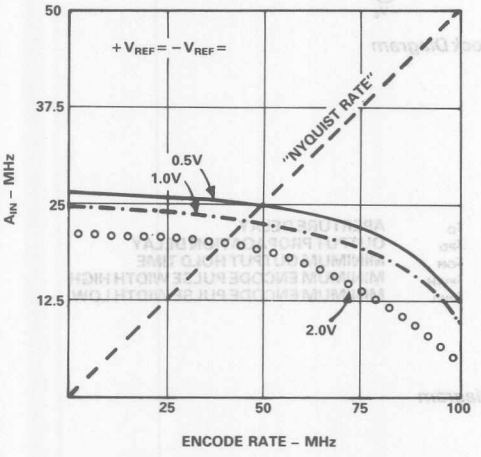
Burn-In Test Circuit

ABOUT THE AD9000

Analog Bandwidth

Quantifying the high-frequency analog performance of the AD9000 is somewhat difficult because of the various criteria that can be applied. At one extreme there is the analog input bandwidth of a single input comparator (which tends to be extremely high). At the other end of the performance criteria is the "no missing codes" restriction, which tends to be the most conservative measure of analog bandwidth.

The "no missing codes" criteria simply means that the converter is capable of generating all 64 output codes for an analog and ENCODE frequency. At higher ENCODE rates to analog frequencies, the converter continues to function, but with reduced resolution. The graph below details the "no missing codes" region of operation for the AD9000 at several reference levels. Note that nearly all analog-to-digital converter applications operate in the oversampled region to avoid generation of indeterminate data (aliasing).

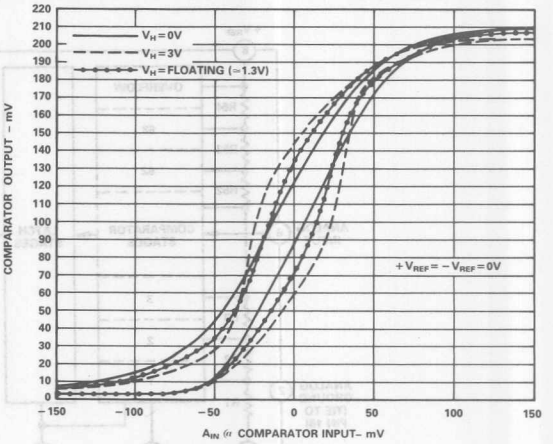


Analog Input vs. Encode Rate "No Missing Codes"

High-Speed Performance Enhancements

The AD9000 employs a hysteresis control pin which affects comparator sensitivity. The error rate (number of full-scale errors in a given period) is directly affected by the comparator sensitivity. By varying the voltage on the hysteresis control pin, the error rate can be reduced. The AD9000 is capable of extremely low error rate operation, which makes it ideal for error sensitive applications like QAM demodulation. If the hysteresis control pin is used, it should be decoupled to ground through a 0.1μF capacitor, otherwise it may be left floating.

At the highest encode rates, overall accuracy can be improved by skewing the ENCODE signal duty-cycle to allow more time in the "latch" mode. Specifically, extending the logic HIGH portion of the ENCODE signal allows the comparators more time to achieve an appropriate logic level prior to the decoding cycle that begins on the rising edge of the ENCODE pulse.



Comparator Switching vs. Hysteresis Voltage

Layout Considerations

The AD9000, like all high-speed circuits, requires certain precautions be taken to insure optimum performance. The foremost of these is the use of a substantial low impedance ground plane around and under the AD9000. Just as important are high quality ground connections to the AD9000 itself. It is probably more effective to keep the analog and digital grounds separate, except at the AD9000 where they should be connected together. Sockets should generally be avoided due to the increased interlead capacitance they induce. If socketing must be used, pin sockets are preferred.

Decoupling is especially important to high-speed analog circuits. Each supply should be decoupled to ground with 0.1μF ceramic and 0.001μF mica capacitors. The ladder reference pins should be treated in a similar manner. In addition to decoupling the reference ladder, the reference ladder should be driven from a low output impedance source for the best noise rejection. In all cases, chip capacitors are recommended, where practical, to reduce the effects of lead inductance associated with standard discrete capacitors.

MIL-STD-883 Compliance Information

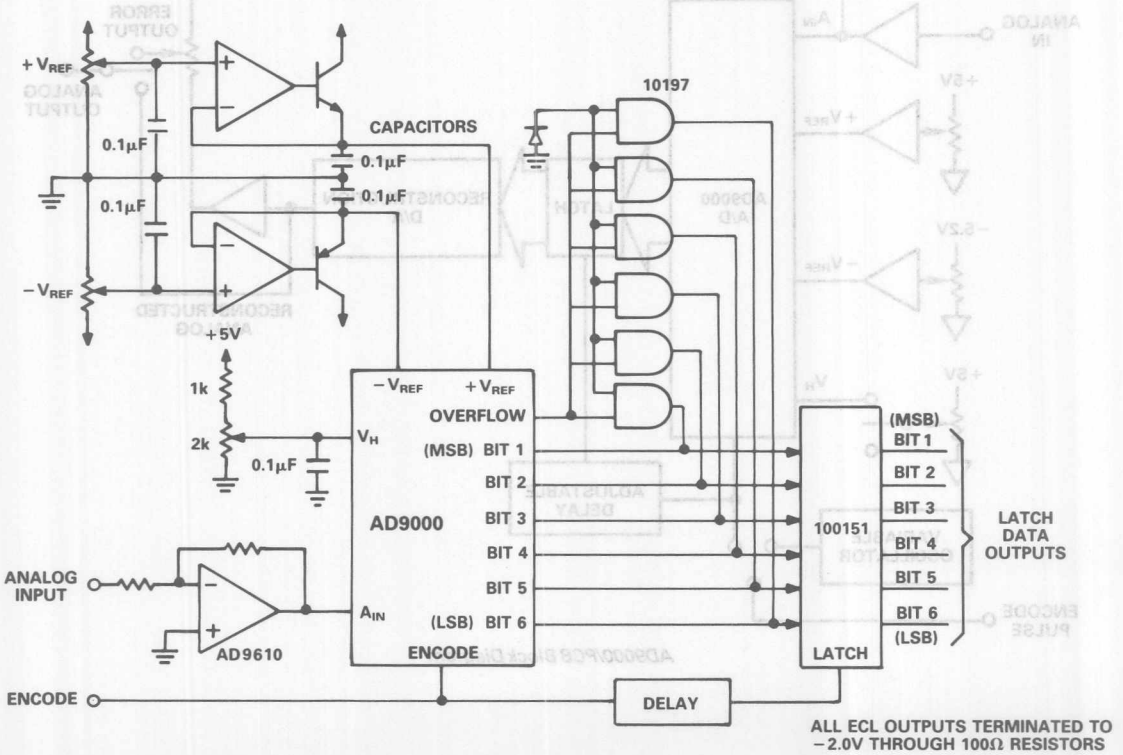
The AD9000SE/SD/883C are classified within microcircuits group 57-technology group D (bipolar A/D converters), and are constructed in accordance with the latest revision of MIL-STD-883. The AD9000 is electrostatic sensitive and falls within electrostatic sensitivity classification Category A. PDA (Percent Defective Allowance) is computed based of Subgroups 1 of the specified Group A test list. QA screening is in accordance with "Alternate Method A" of method 5005. The following apply: Burn-In per 1015, Life Test per 1005, Electrical Testing per 5004. (Note: Group A electrical Testing assumes $T_A = T_C = T_J$.)

TYPICAL APPLICATION

The AD9000 is a relatively flexible device which can be configured in a number of ways. One very useful feature of the AD9000 is the open emitter outputs. The open emitters allow the outputs of several AD9000s to be OR-WIRED in stacking applications for increased resolution. This kind of application depends on the return-to-zero nature of the output bits when $A_{IN} \geq +V_{REF}$ (overflow). In circuits which employ only one AD9000, this is not always an advantage. The circuit below illustrates one method of converting the outputs to nonreturn-to-zero.

The 10197 (standard 10K ECL logic) hex-AND group senses the active OVERFLOW output and forces all other bits to logic HIGH. The 10151 latch is not required for AD9000 applications, but it may ease data transfer sensitivities in asnychronous data collection systems.

The reference driver circuits should provide a low source impedance to prevent noise on the reference inputs from affecting the AD9000's accuracy. This is accomplished to a large extent by adequately decoupling the reference pins to ground. An improved method is employed below. The reference voltages ($+V_{REF}$, $-V_{REF}$) are buffered by a transistor/amplifier combination. This has the advantages of wide bandwidth (hence low impedance over a wide frequency range to eliminate high frequency noise components), and improved temperature stability.

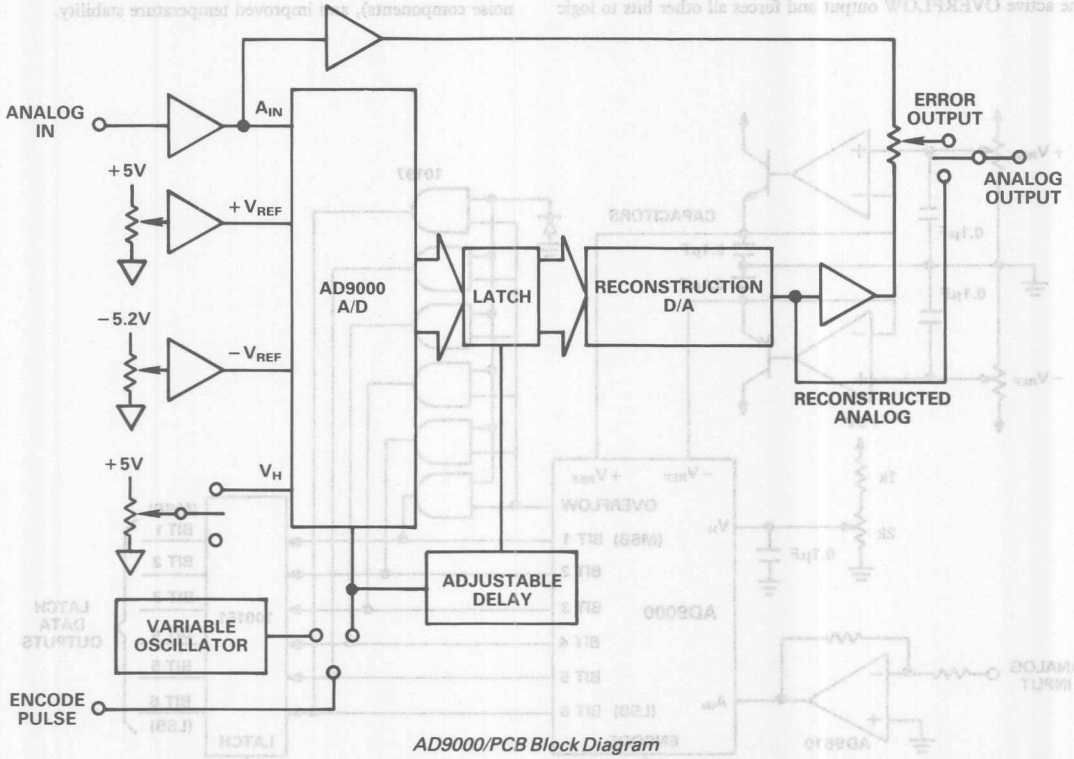


AD9000/PCB EVALUATION AND TEST BOARD

Evaluating and testing the AD9000 is greatly simplified with the AD9000/PCB evaluation board. The printed circuit board contains all of the driver and buffering circuits needed to test and evaluate the AD9000. The board outputs include both a high quality reconstructed representation of the input waveform, and a dc error waveform output which can be used to determine device linearities.

Inputs to the AD9000/PCB evaluation board include the analog signal to be digitized, as well as an optional ENCODE input for high stability measurements. All components, except the AD9000, are soldered onto the 8.5″ × 6.3″ board. The AD9000 is socketed to facilitate moderate volume testing. The evaluation board is offered with either a commercial temperature range AD9000, or an extended temperature range device installed.

The respective ordering numbers are AD9000JD/PCB and AD9000SD/PCB.



AD9000/PCB Block Diagram

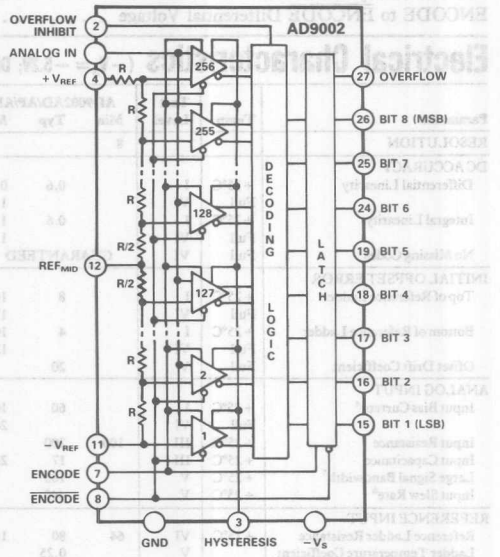
High Speed 8-Bit Monolithic A/D Converter

AD9002

FEATURES
150MSPS Encode Rate
Low Input Capacitance: 17pF
Low Power: 750mW
−5.2V Single Supply
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Radar Systems
Digital Oscilloscopes/ATE Equipment
Laser/Radar Warning Receivers
Digital Radio
Electronic Warfare (ECM, ECCM, ESM)
Communication/Signal Intelligence

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9002 is an 8-bit, high speed, analog-to-digital converter. The AD9002 is fabricated in an advanced bipolar process which allows operation at sampling rates in excess of 150 megasamples/second. Functionally, the AD9002 is comprised of 256 parallel comparator stages whose outputs are decoded to drive the ECL compatible output latches.

An exceptionally wide large signal analog input bandwidth of 160MHz is due to an innovative comparator design and very close attention to device layout considerations. The wide input bandwidth of the AD9002 allows very accurate acquisition of high speed pulse inputs, without an external track-and-hold. The comparator output decoding scheme minimizes false codes which is critical to high speed linearity.

The AD9002 provides an external hysteresis control pin which can be used to optimize comparator sensitivity to further improve performance. Additionally, the AD9002's low power dissipation of 750mW makes it usable over the full extended temperature range. The AD9002 also incorporates an overflow bit to indicate overrange inputs. This overflow output can be disabled with the overflow inhibit pin.

The AD9002 is available in two grades, one with 0.5LSB linearity and one with 0.75LSB linearity. Both versions are offered in an industrial grade, −25°C to +85°C, packaged in a 28-pin DIP and a 28-pin PLCC. The military temperature range devices, −55°C to +125°C, are available in ceramic DIP and LCC packages and are compliant to MIL-STD-883 Class B.

Supply Voltage ($-V_S$) . . . . . −6V
Analog-to-Digital Supply Voltage Differential 0.5V
Analog Input Voltage . . . . . $-V_S$ to +0.5V
Digital Input Voltage . . . . . $-V_S$ to 0V
Reference Input Voltage $(+V_{REF} - V_{REF})^2$. −3.5V to 0.1V
Differential Reference Voltage 2.1V
Reference Midpoint Current . . . . . ±4mA
ENCODE to $\overline{\text{ENCODE}}$ Differential Voltage 4V

Digital Output Current 20mA
Operating Temperature Range
AD9002AD/BD/AN/BN/AP/BP . . . . . −25°C to +85°C
AD9002SE/SD/TD/TE . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature[3] . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

Electrical Characteristics ($-V_S = -5.2V$; Differential Reference Voltage = 2.0V, unless otherwise stated)

Parameter	Temp	Test Level	AD9002AD/AP/AN Min	Typ	Max	AD9002BD/BP/BN Min	Typ	Max	AD9002SD/SE Min	Typ	Max	AD9002TD/TE Min	Typ	Max	Units
RESOLUTION			8			8			8			8			Bits
DC ACCURACY															
Differential Linearity	+25°C	I		0.6	0.75		0.4	0.5		0.6	0.75		0.4	0.5	LSB
	Full	VI			1.0			0.75			1.0			0.75	LSB
Integral Linearity	+25°C	I		0.6	1.0		0.4	0.5		0.6	1.0		0.4	0.5	LSB
	Full	VI			1.2			1.2			1.2			1.2	LSB
No Missing Codes	Full	VI	GUARANTEED			GUARANTEED			GUARANTEED			GUARANTEED			
INITIAL OFFSET ERROR															
Top of Reference Ladder	+25°C	I		8	14		8	14		8	14		8	14	mV
	Full	VI			17			17			17			17	mV
Bottom of Reference Ladder	+25°C	I		4	10		4	10		4	10		4	10	mV
	Full	VI			12			12			12			12	mV
Offset Drift Coefficient	Full	V		20			20			20			20		µV/°C
ANALOG INPUT															
Input Bias Current[4]	+25°C	I		60	100		60	100		60	100		60	100	µA
	Full	VI			200			200			200			200	µA
Input Resistance	+25°C	III	100	200		100	200		100	200		100	200		kΩ
Input Capacitance	+25°C	III		17	22		17	22		17	22		17	22	pF
Large Signal Bandwidth[5]	+25°C	V		160			160			160			160		MHz
Input Slew Rate[6]	+25°C	V		440			440			440			440		V/µs
REFERENCE INPUT															
Reference Ladder Resistance	+25°C	VI	64	80	110	64	80	110	64	80	110	64	80	110	Ω
Ladder Temperature Coefficient		V		0.25			0.25			0.25			0.25		Ω/°C
Reference Input Bandwidth	+25°C	V		10			10			10			10		MHz
DYNAMIC PERFORMANCE															
Conversion Rate	+25°C	I	125	150		125	150		125	150		125	150		MSPS
Aperture Delay	+25°C	V		1.3			1.3			1.3			1.3		ns
Aperture Uncertainty (Jitter)	+25°C	V		15			15			15			15		ps
Output Delay (t_{PD})[7,8]	+25°C	I	2.5	3.7	5.5	2.5	3.7	5.5	2.5	3.7	5.5	2.5	3.7	5.5	ns
Transient Response[9]	+25°C	V		6			6			6			6		ns
Overvoltage Recovery Time[10]	+25°C	V		6			6			6			6		ns
Output Rise Time[7]	+25°C	I		3.0				3.0		3.0				3.0	ns
Output Fall Time[7]	+25°C	I		2.5				2.5		2.5				2.5	ns
Output Time Skew[7,11]	+25°C	V		0.6			0.6			0.6			0.6		ns
ENCODE INPUT															
Logic "1" Voltage[7]	Full	VI	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage[7]	Full	VI			−1.5			−1.5			−1.5			−1.5	V
Logic "1" Current	Full	VI			150			150			150			150	µA
Logic "0" Current	Full	VI			120			120			120			120	µA
Input Capacitance	+25°C	V		3			3			3			3		pF
Encode Pulse Width (Low)[12]	+25°C	I	1.5			1.5			1.5			1.5			ns
Encode Pulse Width (High)[12]	+25°C	I	1.5			1.5			1.5			1.5			ns
OVERFLOW INHIBIT INPUT															
0V Input Current	Full	VI		144	300		144	300		144	300		144	300	µA
AC LINEARITY[13]															
Effective Bits[14]	+25°C	V		7.6			7.6			7.6			7.6		Bits
In-Band Harmonics															
dc to 1.23MHz	+25°C	I	48	55		48	55		48	55		48	55		dB
dc to 9.3MHz	+25°C	V		50			50			50			50		dB
dc to 19.3MHz	+25°C	V		44			44			44			44		dB
Signal-to-Noise Ratio[15]	+25°C	I	46	47.6		46	47.6		46	47.6		46	47.6		dB
Two Tone Intermod Rejection[16]	+25°C	V		60			60			60			60		dB
DIGITAL OUTPUTS[7]															
Logic "1" Voltage	Full	VI	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			−1.5			−1.5			−1.5	V
POWER SUPPLY[17]															
Supply Current (−5.2V)	+25°C	I		145	175		145	175		145	175		145	175	mA
	Full	VI			200			200			200			200	mA
Nominal Power Dissipation	+25°C	V		750			750			750			750		mW
Reference Ladder Dissipation	+25°C	V		50			50			50			50		mW
Power Supply Rejection Ratio[18]	+25°C	I		0.8	1.5		0.8	1.5		0.8	1.5		0.8	1.5	mV/V

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

[2]$+V_{REF} \geq -V_{REF}$ under all circumstances.

[3]Maximum junction temperature (t_J max) should not exceed 175°C for ceramic packages, and 150°C for plastic packages:

$t_J = PD\ (\theta_{JA}) + t_A$

$PD\ (\theta_{JC}) + t_C$

where

PD = power dissipation

θ_{JA} = thermal impedance from junction to ambient (°C/W)

θ_{JC} = thermal impedance from junction to case (°C/W)

t_A = ambient temperature (°C)

t_C = case temperature (°C)

typical thermal impedances are:

Ceramic DIP $\theta_{JA} = 56°C/W$; $\theta_{JC} = 20°C/W$

Plastic DIP $\theta_{JA} = 60°C/W$; $\theta_{JC} = 20°C/W$

Ceramic LCC $\theta_{JA} = 69°C/W$; $\theta_{JC} = 23°C/W$

PLCC $\theta_{JA} = 60°C/W$, $\theta_{JC} = 19°C/W$.

[4]Measured with AIN = 0V.

[5]Measured by FFT analysis where fundamental is −3dBc.

[6]Input slew rate derived from rise time (10 to 90%) of full scale input.

[7]Outputs terminated through 100Ω to −2V.

[8]Measured from ENCODE in to data out for LSB only.

[9]For full-scale step input, 8-bit accuracy is attained in specified time.

[10]Recovers to 8-bit accuracy in specified time after 150% full-scale input overvoltage.

[11]Output time skew includes high-to-low and low-to-high transitions as well as bit-to-bit time skew differences.

[12]ENCODE signal rise/fall times should be less than 10ns for normal operation.

[13]Measured at 125MSPS encode rate.

[14]Analog input frequency = 1.23MHz.

[15]RMS signal to rms noise, with 1.23MHz analog input signal.

[16]Input signals 1V p-p @1.23MHz and 1V p-p @2.30MHz.

[17]Supplies should remain stable within ±5% for normal operation.

[18]Measured at −5.2V ±5%.

Specifications subject to change without notice.

2

Recommended Operating Conditions

Parameter	Input Voltage Min	Nominal	Max
$-V_S$	−5.46	−5.20	−4.94
$+V_{REF}$	$-V_{REF}$	0.0V	+0.1
$-V_{REF}$	−2.1	−2.0	$+V_{REF}$
Analog Input	$-V_{REF}$		$+V_{REF}$

EXPLANATION OF TEST LEVELS

Test Level I – 100% production tested.

Test Level II – 100% production tested at +25°C, and sample tested at specified temperatures.

Test Level III – Sample tested only.

Test Level IV – Parameter is guaranteed by design and characterization testing.

Test Level V – Parameter is a typical value only.

Test Level VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Model	Linearity	Temperature Range	Package Option[1]
AD9002AD	0.75LSB	−25°C to +85°C	D-28
AD9002BD	0.50LSB	−25°C to +85°C	D-28
AD9002AN	0.75LSB	−25°C to +85°C	N-28
AD9002BN	0.50LSB	−25°C to +85°C	N-28
AD9002AP	0.75LSB	−25°C to +85°C	P-28A
AD9002BP	0.50LSB	−25°C to +85°C	P-28A
AD9002SD[2]	0.75 LSB	−55°C to +125°C	D-28
AD9002SE[2]	0.75 LSB	−55°C to +125°C	E-28A
AD9002TD[2]	0.50 LSB	−55°C to +125°C	D-28
AD9002TE[2]	0.50 LSB	−55°C to +125°C	E-28A

NOTES

[1]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

[2]MIL-STD-883 versions available: Contact factory.

FUNCTIONAL DESCRIPTION

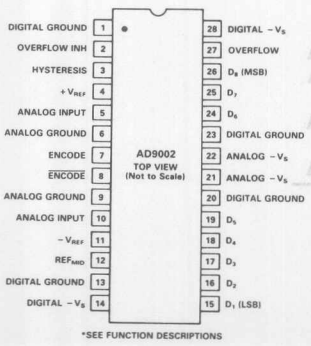
Pin #	Name	Description
1	DIGITAL GROUND	One of four digital ground pins. All digital ground pins should be connected together.
2	OVERFLOW INH	OVERFLOW INHIBIT controls the data output polarity for overvoltage inputs.

ANALOG INPUT	OVERFLOW ENABLED (FLOATING OR −5.2V) OF D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8	OVERFLOW INHIBITED (GND) OF D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8
$V_{IN} > +V_{REF}$	1 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1
$V_{IN} \leq +V_{REF}$	0 X X X X X X X X	0 X X X X X X X X

3	HYSTERESIS	The Hysteresis control voltage varies the comparator hysteresis from 0mV to 10mV, for a change from −5.2V to −2.2V at the Hysteresis control pin.
4	$+V_{REF}$	The most positive reference voltage for the internal resistor ladder.
5	ANALOG INPUT	One of two analog input pins. Both analog input pins should be connected together.
6	ANALOG GROUND	One of two analog ground pins. Both analog ground pins should be connected together.
7	ENCODE	Noninverted input of the differential encode input. This pin is driven in conjunction with $\overline{\text{ENCODE}}$. Data is latched on the rising edge of the ENCODE signal.
8	$\overline{\text{ENCODE}}$.	Inverted input of the differential encode input. This pin is driven in conjunction with ENCODE.
9	ANALOG GROUND	One of two analog ground pins. Both analog ground pins should be connected together.
10	ANALOG INPUT	One of two analog input pins. Both analog inputs should be connected together.
11	$-V_{REF}$	The most negative reference voltage for the internal resistor ladder.
12	REF_{MID}	The midpoint tap on the internal resistor ladder.
13	DIGITAL GROUND	One of four digital ground pins. All digital ground pins should be connected together.
14	DIGITAL $-V_S$	One of two negative digital supply pins (nominally −5.2V). Both digital supply pins should be connected together.
15	D1	Digital data output (LSB).
16-19	D2-D5	Digital data output.
20	DIGITAL GROUND	One of four digital ground pins. All digital ground pins should be connected together.
21, 22	ANALOG $-V_S$	One of two negative analog supply pins (nominally −5.2V). Both analog supply pins should be connected together.
23	DIGITAL GROUND	One of four digital ground pins. All digital ground pins should be connected together.
24, 25	D6, D7	Digital data output.
26	D8	Digital data output (MSB).
27	OVERFLOW	Overflow data output. Logic high indicates an input overvoltage ($V_{IN} > +V_{REF}$) if OVERFLOW INHIBIT is enabled (overflow enabled, −5.2V). See OVERFLOW INHIBIT.
28	DIGITAL $-V_S$	One of two negative digital supply pins (nominally −5.2V). Both digital supply pins should be connected together.

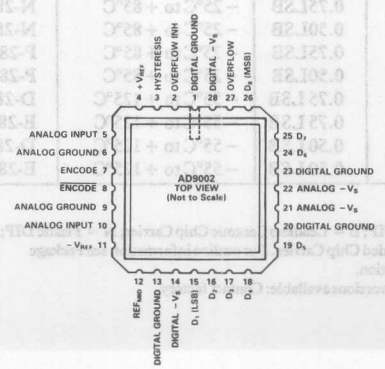
PIN DESIGNATIONS

DIP

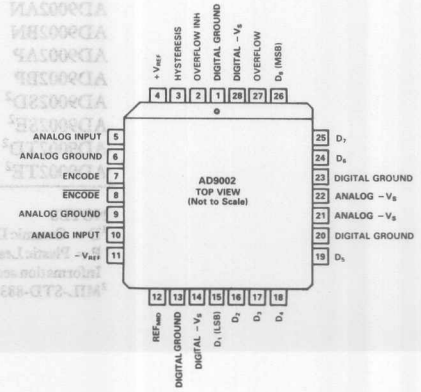


*SEE FUNCTION DESCRIPTIONS

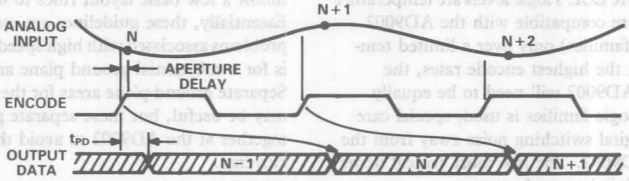
LCC



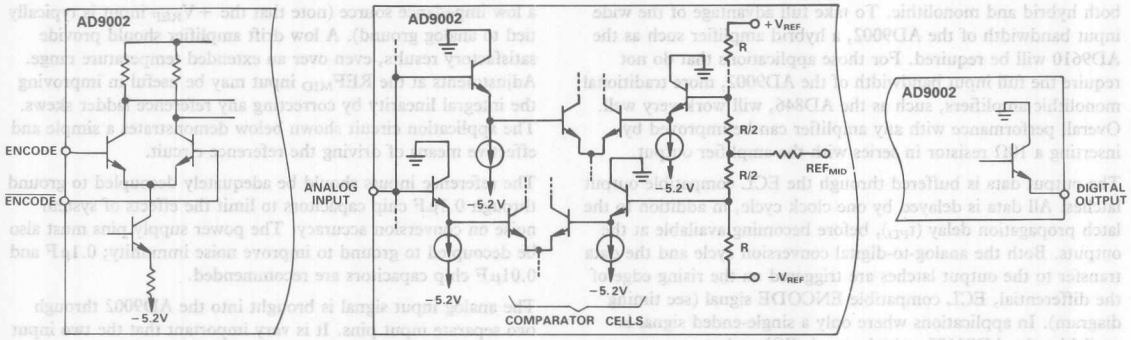
PLCC



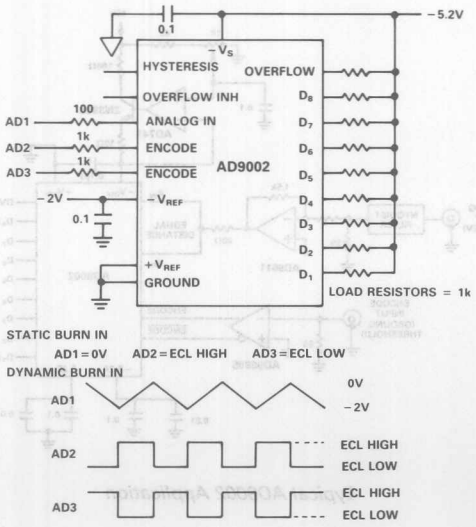
TIMING DIAGRAM



INPUT OUTPUT CIRCUITS

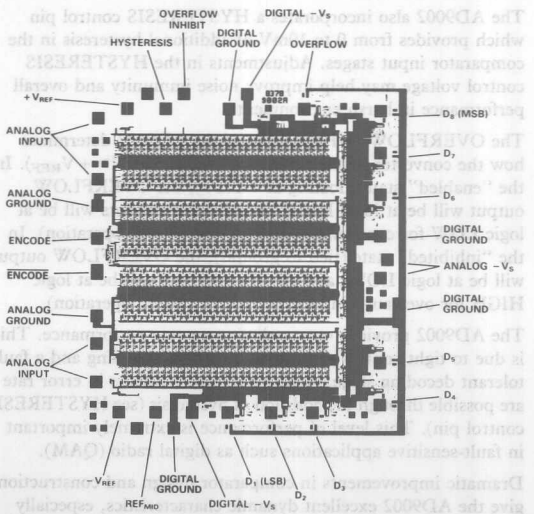


BURN-IN DIAGRAM



ALL RESISTORS ±5%, Ω
ALL CAPACITORS ±20%, µF
ALL SUPPLIES ±5%

DIE LAYOUT AND MECHANICAL INFORMATION



Die Dimensions	106 × 114 × 15 (±2) mils
Pad Dimensions	4 × 4 mils
Metalization	Gold
Backing	None
Substrate Potential	$-V_S$
Passivation	Nitride
Die Attach	Gold Eutectic (Ceramic) Epoxy (Plastic)
Bond Wire	1–1.3 mil Gold; Gold Ball Bonding

APPLICATION INFORMATION

The AD9002 is compatible with all standard ECL logic families, including 10K and 10KH. 100K ECL's logic levels are temperature compensated, and are therefore compatible with the AD9002 (and most other ECL device families) only over a limited temperature range. To operate at the highest encode rates, the supporting logic around the AD9002 will need to be equally fast. Whichever of the ECL logic families is used, special care must be exercised to keep digital switching noise away from the analog circuits around the AD9002. The two most critical items are digital supply lines and digital ground return.

The input capacitance of the AD9002 is an exceptionally low 17pF. This allows the use of a wide range of input amplifiers, both hybrid and monolithic. To take full advantage of the wide input bandwidth of the AD9002, a hybrid amplifier such as the AD9610 will be required. For those applications that do not require the full input bandwidth of the AD9002, more traditional monolithic amplifiers, such as the AD846, will work very well. Overall performance with any amplifier can be improved by inserting a 10Ω resistor in series with the amplifier output.

The output data is buffered through the ECL compatible output latches. All data is delayed by one clock cycle, in addition to the latch propagation delay (t_{PD}), before becoming available at the outputs. Both the analog-to-digital conversion cycle and the data transfer to the output latches are triggered on the rising edge of the differential, ECL compatible ENCODE signal (see timing diagram). In applications where only a single-ended signal is available, the AD96685, a high speed, ECL voltage comparator, can be employed to generate the differential signals. All ECL signals (including the overflow bit) should be terminated properly to avoid ringing and reflection.

The AD9002 also incorporates a HYSTERESIS control pin which provides from 0 to 10mV of additional hysteresis in the comparator input stages. Adjustments in the HYSTERESIS control voltage may help improve noise immunity and overall performance in harsh environments.

The OVERFLOW INHIBIT pin of the AD9002 determines how the converter handles overrange inputs ($AIN \geq +V_{REF}$). In the "enabled" state (floating at $-5.2V$), the OVERFLOW output will be at logic HIGH and all other outputs will be at logic LOW for overrange inputs (return-to-zero operation). In the "inhibited" state (tied to ground), the OVERFLOW output will be at logic LOW, and all other outputs will be at logic HIGH for overrange inputs (nonreturn-to-zero operation).

The AD9002 provides outstanding error rate performance. This is due to tight control of comparator offset matching and a fault tolerant decoding stage. Additional improvements in error rate are possible through the addition of hysteresis (see HYSTERESIS control pin). This level of performance is extremely important in fault-sensitive applications such as digital radio (QAM).

Dramatic improvements in comparator design and construction give the AD9002 excellent dynamic characteristics, especially SNR (signal-to-noise ratio). The 160MHz input bandwidth and low error rate performance give the AD9002 an SNR of 48dB with a 1.23MHz input. High SNR performance is particularly important in wide bandwidth applications, such as pulse signature analysis, commonly performed in advanced radar receivers.

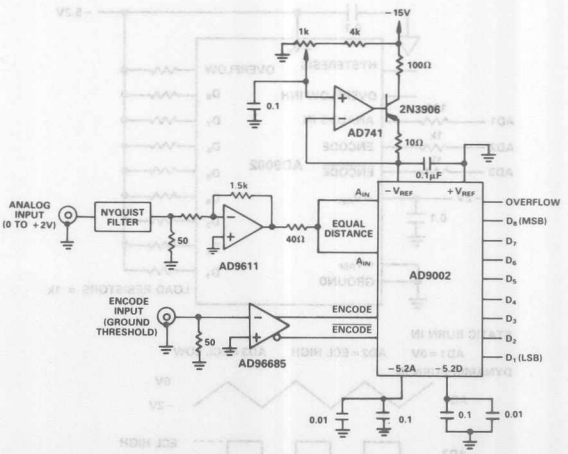
LAYOUT SUGGESTIONS

Designs using the AD9002, like all high speed devices, must follow a few basic layout rules to insure optimum performance. Essentially, these guidelines are meant to avoid many of the problems associated with high speed designs. The first requirement is for a substantial ground plane around and under the AD9002. Separate ground plane areas for the digital and analog components may be useful, but these separate grounds should be connected together at the AD9002 to avoid the effects of "ground loop" currents.

The second area that requires an extra degree of attention involves the three reference inputs, $+V_{REF}$, REF_{MID}, and $-V_{REF}$. The $+V_{REF}$ input and the $-V_{REF}$ input should both be driven from a low impedance source (note that the $+V_{REF}$ input is typically tied to analog ground). A low drift amplifier should provide satisfactory results, even over an extended temperature range. Adjustments at the REF_{MID} input may be useful in improving the integral linearity by correcting any reference ladder skews. The application circuit shown below demonstrates a simple and effective means of driving the reference circuit.

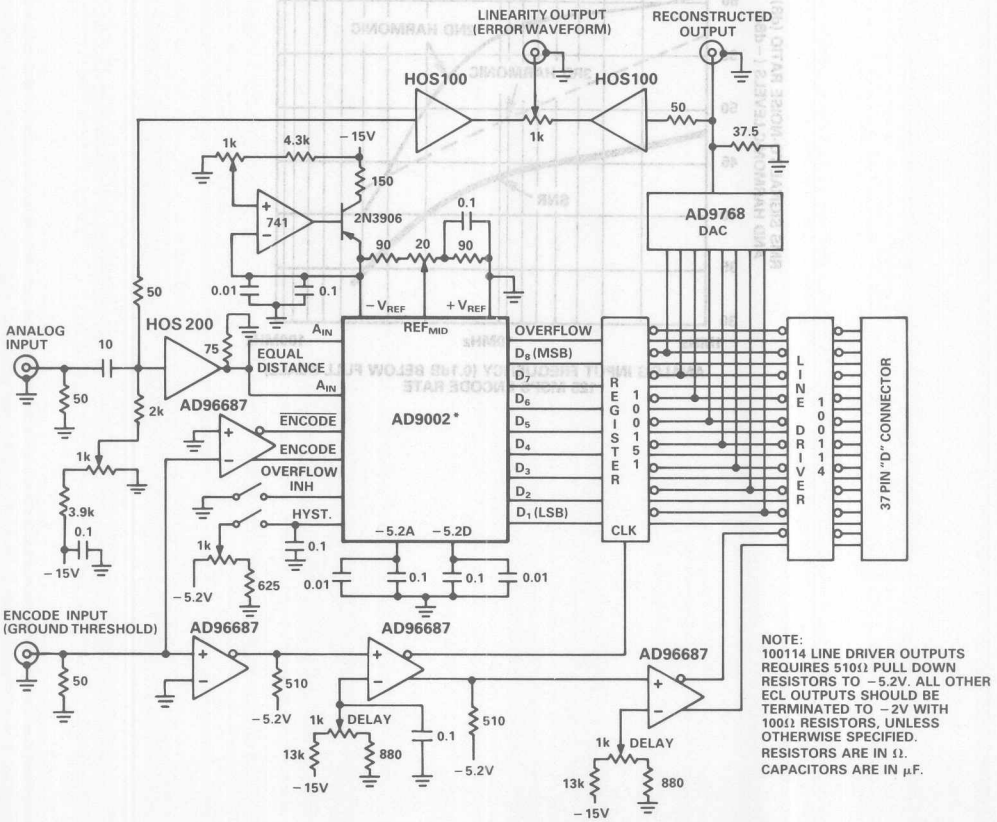
The reference inputs should be adequately decoupled to ground through 0.1μF chip capacitors to limit the effects of system noise on conversion accuracy. The power supply pins must also be decoupled to ground to improve noise immunity; 0.1μF and 0.01μF chip capacitors are recommended.

The analog input signal is brought into the AD9002 through two separate input pins. It is very important that the two input pins be driven symmetrically with equal length electrical connections. Otherwise, aperture delay errors may degrade converter performance at high frequencies.



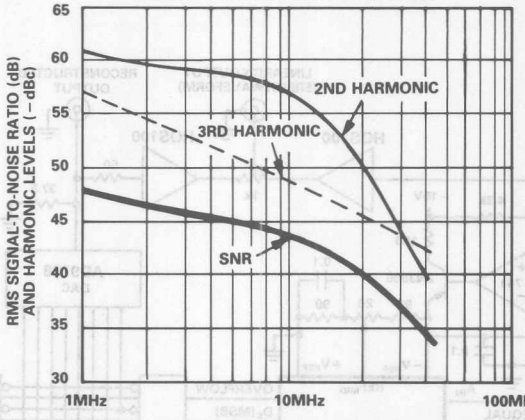
Typical AD9002 Application

AD9002 EVALUATION CIRCUIT



*CONTACT FACTORY ABOUT EVALUATION BOARD AVAILABILITY

AD9002 DYNAMIC PERFORMANCE



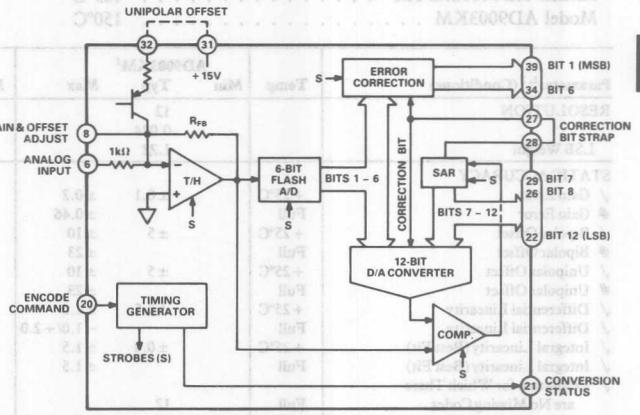
12-Bit, 1 MSPS A/D Converter

AD9003

FEATURES
- 12-Bit Resolution
- 1 MSPS Word Rates
- T/H and Timing Included
- Single 40-Pin DIP

APPLICATIONS
- Radar Systems
- Digital Oscilloscopes
- Test Systems
- Analytical Instrumentation
- Waveform Analyzers

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9003 is a complete 12-bit, 1 MSPS analog-to-digital converter (ADC) which combines low cost and high performance in a single 40-pin DIP. This unique converter includes track-and-hold (T/H), timing, and encoding functions with a power dissipation of only 2.2 watts.

This remarkable unit is capable of converting analog signals to the Nyquist limit at word rates through 1 MSPS. Its 1μs conversion interval includes acquisition time for the internal T/H, making it a true 1 MSPS converter.

Proprietary conversion techniques achieve linearity equivalent to the best successive approximation ADC along with subranging conversion speeds. A conversion status signal simplifies transferring output data into system logic. Innovative thick- and thin-film technologies assure excellent performance over temperature without compromising ac characteristics.

The AD9003KM operates at case temperatures from 0 to +70°C; the SM and TM units operate from −25°C to +100°C.

AD9003 — SPECIFICATIONS (typical with nominal supplies, unless otherwise noted.)

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- $\pm V_S$ . . . . . ±18V
- V_{CC} . . . . . −0.5V to +7V

Analog Input . . . . . ±15V
Digital Inputs . . . . . −0.5 to V_{CC}
Maximum Junction Temperature
- Models AD9003SM/TM . . . . . 165°C
- Model AD9003KM . . . . . 150°C

Operating Temperature Range (Case)
- AD9003KM . . . . . 0 to +70°C
- AD9003SM/TM . . . . . −25°C to +100°C

Storage Temperature . . . . . −65°C to +150°C
Lead Soldering Temperature (10 sec) . . . . . +300°C

Parameter[1, 2] (Conditions)	Temp	AD9003KM[1] Min	Typ	Max	AD9003SM[2] Min	Typ	Max	AD9003TM[2] Min	Typ	Max	Units
RESOLUTION			12			12			12		Bits
			0.024			0.024			0.024		%FS
LSB Weight			1.22			1.22			1.22		mV
STATIC ACCURACY											
√ Gain Error	+25°C		±0.1	±0.2		±0.1	±0.2		±0.1	±0.2	%FS
# Gain Error	Full			±0.46			±0.6			±0.6	%FS
√ Bipolar Offset	+25°C		±5	±10		±5	±10		±5	±10	mV
# Bipolar Offset	Full			±23			±32			±32	mV
√ Unipolar Offset	+25°C		±5	±10		±5	±10		±5	±10	mV
# Unipolar Offset	Full			±23			±32			±32	mV
√ Differential Linearity	+25°C		±0.5	±1.0		±0.5	±1.0		±0.5	±1.0	LSB
√ Differential Linearity	Full			−1.0/+2.0			−1.0/+2.0			±1.0	LSB
√ Integral Linearity (Best Fit)	+25°C		±0.8	±1.5		±0.8	±1.5		±0.8	±1.5	LSB
√ Integral Linearity (Best Fit)	Full			±1.5			±2.0			±2.0	LSB
√ Resolution for Which There are No Missing Codes	Full		12			12			12		Bits
DYNAMIC CHARACTERISTICS (Conversion Rate = 1MHz)[3]											
In-Band Harmonics[4]											
√ dc to 100kHz	+25°C	74	80		74	80		74	80		dB
√ dc to 100kHz	Full	72			72			72			dB
# 100kHz to 500kHz	+25°C		75			75			75		dB
√ Conversion Time[5]	+25°C		820	850		820	850		820	850	ns
# Effective Aperture Delay Time	+25°C	6	16	27	6	16	27	6	16	27	ns
# Aperture Uncertainty (Jitter)	+25°C		26			26			26		ps, rms
√ Signal-to-Noise Ratio[6]	+25°C	65	69		65	69		65	69		dB
√ Signal-to-Noise Ratio[6]	Full	65			65			65			dB
# Transient Response[7]	+25°C		200			200			200		ns
# Overvoltage Recovery Time[8]	+25°C			1500			1500			1500	ns
# Two-Tone Intermodulation[9]	+25°C		87			87			87		dB
ANALOG INPUT											
# Voltage Range (Full Scale)[10]	Full		5			5			5		V, p-p
# Input Impedance	+25°C	950	1000	1050	950	1000	1050	950	1000	1050	Ω
# Input Impedance	Full	950	1000	1050	950	1000	1050	950	1000	1050	Ω
Input Bandwidth											
# Small Signal, −3dB[11]	+25°C		10			10			10		MHz
# Large Signal, −3dB[12]	+25°C		8			8			8		MHz
TEMPERATURE DRIFT											
Offset Temperature Coefficient											
√ Bipolar	Full		±10	±35		±10	±40		±10	±40	ppm/°C
√ Unipolar	Full		±10	±35		±10	±40		±10	±40	ppm/°C
√ Gain Temperature Coefficient	Full		±15	±40		±15	±40		±15	±40	ppm/°C
# Differential Linearity Tempco	Full		±1.5	±3.5		±1.5	±3.5		±1.5	±3.5	ppm/°C
DIGITAL INPUTS											
# Logic Compatibility	Full		TTL			TTL			TTL		
# Logic "1" Voltage	Full	+2.0		V_{CC}	+2.0		V_{CC}	+2.0		V_{CC}	V
# Logic "0" Voltage	Full	−0.5		+0.8	−0.5		+0.8	−0.5		+0.8	V
Encode Command[13]											
Input Current											
# Logic "1"	Full			60			60			60	μA
# Logic "0"	Full			−1.2			−1.2			−1.2	mA
# Width[14]	Full	200		750	200		750	200		750	ns
# Rate	Full	dc		1.0	dc		1.0	dc		1.0	MSPS
# Rise/Fall Times	Full			10			10			10	ns

Parameter[1, 2] (Conditions)	Temp	AD9003KM[1] Min	Typ	Max	AD9003SM[2] Min	Typ	Max	AD9003TM[2] Min	Typ	Max	Units
DIGITAL OUTPUTS											
# Logic Compatibility	Full		TTL			TTL			TTL		
# Logic "1" Voltage	Full	+2.4			+2.4			+2.4			V
# Logic "0" Voltage	Full			+0.4			+0.4			+0.4	V
# Output Drive	Full		1 Standard			1 Standard			1 Standard		TTL Load
Format			Parallel			Parallel			Parallel		
Coding											
Unipolar Mode			Complementary Binary			Complementary Binary			Complementary Binary		
Bipolar Mode			Complementary Offset Binary			Complementary Offset Binary			Complementary Offset Binary		
POWER REQUIREMENTS											
$+V_S$ Voltage	Full	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	V
✓ $+V_S$ Current	Full		78	90		78	90		78	90	mA
$-V_S$ Voltage	Full	−14.5	−15.0	−15.5	−14.5	−15.0	−15.5	−14.5	−15.0	−15.5	V
✓ $-V_S$ Current	Full		44	49		44	49		44	49	mA
V_{CC} Voltage	Full	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	V
✓ V_{CC} Current	Full		75	200		75	200		75	200	mA
✓ Power Dissipation	Full		2.2	3.2		2.2	3.2		2.2	3.2	W
# PSRR[15]	+25°C		45			45			45		dB
THERMAL RESISTANCE											
Junction to Air, θ_{CA}[16]			19			19			19		°C/W
Junction to Case, θ_{JC}			3			3			3		°C/W
MTBF[17]											
Mean Time Between Failures					7.84 × 10^4			7.84 × 10^4			Hours
PACKAGE OPTION[18]											
M-40			AD9003KM			AD9003SM			AD9003TM		

NOTES

✓ 100% tested (See Notes 1 and 2). #Specification guaranteed by design; not tested.

[1]AD9003KM parameters preceded by a check (✓) are tested at +25°C ambient temperature; performance is guaranteed over the commercial temperature range (0 to +70°C case temperature).

[2]AD9003SM and TM parameters preceded by a check (✓) are tested at −25°C case, +25°C ambient, and +100°C case temperatures.

[3]Converting in excess of 1.0MHz is possible; however, acquisition time is reduced, which may increase distortion of high-frequency analog signals.

[4]In-band harmonics are expressed in dB below FS in terms of spurious in-band signals generated at 1MHz encode rate and single tone analog input in range shown.

[5]Measured from leading edge of encode command to trailing (rising) edge of conversion status signal (see Timing Diagram).

[6]RMS signal to rms noise ratio; analog input 1dB below FS @ 100kHz; 1MHz encode rate.

[7]For full-scale step input, 12-bit accuracy attained in specified time.

[8]Recovers to 12-bit accuracy in specified time after 2 × FS input overvoltage. (See text and Figure 5 for information on overloads.)

[9]Intermodulation measured in dB below FS at 1MHz encode rate with input frequencies of 75kHz and 105kHz; each 7dB below FS.

[10]Voltage Range = ±2.5V or 0V to −5.0V.

[11]With analog input 40dB below FS.

[12]With FS analog input. (Large-signal BW flat within 0.5dB, dc to 500kHz.)

[13]Transition from "0" to "1" initiates conversion.

[14]For 1MHz encode rate. At conversions below 1MHz, max width is conversion period minus 250ns. Optimum linearity at 200 to 250ns widths.

[15]Power Supply Rejection Ratio (PSRR) is sensitivity of offset to V_{CC}. This is parameter which is most sensitive to variations in supply voltage.

[16]The relationship between the device package and outside environment (θ_{ca}) varies with the application. Value shown is based on measuring case temperature with supply voltages applied to a device installed in a ZIF socket mounted on a standard "EJ" burn-in board.

[17]Calculated for SM/TM versions using MIL-HNBK-217; Ground Fixed; +80°C case temperature.

[18]M = Metal Can DIP. For outline information see Package Information section.

ORDERING INFORMATION

For operating case temperatures from 0 to +70°C, order part number AD9003KM. Two models are available for operation at case temperatures betweeen −25°C and +100°C. With the exception of differential linearity, the electrical specifications on these devices are the same. The AD9003SM guarantees no missing codes over temperature; the AD9003TM is screened for differential nonlinearity of ±1LSB maximum.

Both the commercial temperature and extended temperature versions are packaged in 40-pin metal can DIPs.

PIN	FUNCTION	PIN	FUNCTION
40	DIGITAL GROUND	1	+5V
39	BIT 1	2	REFERENCE BYPASS[1]
38	BIT 2	3	DIGITAL GROUND
37	BIT 3	4	DIGITAL GROUND
36	BIT 4	5	−15V
35	BIT 5	6	ANALOG INPUT
34	BIT 6	7	DO NOT CONNECT
33	+5V	8	GAIN & OFFSET ADJUST
32	UNIPOLAR OFFSET[2]	9	ANALOG GROUND
31	UNIPOLAR OFFSET[1,2]	10	ANALOG GROUND
30	+15V	11	ANALOG GROUND
29	BIT 7	12	ANALOG GROUND
28	CORRECTION BIT[3]	13	ANALOG GROUND
27	CORRECTION BIT[3]	14	ANALOG GROUND
26	BIT 8	15	ANALOG GROUND
25	BIT 9	16	ANALOG GROUND
24	BIT 10	17	+5V
23	BIT 11	18	DIGITAL GROUND
22	BIT 12	19	−15V
21	CONVERSION STATUS	20	ENCODE COMMAND

NOTES
Although Grounds are Designated as Analog or Digital, All Grounds Should Be Connected to a Single Common Low-Impedance Ground Plane for Best Results.

[1]Pins 2 and 31 Must Be Bypassed to Ground with 0.1μF for Optimum Performance.
[2]For Unipolar Operation, Connect Pins 31 and 32; for Bipolar Operation, Ground Pin 32 and Connect Pin 31 Only to 0.1μF.
[3]Pins 27 and 28 Must Always Be Strapped Together with No Other Connections.

THEORY OF OPERATION

Refer to the block diagram of the AD9003.

Basically, the design of the unit is based on successive approximation techniques. However, the AD9003 also uses parallel encoding for the most significant bits (MSBs).

When a TTL-compatible Encode Command signal is applied to Pin 20, it causes the internal Timing Generator to generate strobe pulses used for controlling the timing of the various actions within the device.

The encode command causes the track-and-hold (T/H) to switch from a "track" mode to a "hold" mode; switches the 6-bit flash converter to a tracking mode of operation to allow it to reach the held value from the T/H; and resets the SAR. When the flash converter output has been determined, Bits 1 – 6 become inputs to the 12-bit D/A converter.

If the D/A voltage applied to the comparator is greater than the "held" value being applied to the comparator, a correction bit is turned on. If the D/A voltage is less, there is no correction bit and no change in the signal.

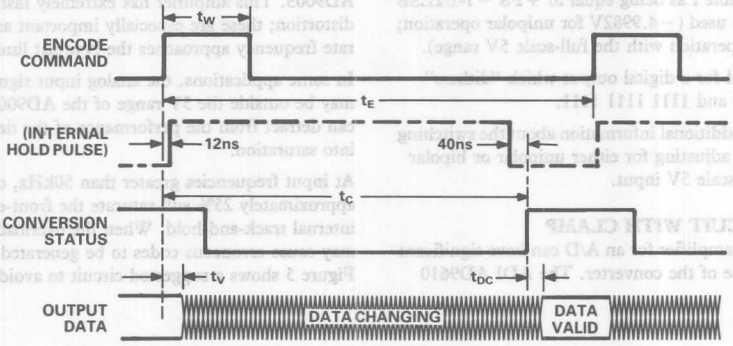
At this point, the D/A output voltage and the correction circuit outputs are 12-bit accurate. Standard successive approximation techniques are used to determine Bits 7 – 12; the end result is a 12-bit parallel output from the AD9003 A/D Converter.

The overall linearity of the AD9003 is independent of the flash converter, which materially enhances the performance of the unit. In addition, the architecture used in the converter makes it less sensitive to nonlinearities caused by D/A and/or comparator settling.

Performance of the AD9003 is equivalent to that of an ultrahigh-speed SAR type of design. But the design techniques which are used relieve the stringent comparator/DAC settling requirements usually associated with SAR designs. Instead, the AD9003 reaps the benefits of combining the best characteristics of flash converters and SARs while avoiding the penalties which are inherent in each individually.

Refer to Figure 1, the timing diagram for the AD9003. In this illustration, spacing between encode commands is shown as it would be for a 1MHz word rate, i.e., 1000ns. The width of the encode pulse is at its minimum value of 200ns.

The period of data validity associated with each encode command appears, in the figure, to be relatively short. Remember, however, each encode command generates the necessary switching to perform the digitizing function, and causes the output data to begin changing.



		MIN	MAX
t_W	ENCODE COMMAND PULSE WIDTH	200ns	750ns
t_E	SPACING BETWEEN ENCODE COMMANDS	1000ns	
t_C	CONVERSION TIME		850ns
t_V	DATA VALID		50ns
t_{DC}	DATA CHANGING		35ns

Figure 1. AD9003 Timing Diagram

In Figure 1, the timing is based on a maximum encode rate, with minimum spacing between encode commands. At lower conversion rates, this spacing would be lengthened correspondingly and the interval when data are valid would become longer.

Internal timing within the AD9003 typically requires 770ns to accomplish the necessary switching and processing of the analog input "frozen" by the encode command. Since the AD9003 is a true 1MHz converter, this leaves 230ns for the T/H to re-establish full accuracy when it returns to the "track" mode at the completion of the digitizing period.

This addition of the required 770ns and the 230ns accuracy increment shows up as a total of 1,000ns minimum between encode commands in Figure 1; any shorter interval will detract from the overall performance of the unit. Higher encode rates, i.e., shorter intervals between encode commands, are possible; but they may cause distortion on high-frequency analog signals because the T/H will not be fully settled when it is switched to the "hold" mode.

SETTING GAIN AND OFFSET

Varying gain and offset for the AD9003 enhances performance of the unit and increases its flexibility in applications. One suggested method of obtaining approximately 5% variation in each is shown in Figure 2.

The AD9003 can be operated in a unipolar mode or a bipolar mode; strap options and adjustments of the external controls shown in Figure 2 determine which is used. When calibrating for either mode, apply an encode command at the word rate frequency of the system to Pin 20.

Connect a precision voltage source between the ANALOG INPUT connection shown in Figure 2 and ground. Set its output for the voltage shown in Table I as being equal to −FS + 1/2LSB for the input range to be used (−0.6mV for unipolar operation and +2.4994V for bipolar operation if using the full-scale 5V input range of the AD9003).

Adjust the OFFSET control for a digital output which "dithers" between 0000 0000 0000 and 0000 0000 0001.

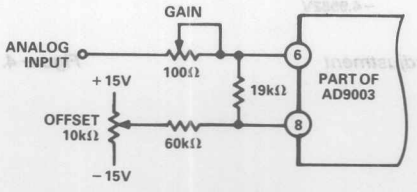


Figure 2. AD9003 Gain and Offset

To set gain, readjust the output of the voltage reference source to the value shown in Table I as being equal to +FS −1-1/2LSB for the input range to be used (−4.9982V for unipolar operation; −2.4982V for bipolar operation with the full-scale 5V range).

Adjust the GAIN control for a digital output which "dithers" between 1111 1111 1110 and 1111 1111 1111.

Figures 3 and 4 provide additional information about the switching points of the LSB when adjusting for either unipolar or bipolar operation using the full-scale 5V input.

AD9003 DRIVER CIRCUIT WITH CLAMP

The choice of the driver amplifier for an A/D can have significant effect on the performance of the converter. The ADI AD9610 Op Amp is the recommended choice for operation with the AD9003. This amplifier has extremely fast settling time and low distortion; these are especially important as the selected word rate frequency approaches the Nyquist limit.

In some applications, the analog input signals to be digitized may be outside the 5V range of the AD9003 converter, which can detract from the performance of the device by driving it into saturation.

At input frequencies greater than 50kHz, overloads larger than approximately 25% will saturate the front-end circuits of the internal track-and-hold. When the overload is removed, the T/H may cause erroneous codes to be generated at the output. Figure 5 shows a suggested circuit to avoid this.

Table I.

For UNIPOLAR Input	Apply Reference	And Adjust	For "Dither" Between	For BIPOLAR Input	Apply Reference	And Adjust	For "Dither" Between
0 to −5V	−0.6mV	OFFSET	0000 0000 0000 and 0000 0000 0001	0.00	0.00	OFFSET	0111 1111 1111 and 1000 0000 0000
0 to −5V	−4.9982V	GAIN	1111 1111 1110 and 1111 1111 1111	±2.5V	−2.4982V	GAIN	1111 1111 1110 and 1111 1111 1111

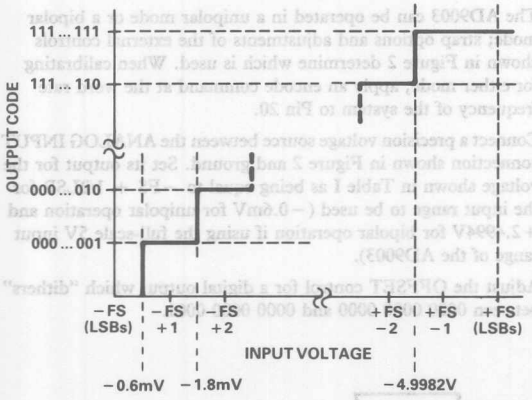


Figure 3. AD9003 Unipolar Adjustment

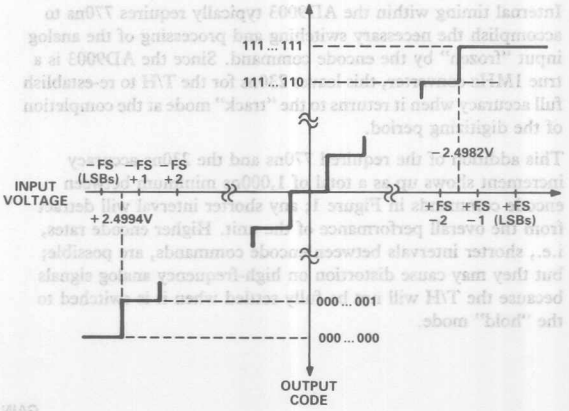


Figure 4. AD9003 Bipolar Adjustment

In this diagram, the value of the feed forward resistor R_{FF} is calculated on the basis of the equation:

$$R_{FF} = |\text{Desired Full-Scale Bipolar Voltage}| \times 500$$

The circuit eliminates saturating the internal T/H of the AD9003. Using an Analog Devices AD9610 ahead of the converter allows ±3x overdrives before the amplifier goes into saturation. Even in those instances in which the input signal exceeds the ±3x limit, the AD9610 comes out of saturation much more quickly than the input circuits of the converter would under the same circumstances.

Bipolar inputs to the AD9003 are held to a maximum of ±2.5V by the clamp circuits made up of 1N2810 Schottky diodes. The Analog Devices AD744 amplifiers and their associated circuits are for the purpose of clamping the Schottky diodes at the desired maximum input levels. As shown, +CLAMP ADJUST and −CLAMP ADJUST are set for +2.530V and −2.530V respectively.

These adjustment values take into account the gain and offset tolerances of the AD9003. If resistors with low temperature coefficients are selected, the clamp circuit will operate over the entire temperature range of the converter.

The bipolar circuit in Figure 5 can also be used for unipolar operation of the A/D with only minor changes. For this mode, the upper op amp (AD744 #1) and its associated reference circuits are removed; the upper 1N2810 clamp is connected, instead, to ground.

With these changes, the unipolar full-scale overdrive limit is 1.5x rather than the 3x of the bipolar connections; but this will prevent saturating the front end circuits of the AD9003. The value of R_{FF} in the unipolar circuit is based on:

$$R_{FF} = |\text{Desired Full-Scale Unipolar Voltage}| \times 250$$

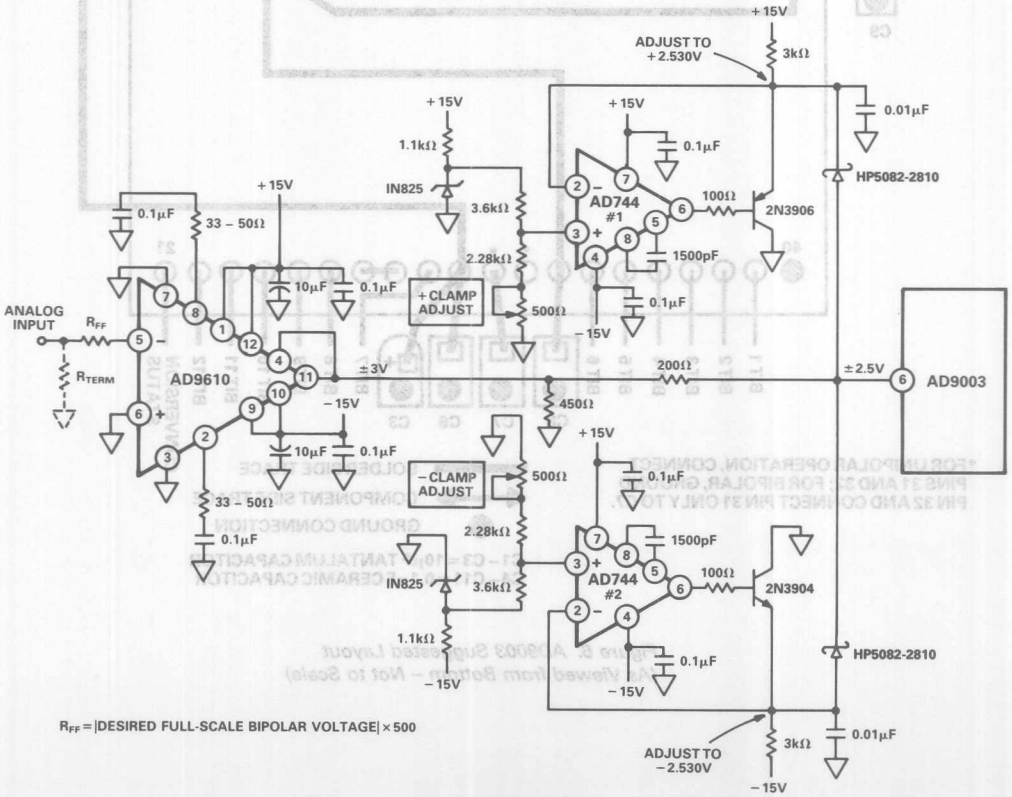


Figure 5. AD9003 Driver Circuit with Clamp

in laying out the circuit. It is critical to use the shortest possible lead lengths and circuit runs. Construct the circuit on a large, low-impedance ground plane containing the maximum possible power supplies; these should be connected as closely as possible to the supply pins. A suggested layout for the AD9003 when it is mounted on a printed circuit board is shown in Figure 6.

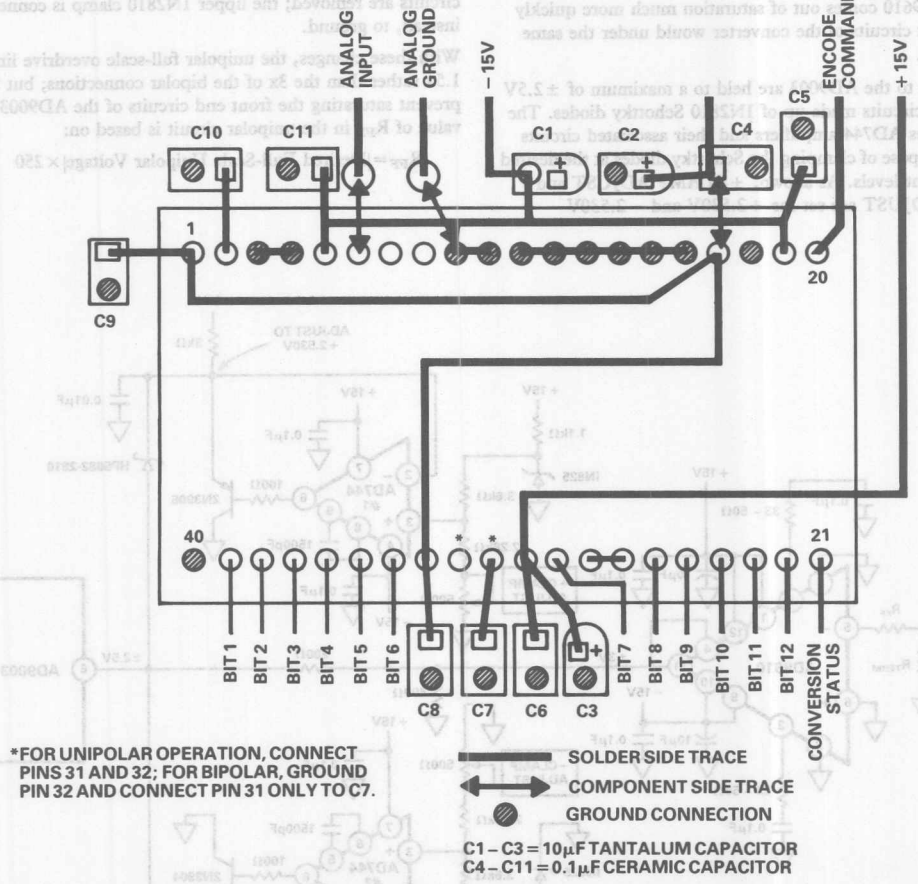


Figure 6. AD9003 Suggested Layout (As Viewed from Bottom – Not to Scale)

12-Bit, 10 MSPS A/D Converter

AD9005A

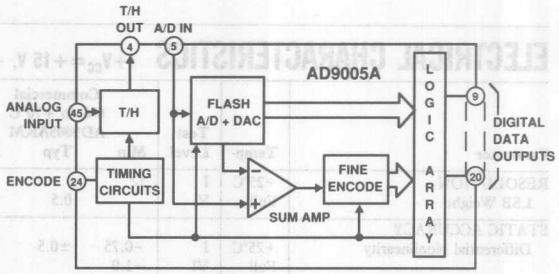
FEATURES

- Complete 12-Bit A/D Converter
- Includes Track and Hold, Reference, and Timing
- Bipolar Analog Input (±1.024 V)
- Up to 10 MSPS Sampling Rate
- Low Power Dissipation: 3.2 W
- Low Harmonic Distortion
- MIL-STD-883-Compliant Versions Available

APPLICATIONS

- Radar
- Digital Receivers
- Electro-Optics
- Medical Scanners
- Signal Intelligence
- Spectrum Analyzers

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9005A is a complete 12-bit A/D converter which includes on-board track-and-hold amplifier, voltage reference, and timing circuits. Featuring sampling rates from dc to 10 MSPS, the AD9005A uses a subranging converter architecture to achieve high speed and high resolution. Dynamic performance includes a SNR of 64 dB and harmonic distortion of −72 dBc with a 4.3 MHz analog input.

This unit replaces its predecessor, the AD9005. The AD9005A uses a higher level of integration than the earlier design to provide increased performance, better reliability, and reduced cost.

The AD9005ALM guarantees a minimum 76 dBc (@ 2.3 MHz) spurious free dynamic range (SFDR) for applications which have demanding ac performance requirements. All grades are fully tested for dynamic performance.

Critical to the performance of the AD9005A is the use of advanced bipolar integrated circuits, custom designed for this device and manufactured by Analog Devices. The AD9005A is TTL-compatible with offset binary outputs. It is available in a 46-pin hermetic metal DIP in two temperature ranges: 0°C to +70°C commercial range and −55°C to +125°C military range (case temperature).

The AD9005A is available in versions compliant with MIL-STD-883. Refer to the *Analog Devices Military Products Databook* or current AD9005A/883B data sheet for detailed specifications.

AD9005A—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_{CC}$) . . . . . +18 V
Negative Supply Voltage ($-V_{EE}$) . . . . . −18 V
Positive Supply Voltage ($+V_S$) . . . . . +6 V
Negative Supply Voltage ($-V_S$) . . . . . −6 V
Analog Input Voltage (Pin 45) . . . . . ±3.0 V dc
Digital Input Voltage . . . . . −0.5 V to $+V_S$
Digital Output Current . . . . . 4 mA

Operating Temperature Range (Case)
AD9005KM . . . . . 0°C to +70°C
AD9005TM . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature[2] . . . . . +175°C
Lead Soldering Temperature (10 sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS ($+V_{CC}$=+15 V, $-V_{EE}$=−15 V, $+V_S$=+5 V, $-V_S$=−5.2 V, unless otherwise stated)

			Commercial 0°C to +70°C AD9005AKM			Commercial 0°C to +70°C AD9005ALM			Military −55°C to +125°C AD9005ATM			
Parameter	Temp	Test Level	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
RESOLUTION	+25°C	I	12			12			12			Bits
LSB Weight	Full	V		0.5			0.5			0.5		mV
STATIC ACCURACY												
Differential Nonlinearity	+25°C	I	−0.75	±0.5	+0.75	−0.75	±0.5	+0.75	−0.75	±0.5	+0.75	LSB
	Full	VI	−1.0		+1.5	−1.0		+1.5	−1.0		+1.5	LSB
Integral Nonlinearity	+25°C	I		±1.0	±1.25		±1.0	±1.25		±1.0	±1.25	LSB
	Full	IV			±2.25			±2.25			±2.25	LSB
No Missing Codes	Full	VI		GUARANTEED			GUARANTEED			GUARANTEED		
Gain Error	+25°C	I		±0.5	±1.0		±0.5	±1.0		±0.5	±1.0	% FS
	Full	VI			±2.0			±2.0			±2.0	% FS
Offset Error	+25°C	I		±4	±15		±4	±15		±4	±15	mV
	Full	VI			±30			±40			±40	mV
ANALOG INPUT												
Input Voltage Range	Full	V		±1.024			±1.024			±1.024		V p–p
Input Resistance	Full	VI	950	1000	1050	950	1000	1050	950	1000	1050	Ω
Input Capacitance	+25°C	V		5			5			5		pF
Large Signal Input Bandwidth[3]	Full	V		38			38			38		MHz
DYNAMIC CHARACTERISTICS[5]												
Maximum Conversion Rate	Full	I	10			10			10			MSPS
Output Data Delay[6, 9] (t_{PD})	+25°C	V		90			90			90		ns
Aperture Delay (t_A)	+25°C	V		5			5			5		ns
Aperture Uncertainty	+25°C	IV		10	20		10	20		10	20	ps rms
Transient Response (to ±1 LSB)[7]	+25°C	IV			120			120			120	ns
Overvoltage Recovery Time[8] (to ±1 LSB)	+25°C	IV			250			250			250	ns
Harmonic Distortion[10, 4]												
F_{IN} = 540 kHz	+25°C	IV	−73	−78		−79	−83		−73	−78		dBc
F_{IN} = 2.3 MHz	+25°C	I	−68	−72		−76	−80		−68	−72		dBc
	Full	VI	−67			−75			−66			dBc
F_{IN} = 4.3 MHz	+25°C	I	−66	−72		−68	−75		−66	−72		dBc
	Full	VI	−65			−67			−63			dBc
Signal to Noise Ratio[11, 4]												
F_{IN} = 540 kHz	+25°C	IV	65	67		66	68		65	67		dB
F_{IN} = 2.3 MHz	+25°C	I	63	65		65	66		63	65		dB
	Full	VI	63			64			60			dB
F_{IN} = 4.3 MHz	+25°C	I	62	64		63	65		62	64		dB
	Full	VI	61			62			60			dB
Two-Tone Intermodulation Distortion[12]												
F_{IN} = 2.2 MHz + 2.3 MHz	+25°C	V		−75			−76			−75		dBc
ENCODE INPUT[14]												
Logic "1" Voltage	Full	IV	2.0			2.0			2.0			V
Logic "0" Voltage	Full	IV			0.8			0.8			0.8	V
Logic "1" Current	Full	I			150			150			150	μA
Logic "0" Current	Full	I			150			150			150	μA
Input Capacitance	+25°C	V		5			5			5		pF
Encode Pulse Width (High)	+25°C	IV	25			25			25			ns
DIGITAL OUTPUTS												
Logic "1" Voltage (2 mA Source)	Full	I	2.4			2.4			2.4			V
Logic "0" Voltage (4 mA Sink)	Full	I			0.4			0.4			0.4	V
Logic Coding	Full	IV		Offset Binary			Offset Binary			Offset Binary		

Parameter	Temp	Test Level	Commercial 0°C to +70°C AD9005AKM Min	Typ	Max	Commercial 0°C to +70°C AD9005ALM Min	Typ	Max	Military −55°C to +125°C AD9005ATM Min	Typ	Max	Units
POWER SUPPLY												
Supply Voltage $+V_{CC}$	Full	VI	+14.25	+15.0	+15.75	+14.25	+15.0	+15.75	+14.25	+15.0	+15.75	V
Supply Current $+V_{CC}$	Full	VI		15	25		15	25		15	25	mA
Supply Voltage $-V_{EE}$	Full	VI	−14.25	−15.0	−15.75	−14.25	−15.0	−15.75	−14.25	−15.0	−15.75	V
Supply Current $-V_{EE}$	Full	VI		30	55		30	55		30	55	mA
Supply Voltage $+V_S$	Full	VI	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
Supply Current Analog $+V_S$	Full	VI		180	210		180	210		180	210	mA
Supply Current Digital $+V_S$	Full	VI		43	60		43	60		43	60	mA
Supply Voltage $-V_S$	Full	VI	−4.95	−5.2	−5.45	−4.95	−5.2	−5.45	−4.95	−5.2	−5.45	V
Supply Current Analog $-V_S$	Full	VI		210	250		210	250		210	250	mA
Supply Current Digital $-V_S$	Full	VI		65	100		65	100		65	100	mA
Nominal Power Dissipation	Full	VI		3.2	4.0		3.2	4.0		3.2	4.0	W
PSRR[13, 15]	+25°C	I		0.01	0.02		0.01	0.02		0.01	0.02	%/%

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute rating conditions for extended periods of time may affect device reliability.

[2]Maximum junction temperature should not be allowed to exceed +175°C. Hybrid thermal model:

$t_{JUNCTION} = t_{AMBIENT} + P_{DISSIPATION} \times (\theta_{CA}) + (T_S - T_C)$ max

where $(T_S - T_C)$ max = 10°C

46 Pin metal DIP: θ_{CA} = 14°C/W in still air;

θ_{CA} = 6°C/W with 500 LFPM air flow

[3]Determined by 3 dB reduction in reconstructed output.

[4]Input at 1 dB below full scale.

[5]Measured at 10 MHz encode rate.

[6]Measured from ENCODE in to data out for LSB only.

[7]For full-scale step input; 12-bit accuracy is attained in the specified time.

[8]Recovers to 12-bit accuracy in specified time following 200% full-scale input voltage.

[9]Excludes pipeline delay of two clock cycles (see timing diagram).

[10]Worst case spurious in-band signal relative to input level.

[11]RMS signal to RMS noise, including harmonics.

[12]Worst case spurious in-band signal relative to level of input tones, which are both −7 dB below full scale.

[13]Sensitivity of full-scale gain error with respect to power supply variation within supply Min/Max limits.

[14]ENCODE signal rise and fall times should be less than 5 ns for normal operation. Transition from "0" to "1" initiates conversion.

[15]PSRR is tested over given voltage range.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

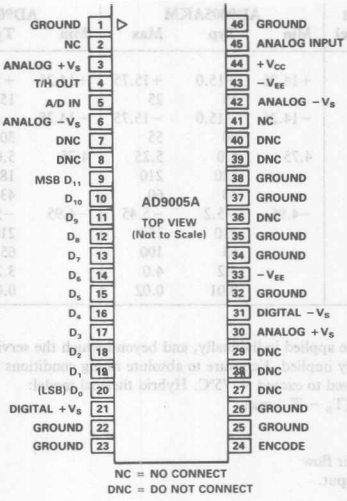
II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Periodically sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for military temperature devices. Guaranteed, not tested, for commercial temperature range



AD9005A PIN DESCRIPTIONS

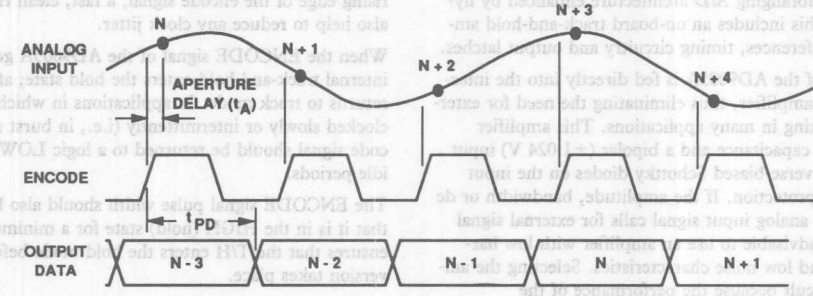
Pin	Name	Description
1	GROUND	Circuit ground. All grounds should be connected together near the AD9005A.
2	NC	Not internally connected.
3	ANALOG $+V_S$	Positive analog supply pin. Nominally +5 V dc.
4	T/H OUT	Output of internal track-and-hold amplifier. Connect to Pin 5 for normal operation.
5	A/D IN	Input to internal A/D encoder. Connect to Pin 4 for normal operation.
6	ANALOG $-V_S$	Negative analog supply pin. Nominally −5.2 V dc.
7, 8	DNC	Do not connect. Internal test point.
9	D_{11} (MSB)	Most significant bit of digital output data.
10–19	D_1–D_{10}	Digital data outputs.
20	D_0 (LSB)	Least significant bit of digital output data.

OUTPUT CODING

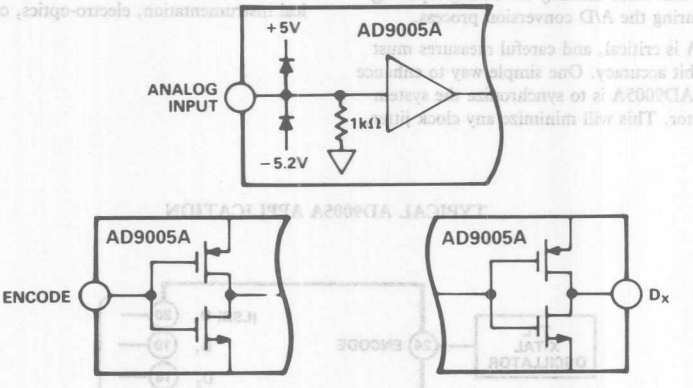
ANALOG INPUT	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
≥+1.024V	1	1	1	1	1	1	1	1	1	1	1	1
≤−1.024V	0	0	0	0	0	0	0	0	0	0	0	0

21	DIGITAL $+V_S$	Positive digital supply pin. Nominally +5 V dc.
22, 23	GROUND	Circuit ground. All grounds should be connected together near the AD9005A.
24	ENCODE	Convert command. TTL compatible, rising edge triggered.
25, 26	GROUND	Circuit ground. All grounds should be connected together near the AD9005A.
27–29	DNC	Do not connect. Internal test point.
30	ANALOG $+V_S$	Positive analog supply pin. Nominally +5 V dc.
31	DIGITAL $-V_S$	Negative digital supply pin. Nominally −5.2 V dc.
32	GROUND	Circuit ground. All grounds should be connected together near the AD9005A.
33	$-V_{EE}$	Negative analog supply pin. Nominally −15 V dc.
34, 35	GROUND	Circuit ground. All grounds should be connected together near the AD9005A.
36	DNC	Do not connect. Internal test point.
37, 38	GROUND	Circuit ground. All grounds should be connected together near the AD9005A.
39, 40	DNC	Do not connect. Internal test point.
41	NC	Not internally connected.
42	ANALOG $-V_S$	Negative analog supply pin. Nominally −5.2 V dc.
43	$-V_{EE}$	Negative analog supply pin. Nominally −15 V dc.
44	$+V_{CC}$	Positive analog supply pin. Nominally +15 V dc.
45	ANALOG INPUT	Analog input. Full scale of ±1.024 V.
46	GROUND	Circuit ground. All grounds should be connected together near the AD9005A.

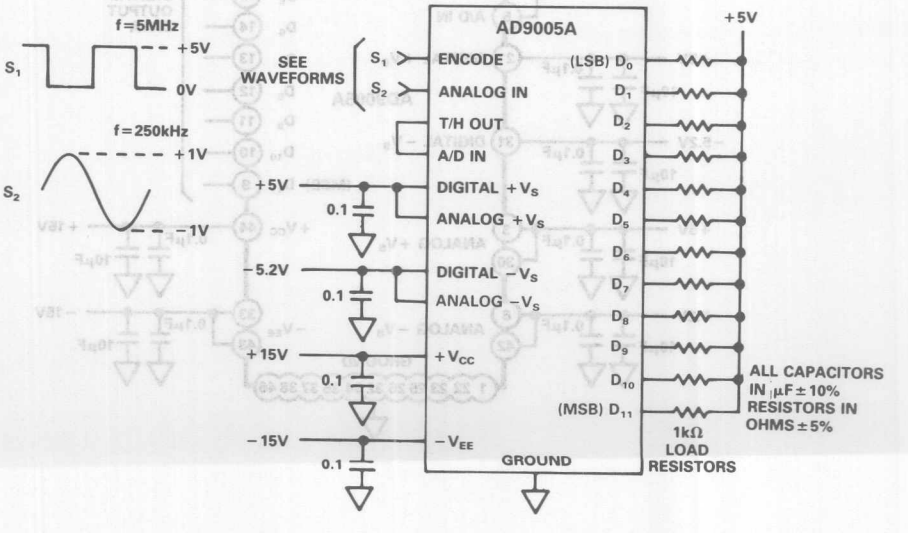
TIMING DIAGRAM



EQUIVALENT INPUT/OUTPUT CIRCUITS



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

The AD9005A is a complete analog-to-digital converter. The AD9005A uses a subranging A/D architecture enhanced by hybrid technology. This includes an on-board track-and-hold amplifier, on-board references, timing circuitry and output latches.

The analog input of the AD9005A is fed directly into the internal track-and-hold amplifier, thus eliminating the need for external signal conditioning in many applications. This amplifier provides low input capacitance and a bipolar (±1.024 V) input range. Normally reverse-biased Schottky diodes on the input provide overrange protection. If the amplitude, bandwidth or dc voltage level of the analog input signal calls for external signal conditioning, it is advisable to use an amplifier with low harmonic distortion and low noise characteristics. Selecting the amplifier may be difficult because the performance of the AD9005A will probably exceed the performance of most commercially available amplifiers. A notable exception is the AD9617, a wideband, low noise current feedback amplifier. It is important to remember that band limiting the analog input signal can avoid aliasing during the A/D conversion process.

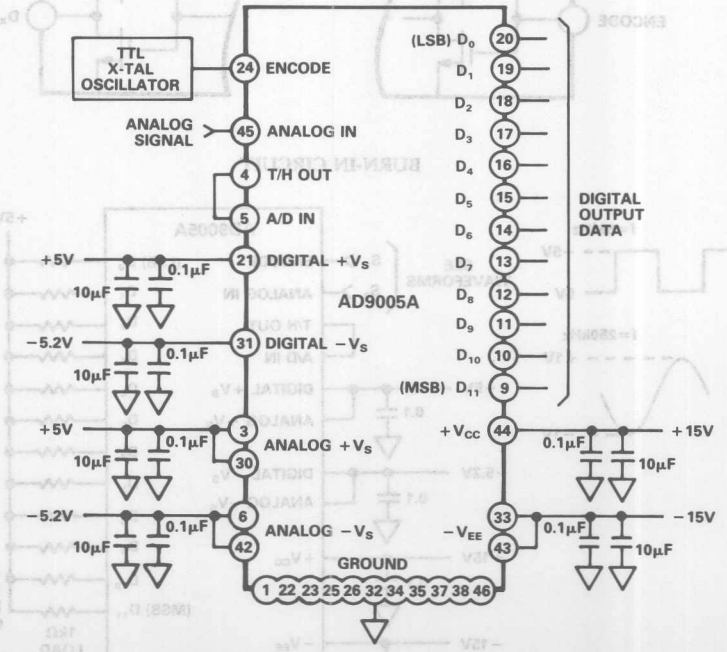
Timing in the AD9005A is critical, and careful measures must be taken to support 12-bit accuracy. One simple way to enhance the performance of the AD9005A is to synchronize the system clock to a crystal oscillator. This will minimize any clock jitter, a must for maintaining the spectral purity of analog signals near Nyquist limits. Because the conversion cycle begins with the rising edge of the encode signal, a fast, clean rising edge will also help to reduce any clock jitter.

When the ENCODE signal of the AD9005A goes HIGH, the internal track-and-hold enters the hold state; after 65 ns, it returns to track mode. In applications in which the AD9005A is clocked slowly or intermittently (i.e., in burst mode), the encode signal should be returned to a logic LOW state during the idle periods.

The ENCODE signal pulse width should also be adjusted so that it is in the HIGH (hold) state for a minimum of 25 ns. This ensures that the T/H enters the hold mode before the A/D conversion takes place.

The AD9005A has many appealing characteristics for 12-bit A/D converter applications. Its dynamic performance is state-of-the-art in hybrid technology. Typical applications include radar, missile guidance, digital oscilloscopes, waveform analyzers, medical instrumentation, electro-optics, communications and ESM.

TYPICAL AD9005A APPLICATION



Layout Information

The accuracy of a 12-bit converter, especially one with the dynamic performance level of the AD9005A, requires that designers pay careful attention to printed circuit board layouts. Analog signal paths should be impedance matched, with termination/load resistors at or near package connections. Analog signal paths should also be isolated from digital signal paths. Otherwise digital signals can be capacitively coupled into the analog section of the circuit, degrading the overall performance of the A/D converter.

Digital switching noise on power supplies can also degrade converter performance. Because of this noise (inherent with TTL logic), the digital power supplies of the AD9005A should be separated from the analog power supplies. In addition, each power supply should be capacitively decoupled to ground. To accomplish this, a single large value capacitor with a high resonant frequency (a 10 μF tantalum capacitor for example) should be used on each of the AD9005A's power supplies, at or near the package. In addition, a lower value capacitor with good high frequency characteristics (a 0.1 μF ceramic chip capacitor is recommended) should be connected to each power supply pin connection.

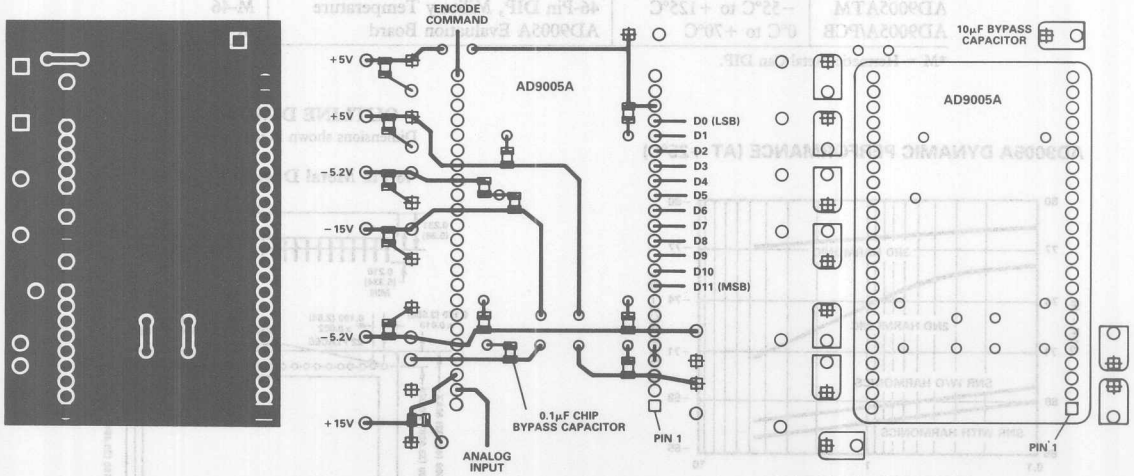
For applications in which only single +5 V and/or −5.2 V supplies are available, a ferrite bead, placed in series between the analog and digital power pins, can be used to isolate the digital noise from the analog circuits.

Noise on the circuit ground is often the limiting factor in A/D converter performance. Perhaps the most critical concerns of circuit layout are the ground connections. To reduce ground noise, a two-sided printed circuit board is recommended, the component side being reserved (as much as possible) for a single, low impedance ground plane. The other side should be used for all (possible) power and signal connections. Each of the ground connections of the AD9005A should be connected to the ground plane, and most of the area under the AD9005A should be part of this ground plane. The metal case of the AD9005A is connected to ground.

Operation of the AD9005A requires that Pin 4, the output of the internal track-and-hold, be connected to Pin 5, the input to the AD9005A's A/D converter circuitry. A suggested layout, showing this connection, is shown below.

A final suggestion regarding circuit layout concerns the use of sockets. Ideally, parts should be soldered into boards in final designs. If sockets must be used, individual pin sockets are recommended to avoid lead inductance and capacitive coupling between adjacent pins. Pin sockets are available from Amp, part #6−330808−0.

SUGGESTED LAYOUT

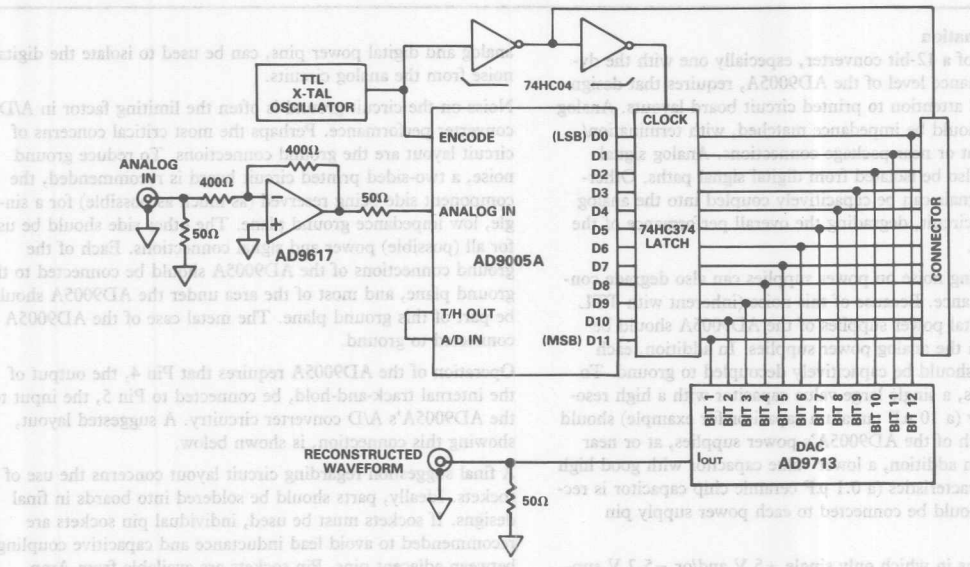


GND Plane Side (As Viewed from Top)

Solder Side (As Viewed from Top)

Component Mounting (As Viewed from Top)

EVALUATION CIRCUIT

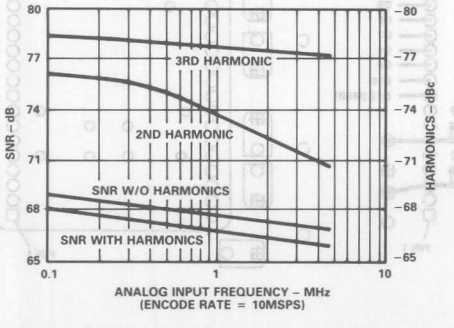


ORDERING GUIDE

Model	Temperature Range	Package	Package Option*
AD9005AKM	0°C to +70°C	46-Pin DIP, Commercial Temperature	M-46
AD9005ALM	0°C to +70°C	46-Pin DIP, Commercial Temperature	M-46
AD9005ATM	−55°C to +125°C	46-Pin DIP, Military Temperature	M-46
AD9005A/PCB	0°C to +70°C	AD9005A Evaluation Board	M-46

*M = Hermetic Metal Can DIP.

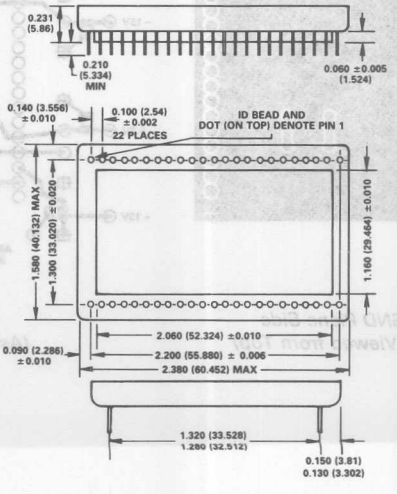
AD9005A DYNAMIC PERFORMANCE (AT +25°C)



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

46-Pin Metal Dual In-Line Can



High Speed 6-Bit A/D Converters

AD9006/AD9016

FEATURES

500MSPS Encode Rate
Very Low Input Capacitance: 8pF
30dB SNR @ 200MHz Analog Input
MIL-STD-883 Available
Bipolar Input Range (±1V)
Demultiplexed Outputs (AD9016)
MIL-STD-883-Compliant Versions Available

APPLICATIONS

Radar Warning Receivers
Electronic Countermeasures
Transient Recorders
"Smart" Munitions
Digital Oscilloscopes

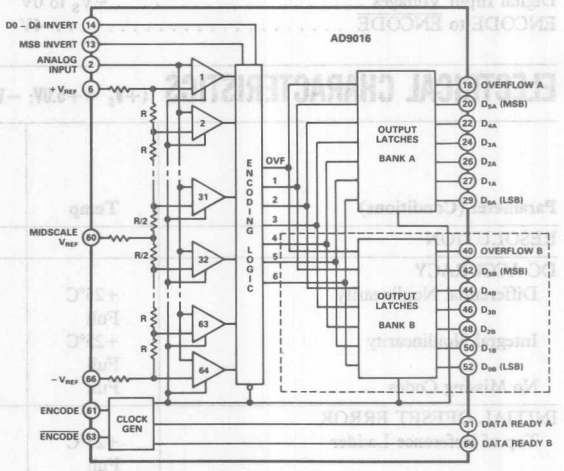
GENERAL DESCRIPTION

The AD9006 and AD9016 are 6-bit, ultrahigh speed analog-to-digital converters. Both are fabricated in an advanced bipolar process, assuring exceptionally wide analog input bandwidth, and encode rates up to 500MSPS. Functionally, the AD9006 and AD9016 use "flash" architecture; the outputs of 64 parallel comparator stages are decoded to drive a bank of ECL output latches.

The AD9006 features a bipolar analog input range (±1V). Output data is provided in a single 6-bit data bank; the data is ECL compatible and also includes complementary Data Ready signals and an overflow bit. ECL-level control pins allow the user to invert the MSB and/or LSBs. The AD9006 exhibits excellent SNR performance (30dB SNR @ 200MHz input), and requires less than two watts of power.

In the AD9016, the performance and features of the AD9006 are combined with on-board demultiplexing circuits. Output data of the AD9016 are demultiplexed to two 6-bit data banks, each of which includes a Data Ready signal and overflow bit.

FUNCTIONAL BLOCK DIAGRAM



(Dotted Area Not Included in AD9006)

The AD9006 and AD9016 are available as commercial temperature range devices: 0 to +70°C; and military temperature range devices: −55°C to +125°C. Both versions are offered in a ceramic 68-pin LCC, and a ceramic 68-pin leaded package.

The AD9006/AD9016 are available in versions compliant with MIL-STD-883. Refer to the *Analog Devices Military Products Databook* or current AD9006/AD9016/883B data sheet for detailed specifications

$+V_S$ to Ground . . . . . −0.5V dc to +7.0V dc
AGND to DGND . . . . . −0.5V dc to +0.5V dc
$-V_S$ to Ground . . . . . +0.5V dc to −6.0V dc
ANALOG IN, $+V_{REF}$–V_{REF} . . . . . −1.5V to +1.5V
MIDSCALE V_{REF}[2]
$+V_{REF}$ to $-V_{REF}$ 2.1V
MIDSCALE V_{REF} Current . . . . . ±4mA
Digital Input Voltages . . . . . $-V_S$ to 0V
ENCODE to $\overline{\text{ENCODE}}$ 4V
HYSTERESIS Input . . . . . $-V_S$ to +3V
ANALOG $-V_S$ to DIGITAL $-V_S$ . . . . . ±0.5V
Operating Temperature Range
AD9006/AD9016KE/KZ . . . . . 0 to +70°C
AD9006/AD9016TE/TZ/883 . . . . . −55°C to +125°C
Maximum Junction Temperature[3] . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5.0V; $-V_S$ = −5.2V; $+V_{REF}$ = +1V; $-V_{REF}$ = −1V, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9006/AD9016KE AD9006/AD9016KZ Min	Typ	Max	Units
RESOLUTION			6			Bits
DC ACCURACY						
Differential Nonlinearity	+25°C	I		0.2	0.25	LSB
	Full	VI		0.25	0.5	LSB
Integral Nonlinearity	+25°C	I		0.2	0.25	LSB
	Full	VI		0.25	0.5	LSB
No Missing Codes	Full	VI		GUARANTEED		
INITIAL OFFSET ERROR						
Top of Reference Ladder	+25°C	I		15	20	mV
	Full	VI			20	mV
Bottom of Reference Ladder	+25°C	I		14	20	mV
	Full	VI			20	mV
Offset Drift Coefficient	Full	V		20		µV/°C
ANALOG INPUT						
Input Voltage Range	Full	V		±1		V
Input Bias Current[4]	+25°C	I		60	100	µA
	Full	VI			130	µA
Input Resistance	+25°C	III	25	70		kΩ
Input Capacitance	+25°C	III		8	10	pF
Analog Bandwidth[5]	+25°C	V		550		MHz
REFERENCE INPUT						
Reference Ladder Resistance	+25°C	I	64	80	110	Ω
	Full	VI	50		135	Ω
Ladder Temperature Coefficient	Full	V		0.24		Ω/°C
Reference Input Bandwidth	Full	V		30		MHz
DYNAMIC PERFORMANCE[6]						
Conversion Rate	+25°C	I	470	500		MSPS
Aperture Delay (t_A)	+25°C	V		1.2		ns
Aperture Uncertainty (Jitter)	+25°C	V		3		ps
Output Delay (t_{OD})[7]	+25°C	I	2.7	3.6	4.4	ns
Output Rise Time	+25°C	I		1.3	1.5	ns
Output Fall Time	+25°C	I		1.3	1.5	ns
Output Time Skew[8]	+25°C	I		0.45	0.7	ns
Data Ready Output Delay (t_{DR})[9]						
AD9006	+25°C	I	2.7	3.2	4.4	ns
AD9016	+25°C	I	3	3.6	4.7	ns
Transient Response[10]	+25°C	V		1		ns
Overvoltage Recovery Time[11]	+25°C	V		1		ns

Parameter (Conditions)	Temp	Test Level	AD9006/AD9016KE AD9006/AD9016KZ Min	Typ	Max	Units
ENCODE INPUT						
Logic "1" Voltage	Full	VI	−1.1			V
Logic "0" Voltage	Full	VI			−1.5	V
Logic "1" Current	Full	VI			400	μA
Logic "0" Current	Full	VI			200	μA
Input Capacitance	+25°C	V		3		pF
Encode Pulse Width[12]	+25°C	I	1.0			ns
AC LINEARITY[13]						
Effective Number of Bits (ENOB)						
Analog Input @ 49MHz	+25°C	I	5.2	5.5		Bits
Analog Input @ 196MHz	+25°C	I	4.4	5.0		Bits
In-Band Harmonics						
Analog Input @ 9.3MHz	+25°C	I	42	48		dBc
Analog Input @ 49MHz	+25°C	I	38	44		dBc
Analog Input @ 92MHz	+25°C	I	33	36		dBc
Analog Input @ 145MHz	+25°C	I	33	36		dBc
Analog Input @ 196MHz	+25°C	I	31	36		dBc
Signal-to-Noise Ratio[14]						
(With Harmonics)						
Analog Input @ 9.3MHz	+25°C	I	34	37		dB
Analog Input @ 49MHz	+25°C	I	30	35		dB
Analog Input @ 92MHz	+25°C	I	30	34		dB
Analog Input @ 145MHz	+25°C	I	30	33		dB
Analog Input @ 196MHz	+25°C	I	29	32		dB
Signal-to-Noise Ratio[14]						
(Without Harmonics)						
Analog Input @ 9.3MHz	+25°C	I	36	37		dB
Analog Input @ 49MHz	+25°C	I	33	36		dB
Analog Input @ 92MHz	+25°C	I	33	36		dB
Analog Input @ 145MHz	+25°C	I	33	35		dB
Analog Input @ 196MHz	+25°C	I	31	34		dB
Two-Tone Intermodulation Distortion Rejection[15]	+25°C	V		50		dB
DIGITAL OUTPUTS[6]						
Logic "1" Voltage	Full	VI	−1.1			V
Logic "0" Voltage	Full	VI			−1.5	V
POWER SUPPLY (AD9006)						
Positive Supply Current	+25°C	I		25	29	mA
($+V_S$ = +5.0V)	Full	VI			30	mA
Negative Supply Current	+25°C	I		320	380	mA
($-V_S$ = −5.2V)	Full	VI			395	mA
Nominal Power Dissipation	+25°C	V		1.7		W
Reference Ladder Dissipation	+25°C	V		50		mW
Power Supply Rejection Ratio[16]	Full	VI		2	4	mV/V
POWER SUPPLY (AD9016)						
Positive Supply Current	+25°C	I		25	29	mA
($+V_S$ = +5.0V)	Full	VI			30	mA
Negative Supply Current	+25°C	I		375	420	mA
($-V_S$ = −5.2V)	Full	VI			450	mA
Nominal Power Dissipation	+25°C	V		2.0		W
Reference Ladder Dissipation	+25°C	V		50		mW
Power Supply Rejection Ratio[16]	Full	VI		2	4	mV/V

NOTES
[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]$+V_{REF} > -V_{REF}$ under all circumstances.
[3]Typical thermal impedances:
68-pin leaded ceramic chip carrier θ_{JA} = 31°C/W; θ_{JC} = 1.1°C/W.
68-pin ceramic LCC θ_{JA} =36°C/W; θ_{JC} = 2.6°C/W.
[4]Measured with analog input =0V.
[5]Measured with use of Fast Fourier Transform (FFT). See Definitions.
[6]Outputs terminated through 100Ω to −2.0V; C_L<4pF
[7]Measured from 50% point of leading edge of ENCODE command to −1.3V point of output data.
[8]Output time skew includes HIGH-to-LOW and LOW-to-HIGH transitions as well as bit-to-bit time skew differences.
[9]Measured from 50% point of trailing edge of ENCODE command to 50% point of Data Ready pulse.
[10]For full scale step input, 6-bit accuracy is attained in the specified time.
[11]Recovers to 6-bit accuracy in specified time after 150% full scale input overvoltage.
[12]ENCODE command rise/fall times should be less than 2.5ns for normal operation.
[13]Measured at 400MSPS encode rate; input level 1.0dB below full scale (FS).
[14]RMS signal to rms noise with analog input signal of 1dB below full scale at specified frequency.
[15]Intermodulation measured with analog input frequencies of 60MHz and 70MHz at 7dB below full scale.
[16]Measured at $+V_S$ =+5.0V ±5% or $-V_S$ =−5.2V ±5%; specification shown is for worst case (see Definitions).
Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

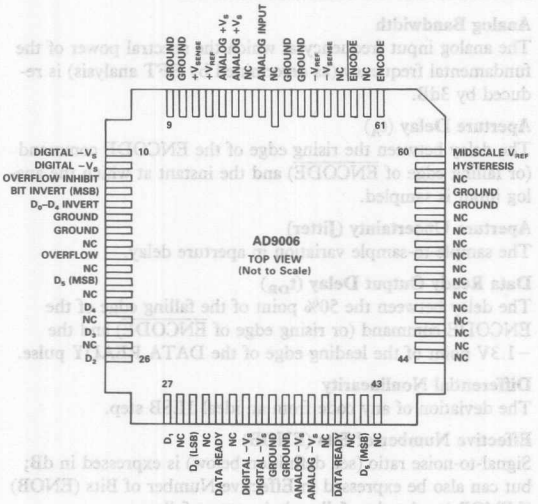
Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

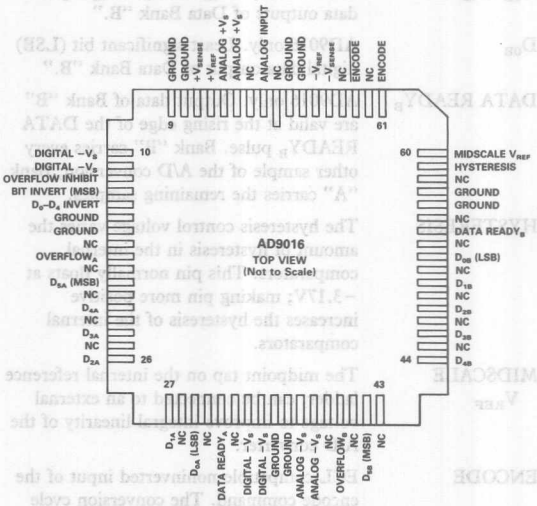
ORDERING GUIDE

Model[1]	Temperature	Description	Package Option[2]
AD9006KE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9006KZ	0 to +70°C	68-Pin Leaded Ceramic Chip Carrier	Z-68
AD9016KE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9016KZ	0 to +70°C	68-Pin Leaded Ceramic Chip Carrier	Z-68
AD9016KE/PCB	0 to +70°C	Evaluation Board; AD9016KE Installed	
AD9016/PCB	0 to +70°C	Evaluation Board; No Converter	

NOTES
[1]MIL-STD-883 versions available; contact factory.
[2]E = Ceramic Leadless Chip Carrier; Z = Ceramic Leaded Chip Carrier. For outline information see Package Information section.



AD9006 Pin Designations



AD9016 Pin Designations

AD9006/AD9016 PIN DESCRIPTIONS

NC — Not internally connected.

ANALOG IN — Analog input connection. Analog input is nominally between −1.0V and +1.0V.

ANALOG $+V_S$ — Positive supply pins; nominally +5.0V.

$+V_{REF}$ — The positive reference voltage applied to the internal resistor ladder.

$+V_{SENSE}$ — Voltage sense line to the most positive reference voltage of the resistor ladder. The sense line is intended for connection to a high impedance node and has limited current capability. It is intended to be used to null offset at the top of the reference ladder.

GROUND — Analog and digital ground connections for the AD9006/AD9016 units. For optimum performance, all grounds should be connected together and to a low impedance ground plane as close to the device as possible. [NOTE: On both the AD9006 and the AD9016, Pins 8, 9, 15, 16, 35, 36, 56 and 57 are digital ground (DGND); pins 67 and 68 are analog ground (AGND).]

OVERFLOW INHIBIT — Overflow bit control pin. OVERFLOW INHIBIT is connected to ground for normal operation (no overflow bit, nonreturn-to- zero operation). When overflow inhibit is connected to −5.2V or allowed to float, OVERFLOW = HIGH and output bits = LOW when the analog input voltage exceeds $+V_{SENSE}$).

BIT INVERT (MSB) — Most significant bit (D_{05}) control pin. BIT INVERT (MSB) is connected to ground for normal operation. When connected to −5.2V or allowed to float, MSB output is inverted.

D_0–D_4 INVERT — Bits D_0–D_4 control pin, connected to ground for normal operation. When connected to −5.2V or allowed to float, D_0–D_4 data outputs are inverted.

$OVERFLOW_A$ — AD9016 only. Overflow data output for Data Bank "A." Logic HIGH indicates the analog input is greater than $+V_{SENSE}$ when OVERFLOW INHIBIT pin is LOW (−5.2V).

D_{5A} — AD9016 only. Most significant bit (MSB) digital data output of Data Bank "A."

D_{1A}–D_{4A} — AD9016 only. D_{1A} through D_{4A} digital data outputs from Data Bank "A."

D_{0A} — AD9016 only. Least significant bit (LSB) digital data output of Data Bank "A."

$DATA\ READY_A$ — AD9016 only. Output Data of Bank "A" are valid at the rising edge of the $DATA\ READY_A$ pulse. Bank "A" carries every other sample of the A/D conversion; Bank "B" carries the remaining samples.

DIGITAL $-V_S$ — Negative digital supply pins, nominally −5.2V.

ANALOG $-V_S$ — Negative analog supply pins, nominally −5.2V.

$OVERFLOW_B$ — AD9016 only. Overflow data output for Data Bank "B." Logic HIGH indicates analog input is greater than $+V_{SENSE}$ when OVERFLOW INHIBIT pin is LOW (−5.2V).

D_{5B} — AD9016 only. Most significant bit (MSB) digital data output of Data Bank "B."

D_{0B}	AD9016 only. Least significant bit (LSB) digital data output of Data Bank "B."
DATA $READY_B$	AD9016 only. Output data of Bank "B" are valid at the rising edge of the DATA $READY_B$ pulse. Bank "B" carries every other sample of the A/D conversion; Bank "A" carries the remaining samples.
HYSTERESIS	The hysteresis control voltage varies the amount of hysteresis in the internal comparators. This pin normally floats at −3.17V; making pin more positive increases the hysteresis of the internal comparators.
MIDSCALE V_{REF}	The midpoint tap on the internal reference ladder; can be connected to an external voltage to improve integral linearity of the A/D converter.
ENCODE	ECL-compatible noninverted input of the encode command. The conversion cycle begins on the rising edge of the ENCODE signal.
$\overline{\text{ENCODE}}$	ECL-compatible inverted input of the encode command, used when a differential encode signal is used. $\overline{\text{ENCODE}}$ should be tied to a voltage corresponding to the midpoint of the encode signal when a single-ended encode signal is used.
$-V_{SENSE}$	Voltage sense line to the most negative reference voltage of the resistor ladder. The sense line is intended for connection to a high impedance node and has limited current capability. It is intended to be used to null offset at the bottom of the reference ladder.
$-V_{REF}$	The negative reference voltage applied to the internal resistor ladder.
D_0	AD9006 only. Least significant bit (LSB) of the output data.
D_1–D_4	AD9006 only. D_1 through D_4 digital data outputs.
D_5	AD9006 only. Most significant bit (MSB) of digital data output.
OVERFLOW	AD9006 only. Overflow data output. Logic HIGH indicates the analog input is greater than $+V_{SENSE}$ when OVERFLOW INHIBIT pin is LOW (−5.2V).
DATA READY	AD9006 only. Output data are valid at the rising edge of the DATA READY pulse.
$\overline{\text{DATA READY}}$	AD9006 only. Output data valid at the falling edge of the $\overline{\text{DATA READY}}$ pulse.

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3dB.

Aperture Delay (t_A)
The delay between the rising edge of the ENCODE command (or falling edge of $\overline{\text{ENCODE}}$) and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Data Ready Output Delay (t_{DR})
The delay between the 50% point of the falling edge of the ENCODE command (or rising edge of $\overline{\text{ENCODE}}$) and the −1.3V point of the leading edge of the DATA READY pulse.

Differential Nonlinearity
The deviation of any code from an ideal 1LSB step.

Effective Number of Bits (ENOB)
Signal-to-noise ratio (see definition below) is expressed in dB; but can also be expressed in Effective Number of Bits (ENOB) if ENOB is related to full scale inputs as follows:

$$ENOB = (SNR - 1.78)/6.02$$

ENOB is calculated with a sine wave curve fit method.

In-Band Harmonics
The rms value of the fundamental divided by the rms value of the worst of the first six harmonics.

Integral Nonlinearity
This specification (often called "linearity error") is the deviation of the transfer function from a reference line and is expressed in either % or ppm of full scale range, or in fractions of 1LSB. In the AD9006 and AD9016 devices, this spec is measured in fractions of 1LSB and uses a best-fit straight line determined by a least square curve fit.

Output Delay (t_{OD})
The delay between the 50% point of the rising edge of the ENCODE command (or falling edge of $\overline{\text{ENCODE}}$) and the −1.3V point of output data.

Output Time Skew
Bit-to-bit time variations among Bits D_0 to D_5 and the overflow bit. In the AD9006 and AD9016 specifications, time skew includes HIGH-to-LOW and LOW-to-HIGH transitions of the digital output bits.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 6-bit accuracy after an analog input overvoltage signal of 150% is reduced to the valid range of the converter.

Pipeline Delay
This is equal to one clock cycle and is the delay between the 50% points on the rising edges of two successive ENCODE commands (or falling edges of $\overline{\text{ENCODE}}$ commands).

Power Supply Rejection Ratio
The ratio of the change in power supply voltage to a corresponding change in input offset voltage. In the AD9006 and AD9016 units, $+V_S$ (+5V) or $-V_S$ (−5.2V) are within ±5% of their nominal values for this test. Value shown in SPECIFICATIONS is worst case.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude to the rms value of "noise", which is defined as the sum of all other spectral components, including harmonics but excluding dc, with an analog input signal 1dB below full scale.

Transient Response
The time required for the converter to achieve 6-bit accuracy when a full scale step function input is applied to the unit.

Two-Tone Intermodulation Distortion (IMD) Rejection
The ratio of the power of a two-tone signal to the power of the strongest third-order IMD signal.

RECOMMENDED OPERATING CONDITIONS

Parameter	Input Voltage		
	Min	Nominal	Max
$+V_S$	+4.75	+5.00	+5.25
$-V_S$	−5.46	−5.20	−4.94
$+V_{REF}$	$-V_{REF}$	+1.0	+1.1
$-V_{REF}$	−1.1	−1.0	$+V_{REF}$
ANALOG INPUT	−1.0		+1.0

THEORY OF OPERATION

Refer to the block diagram of the AD9016 A/D converter.

"Flash" architecture used in the AD9006 and AD9016 units makes it unnecessary to use a track-and-hold (T/H) ahead of the converter in many applications. The analog input signal is impressed across 64 parallel comparator stages.

Bias points of these comparators are established by the voltages applied to the reference ladder via $+V_{REF}$, $MIDSCALE_{REF}$ and $-V_{REF}$.

The outputs of the comparators are applied to the decoding logic; from here, the data are applied to output latches as six bits of digital data and an overflow bit. The overflow bit can be used to stack converters to obtain additional bits of resolution and can also be used as a "flag" for indicating positive out-of-range inputs.

Capturing output data at the (guaranteed) encode rates of 470MSPS of the AD9016 is simplified by virtue of using two Data Ready pulses. Output data words alternate between Bank A and Bank B; this allows clocking demultiplexed data from the AD9016 at half the converter's sample rate.

The Data Ready pulses track the propagation delay of the output data and relieve the need to build an external clock circuit for tracking prop delay over the full operating temperature range.

Demultiplexed ports connected to Bank A and Bank B allow the user to capture output data with 100K ECL logic even when the converter is operating at 470MSPS. The AD9016 introduces only one pipeline delay in the processing of these digital output data, thereby reducing the number of clock cycles required to obtain the digital representation of the analog input at the appropriate output port.

The analog input voltage range is determined by the user-supplied voltage references: $+V_{REF}$ and $-V_{REF}$. The references can be adjusted between −1V and +1V. In all cases, $+V_{REF}$ should be greater than $-V_{REF}$; and the differential voltage between the references should not exceed 2.1V. MIDSCALE V_{REF} can be used to improve the integral linearity of the converter.

Another attractive feature of the analog input characteristics of the AD9016 is its low input capacitance of 8pF. In many other flash converters, this value is three or four times larger, making them difficult to drive at high input frequencies.

For those applications in which a single output port is preferred, the recommended choice is the AD9006 A/D converter.

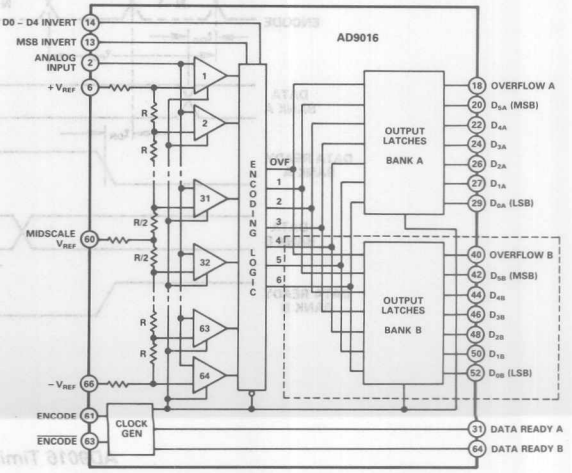
The AD9006 is identical to the AD9016 in performance specifications; it is best suited for systems in which demultiplexing is not performed immediately after the flash converter. As in the AD9016, the AD9006 produces Data Ready pulses on chip; these can be used to clock external latches.

There are two control pins for determining the format of the output data on the AD9006/AD9016. BIT INVERT (MSB) allows the user to invert the most significant bit ($D0_5$); and D_0–D_4 INVERT allows the five least significant bits to be inverted. The AD9006/AD9016 Truth Table elsewhere in the data sheet provides the necessary information to select among binary, inverted binary, twos complement and inverted twos complement coding schemes.

The OVERFLOW INHIBIT pin controls the overflow bit (called out as OVERFLOW BIT in the AD9006, and $OVERFLOW_A$ and $OVERFLOW_B$ in the AD9016). In normal operation, the OVERFLOW INHIBIT is connected to −5.2V, and OVERFLOW will be a digital HIGH whenever the analog input voltage exceeds the most positive comparator reference ($+V_{SENSE}$). The digital outputs (D_0– D_5) will be LOW, i.e., returned-to-zero operation.

This feature means two AD9006 devices can be cascaded or "stacked" to obtain seven-bit operation, as shown in the diagram below.

Connecting OVERFLOW INHIBIT to ground forces the overflow bit to remain low and disables the return-to-zero operation.

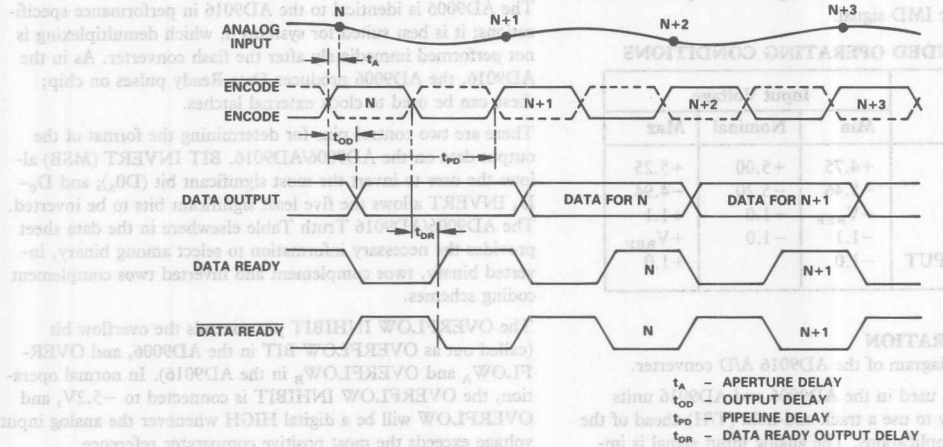


AD9016 Functional Block Diagram
(Dotted Area Not Included in AD9006)

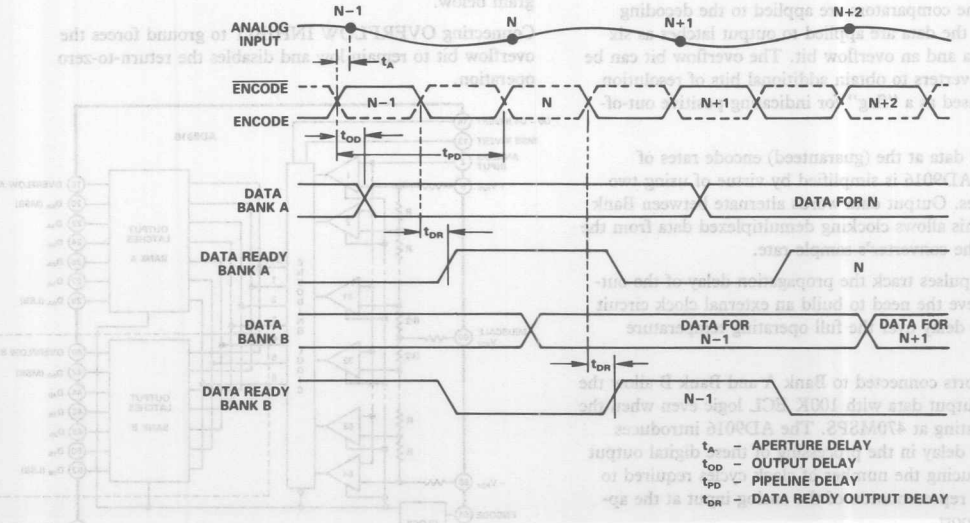
Timing for the AD9006 and AD9016 is shown in their respective timing diagrams. In both illustrations, the complementary encode command is shown in dashed lines.

The DATA READY and $\overline{\text{DATA READY}}$ pulses of the AD9006 correspond, respectively, to the DATA READY BANK A and DATA READY BANK B pulses of the AD9016. As shown in the SPECIFICATIONS table, Data Ready Output Delay is slightly different in the two units: 3.2ns in the AD9006 and 3.6ns in the AD9016.

Availability and timing of a DATA READY pulse help in retrieving data from either the AD9006 or the AD9016. When setting system timing, the user simply takes into account the (single) pipeline delay and the Data Ready Output Delay (3.2ns in the AD9006; 3.6ns in the AD9016) and uses the next DATA READY (or $\overline{\text{DATA READY}}$ in the AD9006) to strobe the desired output into external circuits.



AD9006 Timing Diagram



AD9016 Timing Diagram

APPLYING THE AD9006/AD9016

Setting Reference Levels

The AD9006/AD9016 requires that the user provide two voltage references: $+V_{REF}$ and $-V_{REF}$. These two voltages are applied across the internal resistor ladder (nominally 80Ω) and determine the analog input range of the converter.

Care should be taken to assure that these references are driven from stable, low impedance sources. Reference connections should be capacitively coupled to ground to reduce interference generated by noise and/or digital switching.

Resistance between the reference connections and the point at which the first comparator threshold is connected causes offset errors. These errors, called "top and bottom of the ladder offsets," can be nulled out using the $+V_{SENSE}$ and $-V_{SENSE}$ connections. These sense lines are intended for connection only to high impedance (low current) nodes such as the input of an op amp.

Applying a voltage greater than 2.1V across the internal resistor ladder will cause current densities to exceed rated values and may cause permanent damage to the AD9006/AD9016.The amount of current available at the reference connections must be limited.

One method of nulling the offset errors is shown in Figure 1.

The Analog Devices AD1403 voltage reference supplies a stable 2.5V reference for the circuit, and R_{LIMIT} determines the range over which the reference can be adjusted. R_1 adjusts the voltage at the top of the internal reference ladder through the AD642/2N3904 combination. Feedback from the $+V_{SENSE}$ line causes the op amp to compensate for offset which appears at the top comparator threshold. The transistor limits the amount of current drawn directly from the op amp; resistors at the base and emitter of the transistor stabilize its operation.

Voltage at the bottom of the reference ladder is controlled in essentially the same way, using R_2 to adjust the reference ladder voltage; and using feedback from the $-V_{SENSE}$ connection to null any offset between the reference and the threshold of the bottom comparator.

The midpoint of the comparator reference ladder (MIDSCALE V_{REF}) is shown tied to ground in Figure 1. This allows the user to adjust the voltage reference for minimum integral nonlinearity. This feature becomes important in applications with reduced analog input ranges because integral nonlinearity increases under these conditions.

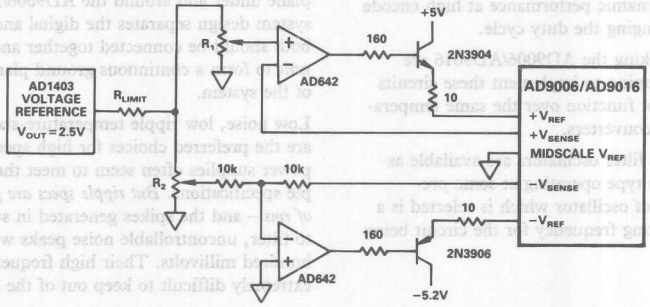


Figure 1. Reference Circuit

Driving the Analog Input

Careful design and layout of the AD9006/AD9016 have resulted in a typical input capacitance of 8pF (9.5pF max). This is low in comparison to most flash converters, but it is still a significant load at high input frequencies and must be taken into account when choosing a drive amplifier.

DC-coupled applications require the performance characteristics of a wide bandwidth, low distortion op amp such as the Analog Devices AD9611. AC-coupled applications at high frequencies may be better served by using a low distortion gain block for the driver.

Figure 2 illustrates possible connections for both approaches.

Regardless of which driving circuit is selected for the application, the overall dynamic performance of the amplifier is enhanced by inserting a small series resistor between the output of the amplifier and the analog input of the converter.

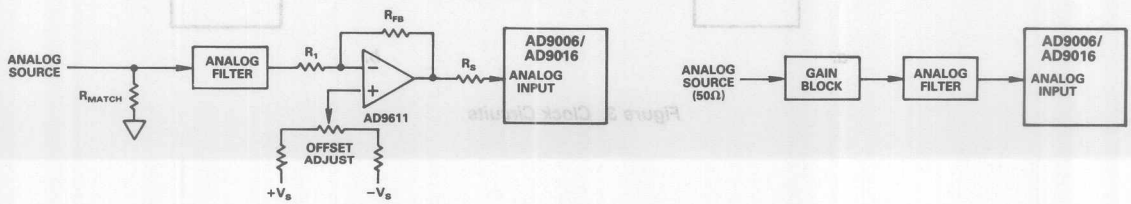


Figure 2. Analog Input Circuits

Clocking the Converter

The encode command circuits of the AD9006/AD9016 (ENCODE and $\overline{\text{ENCODE}}$) are designed to be driven by a differential ECL source.

A differential signal is recommended as the encode command to reduce jitter of the encode signal; increased jitter raises the noise floor of the converter. Full logic levels are preferred for triggering the clock circuits, but reduced levels can also be used. Caution should be exercised when using reduced-level encode commands because their slew rates will be decreased, which can raise the noise floor.

Refer again to the timing diagrams for the AD9006 and AD9016.

The rising edge of the ENCODE signal initiates the conversion process in the AD9006 unit. This same signal, delayed, becomes the DATA READY and complementary $\overline{\text{DATA READY}}$ pulses. Fast rise and fall times (<0.5ns) and "clean" edges are always required for encode commands, but are especially critical for high frequency analog signals.

In the AD9016, the leading edges of the DATA READY_A and DATA READY_B pulses are triggered by the trailing edge of an ENCODE command. Their trailing edges are triggered by the trailing edge of the next ENCODE command.

Although the AD9006/AD9016 is designed and tested to operate with a 50% duty cycle, the dynamic performance at high encode rates can be improved by changing the duty cycle.

Two possible methods of clocking the AD9006/AD9016 are shown in Figure 3. Users planning to implement these circuits need to be aware they may not function over the same temperature ranges possible with the converters.

Both ECL oscillators and saw filter oscillators are available as comercial products, with each type operating at some preselected frequency. The type of oscillator which is selected is a function of the desired operating frequency for the circuit being designed.

Layout and Power Supplies

Correct layout of high speed circuits is always critical, but is particularly important when both analog and digital signals are involved.

Analog signal paths should be kept as short as practical, and be properly terminated to avoid reflections and signal distortions. The analog input and voltage references should be kept away from digital signal paths; this reduces the possibility of capacitively coupling digital switching noise into the analog section of the circuit.

Digital signal paths should also be kept short, and digital run lengths should be matched because propagation delays through digital paths become significant at high data rates. Proper ECL terminations should be used at or near the packages containing successive gates.

Ideally, analog signal paths and digital signal paths should be routed as far away from one another as possible and should never closely parallel one another's paths. If they must cross, they should do so at right angles to avoid interference.

In any layout of high speed circuits, the layout of ground connections is the most important factor. To reduce noise and interference on the circuit ground, a double-sided copper-clad printed circuit board (PCB) is recommended. Every part of the board not used for components or conducting runs should be ground plane. Components are mounted on one side; the opposite side is used for power and signal connections.

It is especially important to retain the continuity of the ground plane under and around the AD9006/AD9016 converter. If the system design separates the digital and analog ground returns, both should be connected together and to ground close to the unit to form a continuous ground plane around the A/D section of the system.

Low noise, low ripple temperature-stable linear power supplies are the preferred choices for high speed circuits. Switching power supplies often seem to meet these criteria, including ripple specifications. *But ripple specs are generally expressed in terms of rms* – and the spikes generated in switchers can produce hard-to-filter, uncontrollable noise peaks with amplitudes of several hundred millivolts. Their high frequency components may be extremely difficult to keep out of the ground system.

If switching power supplies cannot be avoided for high speed designs, they should be *carefully* shielded and their outputs should be well filtered.

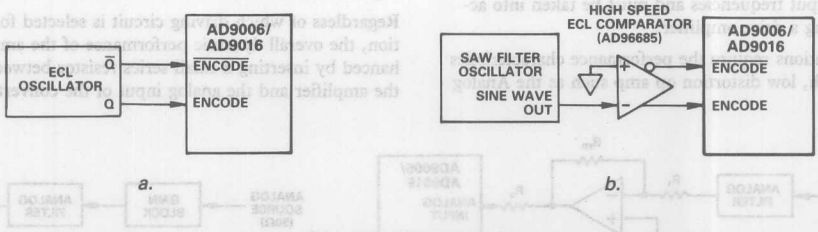


Figure 3. Clock Circuits

Every power supply line leading into a high speed PCB or data acquisition circuit must be carefully bypassed to its ground return to prevent noise from entering the circuit. Ceramic capacitors, ranging in value from 0.01μF to 0.1μF, should be used generously in the layout, mounted as closely as possible to the device or circuit being bypassed.

The capacitors which are used should have a high resonant frequency to insure they maintain their characteristics in the range of frequencies involved in the encoding process. Ceramic surface mount (chip) capacitors meet that requirement and are easily placed near the package connections.

At least one high quality tanatalum capacitor of 3μF– 20μF should be assigned to each power supply voltage, mounted as near as possible to the incoming power pins to minimize low frequency ripple.

Handling the AD9006/AD9016 Package

Several precautions have been included in the design of the AD9006/AD9016 converter to help reduce its sensitivity to electrostatic discharge (ESD). But the user should always use normal ESD precautions to help insure device reliability and avoid degrading the unit's performance.

Package options which are available include both leaded and leadless 68-pin ceramic chip carriers; these are shown in the data sheet as leaded ceramic chip carrier and leadless chip carrier (LC), respectively. Both of these packages have been specially designed to maintain the converter's high frequency parameters while operating over a standard military temperature range.

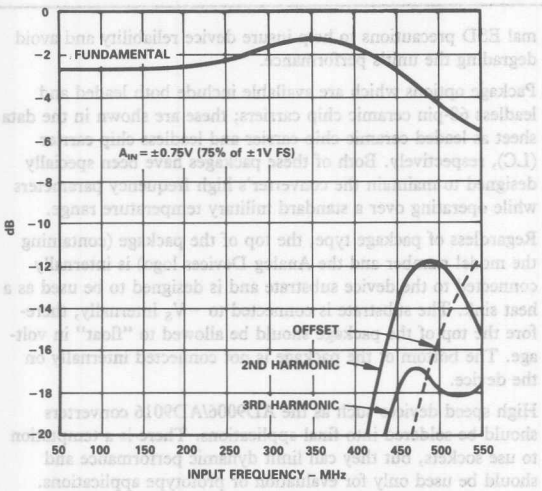
Regardless of package type, the top of the package (containing the model number and the Analog Devices logo) is internally connected to the device substrate and is designed to be used as a heat sink. The substrate is connected to $-V_S$ internally; therefore the top of the package should be allowed to "float" in voltage. The bottom of the package is not connected internally on the device.

High speed devices such as the AD9006/AD9016 converters should be soldered into final applications. There is a temptation to use sockets, but they can limit dynamic performance and should be used only for evaluation or prototype applications.

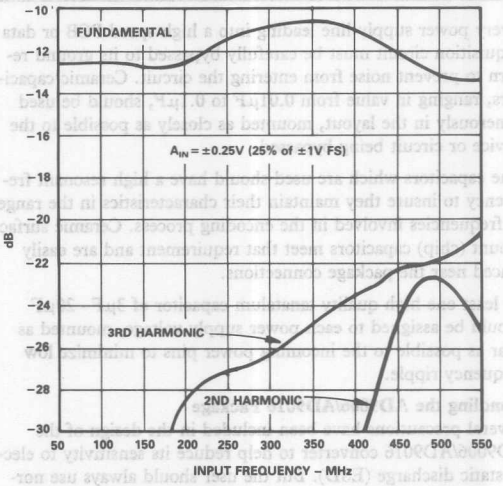
Step	Input Voltage (FS =±1.0V)	Binary		Offset Twos Complement	
		True	Inverted	True	Inverted
		MSB INVERT =1 D_0–D_4 INV =1	MSB INVERT =0 D_0–D_4 INV =0	MSB INVERT =0 D_0–D_4 INV =1	MSB INVERT =1 D_0–D_4 INV =0
00	−1.000	000000	111111	100000	011111
01	−0.968	000001	111110	100001	011110
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
31	−0.031	011111	100000	111111	000000
32	0.000	100000	011111	000000	111111
33	+0.031	100001	011110	000001	111110
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
62	+0.938	111110	000001	011110	100001
63	+0.969	111111	000000	011111	100000
63+	+1.000	(0)111111* (1)000000#	(0)000000* (1)111111#	(0)011111* (1)100000#	(0)100000* (1)011111#

*OVERFLOW INHIBIT ="1"; #OVERFLOW INHIBIT ="0."
The overflow bit is always 0 except where noted in parentheses ( ). MSB INVERT, D_0–D_4 INVERT and OVERFLOW INHIBIT are considered dc controls. They are tied to ground for logic "1" and $-V_S$ for logic "0"; their "trip point" occurs at approximately −1.3V.

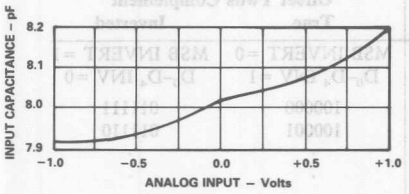
AD9006/AD9016 Truth Table



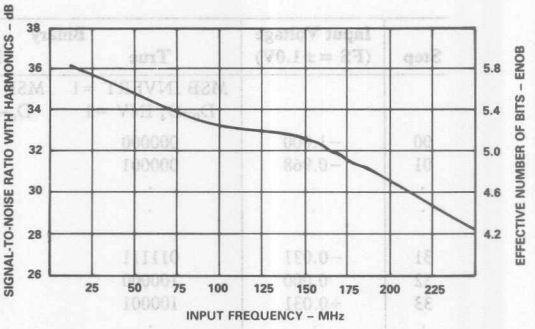
Harmonics vs. Input Frequency – Large Signal



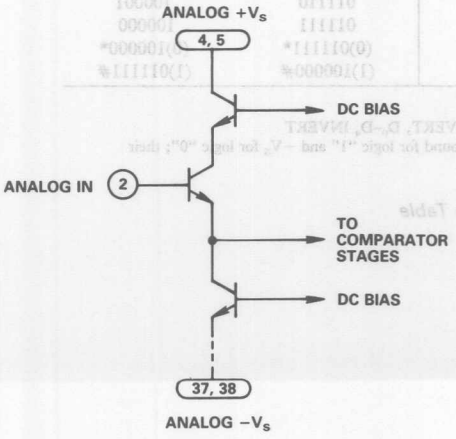
Harmonics vs. Input Frequency – Small Signal



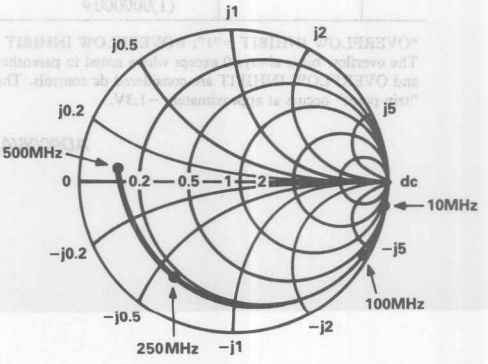
Input Capacitance vs. Input Voltage



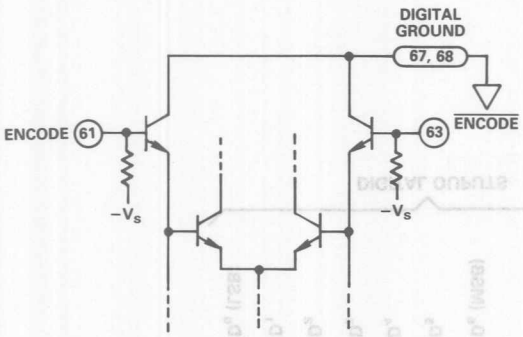
SNR and Effective Number of Bits (ENOB) vs. Input Frequency



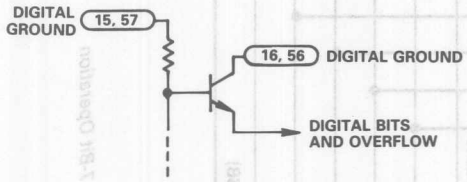
Equivalent Analog Input



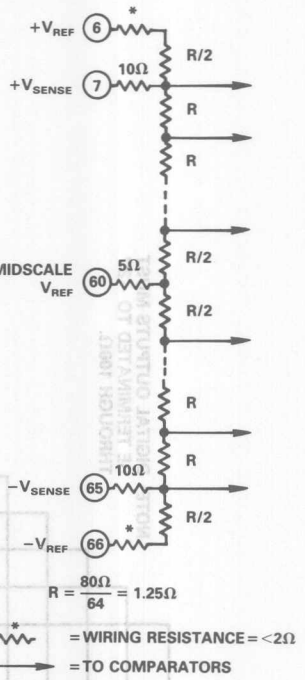
Normalized 50Ω Input Impedance vs. Input Frequency



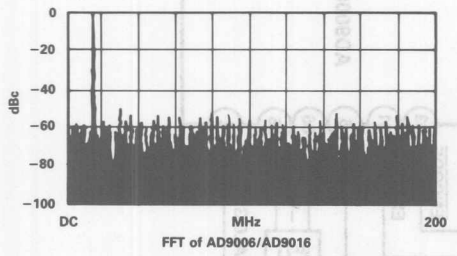
Encode and $\overline{Encode}$ Equivalent Circuits



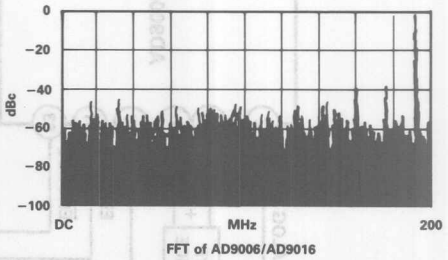
Equivalent Digital Outputs



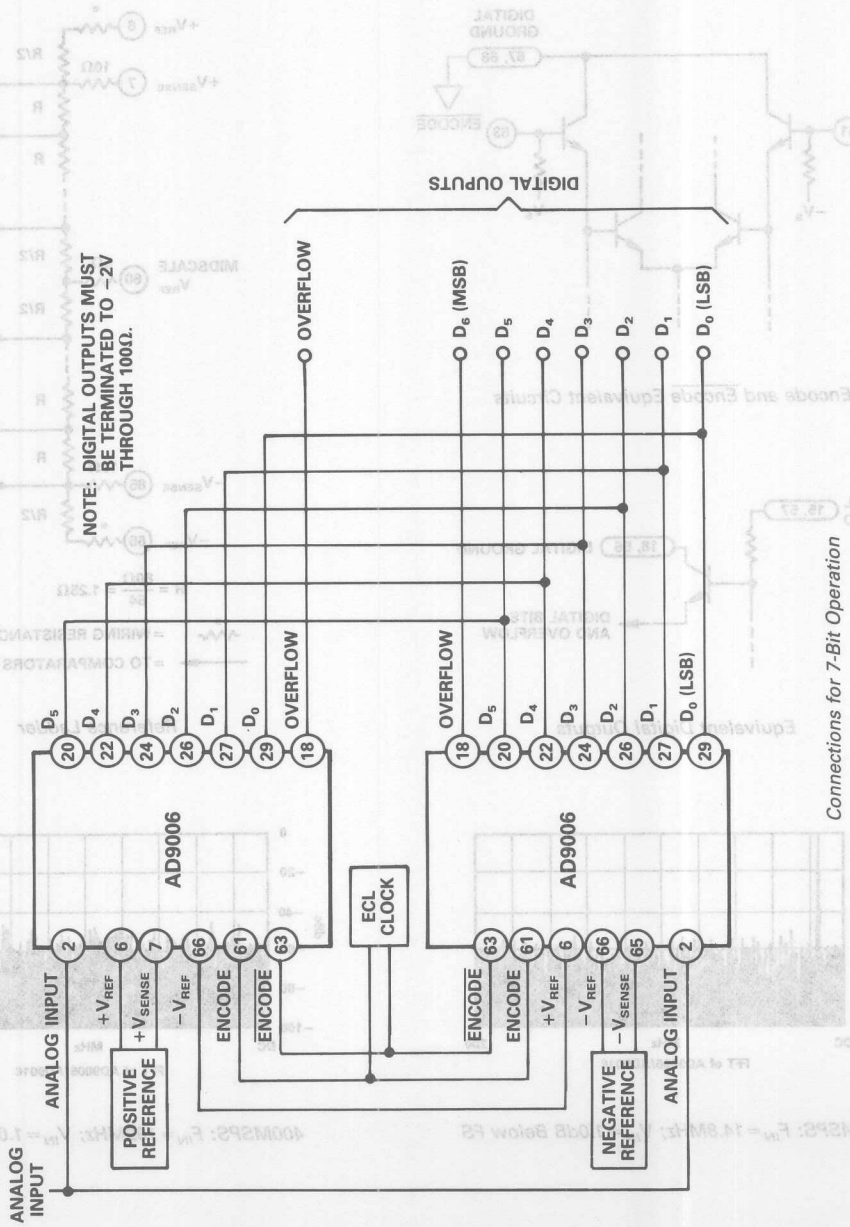
Reference Ladder



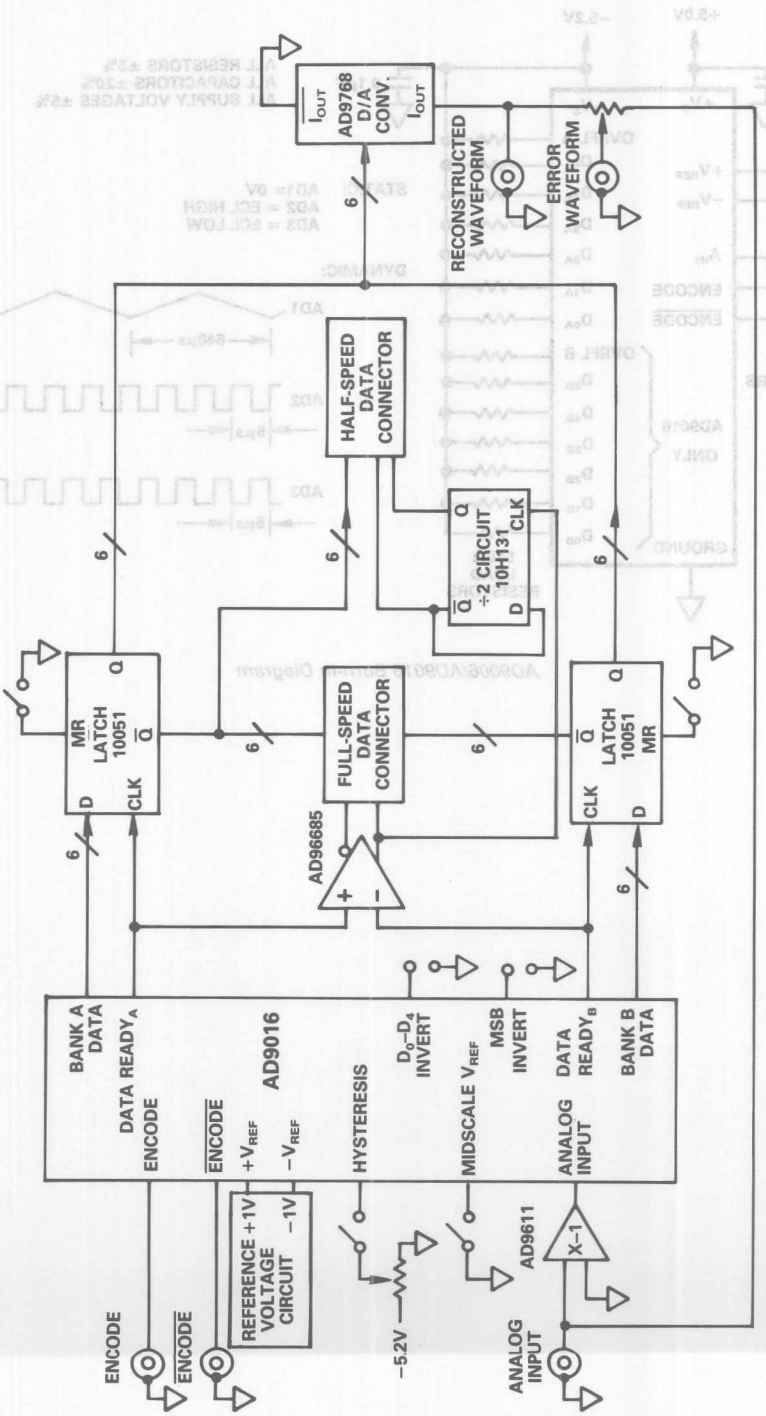
400MSPS: F_{IN} = 14.8MHz; V_{IN} = 1.0dB Below FS



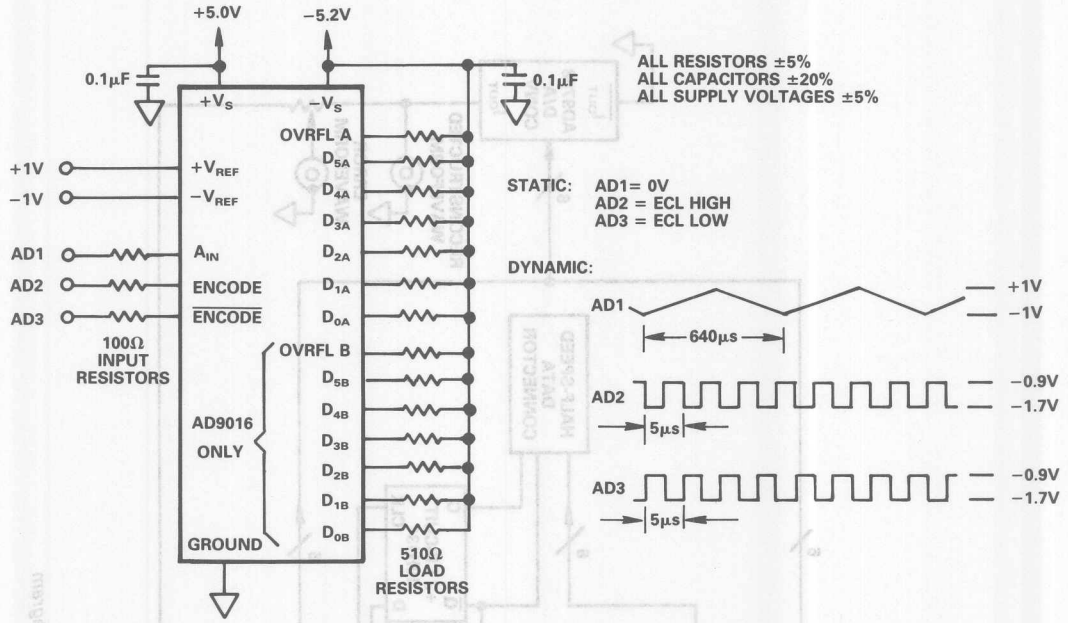
400MSPS: F_{IN} = 192MHz; V_{IN} = 1.0dB Below FS



Connections for 7-Bit Operation



AD9016/PCB Block Diagram

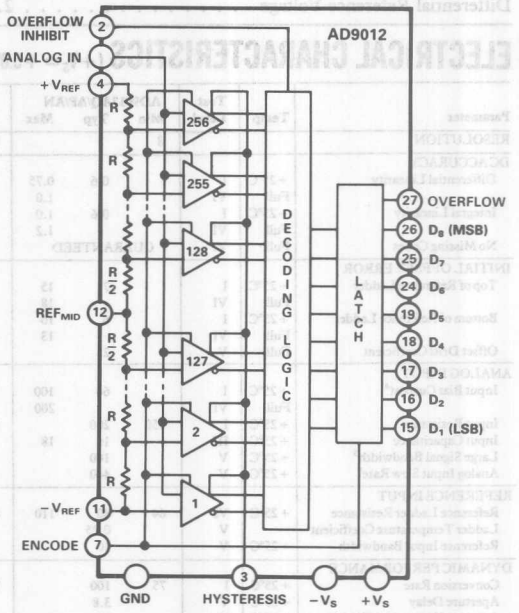


AD9006/AD9016 Burn-In Diagram

FEATURES
100MSPS Encode Rate
Very Low Input Capacitance – 16pF
Low Power – 1W
TTL Compatible Outputs
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Radar Guidance
Digital Oscilloscopes/ATE Equipment
Laser/Radar Warning Receivers
Digital Radio
Electronic Warfare (ECM, ECCM, ESM)
Communication/Signal Intelligence

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9012 is an 8-bit, ultrahigh speed, analog-to-digital converter. The AD9012 is fabricated in an advanced bipolar process, which allows operation at sampling rates up to 100 megasamples/second. Functionally, the AD9012 is comprised of 256 parallel comparator stages whose outputs are decoded to drive the TTL compatible output latches.

The exceptionally wide large signal analog input bandwidth of 160MHz is due to an innovative comparator design and very close attention to device layout considerations. The wide input bandwidth of the AD9012 allows very accurate acquisition of high speed pulse inputs without an external track-and-hold. The comparator output decoding scheme minimizes false codes, which is critical to high speed linearity.

The AD9012 is available in two grades, one with 0.5LSB linearity and one with 0.75LSB linearity. Both versions are offered in an industrial grade, −25°C to +85°C, packaged in a 28-pin DIP and a 28-pin PLCC. The military temperature range devices, −55°C to +125°C, are available in ceramic DIP and LCC packages and are compliant to MIL-STD-883 Class B.

The AD9012 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD9012/883B data sheet for detailed specifications.

AD9012—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) . . . . . +6V
Analog to Digital Supply Voltage Differential ($-V_S$) . . . 0.5V
Negative Supply Voltage ($-V_S$) . . . . . −6V
Analog Input Voltage . . . . . $-V_S$ to +0.5V
ENCODE Input Voltage . . . . . −0.5V to +5V
OVERFLOW INH Input Voltage . . . . . −5.2V to 0V
Reference Input Voltage ($+V_{REF} - V_{REF}$)[2] . −3.5V to +0.1V
Differential Reference Voltage 2.1V
Reference Midpoint Current . . . . . ±4mA
Digital Output Current 30mA
Operating Temperature Range
AD9012AQ/BQ/AP/AN/BP/BN . . . . . −25°C to +85°C
AD9012SE/SQ/TE/TQ . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature[3] . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS ($+V_S = +5.0V$; $-V_S = -5.2V$; Differential Reference Voltage = 2.0V, unless otherwise noted)

Parameter	Temp	Test Level	AD9012AQ/AP/AN Min	Typ	Max	AD9012BQ/BP/BN Min	Typ	Max	AD9012SQ/SE Min	Typ	Max	AD9012TQ/TE Min	Typ	Max	Units
RESOLUTION			8			8			8			8			Bits
DC ACCURACY															
Differential Linearity	+25°C	I		0.6	0.75		0.4	0.5		0.6	0.75		0.4	0.5	LSB
	Full	VI			1.0			0.75			1.0			0.75	LSB
Integral Linearity	+25°C	I		0.6	1.0		0.4	0.5		0.6	1.0		0.4	0.5	LSB
	Full	VI			1.2			1.2			1.2			1.2	LSB
No Missing Codes	Full	VI	GUARANTEED			GUARANTEED			GUARANTEED			GUARANTEED			
INITIAL OFFSET ERROR															
Top of Reference Ladder	+25°C	I		7	15		7	15		7	15		7	15	mV
	Full	VI			18			18			18			18	mV
Bottom of Reference Ladder	+25°C	I		6	10		6	10		6	10		6	10	mV
	Full	VI			13			13			13			13	mV
Offset Drift Coefficient	Full	V		25			25			25			25		µV/°C
ANALOG INPUT															
Input Bias Current[4]	+25°C	I		60	100		60	100		60	100		60	100	µA
	Full	VI			200			200			200			200	µA
Input Resistance	+25°C	I	150	200		150	200		150	200		150	200		kΩ
Input Capacitance	+25°C	III		16	18		16	18		16	18		16	18	pF
Large Signal Bandwidth[5]	+25°C	V		160			160			160			160		MHz
Analog Input Slew Rate[6]	+25°C	V		440			440			440			440		V/µs
REFERENCE INPUT															
Reference Ladder Resistance	+25°C	VI	64	80	110	64	80	110	64	80	110	64	80	110	Ω
Ladder Temperature Coefficient		V		0.25			0.25			0.25			0.25		Ω/°C
Reference Input Bandwidth	+25°C	V		10			10			10			10		MHz
DYNAMIC PERFORMANCE															
Conversion Rate	+25°C	I	75	100		75	100		75	100		75	100		MSPS
Aperture Delay	+25°C	V		3.8			3.8			3.8			3.8		ns
Aperture Uncertainty (Jitter)	+25°C	V		15			15			15			15		ps
Output Delay (t_{PD})[7, 8]	+25°C	I	4	4.9	11	4	4.9	11	4	4.9	11	4	4.9	11	ns
Transient Response[9]	+25°C	V		8			8			8			8		ns
Overvoltage Recovery Time[10]	+25°C	V		8			8			8			8		ns
Output Rise Time[7]	+25°C	I		6.6	8.0		6.6	8.0		6.6	8.0		6.6	8.0	ns
Output Fall Time[7]	+25°C	I		3.3	4.3		3.3	4.3		3.3	4.3		3.3	4.3	ns
Output Time Skew[7, 11]	+25°C	V		3.0			3.0			3.0			3.0		ns
ENCODE INPUT															
Logic "1" Voltage[7]	Full	VI	2.0			2.0			2.0			2.0			V
Logic "0" Voltage[7]	Full	VI			0.8			0.8			0.8			0.8	V
Logic "1" Current	Full	VI			250			250			250			250	µA
Logic "0" Current	Full	VI			400			400			400			400	µA
Input Capacitance	+25°C	V		2.5			2.5			2.5			2.5		pF
Encode Pulse Width (Low)[12]	+25°C	I	2.5			2.5			2.5			2.5			ns
Encode Pulse Width (High)[12]	+25°C	I	2.5			2.5			2.5			2.5			ns
OVERFLOW INHIBIT INPUT															
0V Input Current	Full	VI		200	250		200	250		200	250		200	250	µA
AC LINEARITY[13]															
Effective Bits[14]	+25°C	V		7.5			7.5			7.5			7.5		Bits
In-Band Harmonics															
dc to 1.23MHz	+25°C	I	48	55		48	55		48	55		48	55		dBc
dc to 9.3MHz	+25°C	V		50			50			50			50		dBc
dc to 19.3MHz	+25°C	V		44			44			44			44		dBc
Signal-to-Noise Ratio[15]	+25°C	I	46	47.6		46	47.6		46	47.6		46	47.6		dBc
Noise Power Ratio[16]	+25°C	V		37			37			37			37		dBc
DIGITAL OUTPUT															
Logic "1" Voltage	Full	VI	2.4			2.4			2.4			2.4			V
Logic "0" Voltage	Full	VI			0.4			0.4			0.4			0.4	V
POWER SUPPLY[17]															
Positive Supply Current (+5.0V)	+25°C	I		33	45		33	45		33	45		33	45	mA
	Full	VI			48			48			48			48	mA
Supply Current (−5.2V)	+25°C	I		152	179		152	179		152	179		152	179	mA
	Full	VI			191			191			191			191	mA
Nominal Power Dissipation	+25°C	V		955			955			955			955		mW
Reference Ladder Dissipation	+25°C	V		44			44			44			44		mW
Power Supply Rejection Ratio[18]	+25°C	I		0.85	2.5		0.85	2.5		0.8	2.5		0.8	2.5	mV/V

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]$+V_{REF} \geq -V_{REF}$ under all circumstances.

[3]Maximum junction temperature (t_J max) should not exceed +175°C for ceramic packages, and +150°C for plastic packages:

$t_J = PD\ (\theta_{JA}) + t_A$
$PD\ (\theta_{JC}) + t_C$

where

PD = power dissipation
θ_{JA} = thermal impedance from junction to ambient (°C/W)
θ_{JC} = thermal impedance from junction to case (°C/W)
t_A = ambient temperature (°C)
t_C = case temperature (°C)

typical thermal impedances are:

Ceramic DIP $\theta_{JA} = 56°C/W$; $\theta_{JC} = 20°C/W$
Plastic DIP $\theta_{JA} = 60°C/W$; $\theta_{JC} = 20°C/W$
Ceramic LCC $\theta_{JA} = 69°C/W$; $\theta_{JC} = 23°C/W$
PLCC $\theta_{JA} = 60°C/W$; $\theta_{JC} = 19°C/W$.

[4]Measured with Analog Input = 0V.

[5]Measured by FFT analysis where fundamental is −3dBc.

[6]Input slew rate derived from rise time (10% to 90%) of full-scale step input.

[7]Outputs terminated with two equivalent 'LS00 type loads. (See load circuit.)

[8]Measured from ENCODE into data out for LSB only.

[9]For full-scale step input, 8-bit accuracy is attained in specified time.

[10]Recovers to 8-bit accuracy in specified time, after 150% full-scale input overvoltage.

[11]Output time skew includes high-to-low and low-to-high transitions as well as bit-to-bit time skew differences.

[12]ENCODE signal rise/fall times should be less than 30ns for normal operation.

[13]Measured at 75MSPS encode rate. Harmonic data based on worst case harmonics.

[14]Analog input frequency = 1.23MHz.

[15]RMS signal to rms noise, including harmonics with 1.23MHz analog input signal.

[16]NPR measured @ 0.5MHz. Noise Source is 250mW (rms) from 0.5MHz to 8MHz.

[17]Supplies should remain stable within ±5% for normal operation.

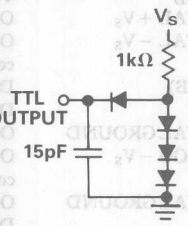
[18]Measured at −5.2V ±5% and +5.0V ±5%.

Specifications subject to change without notice.

Recommended Operating Conditions

Parameter	Input Voltage Min	Nominal	Max
$-V_S$	−5.46	−5.20	−4.94
$+V_S$	+4.75	5.00	+5.25
$+V_{REF}$	$-V_{REF}$	0.0V	+0.1
$-V_{REF}$	−2.1	−2.0	$+V_{REF}$
Analog Input	$-V_{REF}$		$+V_{REF}$

LOAD CIRCUIT



EXPLANATION OF TEST LEVELS

Test Level I – 100% production tested.
Test Level II – 100% production tested at +25°C, and sample tested at specified temperatures.
Test Level III – Sample tested only.
Test Level IV – Parameter is guaranteed by design and characterization testing.
Test Level V – Parameter is a typical value only.
Test Level VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Device	Linearity	Temperature Range	Package Option*
AD9012AQ	0.75LSB	−25°C to +85°C	Q-28
AD9012BQ	0.50LSB	−25°C to +85°C	Q-28
AD9012AN	0.75LSB	−25°C to +85°C	N-28
AD9012BN	0.50LSB	−25°C to +85°C	N-28
AD9012AP	0.75LSB	−25°C to +85°C	P-28A
AD9012BP	0.50LSB	−25°C to +85°C	P-28A
AD9012SQ	0.75LSB	−55°C to +125°C	Q-28
AD9012SE	0.75LSB	−55°C to +125°C	E-28A
AD9012TQ	0.50LSB	−55°C to +125°C	Q-28
AD9012TE	0.50LSB	−55°C to +125°C	E-28A

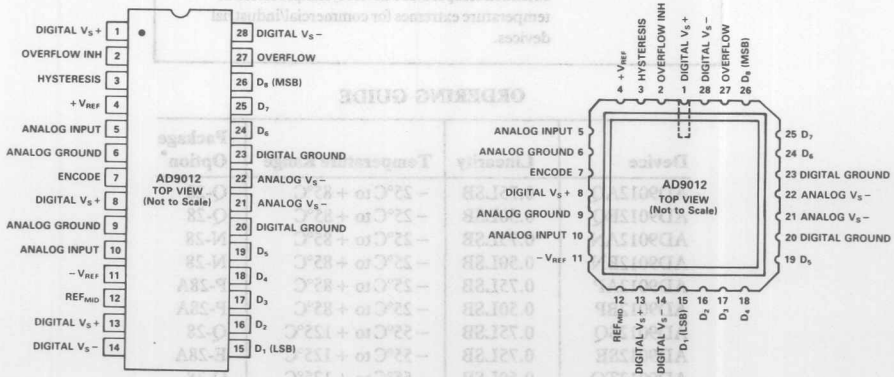
*E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

1	DIGITAL $+V_S$	One of three positive digital supply pins (nominally $+5.0V$).
2	OVERFLOW INH	OVERFLOW INHIBIT controls the data output coding for overvoltage inputs ($AIN \geq +V_{REF}$).

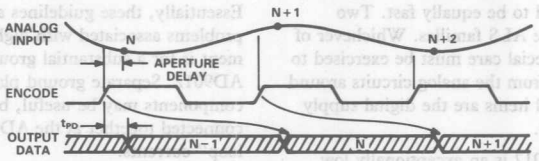
ANALOG INPUT	OVERFLOW ENABLED (FLOATING) OF	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	OVERFLOW INHIBITED (GND) OF	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8
$V_{IN} \geq +V_{REF}$	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$V_{IN} < +V_{REF}$	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X

3	HYSTERESIS	The Hysteresis control voltage varies the comparator hysteresis from 0mV to 10mV, for a change from $-5.2V$ to $-2.2V$ at the Hysteresis control pin.
4	$+V_{REF}$	The most positive reference voltage for the internal resistor ladder.
5	ANALOG INPUT	One of two analog input pins. Both analog input pins should be connected together.
6	ANALOG GROUND	One of two analog ground pins. Both analog ground pins should be connected together.
7	ENCODE	TTL level encode command input. ENCODE is rising edge sensitive.
8	DIGITAL $+V_S$	One of three positive digital supply pins (nominally $+5.0V$).
9	ANALOG GROUND	One of two analog ground pins. Both analog ground pins should be connected together.
10	ANALOG INPUT	One of two analog input pins. Both analog inputs should be connected together.
11	$-V_{REF}$	The most negative reference voltage for the internal resistor ladder.
12	REF_{MID}	The midpoint tap on the internal resistor ladder.
13	DIGITAL $+V_S$	One of three positive digital supply pins (nominally $+5.0V$)
14	DIGITAL $-V_S$	One of two negative digital supply pins (nominally $-5.2V$). Both digital supply pins should be connected together.
15	D_1 (LSB)	Digital data output. D_1 (LSB) is the least significant bit of the digital output word.
16-19	D_2-D_5	Digital data output.
20	DIGITAL GROUND	One of two digital ground pins. Both digital grounds pins should be connected together.
21, 22	ANALOG $-V_S$	One of two negative analog supply pins (nominally $-5.2V$). Both analog supply pins should be connected together.
23	DIGITAL GROUND	One of two digital ground pins. Both digital ground pins should be connected together.
24, 25	D_6, D_7	Digital data output.
26	D_8 (MSB)	Digital data output D_8 (MSB) is the most significant bit of the digital output word.
27	OVERFLOW	Overflow data output. Logic HIGH indicates an input overvoltage ($V_{IN} > +V_{REF}$), if OVERFLOW INHIBIT is enabled (overflow enabled, floating). See OVERFLOW INHIBIT.
28	DIGITAL $-V_S$	One of two negative digital supply pins (nominally $-5.2V$). Both digital supply pins should be connected together.

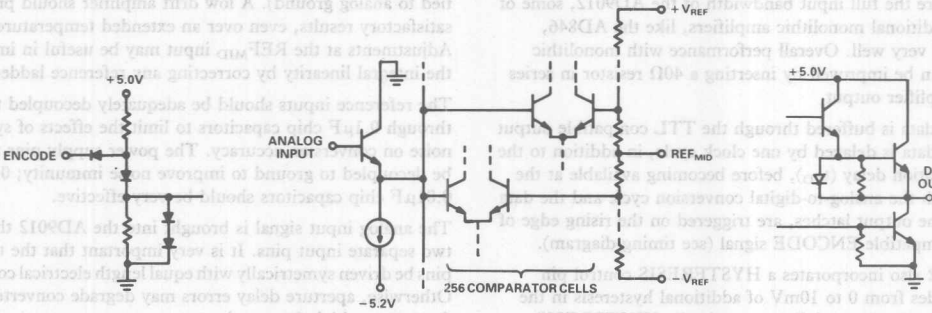
PIN DESIGNATIONS



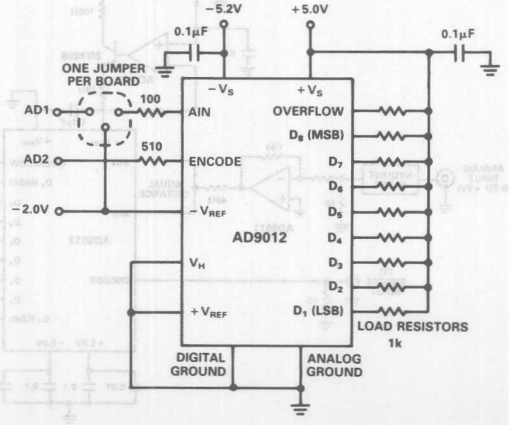
TIMING DIAGRAM



INPUT OUTPUT CIRCUITS

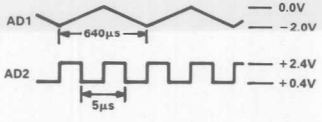


BURN-IN DIAGRAM

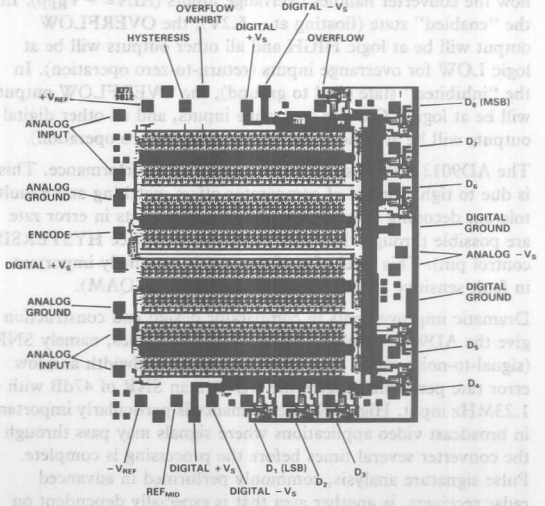


ALL RESISTORS ±5%
ALL CAPACITORS ±20%
ALL SUPPLY VOLTAGES ±5%

OPTION #1 (STATIC) AD1 = −2.0V; AD2 = +2.4V
OPTION #2 (DYNAMIC) SEE WAVEFORMS



DIE LAYOUT AND MECHANICAL INFORMATION



Die Dimensions	111 × 123 × 15 (±2) mils
Pad Dimensions	4 × 4 mils
Metalization	Gold
Backing	None
Substrate Potential	$-V_S$
Passivation	Nitride
Die Attach	Gold Eutectic (Ceramic) Epoxy (Plastic)
Bond Wire	1–1.3 mil Gold; Gold Ball Bonding

APPLICATION INFORMATION

The AD9012 is compatible with all standard TTL logic families. However, to operate at the highest encode rates, the supporting logic around the AD9012 will need to be equally fast. Two possible choices are the AS and the ALS families. Whichever of the TTL logic families is used, special care must be exercised to keep digital switching noise away from the analog circuits around the AD9012. The two most critical items are the digital supply lines and the digital ground return.

The input capacitance of the AD9012 is an exceptionally low 16pF. This allows the use of a wide range of input amplifiers, both hybrid and monolithic. To take full advantage of the 160MHz input bandwidth of the AD9012, a hybrid amplifier like the AD9610/AD9611 will be required. For those applications that do not require the full input bandwidth of the AD9012, some of the more traditional monolithic amplifiers, like the AD846, should work very well. Overall performance with monolithic amplifiers can be improved by inserting a 40Ω resistor in series with the amplifier output.

The output data is buffered through the TTL compatible output latches. All data is delayed by one clock cycle, in addition to the latch propagation delay (t_{PD}), before becoming available at the outputs. Both the analog-to-digital conversion cycle and the data transfer to the output latches, are triggered on the rising edge of the TTL compatible ENCODE signal (see timing diagram).

The AD9012 also incorporates a HYSTERESIS control pin which provides from 0 to 10mV of additional hysteresis in the comparator input stages. Adjustments in the HYSTERESIS control voltage may help to improve noise immunity and overall performance in harsh environments.

The OVERFLOW INHIBIT pin of the AD9012 determines how the converter handles overrange inputs (AIN≥ $+V_{REF}$). In the "enabled" state (floating at −5.2V), the OVERFLOW output will be at logic HIGH and all other outputs will be at logic LOW for overrange inputs (return-to-zero operation). In the "inhibited" state (tied to ground), the OVERFLOW output will be at logic LOW for overrange inputs, and all other digital outputs will be at logic HIGH (nonreturn-to-zero operation).

The AD9012 provides outstanding error rate performance. This is due to tight control of comparator offset matching and a fault tolerant decoding stage. Additional improvements in error rate are possible through the addition of hysteresis (see HYSTERSIS control pin). This level of performance is extremely important in fault sensitive applications like digital radio (QAM).

Dramatic improvements in comparator design and construction give the AD9012 excellent dynamic characteristics, namely SNR (signal-to-noise ratio). The 160MHz input bandwidth and low error rate performance give the AD9012 an SNR of 47dB with a 1.23MHz input. High SNR performance is particularly important in broadcast video applications where signals may pass through the converter several times before the processing is complete. Pulse signature analysis, commonly performed in advanced radar receivers, is another area that is especially dependent on high quality dynamic performance.

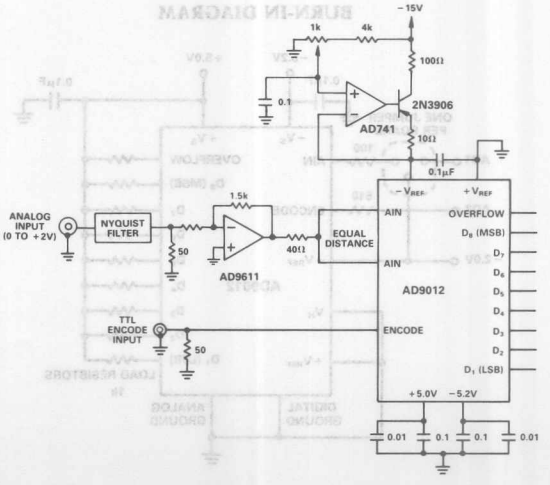
LAYOUT SUGGESTIONS

Designs using the AD9012, like all high-speed devices, must follow a few basic layout rules to insure optimum performance. Essentially, these guidelines are meant to avoid many of the problems associated with high-speed designs. The first requirement is for a substantial ground plane around and under the AD9012. Separate ground plane areas for the digital and analog components may be useful, but the separate grounds should be connected together at the AD9012 to avoid the effects of "ground loop" currents.

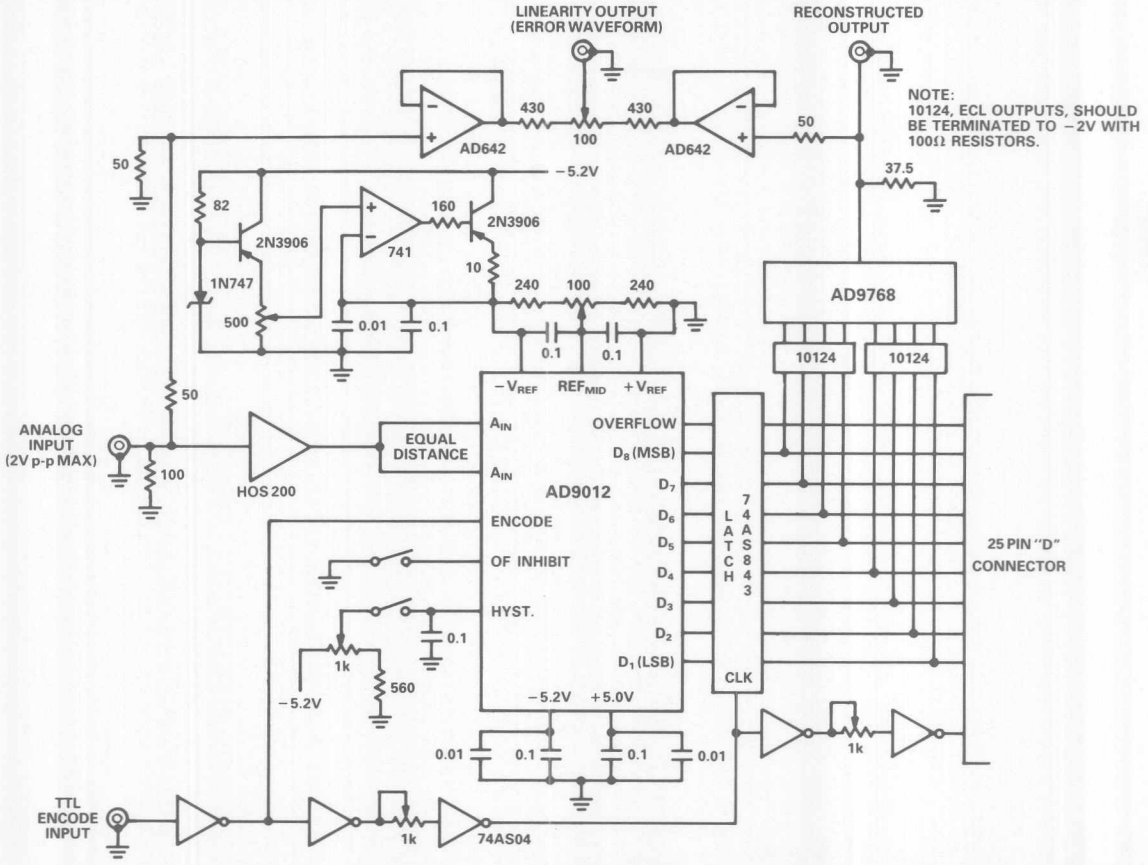
The second area that requires an extra degree of attention involves the three reference inputs, $+V_{REF}$, REF_{MID}, and $-V_{REF}$. The $+V_{REF}$ input and the $-V_{REF}$ input should both be driven from a low impedance source (note that the $+V_{REF}$ input is typically tied to analog ground). A low drift amplifier should provide satisfactory results, even over an extended temperature range. Adjustments at the REF_{MID} input may be useful in improving the integral linearity by correcting any reference ladder skews.

The reference inputs should be adequately decoupled to ground through 0.1μF chip capacitors to limit the effects of system noise on conversion accuracy. The power supply pins must also be decoupled to ground to improve noise immunity; 0.1μF and 0.01μF chip capacitors should be very effective.

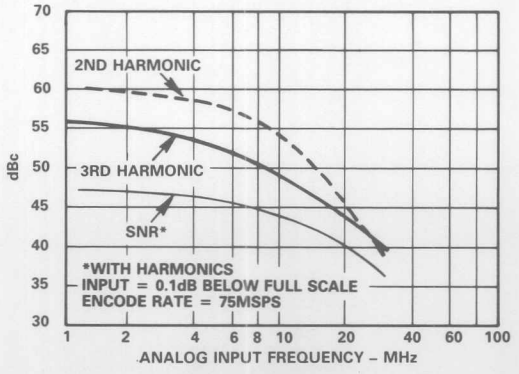
The analog input signal is brought into the AD9012 through two separate input pins. It is very important that the two input pins be driven symetrically with equal length electrical connections. Otherwise, aperture delay errors may degrade converter performance at high frequencies.



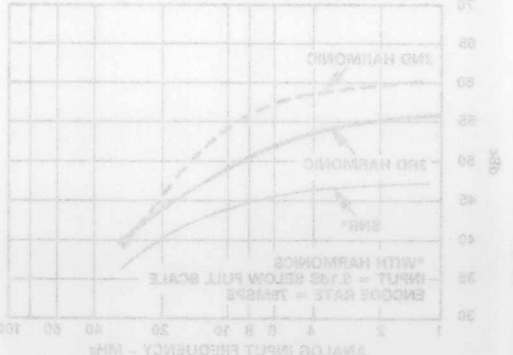
Typical AD9012 Application



AD9012 Evaluation Circuit



Dynamic Performance

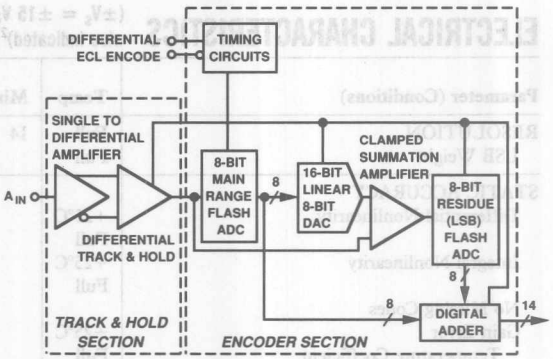


AD9014

FEATURES
Sample Rate: 10 MSPS
Spurious Free Dynamic Range: 92 dB @ 2.3 MHz A_{IN}; 88 dB @ 4.3 MHz A_{IN}; 72 dB @ 10 MHz A_{IN}
Low Intermodulation Distortion: –95 dBFS @ 2.3 MHz
SNR: 75 dB
Differential Encode Clock
Complete Subsystem

APPLICATIONS
Radar Signal Analysis
Visible & Infrared Imaging
FFT Spectrum Analysis
Medical Imaging
SIGINT/ECM/EW

AD9014 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9014 is a high performance 14-bit analog-to-digital converter designed to provide extremely wide dynamic range for spectrum analysis and imaging applications. It is a complete subsystem that requires the user to provide only power and an encode clock.

Careful consideration to the design of the converter, along with the development of several custom linear and digital IC building blocks, has resulted in a converter with unsurpassed dynamic range. Sampling at 10 MSPS, the spurious free dynamic range (SFDR) is a function of analog input frequency as shown below:

Analog Input	SFDR
100 kHz	90 dB (min)
2.3 MHz	90 dB (min)
4.3 MHz	86 dB (min)
10 MHz	72 dB (typ)

For the AD9014, DNL is 0.5 LSBs; transient response to 0.01% is 30 ns; full power bandwidth is 50 MHz; and the SNR is 75 dB. These attributes make the AD9014 ideal for applications that require fast sampling of relatively low frequency analog input signals, such as CCD and infrared imaging.

The AD9014 consists of two custom hybrids mounted on a small multilayer PCB. The hybrid differential track-and-hold achieves first order cancellation of the even order harmonics while suppressing common-mode noise. The second hybrid is a digitally corrected subranging A/D encoder that uses two 8-bit flash converters with two bits of overlap correction. Decoupling capacitors have been designed into both hybrids, as well as on the mother board. This onboard decoupling simplifies the task of successfully using the converter.

Each AD9014 is tested at a 10 MSPS encode rate at multiple analog input frequencies. For each input frequency, the FFT testing is repeated for various A_{IN} power levels. This technique verifies that the dynamic performance of the converter is maintained even when low level input signals are being digitized.

Two versions of the AD9014 are available. The AD9014K is intended for applications that require the highest possible spurious free dynamic range performance; the AD9014J is intended for applications where spectral domain information is not as important, such as in imaging. The analog input signal can be applied to the ADC via either an onboard SMA connector or through a pin connected to the connector. Logic is ECL; the encode clock is differential ECL.

Consult Analog Devices about special needs and/or specific applications.

Supply Voltages ($\pm V_S$)	±18 V
V_{CC} Supply Voltage	+6 V
V_{EE} Supply Voltage	−6 V
Analog Input Voltage $V_{EE} \leq A_{IN} \leq V_{CC}$ (or whichever is less)	±4 V
Digital Input Voltage	V_{EE} to +0.5 V
Digital Output Current	4 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

($\pm V_S$ = ±15 V; V_{CC} = +5 V; V_{EE} = −5.2 V; Encode Rate = 10.0 MSPS unless otherwise indicated)[2]

Parameter (Conditions)	Temp	AD9014J Min	AD9014J Typ	AD9014J Max	AD9014K Min	AD9014K Typ	AD9014K Max	Units
RESOLUTION	Full	14			14			Bits
LSB Weight	Full		0.122			0.122		mV
STATIC ACCURACY								
Differential Nonlinearity	+25°C		0.6			0.5		LSB
	Full		0.6			0.5		LSB
Integral Nonlinearity	+25°C		1.0			0.75		LSB
	Full		1.5			1.0		LSB
No Missing Codes			Guaranteed			Guaranteed		
Gain Error	+25°C		0.2	1.0		0.2	1.0	% FS
Temperature Coefficient	Full		15			15		ppm/°C
Offset Error	+25°C		0.2	1.0		0.2	1.0	% FS
Temperature Coefficient	Full		8			8		ppm/°C
ANALOG INPUT								
Input Voltage Range	Full		±1.0			±1.0		V
Input Resistance	Full		75			75		Ω
Input Capacitance (at SMA connector)[3]	+25°C		7			7		pF
Full Power Input Bandwidth	Full		60			60		MHz
SWITCHING PERFORMANCE								
Conversion Rate[4]	Full			10.00			10.00	MSPS
Pipeline Delay	Full		1			1		Clock Cycle
Output Data Delay (t_{OD})[5]	+25°C		30			30		ns
Aperture Delay	+25°C		4			4		ns
Aperture Jitter	+25°C		1.5			1.5		ps rms
DYNAMIC CHARACTERISTICS[4, 6]								
Transient Response (to 0.01%)	+25°C		30			30		ns
Overvoltage Recovery Time (1.5 × to 0.01%)	+25°C		100			100		ns
Overvoltage Recovery Time (1.5 × to 0.0025%)	+25°C		200			200		ns
Worst-Case Harmonic Distortion[7]								
A_{IN} = 100 kHz	+25°C	−84			−90			dBFS
A_{IN} = 2.3 MHz	+25°C	−84			−90			dBFS
A_{IN} = 4.3 MHz	+25°C	−82			−86			dBFS
A_{IN} = 10 MHz	+25°C		−72			−72		dBFS
Signal-to-Noise Ratio (A_{IN} = 100 kHz)[8]	+25°C		75			75		dB
Signal-to-Noise Ratio (A_{IN} = 2.3 MHz)[8]	+25°C		75			75		dB
Two-Tone Intermodulation								
2.3 MHz & 2.4 MHz (each −7 dBFS)	+25°C	−84			−90			dBFS
ENCODE INPUT[9]		Differential ECL			Differential ECL			
Logic "1" Voltage	Full	−1.1			−1.1			V
Logic "0" Voltage	Full			−1.5			−1.5	V
Logic "1" Current	Full		8			8		mA
Logic "0" Current	Full		8			8		mA
Input Capacitance	+25°C		5			5		pF
Encode Pulse Width	+25°C	10			10			ns
Encode Pulse Width (% of duty cycle)	+25°C			50			50	%

Parameter (Conditions)	Temp	AD9014J Min	AD9014J Typ	AD9014J Max	AD9014K Min	AD9014K Typ	AD9014K Max	Units
DIGITAL OUTPUTS[10]								
Logic "1" Voltage	Full	−1.1			−1.1			V
Logic "0" Voltage	Full			−1.5			−1.5	V
Logic Coding	Full		Offset Binary			Offset Binary		
POWER SUPPLIES								
$+V_S$ Supply Voltage	Full	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	V
$+V_S$ Supply Current	Full		245			245		mA
$-V_S$ Supply Voltage	Full	−14.5	−15.0	−15.5	−14.5	−15.0	−15.5	V
$-V_S$ Supply Current	Full		130			130		mA
V_{CC} Supply Voltage	Full	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	V
V_{CC} Supply Current	Full		422			422		mA
V_{EE} Supply Voltage	Full	−4.95	−5.2	−5.45	−4.95	−5.2	−5.45	V
V_{EE} Supply Current	Full		980			980		mA
Power Dissipation (Operating)	Full		12.8			12.8		W
Power Supply Rejection Ratio (PSRR)								
$+V_S$ (ΔV_S = ±0.5 V)	+25°C		0.02			0.02		%/%
$-V_S$ (ΔV_S = ±0.5 V)	+25°C		0.01			0.01		%/%
V_{CC} (ΔV_{CC} = ±0.25 V)	+25°C		0.01			0.01		%/%
V_{EE} (ΔV_{EE} = ±0.25 V)	+25°C		0.01			0.01		%/%

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

[2]Cooling air at 500 LFPM applied. Parts must have 30 second warm-up time.

[3]The capacitance seen at the analog input pin of the T/H hybrid is 2.0 pF.

[4]Consult factory regarding availability of units with lower spur levels; units capable of 10.24 MSPS rates are also available.

[5]Measured from rising edge of Encode Command (Pin 16) to instant of final change in data output.

[6]During factory testing, analog input is applied to AD9014 via onboard SMA connector.

[7]Power of the analog input is swept from −1 dBFS to approximately −60 dBFS; and multiple FFTs are taken for "K-grade" parts. The specification is equivalent to the spurious free dynamic range (SFDR).

[8]Including noise and all spurs.

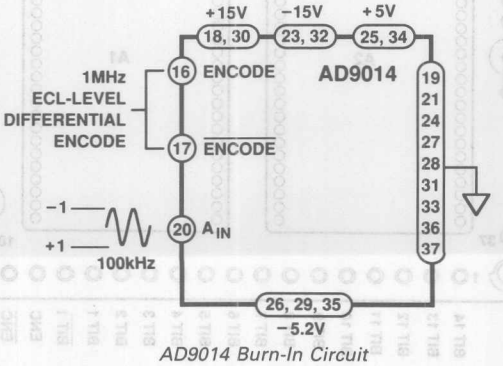
[9]10Kvoltage-level-compatible. Encode inputs have 50 Ω differential terminations.

[10]Each digital output is terminated to −5.2 V through a 2 kΩ resistor with a 1k resistor in series with the output. See diagram elsewhere in data sheet.

ORDERING GUIDE

Model*	Temperature Range	SFDR
AD9014J	0°C to +70°C	84 dB
AD9014K	0°C to +70°C	90 dB

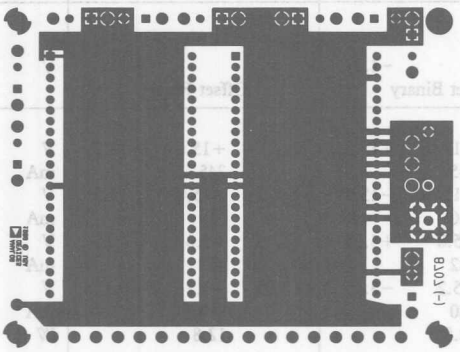
*Add −50 to part number to specify 50 Ω input impedance.



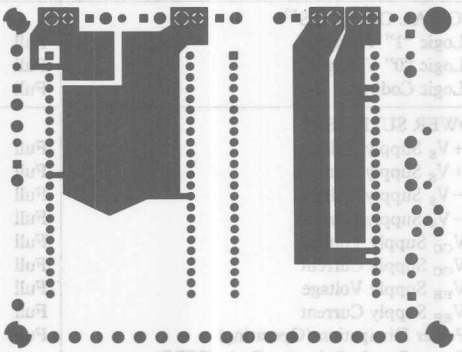
AD9014 Burn-In Circuit

AD9014 PRINTED CIRCUIT BOARD LAYERS

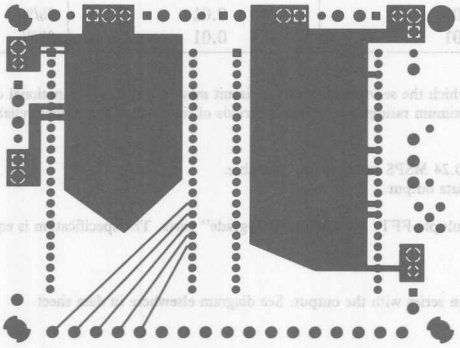
All layers shown from component (top) side.



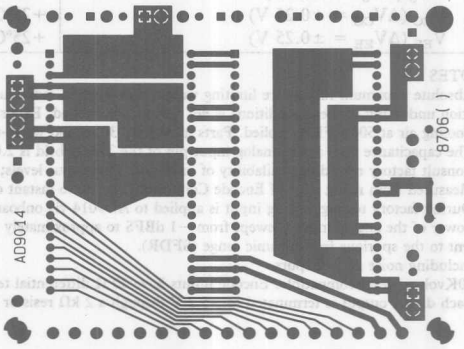
Layer 1 (Bottom)



Layer 2

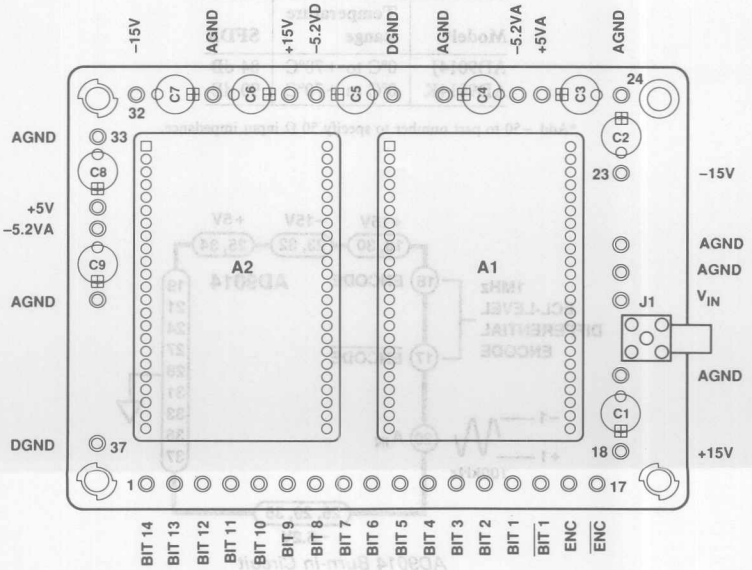


Layer 3



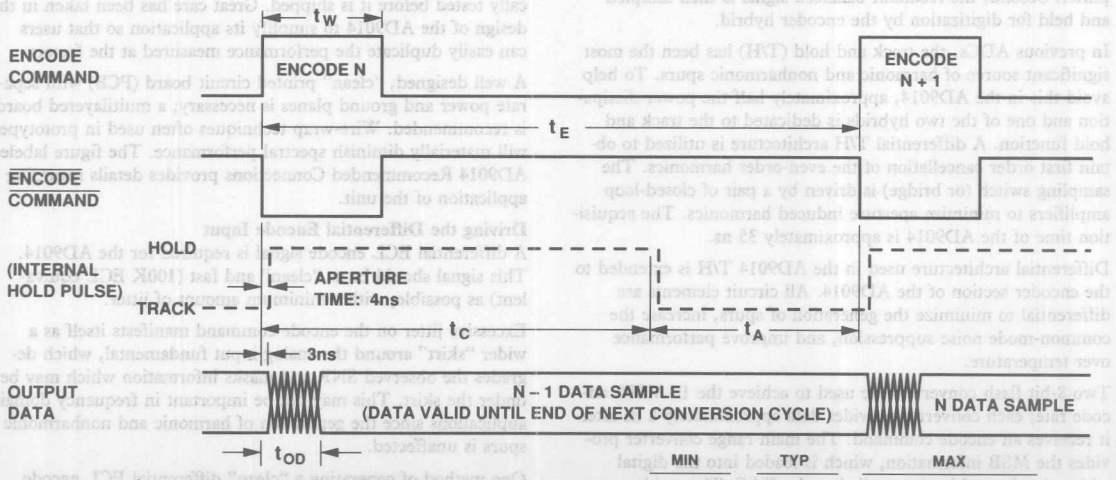
Layer 4 (Top)

AD9014 PIN CONFIGURATION



AD9014 PIN DESCRIPTIONS

Pin No.	Name	Function
1 through 14	Bit 14 (LSB) through Bit 1 (MSB)	True ECL outputs. Each is internally terminated to −5.2 V through a 2 kΩ resistor and has limited drive capability; a 1 kΩ isolation resistor is connected in series with the output. Additional termination will increase current spikes within the hybrid, and possibly degrade A/D performance. These pins should be interfaced to ECL receivers or latches located as close as possible to the AD9014. Positive full scale is represented by all "1"s. (See equivalent circuit elsewhere in data sheet.)
15	$\overline{\text{Bit 1 (MSB)}}$	Complement of Bit 1 (see above).
16	ENCODE	Differential ECL ENCODE inputs; 50 Ω internal terminations. User-supplied ENCODE command should contain smallest possible amount of jitter for optimum performance.
17	$\overline{\text{ENCODE}}$	
18, 30	+15 V	Analog supply pins; decoupling capacitors included on AD9014 card.
19, 24, 27	AGND	Analog ground; should be connected to low impedance ground plane.
20	A_{IN}	Analog input to AD9014; interface is via either SMA connector or this pin, nominally 75 Ω input impedance. (See equivalent circuit.)
21	AGND	Signal ground reference; should be connected to signal source reference.
22	AGND	Signal ground reference; should be connected to signal source reference.
23, 32	−15 V	Analog supply pins; decoupling capacitors included on AD9014 card.
25, 34	+5 V	V_{CC} analog supply pins; decoupling included on AD9014 board.
26, 35	−5.2 V	V_{EE} analog supply pins; decoupling included on AD9014 board.
31, 33, 36	AGND	Analog ground; should be connected to low impedance ground plane.
29	−5.2 V	Digital V_{EE} supply pin.
28, 37	DGND	Digital ground; should be connected to low impedance ground plane.



		MIN	TYP	MAX
t_W	ENCODE COMMAND PULSE WIDTH	10ns		50% OF DUTY CYCLE
t_E	SPACING BETWEEN ENCODE COMMANDS	100ns		
t_C	CONVERSION TIME		65ns	
t_A	ACQUISITION TIME *		35ns	
t_{OD}	OUTPUT DELAY [DRIVING SINGLE 10K LOGIC GATE ADJACENT TO UNIT (SEE APPLICATIONS SECTION)]		30ns	

*APPLICATIONS WITH SLIGHTLY FASTER SAMPLING RATE (10.24 MSPS) WILL HAVE ACQUISITION TIME WHICH IS APPROXIMATELY 2ns SHORTER

AD9014 Timing Diagram

The AD9014 is a two-step subranging analog to digital converter that provides extremely wide dynamic range performance. Its major system building blocks include a single to differential amplifier; track and hold amplifier; 8-bit main range flash ADC; 16-bit-linear, 8-bit DAC; clamped monolithic summation amplifier; 8-bit residue flash ADC; and digital adder logic.

The AD9014 consists of two custom hybrids mounted on a small multilayered PCB. It was made possible by a judicious combination of innovative design topologies, new custom chips, and mature manufacturing processes including laser trimming of thin-film resistors.

Subranging architecture has been utilized in numerous ADCs and has proven to be an efficient way to obtain wide dynamic range at high sampling rates. Briefly, a single-ended analog input signal is converted to a balanced differential signal that is "sampled and held" by a track and hold amplifier. This held value is then digitized by the main range 8-bit flash A/D converter. The resulting 8-bit word is converted back to an analog value via a 16-bit-linear, 8-bit DAC and is compared to the "held" value via a high accuracy, clamped summation amplifier. The difference of the two signals is then digitized by a second 8-bit flash ADC. In the final step, the two 8-bit words are combined via digital adder logic.

Refer to the block diagram of the AD9014 on the first page of this data sheet. The track and hold hybrid accomplishes two functions. First, the single-ended analog input is converted to a balanced differential signal via an extremely low distortion single to differential amplifier. The 75 Ω input impedance of the AD9014 can be regarded as the feed-forward resistor of this amplifier. Second, the resultant balanced signal is then sampled and held for digitization by the encoder hybrid.

In previous ADCs, the track and hold (T/H) has been the most significant source of harmonic and nonharmonic spurs. To help avoid this in the AD9014, approximately half the power dissipation and one of the two hybrids is dedicated to the track and hold function. A differential T/H architecture is utilized to obtain first order cancellation of the even-order harmonics. The sampling switch (or bridge) is driven by a pair of closed-loop amplifiers to minimize aperture induced harmonics. The acquisition time of the AD9014 is approximately 35 ns.

Differential architecture used in the AD9014 T/H is extended to the encoder section of the AD9014. All circuit elements are differential to minimize the generation of spurs, increase the common-mode noise suppression, and improve performance over temperature.

Two 8-bit flash converters are used to achieve the 10 MSPS encode rate; each converter provides data approximately 8 ns after it receives an encode command. The main range converter provides the MSB information, which is loaded into the digital adder circuits and is also applied to the DAC. The residue converter provides the LSB information. Two overlap or correction bits are utilized in the digital correction logic where the two 8-bit words are combined into the final 14-bit digital output.

In addition to the track-and-hold, the digital-to-analog converter looms as a large contributor of spurs. The DAC in the AD9014 utilizes unique differential diode switching current sources and laser-trimmed thin film resistors. This optimizes the performance of the ADC as a function of temperature and time.

Laser trimmed thin film resistors are inherently stable over time. Any resistor shifts that occur are transparent to the user matched counterpart. The trimmed DAC settles to 16-bit accuracy in approximately 10 ns.

The output of the DAC is compared to the held dc value via a clamped summation amplifier. This amplifier is set for a gain of 10 V/V and drives the residue 8-bit flash converter. It settles in 35 ns and comes out of overdrive in 5 ns. The settling time of this amplifier is the major factor affecting the maximum sample rate of the AD9014.

The final major source of spurs are the nonlinearities in the two flash converters. Differential nonlinearity (DNL) and integral nonlinearity (INL) errors in the main range converter determine how much of the error correction budget is actually used.

If the INL of the residue converter is sufficiently large, nonlinearities of the main range converter set the DNL of the AD9014 at the digitally compensated subranging points. If the main range converter is sufficiently linear, the DNL of the residue converter sets the overall AD9014 DNL. The flash converters used in the AD9014 are inherently linear; die are screened by probe testing before they are used in the encoder hybrid.

Finally, the two 8-bit digital words from the main range and residue flash converters are latched into a 16-bit register, where they are added to form the 14-bit digital output word. The actual error correction takes place in this adder. If the analog input exceeds positive or negative full scale, the digital output remains, respectively, at all "1" or all "0"; it does not roll over.

USING THE AD9014

The AD9014 A/D converter has been carefully designed to offer users the widest possible dynamic range. Each unit is dynamically tested before it is shipped. Great care has been taken in the design of the AD9014 to simplify its application so that users can easily duplicate the performance measured at the factory.

A well designed, "clean" printed circuit board (PCB) with separate power and ground planes is necessary; a multilayered board is recommended. Wire-wrap techniques often used in prototypes will materially diminish spectral performance. The figure labeled AD9014 Recommended Connections provides details regarding application of the unit.

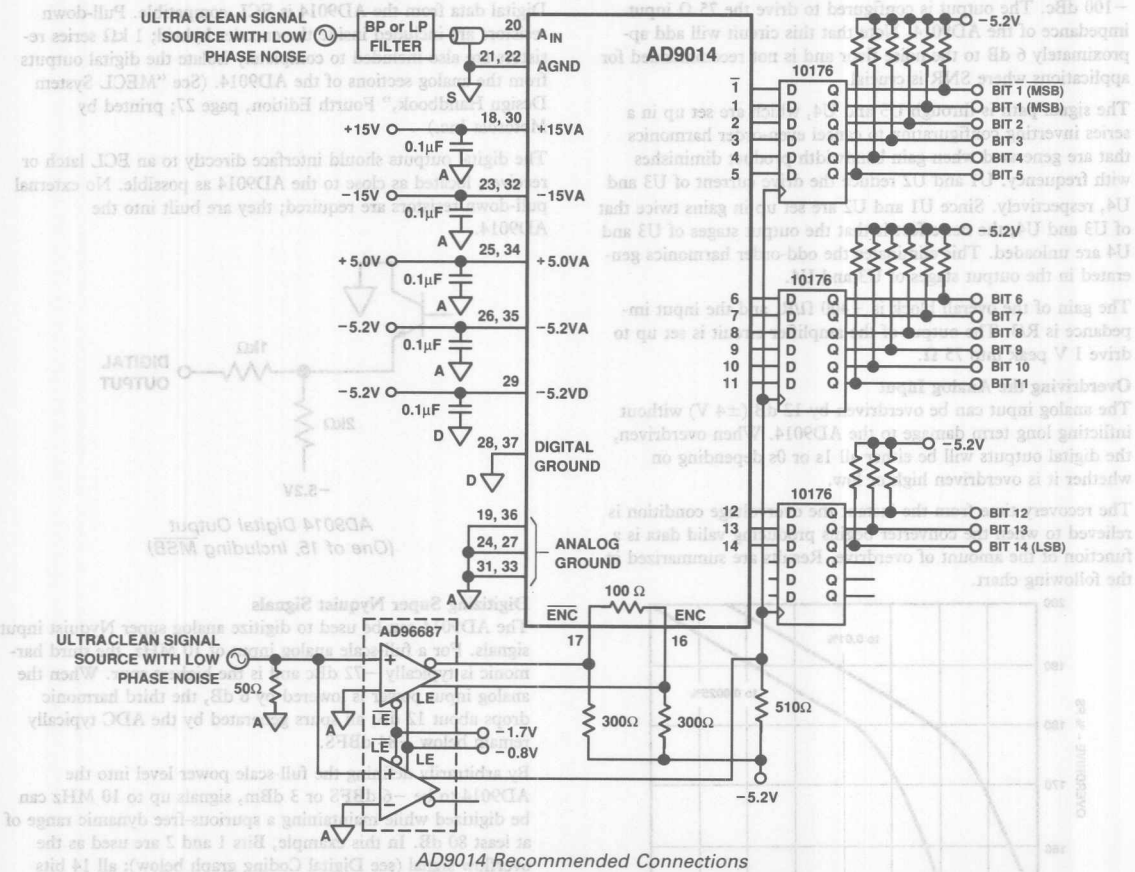
Driving the Differential Encode Input

A differential ECL encode signal is required for the AD9014. This signal should be as "clean" and fast (100K ECL equivalent) as possible, with a minimum amount of jitter.

Excessive jitter on the encode command manifests itself as a wider "skirt" around the analog input fundamental, which degrades the observed SNR and masks information which may be under the skirt. This may not be important in frequency domain applications since the generation of harmonic and nonharmonic spurs is unaffected.

One method of generating a "clean" differential ECL encode signal is to use a spectrally pure low phase noise sine wave to drive an AD96687 ultrafast ECL comparator, as shown in the "AD9014 Recommended Connections" figure on the next page. (Signal generators such as the HP 8642A and Rohde & Schwarz SMHU can be used.)

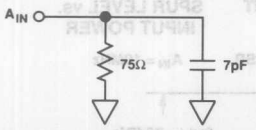
Careful consideration must be given to routing the encode signal. The comparator should be located as close as possible to the AD9014. The inputs to and outputs from the AD96687 should be as short as possible and terminated right at the unit.



AD9014 Recommended Connections

Matching the Analog Input Impedance

As described in the Theory of Operations, the analog input impedance into the track and hold is 75 Ω ‖ 7 pF. This is shown graphically in the figure below.



AD9014 Analog Input Circuit

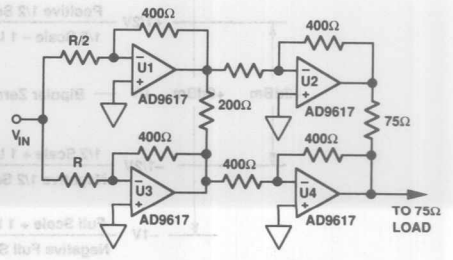
The Analog input signal can be applied to the ADC either via the SMA connector or through Pin 20. The drive source should be matched to the impedance of the ADC. The AD9014 can be set up for a 50 Ω system by soldering the appropriate resistor between Pins 20 and 21. This option will be installed at the factory if "−50" is added to the part number when the order is placed.

Driving the Analog Input

Special care must be taken to ensure that the analog input signal is not compromised before it reaches the A/D converter. Any required filtering should be done as close to the AD9014 as possible, and away from any digital lines.

The full-scale analog input range of the AD9014 is 9 dBm (±1 V into 75 Ω). In many applications, the analog input is at a much lower level and must be amplified to meet the full-scale range of the AD9014. The optimum way to achieve this amplification depends largely on the application.

For frequency domain applications, the circuit shown below is recommended when gain is required. This configuration works well for analog input frequencies through 10 MHz without introducing spurs that degrade the ADC's capabilities. At



Low-Distortion Drive Circuit for AD9014

2.3 MHz and 2 V p–p output, all spurs generated are less than −100 dBc. The output is configured to drive the 75 Ω input impedance of the AD9014. Note that this circuit will add approximately 6 dB to the noise floor and is not recommended for applications where SNR is crucial.

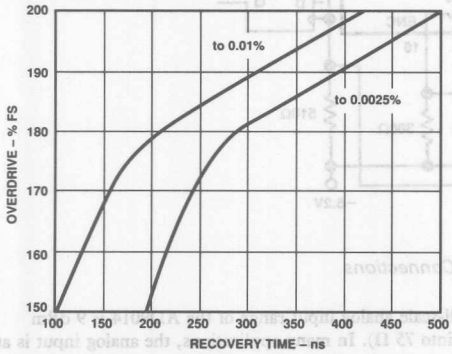
The signal path is through U3 and U4, which are set up in a series inverting configuration to cancel even-order harmonics that are generated when gain bandwidth product diminishes with frequency. U1 and U2 reduce the drive current of U3 and U4, respectively. Since U1 and U2 are set up in gains twice that of U3 and U4, the net effect is that the output stages of U3 and U4 are unloaded. This eliminates the odd-order harmonics generated in the output stages of U3 and U4.

The gain of the overall block is +400 Ω/R, and the input impedance is R/3. The output of the amplifier circuit is set up to drive 1 V peak into 75 Ω.

Overdriving the Analog Input

The analog input can be overdriven by 12 dB (±4 V) without inflicting long term damage to the AD9014. When overdriven, the digital outputs will be either all 1s or 0s depending on whether it is overdriven high or low.

The recovery time from the instant the overvoltage condition is relieved to when the converter begins producing valid data is a function of the amount of overdrive. Results are summarized in the following chart.

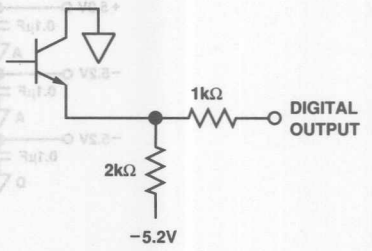


Overvoltage Recovery Time

Collecting the Digital Output Data

Digital data from the AD9014 is ECL compatible. Pull-down resistors are included inside the encoder hybrid; 1 kΩ series resistors are also included to completely isolate the digital outputs from the analog sections of the AD9014. (See "MECL System Design Handbook," Fourth Edition, page 27; printed by Motorola Inc.)

The digital outputs should interface directly to an ECL latch or receiver, located as close to the AD9014 as possible. No external pull-down resistors are required; they are built into the AD9014.

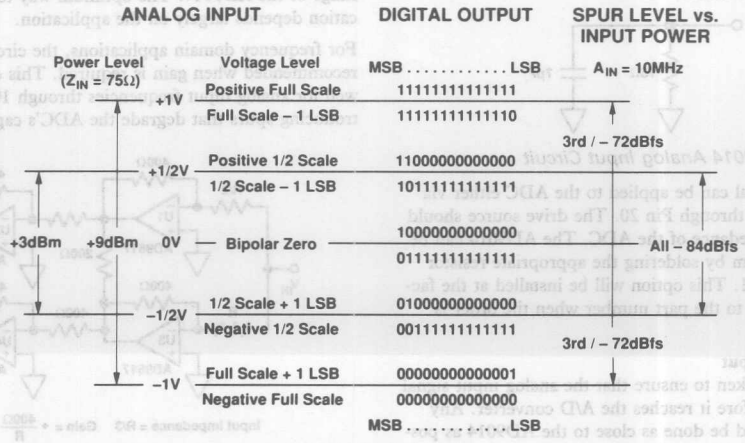


AD9014 Digital Output
(One of 15, Including $\overline{MSB}$)

Digitizing Super Nyquist Signals

The AD9014 can be used to digitize analog super Nyquist input signals. For a full-scale analog input of 10 MHz, the third harmonic is typically −72 dBc and is the highest spur. When the analog input power is lowered by 6 dB, the third harmonic drops about 12 dB; all spurs generated by the ADC typically remain below −84 dBFS.

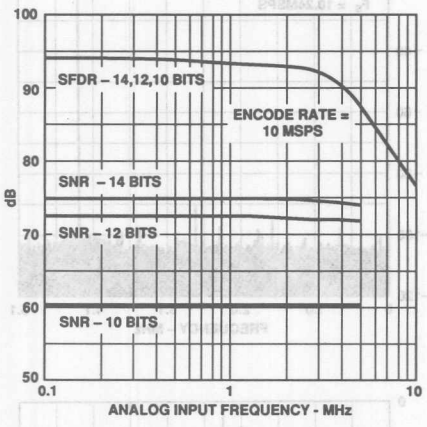
By arbitrarily defining the full-scale power level into the AD9014 to be −6 dBFS or 3 dBm, signals up to 10 MHz can be digitized while maintaining a spurious-free dynamic range of at least 80 dB. In this example, Bits 1 and 2 are used as the overflow signal (see Digital Coding graph below); all 14 bits from the converter must be used, are valid, and should be processed.



AD9014 Digital Coding

Utilizing Fewer than 14 Bits

In some cases it is advantageous to ignore the AD9014's LSBs. As an example, if a previously designed DSP or buffer memory is able to process only 10- or 12-bit words, retrofitting the system using the AD9014 may provide significant improvements.



AD9014 SFDR and SNR vs. Frequency

The spurious free dynamic range (SFDR) of any A/D is a function of the converter linearity, while the "number of bits" of the converter's output affects the level of the noise floor. The level of the internally generated spurs will not rise as bits are omitted, but the noise floor rises for each bit that is dropped. The chart below summarizes the AD9014 SFDR as a function of the number of bits being processed.

Noise Figure Estimates

An estimate of the noise figure of the AD9014 can be calculated from information contained in the specification table. It is defined as the degradation of the signal-to-noise ratio as an analog signal passes through the device.

Since the AD9014 has no gain, the noise figure can be determined by comparing the noise level at the output to the noise at the input. For a 50 Ω system, the input noise can be determined using Boltzmann's Constant, the absolute temperature, and the bandwidth. For a 1 Hz bandwidth at room temperature, this value is −174 dBm/Hz.

The noise level at the output of the AD9014 can be calculated from the specified signal to noise-ratio (SNR) which is 75 dB. Since the full-scale analog input signal is +9 dBm, the noise level at the output of the AD9014 is −66 dBm for the 5 MHz band.

The noise figure can be determined using the following equation:

$$NF = Output\ Noise - 10\log_{10}(BWo/BWi) - Input\ Noise\ Level$$

where BWo = 5 MHz and BWi = 1 Hz

For the AD9014, the noise figure calculates to:

$$NF = -66\ dB - 67\ dB - (-174\ dB) = 41\ dB$$

Third Order Intercept Point

Traditionally, the third order two-tone intermodulation specification of mixers is the most troublesome, since the resultant frequencies are very close to the fundamental signals and are difficult to filter. The differential design of the AD9014 ensures that the generation of two-tone IMD spurs is minimized.

The two-tone IMD intercept point for the AD9014 can be easily estimated for a given frequency if the harmonic suppression of the IMD spur levels is known (or can be measured). As shown in the typical performance section of the data sheet, for 2 dBm (−7 dBFS) analog input tones of 2.3 MHZ and 2.4 MHz, the relevant IMD spurs are located at 2.2 MHz and 2.5 MHz, and are −95 dBm (−102 dBFS).

The following equation can be used to determine the converter's intercept point:

$$Intercept\ Point = [Harmonic\ Suppression/(N-1)] + Input\ Power$$

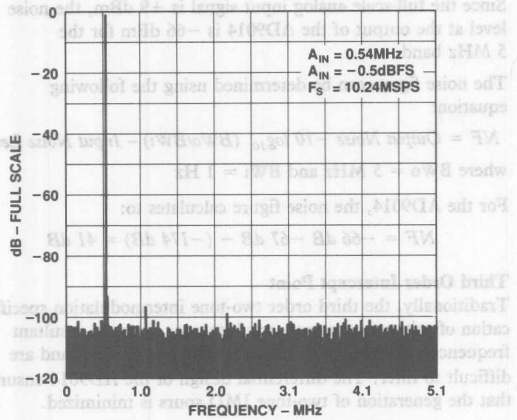
where N = the order of the IMD (3 in this case)

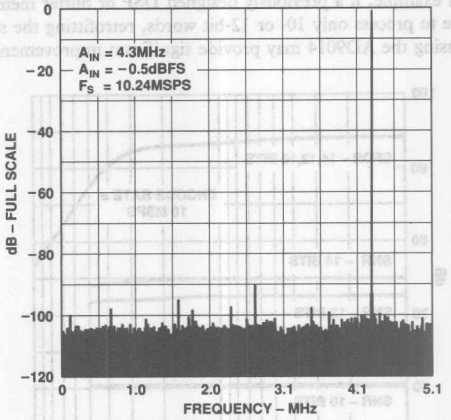
$$AD9014\ Intercept\ Point = 95/2 + 2\ dBm = 49.5\ dBm$$

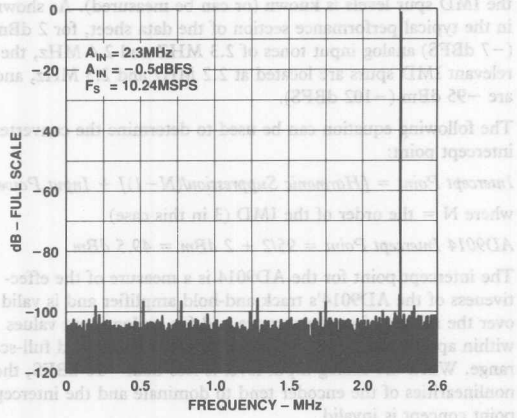
The intercept point for the AD9014 is a measure of the effectiveness of the AD9014's track-and-hold amplifier and is valid over the relevant frequency range and for analog input values within approximately 10 dB of the converter's specified full-scale range. When the analog input level is less than −10 dBFS, the nonlinearities of the encoder tend to dominate and the intercept point concept is invalid.

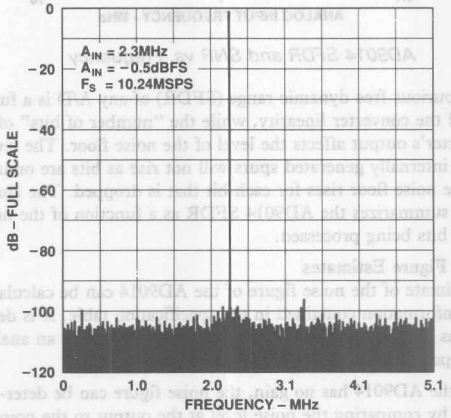
TYPICAL AD9014K SPECTRAL PERFORMANCE

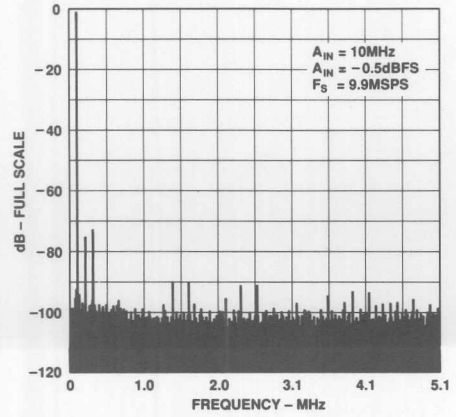
Five-sample average of 8,192-point FFTs; all harmonics are aliased.

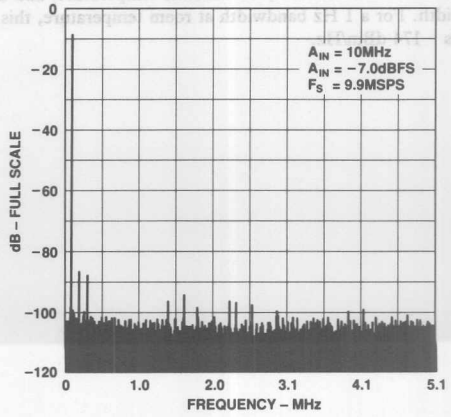


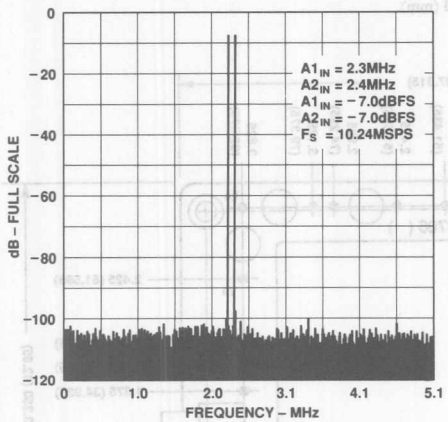


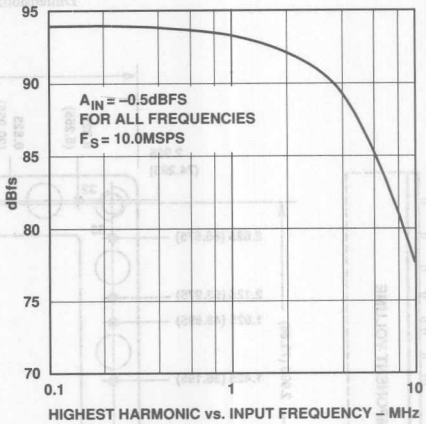




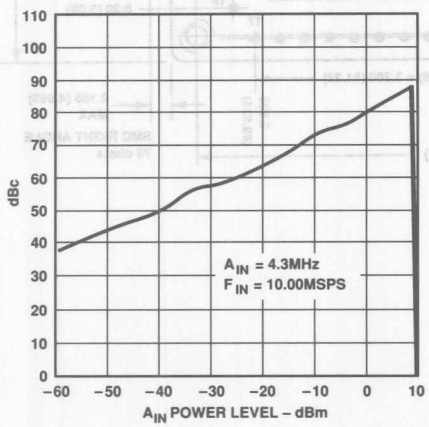


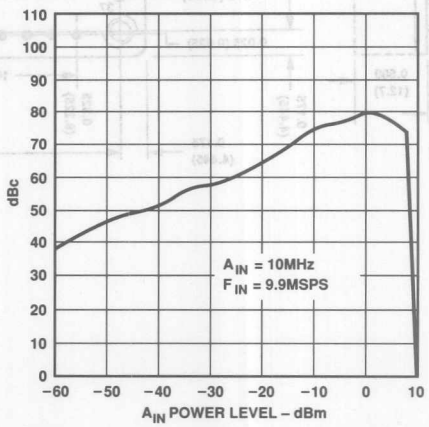


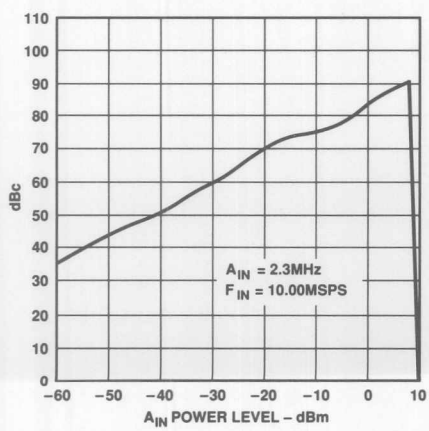


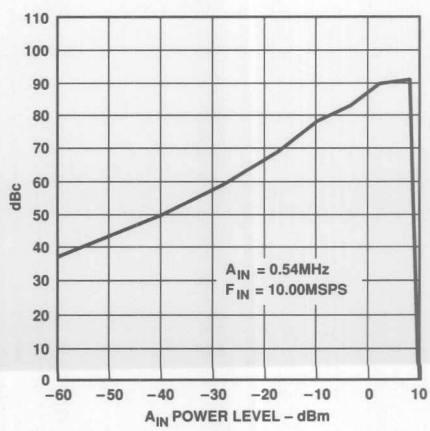


AD9014K TYPICAL PERFORMANCE
SPURIOUS FREE DYNAMIC RANGE (SFDR) VS. INPUT POWER LEVEL



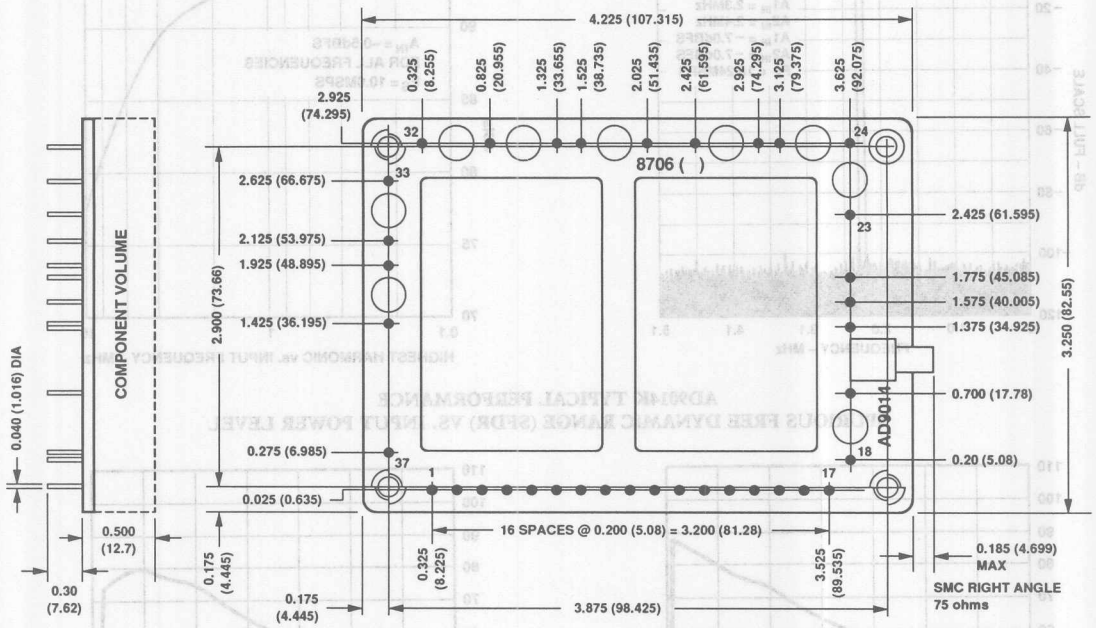






OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AD9020

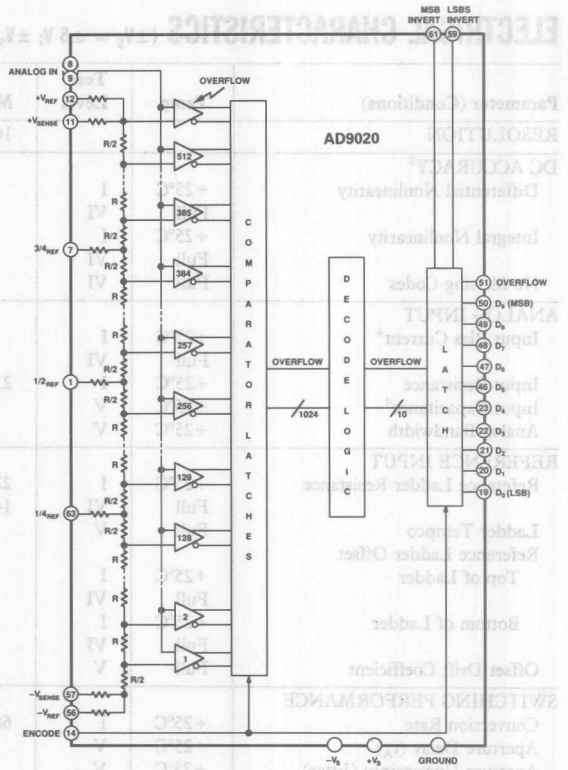
FEATURES

- Monolithic 10-Bit/60 MSPS Converter
- TTL Outputs
- Bipolar (±1.75 V) Analog Input
- 56 dB SNR @ 2.3 MHz Input
- Low (45 pF) Input Capacitance
- MIL-STD-883 Compliant Versions Available

APPLICATIONS

- Digital Oscilloscopes
- Medical Imaging
- Professional Video
- Radar Warning/Guidance Systems
- Infrared Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9020 A/D converter is a 10-bit monolithic converter capable of word rates of 60 MSPS and above. Innovative architecture using 512 input comparators instead of the traditional 1024 required by other flash converters reduces input capacitance and improves linearity.

Encode and outputs are TTL-compatible, making the AD9020 an ideal candidate for use in low power systems. An overflow bit is provided to indicate analog input signals greater than $+V_{SENSE}$.

Voltage sense lines are provided to insure accurate driving of the $\pm V_{REF}$ voltages applied to the units. Quarter-point taps on the resistor ladder help optimize the integral linearity of the unit.

Either 68-pin ceramic leaded (gull wing) packages or ceramic LCCs are available and are specifically designed for low thermal impedances. Two performance grades for temperatures of both 0 to +70°C and −55°C to +125°C ranges are offered to allow the user to select the linearity best suited for each application. Dynamic performance is fully characterized and production tested at +25°C. MIL-STD-883 units are available.

The AD9020 A/D Converter is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD9020/883B data sheet for detailed specifications.

$+V_S$	
$-V_S$	−6 V
ANALOG IN	−2 V to +2 V
$+V_{REF}$, $-V_{REF}$, $3/4_{REF}$, $1/2_{REF}$, $1/4_{REF}$	−2 V to +2 V
$+V_{REF}$ to $-V_{REF}$	4.0 V
DIGITAL INPUTS	−0.5 V to $+V_S$

Operating Temperature	
AD9020JE/KE/JZ/KZ	0 to +70°C
Storage Temperature	−65°C to +150°C
Maximum Junction Temperature[2]	+175°C
Lead Soldering Temp (10 sec)	+300°C

ELECTRICAL CHARACTERISTICS ($\pm V_S$ = ±5 V; $\pm V_{SENSE}$ = ±1.75 V; ENCODE = 40 MSPS unless otherwise noted)[3]

Parameter (Conditions)	Temp	Test Level	AD9020JE/JZ Min	AD9020JE/JZ Typ	AD9020JE/JZ Max	AD9020KE/KZ Min	AD9020KE/KZ Typ	AD9020KE/KZ Max	Units
RESOLUTION			10			10			Bits
DC ACCURACY[3]									
Differential Nonlinearity	+25°C	I		1.0	1.25		0.75	1.0	LSB
	Full	VI			1.5			1.25	LSB
Integral Nonlinearity	+25°C	I		1.25	2.0		1.0	1.5	LSB
	Full	VI			2.5			2.0	LSB
No Missing Codes	Full	VI					Guaranteed		
ANALOG INPUT									
Input Bias Current[4]	+25°C	I		0.4	1.0		0.4	1.0	mA
	Full	VI			2.0			2.0	mA
Input Resistance	+25°C	I	2.0	7.0		2.0	7.0		kΩ
Input Capacitance[4]	+25°C	V		45			45		pF
Analog Bandwidth	+25°C	V		175			175		MHz
REFERENCE INPUT									
Reference Ladder Resistance	+25°C	I	22	37	56	22	37	56	Ω
	Full	VI	14		66	14		66	Ω
Ladder Tempco	Full	V		0.1			0.1		Ω/°C
Reference Ladder Offset									
Top of Ladder	+25°C	I		45	90		45	90	mV
	Full	VI			90			90	mV
Bottom of Ladder	+25°C	I		45	90		45	90	mV
	Full	VI			90			90	mV
Offset Drift Coefficient	Full	V		50			50		µV/°C
SWITCHING PERFORMANCE									
Conversion Rate	+25°C	I	60			60			MSPS
Aperture Delay (t_A)	+25°C	V		1			1		ns
Aperture Uncertainty (Jitter)	+25°C	V		5			5		ps, rms
Output Delay (t_{OD})[5]	+25°C	I	6	10	13	6	10	13	ns
Output Time Skew[5]	+25°C	I		3	5		3	5	ns
DYNAMIC PERFORMANCE									
Transient Response	+25°C	V		10			10		ns
Overvoltage Recovery Time	+25°C	V		10			10		ns
Effective Number of Bits (ENOB)									
f_{IN} = 2.3 MHz	+25°C	I	8.6	9.0		8.6	9.0		Bits
f_{IN} = 10.3 MHz	+25°C	IV	8.0	8.4		8.0	8.4		Bits
f_{IN} = 15.3 MHz	+25°C	IV	7.5	8.0		7.5	8.0		Bits
Signal-to-Noise Ratio[6]									
f_{IN} = 2.3 MHz	+25°C	I	54	56		54	56		dB
f_{IN} = 10.3 MHz	+25°C	I	50	53		50	53		dB
f_{IN} = 15.3 MHz	+25°C	I	47	50		47	50		dB
Signal-to-Noise Ratio[6] (Without Harmonics)									
f_{IN} = 2.3 MHz	+25°C	I	54	56		54	56		dB
f_{IN} = 10.3 MHz	+25°C	I	51	54		51	54		dB
f_{IN} = 15.3 MHz	+25°C	I	48	52		48	52		dB

Parameter (Conditions)	Temp	Test Level	AD9020JE/JZ Min	AD9020JE/JZ Typ	AD9020JE/JZ Max	AD9020KE/KZ Min	AD9020KE/KZ Typ	AD9020KE/KZ Max	Units
DYNAMIC PERFORMANCE (CONTINUED)									
Harmonic Distortion									
f_{IN} = 2.3 MHz	+25°C	I	61	67		61	67		dBc
f_{IN} = 10.3 MHz	+25°C	I	55	59		55	59		dBc
f_{IN} = 15.3 MHz	+25°C	I	49	53		49	53		dBc
Two-Tone Intermodulation Distortion Rejection[7]	+25°C	V		70			70		dBc
Differential Phase	+25°C	V		0.5			0.5		Degree
Differential Gain	+25°C	V		1			1		%
ENCODE INPUT									
Logic "1" Voltage	Full	VI	2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8	V
Logic "1" Current	Full	VI			20			20	μA
Logic "0" Current	Full	VI			800			800	μA
Input Capacitance	+25°C	V		5			5		pF
Pulse Width (High)	+25°C	I	6			6			ns
Pulse Width (Low)	+25°C	I	6			6			ns
DIGITAL OUTPUTS									
Logic "1" Voltage (I_{OH} = 2 mA)	Full	VI	2.4			2.4			V
Logic "0" Voltage (I_{OL} = 10 mA)	Full	VI			0.4				V
POWER SUPPLY									
$+V_S$ Supply Current	+25°C	I		440	530		440	530	mA
	Full	VI			542			542	mA
$-V_S$ Supply Current	+25°C	I		140	170		140	170	mA
	Full	VI			177			177	mA
Power Dissipation	+25°C	I		2.8	3.3		2.8	3.3	W
	Full	VI			3.4			3.4	W
Power Supply Rejection Ratio (PSRR)[8]	Full	VI		6	10		6	10	mV/V

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances (part soldered onto board): 68-pin leaded ceramic chip carrier: θ_{JC} = 1°C/W; θ_{JA} = 17°C/W (no air flow); θ_{JA} = 15°C/W (air flow = 500 LFM). 68-pin ceramic LCC: θ_{JC} = 2.6°C/W; θ_{JA} = 15°C/W (no air flow); θ_{JA} = 13°C/W (air flow = 500 LFM).

[3]$3/4_{REF}$, $1/2_{REF}$, and $1/4_{REF}$ reference ladder taps are driven from dc sources at +0.875 V, 0 V, and −0.875 V, respectively. Accuracy of the overflow comparator is not tested and not included in linearity specifications.

[4]Measured with ANALOG IN = $+V_{SENSE}$.

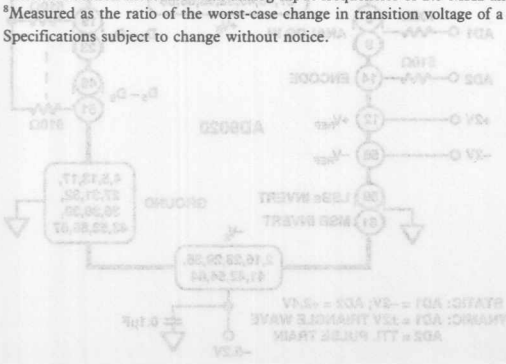
[5]Output delay measured as worst-case time from 50% point of the rising edge of ENCODE to 50% point of the slowest rising or falling edge of D_0–D_9. Output skew measured as worst-case difference in output delay among D_0–D_9.

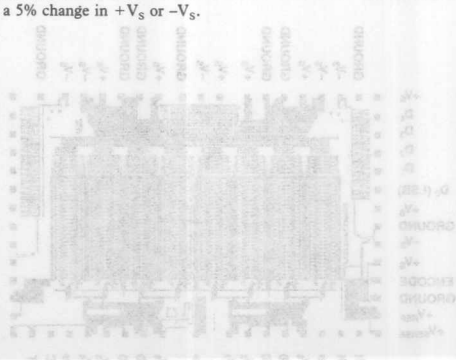
[6]RMS signal to rms noise with analog input signal 1 dB below full scale at specified frequency.

[7]Intermodulation measured with analog input frequencies of 2.3 MHz and 3.0 MHz at 7 dB below full scale.

[8]Measured as the ratio of the worst-case change in transition voltage of a single comparator for a 5% change in $+V_S$ or $-V_S$.

Specifications subject to change without notice.





EXPLANATION OF TEST LEVELS
Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

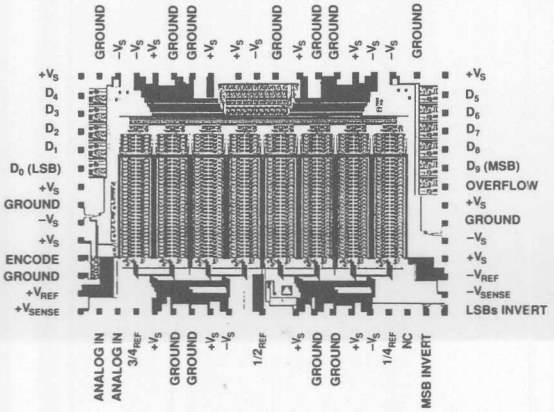
ORDERING GUIDE

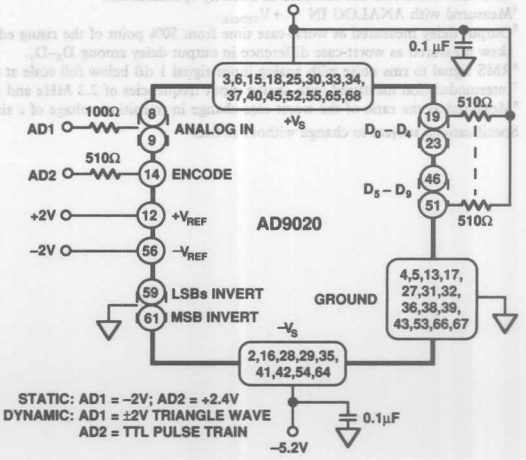
Device	Temperature Range	Description	Package Option*
AD9020JZ	0 to +70°C	68-Pin Leaded Ceramic	Z-68
AD9020JE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9020KZ	0 to +70°C	68-Pin Leaded Ceramic	Z-68
AD9020KE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9020SZ/883	−55°C to +125°C	68-Pin Leaded Ceramic	Z-68
AD9020SE/883	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9020TZ/883	−55°C to +125°C	68-Pin Leaded Ceramic	Z-68
AD9020TE/883	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9020/PCB	0 to +70°C	Evaluation Board	

*E = Ceramic Leadless Chip Carrier; Z = Ceramic Leaded Chip Carrier.
For outline information see Package Information section.

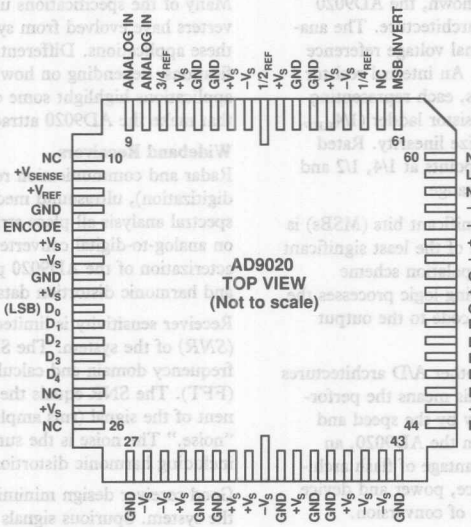
DIE LAYOUT AND MECHANICAL INFORMATION

Die Dimensions . . . . . 206 × 140 × 15 (±2) mils
Pad Dimensions . . . . . 4 × 4 mils
Metalization . . . . . Gold
Backing . . . . . None
Substrate Potential . . . . . $-V_S$
Passivation . . . . . Nitride





AD9020 Burn-In Circuit



AD9020 Pin Designations

AD9020 PIN DESCRIPTIONS

Pin No.	Name	Function
1	$1/2_{REF}$	Midpoint of internal reference ladder.
2, 16, 28, 29, 35, 41, 42, 54, 64	$-V_S$	Negative supply voltage; nominally −5.0 V ±5%.
3, 6, 15, 18, 25, 30, 33, 34, 37, 40, 45, 52, 55, 65, 68	$+V_S$	Positive supply voltage; nominally +5 V ±5%.
4, 5, 13, 17, 27, 31, 32 36, 38, 39, 43, 53, 66, 67	GROUND	All ground pins should be connected together and to low-impedance ground plane.
7	$3/4_{REF}$	Three-quarter point of internal reference ladder.
8, 9	ANALOG IN	Analog input; nominally between ±1.75 V.
11	$+V_{SENSE}$	Voltage sense line to most positive point on internal resistor ladder. Normally +1.75 V.
12	$+V_{REF}$	Voltage force connection for top of internal reference ladder. Normally driven to provide +1.75 V at $+V_{SENSE}$.
14	ENCODE	TTL-compatible convert command used to begin digitizing process.
19–23, 46–50	D_0–D_9	TTL-compatible digital output data.
51	OVERFLOW	TTL-compatible output indicating ANALOG IN > $+V_{SENSE}$.
56	$-V_{REF}$	Voltage force connection for bottom of internal reference ladder. Normally driven to provide −1.75 V at $-V_{SENSE}$.
57	$-V_{SENSE}$	Voltage sense line to most negative point on internal resistor ladder. Normally −1.75 V.
59	LSBs INVERT	Normally grounded. When connected to $+V_S$, lower order bits (D_0–D_8) are inverted.
61	MSB INVERT	Normally grounded. When connected to $+V_S$, most significant bit (MSB; D_9) is inverted.
63	$1/4_{REF}$	One-quarter point of internal reference ladder.

THEORY OF OPERATION

Refer to the AD9020 block diagram. As shown, the AD9020 uses a modified "flash", or parallel, A/D architecture. The analog input range is determined by an external voltage reference ($+V_{REF}$ and $-V_{REF}$), nominally ±1.75 V. An internal resistor ladder divides this reference into 512 steps, each representing two quantization levels. Taps along the resistor ladder ($1/4_{REF}$, $1/2_{REF}$ and $3/4_{REF}$) are provided to optimize linearity. Rated performance is achieved by driving these points at 1/4, 1/2 and 3/4, respectively, of the voltage reference range.

The A/D conversion for the nine most significant bits (MSBs) is performed by 512 comparators. The value of the least significant bit (LSB) is determined by a unique interpolation scheme between adjacent comparators. The decoding logic processes the comparator outputs and provides a 10-bit code to the output stage of the converter.

Flash architecture has an advantage over other A/D architectures because conversion occurs in one step. This means the performance of the converter is limited primarily by the speed and matching of the individual comparators. In the AD9020, an innovative interpolation scheme takes advantage of flash architecture but minimizes the input capacitance, power and device count usually associated with that method of conversion.

These advantages occur because of using only half the normal number of input comparator cells to accomplish the conversion. In addition, a proprietary decoding scheme minimizes error codes. Input control pins allow the user to select from among Binary, Inverted Binary, Twos Complement and Inverted Twos Complement coding (See AD9020 Truth Table).

APPLICATIONS

Many of the specifications used to describe analog/digital converters have evolved from system performance requirements in these applications. Different systems emphasize particular specifications, depending on how the part is used. The following applications highlight some of the specifications and features that make the AD9020 attractive in these systems.

Wideband Receivers

Radar and communication receivers (baseband and direct IF digitization), ultrasound medical imaging, signal intelligence and spectral analysis all place stringent ac performance requirements on analog-to-digital converters (ADCs). Frequency domain characterization of the AD9020 provides signal-to-noise ratio (SNR) and harmonic distortion data to simplify selection of the ADC.

Receiver sensitivity is limited by the *Signal-to-Noise Ratio (SNR)* of the system. The SNR for an ADC is measured in the frequency domain and calculated with a Fast Fourier Transform (FFT). The SNR equals the ratio of the fundamental component of the signal (rms amplitude) to the rms value of the "noise." The noise is the sum of all other spectral components, including harmonic distortion, but excluding dc.

Good receiver design minimizes the level of spurious signals in the system. Spurious signals developed in the ADC are the result of imperfections in the device transfer function (nonlinearities, delay mismatch, varying input impedance, etc.). In the ADC, these spurious signals appear as Harmonic Distortion. Harmonic Distortion is also measured with an FFT and is specified as the ratio of the fundamental component of the signal (rms amplitude) to the rms value of the worst case harmonic (usually the 2nd or 3rd).

Two-Tone Intermodulation Distortion (IMD) is a frequently cited specification in receiver design. In narrow-band receivers, third-order IMD products result in spurious signals in the pass band of the receiver. Like mixers and amplifiers, the ADC is characterized with two, equal-amplitude, pure input frequencies. The IMD equals the ratio of the power of either of the two input signals to the power of the strongest third-order IMD signal. Unlike mixers and amplifiers, the IMD does not always behave as it does in linear devices (reduced input levels do not result in predictable reductions in IMD).

Performance graphs provide typical harmonic and SNR data for the AD9020 for increasing analog input frequencies. In choosing an A/D converter, always look at the dynamic range for the analog input frequency of interest. The AD9020 specifications provide guaranteed minimum limits at three analog test frequencies.

Aperture Delay is the delay between the rising edge of the ENCODE command and the instant at which the analog input is sampled. Many systems require simultaneous sampling of more than one analog input signal with multiple ADCs. In these situations, timing is critical and the absolute value of the aperture delay is not as critical as the matching between devices.

Aperture Uncertainty, or jitter, is the sample-to-sample variation in aperture delay. This is especially important when sampling high slew rate signals in wide bandwidth systems. Aperture uncertainty is one of the factors which degrades dynamic performance as the analog input frequency is increased.

Digitizing Oscilloscopes

Oscilloscopes provide amplitude information about an observed waveform with respect to time. Digitizing oscilloscopes must accurately sample this signal, without distorting the information to be displayed.

One figure of merit for the ADC in these applications is *Effective Number of Bits (ENOBs)*. ENOB is calculated with a sine wave curve fit and equals:

$$ENOB = N - LOG_2 [Error\ (measured)/Error\ (ideal)]$$

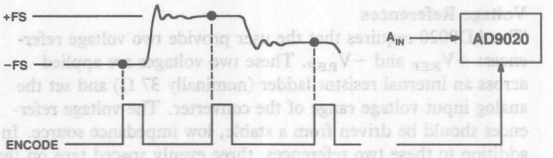
N is the resolution (number of bits) of the ADC. The measured error is the actual rms error calculated from the converter outputs with a pure sine wave input.

The *Analog Bandwidth* of the converter is the analog input frequency at which the spectral power of the fundamental signal is reduced 3 dB from its low frequency value. The analog bandwidth is a good indicator of a converter's slewing capabilities.

The *Maximum Conversion Rate* is defined as the encode rate at which the SNR for the lowest analog signal test frequency tested drops by no more than 3 dB below the guaranteed limit.

Imaging

Visible and infrared imaging systems both require similar characteristics from ADCs. The signal input (from a CCD camera, or multiplexer) is a time division multiplexed signal consisting of a series of pulses whose amplitude varies in direct proportion to the intensity of the radiation detected at the sensor. These varying levels are then digitized by applying encode commands at the correct times, as shown below.



Imaging Application Using AD9020

The actual resolution of the converter is limited by the thermal and quantization noise of the ADC. The low frequency test for SNR or ENOB is a good measure of the noise of the AD9020. At this frequency, the static errors in the ADC determine the useful dynamic range of the ADC.

Although the signal being sampled does not have a significant slew rate, this does not imply dynamic performance is not important. The *Transient Response and Overvoltage Recovery Time* specifications insure that the ADC can track full-scale changes in the analog input sufficiently fast to capture a valid sample.

Transient Response is the time required for the AD9020 to achieve full accuracy when a step function is applied. *Overvoltage Recovery Time* is the time required for the AD9020 to recover to full accuracy after an analog input signal 150% of full scale is reduced to the full-scale range of the converter.

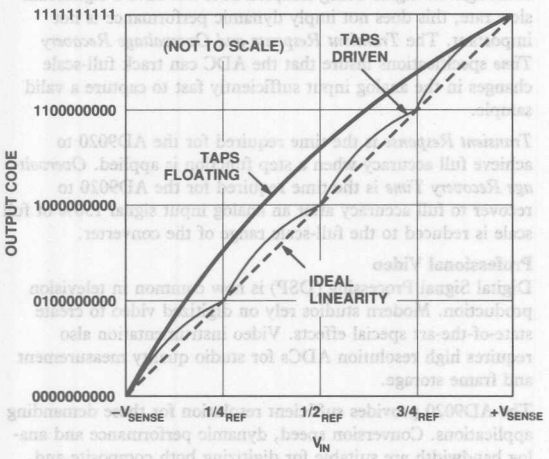
Professional Video

Digital Signal Processing (DSP) is now common in television production. Modern studios rely on digitized video to create state-of-the-art special effects. Video instrumentation also requires high resolution ADCs for studio quality measurement and frame storage.

The AD9020 provides sufficient resolution for these demanding applications. Conversion speed, dynamic performance and analog bandwidth are suitable for digitizing both composite and RGB video sources.

Voltage References

The AD9020 requires that the user provide two voltage references: $+V_{REF}$ and $-V_{REF}$. These two voltages are applied across an internal resistor ladder (nominally 37 Ω) and set the analog input voltage range of the converter. The voltage references should be driven from a stable, low impedance source. In addition to these two references, three evenly spaced taps on the resistor ladder ($1/4_{REF}$, $1/2_{REF}$, $3/4_{REF}$) are available. Providing a reference to these quarter points on the resistor ladder will improve the integral linearity of the converter and improve ac performance. (AC and dc specifications are tested while driving the quarter points at the indicated levels.) The figure below is not intended to show the transfer function of the ADC, but illustrates how the linearity of the device is affected by reference voltages applied to the ladder.



Effect of Reference Taps on Linearity

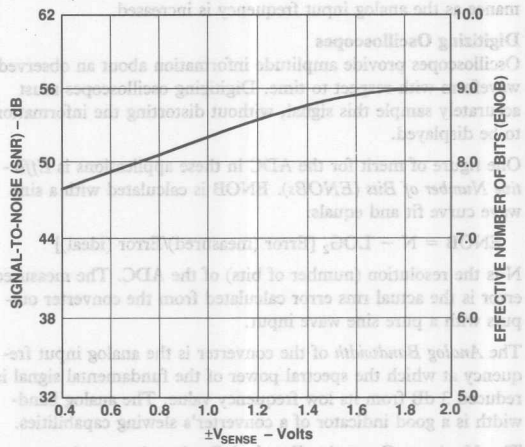
Resistance between the reference connections and the taps of the first and last comparators causes offset errors. These errors, called "top and bottom of the ladder offsets," can be nulled by using the voltage sense lines, $+V_{SENSE}$ and $-V_{SENSE}$, to adjust the reference voltages. Current through the sense lines should be limited to less than 100 μA. Excessive current drawn through the voltage sense lines will affect the accuracy of the sense line voltage.

The next page shows a reference circuit which nulls out the offset errors using two op amps and provides appropriate voltage references to the quarter-point taps. Feedback from the sense lines causes the op amps to compensate for the offset errors. The two transistors limit the amount of current drawn directly from the op amps; resistors at the base connections stabilize their operation. The 10 kΩ resistors (R1–R4) between the voltage sense lines form an external resistor ladder; the quarter point voltages are taken off this external ladder and buffered by an op amp. The actual values of resistors R1–R4 are not critical, but they should match well and be large enough (≥10 kΩ) to limit the amount of current drawn from the voltage sense lines.

be a potentiometer) are chosen to adjust the quarter-point voltage references, but are not necessary if R1–R4 match within 0.05%.

An alternative approach for defining the quarter-point references of the resistor ladder is to evaluate the integral linearity error of an individual device, and adjust the voltage at the quarter-points to minimize this error. This may improve the low frequency ac performance of the converter.

Performance of the AD9020 has been optimized with an analog input voltage of ±1.75 V (as measured at $\pm V_{SENSE}$). If the analog input range is reduced below these values, relatively larger differential nonlinearity errors may result because of comparator mismatches. As shown in the figure below, performance of the converter is a function of $\pm V_{SENSE}$.



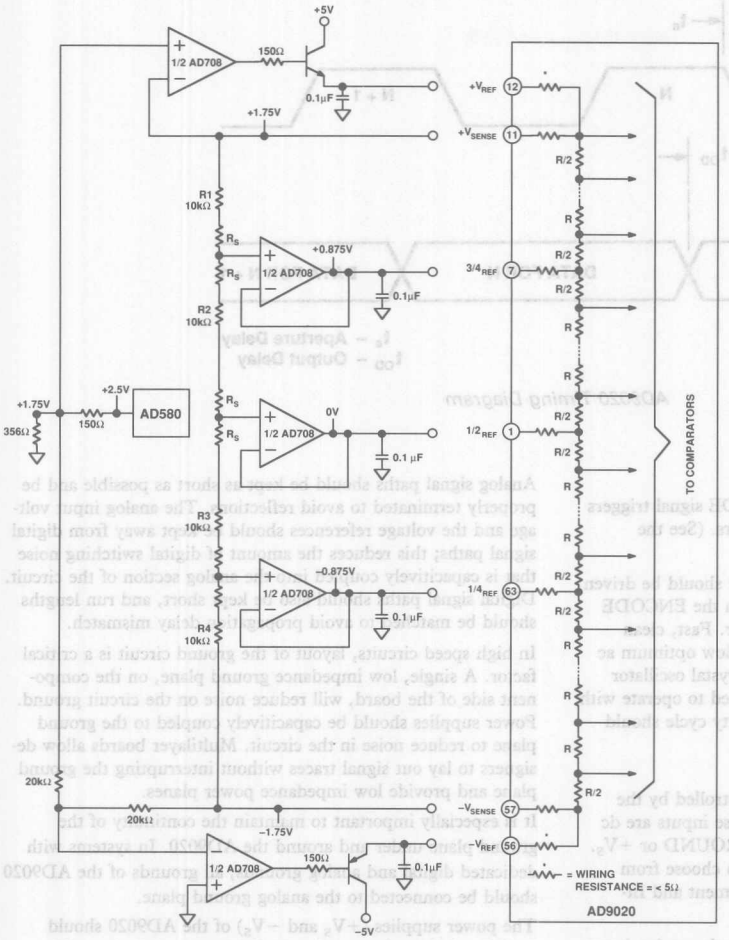
AD9020 SNR and ENOB vs. Reference Voltage

Applying a voltage greater than 4 V across the internal resistor ladder will cause current densities to exceed rated values, and may cause permanent damage to the AD9020. The design of the reference circuit should limit the voltage available to the references.

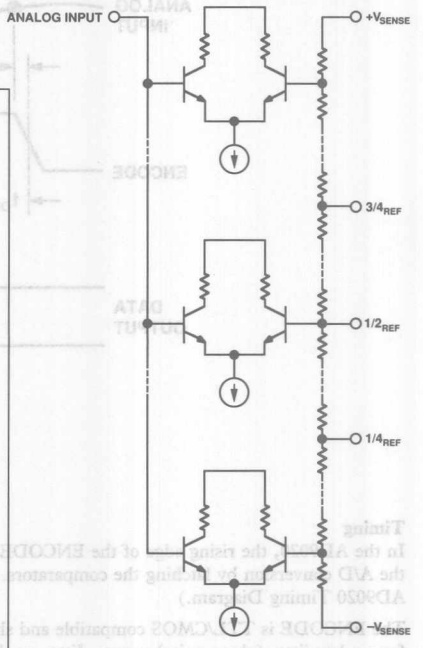
Analog Input Signal

The signal applied to ANALOG IN drives the inputs of 512 parallel comparator cells (see Equivalent Analog Input figure). This connection typically has an input resistance of 7 kΩ, and input capacitance of 45 pF. The input capacitance is nearly constant over the analog input voltage range, as shown in the graph which illustrates that characteristic.

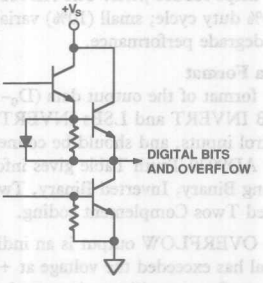
The analog input signal should be driven from a low distortion, low noise amplifier. A good choice is the AD9617, a wide bandwidth, monolithic operational amplifier with excellent ac and dc performance. The input capacitance should be isolated by a small series resistor (24 Ω for the AD9617) to improve the ac performance of the amplifier (see AD9020/PCB Evaluation Board Block Diagram).



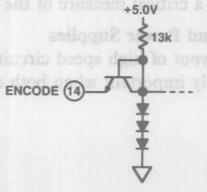
AD9020 Reference Circuit



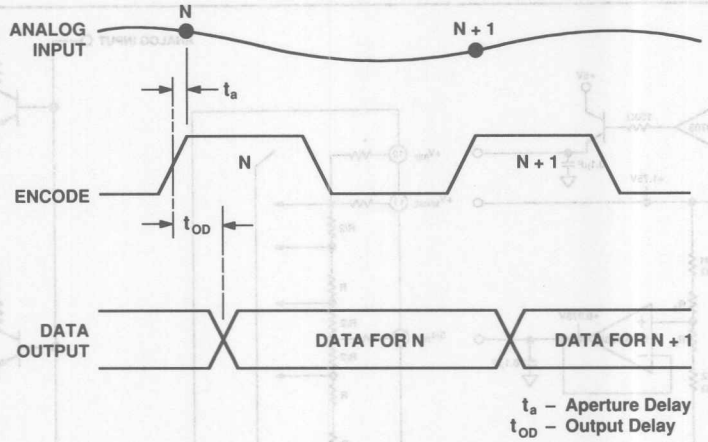
AD9020 Equivalent Analog Input



AD9020 Equivalent Digital Outputs



AD9020 Equivalent Encode Circuit



AD9020 Timing Diagram

Timing

In the AD9020, the rising edge of the ENCODE signal triggers the A/D conversion by latching the comparators. (See the AD9020 Timing Diagram.)

The ENCODE is TTL/CMOS compatible and should be driven from a low jitter (phase noise) source. Jitter on the ENCODE signal will raise the noise floor of the converter. Fast, clean edges will reduce the jitter in the signal and allow optimum ac performance. Locking the system clock to a crystal oscillator also helps reduce jitter. The AD9020 is designed to operate with a 50% duty cycle; small (10%) variations in duty cycle should not degrade performance.

Data Format

The format of the output data (D_0– D_9) is controlled by the MSB INVERT and LSBs INVERT pins. These inputs are dc control inputs, and should be connected to GROUND or $+V_S$. The AD9020 Truth Table gives information to choose from among Binary, Inverted Binary, Twos Complement and Inverted Twos Complement coding.

The OVERFLOW output is an indication that the analog input signal has exceeded the voltage at $+V_{SENSE}$. The accuracy of the overflow transition voltage and output delay are not tested or included in the data sheet limits. Performance of the overflow indicator is dependent on circuit layout and slew rate of the encode signal. The operation of this function does not affect the other data bits (D_0–D_9). It is not recommended for applications requiring a critical measure of the analog input voltage.

Layout and Power Supplies

Proper layout of high speed circuits is always critical but is particularly important when both analog and digital signals are involved.

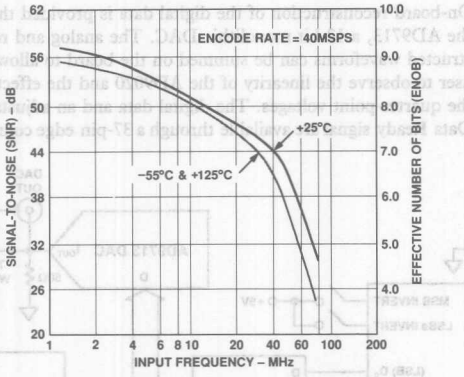
Analog signal paths should be kept as short as possible and be properly terminated to avoid reflections. The analog input voltage and the voltage references should be kept away from digital signal paths; this reduces the amount of digital switching noise that is capacitively coupled into the analog section of the circuit. Digital signal paths should also be kept short, and run lengths should be matched to avoid propagation delay mismatch.

In high speed circuits, layout of the ground circuit is a critical factor. A single, low impedance ground plane, on the component side of the board, will reduce noise on the circuit ground. Power supplies should be capacitively coupled to the ground plane to reduce noise in the circuit. Multilayer boards allow designers to lay out signal traces without interrupting the ground plane and provide low impedance power planes.

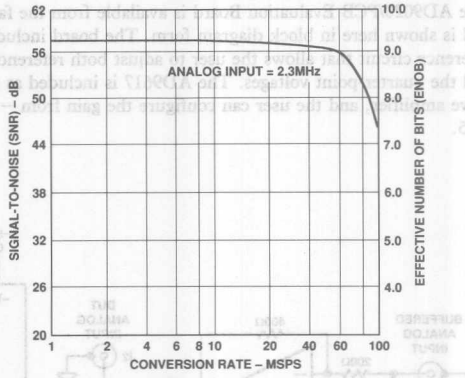
It is especially important to maintain the continuity of the ground plane under and around the AD9020. In systems with dedicated digital and analog grounds, all grounds of the AD9020 should be connected to the analog ground plane.

The power supplies ($+V_S$ and $-V_S$) of the AD9020 should be isolated from the supplies used for external devices; this further reduces the amount of noise coupled into the A/D converter. Sockets limit the dynamic performance and should be used only for prototypes or evaluation—PCK Elastomerics Part # CCS-68-55 is recommended for the LCC package. (Tel. 215-672-0787)

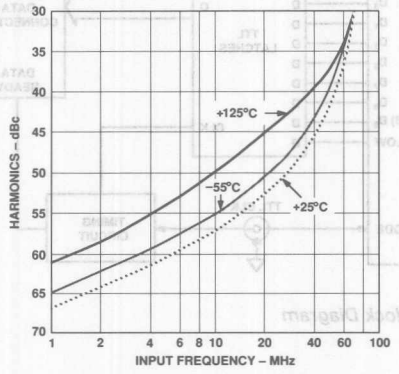
An evaluation board is available to aid designers and provide a suggested layout.



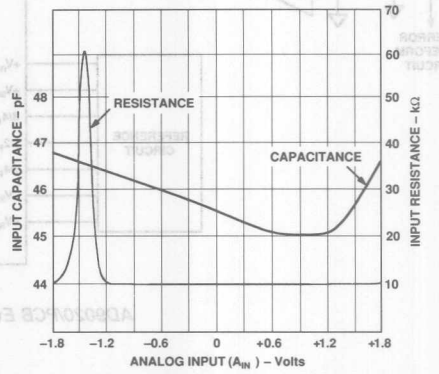
AD9020 SNR and ENOB vs. Input Frequency



AD9020 SNR and ENOB vs. Conversion Rate



AD9020 Harmonics vs. Input Frequency



Input Capacitance/Resistance vs. Input Voltage

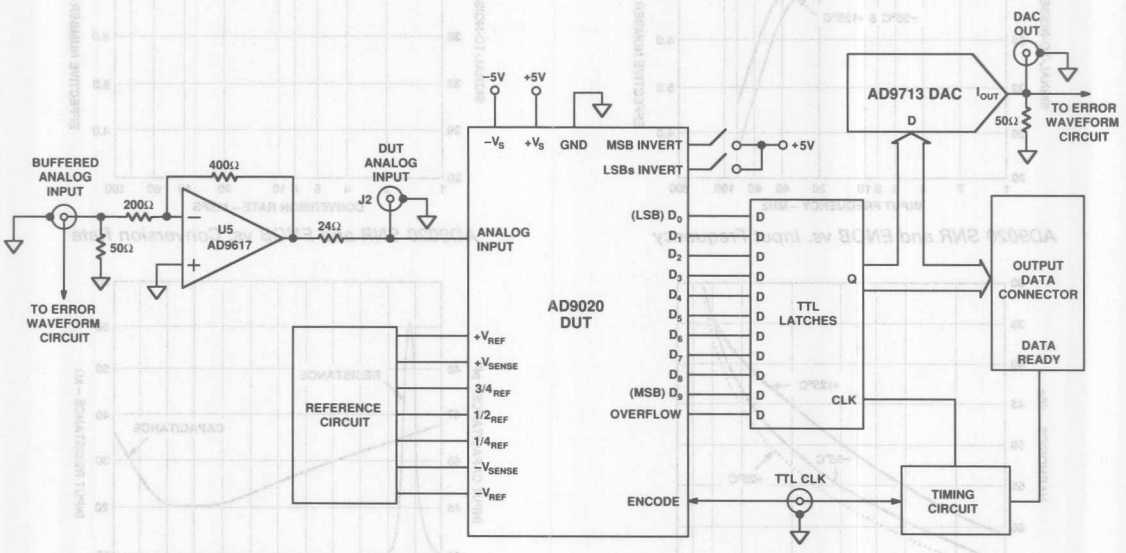
Step	Range	Offset Binary		Twos Complement	
		True	Inverted	True	Inverted
	0 = −1.75 V FS = +1.75 V	MSB INV = "0" LSBs INV = "0"	MSB INV = "1" LSBs INV = "1"	MSB INV = "1" LSBs INV = "0"	MSB INV = "0" LSBs INV = "1"
1024	>+1.7500	(1)1111111111	(1)0000000000	(1)0111111111	(1)1000000000
1023	+1.7466	1111111111	0000000000	0111111111	1000000000
1022	+1.7432	1111111110	0000000001	0111111110	1000000001
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
512	+0.0034	1000000000	0111111111	0000000000	1111111111
511	0.000	0111111111	1000000000	1111111111	0000000000
510	−0.0034	0111111110	1000000001	1111111110	0000000001
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
02	−1.7432	0000000010	1111111101	1000000010	0111111101
01	−1.7466	0000000001	1111111110	1000000001	0111111110
00	<−1.7466	0000000000	1111111111	1000000000	0111111111

The overflow bit is always 0 except where noted in parentheses ( ). MSB INVERT and LSBs INVERT are considered dc controls.

AD9020 Truth Table

The AD9020/PCB Evaluation Board is available from the factory and is shown here in block diagram form. The board includes a reference circuit that allows the user to adjust both references and the quarter-point voltages. The AD9617 is included as the drive amplifier, and the user can configure the gain from −1 to −15.

On-board reconstruction of the digital data is provided through the AD9713, a 12-bit monolithic DAC. The analog and reconstructed waveforms can be summed on the board to allow the user to observe the linearity of the AD9020 and the effects of the quarter-point voltages. The digital data and an adjustable Data Ready signal are available through a 37-pin edge connector.



AD9020/PCB Evaluation Board Block Diagram

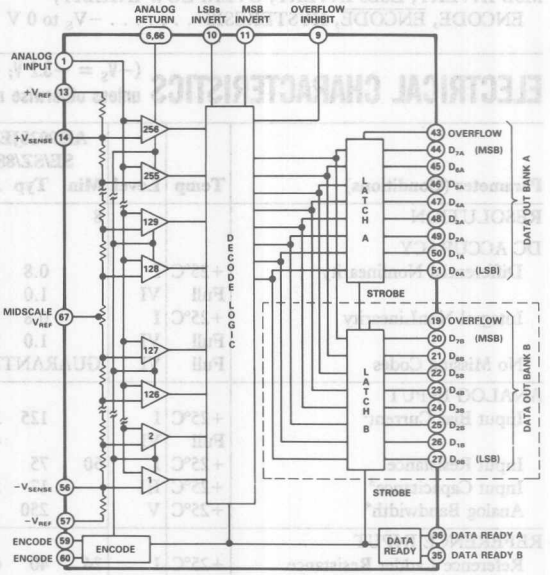
High Speed 8-Bit A/D Converters

AD9028/AD9038

FEATURES
300 MSPS Encode Rate
250 MHz Large Signal Input Bandwidth
Low Input Capacitance: 17 pF
Excellent SNR
Single −5.2 V Power Supply
Overflow Bit & Bit Invert Functions
1:2 Demultiplexed Outputs (AD9038)
MIL-STD-883-Compliant Versions Available

APPLICATIONS
Digital Oscilloscopes
Waveform Digitizers
Radar Receivers
Electronic Countermeasures

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9028 and AD9038 are ECL-compatible 8-bit, high speed flash analog-to-digital converters. Both are fabricated in an advanced bipolar VLSI process which ensures exceptionally wide analog input bandwidth (250 MHz) and encode rates up to 300 MSPS.

Output data for the AD9028 include Overflow and Data Ready signals; control pins allow the user to invert the MSB and/or LSBs. The AD9038 combines the features of the AD9028 with on-board demultiplexing circuits to provide two sets of output data. These ease the task of interfacing the converter by reducing the data rate to half the encode rate.

The analog input is designed for 0 to −2.0 volt operation. Sense pins for the $+V_{REF}$ and $-V_{REF}$ inputs allow full-scale calibration of the input range; a tap at the midpoint of the reference ladder is available to minimize integral nonlinearity. Dynamic performance is enhanced by driving the ANALOG RETURN pins with a buffered analog input; see the Applications section.

There are two linearity grades of each device. Commercial temperature ranges of 0 to +70°C and military temperature ranges of −55°C to +125°C are available. Both components are offered in a ceramic 68-pin LCC, and a ceramic 68-pin leaded package. These packages are specially designed for low thermal impedance.

The AD9028/AD9038 A/D Converter is available in versions compliant with MIL-STD-883. Refer to the *Analog Devices Military Products Databook* or current AD9028/AD9038/883B data sheet for detailed specifications.

AD9028/AD9038—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

ANALOG INPUT . . . . . $-V_S$ to +0.5 V
ANALOG RETURN . . . . . 0 V to +2.0 V
$-V_S$ to GROUND . . . . . +0.5 V dc to −6.0 V dc
$+V_{REF}$, $-V_{REF}$, MIDSCALE V_{REF} . . . . . −2.1 V to +0.1 V
$+V_{REF}$ to $-V_{REF}$ . . . . . 2.1 V
MIDSCALE V_{REF}, $+V_{SENSE}$, $-V_{SENSE}$ Current . . . . ±4 mA
MSB INVERT, LSBs INVERT, OVERFLOW INHIBIT, ENCODE, $\overline{\text{ENCODE}}$, HYSTERESIS . . . . . $-V_S$ to 0 V
ENCODE to $\overline{\text{ENCODE}}$ . . . . . 4 V
Digital Output Current . . . . . 20 mA
ANALOG $-V_S$ to DIGITAL $-V_S$ . . . . . ±0.5 V
Operating Temperature Range
AD9028/AD9038KE/KZ/JE/JZ . . . . . 0 to +70°C
AD9028/AD9038TE/TZ/SE/SZ/883 . . . . . −55°C to +125°C
Maximum Junction Temperature[2] . . . . . +175°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS ($-V_S = -5.2$ V; $+V_{REF} = 0$ V; $-V_{REF} = -2$ V; ANALOG RETURN = 0 V, unless otherwise noted)

Parameter (Conditions)	Temp	Level	AD9028JE/JZ SE/SZ/883 Min	Typ	Max	AD9028KE/KZ TE/TZ/883 Min	Typ	Max	AD9038JE/JZ SE/SZ/883 Min	Typ	Max	AD9038KE/KZ TE/TZ/883 Min	Typ	Max	Units
RESOLUTION			8			8			8			8			Bits
DC ACCURACY															
Differential Nonlinearity	+25°C	I		0.8	1.0		0.6	0.75		0.8	1.0		0.6	0.75	LSB
	Full	VI		1.0	1.2		0.8	1.0		1.0	1.2		0.8	1.0	LSB
Integral NonLinearity	+25°C	I		0.8	1.0		0.6	0.75		0.8	1.0		0.6	0.75	LSB
	Full	VI		1.0	1.2		0.8	1.0		1.0	1.2		0.8	1.0	LSB
No Missing Codes	Full	VI	GUARANTEED			GUARANTEED									
ANALOG INPUT															
Input Bias Current[3]	+25°C	I		125	250		125	250		125	250		125	250	μA
	Full	VI			400			400			400			400	μA
Input Resistance	+25°C	I	50	75		50	75		50	75		50	75		kΩ
Input Capacitance[3]	+25°C	III		17	21		17	21		17	21		17	21	pF
Analog Bandwidth[4]	+25°C	V		250			250			250			250		MHz
REFERENCE INPUT															
Reference Ladder Resistance	+25°C	I	24	40	60	24	40	60	24	40	60	24	40	60	Ω
	Full	VI	20		75	20		75	20		75	20		75	Ω
Ladder Tempco	Full	V		0.13			0.13			0.13			0.13		Ω/°C
Ref. Input Bandwidth	Full	V		30			30			30			30		MHz
Reference Ladder Offset[4]	+25°C	I		32	45		32	45		32	45		32	45	mV
(Top)	Full	VI			47			47			47			47	mV
Reference Ladder Offset[4]	+25°C	I		26	37		26	37		26	37		26	37	mV
(Bottom)	Full	VI			39			39			39			39	mV
Offset Drift Coefficient	Full	V		20			20			20			20		μV/°C
SWITCHING PERFORMANCE[4, 5]															
Maximum Conversion Rate	+25°C	I	300	325		300	325		300	325		300	325		MSPS
Aperture Delay (t_A)	+25°C	V		1.4			1.4			1.4			1.4		ns
Aperture Uncertainty (Jitter)	+25°C	V		3			3			3			3		ps, rms
Output Delay (t_{OD})	+25°C	I	4.7	6	7.3	4.7	6	7.3	4.7	6	7.3	4.7	6	7.3	ns
Output Rise Time	+25°C	I		1.0	1.6		1.0	1.6		1.0	1.6		1.0	1.6	ns
Output Fall Time	+25°C	I		1.0	1.6		1.0	1.6		1.0	1.6		1.0	1.6	ns
Output Time Skew	+25°C	I		0.25	0.7		0.25	0.7		0.25	0.7		0.25	0.7	ns
Data Ready															
Output Delay (t_{DR})	+25°C	I	4.1	5.4	6.7	4.1	5.4	6.7	4.8	6.1	7.4	4.8	6.1	7.4	ns
ENCODE INPUT															
Logic "1" Voltage	Full	IV	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	IV			−1.5			−1.5			−1.5			−1.5	V
Logic "1" Current	Full	VI		125	285		125	285		125	285		125	285	μA
Logic "0" Current	Full	VI		100	285		100	285		100	285		100	285	μA
Input Capacitance	+25°C	V		3.6			3.6			3.6			3.6		pF
Pulse Width (High)[6]	+25°C	I	1			1			1			1			ns
Pulse Width (Low)[6]	+25°C	I	2			2			2			2			ns

Parameter (Conditions)	Temp	Level	AD9028JE/JZ SE/SZ/883 Min	Typ	Max	AD9028KE/KZ TE/TZ/883 Min	Typ	Max	AD9038JE/JZ SE/SZ/883 Min	Typ	Max	AD9038KE/KZ TE/TZ/883 Min	Typ	Max	Units
DYNAMIC PERFORMANCE[7]															
Transient Response	+25°C	V		3			3			3			3		ns
Overvoltage Recovery Time	+25°C	V		3			3			3			3		ns
Effective Number of Bits (ENOB)															
Analog Input @ 9.3 MHz	+25°C	I	7.0	7.1		7.2	7.5		7.0	7.2		7.2	7.5		Bits
@ 49 MHz	+25°C	I	6.5	7.0		6.5	7.0		6.5	7.0		6.5	7.0		Bits
@ 92 MHz	+25°C	I	5.4	5.8		5.4	5.8		5.4	5.8		5.4	5.8		Bits
In-Band Harmonics															
Analog Input @ 9.3 MHz	+25°C	I	48	53		54	56		48	53		54	56		dBc
@ 49 MHz	+25°C	I	41	48		41	48		41	48		41	48		dBc
@ 92 MHz	+25°C	I	36	40		36	40		36	40		36	40		dBc
Signal-to-Noise Ratio[8]															
Analog Input @ 9.3 MHz	+25°C	I	44	45		45.5	47		44	45		45.5	47		dB
@ 49 MHz	+25°C	I	40	43		40	43		40	43		40	43		dB
@ 92 MHz	+25°C	I	33	36		33	36		33	36		33	36		dB
Signal-to-Noise Ratio[8] (without harmonics)															
Analog Input @ 9.3 MHz	+25°C	I	45.5	48		45.5	48		45.5	48		45.5	48		dB
@ 49 MHz	+25°C	I	43	46		43	46		43	46		43	46		dB
@ 92 MHz	+25°C	I	38	43		38	43		38	43		38	43		dB
Two-Tone Intermodulation Distortion Rejection[9]	+25°C	I	42	49		42	49		42	49		42	49		dB
DIGITAL OUTPUTS[5]															
Logic "1" Voltage	Full	VI	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			1.5			−1.5			1.5	V
POWER SUPPLY															
Analog Return	+25°C	V		14.4			14.4			14.4			14.4		mA
Negative Supply Current	+25°C	I		390	475		390	475		430	495		430	495	mA
($-V_S$ = −5.2 V)	Full	VI			515			515			550			550	mA
Power Dissipation	+25°C	V		2.0			2.0			2.2			2.2		W
Ref. Ladder Dissipation	+25°C	V		100			100			100			100		mW
Power Supply															
Rejection Ratio (PSRR)	+25°C	I		1.2	3		1.2	3		1.2	3		1.2	3	mV/V
Rejection Ratio (PSRR)	+25°C	I		1.2	3		1.2	3		1.2	3		1.2	3	mV/V
Rejection Ratio (PSRR)	+25°C	I		1.2	3		1.2	3		1.2	3		1.2	3	mV/V

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances:68-pin leaded ceramic chip carrier θ_{JA}=31°C/W, θ_{JC}=1.1°C/W; 68-pin ceramic LCC θ_{JA}=36°C/W, θ_{JC}=2.6°C/W.

[3]Measured with analog input = 0 V.

[4]See definitions of specifications.

[5]Outputs terminated through 100 Ω to −2.0 V; C_L<4 pF

[6]ENCODE command rise/fall times should be less than 2.5 ns for normal operation.

[7]Measured at 250 MSPS encode rate; analog return is tied to +1 V dc. (See text and diagrams.)

[8]RMS signal to rms noise with analog input signal 1 dB below full scale at specified frequency.

[9]Intermodulation measured with analog input frequencies of 60 MHz and 70 MHz at 7 dB below full scale.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level		
I	–	100% production tested.
II	–	100% production tested at +25°C, and sample tested at specified temperatures.
III	–	Sample tested only.
IV	–	Parameter is guaranteed by design and characterization testing.
V	–	Parameter is a typical value only.
VI	–	All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

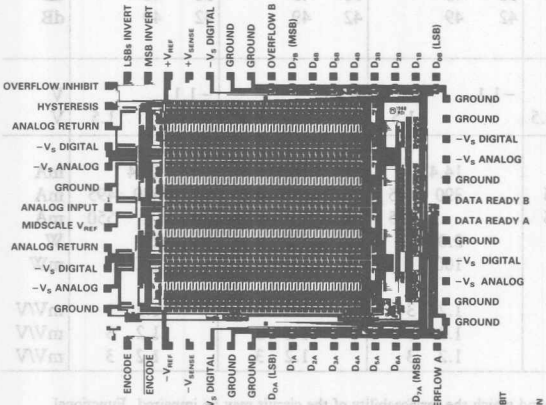
RECOMMENDED OPERATING CONDITIONS

Parameter	Input Voltage Min	Nominal	Max
$-V_S$	−5.46	−5.2	−4.94
$+V_{REF}$	$-V_{REF}$	0	+0.1
$-V_{REF}$	−2.1	−2.0	$+V_{REF}$
ANALOG INPUT	$-V_{REF}$		$+V_{REF}$
ANALOG RETURN	Analog In		Analog In +2.0 V

ORDERING GUIDE

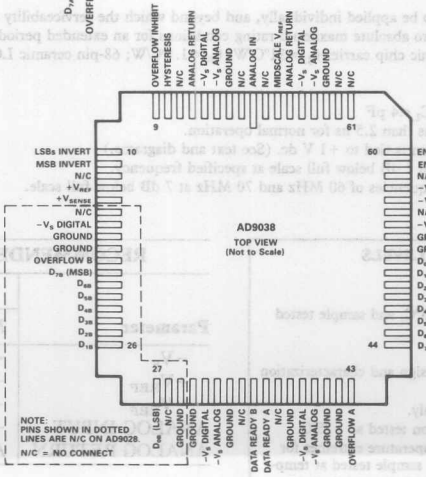
Model	Temperature	Description	Package Option[1]
AD9028JE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9028KE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9028JZ	0 to +70°C	68-Pin Leaded Ceramic	Z-68
AD9028KZ	0 to +70°C	68-Pin Leaded Ceramic	Z-68
AD9028SE/883[2]	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9028TE/883[2]	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9028SZ/883[2]	−55°C to +125°C	68-Pin Leaded Ceramic	Z-68
AD9028TZ/883[2]	−55°C to +125°C	68-Pin Leaded Ceramic	Z-68
AD9038JE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9038KE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9038JZ	0 to +70°C	68-Pin Leaded Ceramic	Z-68
AD9038KZ	0 to +70°C	68-Pin Leaded Ceramic	Z-68
AD9038SE/883[2]	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9038TE/883[2]	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9038SZ/883[2]	−55°C to +125°C	68-Pin Leaded Ceramic	Z-68
AD9038TZ/883[2]	−55°C to +125°C	68-Pin Leaded Ceramic	Z-68

NOTES
[1]E = Ceramic Leadless Chip Carrier; Z = Ceramic Leaded Chip Carrier. For outline information see Package Information section.
[2]For specifications, refer to Analog Devices *Military Products Databook*.



MECHANICAL INFORMATION

Die Dimensions . . . . . .178 × 148 × 15 (±2) mils
Pad Dimensions. . . . . .4 × 4 mils
Metalization . . . . . Gold
Backing . . . . . None
Substrate Potential . . . . . $-V_S$
Passivation . . . . . .Nitride
Die Attach . . . . . .Gold Eutectic
Bond Wire . . . . . 1.3 mil, Gold; Gold Ball Bonding



AD9028/AD9038 Pin Designations
(Note: Chip Cavity Opening Is On Bottom of Package.)

AD9028/AD9038 PIN DESCRIPTIONS

Pin No.	Name	Function
1	ANALOG INPUT	Analog input is nominally between 0 and −2 Volts.
6, 66	ANALOG RETURN	Normally grounded; supplies current to input comparator circuits. Pins can be tied to postive potential (+2.0 V max), or buffered version of analog input to reduce capacitance and enhance dynamic performance. (See Applications.)
36	DATA READY A	Rising edge of signal can be used to externally latch D_{0A}–D_{7A}.
35	DATA READY B	Rising edge of signal can be used to externally latch D_{0B}–D_{7B}.
44–51	D_{7A}–D_{0A}	ECL digital data from Data Bank A.
20–27	D_{7B}–D_{0B}	ECL digital data from Data Bank B.
59, 60	ENCODE, ENCODE	Differential ECL convert signals.
3, 17, 18, 29, 30, 33, 38, 41, 42, 52, 53, 63	GROUND	All ground pins should be connected together.
8	HYSTERESIS	Normally grounded; hysteresis control pin.
10	LSBs INVERT	Normally connected to $-V_S$. When grounded, lower order bits are inverted.
67	MIDSCALE V_{REF}	Normally floating; midpoint of reference resistor ladder. Can be adjusted to minimize integral nonlinearity.
11	MSB INVERT	Normally connected to $-V_S$. When grounded, MSB is inverted.
43	OVERFLOW A	ECL-compatible output indicating ANALOG IN > $+V_{SENSE}$.
19	OVERFLOW B	ECL-compatible output indicating ANALOG IN > $+V_{SENSE}$.
9	OVERFLOW INHIBIT	Normally floating or tied to $-V_S$. When grounded, OVERFLOW A and B are disabled; D0–D7 remain at ECL logic "1" when ANALOG IN > $+V_{SENSE}$.
13	$+V_{REF}$	Normally 0 V; sets voltage reference at top of ladder.
57	$-V_{REF}$	Normally −2 V; sets voltage reference at bottom of ladder.
4, 32, 40, 64	$-V_S$ ANALOG	−5.2 Volts; analog supply voltage.
5, 16, 31, 39, 54, 65	$-V_S$ DIGITAL	−5.2 Volts; digital supply voltage.
14	$+V_{SENSE}$	Voltage sense line to most positive comparator reference input.
56	$-V_{SENSE}$	Voltage sense line to most negative comparator reference input.

DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Data Ready Output Delay
The delay between the 50% point of the falling edge of the ENCODE command and the 50% point of the rising edge of DATA READY A or DATA READY B.

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

Effective Number of Bits (ENOB)
ENOB is a measure of ac linearity and is calculated from a sine wave curve fit according to the following expression:

$$ENOB = N - LOG_2 [\text{ rms error (actual)/rms error (ideal) }]$$

N is the resolution (number of bits) of the converter. The actual rms error is the deviation from an ideal sine wave, calculated from the converter outputs with a sine wave input.

In-Band Harmonics
The rms value of the fundamental divided by the rms value of the worst harmonic.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Maximum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency tested drops by no more than 3 dB below the guaranteed limit.

Output Delay
The delay between the 50% point of the rising edge of the ENCODE command and the 50% point of output data.

Output Time Skew
Bit-to-bit time variations among D0 to D7 outputs. In the AD9028 and AD9038 specifications, time skew includes HIGH-to-LOW and LOW-to-HIGH transitions of the digital output bits.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 8-bit accuracy after an analog input signal 150% of full scale is reduced to the full scale (0 to −2 V) range of the converter.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage. In the AD9028 and AD9038 units, $-V_S$ (−5.2 V) is within ±5% of its nominal value for this test.

DEFINITIONS OF SPECIFICATIONS (continued)

Reference Ladder Offset
The deviation between the top (or bottom) comparator transition voltage as measured at the analog input, and the voltage at the $+V_{REF}$ (or $-V_{REF}$) pin. This is valuable in determining the accuracy and adjustment range for $\pm V_{REF}$ sources.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude to the rms value of "noise," which is defined as the sum of all other spectral components, including harmonics but excluding dc, with an analog input signal 1 dB below full scale.

Transient Response
The time required for the converter to achieve 8-bit accuracy when a step function is applied to the analog input.

Two-Tone Intermodulation Distortion (IMD) Rejection
The ratio of the power of either of two input signals to the power of the strongest third-order IMD signal.

THEORY OF OPERATION

Refer to the AD9038 Block Diagram. Both units use a "flash," or parallel, A/D architecture. The analog input voltage range is determined by an external voltage reference ($+V_{REF}$ and $-V_{REF}$), nominally 0 to −2 V. An internal resistor ladder divides this reference into 255 levels, each representing a single quantization level.

The A/D conversion, triggered by the ENCODE signal, is performed by 255 comparators. The output of the comparators indicates the appropriate quantization level of the analog input signal. The decoding logic processes the comparator outputs and provides an 8-bit code to the output stage.

Flash architecture has an advantage over other A/D architectures because the conversion occurs in one step, and the performance of the converter is limited primarily by the speed and matching of the individual comparators. A state-of-the-art bipolar process and careful comparator design give the AD9028/AD9038 excellent ac performance. A proprietary decoding scheme minimizes error codes, and control pins allow the user to select among Binary, Inverted Binary, Twos Complement and Inverted Twos Complement coding.

APPLICATIONS

Voltage References
The AD9028/AD9038 requires that the user provide two voltage references: $+V_{REF}$ and $-V_{REF}$, as shown in Figure 1. These two voltages are applied across an internal resistor ladder (nominally 40 Ω) and set the analog input voltage range of the converter. Each voltage reference should be driven from a stable, low impedance source. The reference connections should be capacitively coupled to ground to bypass noise.

Applying a voltage greater than 2.1 V across the internal resistor ladder will cause current densities to exceed rated values, and may cause permanent damage to the AD9028/AD9038. The design of the reference circuit should limit the voltage available to the references.

Resistance between the reference connections and the taps of the first and last comparators causes offset errors. These errors, called "top and bottom of the ladder offsets," can be nulled by using the voltage sense lines, $+V_{SENSE}$ and $-V_{SENSE}$, to adjust the reference voltages. Current through the sense lines should be limited to 100 μA.

The voltage at the midpoint of the resistor ladder, MIDSCALE VREF, can be adjusted to improve the integral linearity of individual devices.

A suggested application in Figure 4 shows a reference circuit which nulls out the offset errors using two op amps. Feedback from the sense lines causes the op amps to compensate for the offset errors. The two transistors limit the amount of current drawn directly from the op amp; resistors at the base and emitter stabilize their operation.

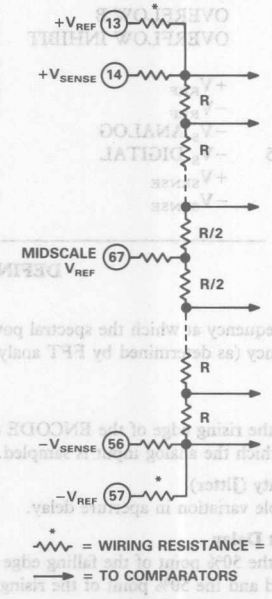


Figure 1. Reference Ladder

Analog Input Signal
The analog input circuit of the AD9028/AD9038 consists of 255 comparator inputs and can be represented by a single transistor as shown in Figure 2.

Typically, the ANALOG INPUT has an input resistance of 100 kΩ. Input capacitance is characterized in Figure 3.

With ANALOG RETURN (collector of the input transistor) connected to ground, collector base capacitance causes the analog input capacitance to be dependent on the analog input voltage. This varying capacitance is typical of flash converters, and requires that the ANALOG INPUT be driven from a low impedance source. This source must be capable of driving a capacitive load to avoid distorting the analog input signal at high

frequencies. In applications where the analog source cannot adequately drive the input capacitance, harmonic distortion will increase; the effect will be greatest on the second harmonic.

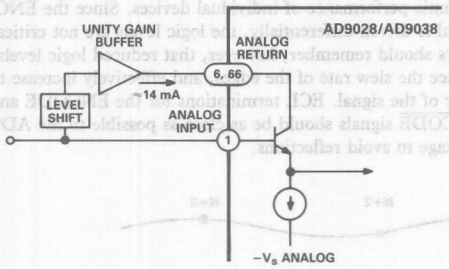


Figure 2. Preferred Analog Input Configuration

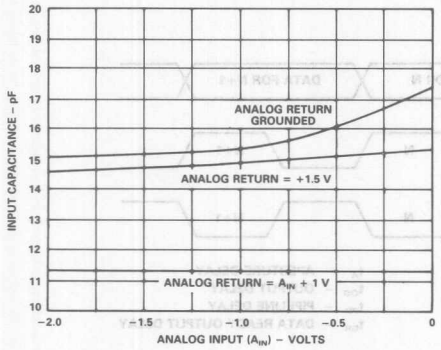


Figure 3. Input Capacitance vs. Input Voltage

AC performance of the AD9028/AD9038 can be improved by connecting the ANALOG RETURN to a dc voltage between ground and +1.5 V. This reduces the analog input capacitance and lessens its dependence on the analog input voltage (see Figure 3).

The circuits shown in Figure 2 and Figure 4 show the ANALOG RETURN driven by a buffered version of the signal presented to the ANALOG INPUT. The dc level of this signal is 1 V higher than the analog input, and thus reduces the analog input capacitance as described above. In addition, the signal cancels the ac voltage between the ANALOG RETURN and ANALOG INPUT connections, which minimizes the collector-base component of the analog input capacitance. The analog input capacitance characteristics under this condition are also shown in Figure 3.

In any of the configurations described above, the user should drive the analog signal from a low distortion, low noise amplifier. A good choice is the AD9611, a wide bandwidth operational amplifier with excellent ac performance.

Selection of the buffer is also important for applications in which the analog input signal is applied to the ANALOG RETURN. The gain of the buffer should be set as close to 1 as possible, and the buffer should have a low phase shift at the frequencies of interest. It must also be able to supply the current required, typically 14 mA.

Harmonic distortion at the ANALOG RETURN is not as critical as that at the ANALOG INPUT, but should remain less than 40 dB (out to 100 MHz) to maximize converter performance. The input impedance at this node is approximately 6.5 kΩ in parallel with 25 pF. Monolithic wideband operational amplifiers and closed loop buffers should be suitable for driving this input.

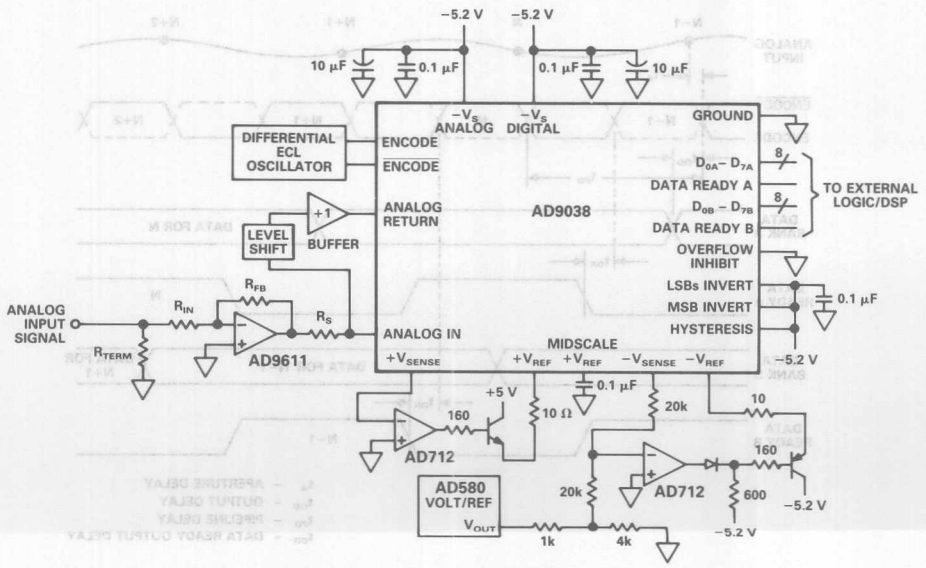
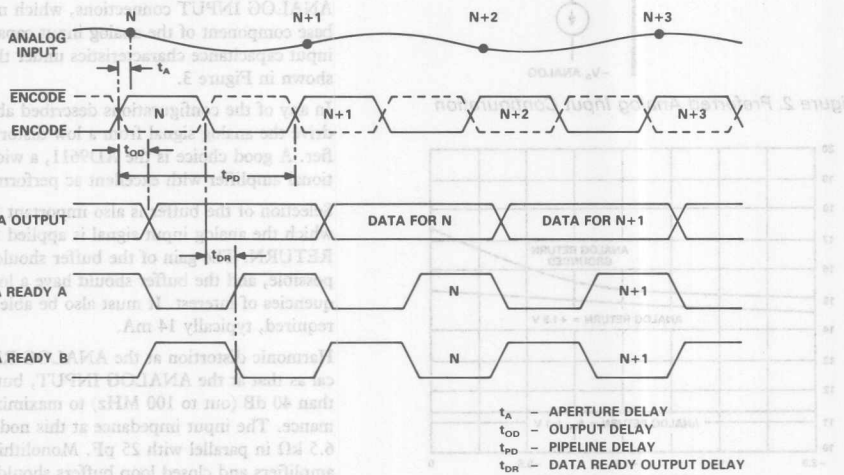


Figure 4. AD9038 Typical Application

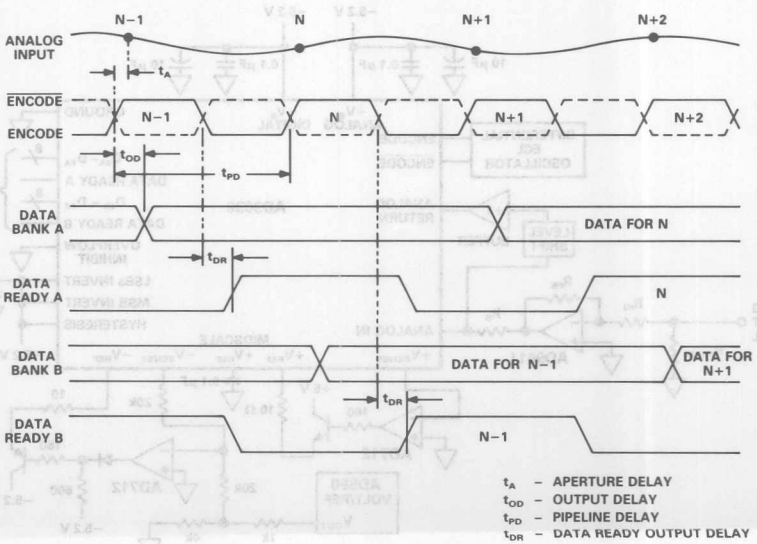
the A/D conversion by latching the comparators. The falling edge of the ENCODE signal returns the comparators to track mode and triggers the Data Ready signal.

ENCODE and $\overline{\text{ENCODE}}$ are ECL compatible and should be driven differentially. Jitter on the ENCODE signal will raise the noise floor of the converter. Differential signals, with fast clean edges, will reduce the jitter in the signal and allow optimum ac performance. In applications with a fixed, high frequency reduced) by using a crystal oscillator as the system clock.

The AD9028 is designed to operate with a 50% duty cycle ENCODE signal; adjustment of the duty cycle may improve the dynamic performance of individual devices. Since the ENCODE signal is driven differentially, the logic levels are not critical. Users should remember, however, that reduced logic levels will reduce the slew rate of the edges, and effectively increase the jitter of the signal. ECL terminations for the ENCODE and $\overline{\text{ENCODE}}$ signals should be as close as possible to the AD9028 package to avoid reflections.



AD9028 Timing Diagram



AD9038 Timing Diagram

Output data of the AD9028, D_{0A}–D_{7A} and OVERFLOW A, as well as the data ready signals, are also ECL compatible, and should be terminated through 100 Ω to −2 V (or an equivalent load). The output data can be latched on the rising edge of the DATA READY A output. For the AD9028, the DATA READY B output is simply the complement of DATA READY A.

Timing for the AD9038 is similar to the AD9028, except at the output, where the data is demultiplexed to two separate ports. Successive data samples alternate between the two ports, reducing the output data rate at either port to one-half the encode rate. Data at port A (D_{0A}–D_{7A} and OVERFLOW A) can be latched externally using the rising edge of DATA READY A. The rising edge of DATA READY B can be used to latch the data at port B (D_{0B}–D_{7B} and OVERFLOW B).

The data ready outputs for both the AD9028 and AD9038 are designed to track timing shifts over temperature.

Data Format

The format of the output data is controlled by the MSB INVERT and LSBs INVERT pins. These inputs are dc control inputs and should be connected to GROUND or $-V_S$. The AD9028/AD9038 Truth Table gives information to choose among Binary, Inverted Binary, Twos Complement and Inverted Twos Complement coding.

The OVERFLOW INHIBIT pin controls how the converter handles overflow situations (ANALOG INPUT > $+V_{SENSE}$). For normal operation, the OVERFLOW INHIBIT is connected to $-V_S$, and the output data bits (D_{0A}–D_{7A} or D_{0B}–D_{7B}) will be at a logic LOW when ANALOG INPUT > $+V_{SENSE}$ (return to zero operation). The overflow bit (OVERFLOW A or OVERFLOW B) will indicate this condition with a logic HIGH. When the ANALOG INPUT is in range (< $+V_{SENSE}$), the overflow bit will remain at logic LOW.

If the OVERFLOW INHIBIT pin is connected to ground, the overflow bit will be disabled, and the output data will remain at logic high for overflow conditions. The overflow bits are not affected by the bit invert control pins (MSB INVERT and LSBs INVERT).

Layout and Power Supplies

Proper layout of high speed circuits is always critical, but is particularly important when both analog and digital signals are involved.

Analog signal paths should be kept as short as possible and be properly terminated to avoid reflections. The analog input voltage and the voltage references should be kept away from digital signal paths; this reduces the amount of digital switching noise that is capacitively coupled into the analog section of the circuit.

Digital signal paths should also be kept short, and run lengths matched to avoid propagation delay mismatch. Proper ECL terminations should be located near the packages of successive gates.

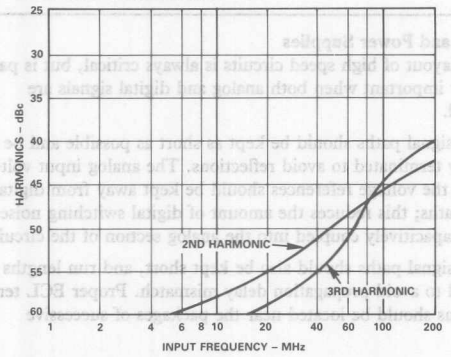
In high speed circuits, layout of the ground circuit is the most important factor. A single, low impedance ground plane, on the component side of the board, will reduce noise on the circuit ground.

Power supplies should be capacitively coupled to the ground plane to reduce noise in the circuit. Multilayer boards allow designers to lay out signal traces without interrupting the ground plane.

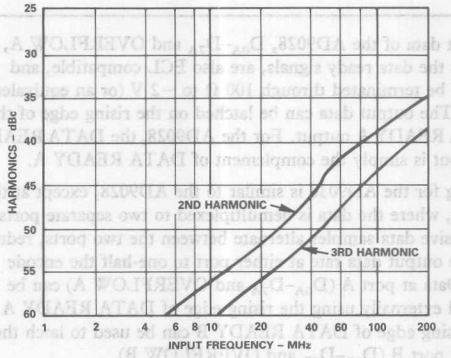
It is especially important to maintain the continuity of the ground plane under and around the AD9028/AD9038. If the system design separates the digital and analog grounds, analog ground is the preferred ground point for the A/D section of the system.

The tops of the AD9028/AD9038 packages are internally connected to the device substrates, and electrically connected to $-V_S$. The top of the package is designed to serve as a heat sink; the bottom of the package is not internally connected.

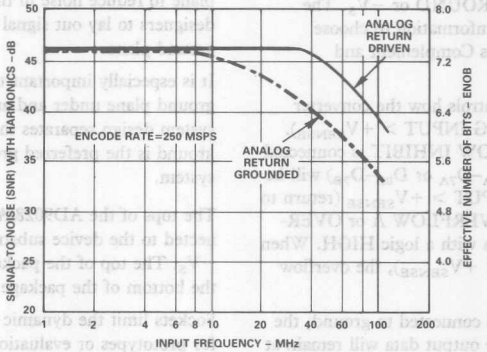
Sockets limit the dynamic performance and should be used only for prototypes or evaluation.



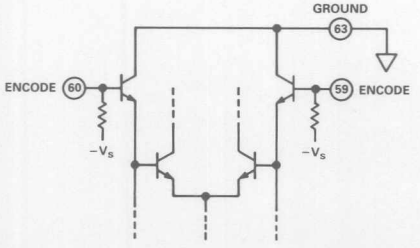
AD9028/AD9038 Harmonics vs. Input Frequency with Analog Return Driven



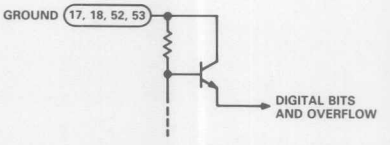
AD9028/AD9038 Harmonics vs. Input Frequency with Analog Return Grounded



AD9028/AD9038 SNR and ENOB vs. Input Frequency



Encode and $\overline{\text{Encode}}$ Equivalent Circuits

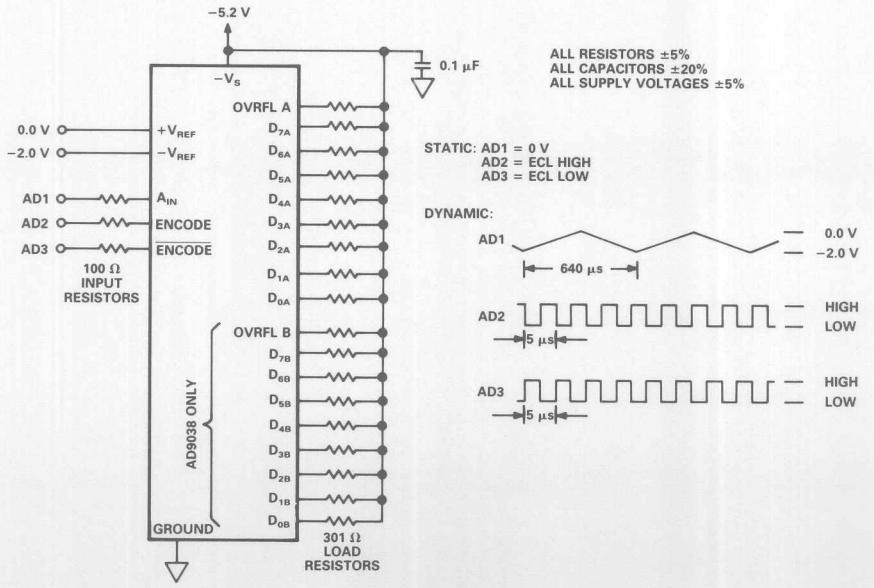


Equivalent Digital Outputs

Step	Range	Ovrfl. Inh.	Offset Binary		Twos Complement	
			True	Inverted	True	Inverted
	0 = −2 V FS = 0 V		MSB INV. = "0" LSBs INV. = "0"	MSB INV. = "1" LSBs INV. = "1"	MSB INV. = "1" LSBs INV. = "0"	MSB INV. = "0" LSBs INV. = "1"
256	≥0.000	"0"	(1)00000000	(1)11111111	(1)10000000	(1)01111111
256	≥0.000	"1"	(0)11111111	(0)00000000	(0)01111111	(0)10000000
255	−0.008	x	11111111	00000000	01111111	10000000
254	−0.016	x	11111110	00000001	01111110	10000001
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
129	−0.992	x	10000000	01111111	00000000	11111111
128	−1.000	x	01111111	10000000	11111111	00000000
127	−1.008	x	01111110	10000001	11111110	00000001
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
02	−1.992	x	00000010	11111101	10000010	01111101
01	−2.000	x	00000001	11111110	10000001	01111110
00	<−2.000	x	00000000	11111111	10000000	01111111

The overflow bit is always 0 except where noted in parentheses ( ). MSB INVERT, LSBs INVERT, and OVERFLOW INHIBIT are considered dc controls.

AD9028/AD9038 Truth Table

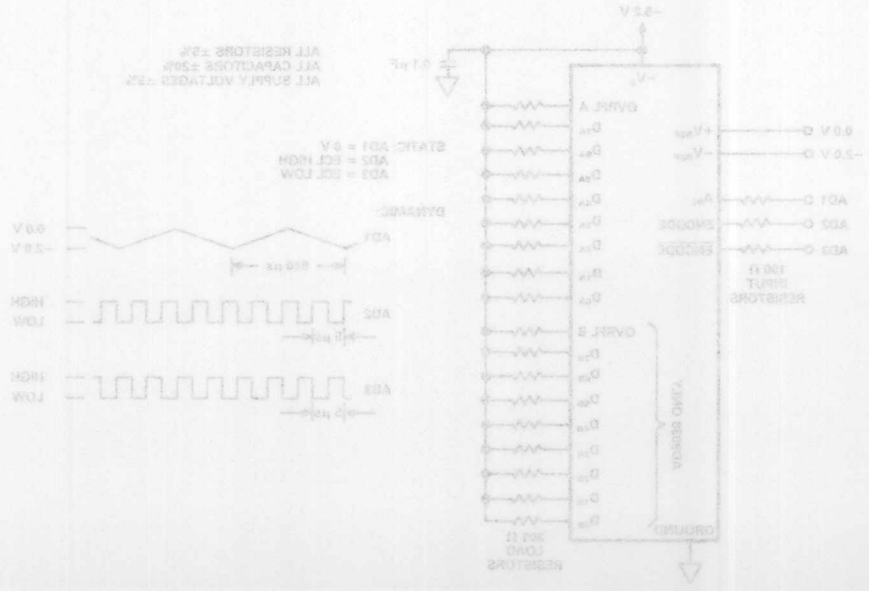


AD9028/AD9038 Burn-In Diagram

Step	Range	Ovfl. Ind.	Offset Binary		Twos Complement	
			True	Inverted	True	Inverted
	0 = −2 V FS = 0 V		MSB INV. = "0" LSBs INV. = "0"	MSB INV. = "1" LSBs INV. = "0"	MSB INV. = "1" LSBs INV. = "0"	MSB INV. = "0" LSBs INV. = "1"
256	≥0.000	"0"	(1)00000000	(1)11111111	(1)10000000	(1)01111111
256	≥0.000	"1"	(0)11111111	(0)00000000	(0)01111111	(0)10000000
255	−0.008	x	11111111	00000000	01111111	10000000
254	−0.016	x	11111110	00000001	01111110	10000001
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
129	−0.992	x	10000000	01111111	00000000	11111111
128	−1.000	x	01111111	10000000	11111111	00000000
127	−1.008	x	01111110	10000001	11111110	00000001
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
02	−1.992	x	00000010	11111101	10000010	01111101
01	−2.000	x	00000001	11111110	10000001	01111110
00	< −2.000	x	00000000	11111111	10000000	01111111

The overflow bit is always 0 except where noted in parentheses ( ). MSB INVERT, LSBs INVERT, and OVERFLOW INHIBIT are considered dc controls.

AD9028/AD9038 Truth Table



AD9028/AD9038 Burn-In Diagram

12-Bit, 25/20 MSPS A/D Converters

AD9032/AD9034

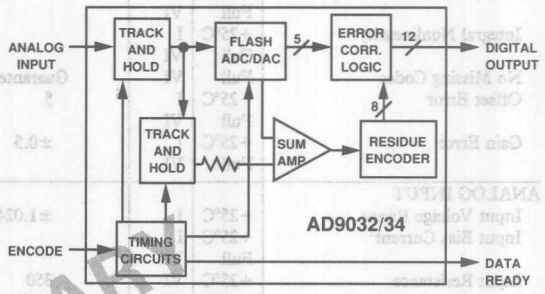
FEATURES

25 MSPS (AD9032), 20 MSPS (AD9034) Conversion Speeds
On-Board T/H, References, Timing
Low Power: 5 W
Single 40-Pin Package
70 dB Spurious-Free Dynamic Range to 10 MHz
Bipolar Input: ±1.024 V

APPLICATIONS

Radar
Signal Intelligence
Digital Spectrum Analyzers
Medical Imaging
Electro-Optics

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD9032 is the world's fastest (25 MSPS) complete 12-bit analog-to-digital converter (ADC), and features the latest in track-and-hold technology. The unit is a complete solution; on-board T/H, voltage references, and timing are all contained in a single 40-pin hybrid package. The pin-compatible AD9034 A/D converter operates at word rates of 20 MSPS.

This ECL-compatible ADC requires only +5 V and −5.2 V supplies, an analog input, and a stable ECL clock to obtain the best dynamic performance available in a 12-bit ADC.

Dynamic performance has been optimized to achieve SNR of 66 dB and a spurious-free dynamic range (SFDR) of 72 dB for analog bandwidths up to 10 MHz. All dynamic performance is guaranteed for sample rates from dc to 25.6 MSPS.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V; $-V_S$ = −5.2 V; Encode = 25.6 MSPS, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9032AD/AZ Min	AD9032AD/AZ Typ	AD9032AD/AZ Max	AD9032BD/BZ Min	AD9032BD/BZ Typ	AD9032BD/BZ Max	AD9032TD/TZ Min	AD9032TD/TZ Typ	AD9032TD/TZ Max	Units
RESOLUTION			12			12			12			Bits
DC ACCURACY												
Differential Nonlinearity	+25°C	I			1.0		0.5	0.7		0.5	0.7	LSB
	Full	VI			1.0			1.0			1.0	LSB
Integral Nonlinearity	+25°C	I			0.7			0.7			0.7	LSB
	Full	VI			1.0			1.0			1.0	LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed			Guaranteed		
Offset Error	+25°C	I		5	10		5	10		5	10	LSB
	Full	VI			25			25			50	LSB
Gain Error	+25°C	I		±0.5	±1.0		±0.5	±1.0		±0.5	±1.0	LSB
	Full	VI			±2.0			±2.0			±2.0	LSB
ANALOG INPUT												
Input Voltage Range	+25°C	I		±1.024			±1.024			±1.024		V
Input Bias Current[1]	+25°C	I			100			100			100	μA
	Full	VI			200			200			200	μA
Input Resistance	+25°C	VI		350			350			350		kΩ
Input Capacitance	+25°C	III		2	10		2	10		2	10	pF
Analog Bandwidth	+25°C	III	150			150			150			MHz
SWITCHING PERFORMANCE[2]												
Conversion Rate	Full	VI			20			26			26	MSPS
Aperture Delay (t_A)	Full	IV	2	4	6	2	4	6	1	4	7	ns
Aperture Uncertainty (Jitter)	Full	IV		5	10		5	10		5	10	ps, rms
Output Delay (t_{OD})	Full	IV	16	20	24	16	20	24	16	20	24	ns
Data Ready Delay	Full	IV	24	28	32	24	28	32	24	28	32	ns
Output Time Skew	Full	IV		1	2		1	2		1	2	ns
ENCODE INPUT												
Logic "1" Voltage	Full	IV	−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	IV			−1.5			−1.5			−1.5	V
Logic "1" Current	Full	VI		150	300		150	300		150	300	μA
Logic "0" Current	Full	VI		150	300		150	300		150	300	μA
Input Capacitance	+25°C	V		5			5			5		pF
Pulse Width (High)	+25°C	IV	10			10			10			ns
Pulse Width (Low)	+25°C	IV	10			10			10			ns
DYNAMIC PERFORMANCE												
Transient Response	+25°C	IV		TBD	40		TBD	40		TBD	40	ns
Overvoltage Recovery Time	+25°C	IV		TBD	70		TBD	70		TBD	70	ns
Harmonic Distortion												
Analog Input @ 1.2 MHz	+25°C	I	TBD	80		TBD	80		TBD	80		dBc
@ 1.2 MHz	Full	VI	TBD			TBD			TBD			dBc
@ 4.3 MHz	+25°C	V		76			76			76		dBc
@ 9.6 MHz	+25°C	I	TBD	74		TBD	74		TBD	74		dBc
@ 9.6 MHz	Full	VI	TBD			TBD			TBD			dBc
Signal-to-Noise Ratio[3]												
Analog Input @ 512 kHz	+25°C	I	66	68		66	68		66	68		dB
@ 512 kHz	Full	VI	65			65			64			dB
@ 4.3 MHz	+25°C	V		TBD			TBD			TBD		dB
@ 9.6 MHz	+25°C	I	64	TBD		64	TBD		64	TBD		dBc
@ 9.6 MHz	Full	VI	63			63			62			dBc
Two-Tone Intermodulation Distortion Rejection[4]	+25°C	V		74			77			77		dBc

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter (Conditions)	Temp	Test Level	AD9032AD/AZ Min	Typ	Max	AD9032BD/BZ Min	Typ	Max	AD9032TD/TZ Min	Typ	Max	Units
DIGITAL OUTPUTS[2]												
Logic "1" Voltage	Full	VI	−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			−1.5			−1.5	V
Output Coding				2s Complement			2s Complement			2s Complement		
POWER SUPPLY												
$+V_S$ Supply Voltage	Full	VI	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	mA
$+V_S$ Supply Analog Current	Full	VI		250	285		250	285		250	285	mA
$-V_S$ Supply Voltage	Full	VI	−5.45	−5.2	−4.95	−5.45	−5.2	−4.95	−5.45	−5.2	−4.95	mA
$-V_S$ Supply Analog Current	Full	VI		500	525		500	525		500	525	mA
$-V_S$ Supply Digital Current	Full	VI		310	330		310	330		310	330	mA
Power Dissipation	Full	VI		5.4	6		5.4	6		5.4	6	W
Power Supply Rejection Ratio (PSRR)[5]	Full	VI		2.5	5.0		2.5	5.0		2.5	5.0	mV/V

NOTES
[1]Measured with analog input = 0 V.
[2]Outputs terminated through 510 Ω to −5.2 V; C_L < 4 pF.
[3]RMS signal to rms noise with analog input signal 1 dB below full scale at specified frequency.
[4]Intermodulation measured with analog input frequencies of 11 MHz and 12 MHz at 7 dB below full scale.
[5]PSRR is sensitivity of offset error to power supply variations within the 5% limits shown.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$ . . . . . +6 V
$-V_S$ . . . . . −6 V
Analog Input . . . . . $-V_S$ to $+V_S$
Digital Inputs . . . . . $-V_S$ to 0 V
Digital Output Current . . . . . 20 mA
Operating Temperature Range
AD9032AD/BD/AZ/BZ . . . . . −25°C to +85°C
AD9032TD/TZ . . . . . −55°C to +125°C
Maximum Junction Temperature[2] . . . . . +175°C
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances: θ_{CA} = 12°C/W; T_J–T_C = 10°C max (worst case die junction temperature rise).

EXPLANATION OF TEST LEVELS

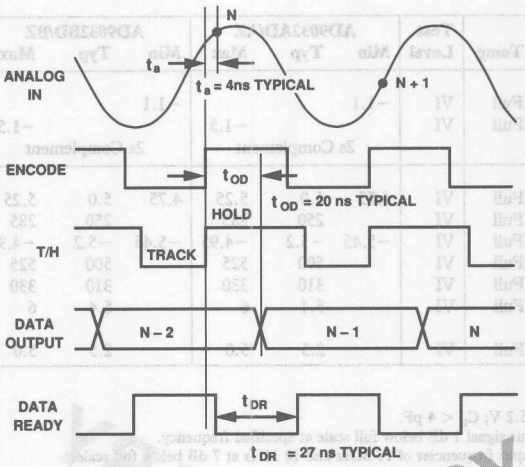
Test Level
I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures. AC testing done on sample basis.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Model	Temperature Range	Description	Package Option[1]
AD9032AD	−25°C to +85°C	40-Pin Ceramic DIP, Industrial Temperature	D-40
AD9032AZ[2]	−25°C to +85°C	40-Pin Leaded Flatpack, Industrial Temperature	Z-40
AD9032BD	−25°C to +85°C	40-Pin Ceramic DIP, Industrial Temperature	D-40
AD9032BZ[2]	−25°C to +85°C	40-Pin Leaded Flatpack, Industrial Temperature	Z-40
AD9032TD	−55°C to +125°C	40-Pin Ceramic DIP, Military Temperature	D-40
AD9032TZ[2]	−55°C to +125°C	40-Pin Leaded Flatpack, Military Temperature	Z-40

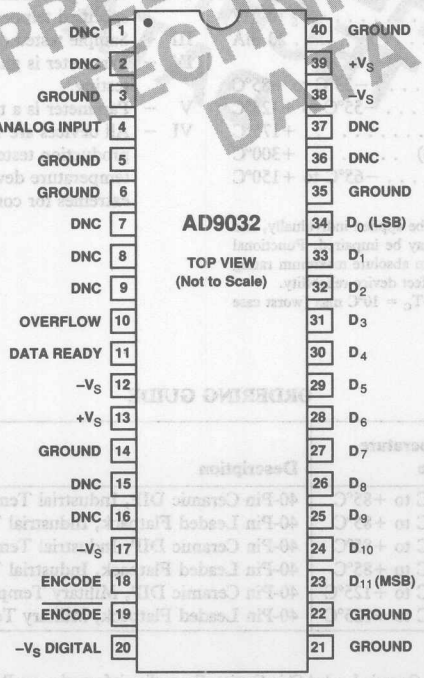
NOTES
[1]D = Ceramic DIP; Z = Ceramic Leaded Chip Carrier. For outline information see Package Information section.
[2]Surface mount leaded packages are tested and shipped with unformed leads. Consult the factory for price and availability of packages with formed leads.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.



AD9032 Timing Diagram

AD9032 PINOUT



PRELIMINARY TECHNICAL DATA

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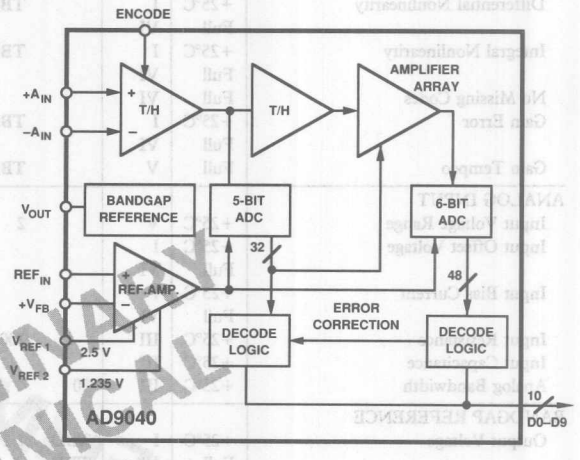
10-Bit, 40 MSPS A/D Converter

AD9040

FEATURES
40 MSPS Conversion Speed
Low Power: < 1 W
On-Board T/H
2 V p–p Analog Input
Fully Characterized Dynamic Performance

APPLICATIONS
Medical Imaging
Digital Oscilloscopes
Professional Video
Communications
Advanced Television (MUSE Decoders)

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9040 is a complete 10-bit sampling analog-to-digital converter (ADC) with on-board track-and-hold. The unit is designed for low cost, high performance applications and requires only an encode signal to achieve 40 MSPS sample rates with 10-bit resolution.

Digital inputs and outputs are TTL/CMOS compatible. The analog input requires a signal of 2 V p–p amplitude and can be driven differentially. The two-step architecture used in the AD9040 is optimized to provide the best dynamic performance available while maintaining low power requirements.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter (Conditions)	Temp	Test Level	AD9040JN/JP Min	Typ	Max	AD9040KN/KP Min	Typ	Max	AD9040TE/TQ Min	Typ	Max	Units
RESOLUTION			10			10			10			Bits
DC ACCURACY												
Differential Nonlinearity	+25°C	I		TBD	TBD		0.5	1.0		0.5	1.0	LSB
	Full	VI			TBD			1.0			1.0	LSB
Integral Nonlinearity	+25°C	I		TBD	TBD		0.5	1.0		0.5	1.0	LSB
	Full	VI			TBD			1.0			1.0	LSB
No Missing Codes	Full	VI					Guaranteed			Guaranteed		
Gain Error	+25°C	I		TBD	TBD		TBD	TBD		TBD	TBD	% FS
	Full	VI			TBD			TBD			TBD	% FS
Gain Tempco	Full	V		TBD			TBD			TBD		ppm/°C
ANALOG INPUT												
Input Voltage Range	+25°C	V		2			2			2		V p–p
Input Offset Voltage	+25°C	I			20			20			20	mV
	Full	VI			25			25			40	mV
Input Bias Current	+25°C	I			1.0			1.0			1.0	μA
	Full	VI			2.0			2.0			2.0	μA
Input Resistance	+25°C	III		100			100			100		kΩ
Input Capacitance	+25°C	III			10			10			10	pF
Analog Bandwidth	+25°C	III	50			50			50			MHz
BANDGAP REFERENCE												
Output Voltage	+25°C	I	TBD	1.2	TBD	TBD	1.2	TBD	TBD	1.2	TBD	V
	Full	VI	TBD		TBD	TBD		TBD	TBD		TBD	V
Temperature Coefficient	Full	V		TBD			TBD			TBD		ppm/°C
SWITCHING PERFORMANCE												
Conversion Rate	+25°C	I	40			40			40			MSPS
Aperture Delay (t_A)	+25°C	V		5			5			5		ns
Aperture Uncertainty (Jitter)	+25°C	V		5			5			5		ps rms
Output Delay (t_{OD})[1]	+25°C	I	TBD	4	TBD	TBD	4	TBD	TBD	4	TBD	ns
	Full		TBD		TBD	TBD		TBD	TBD		TBD	ns
Output Time Skew[1]	+25°C	IV		2			2			2		ns
DYNAMIC PERFORMANCE												
Transient Response	+25°C	V		TBD			TBD			TBD		ns
Overvoltage Recovery Time	+25°C	V		TBD			TBD			TBD		ns
Effective Number of Bits (ENOB)												
f_{IN} = 2.3 MHz	+25°C	I	9.0			9.0			9.0			Bits
f_{IN} = 10.3 MHz	+25°C	I	9.0			9.0			9.0			Bits
Signal-to-Noise Ratio[2]												
f_{IN} = 2.3 MHz	+25°C	I	56	58		56	58		56	58		dB
f_{IN} = 10.3 MHz	+25°C	I	56	58		56	58		56	58		dB
Signal-to-Noise Ratio[2] (without harmonics)												
f_{IN} = 2.3 MHz	+25°C	I	56	58		56	58		56	58		dB
f_{IN} = 10.3 MHz	+25°C	I	56	58		56	58		56	58		dB
2nd Harmonic Distortion												
f_{IN} = 2.3 MHz	+25°C	I	70			70			70			dBc
f_{IN} = 10.3 MHz	+25°C	I	62			62			62			dBc
3rd Harmonic Distortion												
f_{IN} = 2.3 MHz	+25°C	I	70			70			70			dBc
f_{IN} = 10.3 MHz	+25°C	I	62			62			62			dBc
Two-Tone Intermodulation Distortion Rejection[3]	+25°C	V		TBD			TBD			TBD		dBc
Differential Phase	+25°C	III		0.5			0.5			0.5		Degree
Differential Gain	+25°C	III		1			1			1		%

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter (Conditions)	Temp	Test Level	AD9040JN/JP Min	AD9040JN/JP Typ	AD9040JN/JP Max	AD9040KN/KP Min	AD9040KN/KP Typ	AD9040KN/KP Max	AD9040TE/TQ Min	AD9040TE/TQ Typ	AD9040TE/TQ Max	Units
ENCODE INPUT												
Logic "1" Voltage	Full	VI	2.0			2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8			0.8	V
Logic "1" Current	Full	VI			10			10			10	μA
Logic "0" Current	Full	VI			10			10			10	μA
Input Capacitance	+25°C	V		5			5			5		pF
Encode Pulse Width (High) (t_{EH})[4]	+25°C	IV	TBD			TBD			TBD			ns
Encode Pulse Width (Low) (t_{EL})[4]	+25°C	IV	TBD			TBD			TBD			ns
DIGITAL OUTPUTS												
Logic "1" Voltage (I_{OH} = 2 mA)	Full	VI	2.4			2.4			2.4			V
Logic "0" Voltage (I_{OL} = 10 mA)	Full	VI			0.4			0.4			0.4	V
POWER SUPPLY												
V_{DD} Supply Current	Full	VI			TBD			TBD			TBD	mA
V_{CC} Supply Current	Full	VI			TBD			TBD			TBD	mA
V_{SS} Supply Current	Full	VI			TBD			TBD			TBD	mA
V_{EE} Supply Current	Full	VI			TBD			TBD			TBD	mA
Power Dissipation	Full	VI		0.9	1.2		0.9	1.2		0.9	1.2	W
Power Supply Rejection Ratio (PSRR)[5]	+25°C	I		TBD	TBD		TBD	TBD		TBD	TBD	mV/V

NOTES
[1]Output delay measured as worst-case time from 50% point of the falling edge of ENCODE to 50% point of the slowest rising or falling edge of D0–D9. Output skew measured as worst-case difference in output delay among D0–D9.
[2]RMS signal to rms noise with analog input signal 1 dB below full scale at specified frequency.
[3]Intermodulation measured with analog input frequencies of 2.3 MHz and 3.0 MHz at 7 dB below full scale.
[4]For rated performance at 40 MSPS, duty cycle of encode command should be 50% ±5%.
[5]Measured as the ratio of the worst-case change in transition voltage of a single comparator for a 5% change in V_{CC} or V_{EE}.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$ (V_{DD} and V_{CC}) . . . . . +7 V
$-V_S$ (V_{SS} and V_{EE}) . . . . . −7 V
Analog In . . . . . $-V_S$ to $+V_S$
Digital Inputs . . . . . 0 V to $+V_S$
Digital Output Current . . . . . 20 mA
Operating Temperature
AD9040JN/JP/KN/KP . . . . . 0°C to +70°C
AD9040TE/TQ . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Maximum Junction Temperature[2] . . . . . +175°C
Lead Soldering Temp (10 sec) . . . . . +300°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances: "N" Package (Plastic DIP): θ_{JC} = 7°C/W; θ_{JA} = 42°C/W; "P" Package (PLCC): θ_{JC} = 10°C/W; θ_{JA} = 48°C/W; "E" Package (Ceramic LCC): θ_{JC} = 23°C/W; θ_{JA} = 69°C/W; "Q" Package (Ceramic DIP): θ_{JC} = 25°C/W; θ_{JA} = 75°C/W.

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Parameter (Conditions)	Temp	Test Level	AD9040BJN/JP Min	Typ	Max	AD9040KN/KP Min	Typ	Max	AD9040TE/TQ Min	Typ	Max	Units
ENCODE INPUT												
Logic "1" Voltage	Full	VI	2.0			2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8			0.8	V
Logic "1" Current	Full	VI			10			10			10	μA
Logic "0" Current	Full	VI			10			10			10	μA
Input Capacitance	+25°C	V		5			5			5		pF
Encode Pulse Width (High) (t_{EH})[4]	+25°C	IV	TBD			TBD			TBD			ns
Encode Pulse Width (Low) (t_{EL})[4]	+25°C	IV	TBD			TBD			TBD			ns
DIGITAL OUTPUTS												
Logic "1" Voltage (I_{OH} = 2 mA)	Full	VI	2.4			2.4			2.4			V
Logic "0" Voltage (I_{OL} = 10 mA)	Full	VI			0.4			0.4			0.4	V
POWER SUPPLY												
V_{DD} Supply Current	Full	VI			TBD			TBD			TBD	mA
V_{CC} Supply Current	Full	VI			TBD			TBD			TBD	mA
V_{EE} Supply Current	Full	VI			TBD			TBD			TBD	mA
V_{EE} Supply Current	Full	VI			TBD			TBD			TBD	mA
Power Dissipation	Full	VI	0.9	1.2		0.9	1.2		0.9	1.2		W
Power Supply Rejection Ratio (PSRR)[5]	+25°C	I	TBD	TBD		TBD	TBD		TBD	TBD		mV/V

NOTES

[1]Output delay measured as worst-case time from 50% point of the falling edge of ENCODE to 50% point of the slowest rising or falling edge of D0–D9.

[2]Output skew measured as worst-case difference in output delay among D0–D9.

[3]RMS signal to rms noise with analog input signal 1 dB below full scale, encode rate = 5 MSPS.

[4]Intermodulation measured with analog input frequencies of 249 MHz and 1.0 MHz at 7 dB below full scale.

[5]For rated performance at 40 MSPS, duty cycle of encode command should be 50%.

[6]Measured as the ratio of the worst-case change in supply voltage to change in analog output for ±5% change in V_{CC} or V_{EE}.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS[1]

+V_S (V_{DD} and V_{CC}) . . . . . +7V
−V_S (V_{EE} and V_{EE}) . . . . . −7V
Analog In . . . . . −V_S to +V_S
Digital Inputs . . . . . 0 V to +V_S
Digital Output Current . . . . . 20 mA
Operating Temperature
AD9040[J/N/P/K/N/K]P . . . . . 0°C to +70°C
AD9040TE/TQ . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Maximum Junction Temperature[2] . . . . . +175°C
Lead Soldering Temp (10 sec) . . . . . +300°C

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances "N" Package (Plastic DIP): θ_{JA} = 70°C/W; θ_{JC} = 45°C/W; "P" Package (LCC): θ_{JA} = 100°C/W; θ_{JC} = 45°C/W; "E" Package (Ceramic LCC): θ_{JA} = 75°C/W; θ_{JC} = 65°C/W; "Q" Package (Ceramic DIP): θ_{JA} = 85°C/W; θ_{JC} = 15°C/W.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

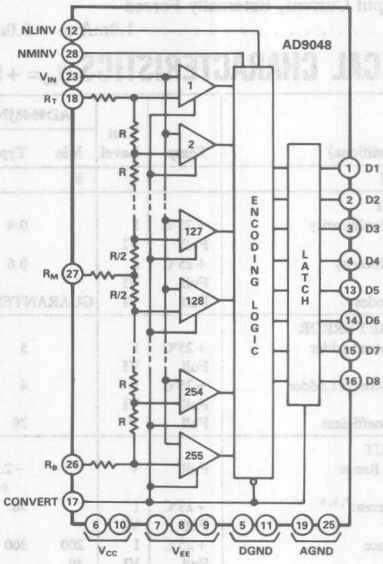
Monolithic 8-Bit Video A/D Converter

AD9048

FEATURES
- 35MSPS Encode Rate
- 16pF Input Capacitance
- 550mW Power Dissipation
- Industry-Standard Pinouts
- MIL-STD-883 Compliant Versions Available

APPLICATIONS
- Professional Video Systems
- Special Effects Generators
- Electro-Optics
- Digital Radio
- Electronic Warfare (ECM, ECCM, ESM)

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9048 is an 8-bit, 35MSPS flash converter, made on a high speed bipolar process, which is an alternate source for the TDC1048 unit but offers enhancements over its predecessor. Lower power dissipation makes the AD9048 attractive for a variety of system designs.

Because of its wide bandwidth, it is an ideal choice for real-time conversion of video signals. Input bandwidth is flat with no missing codes.

Clocked latching comparators, encoding logic and output buffer registers operating at minimum rates of 35MSPS preclude a need for a sample-and-hold (S/H) or track-and-hold (T/H) in most system designs using the AD9048. All digital control inputs and outputs are TTL compatible.

Devices operating over two ambient temperature ranges and with two grades of linearity are available. Linearities of either 0.5LSB or 0.75LSB can be ordered for a commercial range of 0 to +70°C, or extended case temperatures of −55°C to +125°C. Commercial versions are packaged in 28-pin DIPs; extended temperature versions are available in ceramic DIP and ceramic LCC packages. Both commercial units and MIL-STD-883 units are standard products.

The AD9048 A/D converter is available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current AD9048/883B data sheet for detailed specifications.

AGND to DGND . . . . . −0.5V dc to +0.5V dc
V_{EE} to AGND . . . . . +0.5V dc to −7.0V dc
V_{IN}, V_{RT} or V_{RB} to AGND . . . . . +0.5V to V_{EE}
V_{RT} to V_{RB} . . . . . −2.2V dc to +2.2V dc
CONV, NMINV or NLINV to DGND . −0.5V dc to +5.5V dc
Applied Output Voltage to DGND . −0.5V dc to +5.5V dc[2]
Applied Output Current, Externally Forced
. . . . . −1.0mA to +6.0mA[3, 4]

Operating Temperature Range (Ambient)
AD9048JN/KN/JJ/KJ/JQ/KQ . . . . . 0 to +70°C
AD9048SE/SQ/TE/TQ . . . . . −55°C to +125°C
Maximum Junction Temperature (Plastic) . . . . . +150°C[6]
Maximum Junction Temperature (Hermetic) . . . . . +175°C[6]
Lead Temperature (Soldering, 10sec) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0V; V_{EE} = −5.2V; Differential Reference Voltage = 2.0V, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9048JN/JJ/JQ			AD9048KN/KJ/KQ			AD9048SE/SQ			AD9048TE/TQ			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION			8			8			8			8			Bits
DC ACCURACY															
Differential Nonlinearity	+25°C	I		0.4	0.75		0.3	0.5		0.4	0.75		0.3	0.5	LSB
	Full	VI			1.0			0.75			1.0			0.75	LSB
Integral Nonlinearity	+25°C	I		0.6	0.75		0.4	0.5		0.6	0.75		0.4	0.5	LSB
	Full	VI			1.0			0.75			1.0			0.75	LSB
No Missing Codes	Full	VI	GUARANTEED			GUARANTEED			GUARANTEED			GUARANTEED			
INITIAL OFFSET ERROR															
Top of Reference Ladder	+25°C	I		5	12		5	12		5	12		5	12	mV
	Full	VI			12			12			12			12	mV
Bottom of Reference Ladder	+25°C	I		4	8		4	8		4	8		4	8	mV
	Full	VI			8			8			8			8	mV
Offset Drift Coefficient	Full	V		20			20			20			20		µV/°C
ANALOG INPUT															
Input Voltage Range	Full	V		−2.1; +0.1			−2.1; +0.1			−2.1; +0.1			−2.1; +0.1		V
Input Bias Current[7, 8, 9]	+25°C	I		36	60		36	60		36	60		36	60	µA
	Full	VI			100			100			100			100	µA
Input Resistance	+25°C	I	200	300		200	300		200	300		200	300		kΩ
	Full	VI	40			40			40			40			kΩ
Input Capacitance	+25°C	III		16	20		16	20		16	20		16	20	pF
Full Power Bandwidth[10]	+25°C	III	10	15		10	15		10	15		10	15		MHz
REFERENCE INPUT															
Positive Reference Voltage[11]	Full	V		0.0			0.0			0.0			0.0		V
Negative Reference Voltage[11]	Full	V		−2.0			−2.0			−2.0			−2.0		V
Differential Reference Voltage	Full	V		2.0			2.0			2.0			2.0		V
Reference Ladder Resistance	Full	VI	50	90	125	50	90	125	50	90	125	50	90	125	Ω
Ladder Temperature Coefficient	Full	V		0.22			0.22			0.22			0.22		Ω/°C
Reference Ladder Current[12]	Full	VI		23	40		23	40		23	40		23	40	mA
Reference Input Bandwidth	+25°C	V		10			10			10			10		MHz
DYNAMIC PERFORMANCE[13]															
Conversion Rate[12, 14]	+25°C	I	35	38		35	38		35	38		35	38		MHz
Aperture Delay	+25°C	III		2.4	5		2.4	5		2.4	5		2.4	5	ns
Aperture Uncertainty (Jitter)	+25°C	III		25	50		25	50		25	50		25	50	ps
Output Delay (t_{PD})[8, 12]	+25°C	I		13	15		9	15		9	15		9	15	ns
Output Hold Time (t_{OH})[15]	+25°C	I	5	8		5	8		5	8		5	8		ns
Transient Response[16]	+25°C	I		6	20		6	20		6	20		6	20	ns
Overvoltage Recovery Time[17]	+25°C	V		8			8			8			8		ns
Rise Time	+25°C	I			9			9			9			9	ns
Fall Time	+25°C	I			14			14			14			14	ns
Output Time Skew[18]	+25°C	I		4.5	7		4.5	7		4.5	7		4.5	7	ns
NMINV and NLINV INPUTS[8, 12]															
+0.4V Input Current	Full	VI			200			200			200			200	µA
+2.4V Input Current	Full	VI			10			10			10			10	µA
+5.5V Input Current	Full	VI			10			10			10			10	µA
CONVERT INPUT															
Logic "1" Voltage	Full	VI	2.0			2.0			2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8			0.8			0.8	V
Logic "1" Current (V_I = +2.4V)[8, 12]	Full	VI			15			15			15			15	µA
Logic "1" Current (V_I = +5.5V)[8, 12]	Full	VI			15			15			15			15	µA
Logic "0" Current[8, 12]	Full	VI			500			500			500			500	µA
Input Capacitance	+25°C	III		4	6		4	6		4	6		4	6	pF
Convert Pulse Width (LOW)	+25°C	I	18			18			18			18			ns
Convert Pulse Width (HIGH)	+25°C	I	10			10			10			10			ns

Parameter (Conditions)	Temp	Test Level	AD9048JN/JJ/JQ Min	Typ	Max	AD9048KN/KJ/KQ Min	Typ	Max	AD9048SE/SQ Min	Typ	Max	AD9048TE/TQ Min	Typ	Max	Units
AC LINEARITY															
In-Band Harmonics															
dc to 2.438MHz[19]	+25°C	I	47	50		49	55		47	50		49	55		dBc
dc to 9.35MHz[20]	+25°C	V		48			48			48			48		dBc
Signal-to-Noise Ratio (SNR)[19]															
1.248MHz Input Frequency[21]	+25°C	I	43.5	44		45	46		43.5	44		45	46		dB
2.438MHz Input Frequency[21]	+25°C	I	43	44		44	46		43	44		44	46		dB
1.248MHz Input Frequency[22]	+25°C	I	52.5	53		54	55		52.5	53		54	55		dB
2.438MHz Input Frequency[22]	+25°C	I	52	53		53	55		52	53		53	55		dB
Signal-to-Noise Ratio (SNR)[20]															
1.248MHz Input Frequency[21]	+25°C	I	43.5	44		45	46		43.5	44		45	46		dB
9.35MHz Input Frequency[21]	+25°C	V		40.5			40.5			40.5			40.5		dB
Noise Power Ratio (NPR)[23]	+25°C	III	36.5	39		36.5	39		36.5	39		36.5	39		dB
Differential Phase[24]	+25°C	III			1			1			1			1	Degree
Differential Gain[24]	+25°C	III			2			2			2			2	%
DIGITAL OUTPUTS															
Logic "1" Voltage[14]	Full	VI	2.4			2.4			2.4			2.4			V
Logic "0" Voltage[9, 14]	Full	VI			0.5			0.5			0.5			0.5	V
Short Circuit Current[5]	Full	VI			30			30			30			30	mA
POWER SUPPLY															
Positive Supply Current (+5.5V)	+25°C	I		34	46		34	46		34	46		34	46	mA
(V_{EE} = −5.5V)	Full	VI			48			48			48			48	mA
Negative Supply Current (−5.5V)	+25°C	I		90	110		90	110		90	110		90	110	mA
	Full	VI			120			120			120			120	mA
Nominal Power Dissipation	+25°C	V		550			550			550			550		mW
Reference Ladder Dissipation	+25°C	V		45			45			45			45		mW

NOTES:

[1]Maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the device may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

[2]Applied voltage must be current-limited to specified range.

[3]Forcing voltage must be limited to specified range.

[4]Current is specified as negative when flowing into the device.

[5]Output High; one pin to ground; one second duration.

[6]Typical thermal impedances (no air flow) are as follows:

Ceramic DIP: θ_{JA} = 49°C/W; θ_{JC} = 15°C/W LCC: θ_{JA} = 69°C/W; θ_{JC} = 21°C/W

Plastic DIP: θ_{JA} = 58°C/W; θ_{JC} = 16°C/W PLCC: θ_{JA} = 59; θ_{JC} = 19

To calculate junction temperature (T_J), use power dissipation (PD) and thermal impedance:

$T_J = PD(\theta_{JA}) + T_{AMBIENT} = PD(\theta_{JC}) = + T_{CASE}$

[7]Measured with V_{IN} = 0V and CONVERT low (sampling mode).

[8]V_{CC} = +5.5V

[9]V_{EE} = −5.5V

[10]Determined by beat frequency testing for no missing codes.

[11]$V_{RT} \geq V_{RB}$ under all circumstances.

[12]V_{EE} = −4.9V

[13]Outputs terminated with 40pF and 810Ω pull-up resistors.

[14]V_{CC} = +4.5V

[15]Interval from 50% point of leading edge CONVERT pulse to change in output data.

[16]For full scale step input, 8-bit accuracy attained in specified time.

[17]Recovers to 8-bit accuracy in specified time after −3V input overvoltage.

[18]Output time skew includes high-to-low and low-to-high transitions as well as bit-to-bit time skew differences.

[19]Measured at 20MHz encode rate with analog input 1dB below full scale.

[20]Measured at 35MHz encode rate with analog input 1dB below full scale.

[21]RMS signal to rms noise.

[22]Peak signal to rms noise.

[23]DC to 8MHz noise bandwidth with 1.248MHz slot; four sigma loading; 20MHz encode.

[24]Clock frequency = 4 × NTSC = 14.32MHz. Measured with 40-IRE modulated ramp.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level I – 100% production tested.

Test Level II – 100% production tested at +25°C and sample tested at specified temperatures.

Test Level III – Sample tested only.

Test Level IV – Parameter is guaranteed by design and characterization testing.

Test Level V – Parameter is a typical value only.

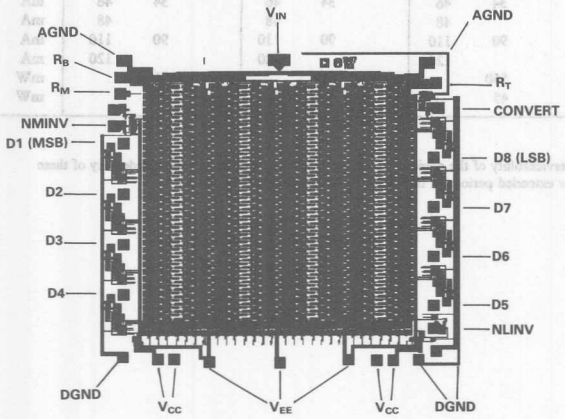
Test Level VI – All devices are 100% production tested at 25°C. 100% production tested at temperature extremes for military temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Model	Linearity	Temperature	Package Option[1]
AD9048JN	0.75LSB	0 to +70°C	N-28
AD9048KN	0.5LSB	0 to +70°C	N-28
AD9048JJ	0.75LSB	0 to +70°C	J-28
AD9048KJ	0.5LSB	0 to +70°C	J-28
AD9048JQ	0.75LSB	0 to +70°C	Q-28
AD9048KQ	0.5LSB	0 to +70°C	Q-28
AD9048SE[2]	0.75LSB	−55°C to +125°C	E-28A
AD9048TE[2]	0.5LSB	−55°C to +125°C	E-28A
AD9048SQ[2]	0.75LSB	−55°C to +125°C	Q-28
AD9048TQ[2]	0.5LSB	−55°C to +125°C	Q-28

NOTES
[1]E = Leadless Ceramic Chip Carrier; J = J-Leaded Ceramic; N = Plastic DIP; Q = Cerdip. For outline information see Package Information section.
[2]For specifications, refer to Analog Devices *Military Products Databook*.

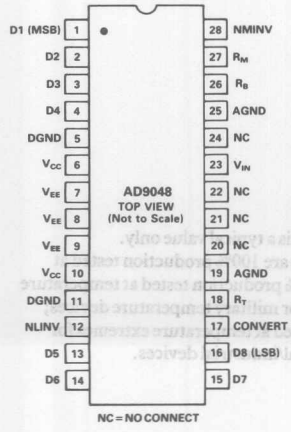
MECHANICAL INFORMATION



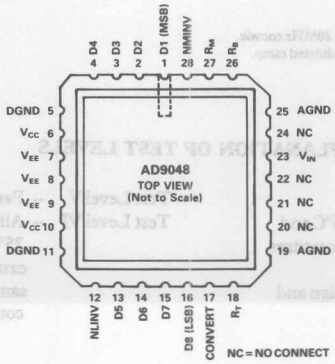
Die Dimensions	127 × 140 × 4 (±2) mils
Pad Dimensions	4 × 4 mils
Metalization	Gold
Backing	None
Substrate Potential	V_{EE}
Passivation	Nitride
Die Attach	Gold Eutectic
Bond Wire	1 mil Gold; Gold Ball Bonding

PIN CONFIGURATIONS

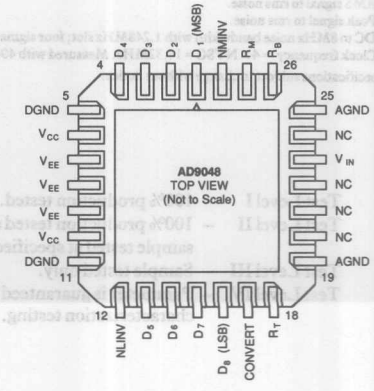
DIP



LCC

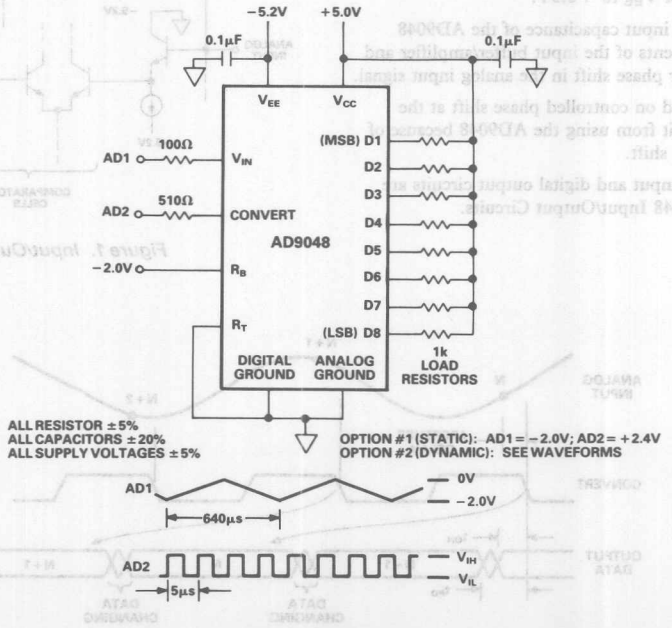


J-Leaded Ceramic



FUNCTIONAL DESCRIPTION

Pin Name	Description
D1 – D8	Eight digital outputs. D1 (MSB) is the most significant bit of the digital output word; D8 (LSB) is the least significant bit.
AGND	One of two analog ground returns. Both grounds should be connected together and to low impedance ground plane near the AD9048.
DGND	One of two digital ground returns. Both grounds should be connected together and to low impedance ground plane near the AD9048.
V_{CC}	Positive supply terminals; nominally +5.0V.
V_{EE}	Negative supply terminals; nominally −5.2V.
CONVERT	Input for conversion signal; sample of analog input signal taken on rising edge of this pulse.
R_B	Most negative reference voltage for internal reference ladder.
R_M	Midpoint tap on internal reference ladder.
R_T	Most positive reference voltage for internal reference ladder.
V_{IN}	Analog input signal pin.
NMINV	"Not Most Significant Bit Invert." In normal operation, this pin floats high; logic LOW at NMINV inverts most significant bit of digital output word [D1 (MSB)].
NLINV	"Not Least Significant Bit Invert." In normal operation, this pin floats high; logic LOW at NLINV inverts the seven least significant bits of the digital output word.



AD9048 Burn-In Diagram

THEORY OF OPERATION

Refer to the block diagram of the AD9048. The AD9048 comprises three functional sections: a comparator array, encoding logic, and output latches.

Within the array, the analog input signal to be digitized is compared with 255 reference voltages. The outputs of all comparators whose references are below the input signal level will be high; and outputs whose references are above that level will be low.

The n-of-255 code which results from this comparison is applied to the encoding logic where it is converted into binary coding. When it is inverted with dc signals applied to the NLINV and/or NMINV pins, it becomes twos complement.

After encoding, the signal is applied to the output latch circuits where it is held constant between updates controlled by the application of CONVERT pulses.

The AD9048 uses strobed latching comparators in which comparator outputs are either high or low, as dictated by the analog input level. Data appearing at the output pins have a pipeline delay of one encode cycle.

Input signal levels between the references applied to R_T (Pin 18) and R_B (Pin 26) will appear at the output as binary numbers between 0 and 255, inclusive. Signals outside that range will show up as either full-scale positive or full-scale negative outputs. No damage will occur to the AD9048 as long as the input is within the voltage range of V_{EE} to +0.5V.

The significantly reduced input capacitance of the AD9048 lowers the drive requirements of the input buffer/amplifier and also induces much smaller phase shift in the analog input signal.

Applications which depend on controlled phase shift at the converter input can benefit from using the AD9048 because of its inherently lower phase shift.

The CONVERT, analog input and digital output circuits are shown in Figure 1, AD9048 Input/Output Circuits.

System timing which provides details on delays through the AD9048, as well as the relationships of various timing events, is shown in Figure 2, AD9048 Timing Diagram.

Dynamic performance of the AD9048, i.e., typical signal-to-noise ratio, is illustrated in Figures 3 and 4.

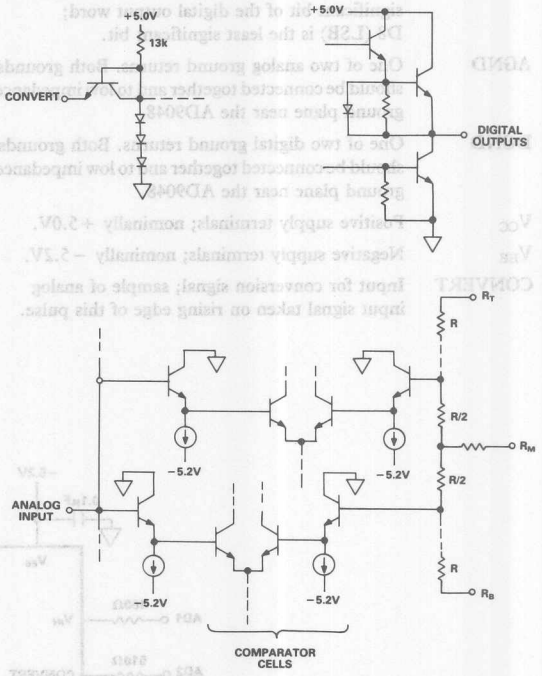


Figure 1. Input/Output Circuits

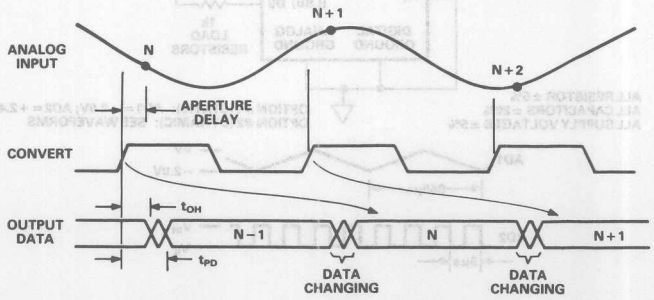


Figure 2. AD9048 Timing Diagram

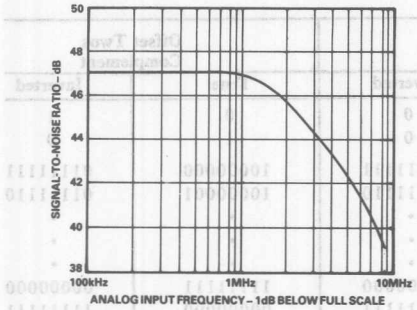


Figure 3. AD9048 Dynamic Performance (20MHz Encode Rate)

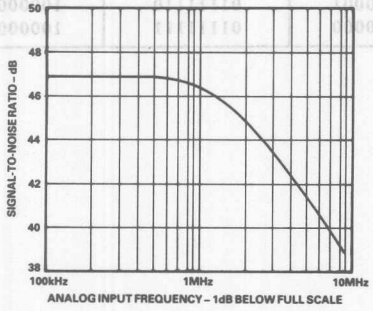


Figure 4. AD9048 Dynamic Performance (35MHz Encode Rate)

LAYOUT SUGGESTIONS

Designs which use the AD9048 or any other high-speed device must follow some basic layout rules to insure optimum performance.

The first requirement is to have a large, low impedance ground plane under and around the converter. If the system uses separate analog and digital grounds, both should be connected solidly together and to the ground plane as close to the AD9048 as practical, to avoid ground loop currents.

Ceramic 0.1μF decoupling capacitors should be placed as close as possible to the supply pins of the AD9048. For decoupling low frequency signals, use 10μF tantalum capacitors, also connected as close as practical to voltage supply pins.

Within the AD9048, reference currents may vary because of coupling between the clock and input signals. Because of this, it is important that the ends of the reference ladder, R_T (Pin 18) and R_B (Pin 28), be connected to low impedances (as measured from ground).

If the AD9048 is being used in a circuit in which the reference is not varied, a bypass capacitor to ground is strongly recommended. In applications which use varying references, they must be driven from a low impedance source.

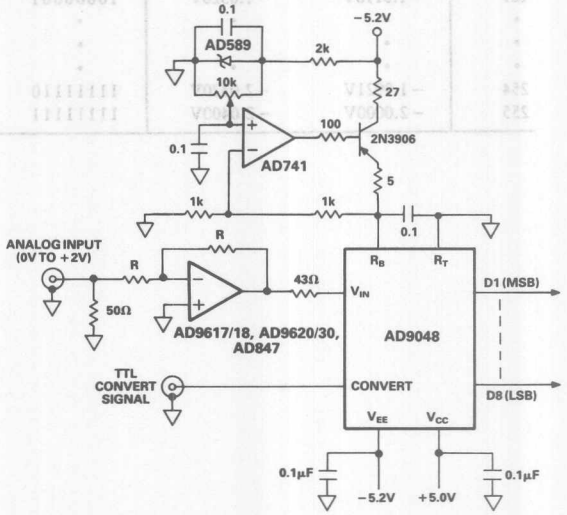
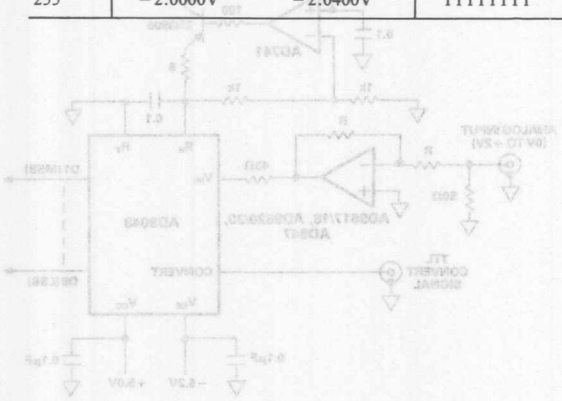
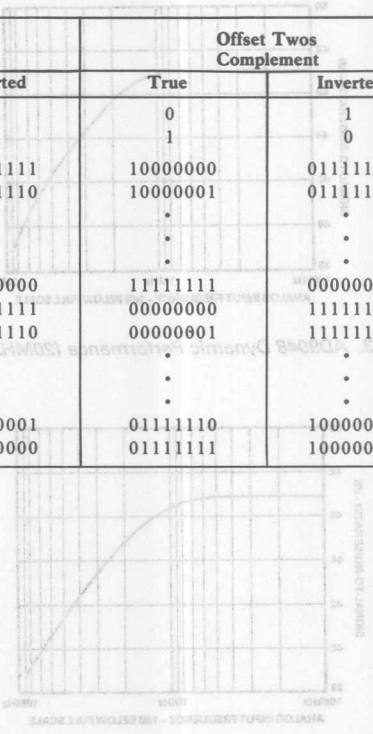


Figure 5. AD9048 Typical Connections

Step	Range		Binary		Offset Twos Complement	
			True	Inverted	True	Inverted
	−2.000V FS	−2.0480V FS	NMINV = 1	0	0	1
	7.8431mV Step	8.000mV Step	NLINV = 1	0	1	0
000	0.0000V	0.0000V	00000000	11111111	10000000	01111111
001	−0.0078V	−0.0080V	00000001	11111110	10000001	01111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
127	−0.9961V	−1.0160V	01111111	10000000	11111111	00000000
128	−1.0039V	−1.0240V	10000000	01111111	00000000	11111111
129	−1.0118V	−1.0320V	10000001	01111110	00000001	11111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
254	−1.9921V	−2.0320V	11111110	00000001	01111110	10000001
255	−2.0000V	−2.0400V	11111111	00000000	01111111	10000000





Dual 8-Bit, 50 MSPS A/D Converter

AD9058

FEATURES
Two Matched ADCs on Single Chip
50 MSPS Conversion Speed
On-Board Voltage Reference
Low Power (<1W)
Low Input Capacitance (10 pF)
±5 V Power Supplies
Flexible Input Range

APPLICATIONS
Quadrature Demodulation for Communications
Digital Oscilloscopes
Electronic Warfare
Radar

GENERAL DESCRIPTION

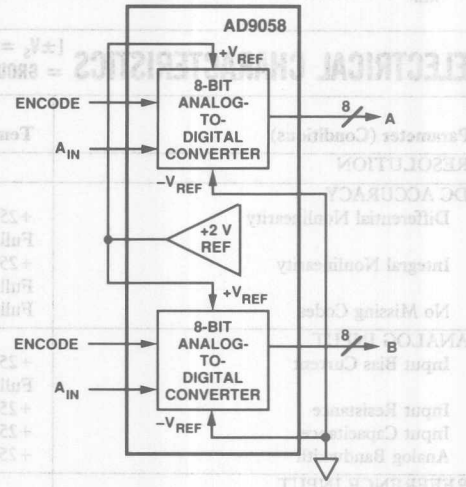
The AD9058 combines two independent high performance 8-bit analog-to-digital converters (ADCs) on a single monolithic IC. Combined with an optional on-board voltage reference, the AD9058 provides a cost effective alternative for systems requiring two or more ADCs.

Dynamic performance (SNR, ENOB) is optimized to provide up to 50 MSPS conversion rates. The unique architecture results in low input capacitance while maintaining high performance and low power (<0.5 watt/channel). Digital inputs and outputs are TTL compatible.

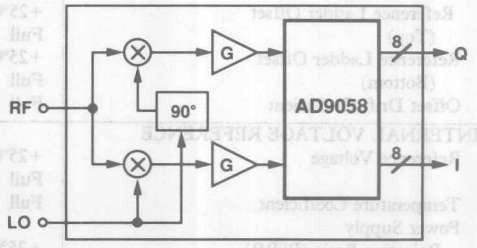
Performance has been optimized for an analog input of 2 V p–p (±1 V; 0 to +2 V). Using the on-board +2 V voltage reference, the AD9058 can be set up for unipolar positive operation (0 to +2 V). This internal voltage reference can drive both ADCs.

Commercial (0°C to +70°C) and military (−55°C to +125°C) temperature range parts are available. Parts are supplied in hermetic 48-pin DIP and 44-pin "J" lead packages.

FUNCTIONAL BLOCK DIAGRAM



QUADRATURE RECEIVER



AD9058—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Analog Input	−1.5 V to +2.5 V
$+V_S$	+6 V
$-V_S$	+0.8 V to −6 V[2]
Digital Inputs	−0.5 V to $+V_S$
Digital Output Current	20 mA
Voltage Reference Current	53 mA
$+V_{REF}$	+2.5 V
$-V_{REF}$	−1.5
Operating Temperature Range	
AD9508JD/JJ/KD/KJ	0°C to +70°C
Maximum Junction Temperature[3]	
AD9058JD/JJ/KD/KJ	+175°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

ELECTRICAL CHARACTERISTICS

[$\pm V_S$ = ±5 V; V_{REF} = +2 V (internal); ENCODE = 40 MSPS; A_{IN} = 0 V to +2 V; $-V_{REF}$ = GROUND, unless otherwise noted.][2] All specifications apply to either of the two ADCs.

Parameter (Conditions)	Temp	Test Level	AD9058JD/JJ Min	AD9058JD/JJ Typ	AD9058JD/JJ Max	AD9058KD/KJ Min	AD9058KD/KJ Typ	AD9058KD/KJ Max	Units
RESOLUTION			8			8			Bits
DC ACCURACY									
Differential Nonlinearity	+25°C	I		0.25	0.65		0.25	0.5	LSB
	Full	VI			0.8			0.7	LSB
Integral Nonlinearity	+25°C	I		0.5	1.3		0.5	1.0	LSB
	Full	VI			1.4			1.25	LSB
No Missing Codes	Full	VI	GUARANTEED			GUARANTEED			
ANALOG INPUT									
Input Bias Current	+25°C	I		75	170		75	170	μA
	Full	VI			340			340	μA
Input Resistance	+25°C	I	12	28		12	28		kΩ
Input Capacitance	+25°C	IV		10	15		10	15	pF
Analog Bandwidth	+25°C	V		175			175		MHz
REFERENCE INPUT									
Reference Ladder Resistance	+25°C	I	120	170	220	120	170	220	Ω
	Full	VI	80		270	80		270	Ω
Ladder Tempco	Full	V		0.45			0.45		Ω/°C
Reference Ladder Offset	+25°C	I		8	16		8	16	mV
(Top)	Full	VI			24			24	mV
Reference Ladder Offset	+25°C	I		8	23		8	23	mV
(Bottom)	Full	VI			33			33	mV
Offset Drift Coefficient	Full	V		50			50		μV/°C
INTERNAL VOLTAGE REFERENCE									
Reference Voltage	+25°C	I	1.95	2.0	2.20	1.95	2.0	2.20	V
	Full	VI	1.90		2.25	1.90		2.25	V
Temperature Coefficient	Full	V		150			150		μV/°C
Power Supply									
Rejection Ratio (PSRR)	+25°C	I		10	25		10	25	mV/V
SWITCHING PERFORMANCE									
Maximum Conversion Rate[4]	+25°C	I		50		50	60		MSPS
Aperture Delay (t_A)	+25°C	IV	0.1	0.8	1.5	0.1	0.8	1.5	ns
Aperture Delay Matching	+25°C	IV		0.2	0.5		0.2	0.5	ns
Aperture Uncertainty (Jitter)	+25°C	V		10			10		ps, rms
Output Delay (Valid) (t_V)[4]	+25°C	I		8		5	8		ns
Output Delay (t_V) Tempco	Full	V		16			16		ps/°C
Propagation Delay (t_{PD})[4]	+25°C	I		12			12	19	ns
Propagation Delay (t_{PD}) Tempco	Full	V		−16			−16		ps/°C
Output Time Skew	+25°C	V		1			1		ns
ENCODE INPUT									
Logic "1" Voltage	Full	VI	2			2			V
Logic "0" Voltage	Full	VI			0.8			0.8	V
Logic "1" Current	Full	VI			600			600	μA
Logic "0" Current	Full	VI			1000			1000	μA
Input Capacitance	+25°C	V		5			5		pF
Pulse Width (High)	+25°C	I		8		8			ns
Pulse Width (Low)	+25°C	I		8		8			ns

Parameter (Conditions)	Temp	Level	Min	Typ	Max	Min	Typ	Max	Units
DYNAMIC PERFORMANCE									
Transient Response	+25°C	V		2			2		ns
Overvoltage Recovery Time	+25°C	V		2			2		ns
Effective Number of Bits (ENOB)[5]									
Analog Input @ 2.3 MHz	+25°C	I		7.7		7.2	7.7		Bits
@ 10.3 MHz	+25°C	I		7.4		7.1	7.4		Bits
Signal-to-Noise Ratio[5]									
Analog Input @ 2.3 MHz	+25°C	I		48		45	48		dB
@ 10.3 MHz	+25°C	I		46		44	46		dB
Signal-to-Noise Ratio[5] (Without Harmonics)									
Analog Input @ 2.3 MHz	+25°C	I		48		46	48		dB
@ 10.3 MHz	+25°C	I		47		45	47		dB
2nd Harmonic Distortion									
Analog Input @ 2.3 MHz	+25°C	I		58		48	58		dBc
@ 10.3 MHz	+25°C	I		58		48	58		dBc
3rd Harmonic Distortion									
Analog Input @ 2.3 MHz	+25°C	I		58		50	58		dBc
@ 10.3 MHz	+25°C	I		58		50	58		dBc
Crosstalk Rejection[6]	+25°C	IV		60		48	60		dBc
DIGITAL OUTPUTS									
Logic "1" Voltage (I_{OH} = 2 mA)	Full	VI	2.4			2.4			V
Logic "0" Voltage (I_{OL} = 2 mA)	Full	VI			0.4			0.4	V
POWER SUPPLY[7]									
$+V_S$ Supply Current	Full	VI		127	154		127	154	mA
$-V_S$Supply Current	Full	VI		27	38		27	38	mA
Power Dissipation	Full	VI		770	960		770	960	mW

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]For applications in which $+V_S$ may be applied before $-V_S$, or $+V_S$ current is not limited to 500 mA, a reverse biased clamping diode should be inserted between ground and $-V_S$ to prevent destructive latch up. See section entitled "Using the AD9058."

[3]Typical thermal impedances: 44-pin hermetic J-Leaded ceramic package: θ_{JA} = 86.4°C/W; θ_{JC} = 24.9°C/W; 48-pin hermetic DIP θ_{JA} = 40°C/W; θ_{JC} = 12°C/W.

[4]To achieve guaranteed conversion rate, connect each data output to ground through a 2 kΩ pull-down resistor.

[5]SNR performance limits for the 48-pin DIP "D" package are 1 dB less than shown. ENOB limits are degraded by 0.3 dB. SNR and ENOB measured with analog input signal 1 dB below full scale at specified frequency.

[6]Crosstalk rejection measured with full-scale signals of different frequencies (2.3 MHz and 3.5 MHz) applied to each channel. With both signals synchronously encoded at 40 MSPS, isolation of the undesired frequency is measured with an FFT.

[7]Applies to both A/Ds and includes internal ladder dissipation.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

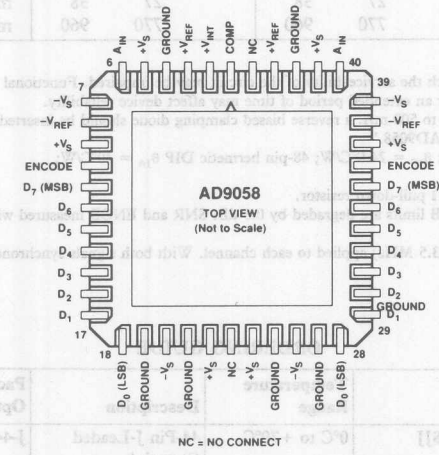
Model	Temperature Range	Description	Package Option*
AD9058JJ	0°C to +70°C	44-Pin J-Leaded Ceramic†	J-44
AD9058KJ	0°C to +70°C	44-Pin J-Leaded Ceramic, AC Tested	J-44
AD9058TJ/883#	−55°C to +125°C	44-Pin J-Leaded Ceramic, AC Tested	J-44
AD9058JD	0°C to +70°C	48-Pin Ceramic DIP	D-48
AD9058KD	0°C to +70°C	48-Pin Ceramic DIP, AC Tested	D-48
AD9058TD/883#	−55°C to +125°C	48-Pin Ceramic DIP, AC Tested	D-48
AD9058/PCB	0°C to +70°C	AD9058 Evaluation Board (J-Lead)	

*D = Hermetic Ceramic DIP Package; J = Leaded Ceramic Package. For outline information see Package Information section.

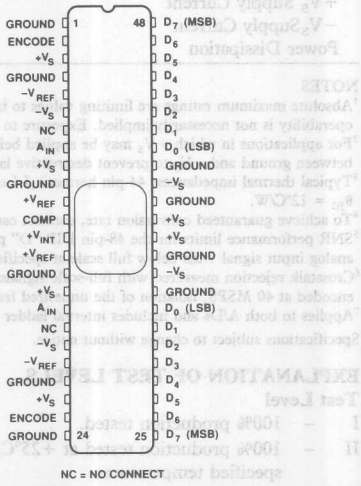
†Hermetically sealed ceramic package; footprint equivalent to PLCC.

#For specifications, refer to Analog Devices Military Products Databook.

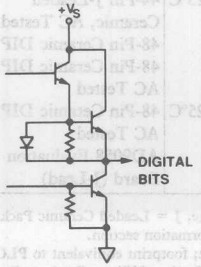
J-Lead Pin Number ADC-A	J-Lead Pin Number ADC-B	Name	Function	Ceramic DIP Pin Number ADC-A	Ceramic DIP Pin Number ADC-B
3	43	$+V_{REF}$	Top of internal voltage reference ladder.	14	11
4	42	GROUND	Analog ground return.	15	10
5	41	$+V_S$	Positive 5 V analog supply voltage.	16	9
6	40	AIN	Analog input voltage.	17	8
7	39	$-V_S$	Negative 5 V supply voltage.	19	6
8	38	$-V_{REF}$	Bottom of internal voltage reference ladder.	20	5
9	37	$+V_S$	Positive 5 V digital supply voltage.	22	3
10	36	ENCODE	TTL compatible convert command.	23	2
11	35	D7 (MSB)	Most significant bit of TTL digital output.	25	48
12–17	34–29	D6–D1	TTL compatible digital output bits.	26–31	47–42
18	28	D0 (LSB)	Least significant bit of TTL digital output.	32	41
19	27	GROUND	Digital ground return.	21, 24, 33	1, 4, 40
20	26	$-V_S$	Negative 5 V supply voltage.	34	39
21	25	GROUND	Analog ground return.	35	38
22	24	$+V_S$	Positive 5 V analog supply voltage.	36	37
COMMON PINS				COMMON PINS	
1		COMP	Connection for external (0.1 μF) compensation capacitor.	12	
2		$+V_{INT}$	Internal +2 V reference; can drive $+V_{REF}$ for both ADCs.	13	



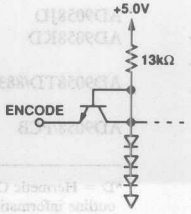
AD9058JJ/KJ Pinouts



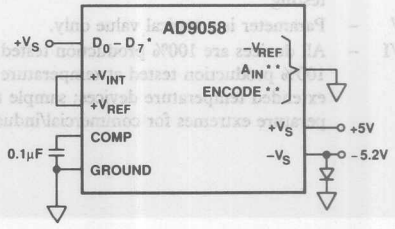
AD9058JD/KD Pinouts



AD9058 Equivalent Digital Outputs



AD9058 Equivalent Encode Circuit



AD9058 Burn-In Connections

THEORY OF OPERATION

The AD9058 contains two separate 8-bit analog-to-digital converters (ADCs) on a single silicon die. The two devices can be operated independently with separate analog inputs, voltage references, and clocks.

In a traditional flash converter, 256 input comparators are required to make the parallel conversion for 8-bit resolution. This is in marked contrast to the scheme used in the AD9058, as shown in Figure 1.

Unlike traditional "flash," or parallel, converters, each of the two ADCs in the AD9058 utilizes a patented interpolating architecture to reduce circuit complexity, die size, and input capacitance. These advantages accrue because, compared to a conventional flash design, only half the normal number of input comparator cells is required to accomplish the conversion.

In this unit, each of the two independent ADCs uses only 128 (2^7) comparators to make the conversion. The conversion for the seven most significant bits (MSBs) is performed by the 128 comparators. The value of the least significant bit (LSB) is determined by interpolation between adjacent comparators in the decoding register. A proprietary decoding scheme processes the comparator outputs and provides an 8-bit code to the output register of each ADC; the scheme also minimizes error codes.

Analog input range is established by the voltages applied at the voltage reference inputs ($+V_{REF}$ and $-V_{REF}$). The AD9058 can operate from 0 V to +2 V using the internal voltage reference, or anywhere between −1 V and +2 V using external references. Input range is limited to 2 V p–p when using external references. The internal resistor ladder divides the applied voltage reference into 128 steps, with each step representing two 8-bit quantization levels.

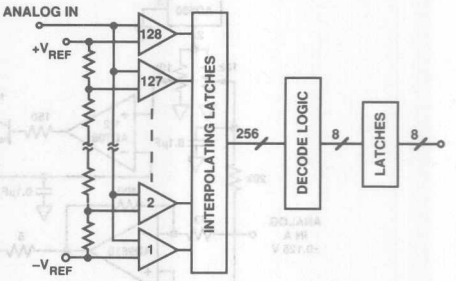


Figure 1. AD9058 Comparator Block Diagram

The on-board voltage reference, $+V_{INT}$, is a bandgap reference which has sufficient drive capability for both reference ladders. It provides a +2 V reference that can drive both ADCs in the AD9058 for unipolar positive operation (0 V to +2 V).

USING THE AD9058

Refer to Figure 2.

Using the internal voltage reference connected to both ADCs as shown reduces the number of external components required to create a complete data acquisition system. The input ranges of the ADCs are positive unipolar in this configuration, ranging from 0 V to +2 V. Bipolar input signals are buffered, amplified, and offset into the proper input range of the ADC using a good low distortion amplifier such as the AD9617 or AD9618.

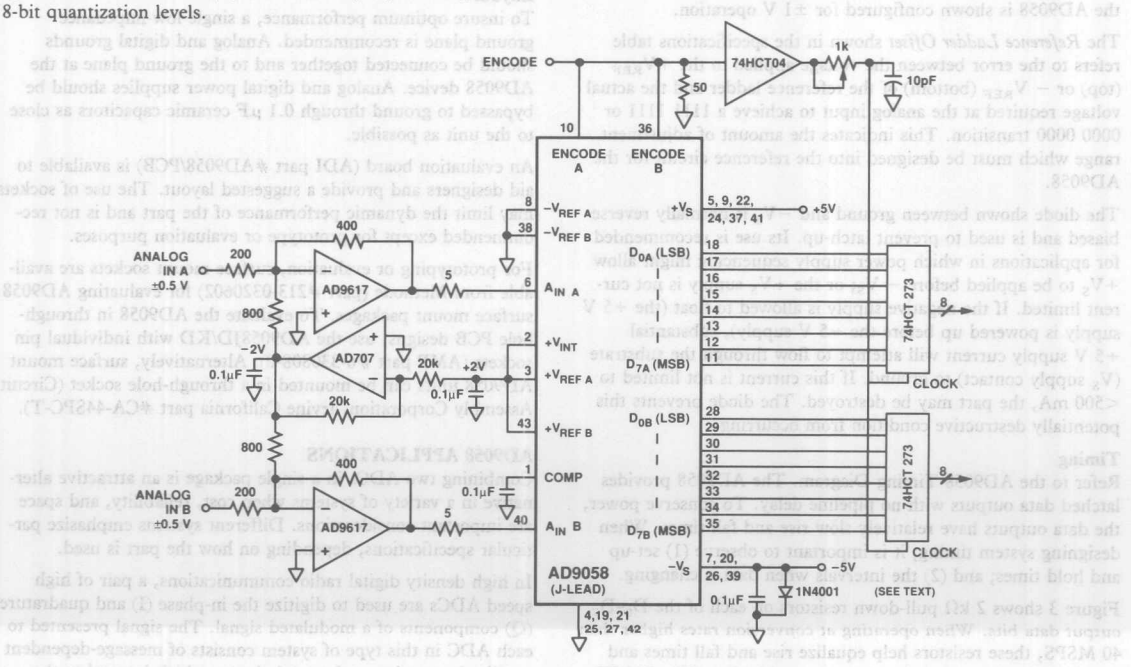


Figure 2. AD9058 Using Internal +2 V Voltage Reference

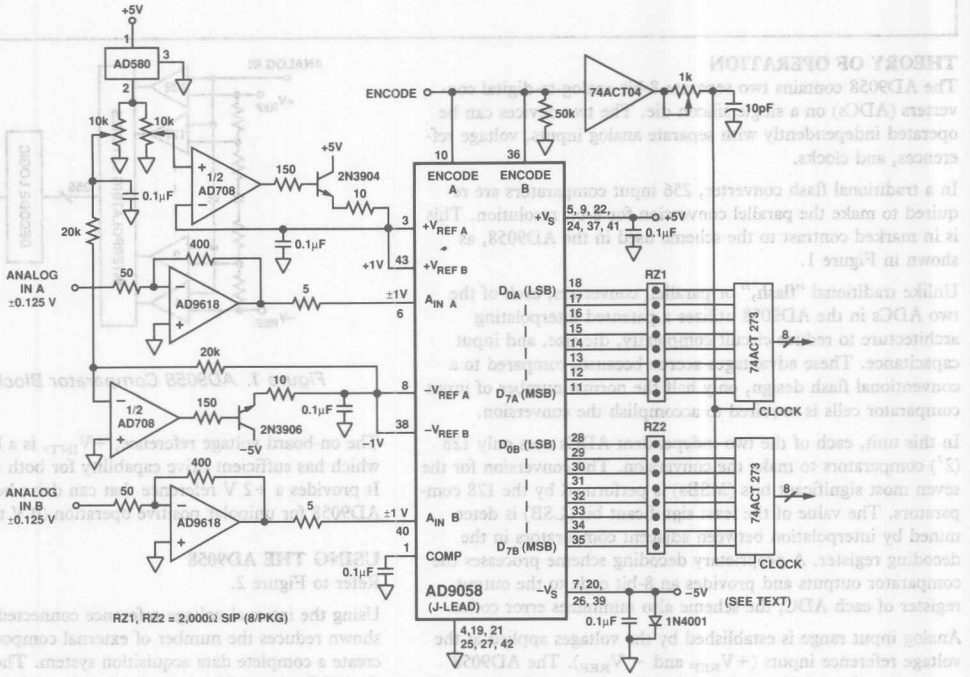


Figure 3. AD9058 Using External Voltage References

The AD9058 offers considerable flexibility in selecting the analog input ranges of the ADCs; the two independent ADCs can even have different input ranges if required. In Figure 3 above, the AD9058 is shown configured for ±1 V operation.

The *Reference Ladder Offset* shown in the specifications table refers to the error between the voltage applied to the $+V_{REF}$ (top) or $-V_{REF}$ (bottom) of the reference ladder and the actual voltage required at the analog input to achieve a 1111 1111 or 0000 0000 transition. This indicates the amount of adjustment range which must be designed into the reference circuit for the AD9058.

The diode shown between ground and $-V_S$ is normally reverse biased and is used to prevent latch-up. Its use is recommended for applications in which power supply sequencing might allow $+V_S$ to be applied before $-V_S$; or the $+V_S$ supply is not current limited. If the negative supply is allowed to float (the +5 V supply is powered up before the −5 V supply), substantial +5 V supply current will attempt to flow through the substrate (V_S supply contact) to ground. If this current is not limited to <500 mA, the part may be destroyed. The diode prevents this potentially destructive condition from occurring.

Timing

Refer to the AD9058 Timing Diagram. The AD9058 provides latched data outputs with no pipeline delay. To conserve power, the data outputs have relatively slow rise and fall times. When designing system timing, it is important to observe (1) set-up and hold times; and (2) the intervals when data is changing.

Figure 3 shows 2 kΩ pull-down resistors on each of the D_0–D_7 output data bits. When operating at conversion rates higher than 40 MSPS, these resistors help equalize rise and fall times and ease latching the output data into external latches. The 74ACT logic family devices have short set-up and hold times and are the recommended choices for speeds of 40 MSPS or more.

Layout

To insure optimum performance, a single low-impedance ground plane is recommended. Analog and digital grounds should be connected together and to the ground plane at the AD9058 device. Analog and digital power supplies should be bypassed to ground through 0.1 μF ceramic capacitors as close to the unit as possible.

An evaluation board (ADI part #AD9058/PCB) is available to aid designers and provide a suggested layout. The use of sockets may limit the dynamic performance of the part and is not recommended except for prototype or evaluation purposes.

For prototyping or evaluation, surface mount sockets are available from Methode (part #213-0320602) for evaluating AD9058 surface mount packages. To evaluate the AD9058 in through-hole PCB designs, use the AD9058JD/KD with individual pin sockets (AMP part #6-330808-0). Alternatively, surface mount AD9058 units can be mounted in a through-hole socket (Circuit Assembly Corporation, Irvine California part #CA-44SPC-T).

AD9058 APPLICATIONS

Combining two ADCs in a single package is an attractive alternative in a variety of systems when cost, reliability, and space are important considerations. Different systems emphasize particular specifications, depending on how the part is used.

In high density digital radio communications, a pair of high speed ADCs are used to digitize the in-phase (I) and quadrature (Q) components of a modulated signal. The signal presented to each ADC in this type of system consists of message-dependent amplitudes varying at the symbol rate, which is equal to the sample rates of the converters.

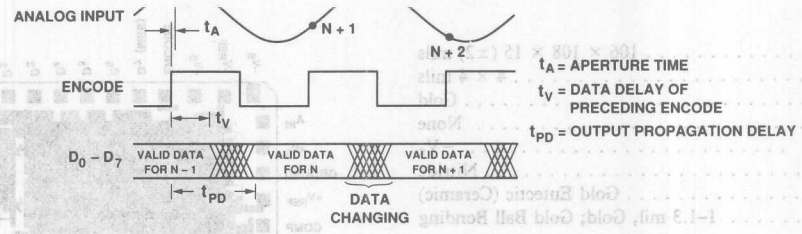


Figure 4. AD9058 Timing Diagram

Figure 5 below shows what the analog input to the AD9058 would look like when observed relative to the sample clock. Signal-to-noise ratio (SNR), transient response, and sample rate are all critical specifications in digitizing this "eye pattern."

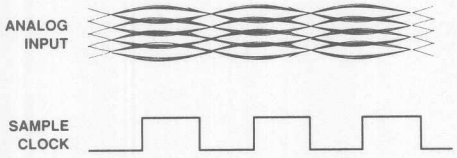


Figure 5. AD9058 I and Q Input Signals

Receiver sensitivity is limited by the SNR of the system. For the ADC, SNR is measured in the frequency domain and calculated with a Fast Fourier Transform (FFT). The *signal-to-noise ratio* equals the ratio of the fundamental component of the signal (rms amplitude) to the rms level of the noise. Noise is the sum of all other spectral components, including harmonic distortion, but excluding dc.

Although the signal being sampled does not have a significant slew rate at the instant it is encoded, dynamic performance of the ADC and the system is still critical. *Transient response* is the time required for the AD9058 to achieve full accuracy when a step function input is applied. *Overvoltage recovery time* is the interval required for the AD9058 to recover to full accuracy after an overdriven analog input signal is reduced to its input range.

Time domain performance of the ADC is also extremely important in digital oscilloscopes. When a track (sample)-and-hold is used ahead of the ADC, its operation becomes similar to that described above for receivers.

The dynamic response to high-frequency inputs can be described by the *effective number of bits* (ENOB). The *effective number of bits* is calculated with a sine wave curve fit and is expressed as:

$$ENOB = N - LOG_2 [Error\ (measured)/Error\ (ideal)]$$

where N is the resolution (number of bits) and measured error is actual rms error calculated from the converter's outputs with a pure sine wave applied as the input.

Maximum conversion rate is defined as the encode (sample) rate at which SNR of the lowest frequency analog test signal drops no more than 3 dB below the guaranteed limit.

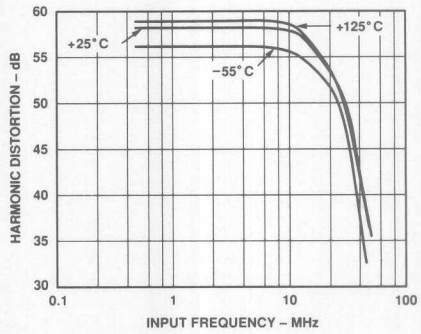


Figure 6. Harmonic Distortion vs. Analog Input Frequency

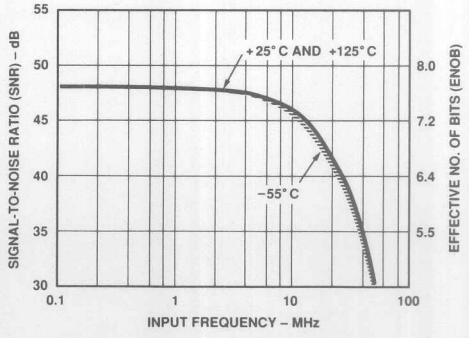
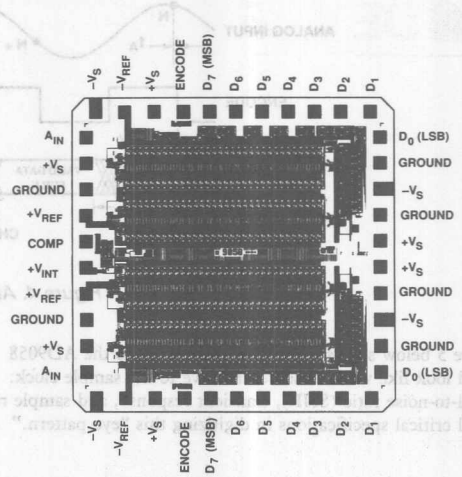
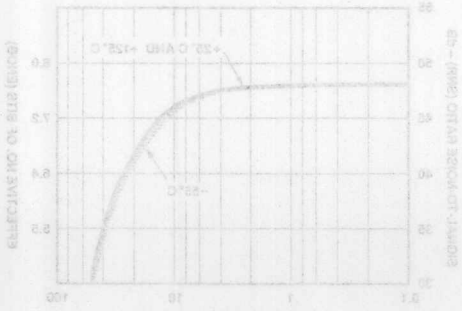


Figure 7. AD9058 Dynamic Performance vs. Analog Input Frequency

MECHANICAL INFORMATION

Die Dimensions	106 × 108 × 15 (±2) mils
Pad Dimensions	4 × 4 mils
Metalization	Gold
Backing	None
Substrate Potential	$-V_S$
Passivation	Nitride
Die Attach	Gold Eutectic (Ceramic)
Bond Wire	1–1.3 mil, Gold; Gold Ball Bonding





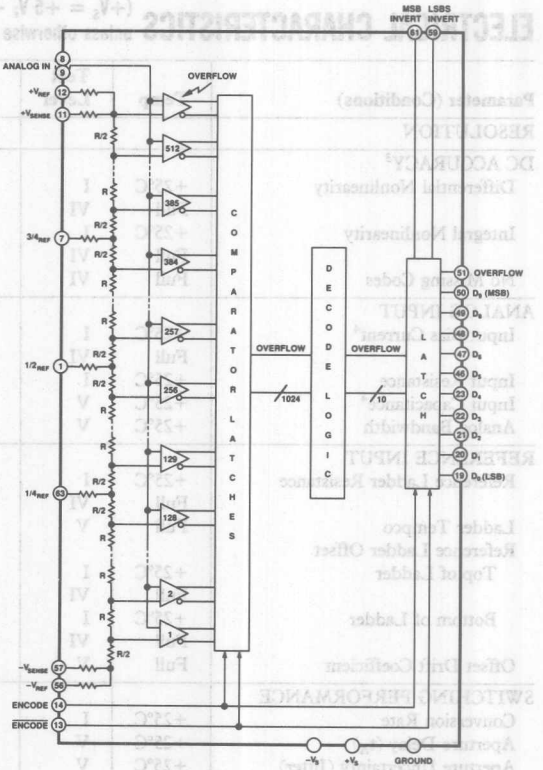
10-Bit, 75 MSPS A/D Converter

AD9060

FEATURES
Monolithic 10-Bit/75 MSPS Converter
ECL Outputs
Bipolar (±1.75 V) Analog Input
57 dB SNR @ 2.3 MHz Input
Low (45 pF) Input Capacitance
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Digital Oscilloscopes
Medical Imaging
Professional Video
Radar Warning/Guidance Systems
Infrared Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9060 A/D converter is a 10-bit monolithic converter capable of word rates of 75 MSPS and above. Innovative architecture using 512 input comparators instead of the traditional 1024 required by other flash converters reduces input capacitance and improves linearity.

Inputs and outputs are ECL-compatible, which makes the AD9060 the recommended choice for systems with conversion rates >30 MSPS, to minimize system noise. An overflow bit is provided to indicate analog input signals greater than $+V_{SENSE}$.

Voltage sense lines are provided to insure accurate driving of the $\pm V_{REF}$ voltages applied to the units. Quarter-point taps on the resistor ladder help optimize the integral linearity of the unit.

Either 68-pin ceramic leaded (gull wing) packages or ceramic LCCs are available and are specifically designed for low thermal impedances. Two performance grades for temperatures of both 0 to +70°C and −55°C to +125°C ranges are offered to allow the user to select the linearity best suited for each application. Dynamic performance is fully characterized and production tested at +25°C. MIL-STD-883 units are available.

The AD9060 A/D converter is available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current AD9060/883B data sheet for detailed specifications.

AD9060—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$	+6 V
$-V_S$	−6 V
ANALOG IN	−2 V to +2 V
$+V_{REF}$, $-V_{REF}$, $3/4_{REF}$, $1/2_{REF}$, $1/4_{REF}$	−2 V to +2 V
$+V_{REF}$ to $-V_{REF}$	4.0 V
ENCODE, $\overline{\text{ENCODE}}$	0 V to $-V_S$
$3/4_{REF}$, $1/2_{REF}$, $1/4_{REF}$ Current	±10 mA
Digital Output Current	20 mA
Operating Temperature	
AD9060JE/KE/JZ/KZ	0 to +70°C
Storage Temperature	−65°C to +150°C
Maximum Junction Temperature[2]	+175°C
Lead Soldering Temp (10 sec)	+300°C

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V; $-V_S$ = −5.2 V; $\pm V_{SENSE}$ = ±1.75 V; ENCODE = 60 MSPS unless otherwise noted)[3]

Parameter (Conditions)	Temp	Test Level	AD9060JE/JZ Min	AD9060JE/JZ Typ	AD9060JE/JZ Max	AD9060KE/KZ Min	AD9060KE/KZ Typ	AD9060KE/KZ Max	Units
RESOLUTION			10			10			Bits
DC ACCURACY[3]									
Differential Nonlinearity	+25°C	I		1.0	1.25		0.75	1.0	LSB
	Full	VI			1.5			1.25	LSB
Integral Nonlinearity	+25°C	I		1.25	2.0		1.0	1.5	LSB
	Full	VI			2.5			2.0	LSB
No Missing Codes	Full	VI					Guaranteed		
ANALOG INPUT									
Input Bias Current[4]	+25°C	I		0.4	1.0		0.4	1.0	mA
	Full	VI			2.0			2.0	mA
Input Resistance	+25°C	I	2.0	7.0		2.0	7.0		kΩ
Input Capacitance[4]	+25°C	V		45			45		pF
Analog Bandwidth	+25°C	V		175			175		MHz
REFERENCE INPUT									
Reference Ladder Resistance	+25°C	I	22	37	56	22	37	56	Ω
	Full	VI	14		66	14		66	Ω
Ladder Tempco	Full	V		0.1			0.1		Ω/°C
Reference Ladder Offset									
Top of Ladder	+25°C	I		45	90		45	90	mV
	Full	VI			90			90	mV
Bottom of Ladder	+25°C	I		45	90		45	90	mV
	Full	VI			90			90	mV
Offset Drift Coefficient	Full	V		50			50		µV/°C
SWITCHING PERFORMANCE									
Conversion Rate	+25°C	I	75			75			MSPS
Aperture Delay (t_A)	+25°C	V		1			1		ns
Aperture Uncertainty (Jitter)	+25°C	V		5			5		ps, rms
Output Delay (t_{OD})[5]	+25°C	I	2	4	9	2	4	9	ns
Output Rise Time	+25°C	I		1	3		1	3	ns
Output Fall Time	+25°C	I		1	3		1	3	ns
Output Time Skew[5]	+25°C	I		1.5	3		1.5	3	ns
DYNAMIC PERFORMANCE									
Transient Response	+25°C	V		10			10		ns
Overvoltage Recovery Time	+25°C	V		10			10		ns
Effective Number of Bits (ENOB)									
f_{IN} = 2.3 MHz	+25°C	I	8.7	9.1		8.7	9.1		Bits
f_{IN} = 10.3 MHz	+25°C	IV	8.0	8.6		8.0	8.6		Bits
f_{IN} = 29.3 MHz	+25°C	IV	7.0	7.4		7.0	7.4		Bits
Signal-to-Noise Ratio[6]									
f_{IN} = 2.3 MHz	+25°C	I	54	56		54	56		dB
f_{IN} = 10.3 MHz	+25°C	I	51	54		51	54		dB
f_{IN} = 29.3 MHz	+25°C	I	44	47		44	47		dB

(CONTINUED)								
Signal-to-Noise Ratio[6]								
(Without Harmonics)								
f_{IN} = 2.3 MHz	+25°C	I	54	56		54	58	dB
f_{IN} = 10.3 MHz	+25°C	I	51	55		51	55	dB
f_{IN} = 29.3 MHz	+25°C	I	46	48		46	48	dB
Harmonic Distortion								
f_{IN} = 2.3 MHz	+25°C	I	61	65		61	65	dBc
f_{IN} = 10.3 MHz	+25°C	I	55	58		55	58	dBc
f_{IN} = 29.3 MHz	+25°C	I	47	50		47	50	dBc
Two-Tone Intermodulation								
Distortion Rejection[7]	+25°C	V		70			70	dBc
Differential Phase	+25°C	V		0.5			0.5	Degree
Differential Gain	+25°C	V		1			1	%
ENCODE INPUT								
Logic "1" Voltage	Full	VI	−1.1			−1.1		V
Logic "0" Voltage	Full	VI			−1.5		−1.5	V
Logic "1" Current	Full	VI		150	300		150	300	μA
Logic "0" Current	Full	VI		150	300		150	300	μA
Input Capacitance	+25°C	V		5			5		pF
Pulse Width (High)	+25°C	I	6			6			ns
Pulse Width (Low)	+25°C	I	6			6			ns
DIGITAL OUTPUTS								
Logic "1" Voltage	Full	VI	−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			−1.5	V
POWER SUPPLY								
$+V_S$ Supply Current	+25°C	VI		420	500		420	500	mA
	Full	VI			500			500	mA
$-V_S$ Supply Current	+25°C	VI		150	180		150	180	mA
	Full	VI			190			190	mA
Power Dissipation	+25°C	VI		2.8	3.3		2.8	3.3	W
	Full	VI			3.5			3.5	W
Power Supply Rejection								
Ratio (PSRR)[8]	Full	VI		6	10		6	10	mV/V

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances (part soldered onto board): 68-pin leaded ceramic chip carrier: θ_{JC} = 1°C/W; θ_{JA} = 17°C/W (no air flow); θ_{JA} = 15°C/W (air flow = 500 LFM). 68-pin ceramic LCC: θ_{JC} = 2.6°C/W; θ_{JA} = 15°C/W (no air flow); θ_{JA} = 13°C/W (air flow = 500 LFM).

[3]$3/4_{REF}$, $1/2_{REF}$, and $1/4_{REF}$ reference ladder taps are driven from dc sources at +0.875 V, 0 V, and −0.875 V, respectively. Outputs terminated through 100 Ω to −2.0 V; C_L < 4 pF. Accuracy of the overflow comparator is not tested and not included in linearity specifications.

[4]Measured with ANALOG IN = $+V_{SENSE}$.

[5]Output delay measured as worst-case time from 50% point of the rising edge of ENCODE to 50% point of the slowest rising or falling edge of D_0–D_9. Output skew measured as worst-case difference in output delay among D_0–D_9.

[6]RMS signal to rms noise with analog input signal 1 dB below full scale at specified frequency.

[7]Intermodulation measured with analog input frequencies of 2.3 MHz and 3.0 MHz at 7 dB below full scale.

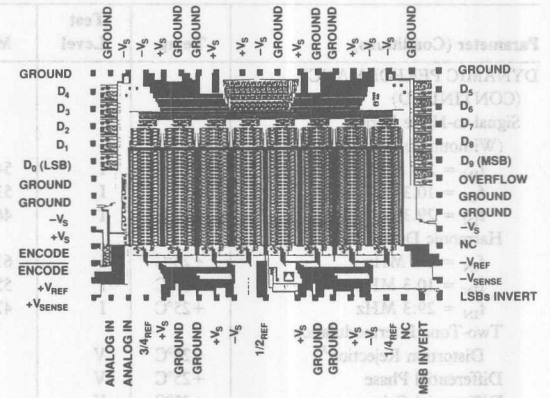
[8]Measured as the ratio of the worst-case change in transition voltage of a single comparator for a 5% change in $+V_S$ or $-V_S$.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.



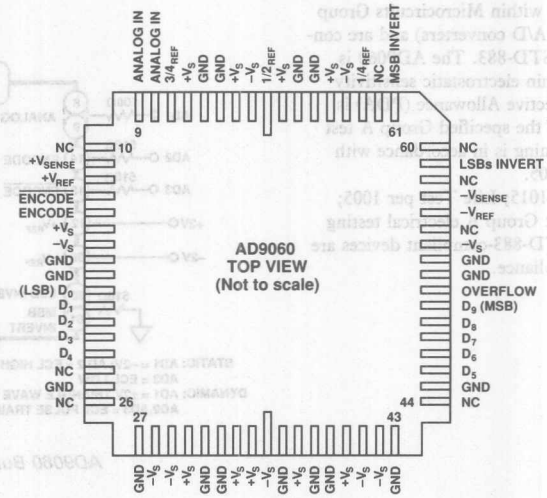
ORDERING GUIDE

Device	Temperature Range	Package Option[1]
AD9060JZ	0 to +70°C	Z-68
AD9060JE	0 to +70°C	E-68A
AD9060KZ	0 to +70°C	Z-68
AD9060KE	0 to +70°C	E-68A
AD9060SZ[2]	−55°C to +125°C	Z-68
AD9060SE[2]	−55°C to +125°C	E-68A
AD9060TZ[2]	−55°C to +125°C	Z-68
AD9060TE[2]	−55°C to +125°C	E-68A
AD9060/PCB	0 to +70°C	Evaluation Board

NOTES
[1]E = Ceramic Leadless Chip Carrier; Z = Ceramic Leaded Chip Carrier. For outline information see Package Information section.
[2]For specifications, refer to Analog Devices *Military Products Databook*.

DIE LAYOUT AND MECHANICAL INFORMATION

Die Dimensions . . . . . 206 × 140 × 15 (±2) mils
Pad Dimensions . . . . . 4 × 4 mils
Metalization . . . . . Gold
Backing . . . . . None
Substrate Potential . . . . . $-V_S$
Passivation . . . . . Nitride



AD9060 Pin Designations

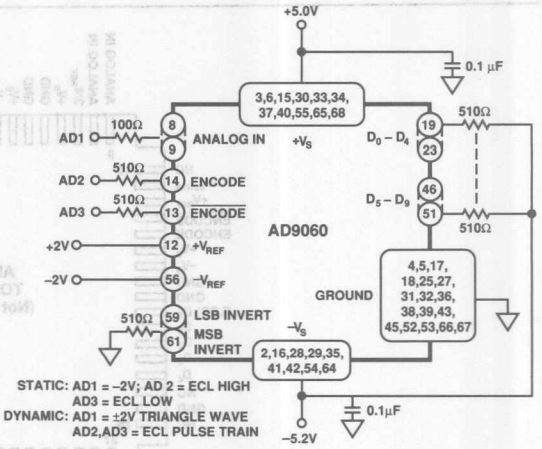
AD9060 PIN DESCRIPTIONS

Pin No.	Name	Function
1	$1/2_{REF}$	Midpoint of internal reference ladder.
2, 16, 28, 29, 35, 41, 42, 54, 64	$-V_S$	Negative supply voltage; nominally −5.2 V ±5%.
3, 6, 15, 30, 33, 34, 37, 40, 65, 68	$+V_S$	Positive supply voltage; nominally +5 V ±5%.
4, 5, 17, 18, 25, 27, 31, 32, 36, 38, 39, 43, 45, 52, 53, 66, 67	GROUND	All ground pins should be connected together and to low-impedance ground plane.
7	$3/4_{REF}$	Three-quarter point of internal reference ladder.
8, 9	ANALOG IN	Analog input; nominally between ±1.75 V.
11	$+V_{SENSE}$	Voltage sense line to most positive point on internal resistor ladder. Normally +1.75 V.
12	$+V_{REF}$	Voltage force connection for top of internal reference ladder. Normally driven to provide +1.75 V at $+V_{SENSE}$.
13	$\overline{\text{ENCODE}}$	Differential ECL convert signal which starts digitizing process.
14	ENCODE	ECL-compatible convert command used to begin digitizing process.
19–23, 46–50	D_0–D_9	ECL-compatible digital output data.
51	OVERFLOW	ECL-compatible output indicating ANALOG IN > $+V_{SENSE}$.
56	$-V_{REF}$	Voltage force connection for bottom of internal reference ladder. Normally driven to provide −1.75 V at $-V_{SENSE}$.
57	$-V_{SENSE}$	Voltage sense line to most negative point on internal resistor ladder. Normally −1.75 V.
59	LSBs INVERT	Normally grounded. When connected to $+V_S$, lower order bits (D_0–D_8) are inverted. Not ECL-compatible.
61	MSB INVERT	Normally grounded. When connected to $+V_S$, most significant bit (MSB; D_9) is inverted. Not ECL-compatible.
63	$1/4_{REF}$	One-quarter point of internal reference ladder.

MIL-STD-883 Compliance Information

The AD9060 devices are classified within Microcircuits Group 57, Technology Group D (bipolar A/D converters) and are constructed in accordance with MIL-STD-883. The AD9060 is electrostatic sensitive and falls within electrostatic sensitivity classification Class 1. Percent Defective Allowance (PDA) is computed based on Subgroup 1 of the specified Group A test list. Quality Assurance (QA) screening is in accordance with Alternate Method A of Method 5005.

The following apply: Burn-In per 1015; Life Test per 1005; Electrical Testing per 5004. (Note: Group A electrical testing assumes $T_A = T_C = T_J$.) MIL-STD-883-compliant devices are marked with "C" to indicate compliance.



AD9060 Burn-In Connections

THEORY OF OPERATION

Refer to the AD9060 block diagram. As shown, the AD9060 uses a modified "flash," or parallel, A/D architecture. The analog input range is determined by an external voltage reference ($+V_{REF}$ and $-V_{REF}$), nominally ±1.75 V. An internal resistor ladder divides this reference into 512 steps, each representing two quantization levels. Taps along the resistor ladder ($1/4_{REF}$, $1/2_{REF}$ and $3/4_{REF}$) are provided to optimize linearity. Rated performance is achieved by driving these points at 1/4, 1/2 and 3/4, respectively, of the voltage reference range.

The A/D conversion for the nine most significant bits (MSBs) is performed by 512 comparators. The value of the least significant bit (LSB) is determined by a unique interpolation scheme between adjacent comparators. The decoding logic processes the comparator outputs and provides a 10-bit code to the output stage of the converter.

Flash architecture has an advantage over other A/D architectures because conversion occurs in one step. This means the performance of the converter is limited primarily by the speed and matching of the individual comparators. In the AD9060, an innovative interpolation scheme takes advantage of flash architecture but minimizes the input capacitance, power and device count usually associated with that method of conversion.

These advantages occur because of using only half the normal number of input comparator cells to accomplish the conversion. In addition, a proprietary decoding scheme minimizes error codes. Input control pins allow the user to select from among Binary, Inverted Binary, Twos Complement and Inverted Twos Complement coding (See AD9060 Truth Table).

APPLICATIONS

Many of the specifications used to describe analog/digital converters have evolved from system performance requirements in these applications. Different systems emphasize particular specifications, depending on how the part is used. The following applications highlight some of the specifications and features that make the AD9060 attractive in these systems.

Wideband Receivers

Radar and communication receivers (baseband and direct IF digitization), ultrasound medical imaging, signal intelligence and spectral analysis all place stringent ac performance requirements on analog-to-digital converters (ADCs). Frequency domain characterization of the AD9060 provides signal-to-noise ratio (SNR) and harmonic distortion data to simplify selection of the ADC.

Receiver sensitivity is limited by the *Signal-to-Noise Ratio (SNR)* of the system. The SNR for an ADC is measured in the frequency domain and calculated with a Fast Fourier Transform (FFT). The SNR equals the ratio of the fundamental component of the signal (rms amplitude) to the rms value of the "noise." The noise is the sum of all other spectral components, including harmonic distortion, but excluding dc.

Good receiver design minimizes the level of spurious signals in the system. Spurious signals developed in the ADC are the result of imperfections in the device transfer function (nonlinearities, delay mismatch, varying input impedance, etc.). In the ADC, these spurious signals appear as *Harmonic Distortion*. Harmonic Distortion is also measured with an FFT and is specified as the ratio of the fundamental component of the signal (rms amplitude) to the rms value of the worst case harmonic (usually the 2nd or 3rd).

Two-Tone Intermodulation Distortion (IMD) is a frequently cited specification in receiver design. In narrow-band receivers, third-order IMD products result in spurious signals in the pass band of the receiver. Like mixers and amplifiers, the ADC is characterized with two, equal-amplitude, pure input frequencies. The IMD equals the ratio of the power of either of the two input signals to the power of the strongest third-order IMD signal. Unlike mixers and amplifiers, the IMD does not always behave as it does in linear devices (reduced input levels do not result in predictable reductions in IMD).

Performance graphs provide typical harmonic and SNR data for the AD9060 for increasing analog input frequencies. In choosing an A/D converter, always look at the dynamic range for the analog input frequency of interest. The AD9060 specifications provide guaranteed minimum limits at three analog test frequencies.

Aperture Delay is the delay between the rising edge of the ENCODE command and the instant at which the analog input is sampled. Many systems require simultaneous sampling of more than one analog input signal with multiple ADCs. In these situations, timing is critical and the absolute value of the aperture delay is not as critical as the matching between devices.

Aperture Uncertainty, or jitter, is the sample-to-sample variation in aperture delay. This is especially important when sampling high slew rate signals in wide bandwidth systems. Aperture uncertainty is one of the factors which degrades dynamic performance as the analog input frequency is increased.

Digitizing Oscilloscopes

Oscilloscopes provide amplitude information about an observed waveform with respect to time. Digitizing oscilloscopes must accurately sample this signal, without distorting the information to be displayed.

One figure of merit for the ADC in these applications is *Effective Number of Bits (ENOBs)*. ENOB is calculated with a sine wave curve fit and equals:

$$ENOB = N - LOG_2 [Error\ (measured)/Error\ (ideal)]$$

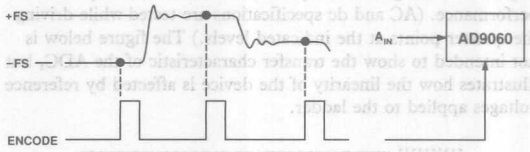
N is the resolution (number of bits) of the ADC. The measured error is the actual rms error calculated from the converter outputs with a pure sine wave input.

The *Analog Bandwidth* of the converter is the analog input frequency at which the spectral power of the fundamental signal is reduced 3 dB from its low frequency value. The analog bandwidth is a good indicator of a converter's slewing capabilities.

The *Maximum Conversion Rate* is defined as the encode rate at which the SNR for the lowest analog signal test frequency tested drops by no more than 3 dB below the guaranteed limit.

Imaging

Visible and infrared imaging systems both require similar characteristics from ADCs. The signal input (from a CCD camera, or multiplexer) is a time division multiplexed signal consisting of a series of pulses whose amplitude varies in direct proportion to the intensity of the radiation detected at the sensor. These varying levels are then digitized by applying encode commands at the correct times, as shown below.



Imaging Application Using AD9060

The actual resolution of the converter is limited by the thermal and quantization noise of the ADC. The low frequency test for SNR or ENOB is a good measure of the noise of the AD9060. At this frequency, the static errors in the ADC determine the useful dynamic range of the ADC.

Although the signal being sampled does not have a significant slew rate, this does not imply dynamic performance is not important. The *Transient Response and Overvoltage Recovery Time* specifications insure that the ADC can track full-scale changes in the analog input sufficiently fast to capture a valid sample.

Transient Response is the time required for the AD9060 to achieve full accuracy when a step function is applied. *Overvoltage Recovery Time* is the time required for the AD9060 to recover to full accuracy after an analog input signal 150% of full scale is reduced to the full-scale range of the converter.

Professional Video

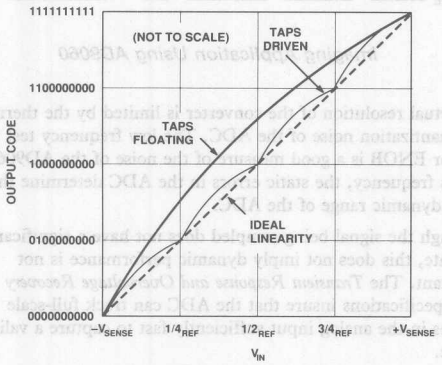
Digital Signal Processing (DSP) is now common in television production. Modern studios rely on digitized video to create state-of-the-art special effects. Video instrumentation also requires high resolution ADCs for studio quality measurement and frame storage.

The AD9060 provides sufficient resolution for these demanding applications. Conversion speed, dynamic performance and analog bandwidth are suitable for digitizing both composite and RGB video sources.

USING THE AD9060

Voltage References

The AD9060 requires that the user provide two voltage references: $+V_{REF}$ and $-V_{REF}$. These two voltages are applied across an internal resistor ladder (nominally 37 Ω) and set the analog input voltage range of the converter. The voltage references should be driven from a stable, low impedance source. In addition to these two references, three evenly spaced taps on the resistor ladder ($1/4_{REF}$, $1/2_{REF}$, $3/4_{REF}$) are available. Providing a reference to these quarter points on the resistor ladder will improve the integral linearity of the converter and improve ac performance. (AC and dc specifications are tested while driving the quarter points at the indicated levels.) The figure below is not intended to show the transfer characteristic of the ADC, but illustrates how the linearity of the device is affected by reference voltages applied to the ladder.

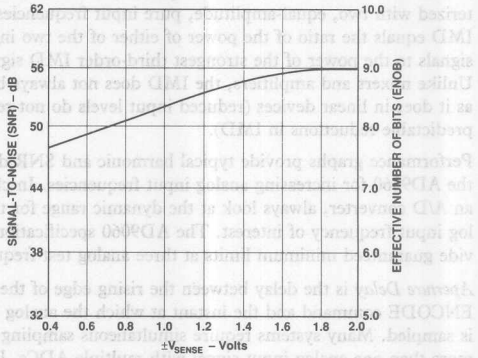


Effect of Reference Taps on Linearity

Resistance between the reference connections and the taps of the first and last comparators causes offset errors. These errors, called "top and bottom of the ladder offsets," can be nulled by using the voltage sense lines, $+V_{SENSE}$ and $-V_{SENSE}$, to adjust the reference voltages. Current through the sense lines should be limited to less than 100 μA. Excessive current drawn through the voltage sense lines will affect the accuracy of the sense line voltage.

The next page shows a reference circuit which nulls out the offset errors using two op amps and provides appropriate voltage references to the quarter-point taps. Feedback from the sense lines causes the op amps to compensate for the offset errors. The two transistors limit the amount of current drawn directly from the op amps; resistors at the base connections stabilize their operation. The 10 kΩ resistors (R1–R4) between the voltage sense lines form an external resistor ladder; the quarter point voltages are taken off this external ladder and buffered by an op amp. The actual values of resistors R1–R4 are not critical, but they should match well and be large enough (≥10 kΩ) to limit the amount of current drawn from the voltage sense lines.

The select resistors (R_S) shown in the schematic (each pair can be a potentiometer) are chosen to adjust the quarter-point voltage references, but are not necessary if R1–R4 match within 0.05%.



AD9060 SNR and ENOB vs. Reference Voltage

An alternative approach for defining the quarter-point references of the resistor ladder is to evaluate the integral linearity error of an individual device, and adjust the voltage at the quarter-points to minimize this error. This may improve the low frequency ac performance of the converter.

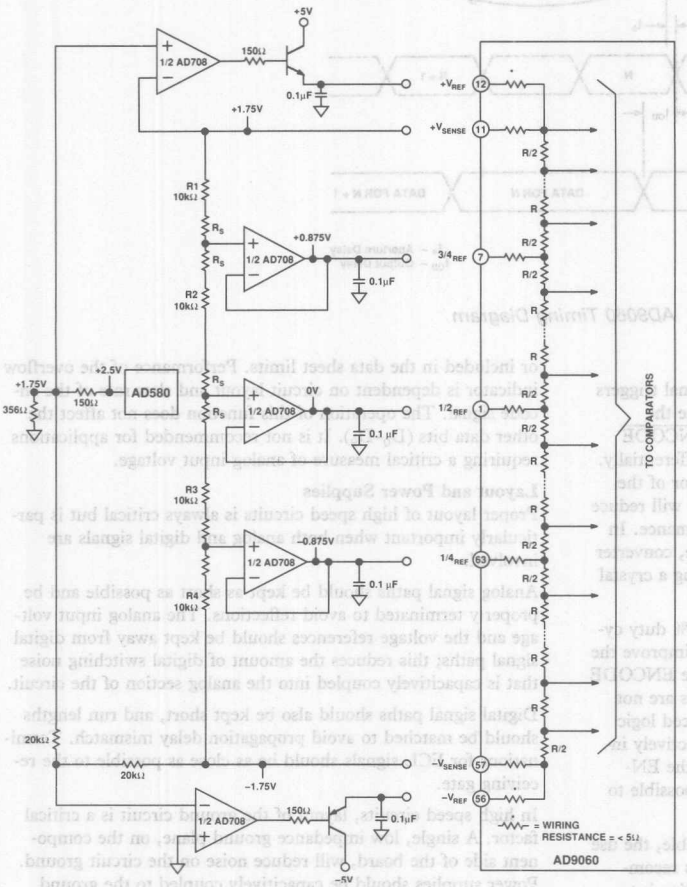
Performance of the AD9060 has been optimized with an analog input voltage of ±1.75 V (as measured at $\pm V_{SENSE}$). If the analog input range is reduced below these values, relatively larger differential nonlinearity errors may result because of comparator mismatches. As shown in the figure below, performance of the converter is a function of $\pm V_{SENSE}$.

Applying a voltage greater than 4 V across the internal resistor ladder will cause current densities to exceed rated values, and may cause permanent damage to the AD9060. The design of the reference circuit should limit the voltage available to the references.

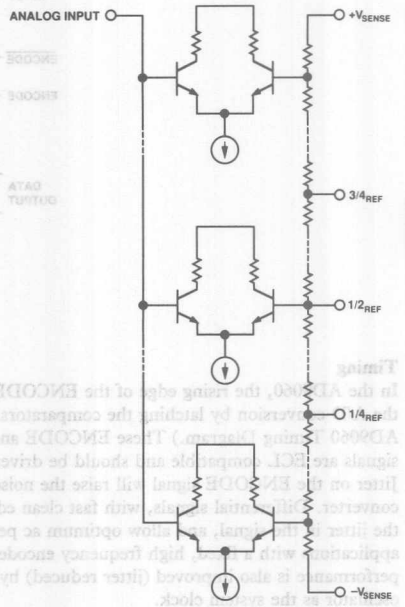
Analog Input Signal

The signal applied to ANALOG IN drives the inputs of 512 parallel comparator cells (see Equivalent Analog Input figure). This connection typically has an input resistance of 7 kΩ, and input capacitance of 45 pF. The input capacitance is nearly constant over the analog input voltage range, as shown in the graph which illustrates that characteristic.

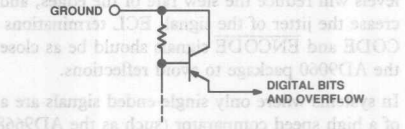
The analog input signal should be driven from a low distortion, low noise amplifier. A good choice is the AD9617, a wide bandwidth, monolithic operational amplifier with excellent ac and dc performance. The input capacitance should be isolated by a small series resistor (24 Ω for the AD9617) to improve the ac performance of the amplifier (see AD9060/PCB Evaluation Board Block Diagram).



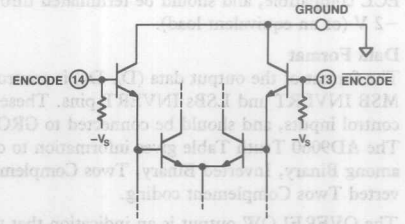
AD9060 Reference Circuit



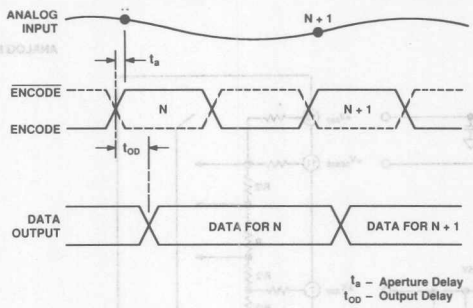
AD9060 Equivalent Analog Input



AD9060 Equivalent Digital Outputs



AD9060 Encode and $\overline{\text{Encode}}$ Equivalent Circuits



AD9060 Timing Diagram

Timing

In the AD9060, the rising edge of the ENCODE signal triggers the A/D conversion by latching the comparators. (See the AD9060 Timing Diagram.) These ENCODE and $\overline{\text{ENCODE}}$ signals are ECL compatible and should be driven differentially. Jitter on the ENCODE signal will raise the noise floor of the converter. Differential signals, with fast clean edges, will reduce the jitter in the signal, and allow optimum ac performance. In applications with a fixed, high frequency encode rate, converter performance is also improved (jitter reduced) by using a crystal oscillator as the system clock.

The AD9060 units are designed to operate with a 50% duty cycle encode signal; adjustment of the duty cycle may improve the dynamic performance of individual devices. Since the ENCODE and $\overline{\text{ENCODE}}$ signals are differential, the logic levels are not critical. Users should remember, however, that reduced logic levels will reduce the slew rate of the edges, and effectively increase the jitter of the signal. ECL terminations for the ENCODE and $\overline{\text{ENCODE}}$ signals should be as close as possible to the AD9060 package to avoid reflections.

In systems where only single-ended signals are available, the use of a high speed comparator (such as the AD96685) is recommended to convert to differential signals. An alternative is to connect +1.3 V (ECL midpoint) to $\overline{\text{ENCODE}}$ and drive the ENCODE connection single ended. In such applications, clean, fast edges are necessary to minimize jitter in the signal.

Output data of the AD9060, D_0–D_9 and OVERFLOW, are also ECL compatible, and should be terminated through 100 Ω to −2 V (or an equivalent load).

Data Format

The format of the output data (D_0–D_9) is controlled by the MSB INVERT and LSBs INVERT pins. These inputs are dc control inputs, and should be connected to GROUND or $+V_S$. The AD9060 Truth Table gives information to choose from among Binary, Inverted Binary, Twos Complement and Inverted Twos Complement coding.

The OVERFLOW output is an indication that the analog input signal has exceeded the voltage at $+V_{SENSE}$. The accuracy of the overflow transition voltage and output delay are not tested or included in the data sheet limits. Performance of the overflow indicator is dependent on circuit layout and slew rate of the encode signal. The operation of this function does not affect the other data bits (D_0–D_9). It is not recommended for applications requiring a critical measure of analog input voltage.

Layout and Power Supplies

Proper layout of high speed circuits is always critical but is particularly important when both analog and digital signals are involved.

Analog signal paths should be kept as short as possible and be properly terminated to avoid reflections. The analog input voltage and the voltage references should be kept away from digital signal paths; this reduces the amount of digital switching noise that is capacitively coupled into the analog section of the circuit.

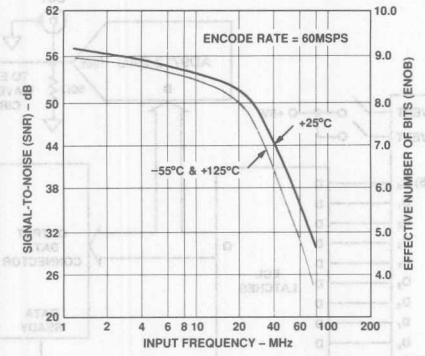
Digital signal paths should also be kept short, and run lengths should be matched to avoid propagation delay mismatch. Terminations for ECL signals should be as close as possible to the receiving gate.

In high speed circuits, layout of the ground circuit is a critical factor. A single, low impedance ground plane, on the component side of the board, will reduce noise on the circuit ground. Power supplies should be capacitively coupled to the ground plane to reduce noise in the circuit. Multilayer boards allow designers to lay out signal traces without interrupting the ground plane and provide low impedance power planes.

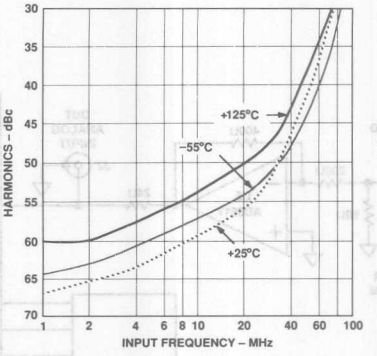
It is especially important to maintain the continuity of the ground plane under and around the AD9060. In systems with dedicated digital and analog grounds, all grounds of the AD9060 should be connected to the analog ground plane.

The power supplies ($+V_S$ and $-V_S$) of the AD9060 should be isolated from the supplies used for external devices; this further reduces the amount of noise coupled into the A/D converter. Sockets limit the dynamic performance and should be used only for prototypes or evaluation—PCK Elastomerics Part No. CCS-68-55 is recommended for the LCC package. (Tel. 215-672-0787)

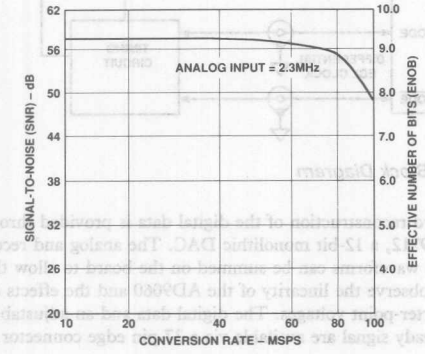
An evaluation board is available to aid designers and provide a suggested layout.



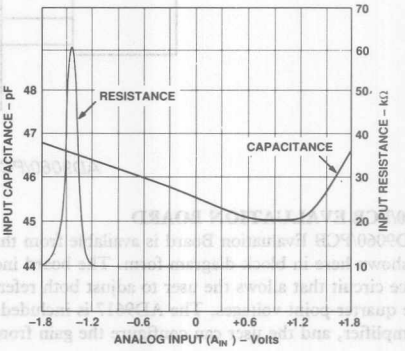
AD9060 SNR and ENOB vs. Input Frequency



AD9060 Harmonics vs. Input Frequency



AD9060 SNR and ENOB vs. Conversion Rate

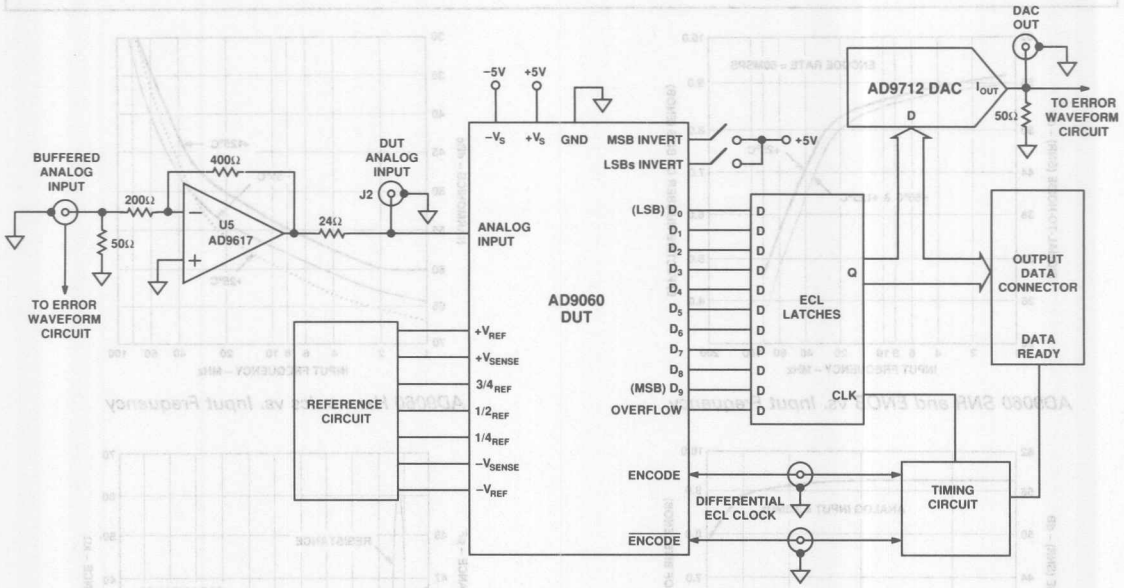


Input Capacitance/Resistance vs. Input Voltage

Step	Range	Offset Binary		Twos Complement	
		True	Inverted	True	Inverted
	0 = −1.75 V FS = +1.75 V	MSB INV = "0" LSBs INV = "0"	MSB INV = "1" LSBs INV = "1"	MSB INV = "1" LSBs INV = "0"	MSB INV = "0" LSBs INV = "1"
1024	>+1.7500	(1)1111111111	(1)0000000000	(1)0111111111	(1)1000000000
1023	+1.7466	1111111111	0000000000	0111111111	1000000000
1022	+1.7432	1111111110	0000000001	0111111110	1000000001
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
512	+0.0034	1000000000	0111111111	0000000000	1111111111
511	0.000	0111111111	1000000000	1111111111	0000000000
510	−0.0034	0111111110	1000000001	1111111110	0000000001
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
02	−1.7432	0000000010	1111111101	1000000010	0111111101
01	−1.7466	0000000001	1111111110	1000000001	0111111110
00	<−1.7466	0000000000	1111111111	1000000000	0111111111

The overflow bit is always 0 except where noted in parentheses ( ). MSB INVERT and LSBs INVERT are considered dc controls.

AD9060 Truth Table



AD9060/PCB Evaluation Board Block Diagram

AD9060/PCB EVALUATION BOARD

The AD9060/PCB Evaluation Board is available from the factory and is shown here in block diagram form. The board includes a reference circuit that allows the user to adjust both references and the quarter-point voltages. The AD9617 is included as the drive amplifier, and the user can configure the gain from −1 to −15.

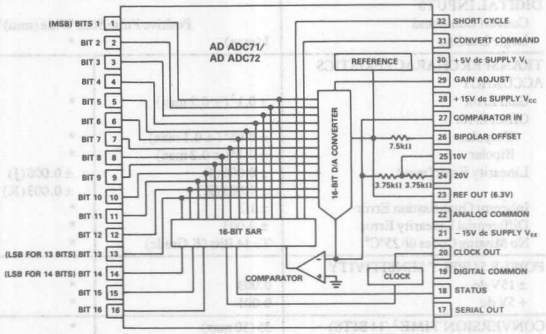
On-board reconstruction of the digital data is provided through the AD9712, a 12-bit monolithic DAC. The analog and reconstructed waveforms can be summed on the board to allow the user to observe the linearity of the AD9060 and the effects of the quarter-point voltages. The digital data and an adjustable Data Ready signal are available via a 37-pin edge connector.

AD ADC71/AD ADC72

FEATURES

Complete 16-Bit Converter With Reference and Clock
±0.003% Maximum Nonlinearity
No Missing Codes to 14 Bits
Fast Conversion – 35μs (14 Bit)
Short Cycle Capability
Parallel and Serial Logic Outputs
Low Power: 645mW Typical
Industry Standard Pin Out

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD ADC71 and AD ADC72 are high resolution 16-bit hybrid IC analog-to-digital converters including reference, clock, and laser-trimmed thin-film components. The package is a compact 32-pin hermetic ceramic DIP. The thin-film scaling resistors allow analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V, and 0 to +20V.

Important performance characteristics of the devices are maximum linearity error of ±0.003% of FSR (AD ADC71K, AD ADC72K and B), and maximum conversion time of 50μs. This performance is due to innovative design and the use of proprietary monolithic D/A converter chips. Laser-trimmed thin-film resistors provide the linearity and wide temperature range for no missing codes.

The AD ADC71 and AD ADC72 provide data in parallel form with corresponding clock and status outputs. The AD ADC71 also provides data in serial form. All digital inputs and outputs are TTL compatible.

APPLICATIONS

The AD ADC71 and AD ADC72 are excellent for use in applications requiring 14-bit accuracy over extended temperature ranges. Typical applications include medical and analytic instrumentation, precision measurement for industrial robots, automatic test equipment (ATE), multichannel data acquisition systems, servo control systems and anywhere that excellent stability and wide dynamic range in the smallest space is required.

PRODUCT HIGHLIGHTS

1. The AD ADC71 and AD ADC72 provide 16-bit resolution with maximum linearity error less than ±0.003% (±0.006% for J and A grades) at 25°C.
2. Conversion time is 35μs typical to 14 bits with short cycle capability.
3. Two binary codes are available on the AD ADC71 and AD ADC72 output. They are complementary straight binary (CSB) for unipolar input voltage ranges and complementary offset binary (COB) for bipolar input ranges. Complementary two's complement (CTC) coding may be obtained by inverting Pin 1 (MSB).
4. The proprietary chips used in this hybrid design provide excellent stability over temperature and lower chip count for improved reliability.

ORDERING GUIDE

Model	Linearity Error (Max)	Specification Temp Range	Package Option*
AD ADC71JD	±0.006% of FSR	0 to +70°C	Ceramic (DH-32E)
AD ADC71KD	±0.003% of FSR	0 to +70°C	Ceramic (DH-32E)
AD ADC72JD	±0.006% of FSR	0 to +70°C	Ceramic (DH-32E)
AD ADC72KD	±0.003% of FSR	0 to +70°C	Ceramic (DH-32E)
AD ADC72AD	±0.006% of FSR	−25°C to +85°C	Ceramic (DH-32E)
AD ADC72BD	±0.003% of FSR	−25°C to +85°C	Ceramic (DH-32E)

*DH-32E = Bottom Brazed Ceramic DIP. See outline information see Package Information section.

This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

ANALOG INPUTS				
Voltage Ranges				
Bipolar	±2.5, ±5, ±10	*	*	Volts
Unipolar	0 to +5, 0 to +10, 0 to +20	*	*	Volts
Impedance (Direct Input)				
0 to +5V, ±2.5V	1.88	*	*	kΩ
0 to +10V, ±5.0V	3.75	*	*	kΩ
0 to +20V, ±10V	7.50	*	*	kΩ
DIGITAL INPUTS[1]				
Convert Command	Positive Pulse 50ns Wide (min) Trailing Edge Initiates Conversion			
Logic Loading	1 (max)	*	*	LSTTL Load
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error	±0.1[2] (±0.2 max)	*	*	%
Offset Error				
Unipolar	±0.05[2] (±0.1 max)	*	*	% of FSR[3]
Bipolar	±0.1[2] (±0.2 max)	*	*	% of FSR
Linearity Error (max)	±0.006 (J)	±0.006 (J)	±0.006 (A)	% of FSR
	±0.003 (K)	±0.003 (K)	±0.003 (B)	% of FSR
Inherent Quantization Error	±1/2	*	*	LSB
Differential Linearity Error	±0.003	*	*	% of FSR
No Missing Codes @ 25°C[4]	To 14 Bits (K Grade)	*	To 14 Bits (B Grade)	Guaranteed
POWER SUPPLY SENSITIVITY				
±15V dc	0.003	*	*	% of FSR/% ΔV_S
+5V dc	0.001	*	*	% of FSR/% ΔV_S
CONVERSION TIME[5] (14 BITS)	35 (50 max)	*	*	µs
WARM-UP TIME	5 (min)	*	*	Minutes
DRIFT				
Gain	±15 (max)	±10 (±20 max)	+7 (±15 max)	ppm/°C
Offset				
Unipolar	±2 (±4 max)	±2 (±4 max)	±2 (±4 max)	ppm of FSR/°C
Bipolar	±10 (max)	±8 (±10 max)	±5 (±10 max)	ppm of FSR/°C
Linearity	±2 (3 max)	±1.5 (2 max)	±1.0 (2 max)	ppm of FSR/°C
Guaranteed No Missing Code Temperature Range[4]				
71JD, 72JD, 72AD (13 Bits)	0 to 70	*	*	°C
71KD, 72KD, 72BD (14 Bits)				
DIGITAL OUTPUT[1]				
(All Codes Complementary)				
Parallel and Serial Output Codes[6]				
Unipolar	CSB	*	*	
Bipolar	COB, CTC[7]	*	*	
Output Drive	5	*	*	LSTTL Loads
Status	Logic "1" During Conversion			
Status Output Drive	5 (max)	*	*	LSTTL Loads
Internal Clock				
Clock Output Drive	5 (max)	*	*	LSTTL Loads
Frequency	400	*	*	kHz
INTERNAL REFERENCE VOLTAGE	6.3	*	*	V dc
Error	±5 max	*	*	%
Max External Current Drain				
With no Degradation of Specs	±200 max	*	*	µA
Temperature Coefficient	±10 max	*	±5 max	ppm/°C
POWER SUPPLY REQUIREMENTS				
Power Consumption	645 (850 max)	*	*	mW
Rated Voltage, Analog	±15 ±0.5 max	*	*	V dc
Rated Voltage, Digital	+5 ±0.25 max	*	*	V dc
Supply Drain +15V dc	+16	*	*	mA
Supply Drain −15V dc	−21	*	*	mA
Supply Drain +5V dc	+18	*	*	mA
TEMPERATURE RANGE				
Specification	0 to +70	*	−25 to +85	°C
Operating (Derated Specs)	−25 to +85	*	−25 to +125	°C
Storage	−55 to +125	*	*	°C

NOTES
[1] Logic "0" = 0.8V, max. Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = +0.4V max. Logic "1" = 2.4V min.
[2] Adjustable to zero.
[3] Full Scale Range.
[4] For definition of "No Missing Codes," refer to Theory of Operation (full data sheet.)
[5] Conversion time may be shortened with "Short Cycle" set for lower resolution.
[6] CSB – Complementary Straight Binary. COB – Complementary Offset Binary. CTC – Complementary Twos Complement.
[7] CTC coding obtained by inverting MSB (Pin 1).
*Specifications same as AD ADC71JD, KD.
Specifications subject to change without notice.

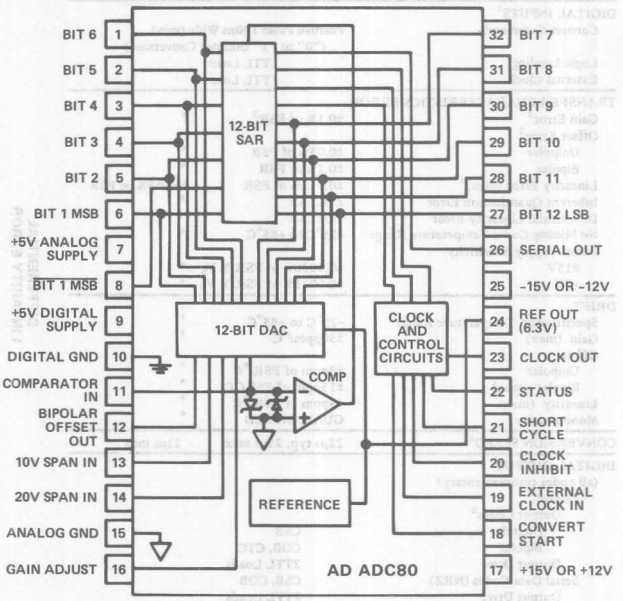
12-Bit Successive Approximation Integrated Circuit A/D Converter

AD ADC80

FEATURES

- True 12-Bit Operation: Max Nonlinearity ±0.012%
- Low Gain T.C.: ±30ppm/°C max
- Low Power: 800mW
- Fast Conversion Time: 25μs
- Precision 6.3V Reference for External Application
- Short-Cycle Capability
- Serial or Parallel Data Outputs
- Monolithic DAC with Scaling Resistors for Stability
- Low Chip Count—High Reliability
- Industry Standard Pinout
- "Z" Models for ±12V Supplies

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD ADC80 is a complete 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide modular performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD ADC80 include a maximum linearity error at +25°C of ±0.012%, max gain T.C. of 30ppm/°C, typical power dissipation of 800mW and max conversion time of 25μs. Monotonic operation of the feedback D/A converter guarantees no missing codes over the temperature range of -25°C to +85°C.

The design of the AD ADC80 includes scaling resistors that provide analog signal ranges of ±2.5, ±5.0, ±10, 0 to +5 or 0 to +10 volts. The 6.3V precision reference may be used for external applications. All digital signals are fully DTL and TTL compatible; output data may be read in both serial and parallel form.

The AD ADC80 is available in two performance grades, the AD ADC80-12 (0.012% of FSR max) and the AD ADC80-10 (0.048% of FSR max). Both grades are specified for use over the -25°C to +85°C temperature range and both are available in a 32-pin ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD ADC80 is a complete 12-bit A/D converter. No external components are required to perform a conversion.
2. A monolithic 12-bit feedback DAC is used for reduced chip count and higher reliability.
3. The internal buried zener reference is laser trimmed to 6.3 volts. The reference voltage is available externally and can supply up to 1.5mA beyond that required for the reference and bipolar offset current.
4. The scaling resistors are included on the monolithic DAC for exceptional thermal tracking.
5. The AD ADC80 directly replaces other devices of this type with significant increases in performance.
6. The fast conversion rate of the AD ADC80 makes it an excellent choice for applications requiring high system throughput rates.
7. The short cycle and external clock options are provided for applications requiring faster conversion speeds or lower resolutions.

AD ADC80—SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise specified)

MODEL	AD ADC80-12	AD ADC80-10
RESOLUTION	12 Bits	10 Bits
ANALOG INPUTS		
Voltage Ranges		
Bipolar	±2.5V, ±5V, ±10V	
Unipolar	0V to +5V, 0V to +10V	
Impedance (Direct Input)		
0V to +5V, ±2.5V	2.5kΩ	*
0V to +10V, ±5V	5kΩ	*
±10V	10kΩ	*
DIGITAL INPUTS[1]		
Convert Command	Positive Pulse 100ns Wide (min) ("0" to "1" Initiates Conversion)	
Logic Loading	1TTL Load	
External Clock	1TTL Load	
TRANSFER CHARACTERISTICS ERROR		
Gain Error[2]	±0.1% of FSR[3]	*
Offset Error[2]		
Unipolar	±0.05% of FSR	*
Bipolar	±0.1% of FSR	*
Linearity Error (max)[4]	±0.012% of FSR	±0.048% of FSR
Inherent Quantization Error	±1/2LSB	*
Differential Linearity Error	±1/2LSB	*
No Missing Codes Temperature Range	-25°C to +85°C	*
Power Supply Sensitivity		
±15V	±0.0030% of FSR/% V_S	*
+5V	±0.0015% of FSR/% V_S	*
DRIFT		
Specification Temperature Range	-25°C to +85°C	*
Gain (max)	±30ppm/°C	*
Offset		
Unipolar	±3ppm of FSR/°C	*
Bipolar (max)	±15ppm of FSR/°C	*
Linearity (max)	±3ppm of FSR/°C	*
Monotonicity	GUARANTEED	*
CONVERSION SPEED[5]	22μs typ, 25μs max	21μs max
DIGITAL OUTPUT		
(all codes complementary)		
Parallel		
Output Codes[6]		
Unipolar	CSB	
Bipolar	COB, CTC	
Output Drive	2TTL Loads	
Serial Data Codes (NRZ)	CSB, COB	
Output Drive	2TTL Loads	
Status	Logic "1" During Conversion	
Status Output Drive	2TTL Loads	
Internal Clock		
Clock Output Drive	2TTL Loads	
Frequency[7]	575kHz	
INTERNAL REFERENCE VOLTAGE	6.3V ±10mV	
Max. External Current (with no degradation of specifications)	1.5mA	
Tempco of Drift	±10ppm/°C typ, ±20ppm/°C max	
POWER REQUIREMENTS		
Rated Voltages	±15V, +5V	
Range for Rated Accuracy	4.75V to 5.25V and ±14.0V to ±16.0V	
Z Models[8]	4.75V to 5.25V and ±11.4V to ±16.0V	
Supply Drain +15V	+10mA	
−15V	−20mA	
+5V	+70mA	
TEMPERATURE RANGE		
Specification	−25°C to +85°C	
Operating (Derated Specs)	−55°C to +100°C	
Storage	−55°C to +125°C	
PACKAGE OPTION[9]		
DH-32D	AD ADC80-12	AD ADC80-10

NOTES
[1] DTL/TTL compatible i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V min for digital inputs, Logic "0" = +0.4V max and "1" = 2.4V min digital outputs.
[2] Adjustable to zero with external trimpots.
[3] FSR means Full Scale Range—for example, unit connected for ±10V range has 20V FSR.
[4] Error shown is the same as ±1/2LSB max for resolution of A/D converter.
[5] Conversion time with internal clock.
[6] See Table 1. CSB – Complementary Straight Binary
COB – Complementary Offset Binary
CTC – Complementary Two's Complement
[7] For conversion speeds specified.
[8] For Z models order AD ADC80Z-12 or AD ADC80Z-10.
[9] For package outline information see Package Information section.

*Specifications same as AD ADC80-12.

Specifications subject to change withoutnoitice.

Specifications subject to change without notice.

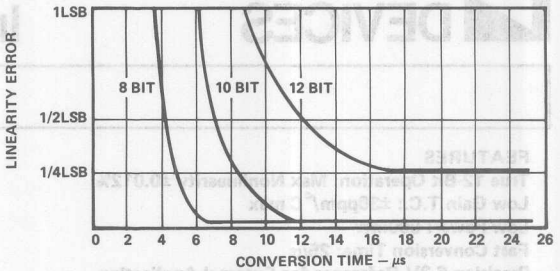


Figure 1. Linearity Error vs. Conversion Time (Normalized)

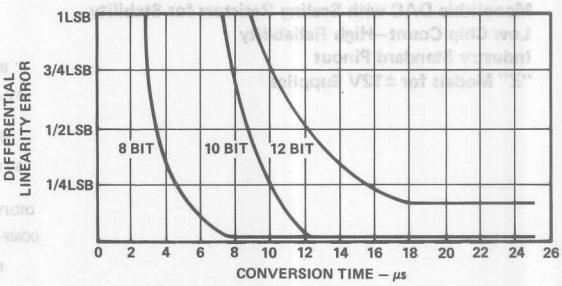


Figure 2. Differential Linearity Error vs. Conversion Time (Normalized)

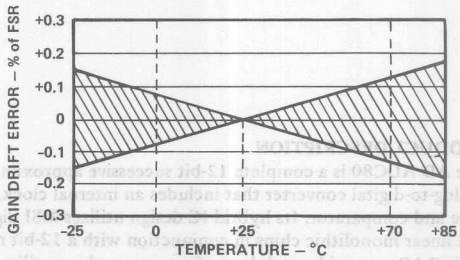


Figure 3. Maximum Gain Drift Error—% of FSR vs. Temperature

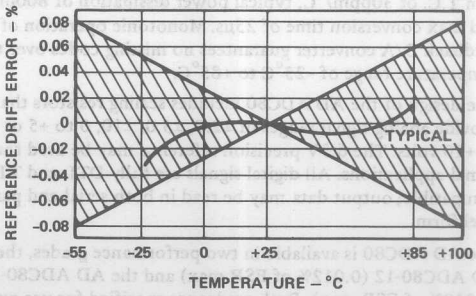


Figure 4. Reference Drift—% Error vs. Temperature

THEORY OF OPERATION

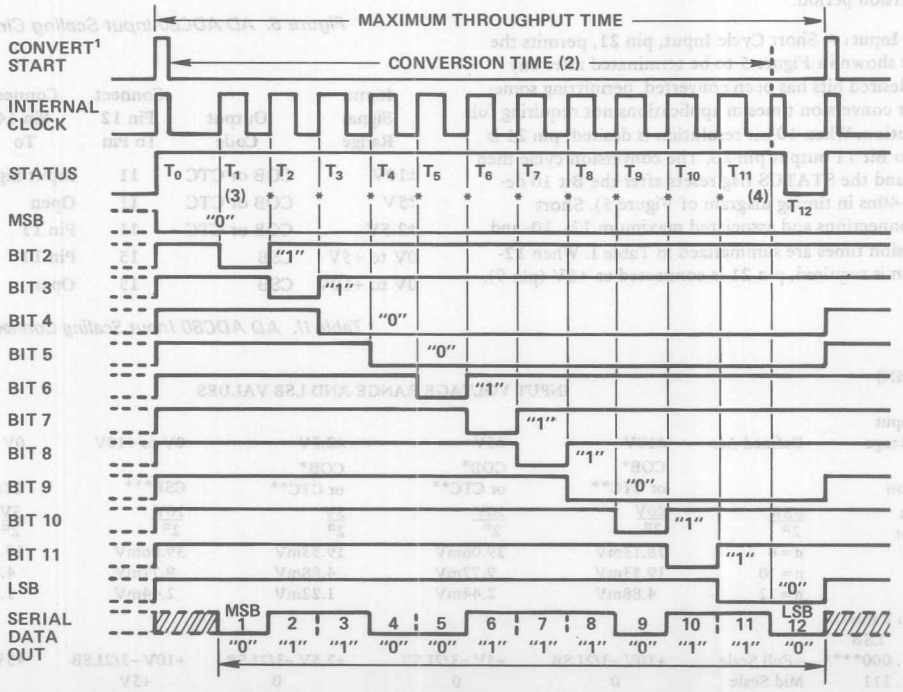
On receipt of a CONVERT START command, the AD ADC80 converts the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 5. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal is removed on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 –B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. After a 40ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the Logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 5).

Incorporation of this 40ns delay guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.



NOTES:
1. THE CONVERT START PULSE WIDTH IS 100ns MIN AND MUST REMAIN LOW DURING A CONVERSION. THE CONVERSION IS INITIATED BY THE "RISING EDGE" OF THE CONVERT COMMAND.
2. 25μs FOR 12 BITS AND 21μs FOR 10 BITS (MAX).
3. MSB DECISION
4. LSB DECISION 40ns PRIOR TO THE STATUS GOING LOW

*BIT DECISIONS

Figure 5. Timing Diagram (Binary Code 011001110110)

Both parallel and serial data from TTL storage registers are in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complementary two's complement binary, depending on whether BIT 1 (pin 6) or its logical inverse BIT 1 (pin 8) is used as the MSB. Parallel data becomes valid approximately 40ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 200ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on these edges as shown in Figure 5. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 5. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

Short Cycle Input: A Short Cycle Input, pin 21, permits the timing cycle shown in Figure 5 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 10-bit resolution is desired, pin 21 is connected to Bit 11 output pin 28. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision (t_{10} +40ns in timing diagram of Figure 5). Short Cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in Table I. When 12-bit resolution is required, pin 21 is connected to +5V (pin 9).

9	12	0.024	25	t_{12} +40ns
28	10	0.100	21	t_{10} +40ns
30	8	0.390	17	t_8 +40ns

Table I. Short Cycle Connections

INPUT SCALING

The AD ADC80 input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 6 for circuit details.

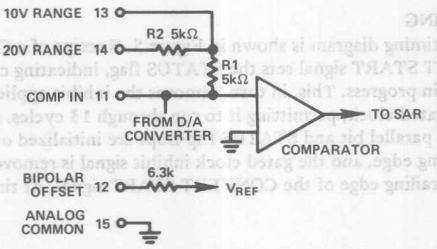


Figure 6. AD ADC80 Input Scaling Circuit

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pin 11	13
0V to +5V	CSB	15	Pin 11	13
0V to +10V	CSB	15	Open	13

Table II. AD ADC80 Input Scaling Connections

Binary (BIN) Output		INPUT VOLTAGE RANGE AND LSB VALUES				
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000 . . . 000****	+Full Scale	+10V −3/2LSB	+5V −3/2LSB	+2.5V −3/2LSB	+10V −3/2LSB	+5V −3/2LSB
011 . . . 111	Mid Scale	0	0	0	+5V	+2.5V
111 . . . 110	−Full Scale	−10V +1/2LSB	−5V +1/2LSB	−2.5V +1/2LSB	0 + 1/2LSB	0 +1/2LSB

NOTES:
*COB = Complementary Offset Binary
**CTC = Complementary Two's complement—obtained by using the complement of the most significant bit ($\overline{MSB}$). $\overline{MSB}$ is available on pin 8.
***CSB = Complementary Straight Binary.
****Voltages given are the nominal value for transition to the code specified.

Table III. Input Voltages and Code Definitions

OFFSET ADJUSTMENT

The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input pin 11 for all ranges. As shown in Figure 7 the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a −1200ppm/°C tempco contributes a worst-case offset tempco of $8 \times 244 \times 10^{-6} \times 1200$ppm/°C = 2.3ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4LSB, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

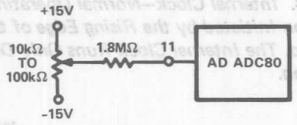


Figure 7. Offset Adjustment Circuit

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 8.

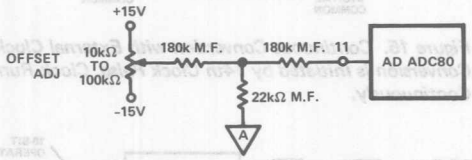


Figure 8. Low Tempco Zero Adjustment Circuit

In either zero adjust circuit, the fixed resistor connected to pin 11 should be located close to this pin to keep the pin 11 connection runs short (Comparator Input pin 11 is quite sensitive to external noise pick-up).

GAIN ADJUSTMENT

The gain adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 10MΩ resistor to the gain adjust pin 16 as shown in Figure 9.

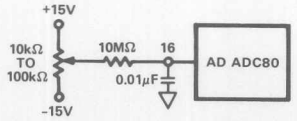


Figure 9. Gain Adjustment Circuit

An alternate gain adjust circuit which contributes negligible gain tempco if metal film resistors (Tempco <100ppm/°C) are used is shown in Figure 10.

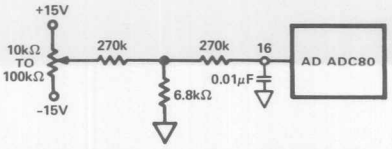


Figure 10. Low Tempco Gain Adjustment Circuit

CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 11 and 12, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and −FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 111111111110. Zero is now calibrated. Set analog input to +FSR −2LSB = +9.9952V. Adjust Gain for 000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 011111111111.

−10V to +10V Range: Set analog input to −9.9951V; adjust Zero for 111111111110 digital output (complementary offset binary) code. Set analog input to +9.9902V; adjust Gain for 000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (complementary offset binary) code should be 0111111111111.

Other Ranges: Representative digital coding for 0 to +10V and −10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, −2.5V to +2.5V and −5V to +5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and −10V to +10V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/4LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes," D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter 3.

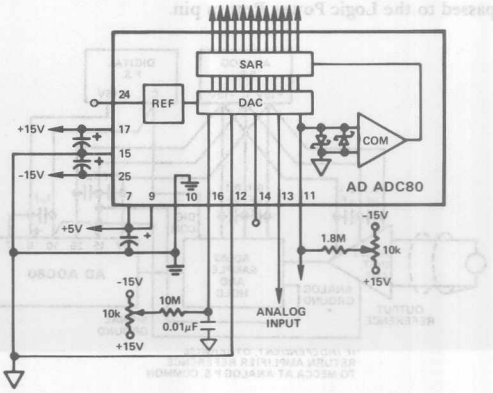


Figure 11. Analog and Power Connections for Unipolar 0–10V Input Range

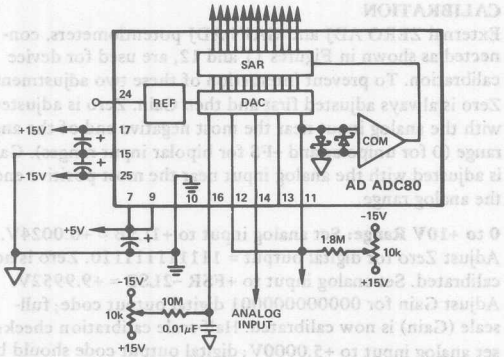


Figure 12. Analog and Power Connections for Bipolar ±10V Input Range

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD ADC80. Therefore, separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point and the two device grounds should be tied together. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD ADC80's supply terminals should be capacitively decoupled as close to the AD ADC80 as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

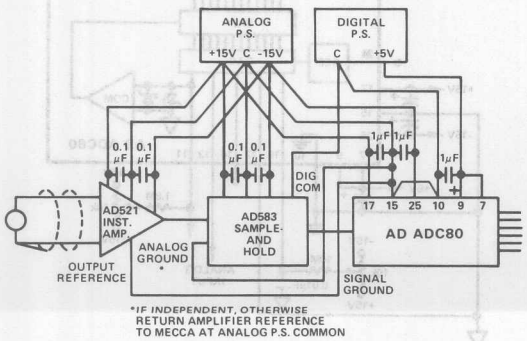


Figure 13. Basic Grounding Practice

CONTROL MODES

The timing sequence of the AD ADC80 allows the device to be easily operated in a variety of systems with different control modes. The most common control modes are illustrated in Figures 14–16.

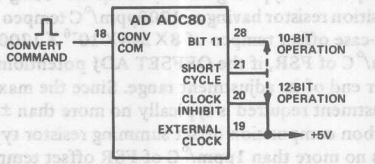


Figure 14. Internal Clock—Normal Operating Mode. Conversion Initiated by the Rising Edge of the Convert Command. The Internal Clock Runs Only During Conversion.

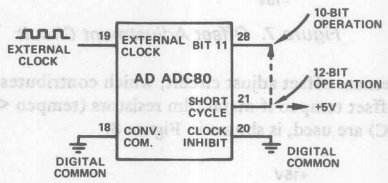


Figure 15. Continuous Conversion with External Clock. Conversion is Initiated by 14th Clock Pulse. Clock Runs Continuously.

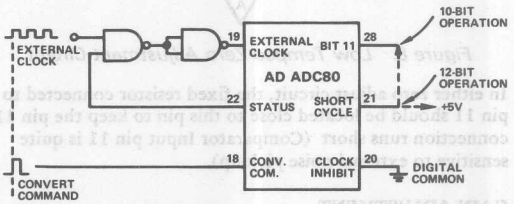


Figure 16. Continuous External Clock. Conversion Initiated by Rising Edge of Convert Command. The Convert Command must be Synchronized with Clock.

Fast, Complete 12-Bit A/D Converters

AD ADC84/AD ADC85/AD5240

FEATURES

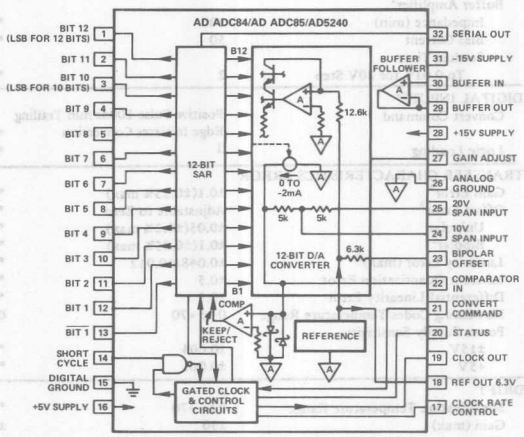
Performance

- Complete 12-Bit A/D Converter with Reference and Clock
- Fast Successive Approximation Conversion: 10μs or 5μs
- Buried Zener Reference for Long Term Stability and Low Gain T.C.: 10ppm/°C
- Max Nonlinearity: <±0.012%
- Low Power: 880mW Typical
- Low Chip Count – High Reliability
- Industry Standard Pin Out
- "Z" Models for ±12V Operation Available
- MIL-STD-883B Processing Available

Versatility

- Negative-True Parallel or Serial Logic Outputs
- Short Cycle Capability
- Precision +6.3V Reference for External Applications

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD ADC84/AD ADC85/AD5240 series devices are high-speed, low-cost 10- and 12-bit successive approximation analog-to-digital converters that include internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide modular performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD ADC84/AD ADC85/AD5240 series include a maximum linearity error at +25°C of ±0.012%, gain T.C. below 15ppm/°C, typical power dissipation of 880mW, and conversion time of less than 10μs for the 12-bit versions. Of considerable significance in severe and aerospace applications is the guaranteed performance from −55°C to +125°C of the AD ADC85S which is also available with environmental screening. Monotonic operation of the feedback D/A converter guarantees no missing codes over temperature ranges of 0 to +70°C, −25°C to +85°C, and −55°C to +125°C.

The design of the AD ADC84/AD ADC85/AD5240 includes scaling resistors that provide analog input signal ranges of ±2.5, ±5, ±10, 0 to +5, or 0 to +10 volts. Adding flexibility and value are the +6.3V precision reference, which also can be used for external applications, and the input buffer amplifier. All digital signals are fully DTL and TTL compatible, and the data output is negative-true and available in either serial or parallel form.

The AD ADC84/AD ADC85/AD5240 series devices are available in two different performance grades. The devices are specified for either 10-bit accuracy (±0.048% FSR max) or 12-bit accuracy (±0.012% FSR max) with 8.4μs, 10μs (AD ADC84/AD ADC85) and 4.1μs, 5μs (AD5240) max conversion times respectively.

The AD ADC84 and AD ADC85C specified for operation over the 0 to +70°C temperature range. The AD ADC85 and AD ADC85S are specified for the −25°C to +85°C, −55°C to +125°C ranges respectively.

PRODUCT HIGHLIGHTS

1. The AD ADC84/AD ADC85/AD5240 series devices are complete 12-bit A/D converters. No external components are required to perform a conversion.
2. The AD ADC84/AD ADC85/AD5240 directly replaces other devices of this type with significant increases in performance.
3. The fast conversion rates of the AD ADC84/AD ADC85 (10μs) and AD5240 (5μs) make them an excellent choice for applications requiring high system throughput rates.
4. The internal buried zener reference is laser trimmed to 6.3V ±0.1% and ±10ppm/°C typical T.C. The reference is available externally and can provide up to 1mA.
5. The integrated package construction provides high quality and reliability with small size and weight.
6. The monolithic 12-bit feedback DAC is used for reduced chip count and higher reliability.
7. The AD ADC85S/883B and AD5240SD/883B come processed to MIL-STD-883, Class B requirements (see ADI Military Products Databook).

MODEL	AD ADC84	AD ADC85C	AD ADC85	AD ADC85S	AD5240SD	UNITS
RESOLUTION	10/12	10/12	10/12	10/12	12	Bits
ANALOG INPUTS						
Voltage Ranges						
Bipolar	±2.5, ±5, ±10	•	•	•	•	Volts
Unipolar	0 to +5, 0 to +10	•	•	•	•	Volts
Impedance (Direct Input)						
0V to +5V, ±2.5V	2.5(±20%)	•	•	•	•	kΩ
0V to +10V, ±5V	5(±20%)	•	•	•	•	kΩ
±10V	10(±20%)	•	•	•	•	kΩ
Buffer Amplifier[1]						
Impedance (min)	100	•	•	•	•	MΩ
Bias Current	50	•	•	•	•	nA
Settling Time						
To 0.01% for 20V Step	2	•	•	•	•	μs
DIGITAL INPUTS[2]						
Convert Command	Positive Pulse 100ns min Trailing Edge Initiates Conversion	•	•	•	•	
Logic Loading	1	•	•	•	•	TTL Load
TRANSFER CHARACTERISTICS ERROR						
Gain Error[3]	±0.1(±0.25% max)	•	•	•	±0.2	%
Offset Error[3]	Adjustable to Zero	•	•	•	•	
Unipolar	±0.05(±0.2% max)	•	•	•	±0.1	% of FSR[4]
Bipolar[5]	±0.1(±0.25% max)	•	•	•	±0.2	% of FSR
Linearity Error (max)[6]	±0.048/±0.012	•	•	•	±0.012	% of FSR
Inherent Quantization Error	±0.5	•	•	•	•	LSB
Differential Linearity Error	±0.5	•	•	•	•	LSB
No Missing Codes Temperature Range	0 to +70	0 to +70	−25 to +85	−55 to +125	0 to +70/−55 to +125	°C
Power Supply Sensitivity						
±15V	±0.004	•	•	•	•	% of FSR/%V
+5V	±0.001	•	•	•	•	% of FSR/%V
DRIFT						
Specification Temperature Range	0 to +70	•	−25 to +85	−55 to +125	0 to +70/−55 to +125	°C
Gain (max)	±30	±40/±25	±20/±15	±25	±30/±25	ppm/°C
Offset						
Unipolar	±3	•	•	±5 max	•	ppm/°C
Bipolar (max)[5]	±15	±20/±12	±10/±7	±10	±15/±7	ppm/°C
Linearity (max)	±3	•	±3/±2	•	±2	ppm/°C
Monotonicity	GUARANTEED	•	•	•	GUARANTEED	
CONVERSION SPEED (MAX)	8.4/10	•	•	•	5	μs
DIGITAL OUTPUT						
(all codes complementary)						
Parallel						
Output Codes[7]						
Unipolar	CSB	•	•	•	•	
Bipolar	COB, CTC	•	•	•	•	
Output Drive	2	•	•	•	•	TTL Loads
Serial Data Codes (NRZ)	CSB, COB	•	•	•	•	
Output Drive	2	•	•	•	•	TTL Loads
Status	Logic "1" during Conversion	•	•	•	•	
Status Output Drive	2	•	•	•	•	TTL Loads
Internal Clock						
Clock Output Drive	2	•	•	•	•	TTL Loads
Frequency	1.9/1.22	•	•	•	2.6	MHz
INTERNAL REFERENCE VOLTAGE	6.3/±15mV max	•	•	•	•	Volts
Max. External Current (with no degradation of specifications)	1.0	•	•	•	•	mA
Tempco of Drift, (max)	±20/max	±10 typ	±5 typ	±5 typ	±10	ppm/°C
POWER REQUIREMENTS						
Rated Voltages	+5, ±15	•	•	•	•	Volts
Range for Rated Accuracy	4.75 to 5.25 and ±13.5 to ±16.5	•	•	•	•	Volts
Z Models[8]	4.75 to 5.25 and ±11.4 to ±16.5	•	•	•	•	Volts
Supply Drain +15V	25 max	•	•	•	15 max	mA
−15V	35 max	•	•	•	35 max	mA
+5V	140 max	•	•	•	100 max	mA
Total Power Dissipation	1500 max	•	•	•	1100 max	mW
TEMPERATURE RANGE						
Specification	0 to +70	•	−25 to +85	−55 to +125	0 to +70/−55 to +125	°C
Operating (Derated Specs)	−25 to +85	•	−55 to +125	−55 to +125	−55 to +125	°C
Storage	−55 to +125	•	•	•	−65 to +150	°C
PACKAGE OPTION[9]						
D11-32F	Ceramic	Ceramic	Ceramic	Ceramic	Ceramic	

NOTES

[1] Buffer Settling time adds to conversion speed when buffer is connected to input.

[2] DTL/TTL compatible Logic "0" = 0.8V max, Logic "1" = 2.0V min for digital output, Logic "0" = 0.4V max, Logic "1" = 2.4V min.

[3] Adjustable to zero.

[4] FSR means Full Scale Range.

[5] Guaranteed at V_{IN} = 0 volts.

[6] Error shown is the same as ±1/2LSB max error in % of FSR.

[7] See Table I.

[8] For ±12V operation add "Z" to model number. Input range limited to a maximum of ±5V.

[9] For package outline information see Package Information section.

*Specifications same as AD ADC84.

Specifications subject to change without notice.

Typical Performance Curves – AD ADC84/AD ADC85/AD5240

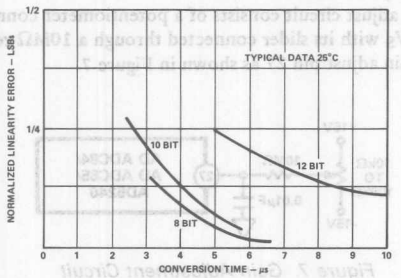


Figure 1a. Linearity Error vs. Conversion Speed (AD ADC84/AD ADC85)

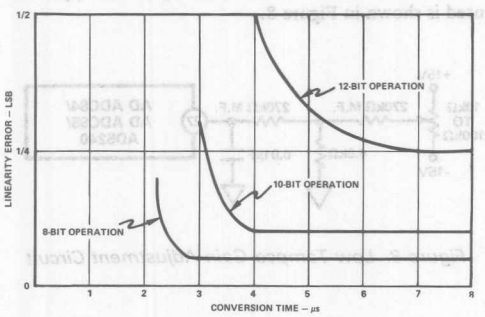


Figure 1b. Linearity Error vs. Conversion Speed (AD5240)

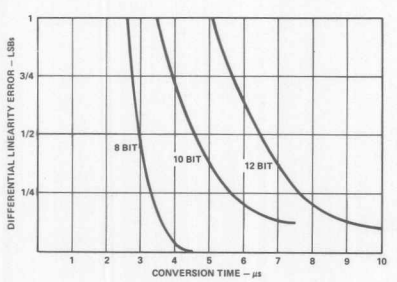


Figure 2a. Change in Differential Linearity vs. Conversion Speed (AD ADC84/AD ADC85)

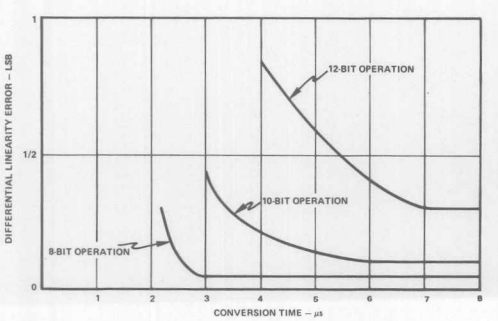


Figure 2b. Change in Differential Linearity vs. Conversion Speed (AD5240)

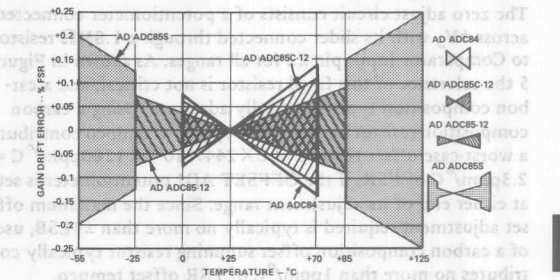


Figure 3a. Gain Drift Error (% FSR) vs. Temperature (AD ADC84/AD ADC85)

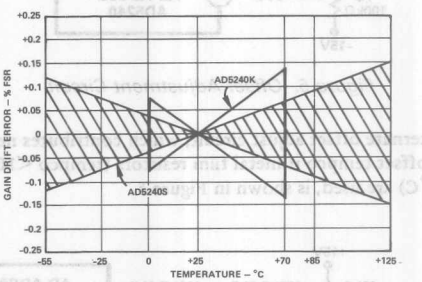


Figure 3b. Gain Drift Error (% FSR) vs. Temperature (AD5240)

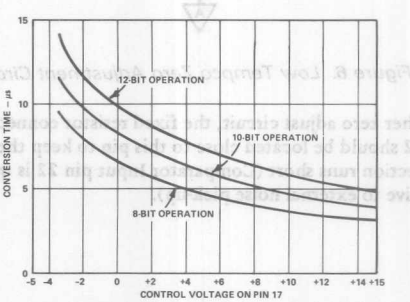


Figure 4a. Conversion Speed vs. Control Voltage (AD ADC84/AD ADC85)

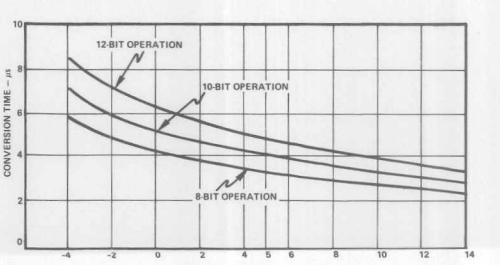


Figure 4b. Conversion Speed vs. Control Voltage (AD5240)

OFFSET ADJUSTMENT

The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input pin 22 for all ranges. As shown in Figure 5 the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a −1200ppm/°C tempco contributes a worst-case offset tempco of $8 \times 244 \times 10^{-6} \times 1200$ppm/°C = 2.3ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4LSB, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

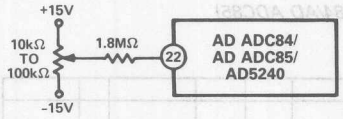


Figure 5. Offset Adjustment Circuit

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 5.

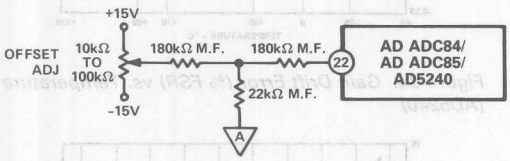


Figure 6. Low Tempco Zero Adjustment Circuit

In either zero adjust circuit, the fixed resistor connected to pin 22 should be located close to this pin to keep the pin connection runs short (Comparator Input pin 22 is quite sensitive to external noise pick-up).

GAIN ADJUSTMENT

The gain adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 10MΩ resistor to the gain adjust pin 27 as shown in Figure 7.

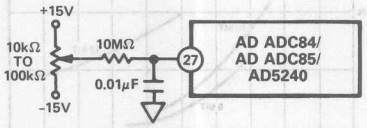


Figure 7. Gain Adjustment Circuit

An alternate gain adjust circuit which contributes negligible gain tempco if metal film resistors (Tempco <100ppm/°C) are used is shown in Figure 8.

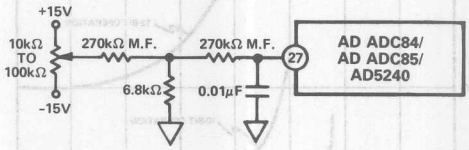


Figure 8. Low Tempco Gain Adjustment Circuit

THEORY OF OPERATION

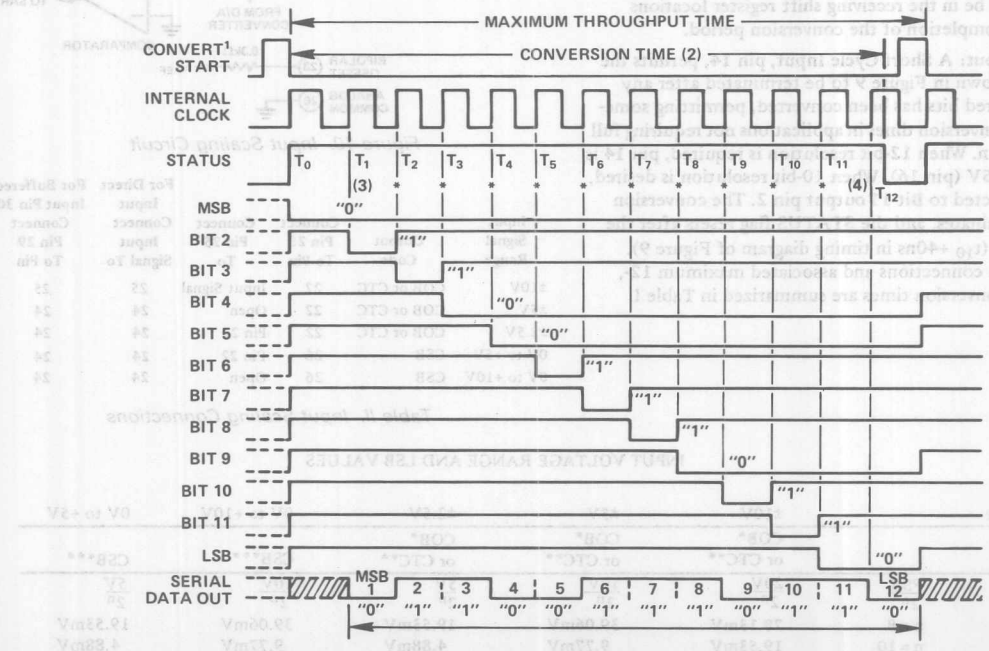
On receipt of a CONVERT START command, the AD ADC84/AD ADC85/AD5240 converts the voltage as its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 9. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All the SAR parallel bits, STATUS flip-flops, and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 – B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. After a 40ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the Logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking into a receiving shift register on these edges (see Figure 9).

Incorporation of this 40ns delay guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.



NOTES
1. THE CONVERT START PULSE WIDTH IS 100ns MIN AND MUST REMAIN LOW DURING A CONVERSION. THE CONVERSION IS INITIATED BY THE "TRAILING EDGE" OF THE CONVERT COMMAND.
2. 10µs FOR 12 BITS AND 8.4µs FOR 10 BITS (AD ADC84/AD ADC85) OR 5µs FOR 12 BITS AND 4.1µs FOR 10 BITS (AD5240).
3. MSB DECISION.
4. LSB DECISION 20ns PRIOR TO THE STATUS GOING LOW.
*BIT DECISIONS.

Figure 9. Timing Diagram (Binary Code 0 1 1 0 0 1 1 1 0 1 1 0)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers are in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complementary two's complement binary, depending on whether BIT 1 (pin 12) or its logical inverse $\overline{\text{BIT 1}}$ (pin 13) is used as the MSB. Parallel data becomes valid approximately 40ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 200ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on the negative-going clock edges as shown in Figure 9. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 9. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

Short Cycle Input: A Short Cycle Input, pin 14, permits the timing cycle shown in Figure 9 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 14 is connected to +5V (pin 16). When 10-bit resolution is desired, pin 14 is connected to Bit 11 output pin 2. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision (t_{10} +40ns in timing diagram of Figure 9). Short Cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in Table I.

Connect Short Cycle Pin 14 To Pin:	Connect Clock Rate Control Pin 17 To	Bits	Resolution (% FSR)	AD ADC84/ AD ADC85 (AD5240) Conversion Time (μs)	Status Flag Reset
16	15	12	0.024	10 (5)	t_{12} +40ns
2	16	10	0.100	8.5 (4.1)	t_{10} +40ns
4	28	8	0.390	6.8 (3.3)	t_8 +40ns

Table I. Short Cycle Connections

INPUT SCALING

The AD ADC84/AD ADC85/AD5240 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 10 for circuit detail.

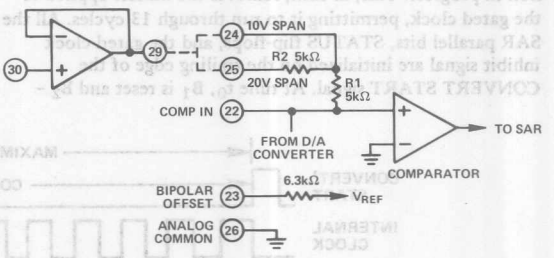


Figure 10. Input Scaling Circuit

Input Signal Range	Output Code	Connect Pin 23 To Pin	Connect Pin 25 To	For Direct Input Connect Input Signal To	For Buffered Input Pin 30 Connect Pin 29 To Pin
±10V	COB or CTC	22	Input Signal	25	25
±5V	COB or CTC	22	Open	24	24
±2.5V	COB or CTC	22	Pin 22	24	24
0V to +5V	CSB	26	Pin 22	24	24
0V to +10V	CSB	26	Open	24	24

Table II. Input Scaling Connections

INPUT VOLTAGE RANGE AND LSB VALUES

Analog Input Voltage Range		±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000 . . . 000****	+Full Scale	+10V –3/2LSB	+5V –3/2LSB	+2.5V –3/2LSB	+10V –3/2LSB	+5V –3/2LSB
011 . . . 111	Mid Scale	0	0	0	+5V	+2.5V
111 . . . 110	–Full Scale	–10V +1/2LSB	–5V +1/2LSB	–2.5V +1/2LSB	0 + 1/2LSB	0 +1/2LSB

NOTES:
*COB = Complementary Offset Binary
**CTC = Complementary Two's complement—obtained by using the complement of the most significant bit ($\overline{\text{MSB}}$). $\overline{\text{MSB}}$ is available to pin 13.
***CSB = Complementary Straight Binary.
****Voltages given are the nominal value for transition to the code specified.

Table III. Input Voltages and Code Definition

CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 11 and 12, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and -FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

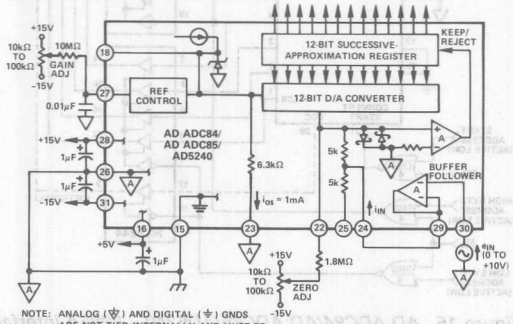


Figure 11. Analog and Power Connections for Unipolar 0 to +10V Input Range with Buffer Follower

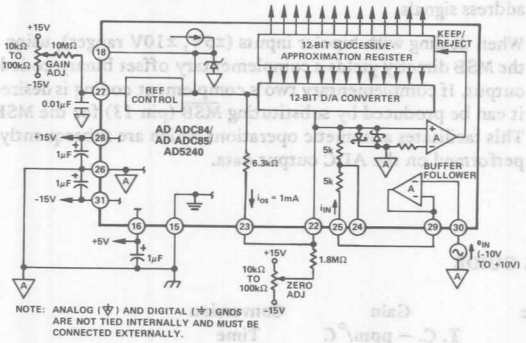


Figure 12. Analog and Power Connections for Bipolar −10V to +10V Input Range with Buffer Follower

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 111111111110. Zero is now calibrated. Set analog input to +FSR -2LSB = +9.9952V. Adjust Gain for 000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 011111111111.

-10V to +10V Range: Set analog input to -9.9951V; adjust Zero for 111111111110 digital output (complementary offset binary) code. Set analog input to +9.9902V; adjust Gain for 000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (complementary offset binary) code should be 0111111111111.

Other Ranges: Representative digital coding for 0 to +10V and -10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, -2.5V to +2.5V and -5V to +5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and -10V to +10V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/4LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level.

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD ADC84/AD ADC85/AD5240. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD ADC84/AD ADC85/AD5240's supply terminals should be capacitively decoupled as close to the device as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

CLOCK RATE CONTROL ALTERNATE CONNECTIONS

If adjustment of the CLOCK RATE is desired for faster conversion speeds, the CLOCK RATE CONTROL may be connected to an external multi-turn trim potentiometer with a TCR of ±100ppm/°C or less as shown in Figures 13 and 14. If the potentiometer is connected to -15V, conversion time can be increased as shown in Figures 4a and 4b. If these adjustments are used, delete the connections shown in Table I for pin 17. See Figures 1a and 1b for nonlinearity error vs. conversion speed and Figures 4a and 4b for the effect of the control voltage on clock speed.

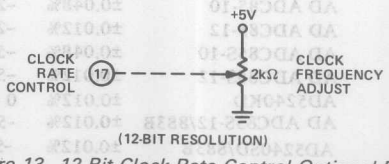


Figure 13. 12-Bit Clock Rate Control Optional Fine Adjust

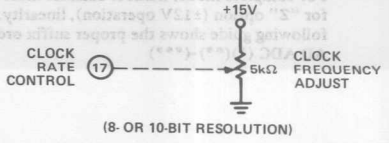


Figure 14. 8-Bit Clock Rate Control Optional Fine Adjust

MICROPROCESSOR INTERFACING

The fast conversion times of the AD ADC84/AD ADC85 and AD5240 suggest several different methods of interface to microprocessors. In systems where the ADC is used for high sampling rates on a single signal which is to be digitally processed, CPU-controlled conversion may be inefficient due to the slow cycle times of most microprocessors. It is generally preferable to perform conversions independently, inserting the resultant digital data directly into memory. This can be done using direct memory access (DMA) which is totally transparent to the CPU. Interface to user-designed DMA hardware is facilitated by the guaranteed data validity on the falling edge of the EOC signal.

Clearly, 12 bits of data must be broken up for interface to an 8-bit wide data bus. There are two possible formats: right-justified and left-justified. In a right-justified system, the least-significant 8 bits occupy one byte and the four MSB's reside in the low nybble of another byte. This format is useful when the data from the ADC is being treated as a binary number between 0 and 4095. The left-justified format supplies the eight most-significant bits in one byte and the 4LSB's in the high nybble of another byte. The data now represents the fractional binary number relating the analog signal to the full-scale voltage. An advantage to this organization is that the most-significant eight bits can be read by the processor as a coarse indication of the true signal value. The full 12-bit word can then be read only when all 12 bits are needed. This allows faster and more efficient control of a process.

Figure 15 shows a typical connection of an 8085-type bus, using a left-justified data format for unipolar inputs. Status polling is optional, and can be read simultaneously with the 4LSBs. If it is desired to right-justify the data, pins 1 through 12 of the AD ADC84/AD ADC85/AD5240 should be reversed,

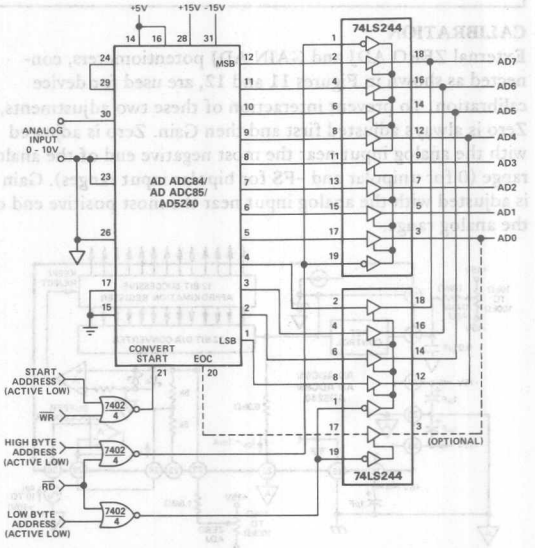


Figure 15. AD ADC84/AD ADC85/AD5240 – 8085A Interface Connections

as well as the connections to the data bus high and low byte address signals.

When dealing with bipolar inputs (±5V, ±10V ranges), using the MSB directly yields a complementary offset binary-coded output. If complementary two's complement coding is desired, it can be produced by substituting $\overline{\text{MSB}}$ (pin 13) for the MSB. This facilitates arithmetic operations which are subsequently performed on the ADC output data.

ORDERING GUIDE

Model[1]	Linearity	Temperature Range	Gain T. C. – ppm/°C	Conversion Time
AD ADC84-10	±0.048%	0 to +70°C	±30	10μs
AD ADC84-12	±0.012%	0 to +70°C	±30	10μs
AD ADC85C-10	±0.048%	0 to +70°C	±40	10μs
AD ADC85C-12	±0.012%	0 to +70°C	±25	10μs
AD ADC85-10	±0.048%	-25°C to +85°C	±20	10μs
AD ADC85-12	±0.012%	-25°C to +85°C	±15	10μs
AD ADC85S-10	±0.048%	-55°C to +125°C	±25	10μs
AD ADC85S-12	±0.012%	-55°C to +125°C	±25	10μs
AD5240KD	±0.012%	0 to +70°C	±30	5μs
AD ADC85S-12/883B	±0.012%	-55°C to +125°C	±25	10μs
AD5240SD/883B	±0.012%	-55°C to +125°C	±25	5μs

[1] For complete model number suffixes must be added for "Z" option (±12V operation), linearity. The following guide shows the proper suffix order.
AD ADC (*)(**)-(***)

*Model Number	Typical Part Numbers
**"Z" Version Designator	AD ADC84-12
***Linearity	AD ADC85SZ-12
	AD5240ZKD

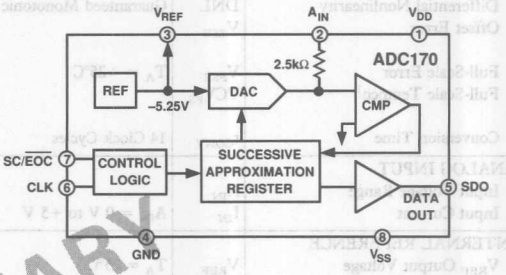
Complete, Serial-Out 5.6 µs, 12-Bit A/D Converter

ADC-170

FEATURES
8-Pin Mini-DIP Package
Fast Conversion Time—5.6 µs
Low Power—135 mW typical
Internal Low Drift Bandgap Reference
0 to +5 V Analog Input Range
3-Wire Signal Interface

APPLICATIONS
Data Acquisition Systems
Medical Diagnostics
Avionic and Navigation Systems
Process Control Equipment
Multichannel Analog I/O
Isolated Industrial Data Acquisition

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The ADC-170 is a complete, serial-output, 12-bit analog-to-digital converter with voltage reference, all in a space-saving 8-pin mini-DIP or 16-pin surface mount SOIC package. Operating from an external 2.5 MHz (max) clock, input signals of up to 5 V are digitized at a 5.6 µs rate. A TTL-compatible three-wire serial interface transfers the digital output data directly to the serial port of the host processor, or easily interfaces with opto isolators or transformers for high voltage isolation.

Fabricated in a complementary bipolar CMOS (CBCMOS) process, the ADC-170 utilizes a successive approximation architecture with a high speed DAC and low noise PNP-input comparator to achieve both high speed and low power operation. Operating from +5 V and −12 V to −15 V supplies, power consumption is only 135 mW. The internal voltage reference is a low drift bandgap which maintains guaranteed accuracy over the full operating temperature range of the device.

Following a start of conversion pulse, the MSB of the new digital word is available at the serial data output after 2 clock cycles, during which the new conversion results are read with the remaining 12 clock cycles. The ADC-170 can be configured for single conversion or continuous operation.

The ADC-170 provides the most complete 12-bit ADC solution available in a compact package. When combined with the serial-input DAC-8043 in the 8-pin mini-DIP package, the result is an unusually dense, high performance analog input/output port.

The ADC-170 is available in 8-pin plastic and Cerdip packages, while the SOIC-16 addresses surface mount applications. All parts are offered in the extended industrial temperature range (−40°C to +85°C). For −55°C to +125°C applications, contact your local Analog Devices sales office to obtain the ADC-170/883 data sheet.

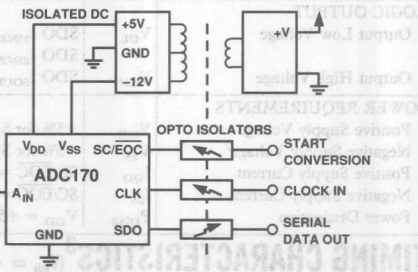


Figure 1. ADC-170 High Voltage Isolation Application

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ADC-170—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_{DD} = +5 V ± 5%, V_{SS} = −11.4 V to −15.75 V; f_{CLK} = 2.5 MHz; −40°C ≤ T_A ≤ +85°C unless otherwise noted.)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
ACCURACY							
Resolution	N			12			Bits
Integral Nonlinearity	INL	T_A = +25°C	ADC170E			±1/2	LSB
			ADC170F			±1	LSB
Differential Nonlinearity	DNL	Guaranteed Monotonic over Temp				±1	LSB
Offset Error	V_{ZSE}		ADC170E			±3	LSB
			ADC170F			±5	LSB
Full-Scale Error	V_{FSE}	T_A = +25°C				±10	LSB
Full-Scale Tempco[1]	TCV_{FS}		ADC170E			±25	ppm/°C
			ADC170F			±45	ppm/°C
Conversion Time	t_{CONV}	14 Clock Cycles			5.6		µs
ANALOG INPUT							
Input Voltage Range	A_{IN}			0		+5	V
Input Current	I_{IN}	A_{IN} = 0 V to +5 V				3.5	mA
INTERNAL REFERENCE							
V_{REF} Output Voltage	V_{REF}	T_A = 25°C		−5.2	−5.25	−5.3	V
V_{REF} Output Tempco[1]	TCV_{REF}		ADC170E		±20		ppm/°C
			ADC170F		±40		ppm/°C
Output Current Sink Capability	I_{REF}					5	mA
POWER SUPPLY REJECTION							
Positive Supply Rejection	V_{DD}	FS Change, V_{SS} = −15 V or −12 V, V_{DD} = 4.75 V to 5.25 V			±1/2		LSB
Negative Supply Rejection	V_{SS}	FS Change, V_{DD} = +5 V	V_{SS} = −14.25 V to −15.75 V		±1/8		LSB
			V_{SS} = −11.4 V to −12.6 V		±1/8		LSB
LOGIC INPUTS							
Input Low Voltage	V_{IL}					0.8	V
Input High Voltage	V_{IH}			2.4			V
Input Capacitance[1]	C_{IN}					10	pF
Input Current	I_{INL}	A_{IN} = 0 to V_{DD}	CLOCK			±10	µA
			SC/$\overline{EOC}$	±200		±500	µA
LOGIC OUTPUT							
Output Low Voltage	V_{OL}	SDO I_{SINK} = 1.6 mA				0.4	V
		SDO I_{SINK} = 6.0 mA			0.3	1.5	V
Output High Voltage	V_{OH}	SDO I_{SOURCE} = 200µA		4			V
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}	±5% for Specified Performance			5		V
Negative Supply Voltage[2]	V_{SS}	±5% for Specified Performance			−15 to −12		V
Positive Supply Current	I_{DD}	SC/$\overline{EOC}$ = V_{DD}, A_{IN} = 0 V			5	8	mA
Negative Supply Current	I_{SS}	SC/$\overline{EOC}$ = V_{DD}, A_{IN} = 0 V			−6	−11	mA
Power Dissipation	P_{DISS}	V_{DD} = +5 V, V_{SS} = −15 V			135	205	mW

TIMING CHARACTERISTICS[3] (V_{DD} = +5 V, V_{SS} = −12 V or −15 V; −40°C ≤ T_A ≤ +85°C)

CLOCK Pulse Width	t_{CH}	CLK HIGH		40			ns
	t_{CL}	CLK LOW		60			ns
SC/$\overline{EOC}$ Pulse Width	t_{SH}	SC/$\overline{EOC}$ HIGH		40			ns
	t_{SL}	SC/$\overline{EOC}$ LOW		60			ns
SC/$\overline{EOC}$ to CLK Skew	t_{SC0}	Leading CLK				40	ns
	t_{SC1}	Leading CLK + 1		200			ns
CLK to SDO Delay	t_{PD}			25		80	ns

NOTES
[1]Guaranteed by design, not subject to test.
[2]Specified performance with −12 V supply is guaranteed by testing offset and full-scale errors.
[3]Timing specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with t_R = t_F = 5 ns (10% to 90% of +5 V) and timed from a voltage level of +1.6 V.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ADC-910

FEATURES

- Includes Clock, Reference, 3-State Buffered Outputs
- Fast Conversion Time 6μs
- Four Input Ranges . . +/−2.5V, +/−5.0V, +5.0V and +10.0V
- 1/2 LSB INL
- No Missing Codes Over Temperature
- Low ESD Sensitivity Due to Rugged Bipolar Processing
- Software Programmable Unipolar/Bipolar
- Easily Interfaced to 8 and 16-Bit μP Bus
- Available in Die Form

ORDERING INFORMATION†

PMI MODEL NO.	TEMPERATURE RANGE
ADC910AT* ADC910BT*	−55°C/+125°C
ADC910ET ADC910FT	−25°C/+85°C
ADC910GT ADC910HT	0°C/+70°C

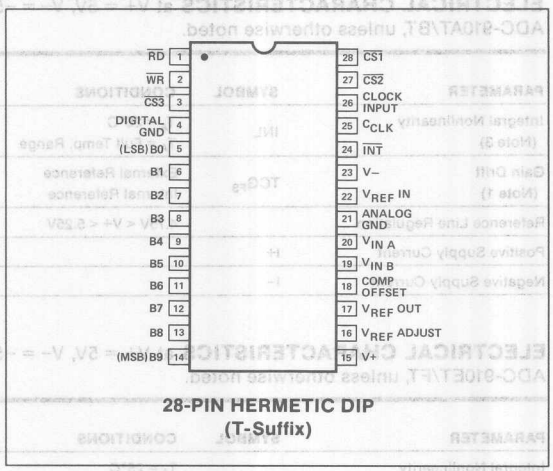
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

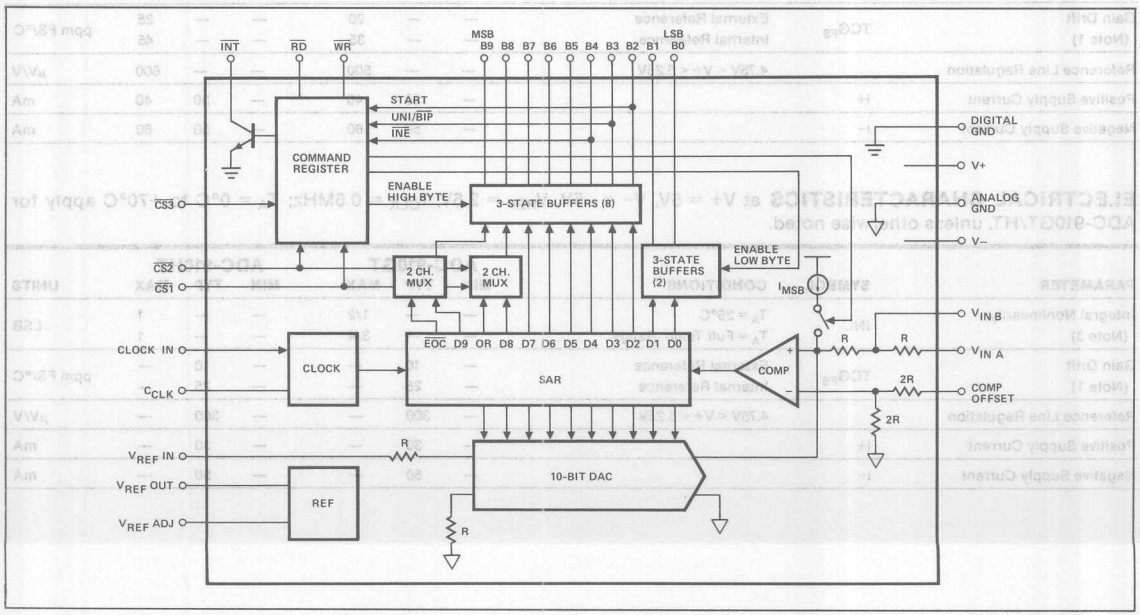
The ADC-910 is a 10-bit A/D converter designed specifically for interfacing with microprocessors. 3-state data outputs allow direct connection to an 8-bit data bus in an MSB byte of 8 bits and an LSB byte of 2 bits. A command register with read/write inputs and 3 Chip Select inputs to control the 10 data lines is included. Interrupt enable, start conversion and bipolar/unipolar mode selection are controlled by the data bus. The use of high-speed Linear Differential Logic results in fast (6μs) conversion time and low power dissipation.

PIN CONNECTIONS



28-PIN HERMETIC DIP (T-Suffix)

SIMPLIFIED SCHEMATIC



Operating Temperature Range
ADC-910AT/BT ..... −55°C to +125°C
ADC-910ET/FT ..... −25°C to +85°C
ADC-910GT/HT ..... 0°C to +70°C
Maximum Junction Temperature (T_j) ..... 175°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Supply Voltage (V+) 6V
Supply Voltage (V−) 6V
V+ to V− 12V
Logic Inputs ..... +6V, −0.3V
$V_{IN\ A}$ 15V
$V_{IN\ B}$ 7.5V
Reference Inputs 3.0V
Digital Ground to Analog Ground Voltage 0.5V

PACKAGE TYPE	Θ_{jA} (Note 1)	Θ_{jC}	UNITS
28-Pin Hermetic DIP (T)	50	7	°C/W

NOTE:
1. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for CerDIP package.

ELECTRICAL CHARACTERISTICS at V+ = 5V, V− = −5V, V_{REF} = 2.5V, f_{CLK} = 0.5MHz; T_A = −55°C to +125°C apply for ADC-910AT/BT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ADC-910AT MIN	ADC-910AT TYP	ADC-910AT MAX	ADC-910BT MIN	ADC-910BT TYP	ADC-910BT MAX	UNITS
Integral Nonlinearity (Note 3)	INL	T_A = 25°C	—	—	1/2	—	—	1	LSB
		T_A = Full Temp. Range	—	—	3/4	—	—	1	
Gain Drift (Note 1)	TCG_{FS}	External Reference	—	—	25	—	—	30	ppm FS/°C
		Internal Reference	—	—	40	—	—	50	
Reference Line Regulation		4.75V < V+ < 5.25V	—	—	500	—	—	600	μV/V
Positive Supply Current	I+		—	30	40	—	30	40	mA
Negative Supply Current	I−		—	50	60	—	50	60	mA

ELECTRICAL CHARACTERISTICS at V+ = 5V, V− = −5V, V_{REF} = 2.5V, f_{CLK} = 0.5MHz; T_A = −25°C to +85°C apply for ADC-910ET/FT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ADC-910ET MIN	ADC-910ET TYP	ADC-910ET MAX	ADC-910FT MIN	ADC-910FT TYP	ADC-910FT MAX	UNITS
Integral Nonlinearity (Note 3)	INL	T_A = 25°C	—	—	1/2	—	—	1	LSB
		T_A = Full Temp. Range	—	—	1/2	—	—	1	
Gain Drift (Note 1)	TCG_{FS}	External Reference	—	—	20	—	—	25	ppm FS/°C
		Internal Reference	—	—	35	—	—	45	
Reference Line Regulation		4.75V < V+ < 5.25V	—	—	500	—	—	600	μV/V
Positive Supply Current	I+		—	30	40	—	30	40	mA
Negative Supply Current	I−		—	50	60	—	50	60	mA

ELECTRICAL CHARACTERISTICS at V+ = 5V, V− = −5V, V_{REF} = 2.5V, f_{CLK} = 0.5MHz; T_A = 0°C to +70°C apply for ADC-910GT/HT, unless otherwise noted.

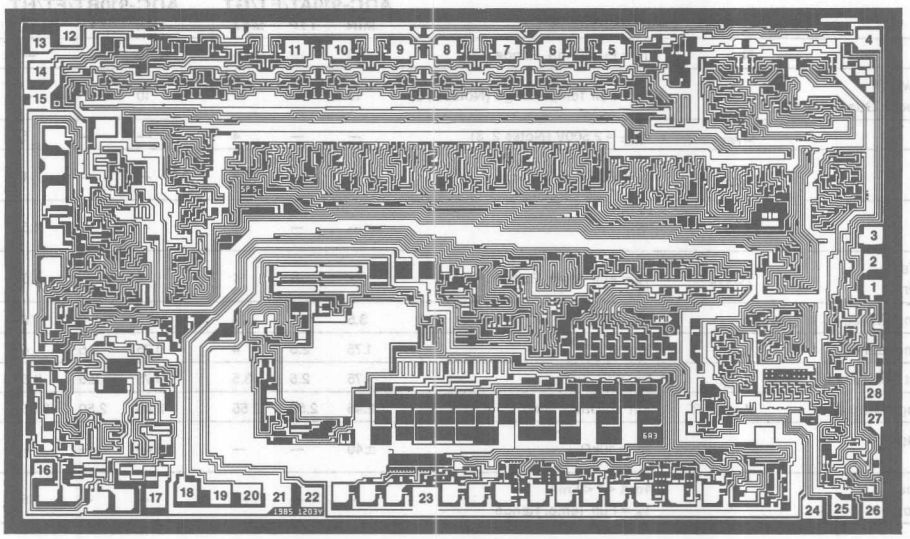
PARAMETER	SYMBOL	CONDITIONS	ADC-910GT MIN	ADC-910GT TYP	ADC-910GT MAX	ADC-910HT MIN	ADC-910HT TYP	ADC-910HT MAX	UNITS
Integral Nonlinearity (Note 3)	INL	T_A = 25°C	—	—	1/2	—	—	1	LSB
		T_A = Full Temp. Range	—	—	3/4	—	—	1	
Gain Drift (Note 1)	TCG_{FS}	External Reference	—	10	—	—	10	—	ppm FS/°C
		Internal Reference	—	25	—	—	25	—	
Reference Line Regulation		4.75V < V+ < 5.25V	—	300	—	—	300	—	μV/V
Positive Supply Current	I+		—	30	—	—	30	—	mA
Negative Supply Current	I−		—	50	—	—	50	—	mA

ELECTRICAL CHARACTERISTICS at V+ = 5V, V− = −5V, V_{REF} = 2.5V, f_{CLK} = 0.5MHz; T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ADC-910AT/ET/GT MIN	TYP	MAX	ADC-910BT/FT/HT MIN	TYP	MAX	UNITS
Resolution	N	T_A = Full Temp. Range	10	—	—	10	—	—	Bits
Resolution for which No Missing Codes Guaranteed		T_A = Full Temp. Range (Notes 2, 3)	10	—	—	10	—	—	Bits
Gain Error	G_{FSE}	V_{REF} = 2.500V (Notes 2, 3)	—	—	4	—	—	6	LSB
Unipolar Mode Offset Error	V_{ZSE}	T_A = Full Temp. Range	—	—	1/2	—	—	1	LSB
Bipolar Mode Offset Error	V_{OSE}		—	—	1	—	—	1.5	LSB
Bipolar Mode Zero-Scale Offset Drift	TCV_{ZS}	T_A = Full Temp. Range (Note 1)	—	—	1	—	—	1.5	LSB
Analog Input Impedance	$R_{IN\,A}$	Pin 20	3.5	5	8	3.5	5	8	kΩ
Analog Input Impedance	$R_{IN\,B}$	Pin 19	1.75	2.5	4	1.75	2.5	4	kΩ
Reference Input Resistance	R_{REF}	Pin 22	1.75	2.5	3.5	1.75	2.5	3.5	kΩ
Reference Voltage Output	$V_{REF}OUT$	Pin 17, Untrimmed	2.45	2.50	2.55	2.45	2.50	2.55	V
Reference Voltage Trim Range		R_T = 10kΩ	±40	—	—	±40	—	—	mV
Reference Output Load Regulation		1mA < I < 5mA, T_A = Full Temp. Range	—	—	1.5	—	—	1.5	mV/mA
Positive Power Supply Sensitivity	$+P_{SS}$	4.75V to 5.25V	—	—	1/2	—	—	1/2	LSB
Negative Power Supply Sensitivity	$-P_{SS}$	−4.75V to −5.25V	—	—	1/2	—	—	1/2	LSB
Conversion Time	T_C	f_{CLK} = 1MHz (Note 4)	—	—	6	—	6	—	μs
Conversion Time	T_C	f_{CLK} = 0.5MHz (Note 5)	—	—	12	—	12	—	μs
Digital Input High	V_{INH}	T_A = Full Temp. Range	2.0	—	—	2.0	—	—	V
Digital Input Low	V_{INL}	T_A = Full Temp. Range	—	—	0.8	—	—	0.8	V
Digital Input Current	I_{INH}	T_A = Full Temp. Range	—	0.4	1	—	0.4	1	μA
Digital Input Current	I_{INL}	T_A = Full Temp. Range	—	10	20	—	10	20	μA
Digital Output High	V_{OH}	I_{OH} = −400μA, T_A = Full Temp. Range	2.4	3.7	—	2.4	3.7	—	V
Digital Output Low	V_{OL}	I_{OL} = 1.6mA, T_A = Full Temp. Range	—	0.1	0.4	—	0.1	0.4	V
Digital Output Current	I_{OH}	V_{OH} = 2.4V	−400	—	—	−400	—	—	μA
Digital Output Current	I_{OL}	V_{OL} = 0.4V	—	—	1.6	—	—	1.6	mA
Three-State Output Leakage	I_{OZ}	T_A = Full Temp. Range	—	5	10	—	5	10	μA

NOTES:
1. Change in 25°C value from 25°C to T_{Min} or T_{Max}.
2. Tested in the 5V unipolar mode at 6μs conversion time.
3. Tested in the ±5V bipolar mode at 12μs conversion time.
4. Applies to 5V input unipolar operation; see Figure 1 for connections.
5. Applies to 10V input unipolar operation, and ±5V/±10V input bipolar operation; see Figure 1 for connections.

DICE CHARACTERISTICS



DIE SIZE 0.131 × 0.221 inch, 28,951 sq. mils
(3.33 × 5.61 mm, 18.68 sq. mm)

1. $\overline{RD}$
2. $\overline{WR}$
3. $\overline{CS3}$
4. DIGITAL GND
5. B0 (LSB)
6. B1
7. B2
8. B3
9. B4
10. B5
11. B6
12. B7
13. B8
14. B9 (MSB)
15. V+
16. V_{REF} ADJUST
17. V_{REF} OUT
18. COMP OFFSET
19. $V_{IN\ B}$
20. $V_{IN\ A}$
21. ANALOG GND
22. V_{REF} IN
23. V−
24. $\overline{INT}$
25. C_{CLK}
26. CLOCK INPUT
27. $\overline{CS2}$
28. $\overline{CS1}$

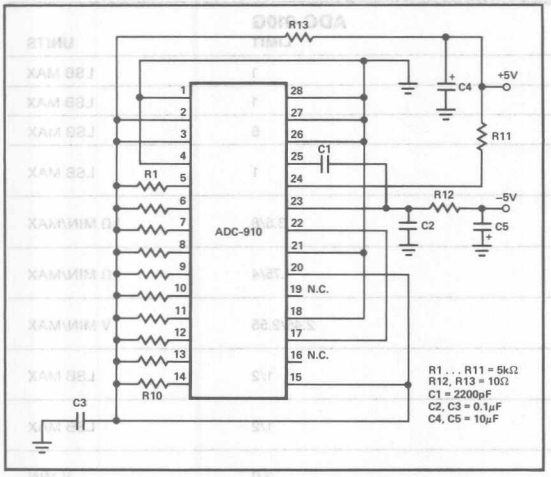
WAFER TEST LIMITS at V+ = 5V, V− = −5V, V_{REF} = 2.5V, and T_A = 25°C.

PARAMETER	SYMBOL	CONDITIONS	ADC-910G LIMIT	UNITS
Integral Nonlinearity	INL		1	LSB MAX
Differential Nonlinearity	DNL		1	LSB MAX
Gain Error	G_{FSE}	V_{REF} = 2.500V	6	LSB MAX
Unipolar Mode Offset Error	V_{ZSE}		1	LSB MAX
Analog Input Impedance	$R_{IN\,A}$	Pin 20	3.5/8	kΩ MIN/MAX
Reference Input Resistance	R_{REF}	Pin 22	1.75/4	kΩ MIN/MAX
Reference Voltage Output	$V_{REF}OUT$	Pin 17, Untrimmed	2.45/2.55	V MIN/MAX
Positive Power Supply Sensitivity	$+P_{SS}$	4.5V to 5.5V	1/2	LSB MAX
Negative Power Supply Sensitivity	$-P_{SS}$	−4.5V to −5.5V	1/2	LSB MAX
Digital Input High	V_{INH}		2.0	V MIN
Digital Input Low	V_{INL}		0.8	V MAX
Digital Input Current	I_{INH} I_{INL}		1 20	μA MAX
Digital Output High	V_{OH}	I_{OH} = −400μA	2.4	V MIN
Digital Output Low	V_{OL}	I_{OL} = 1.6mA	0.4	V MAX
Digital Output Current	I_{OH} I_{OL}	V_{OH} = 2.4V V_{OL} = 0.4V	−400 1.6	μA MIN mA MAX
Three-State Output Leakage	I_{OZ}		10	μA MAX
Positive Supply Current	I+		40	mA MAX
Negative Supply Current	I−		60	mA MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V+ = 5V, V− = −5V, V_{REF} = 2.5V, and T_A = 25°C.

PARAMETER	SYMBOL	CONDITIONS	ADC-910G TYPICAL	UNITS
Conversion Time	T_C	f_{CLK} = 1MHz, 5V Unipolar Mode f_{CLK} = 0.5MHz ±5V Bipolar Mode	6 12	μs



APPLICATIONS INFORMATION

CIRCUIT OPERATION (Refer to the Simplified Schematic)

The ADC-910 uses a successive approximation type A/D conversion routine. When a start command is received by the command register, the SAR, DAC and comparator begin a bit-by-bit trial against the analog input voltage. When all ten bits have been tried, the ten data outputs of the SAR will contain a 10-bit digital representation of the analog input voltage.

When the conversion is complete, a read command and a chip selection will output the data through the 3-state output buffers. Selecting CS1 will output the eight MSBs (the high byte) and selecting CS2 will output the two LSBs (the low byte). Selecting both CS1 and the CS2 will cause all ten data bits to be output through the 3-state output buffers.

When the conversion is complete, the SAR sends an end of conversion (EOC) signal to the command register, which ($\overline{INT}$), providing the interrupt disable bit ($\overline{INE}$) is set to "0". The EOC signal is also multiplexed into the input of the 3-state buffer for bit 9 (B9). Also, at this time, the overrange signal appears at the SAR output and is multiplexed into the input of the 3-state buffer for bit 8 (B8). These two bits of information comprise the status register, which is multiplexed to the data bus with a read command and a selection of $\overline{CS3}$.

Unipolar/bipolar mode selection and the enabling/disabling of the interrupt output is done when the start of conversion command is entered. In the unipolar mode, the I_{MSB} current source is turned off. For bipolar mode operation, the I_{MSB} current source is applied to the summing mode of the comparator. This provides the proper offset of I_{MSB} to do a bipolar conversion.

BASIC CONNECTIONS (Refer to Figure 1)

Power Supply Connections: The ADC-910 is operated on ±5 volt power supplies. +5 volts is applied to pin 15 and −5 volts is applied to pin 23. These lines should be bypassed near the device with a 0.1μF capacitor in parallel with a large value capacitor such as 10μF.

Analog and Digital Ground: Separate analog and digital grounds are provided to maintain optimum noise rejection. Care should be maintained to insure that digital switching noise is not introduced into the analog ground line. This can be accomplished by making the final ground point as close (physically and electrically) as possible to the analog ground pin of the ADC-910.

Analog Inputs: There are two analog voltage inputs to the ADC-910. $V_{IN\,A}$ (pin 20) accepts input signals between 0 volts and +10 volts in the unipolar mode and between −5 volts and +5 volts in the bipolar mode. $V_{IN\,B}$ (pin 19) accepts input signal levels between 0 volts and +5 volts in the unipolar mode and between −2.5 volts and +2.5 volts in the bipolar mode. The input resistance is nominally 5kΩ for $V_{IN\,A}$ and 2.5kΩ for $V_{IN\,B}$. The comparator offset pin (pin 18) is left open when using $V_{IN\,A}$, and is tied to analog ground when using $V_{IN\,B}$.

FIGURE 1: Basic Connections

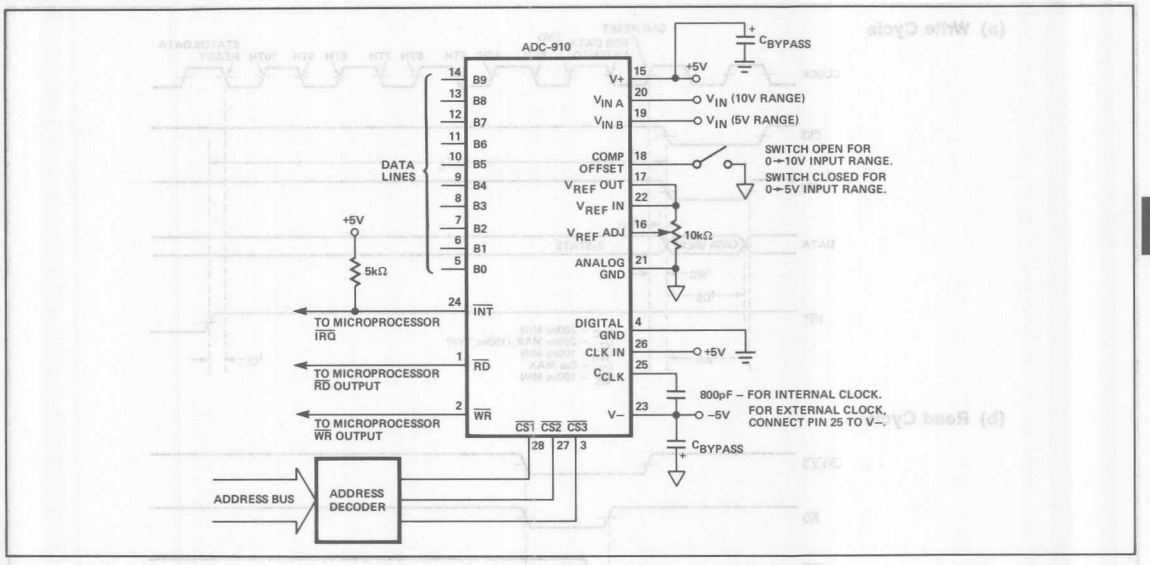


FIGURE 2: Start Conversion and Operating Mode Selection
(Write Mode $\overline{WR}$ = "Low", CS3 = "Low")

MSB B9	B8	B7	B6	B5	B4 (Interrupt Disable/ Enable)	B3 (Unipolar/ Bipolar Select)	B2 (Start Bit)	B1	LSB B0	
X	X	X	X	X	0	0	1	X	X	Start Conversion, Bipolar Mode, Interrupt Enabled.
X	X	X	X	X	1	1	1	X	X	Start Conversion, Unipolar Mode, Interrupt Disabled.

X = "Don't Care"

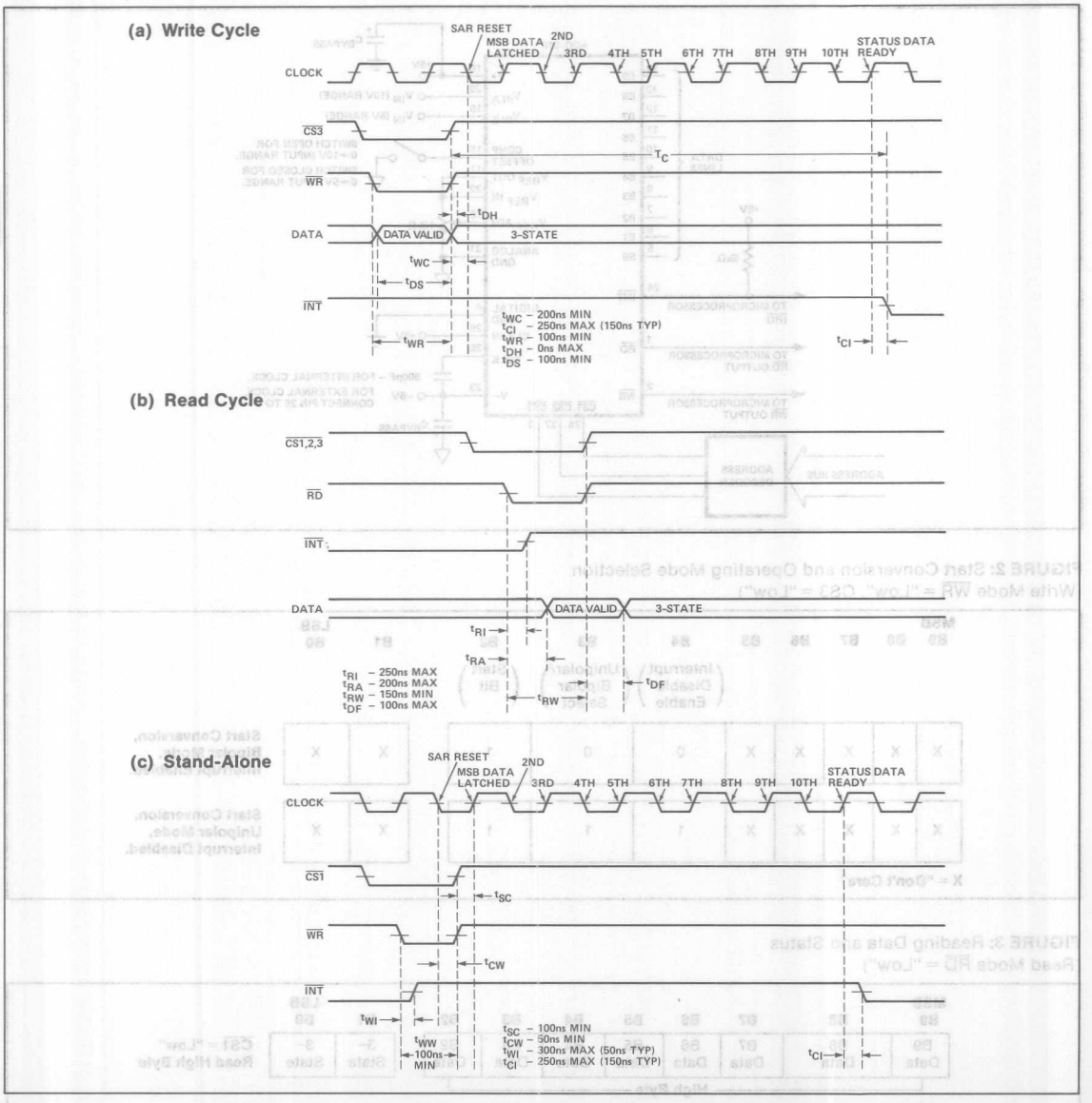
FIGURE 3: Reading Data and Status
(Read Mode $\overline{RD}$ = "Low")

MSB B9	B8	B7	B6	B5	B4	B3	B2	B1	LSB B0	
B9 Data	B8 Data	B7 Data	B6 Data	B5 Data	B4 Data	B3 Data	B2 Data	3-State	3-State	$\overline{CS1}$ = "Low" Read High Byte
				High Byte						
3-State	3-State	3-State	3-State	3-State	3-State	3-State	3-State	B1 Data	B0 Data	$\overline{CS2}$ = "Low" Read Low Byte
								Low Byte		
Busy Bit	Overrange Bit	X	X	X	X	X	X	3-State	3-State	$\overline{CS3}$ = "Low" Read Status

1 = Overrange
0 = Within Range

1 = Busy
0 = Conversion Complete

FIGURE 4: ADC-910 Timing Diagrams



Voltage Reference: The voltage reference for the ADC-910 is nominally +2.5 volts. To use this internal reference, the reference output pin (pin 17) should be tied to the reference input pin (pin 22). Adjustment of the reference voltage may be done by applying a 10kΩ trimmer between the reference output and analog ground with the center tap wiper tied to the reference adjust pin (pin 16).

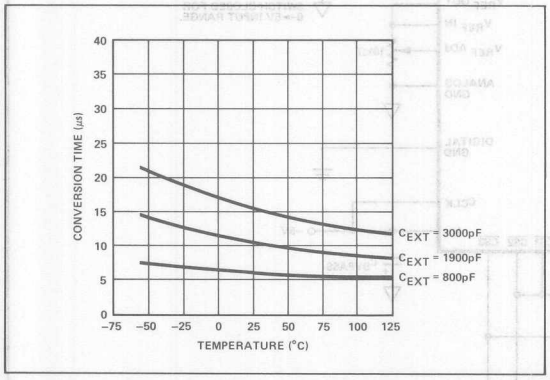
To use an external reference with the ADC-910, simply apply it to the V_{REF} input pin (pin 22). This voltage should be bypassed to analog ground with a 0.01μF capacitor.

Clock: For internal clock operation, the external capacitor (C_{CLK}) sets the conversion rate. The conversion rate graph provides the relationship of C_{CLK} and temperature to conversion rate. The C_{CLK} capacitor is connected between C_{CLK} (pin 25) and the V– supply (pin 23), see Figure 1. The clock input (pin 26) is connected to the V+ supply (pin 15). Internal clock operation exhibits a conversion time variation from device to device for a given C_{CLK}, due to capacitor and internal resistor tolerances of the basic R-C oscillator. For operation at the upper frequencies of 0.5 and 1MHz, an external clock input is recommended.

For external clock operation, no clock capacitor is required. The C_{CLK} pin (pin 25) should be tied to the –5 volt supply and the external clock is applied to the clock input (pin 26). 1.0MHz clock maximum may be used. This will result in a 6μs conversion time. Slower clock rates will result in slower conversion speeds.

$$\text{Conversion time} \approx 6 \times \frac{1}{f_{CLK}}$$

Conversion time (T_C) also depends on user supplied timing relationship between positive $\overline{WR}$ edge and negative clock edge used to reset the SAR. See Figure 4(a) t_{WC} parameter.



CHIP SELECT, READ AND WRITE INPUTS

(Refer to Figure 2)

Start Commands: To start a conversion the $\overline{WR}$ input (pin 2) must be held "low" while $\overline{CS3}$ (pin 3) is held "low" and a logic "high" is applied to bit 2 (pin 7). Another way to start a conversion is to hold $\overline{CS1}$ (pin 28) and $\overline{WR}$ (pin 2) "low" for a complete clock cycle.

Operating mode selection is done when the start command is applied. As with the start command, $\overline{WR}$ and $\overline{CS3}$ are held "low". A logic "high" applied to bit 4 (pin 9) disables the interrupt and a logic "low" enables the interrupt. A logic "high" applied to bit 3 (pin 8) selects unipolar mode and a logic "low" selects bipolar-mode operation.

READING DATA AND CONVERSION STATUS

(Refer to Figure 3)

Data can be read in two ways: a single 10-bit word or in a 8-bit "high byte" with a 2-bit "low byte". When interfacing to a 16-bit bus, single 10-bit word reading is possible. When using an 8-bit data bus, the "high byte" and "low byte" can be multiplexed onto a single 8-bit bus as indicated in Figure 5.

To read all 10 bits at once, the RD (pin 1), CS1 (pin 28) and CS2 (pin 27) are all held "low". This turns on 3-state output buffers and all data bits can be read.

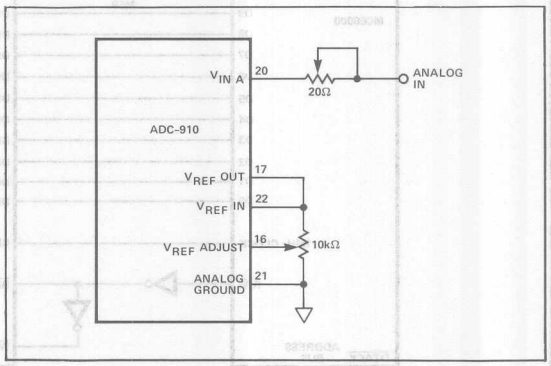
To read the 8-bit "high byte", the RD (pin 1) and CS1 (pin 28) lines are held "low".

To read the 2-bit "low byte", the RD and CS2 lines are held "low".

Included on the ADC-910 is a 2-bit status register which is multiplexed onto the data bus on lines B9 and B8.

To read the status register, RD (pin 1) and CS3 are held "low". End of conversion (EOC) is indicated by a "low" bit 9 (pin 14) and overrange (OR) is indicated by a "high" in bit 8 (pin 13).

FIGURE 5: Calibration Circuit



CALIBRATION (Refer to Figure 5)

Unipolar Mode: To adjust out gain error, a trimmer may be inserted in series with the analog input voltage input. Assuming a 2.500 volt reference is applied at the reference input, gain error trimming is accomplished by adjusting the input trimmer so that the final digital output code transition occurs for an input voltage of $V_A = 9.985$ volts (this is the transition from 1111 1111 10 to 1111 1111 11). When using the internal reference or an adjustable external reference, gain error trimming may be accomplished by adjusting the reference voltage until the final digital output code transition occurs at $V_A = 9.985$ volts.

Bipolar Mode: To trim out offset error, set series trimmer (if used) to 0Ω and tie $V_{IN\,A}$ to analog ground. Adjust V_{REF} to just beyond the major carry transition (that point where the digital output code changes from 0111 1111 11 to 1000 0000 00).

To trim out gain error, tie $V_{IN\,A}$ to voltage source. Adjust the series trimmer so that the final digital output code transition (from 1111 1111 10 to 1111 1111 11) occurs at an input voltage of +4.9902V.

DRIVING THE ANALOG INPUT

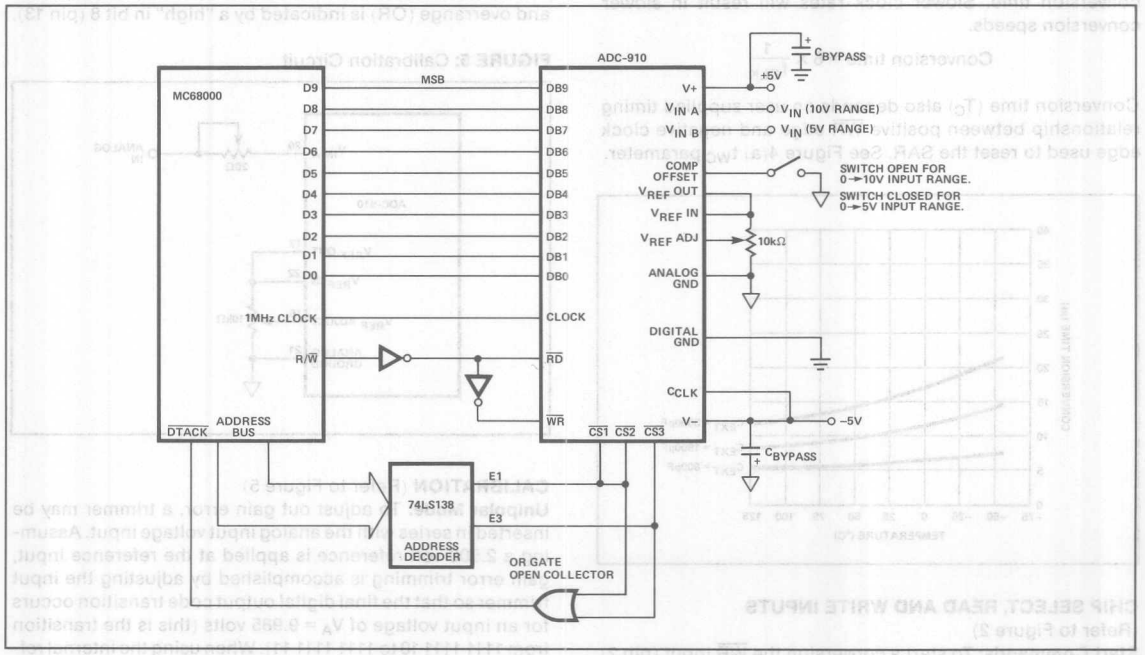
To insure 10-bit accuracy the input to the ADC-910 must be driven by a source which has an output impedance of less than 0.5 ohms at 1MHz.

INTERFACING THE ADC-910 TO THE MC68000

(Refer to Figure 6)

An example of a direct connection to a 16-bit data bus is shown in Figure 6. The 10-bit output of the ADC-910 is connected directly to the 10 least significant bits of the MC68000 data bus. In this example, a Motorola MC68000 Computer Board supports the 68000μP. A flow chart and assembly language program is shown below for a simplified 10-bit wide conversion.

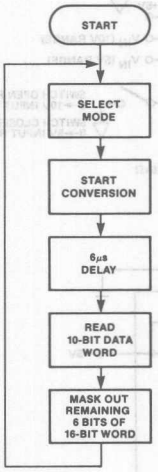
FIGURE 6: ADC-910 Interface to MC68000 Computer Board



INTERFACING THE ADC-910 TO THE 6502μP

(Refer to Figure 7)

An example of direct connection to an 8-bit data bus is shown in Figure 7. Notice that the two least significant bits are connected to data bits B3 and B4. This allows a 10-bit data transfer over an 8-bit bus. In this example, a Synertek Systems SYM-1 Educational Computer Board supports the 6502μP. The flow charts and op codes for a variety of conversion exercises are shown below.



PC	MNEMONIC	COMMENT
1000	MOVEQ #12, D0	Select Mode*
1002	MOVE D0, $50000	Start Conversion
1008	NOP	
100A	NOP	Delay
100C	NOP	
100E	MOVE $20000, D1	Read Data
1014	ANDI #1023, D1	Mask out B15→B10 leaving B9→B0
1018	JMP $1000	Jump to 1000

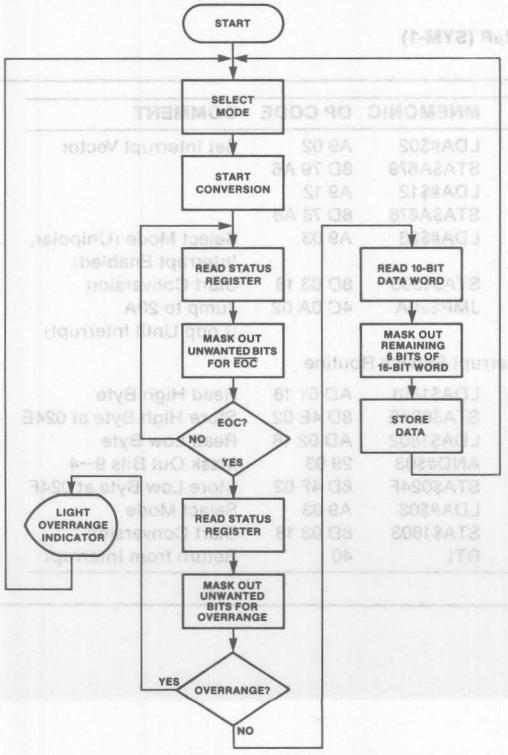
* Loading a decimal 12 into D0 will apply the following binary word to the command register at the start of the conversion:

B9 B8 B7 B6 B5 B4 B3 B2 B1 B0

0 0 0 0 0 0 1 1 0 0

This results in unipolar mode selection with the interrupt disabled.

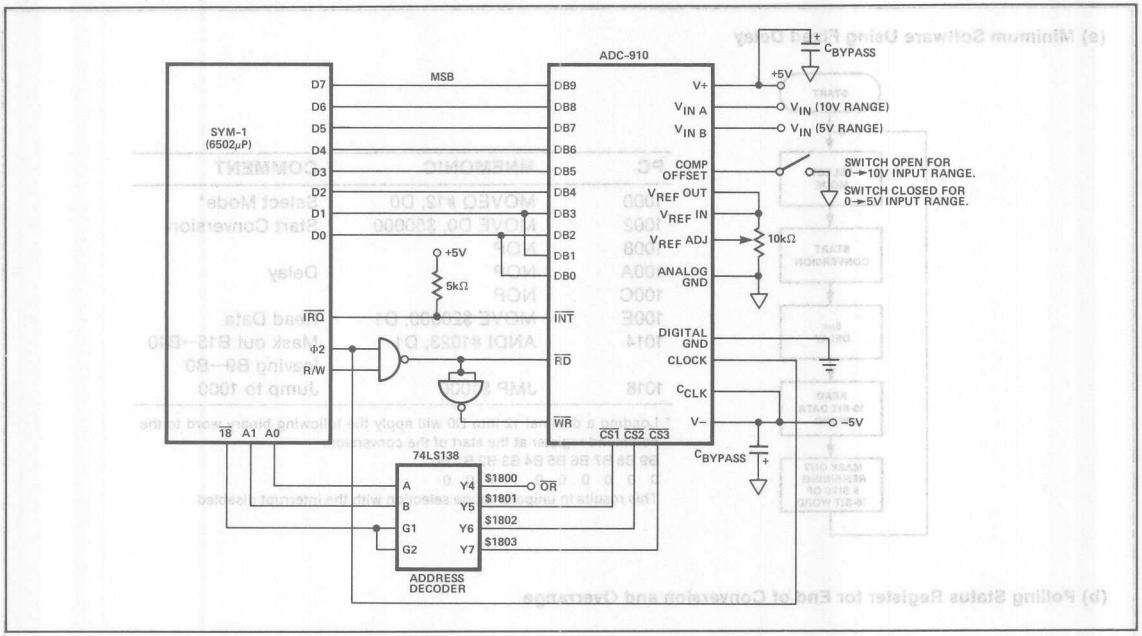
(b) Polling Status Register for End of Conversion and Overrange



PC	MNEMONIC	COMMENT
1000	MOVEQ #X,D0	Select Mode*
1002	MOVE D0, $50000	Start Conversion
1008	MOVE $50000,D1	Read Status Register into D1
100E	AND #512,D1	Mask for EOC Bit (1000000000 = 512 Decimal)
1012	BNE.L $1008	Loop Until EOC
1016	MOVE $50000,D2	Read Status Register
101C	AND #256,D2	Mask for OR Bit (0100000000 = 256 Decimal)
1020	BEQ.L $102E	Branch to $102E Unless OR
1024	MOVE D3,$40000	Light OR Indicator
102A	JMP $1000	Start Over
102E	MOVE $20000,D4	Read and Store 10-Bit Data
1032	AND #1023,D4	Mask Unwanted 6 LSBs
1036	JMP $1000	Start Over

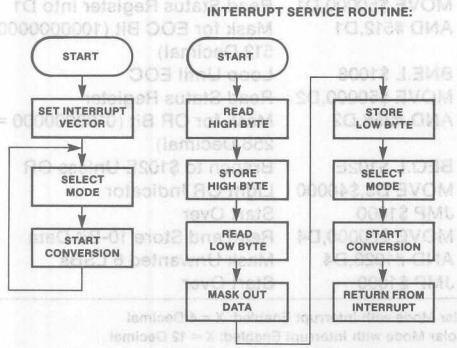
*For Bipolar Mode with Interrupt Enabled: X = 4 Decimal
For Unipolar Mode with Interrupt Enabled: X = 12 Decimal
For Bipolar Mode, Interrupt Disabled: X = 20 Decimal
For Unipolar Mode, Interrupt Disabled: X = 28 Decimal

FIGURE 7: ADC-910 Interface to 6502μP on SYM-1 Board



ADC-910 INTERFACE SOFTWARE AND FLOW CHART FOR 6502μP (SYM-1)

Interrupt-Driven Conversion



PC	MNEMONIC	OP CODE	COMMENT
0200	LDA#$02	A9 02	Set Interrupt Vector
0202	STA$A679	8D 79 A6	
0205	LDA#$12	A9 12	
0207	STA$A678	8D 78 A6	
020A	LDA#$03	A9 03	Select Mode (Unipolar, Interrupt Enabled)
020C	STA$1803	8D 03 18	Start Conversion
020F	JMP$20A	4C 0A 02	Jump to 20A (Loop Until Interrupt)
	Interrupt Service Routine		
0212	LDA$1801	AD 01 18	Read High Byte
0215	STA$024E	8D 4E 02	Store High Byte at 024E
0218	LDA$1802	AD 02 18	Read Low Byte
021B	AND#$03	29 03	Mask Out Bits 9→4
021D	STA$024F	8D 4F 02	Store Low Byte at 024F
0220	LDA#$03	A9 03	Select Mode
0222	STA$1803	8D 03 18	Start Conversion
0225	RTI	40	Return from Interrupt

CMOS Microprocessor-Compatible 12-Bit A/D Converter

ADC-912A

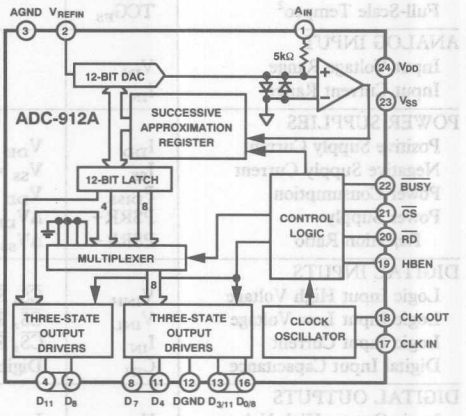
FEATURES

- Low Cost
- Low Transition Noise Between Codes
- 12-Bit Accurate
  - ±1/2 LSB Nonlinearity Error Over Temperature
  - No Missing Codes at All Temperatures
- 10 Microsecond Conversion Time
- Internal or External Clock
- 8- or 16-Bit Data Bus Compatible
- Improved ESD Resistant Design
- Latchup Resistant Epi-CMOS Processing
- Low 95 mW Power Consumption
- Space Saving 24-Pin 0.3″ DIP, or 24-Lead SOIC

APPLICATIONS

- Data Acquisition Systems
- DSP System Front End
- Process Control Systems
- Portable Instrumentation

FUNCTIONAL BLOCK DIAGRAM



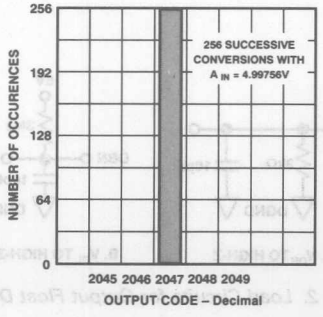
GENERAL DESCRIPTION

The ADC-912A is a monolithic 12-bit accurate CMOS A/D converter. It contains a complete successive approximation A/D converter built with a high accuracy D/A converter, a precision bipolar transistor high-speed comparator, and successive approximation logic including three-state bus interface for logic compatibility. The accuracy of the ADC-912A results from the addition of precision bipolar transistors to Analog Device's advanced-oxide isolated silicon-gate CMOS process. Particular attention was paid to the reduction of transition noise between adjacent codes achieving a 1/6 LSB uncertainty. The low noise design produces the same digital output for dc analog inputs not located at a transition voltage, see the Code Repetition and Transition Noise plots below. NPN digital output transistors provide excellent bus interface timing, 125 ns access and bus disconnect time which results in faster data transfer without the need for wait states. An external 1.25 MHz clock provides a 10 μs conversion time.

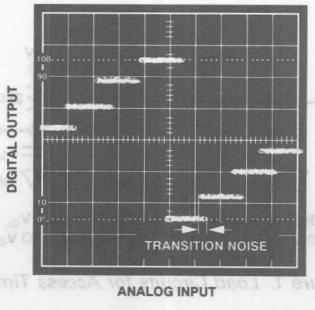
In stand alone applications an internal clock can be used with external crystal.

An external negative five-volt reference sets the 0 to +10 V input range. Plus five and minus 12 volt power supplies result in 95 mW of total power consumption.

For military operating temperature range (−55°C to +125°C) versions contact your local Analog Devices sales office.



Code Repetition



Transition Noise Crossplot

ADC-912A—SPECIFICATIONS

(V_{DD} = +5 V ± 5%, V_{SS} = −11.4 V to −15.75 V, V_{REFIN} = −5 V, Analog Input 0 to +10 V; External f_{CLK} = 1.25 MHz; −40°C to +85°C apply for ADC912AE/F, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC ACCURACY						
Integral Nonlinearity	INL	ADC912AE	−1/2		+1/2	LSB
		ADC912AF	−1		+1	LSB
Differential Nonlinearity	DNL		−1		+1	LSB
Offset Error	V_{ZSE}	V_{DD} = +5 V, V_{SS} = −12 V	−5		+5	LSB
Gain Error	G_{FSE}	V_{DD} = +5 V, V_{SS} = −12 V	−6		+6	LSB
Full-Scale Tempco[2]	TCG_{FS}			5	15	ppm/°C
ANALOG INPUT						
Input Voltage Range	V_{IN}		0		+10	V
Input Current Range	I_{IN}		0		+3	mA
POWER SUPPLIES						
Positive Supply Current	I_{DD}	V_{DD} = +5 V[1]		5	7	mA
Negative Supply Current	I_{SS}	V_{SS} = −12 V[1]		3	5	mA
Power Consumption	P_{DISS}	V_{DD} = +5 V, V_{SS} = −12 V[1]		70	95	mW
Power Supply	PSRR+	ΔV_{DD} = ±5%, AIN = 10 V		1/2	4	LSB
Rejection Ratio	PSRR−	ΔV_{SS} = ±5%, AIN = 10 V		1/2	4	LSB
DIGITAL INPUTS						
Logic Input High Voltage	V_{INH}	$\overline{CS}$, $\overline{RD}$, HBEN	2.4			V
Logic Input Low Voltage	V_{INL}	$\overline{CS}$, $\overline{RD}$, HBEN			0.8	V
Logic Input Current	I_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN			±1	µA
Digital Input Capacitance	C_{IN}	Digital Inputs, $\overline{CS}$, $\overline{RD}$, HBEN, CLKIN		7	10	pF
DIGITAL OUTPUTS						
Logic Output High Voltage	V_{OH}	I_{SOURCE} = 0.2 mA	4			V
Logic Output Low Voltage	V_{OL}	I_{SINK} = 1.6 mA			0.4	V
Three-State Output Leakage	I_{OZ}	D11–D0/8			10	µA
Digital Output Capacitance	C_{OUT}	D11–D0/8[2]		8	15	pF
DYNAMIC PERFORMANCE						
Conversion Time	TC	f_{CLK} = 1.25 MHz[3]				
		Synchronous Clock			10.4	µs
		Asynchronous Clock	10.4		11.2	µs

NOTES
[1]Converter inactive; $\overline{CS}$, $\overline{RD}$ = High, A_{IN} = +10 V.
[2]Guaranteed by design.
[3]See Synchronizing Start Conversion information in Converter Operation Details.

Typicals (typ) are median values measured at +25°C. See Typical Performances Characteristics for additional information.

Specifications subject to change without notice.

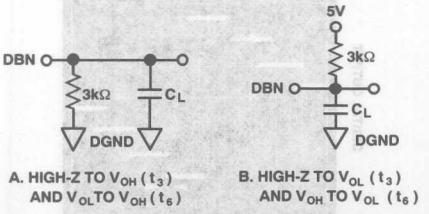


Figure 1. Load Circuits for Access Time

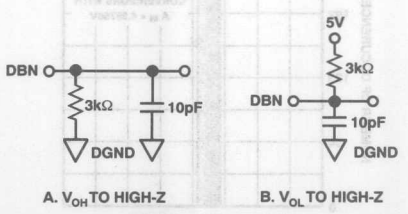


Figure 2. Load Circuits for Output Float Delay

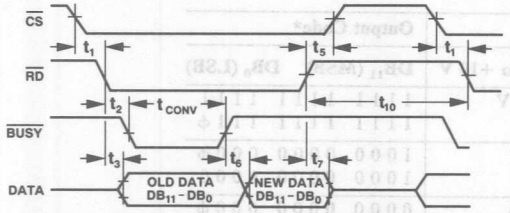
TIMING CHARACTERISTICS[1, 2]

(V_{DD} = +5 V ± 5%, V_{SS} = −11.4 V to −15.75 V, V_{REFIN} = −5 V, Analog Input 0 to +10 V; External f_{CLK} = 1.25 MHz; −40°C to +85°C apply for ADC912AE/F, unless otherwise noted. See Figures 3 to 6.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1		0			ns
$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay	t_2				150	ns
Data Access Time After READ	t_3[3]	C_L = 100 pF		65	125	ns
Read Pulse Width	t_4[3]		90			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		0			ns
New Data Valid After $\overline{BUSY}$	t_6[3]	C_L = 100 pF		−30	0	ns
Bus Disconnect Time	t_7[4]		20	60	90	ns
HBEN to $\overline{RD}$ Setup Time	t_8		0			ns
HBEN to $\overline{RD}$ Hold Time	t_9		0			ns
Delay between Successive Read Operations	t_{10}		350	250		ns

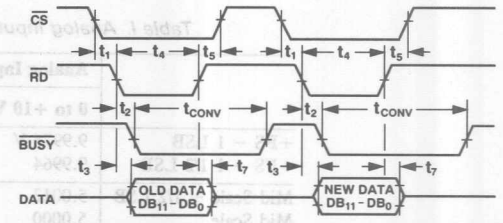
NOTES
[1]Guaranteed by design.
[2]All input control signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[3]t_3, t_4, and t_6 are measured with the load circuits of Figure 1 and timed for and output to cross 0.8 V or 2.4 V.
[4]t_7 is the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.

TIMING DIAGRAMS



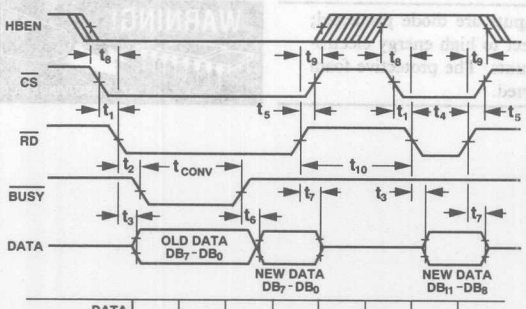
DATA OUTPUTS	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	$D_{3/11}$	$D_{2/10}$	$D_{1/9}$	$D_{0/8}$
READ	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0

Figure 3. Parallel Read Timing Diagram, Slow-Memory Mode (HBEN = LOW)



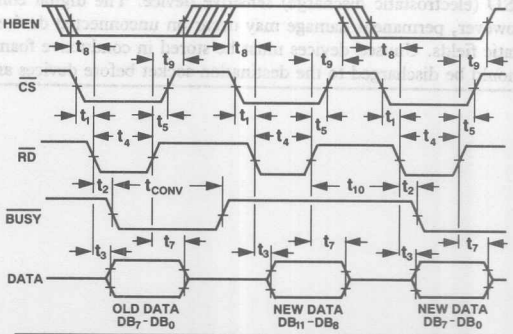
DATA OUTPUTS	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	$D_{3/11}$	$D_{2/10}$	$D_{1/9}$	$D_{0/8}$
FIRST READ (OLD DATA)	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
SECOND READ	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0

Figure 5. Parallel Read Timing Diagram, ROM Mode (HBEN = LOW)



DATA OUTPUTS	D_7	D_6	D_5	D_4	$D_{3/11}$	$D_{2/10}$	$D_{1/9}$	$D_{0/8}$
FIRST READ	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
SECOND READ	LOW	LOW	LOW	LOW	DB_{11}	DB_{10}	DB_9	DB_8

Figure 4. Two-Byte Read Timing Diagram, Slow-Memory Mode



DATA OUTPUTS	D_7	D_6	D_5	D_4	$D_{3/11}$	$D_{2/10}$	$D_{1/9}$	$D_{0/8}$
FIRST READ (OLD DATA)	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
SECOND READ	LOW	LOW	LOW	LOW	DB_{11}	DB_{10}	DB_9	DB_8
THIRD READ	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0

Figure 6. Two-Byte Read Timing Diagram, ROM Mode

V_{DD} to DGND . . . . . −0.3 V to +7 V
V_{SS} to DGND . . . . . +0.3 V to −17 V
V_{REFIN} to DGND . . . . . V_{SS} to V_{DD}
AGND to DGND . . . . . −0.3 V to V_{DD} +0.3 V
A_{IN} to AGND . . . . . −15 V to +15 V
Digital Input Voltage to DGND,
Pins 17, 19–21 . . . . . −0.3 V to V_{DD} +0.3 V
Digital Output Voltage to DGND,
Pins 4–11, 13–16, 18, 22 . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Extended Industrial: ADC912AE/F . . . . . −40°C to +85°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C
Maximum Junction Temperature (T_J max) . . . . . 150°C
Package Power Dissipation . . . . . $(T_J \text{ max} - T_A)/\theta_{JA}$
Thermal Resistance θ_{JA}
Cerdip . . . . . 64°C/W
Plastic DIP . . . . . 57°C/W
SOIC-24 . . . . . 70°C/W

Model	Temperature Range	INL (LSB)	Package Options
ADC912AEW	−40°C to +85°C	±1/2	Cerdip
ADC912AFP	−40°C to +85°C	±1	Plastic DIP
ADC912AFW	−40°C to +85°C	±1	Cerdip
ADC912AFS	−40°C to +85°C	±1	SOIC-24
ADC912AGBC	+25°C	±1	Dice

For devices processed in total compliance to MIL-STD-883, contact our local sales office.

Table I. Analog Input to Digital Output Code Conversion

	Analog Input Voltage		Output Code*	
	0 to +10 V	−10 V to +10 V	DB_{11} (MSB)	DB_0 (LSB)
+FS − 1 LSB	9.9976 V	9.99951 V	1 1 1 1	1 1 1 1	1 1 1 1
+FS − 1 1/2 LSB	9.9964	9.9927	1 1 1 1	1 1 1 1	1 1 1 ϕ
Mid Scale + 1/2 LSB	5.0012	0.0024	1 0 0 0	0 0 0 0	0 0 0 ϕ
Mid Scale	5.0000	0.0000	1 0 0 0	0 0 0 0	0 0 0 0
−FS + 1/2 LSB	0.0012	−9.9976	0 0 0 0	0 0 0 0	0 0 0 ϕ
−FS	0.0000	−10.000	0 0 0 0	0 0 0 0	0 0 0 0

*The symbol "ϕ" indicates a 0 or 1 with equal probability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

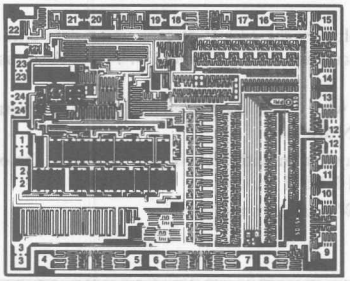


WAFER TEST LIMITS (@ V_{DD} = +10 V, V_{SS} = −12 V or −10 V, V_{REF} = −5 V, A_{IN} = 0 V to +10 V, and T_A = 25°C, unless otherwise noted)

Parameter	Symbol	Conditions	ADC-912AG Limit	Units
Integral Nonlinearity	INL		±1	LSB max
Differential Nonlinearity	DNL		±1	LSB max
Offset Error	V_{ZSE}	Guaranteed by Design	±8	LSB max
Gain Error	G_{FSE}		±8	LSB max
Analog Input Resistance	R_{AIN}		4/6	kΩ min/max
Logic Input High Voltage	V_{INH}	$\overline{CS}$, $\overline{RD}$, HBEN	2.4	V min
Logic Input Low Voltage	V_{INL}	$\overline{CS}$, $\overline{RD}$, HBEN	0.8	V max
Logic Input Current	I_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN	±1	μA max
Logic Output High Voltage	V_{OH}	I_{SOURCE} = 0.2 mA	4	V min
Logic Output Low Voltage	V_{OL}	I_{SINK} = 1.6 mA	0.4	V max
Positive Supply Current	I_{DD}	V_{DD} = +5 V, $\overline{CS}$ = $\overline{RD}$ = V_{DD}, A_{IN} = +10 V	7	mA max
Negative Supply Current	I_{SS}	V_{SS} = −12 V, $\overline{CS}$ = $\overline{RD}$ = V_{DD}, A_{IN} = +10 V	5	mA max

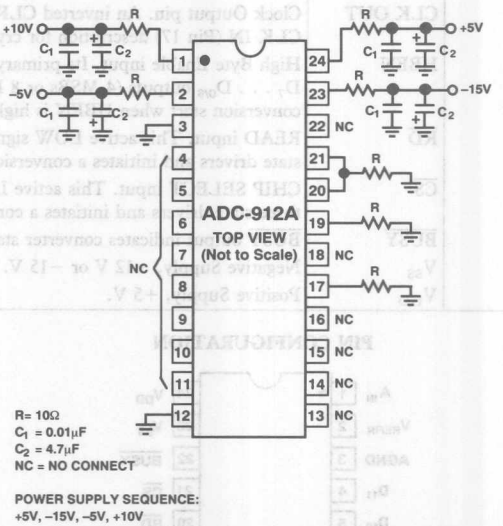
NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

DICE CHARACTERISTICS



Die Size 0.122 × 0.148 inch, 18,056 sq. mils
(3.098 × 3.759 mm, 11.65 sq. mm)

1. A_{IN}
2. V_{REFIN}
3. AGND
4. D_{11}
5. D_{10}
6. D_9
7. D_8
8. D_7
9. D_6
10. D_5
11. D_4
12. DGND
13. $D_{3/11}$
14. $D_{2/10}$
15. $D_{1/9}$
16. $D_{0/8}$
17. CLK IN
18. CLK OUT
19. HBEN
20. $\overline{RD}$
21. $\overline{CS}$
22. $\overline{BUSY}$
23. V_{SS}
24. V_{DD} (Substrate)



Burn-In Circuit

PIN DESCRIPTION

Pin	Mnemonic	Description
1	A_{IN}	Analog Input. 0 to +10 volts.
2	V_{REFIN}	Voltage Reference Input. Requires external −5 V reference.
3	AGND	Analog Ground.
4 . . . 11	D_{11} . . . D_4	Three state data outputs become active when $\overline{CS}$ and $\overline{RD}$ are brought low.
13 . . . 16	$D_{3/11}$ . . . $D_{0/8}$	Individual pin function is dependent upon High Byte Enable (HBEN) input.

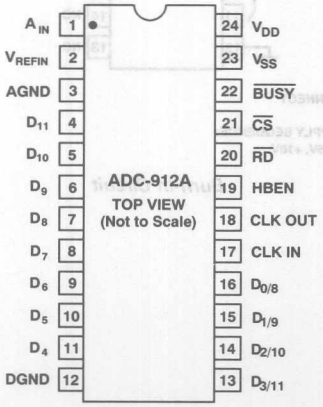
DATA BUS OUTPUT, $\overline{CS}$ & $\overline{RD}$ = LOW

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
Mnemonic*	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	$D_{3/11}$	$D_{2/10}$	$D_{1/9}$	$D_{0/8}$
HBEN = LOW	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
HBEN = HIGH	DB_{11}	DB_{10}	DB_9	DB_8	Low	Low	Low	Low	DB_{11}	DB_{10}	DB_9	DB_8

NOTES
*D_{11} . . . $D_{0/8}$ are the ADC data output pins.
DB_{11} . . . DB_0 are the 12-bit conversion results. DB_{11} is the MSB.

12	DGND	Digital Ground.
17	CLK IN	Clock Input pin. An external TTL compatible clock may be applied to this pin. Alternatively a crystal or ceramic resonator may be connected between CLK IN (Pin 17) and CLK OUT (Pin 18).
18	CLK OUT	Clock Output pin. An inverted CLK IN signal appears at CLK OUT when an external clock is used. See CLK IN (Pin 17) description for crystal (resonator).
19	HBEN	High Byte Enable input. Its primary function is to multiplex the 12-bits of conversion data onto the lower D_7 . . . $D_{0/8}$ outputs (4 MSBs or 8 LSBs). See pin description 4 . . . 11 and 13 . . . 16. Also disables conversion start when HBEN is high.
20	$\overline{RD}$	READ input. This active LOW signal, in conjunction with $\overline{CS}$, is used to enable the output data three-state drivers and initiates a conversion if $\overline{CS}$ and HBEN are low.
21	$\overline{CS}$	CHIP SELECT input. This active LOW signal, in conjunction with $\overline{RD}$, is used to enable the output data three-state drivers and initiates a conversion if $\overline{RD}$ and HBEN are low.
22	$\overline{BUSY}$	$\overline{BUSY}$ output indicates converter status. $\overline{BUSY}$ is LOW during conversion.
23	V_{SS}	Negative Supply, −12 V or −15 V.
24	V_{DD}	Positive Supply, +5 V.

PIN CONFIGURATION



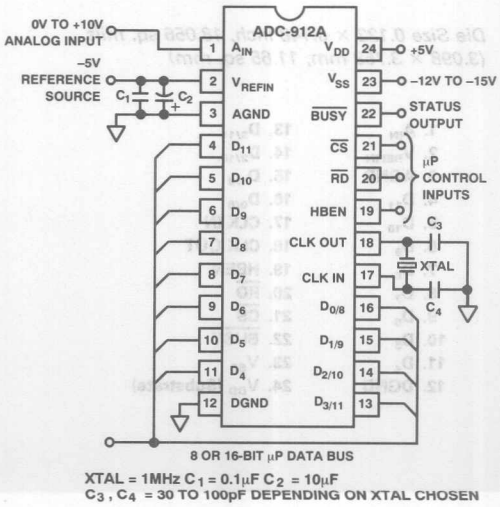
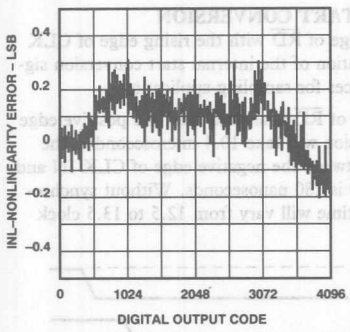
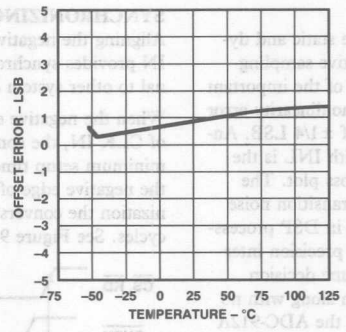


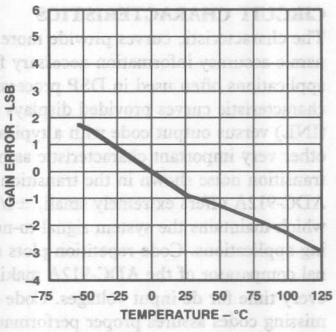
Figure 7. Basic Connection Diagram



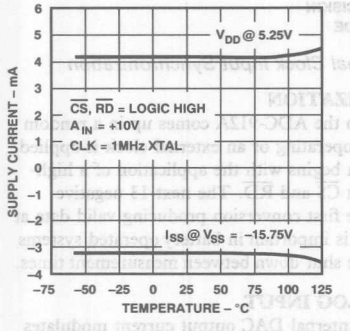
Nonlinearity Error vs. Digital Output Code



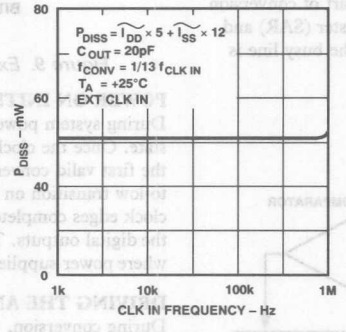
Offset Error vs. Temperature



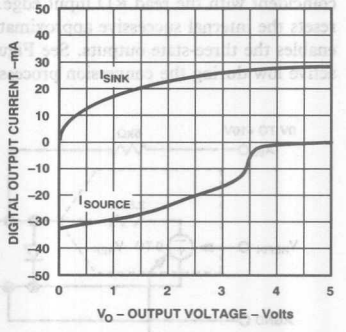
Gain Error vs. Temperature



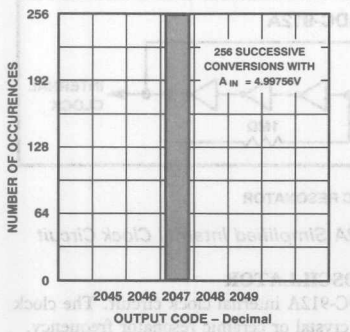
Supply Current vs. Temperature



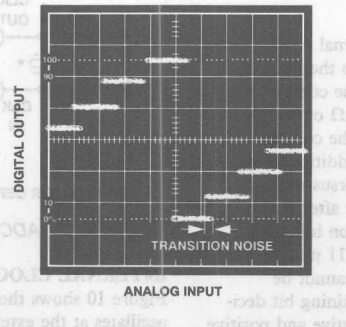
Power Dissipation vs. CLK IN Frequency



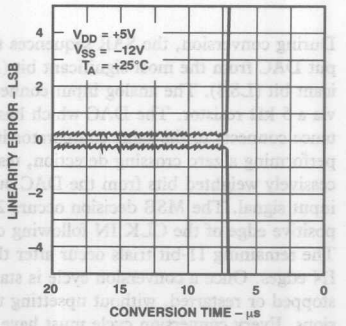
Digital Output Current vs. Output Voltage



Code Repetition



Transition Noise Cross Plot



Linearity Error vs. Conversion Time

CIRCUIT CHARACTERISTICS

The characteristic curves provide more complete static and dynamic accuracy information necessary for repetitive sampling applications often used in DSP processing. One of the important characteristic curves provided displays integral nonlinearity error (INL) versus output code with a typical value of ±1/4 LSB. Another very important characteristic associated with INL is the transition noise shown in the transition noise cross plot. The ADC-912A offers extremely small, ±1/6 LSB, transition noise which maintains the system signal-to-noise ratio in DSP processing applications. Code repetition plots show the precision internal comparator of the ADC-912A making the same decision every time for dc input voltages. Code repetition along with no missing codes assures proper performance when the ADC-912A is used in servo-control systems.

CONVERTER OPERATION DETAILS

The $\overline{CS}$, $\overline{RD}$ and HBEN digital inputs control the start of conversion. A high-to-low on both $\overline{CS}$ and $\overline{RD}$ initiate a conversion sequence. The HBEN high-byte-enable input must be low or coincident with the read $\overline{RD}$ input edge. The start of conversion resets the internal successive approximation register (SAR) and enables the three-state outputs. See Figure 8. The busy line is active low during the conversion process.

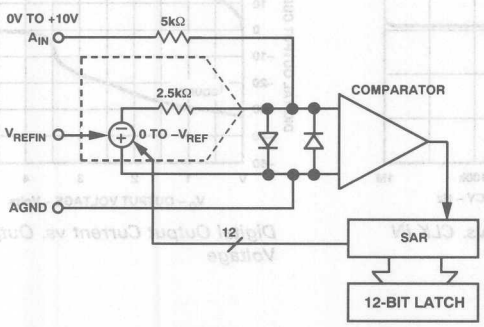


Figure 8. Simplified Analog Input Circuitry of ADC-912A

During conversion, the SAR sequences the internal voltage output DAC from the most significant bit (MSB) to the least significant bit (LSB). The analog input connects to the comparator via a 5 kΩ resistor. The DAC which has a 2.5 kΩ output resistance connects to the same comparator input. The comparator, performing a zero crossing detection, tests the addition of successively weighted bits from the DAC output versus the analog input signal. The MSB decision occurs 200 nsec after the second positive edge of the CLK IN following conversion initiation. The remaining 11-bit trials occur after the next 11 positive CLK IN edges. Once a conversion cycle is started it cannot be stopped or restarted, without upsetting the remaining bit decisions. Every conversion cycle must have 13 negative and positive CLK IN edges. At the end of conversion the comparator input voltage is zero. The SAR contains the 12-bit data word representing the analog input voltage. The $\overline{BUSY}$ line returns to logic high, signaling end of conversion. The SAR transfers the new data to the 12-bit latch.

SYNCHRONIZING START CONVERSION

Aligning the negative edge of $\overline{RD}$ with the rising edge of CLK IN provides synchronization of the internal start conversion signal to other system devices for sampling applications.

When the negative edge of $\overline{RD}$ is aligned with the positive edge of CLK IN, the conversion will take 10.4 microseconds. The minimum setup time between the negative edge of CLK IN and the negative edge of $\overline{RD}$ is 180 nanoseconds. Without synchronization the conversion time will vary from 12.5 to 13.5 clock cycles. See Figure 9.

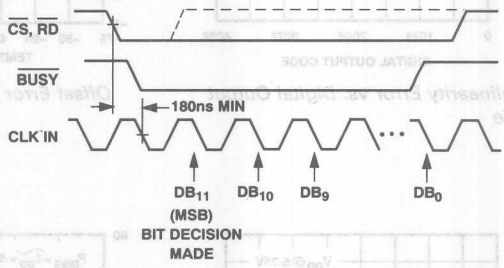


Figure 9. External Clock Input Synchronization

POWER ON INITIALIZATION

During system power-up the ADC-912A comes up in a random state. Once the clock is operating or an external clock is applied, the first valid conversion begins with the application of a high-to-low transition on both $\overline{CS}$ and $\overline{RD}$. The next 13 negative clock edges complete the first conversion producing valid data at the digital outputs. This is important in battery operated systems where power supplies are shut down between measurement times.

DRIVING THE ANALOG INPUT

During conversion, the internal DAC output current modulates the analog input current at the CLK IN frequency of 1.25 MHz. The analog input to the ADC-912A must not change during the conversion process. This requires an external buffer with low output impedance at 1.25 MHz. Suitable devices meeting this requirement include the OP-27, OP-42, and the SMP-11.

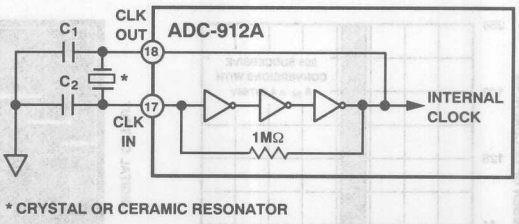


Figure 10. ADC-912A Simplified Internal Clock Circuit

INTERNAL CLOCK OSCILLATOR

Figure 10 shows the ADC-912A internal clock circuit. The clock oscillates at the external crystal or ceramic resonator frequency. The 1.25 MHz crystal or ceramic resonator connects between the CLK IN (Pin 17) and the CLK OUT (Pin 18). Capacitance values (C1, C2) depend on the crystal or ceramic resonator manufacturer. The crystal vendors should be qualified due to variations in C1 and C2 values required from vendor to vendor. Typical values range from 30 pF to 100 pF.

EXTERNAL CLOCK INPUT

A TTL compatible signal connected to CLK IN provides proper converter clock operation. No connection is necessary to the CLK OUT pin. The duty cycle of the external clock input can vary from 45% to 55%. Figure 9 shows the important waveforms.

EXTERNAL REFERENCE

A low output resistance, negative five volt reference is necessary. The external reference should be able to supply 3 mA of reference current. A bypass capacitor is necessary on the reference input lead to minimize system noise as the internal DAC switches. The reference input to the internal DAC is code dependent requiring anywhere from zero to 3 mA. The reference voltage tolerance has a direct influence on A/D converter full-scale voltage, and the maximum input full-scale voltage equals $2 \times -V_{REF}$. The ADC-912A is designed for ratiometric operation, but operation using reference voltages between −5.00 V and 0 V will result in degraded linearity performance. Integral linearity is fully tested and guaranteed for references of −5 V. Figure 11 provides a good negative five volt reference that does not require precision resistors.

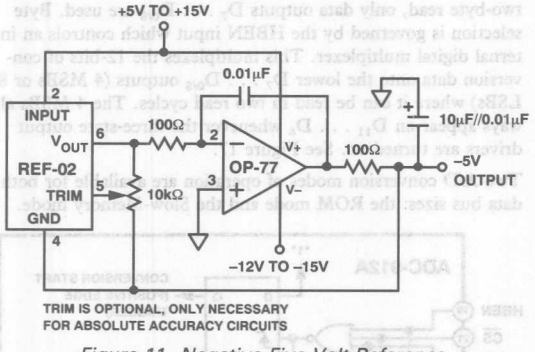


Figure 11. Negative Five Volt Reference

UNIPOLAR ANALOG INPUT OPERATION

Figure 12 shows the ideal input/output characteristic for the 0 V to 10 V input range of the ADC-912A. The designed output-code transitions occur midway between successive integer LSB values (i.e., 0.5 LSB, 1.5 LSBs, 2.5 LSBs . . . FS − 1.5 LSBs). The output code is natural binary with 1 LSB = FS/4096 = (10/4096) V = 2.44 mV. The maximum full-scale input voltage is (10 × 4095/4096) V = 9.9976 V.

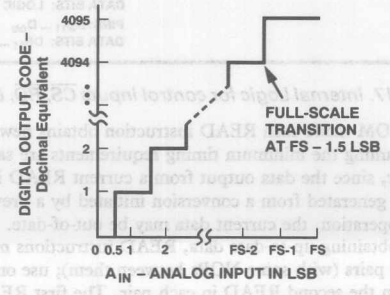


Figure 12. Ideal ADC-912A Input/Output Transfer Characteristic

OFFSET AND FULL-SCALE ERROR ADJUSTMENT, UNIPOLAR OPERATION

For applications where absolute accuracy is important offset and full-scale errors can be adjusted to zero. Figure 13 shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the null offset of the op amp driving A_{IN}.

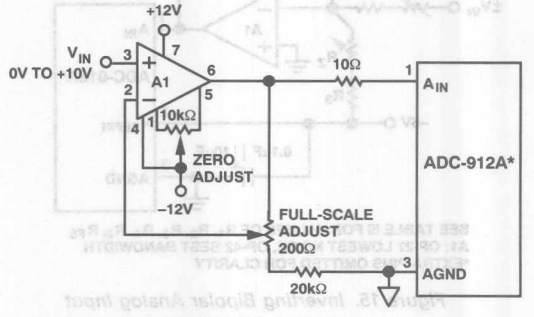


Figure 13. Unipolar 0 V to + 10 V Operation

Adjust the zero scale first by applying 1.22 mV (equivalent to 0.5 LSB input) to V_{IN}. Adjust the op amp offset control until the digital output toggles between 0000 0000 0000 and 0000 0000 0001. The next step is adjustment of full scale. Apply 9.9963 V (equivalent to FS −1.5 LSB) to V_{IN} and adjust R1 until the digital output toggles between 1111 1111 1110 and 1111 1111 1111.

BIPOLAR ANALOG INPUT OPERATION

Bipolar analog input operation is achieved with an external amplifier providing an analog offset. Figures 14 and 15 show two circuit topologies that result in different digital-output coding. In Figure 14, offset binary coding is produced when the external amplifier is connected in the inverting mode. Figure 16 shows the ideal transfer characteristics for both the inverting and non-inverting configurations given in Figures 14 and 15.

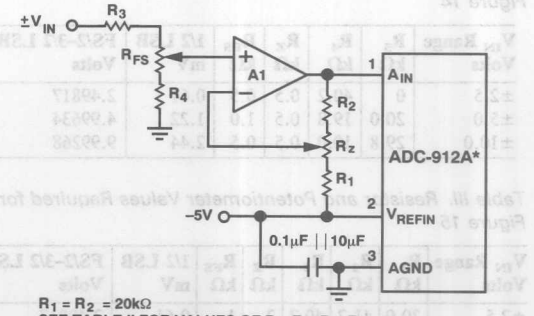


Figure 14. Noninverting Bipolar Analog Input Operation

The scaling resistors chosen in bipolar input applications should be from the same manufacturer to obtain good resistor tracking

performance over temperature. When potentiometers are used for absolute adjustment, 0.1% tolerance resistors should still be used as shown in Figures 14 and 15 to minimize temperature coefficient errors.

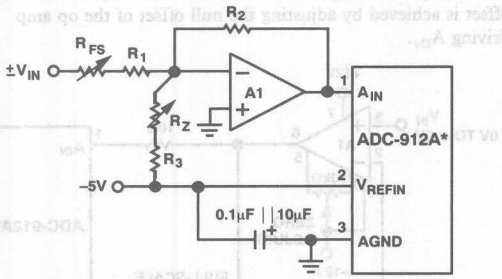


Figure 15. Inverting Bipolar Analog Input

Calibration of the bipolar analog input circuits (Figures 14 and 15) should begin with zero adjustment first. Apply a +1/2 LSB analog input to A_{IN}, (see Tables II and III) and adjust R_Z until the successive digital output codes flicker between the following codes:

For noninverting, Figure 14	1000 0000 0000 1000 0000 0001
For inverting, Figure 15	0111 1111 1111 0111 1111 1110

Next, adjust full scale by applying a FS–3/2 LSB analog input to A_{IN}, (see Tables II and III) and adjust R_{FS} until the successive digital output codes flicker between the following codes:

For noninverting, Figure 14	1111 1111 1110 1111 1111 1111
For inverting, Figure 15	0000 0000 0001 0000 0000 0000

Table II. Resistor and Potentiometer Values Required for Figure 14

V_{IN} Range Volts	R_3 kΩ	R_4 kΩ	R_Z kΩ	R_{FS} kΩ	1/2 LSB mV	FS/2–3/2 LSB Volts
±2.5	0	40.2	0.5	0.5	0.61	2.49817
±5.0	20.0	19.8	0.5	1.0	1.22	4.99634
±10.0	29.8	10.0	0.5	0.5	2.44	9.99268

Table III. Resistor and Potentiometer Values Required for Figure 15

V_{IN} Range Volts	R_1 kΩ	R_2 kΩ	R_3 kΩ	R_Z kΩ	R_{FS} kΩ	1/2 LSB mV	FS/2–3/2 LSB Volts
±2.5	20.0	41.2	40.2	2	1	0.61	2.49817
±5.0	20.0	20.5	20.0	1	1	1.22	4.99634
±10.0	20.0	10.5	10.2	0.5	1	2.44	9.99268

MICROPROCESSOR INTERFACING

The ADC-912A has self-contained logic for both 8-bit and 16-bit

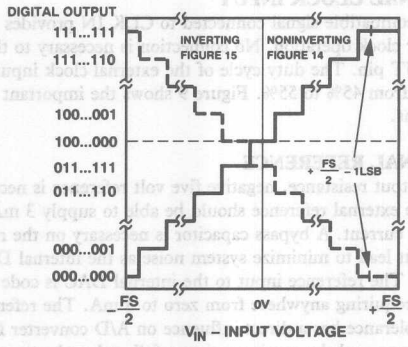


Figure 16. Ideal Input/Output Transfer Characteristics for Bipolar Input Circuits

data bus interfacing. The output data can be formatted into either a 12-bit parallel word for a 16-bit data bus or an 8-bit data word pair for an 8-bit data bus. Data is always right justified, i.e., LSB is the most right-hand bit in a 16-bit word. For a two-byte read, only data outputs $D_7 \ldots D_{0/8}$ are used. Byte selection is governed by the HBEN input which controls an internal digital multiplexer. This multiplexes the 12-bits of conversion data onto the lower $D_7 \ldots D_{0/8}$ outputs (4 MSBs or 8 LSBs) where it can be read in two read cycles. The 4 MSBs always appear on $D_{11} \ldots D_8$ whenever the three-state output drivers are turned on. See Figure 17.

Two A/D conversion modes of operation are available for both data bus sizes: the ROM mode and the Slow-Memory mode.

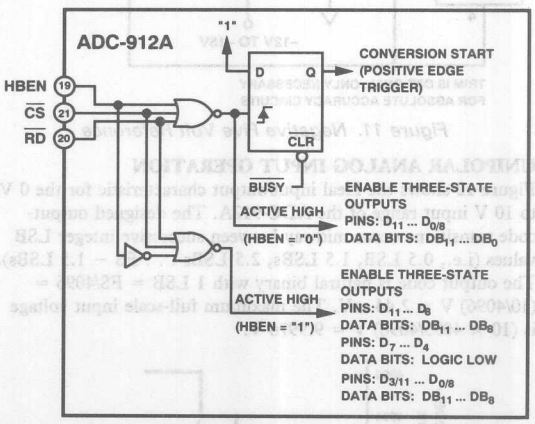


Figure 17. Internal Logic for control Inputs $\overline{CS}$, $\overline{RD}$, & HBEN

In the ROM mode each READ instruction obtains new, valid data assuming the minimum timing requirements are satisfied. However, since the data output from a current READ instruction was generated from a conversion initiated by a previous READ operation, the current data may be out-of-date. To be sure of obtaining up-to-date data, READ instructions may be coded in pairs (with some NOPs between them); use only the data from the second READ in each pair. The first READ starts the conversion, the second READ gets the results.

The Slow-Memory mode is the simplest mode. It is the method of choice where compact coding is essential, or where software bugs are a hazard. In this mode, a single READ instruction will initiate a data conversion, interrupt the microprocessor until completion (WAIT states are introduced), then read the results. If the system throughput tolerates WAIT states, and the hardware is correct, then the Slow-Memory mode is virtually immune to subsequent software modifications. Placing the microprocessor in the WAIT state has an additional advantage of quieting the digital system to reduce noise pickup in the analog conversion circuitry. The 12-bit parallel Slow-Memory mode provides the fastest analog sampling rate combined with digital data transfer rate for sampled-data systems.

PARALLEL READ, SLOW-MEMORY MODE (HBEN = LOW)

Figure 3 shows the timing diagram and data bus status for Parallel Read, Slow-Memory Mode. $\overline{CS}$ and $\overline{RD}$ going low triggers a conversion and the ADC-912A acknowledges by taking $\overline{BUSY}$ low. Data from the previous conversion appears on the three-state data outputs. $\overline{BUSY}$ returns high at the end of conversion, when the output latches have been updated, and the conversion result is placed on data outputs D_{11} . . . $D_{0/8}$.

TWO-BYTE READ, SLOW-MEMORY MODE

For a two-byte read only the 8 data outputs D_7 . . . $D_{0/8}$ are used. Conversion start procedure and data output status for the first read operation is identical to Parallel Read, Slow-Memory Mode. See Figure 4, Timing Diagram and Data Bus Status. At the end of conversion, the low data byte (D_{B7} . . . D_{B0}) is read from the A/D converter. A second READ operation with HBEN high places the high byte on data outputs $D_{3/11}$ . . . $D_{0/8}$ and disables conversion start. Note the 4 MSBs also appear on data outputs D_{11} . . . D_8 during these two READ operations.

PARALLEL READ, ROM MODE (HBEN = LOW)

A conversion is started with a READ operation. The 12 bits of data from the previous conversion are available on data outputs D_{11} . . . $D_{0/8}$ (see Figure 5). This data may be disregarded if not required. A second READ operation reads the new data (DB_{11} . . . DB_0) and starts another conversion. A delay at least as long as the ADC-912A conversion time must be allowed between READ operations. If a READ takes place prior to the end of 13 CLKS of the ADC conversion, the remaining bits not yet tested will be invalid.

TWO-BYTE READ, ROM MODE

For a two-byte read only the data outputs D_7 . . . $D_{0/8}$ are used. Conversion is started in the same way with a READ operation and the data output status is the same as the Parallel Read, ROM Mode. See Figure 6, Two-Byte Read Timing Diagram. Two more READ operations are required to obtain the new conversion result. A delay equal to the ADC-912A conversion time must be allowed between conversion start and places the high byte (4 MSBs) on data outputs $D_{3/11}$ . . . $D_{0/8}$. A third READ operation accesses the low data byte (D_{B7} . . . D_{B0}) and starts another conversion. The 4 MSBs also appear on data outputs D_{11} . . . D_8 during all three read operations above.

CIRCUIT LAYOUT GUIDELINES

As with any high speed A/D converters good circuit layout practice is essential. Wire-wrap boards are not recommended due to stray pickup of the high frequency digital noise. A PC board offers the best results. Digital and analog grounds should be separated even if they are ground planes instead of ground traces. Don't lay digital traces adjacent to high impedance analog traces. Avoid digital layouts that radiate high frequency clock signals, i.e., don't lay out digital signal lines and ground returns in the shape of a loop antenna. Shield the analog input if it comes from a different PC board source. Set up a single point ground at AGND (Pin 3) of the ADC-912A; tie all other analog grounds to this point. Also tie the logic power supply ground, but no other digital grounds, to this point (see Figure 18). Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC. Their trace widths should be as wide as possible. Good power supply bypass capacitors located near the ADC package insures quiet operation. Place a 10 μF capacitor in parallel with a 0.01 μF ceramic capacitor across V_{DD} to ground and V_{SS} to ground (near Pin 3).

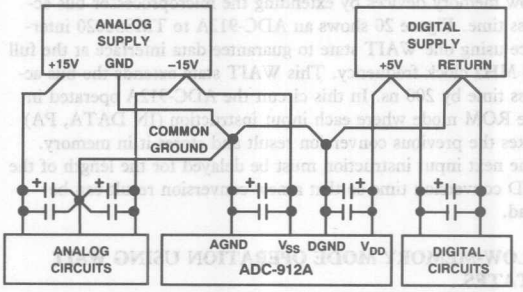


Figure 18. Power Supply Grounding

In applications where the ADC-912A data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get LSB level errors in conversion results. These errors are due to a feedthrough from the microprocessor to the internal comparator. The problem can be minimized by forcing the microprocessor into a WAIT state during conversion (see Slow-Memory microprocessor interfacing). An alternate method is isolation of the data bus with three-state buffers, such as the 74HC541.

INTERFACING TO THE TMS32010 DSP PROCESSOR

Figure 19 shows an ADC-912A to TMS32010 interface. The ADC-912A is operating in the ROM mode. The interface is designed for the maximum TMS32010 clock frequency of 20 MHz.

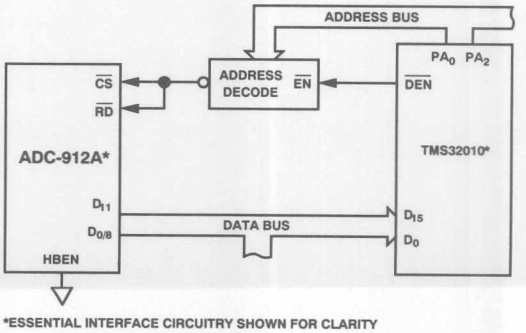


Figure 19. ADC-912A to TMS32010 DSP Processor Interface

The ADC-912A is mapped at a user-selected port address (PA). The following I/O instruction starts a conversion and reads the previous conversion into the data memory:

IN DATA, PA PA = Port Address

DATA = Data Memory Location

When conversion is complete, a second I/O instruction reads the new data into the data memory and starts another conversion. Sufficient A/D conversion time must be allowed between I/O instructions. The very first data read after system power-up should be discarded.

USING WAIT STATES

The TMS32020 DSP processor has the added capability of WAIT states. This feature simplifies the hardware required for slow memory devices by extending the microprocessor bus access time. Figure 20 shows an ADC-912A to TMS32020 interface using one WAIT state to guarantee data interface at the full 20 MHz clock frequency. This WAIT state extends the bus access time by 200 ns. In this circuit the ADC-912A operated in the ROM mode where each input instruction (IN DATA, PA) takes the previous conversion result and stores it in memory. The next input instruction must be delayed for the length of the A/D conversion time so that a new conversion result can be read.

SLOW-MEMORY MODE OPERATION USING WAIT STATES

The WAIT state feature of the TMS32020 can also be used to operate the ADC-912A in the Slow-Memory mode. This is accomplished by driving the clock input of the 7474 flip-flop in Figure 20, from the $\overline{BUSY}$ output of the ADC-912A, instead of the CLK OUT 1 of the TMS32020. Once a conversion has started the READY input of the TMS32020 is not released until the ADC-912A completes its 12-bit A/D conversion. This stops the TMS32020 during the conversion process reducing microprocessor system noise generation. Another advantage for the system software is the single instruction IN MEM, PA used to start, process, and read the results of the A/D conversion. This makes the software code more transportable between systems operating at different clock speeds. The disadvantage is some loss in instruction processing time.

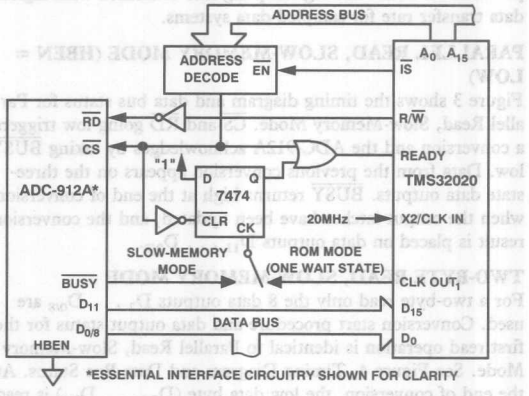


Figure 20. ADC-912A to TMS32020 Interface Using Wait States

Low Cost, 16-Bit Analog-to-Digital Converter

ADC1140

FEATURES

- Guaranteed Nonlinearity: ±0.003% FSR max
- 35μs Maximum Conversion Time
- Small Size 2″ × 2″ × 0.4″
- Wide Power Supply Operation: ±12V to ±17V

APPLICATIONS

- Process Control Data Acquisition
- Seismic Data Acquisition
- Nuclear Instrumentation
- Medical Instrumentation
- Pulse Code Modulation Telemetry
- Industrial Scales
- Robotics

GENERAL DESCRIPTION

The ADC1140 is a low cost 16-bit successive-approximation analog-to-digital converter having a 35μs maximum conversion time. This converter provides high accuracy, high stability and low power consumption all in a 2″ × 2″ × 0.4″ module.

High accuracy performance such as integral and differential nonlinearity of ±0.003% FSR max are both guaranteed. Guaranteed stability such as differential nonlinearity TC of ±2ppm/°C maximum, offset TC of ±30μV/°C maximum, gain TC of ±12ppm/°C maximum and power supply sensitivity of ±0.002% of FSR/% V_S are also provided by the ADC1140.

The ADC1140 makes extensive use of both integrated circuit and thin-film components to obtain excellent performance, small size and low cost. The internal 16-bit DAC incorporates Analog Devices' proprietary thin-film resistor technology and proprietary CMOS current-steering switches. A low noise reference, low power comparator and low power successive-approximation register are also used to optimize the ADC1140's design (shown in Figure 1).

FUNCTIONAL BLOCK DIAGRAM

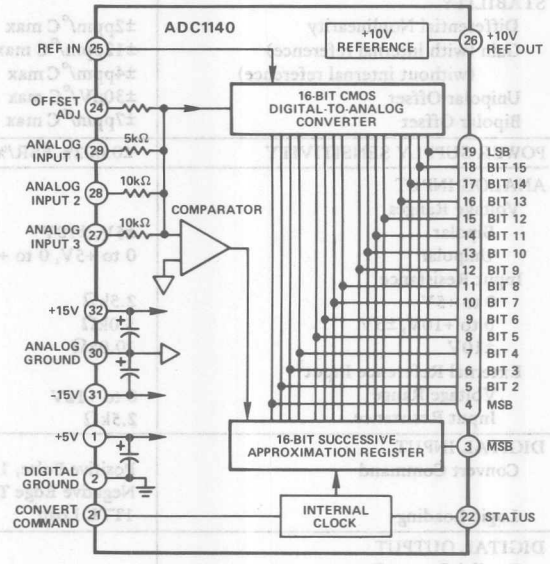


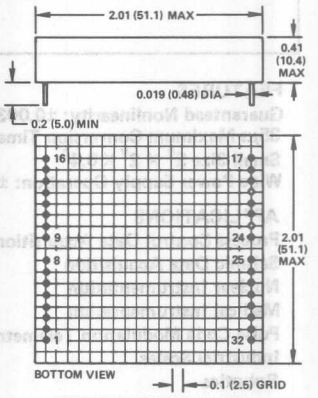
Figure 1.

The ADC1140 can operate with power supplies ranging from ±12V to ±17V and has provisions for a user supplied external reference. Four analog input voltage ranges are selectable via pin programming: ±5V, ±10V, 0 to +5V and 0 to +10V. Bipolar coding is provided in the offset binary and two's complement formats with unipolar coding displayed in true binary.

RESOLUTION	16 Bits
CONVERSION TIME	35μs max
ACCURACY[1]	
Nonlinearity Error	±0.003% FSR[2] max
Differential Nonlinearity Error	±0.003% FSR[2] max
STABILITY	
Differential Nonlinearity	±2ppm/°C max
Gain (with internal reference)	±12ppm/°C max
(without internal reference)	±4ppm/°C max
Unipolar Offset	±30μV/°C max
Bipolar Offset	±7ppm/°C max
POWER SUPPLY SENSITIVITY	±0.002% FSR/% V_S
ANALOG INPUT	
Voltage Ranges	
Bipolar	±5V, ±10V
Unipolar	0 to +5V, 0 to +10V
Input Resistance	
0 to +5V	2.5kΩ
0 to +10V, ±5V	5.0kΩ
±10V	10.0kΩ
External Reference Input[3]	
Voltage Range	0 to +12V
Input Resistance	2.5kΩ
DIGITAL INPUT	
Convert Command	Positive Pulse, 100ns Width min Negative Edge Triggered
Logic Loading	1TTL Load
DIGITAL OUTPUT	
Parallel Output Data	
Unipolar	Binary (BIN)
Bipolar	Offset Binary (OBIN) Two's Complement
Output Drive	1TTL Load
Status	Logic "1" During Conversion
Output Drive	1TTL Load
INTERNAL REFERENCE VOLTAGE	+10V, ±0.3%
External Load Current	
(Rated Performance)	2mA max
Temperature Stability	±8.5ppm/°C max
POWER REQUIREMENTS[4]	
Voltage (Rated Performance)	±15V ±3%, +5V ±3%
Voltage (Operating)	±12V to ±17V, +4.75V to +5.25V
Supply Current Drain ±15V	±25mA
+5V	150mA
TEMPERATURE RANGE	
Specified	0 to +70°C
Operating	−25°C to +85°C
Storage	−55°C to +85°C
SIZE	2" X 2" X 0.4" (51 X 51 X 10.4mm)
Weight	1.2 oz (33g)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS.

MATING CONNECTORS

AC1577 (2 REQUIRED)

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	+5V	32	+15V
2	DIGITAL GROUND	31	-15V
3	MSB	30	ANALOG GROUND
4	MSB	29	ANALOG IN 1
5	BIT 2	28	ANALOG IN 2
6	BIT 3	27	ANALOG IN 3
7	BIT 4	26	+10V REF OUT
8	BIT 5	25	REFERENCE IN
9	BIT 6	24	OFFSET ADJUST
10	BIT 7	23	NOT USED
11	BIT 8	22	STATUS
12	BIT 9	21	CONVERT COMMAND
13	BIT 10	20	NOT USED
14	BIT 11	19	LSB
15	BIT 12	18	BIT 15
16	BIT 13	17	BIT 14

NOTES

[1] Offset and gain error are adjustable to zero by means of external potentiometers. See Figure 3 for proper connection.

[2] FSR means Full Scale Range.

[3] Rated performance is specified with +10.0V reference.

[4] Recommended Power Supply: Analog Devices Model 923.

Specifications subject to change without notice.

OPERATION

For operation, the only connections to the ADC1140 that are necessary are the power supplies, internal or external reference, input voltage pin programming, convert command and digital output. Refer to Table I for input pin programming and Figure 3 for offset and gain calibration.

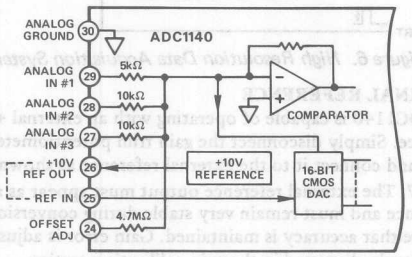


Figure 2. Analog Input Block Diagram

ANALOG INPUT PROGRAMMING

The analog input section consists of three analog input terminals. Analog input range selection is accomplished by pin programming as shown in Table I.

In the unipolar mode, a 0 to +10V or a 0 to +5V input signal develops a 0 to +2mA current that is compared to the 0 to –2mA (shown in Figure 2) current output of the DAC.

In the bipolar mode, a +1mA offset current from the reference is applied to the comparator input via pin programming connections. The ADC1140 can then accept either ±5V or ±10V inputs. These inputs again will be converted to current and compared with the DAC's 0 to –2mA current output.

Table I. Analog Input Voltage Pin Programming

Input Signal Range	Coding	Connect Input Signal To Pin(s)	Connect Pin 26 To Pin*	Connect Pin 30 To Pin(s)
±10V	OBIN, Two's Comp	28	27	29, 2
±5V	OBIN, Two's Comp	29	27	28, 2
0 to +5V	BIN	27, 28, 29	Open	2
0 to +10V	BIN	27, 28	Open	29, 2

*If Internal Reference is used, Pins 25 and 26 must be connected together through a 50Ω potentiometer or 24.9Ω fixed resistor (see Figure 3 and the gain calibration section).

OPTION OFFSET & GAIN CALIBRATION

Initial offset and gain errors can be adjusted to zero by potentiometers as shown in Figure 3. Proper offset and gain calibration requires great care and the use of an accurate and stable voltage reference. The voltage standard used as a signal source must be very stable. It should be capable of being set to within 1μV of the desired value at both ends of its range. The potentiometers selected should be of the good quality Cermet type. Multi-turn potentiometers having ten to fifteen turns and 100ppm/°C temperature coefficients will be adequate. The temperature coefficients contributed by these Cermet potentiometers will be less than 0.1ppm/°C.

By adjusting the offset first, gain and offset adjustments will remain independent of each other.

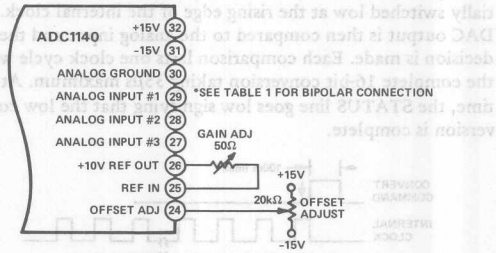


Figure 3. Offset and Gain Calibration

OFFSET CALIBRATION

For 0 to +10V range, set the input voltage precisely to +76μV; for 0 to +5V range, set it at +38μV. Adjust the zero potentiometer until the binary coded converter is just on the verge of switching from 000 . . . 00 to 000 . . . 01.

For ±5V range, set the input voltage precisely to –4.999924V; for ±10V range, set it at –9.999847V. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 000 . . . 00 to 000 . . . 01 and the two's comp. coded units are just on the verge of switching from 100 . . . 0 to 100 . . . 1.

GAIN CALIBRATION

Set the input voltage precisely at +9.99977V for 0 to +10V input range, +4.99977V for ±5V input range, +9.99954V for ±10V input range, or +4.99988V for 0 to +5V input range, adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 111 . . . 0 to 111 . . . 1 and two's comp. coded units are just on the verge of switching from 011 . . . 10 to 011 . . . 11. Note that these values are 1 1/2 LSBs less than nominal full scale.

POWER SUPPLY AND GROUNDING CONNECTIONS

The analog power ground (pin 30) and digital ground (pin 2) are not connected internally. The connection must be made externally. The choice of an optimum "star" point is an important consideration in avoiding ground loops and to minimize coupling between the analog and digital sections. One suggested approach is shown in Figure 4.

Because the ADC1140 contains high quality tantalum capacitors on each of the power supply inputs to ground, external bypass capacitors are not required.

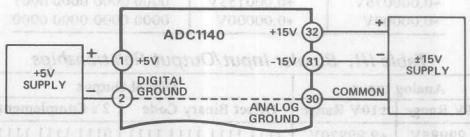


Figure 4. Power Supply and Grounding Techniques

ADC1140 TIMING

Conversion is initiated with the negative going edge of the Convert Command pulse as shown in Figure 5. The Convert Command pulse width must be a minimum of 100ns. Once the conversion process is initiated, it cannot be retriggered until after the end of conversion.

With the negative edge of the Convert Command pulse, all internal logic is reset. The MSB is set low with the remaining digitial outputs set to logic high state, and the status line is set high and remains high thru the full conversion cycle.

During conversion each bit, starting with the MSB, is sequentially switched low at the rising edge of the internal clock. The DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 16-bit conversion taking 35μs maximum. At this time, the STATUS line goes low signifying that the low conversion is complete.

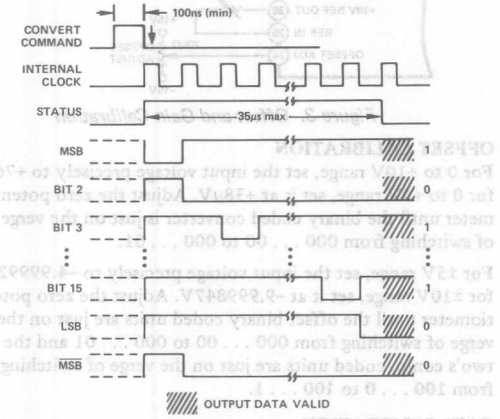


Figure 5. ADC1140 Timing Diagram

ANALOG INPUT/OUTPUT RELATIONSHIPS

The ADC1140 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two's complement output codes. The most significant bit (MSB) is displayed on pin 4 for the binary and offset binary codes or on pin 3 for the two's complement code. Table II shows the unipolar analog input/digital output relationships. Table III shows the bipolar analog input/digital output relationships for offset binary code and two's complement codes.

Table II. Unipolar Input/Output Relationships

Analog Input		Digital Output
0 to +5V Range	0 to +10V Range	Binary Code
+4.999924V	+9.99985V	1111 1111 1111 1111
+2.50000V	+5.00000V	1000 0000 0000 0000
+1.25000V	+2.50000V	0100 0000 0000 0000
+0.62500V	+1.25000V	0010 0000 0000 0000
+0.000076V	+0.000153V	0000 0000 0000 0001
+0.00000V	+0.00000V	0000 0000 0000 0000

Table III. Bipolar Input/Output Relationships

Analog Input		Digital Output	
±5V Range	±10V Range	Offset Binary Code	2's Complement Code
+4.99985V	+9.99970V	1111 1111 1111 1111	0111 1111 1111 1111
+2.50000V	+5.00000V	1100 0000 0000 0000	0100 0000 0000 0000
+0.000153V	+0.000305V	1000 0000 0000 0001	0000 0000 0000 0001
+0.00000V	+0.00000V	1000 0000 0000 0000	0000 0000 0000 0000
-5.00000V	-10.00000V	0000 0000 0000 0000	1000 0000 0000 0000

HIGH RESOLUTION DATA ACQUISITION SYSTEM

Shown in Figure 6 is a high resolution data acquisition system. Here the SHA1144, a high resolution sample-hold amplifier, is used to drive the ADC1140. Conversion is initiated by the negative edge of the convert command pulse. At this time the STATUS pulse goes low causing the SHA1144 to go from the sample mode to the hold mode. When the conversion is complete, 35μs later, the STATUS pulse goes low, thus placing the SHA1144 in the sample mode.

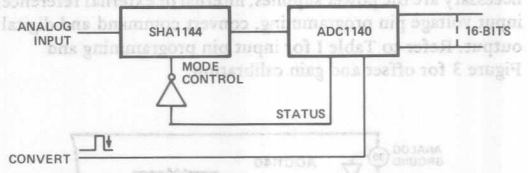


Figure 6. High Resolution Data Acquisition System

EXTERNAL REFERENCE

The ADC1140 is capable of operating with an external +10.0V reference. Simply disconnect the gain trim potentiometer from pin 26 and connect it to the external reference as shown in Figure 7. The external reference output must appear as a low impedance and must remain very stable during conversion to insure that accuracy is maintained. Gain error is adjusted as previously discussed in the gain calibration section.

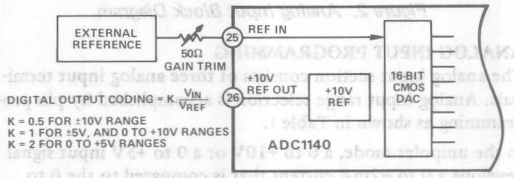


Figure 7. External Reference

The ADC1140 is factory tested and calibrated with the internal +10.0V reference voltage but nonstandard external voltages can be used with the digital output coding being determined by the formula shown in Figure 7.

PIA INTERFACE

The ADC1140 can be used with a PIA to interface directly to a microprocessor. As shown in Figure 8 the 16-bit output of the ADC1140 is split into two 8-bit bytes. Part A of the PIA is programmed to read the eight most-significant-bits while Part B reads the eight least-significant-bits. Output CB2 is used to start the ADC1140 conversion process. CB1, of the PIA, is used to sense the STATUS of the ADC1140 so that the end of conversions can be determined. The control bus, address bus, and data bus are then connected directly to the microprocessor.

With the use of PIAs, control of one or more ADC1140s can be accomplished in many different configurations.

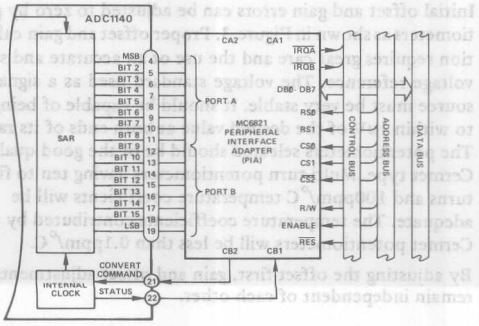


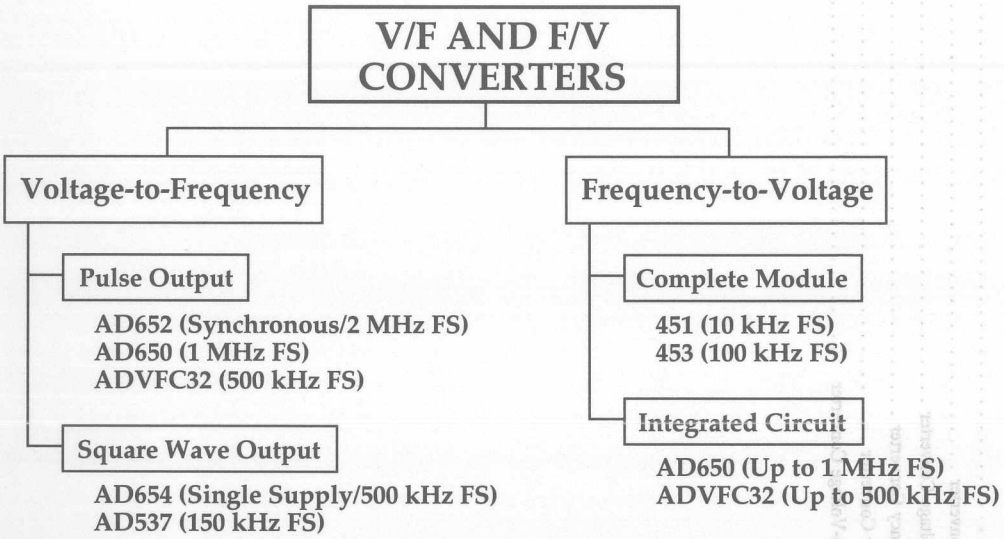
Figure 8. ADC1140 Interface to PIA

V/F & F/V Converters
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3

Selection Tree
V/F & F/V Converters



Selection Guide
V/F and F/V Converters

Voltage-to-Frequency Converters

Model	Full-Scale Frequency MHz	Linearity % max	FS Calib Error % typ	Output Format	Input Range V	Package Options[1]	Temp Range[2]	Page	Comments
AD652	**2**	**0.005–0.05**	**0.25–0.5**	**Pulse Train**	**0 to 10, ±5 0 to −10**	**3, 4, 5**	**C, I, M**	**C II 3–27**	**Synchronous, Multiple Input Ranges, Low Linearity, Single Supply**
AD650	**1**	**0.005–0.1**	**5–10**	**Pulse Train**	**0 to 10, ±5 0 to −10**	**1, 2, 5**	**C, I, M**	**C II 3–15**	**Low Nonlinearity, Multiple Input Ranges**
AD654	**0.5**	**0.1–0.4**	**10**	**Square Wave**	**0 to (V_S)**	**2, 6**	**C**	**C II 3–43**	**Single Supply, Low Cost**
ADVFC32	0.5	0.01–0.2	5	Pulse Train	0 to 10	2, 7	C, I, M	C II 3–51	Industry Standard
AD537	0.15	0.07–0.25	5	Square Wave	$-V_S$ to $(+V_S -4)$	1, 7	C, M	C II 3–7	Single Supply, Military Grade

Frequency-to-Voltage Converters

Model	Input Range kHz	Linearity % max	Response Time ms typ	Package Options[1]	Temp Range[2]	Page	Comments
451	0 to 10	0.03–0.008	4	Module	I	C I 11–4, C II 12–4	Complete, No External Components
453	0 to 100	0.03–0.008	0.8	Module	I	C I 11–4, C II 12–4	Complete, No External Components
AD650	**0 to 1000**	**0.005–0.1**	–	**1, 2, 5**	**C, I, M**	**C II 3–15**	**Low Nonlinearity**
ADVFC32	0 to 500	0.01–0.2	–	2, 7	C, I, M	C II 3–51	Industry Standard

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-In-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92.
[2]Temperature Ranges: C = Commercial, 0 to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.

Orientation
V/F & F/V Converters

VOLTAGE-TO-FREQUENCY CONVERTERS

Voltage-to-frequency converters (VFCs) convert analog voltage or current levels to pulse trains or square waves in a logic-compatible form (usually TTL) at frequencies that are accurately proportional to the analog quantity. The output continuously tracks the input signal, responding directly to changes in the input signal; external clock synchronization is not required. V/F converters find applications in analog-to-digital converters with high resolution, long-term high-precision integrators, two-wire high-noise-immunity digital transmission and digital voltmeters.

FREQUENCY-TO-VOLTAGE CONVERTERS

Frequency-to-voltage converters (FVCs) perform the inverse operation; they accept a wide variety of periodic waveforms and produce an analog output proportional to frequency. Combining adjustable threshold, gain and output offset with low linearity error, F/V converters offer economical solutions to a wide variety of applications where it is required to convert frequency to an analog voltage. Examples are motor-speed controllers, power-line frequency monitors and VCO stabilization circuits. In analog-to-analog data transmission, they convert serially transmitted data in the form of pulse streams back to analog voltage.

Applications of both forms of conversion, as appropriate to specific device types, are illustrated with varying degrees of detail on the individual data sheets.

FACTORS IN CHOOSING VFCs AND FVCs

The charge-balance and the astable-multivibrator type architectures are two design techniques used to implement the voltage-to-frequency function. The output of a charge balance VFC is a train of pulses of constant width and height, with very low duty cycles for small analog inputs. An astable-multivibrator VFC produces a square wave for its output.

The charge-balance converter architecture used for the AD650 is shown in Figure 1. It comprises a summing integrator, a current source and steering switch, a comparator, a one-shot, and an output transistor. The input signal current may be provided directly by a current source or be generated by an input voltage across R_{IN}. This current is *exactly* balanced by an internal feedback current delivered in the form of precision pulses from the switched 1 mA internal current source. These current pulses can be thought of as precisely defined packets of charge. The required number of charge packets, each producing one pulse at the output transistor, depends upon the amplitude of the input current signal. Since the number of charge packets delivered per unit time to the summing junction is related to the input signal current amplitude by a linear function, the voltage-to-frequency transformation is achieved.

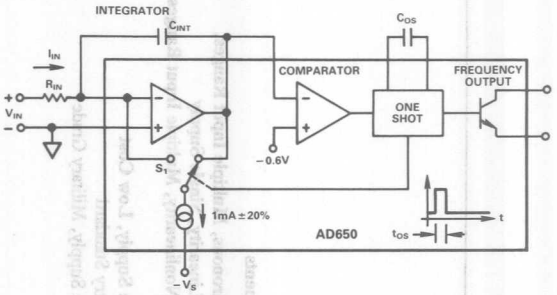


Figure 1. Block Diagram of the AD650

This architecture allows for a full-scale frequency up to 1MHz and can achieve linearity errors as low as 0.005%. Excellent noise rejection is achieved since the charge balance architecture is performing a continuous integration on the input signal. Also, it has a dynamic range of up to six decades allowing for extremely high resolution measurements. A F-V conversion may be easily implemented with this architecture. Full-scale frequency, gain error, and linearity are significantly determined by the stability, accuracy, and proper selection of the one-shot capacitor and R_{IN}.

A variation of this architecture known as a synchronous voltage-to-frequency converter is used on the AD652 shown in Figure 2. This modified charge-balance type architecture uses an external clock to define the full-scale output frequency, rather than depend on the stability of an external one-shot capacitor, therefore improving upon the temperature drift specifications. It is capable of producing a 2 MHz full-scale output and can achieve linearity errors as low as 0.002%. Also, by referencing the comparator and analog input to an on-chip 5 volt reference, the device may operate single supply.

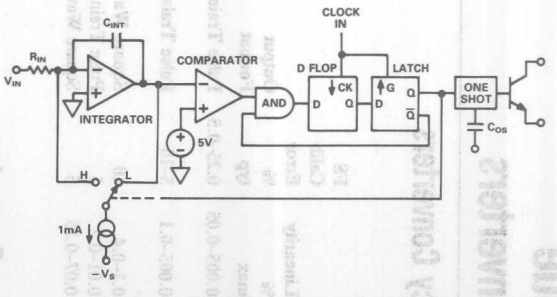


Figure 2. Block Diagram of the AD652

The astable-multivibrator architecture used on the AD654 and the AD537 is shown in Figure 3. It uses a current controlled precision multivibrator as the primary timing element. An operational amplifier converts the input voltage into a proportional unipolar current which drives the multivibrator circuit and timing capacitor through n-p-n transistors. This current determines the charging and discharging rate of the timing capacitor which in turn determines the frequency of operation of the multivibrator circuit. The frequency output is a square wave delivered via an open-collector n-p-n transistor whose emitter is returned to digital ground for high noise immunity against digital spikes.

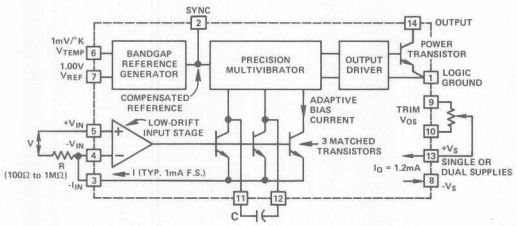


Figure 3. Block Diagram of the AD537

The power consumption of a multivibrator VFC can be very low: for example, the AD654 can operate on single supply voltages as low as 4.5 volts and consume a maximum of 3.0 mA quiescent current. The device can operate with a full-scale frequency up to 500 kHz and achieve voltage-to-frequency nonlinearity as low as 0.03%. Also, the square wave output allows it to be ac coupled without introducing dc level shifts with a change in frequency.

The frequency-to-voltage conversion may be easily implemented with the charge-balance VFCs such as the AD650 by reconfiguring it and by adding a simple logic biasing network. The device may convert frequencies up to 1 MHz to full-scale output voltages up to 10 volts. The AD652 synchronous VFC may also be configured for this function when an application requires a higher degree of linearity. The AD537 and AD654 may also be used in a F-V converter application as the oscillator in a phase locked loop when used in conjunction with a quad nand gate which serves as a phase comparator.

SPECIFICATIONS

The salient specifications for VFCs are *(non)linearity*, as a percentage of full-scale frequency; *frequency range*, the greater the frequency range, the greater the resolution for a given counting period; *full-scale-calibration error; gain-temperature coefficient*, in ppm of signal per °C, where "gain" is the ratio of full-scale frequency to full-scale voltage; *input-offset temperature coefficient; overrange capability*, within rated specifications, and *step response*, the worst-case time interval required for the frequency to respond to a full-scale-step input change.

For FVCs, important specs, in addition to accuracy specs corresponding to the above, include *output ripple* (for specified input frequencies), *threshold* (for recognition that another cycle has been initiated and for versatility in interfacing various types of sensors directly), *hysteresis* (to provide a degree of insensitivity to noise superimposed on a slowly-varying input waveform) and *dynamic response* (important in motor control).

Definitions of some critical specifications, and the conditions for adjusting or measuring them, are detailed on individual data sheets.

Integrated Circuit Voltage-to-Frequency Converter

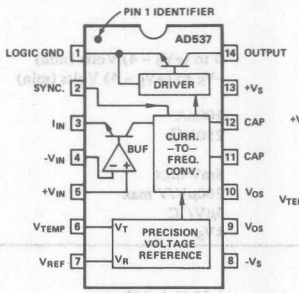
AD537*

FEATURES

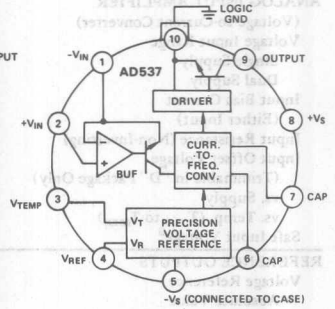
- Low Cost A-D Conversion
- Versatile Input Amplifier
  - Positive or Negative Voltage Modes
  - Negative Current Mode
  - High Input Impedance, Low Drift
- Single Supply, 5 to 36 Volts
- Linearity: ±0.05% FS
- Low Power: 1.2mA Quiescent Current
- Full Scale Frequency up to 100kHz
- 1.00 Volt Reference
- Thermometer Output (1mV/K)
- F-V Applications
- F-V Applications
- MIL-STD-883 Compliant Versions Available

PIN CONFIGURATIONS

"D" Package – TO-116



"H" Package – TO-100



PRODUCT DESCRIPTION

The AD537 is a monolithic V-F converter consisting of an input amplifier, a precision oscillator system, an accurate internal reference generator and a high current output stage. Only a single external RC network is required to set up any full scale (F.S.) frequency up to 100kHz and any F.S. input voltage up to ±30V. Linearity error is as low as ±0.05% for 10kHz F.S., and operation is guaranteed over an 80dB dynamic range. The overall temperature coefficient (excluding the effects of external components) is typically ±30ppm/°C. The AD537 operates from a single supply of 5 to 36V and consumes only 1.2mA quiescent current.

A temperature-proportional output, scaled to 1.00mV/K, enables the circuit to be used as a reliable temperature-to-frequency converter; in combination with the fixed reference output of 1.00V, offset scales such as 0°C or 0°F can be generated.

The low drift (1μV/°C typ) input amplifier allows operation directly from small signals (e.g., thermocouples or strain gages) while offering a high (250MΩ) input resistance. Unlike most V-F converters, the AD537 provides a square-wave output, and can drive up to 12 TTL loads, LEDs, very long cables, etc.

The excellent temperature characteristics and long-term stability of the AD537 are guaranteed by the primary band-gap reference generator and the low T.C. silicon chromium thin film resistors used throughout.

The device is available in either a TO-116 ceramic DIP or a TO-100 metal can; both are hermetically sealed packages.

The AD537 is available in three performance/temperature grades; the J and K grades are specified for operation over the 0 to +70°C range while the AD537S is specified for operation over the extended temperature range, -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD537 is a complete V-F converter requiring only an external RC timing network to set the desired full scale frequency and a selectable pull-up resistor for the open-collector output stage. Any full-scale input voltage range from 100mV to 10 volts (or greater, depending on $+V_S$) can be accommodated by proper selection of timing resistor. The full scale frequency is then set by the timing capacitor from the simple relationship, f = V/10RC.
2. The power supply requirements are minimal, only 1.2mA quiescent current is drawn from a single positive supply from 4.5 to 36 volts. In this mode, positive inputs can vary from 0 volts (ground) to ($+V_S$ - 4) volts. Negative inputs can easily be connected for below ground operation.
3. F-V converters with excellent characteristic are also easy to build by connecting the AD537 in a phase-locked loop. Application particulars are shown in Figure 6.
4. The versatile open-collector NPN output stage can sink up to 20mA with a saturation voltage less than 0.4 volts. The Logic Common terminal can be connected to any level between ground (or $-V_S$) and 4 volts below $+V_S$. This allows easy direct interface to any logic family with either positive or negative logic levels.
5. The AD537 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Product Databook or current AD537/883B data sheet for detailed specifications.

*Protected by Patent Nos. 3,887,963 and RE 30,586.

AD537—SPECIFICATIONS (typical @ +25°C with V_S (total) = 5 to 36V, unless otherwise noted.)

MODEL	AD537JH	AD537JD	AD537KD AD537KH	AD537SD[1] AD537SH[1]
CURRENT-TO-FREQUENCY CONVERTER				
Frequency Range	0 to 150kHz	*	*	*
Nonlinearity[1]				
f_{max} = 10kHz	0.15% max (0.1% typ)	*	0.07% max	**
f_{max} = 100kHz	0.25% max (0.15% typ)	*	0.1% max	**
Full Scale Calibration Error				
C = 0.01μF, I_{IN} = 1.000mA	±10% max	±7% max	±5% max	**
vs. Supply (f_{max} < 100kHz)	±0.1%/V max (0.01% typ)	*	*	*
vs. Temp. (T_{min} to T_{max})	±150ppm/°C max (50ppm typ)	*	50ppm/°C max (30ppm typ)[2]	150ppm/°C max
ANALOG INPUT AMPLIFIER				
(Voltage-to-Current Converter)				
Voltage Input Range				
Single Supply	0 to (+V_S – 4) Volts (min)	*	*	*
Dual Supply	–V_S to (+V_S – 4) Volts (min)	*	*	*
Input Bias Current				
(Either Input)	100nA	*	*	*
Input Resistance (Non-Inverting)	250MΩ	*	*	*
Input Offset Voltage				
(Trimmable in "D" Package Only)	5mV max	*	2mV max	**
vs. Supply	200μV/V max	100μV/V max	100μV/V max	**
vs. Temp. (T_{min} to T_{max})	5μV/°C	*	1μV/°C	10μV/°C max
Safe Input Voltage[3]	±V_S	*	*	*
REFERENCE OUTPUTS				
Voltage Reference				
Absolute Value	1.00 Volt ±5% max	*	*	*
vs. Temp. (T_{min} to T_{max})	50ppm/°C	*	100ppm/°C max	**
vs. Supply	±0.03%/V max	*	*	*
Output Resistance[4]	380Ω	*	*	*
Absolute Temperature Reference[5]				
Nominal Output Level	1.00mV/K	*	*	*
Initial Calibration @ +25°C	298mV (±5mV)	*	298mV (±5mV max)	**
Slope Error from 1.00mV/K	±0.02mV/K	*	*	*
Slope Nonlinearity	±0.1K	*	*	*
Output Resistance[5]	900Ω	*	*	*
OUTPUT INTERFACE (Open Collector Output)				
(Symmetrical Square Wave)				
Output Sink Current in Logic "0"				
V_{OUT} = 0.4V max, T_{min} to T_{max})	20mA min	20mA min	20mA min	10mA min
Output Leakage Current in Logic "1"				
(T_{min} to T_{max})	200nA max	*	*	2μA max
Logic Common Level Range	–V_S to (+V_S – 4) Volts	*	*	*
Rise/Fall Times (C_T = 0.01μF)				
I_{IN} = 1mA	0.2μs	*	*	*
I_{IN} = 1μA	1μs	*	*	*
POWER SUPPLY				
Voltage, Rated Performance				
Single Supply	4.5V to 36V	*	*	*
Dual Supply	±5 to ±18V	*	*	*
Quiescent Current	1.2mA (2.5mA max)	*	*	*
TEMPERATURE RANGE				
Rated Performance	0 to +70°C	*	*	–55°C to +125°C
Storage	–65°C to +150°C	*	*	*
PACKAGE OPTIONS[6,7]				
TO-116 Ceramic DIP (D-14)		AD537JD	AD537KD	AD537SD
TO-100 Header (H-10A)	AD537JH		AD537KH	AD537SH

NOTES

*Specifications same as AD537JH.

**Specifications same as AD537K.

Specifications subject to change without notice.

[1] Nonlinearity is specified for a current input level (I_{IN}) to the converter from 0.1 to 1000μA. Converter has 100% overrange capability up to I_{IN} = 2000μA with slightly reduced linearity. Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a percentage of full scale.

[2] Guaranteed not tested.

[3] Maximum voltage input level is equal to the supply on either input terminal. However, large negative voltage levels can be applied to the negative terminal if the input is scaled to a nominal 1mA full scale through an appropriate value resistor (see Figure 2).

[4] Loading the 1.0 volt or 1mV/K outputs can cause a significant change in overall circuit performance, as indicated in the applications section. To maintain normal operation, these outputs should be operated into the external buffer or an external amplifier.

[5] Temperature reference output performance is specified from 0 to +70°C for "J" and "K" devices, –55°C to +125°C for "S" model.

[6] D = Ceramic DIP; H = Hermetic Metal Can. For outline information see Package Information section.

[7] For AD537/883B specifications, refer to Analog Devices Military Products Databook.

CIRCUIT OPERATION

Block diagrams of the AD537 are shown above. A versatile operational amplifier (BUF) serves as the input stage; its purpose is to convert and scale the input voltage signal to a drive current in the NPN follower. Optimum performance is achieved when, at the full scale input voltage, a 1mA drive current is delivered to the current-to-frequency converter. The drive current to the current-to-frequency converter (an astable multivibrator) provides both the bias levels and the charging current to the externally connected timing capacitor. This "adaptive" bias scheme allows the oscillator to provide low nonlinearity over the entire current input range of 0.1 to 2000μA. The square wave oscillator output goes to the output driver which provides a floating base drive to the NPN power transistor. This floating drive allows the logic interface to be referenced to a different level than $-V_S$. The "SYNC" input ("D" package only) allows the oscillator to be slaved to an external master oscillator; this input can also be used to shut off the oscillator.

The reference generator uses a band-gap circuit (this allows single-supply operation to 4.5 volts which is not possible with low T.C. zeners) to provide the reference and bias levels for the amplifier and oscillator stages. The reference generator also provides the precision, low T.C. 1.00 volt output and the V_{TEMP} output which tracks absolute temperature at 1mV/K.

V-F CONNECTION FOR POSITIVE INPUT VOLTAGES

The positive voltage input range is from $-V_S$ (ground in single supply operation) to 4 volts below the positive supply. The connection shown in Figure 1 provides a very high (250MΩ) input impedance. The input voltage is converted to the proper drive current at pin 3 by selecting a scaling resistor. The full scale current is 1mA, so, for example a 10 volt range would require a nominal 10kΩ resistor. The trim range required will depend on capacitor tolerance. Full scale currents other than 1mA can be chosen, but linearity will be reduced; 2mA is the maximum allowable drive.

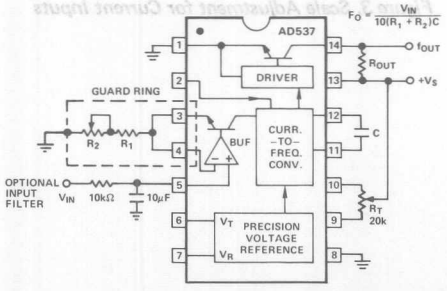


Figure 1. Standard V-F Connection for Positive Input Voltages

As indicated by the scaling relationship in Figure 1, a 0.01μF timing capacitor will give a 10kHz full scale frequency, and 0.001μF will give 100kHz with a 1mA drive current. The maximum frequency is 150kHz. Polystyrene or NPO ceramic capacitors are preferred for T.C. and dielectric absorption; polycarbonate or mica are acceptable; other types will degrade linearity. The capacitor should be wired very close to the AD537.

V-F CONNECTIONS FOR NEGATIVE INPUT VOLTAGE OR CURRENT

A wide range of negative input voltages can be accommodated with proper selection of the scaling resistor, as indicated in Figure 2. This connection, unlike the buffered positive connection, is not high impedance since the 1mA F.S. drive current must be supplied by the signal source. However, very large negative voltages beyond the supply can be handled easily; just modify the scaling resistors appropriately. Diode CR1 (HP5082-2811) is necessary for overload and latchup protection for current or voltage inputs.

If the input signal is a true current source, R_1 and R_2 are not used. Full scale calibration can be accomplished by connecting a 200kΩ pot in series with a fixed 27kΩ from pin 7 to $-V_S$ (see calibration section, below).

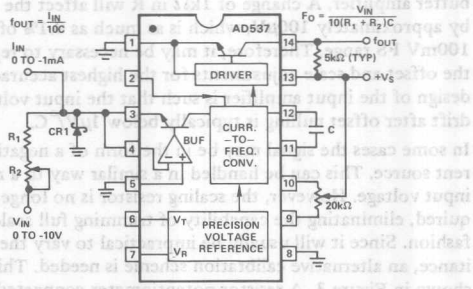


Figure 2. V-F Connections for Negative Input Voltage or Current

first is trimmed by adjustment of the scaling resistor R and the second by the (optional) potentiometer connected to $+V_S$ and the V_{OS} pins ("D" package only). Precise calibration requires the use of an accurate voltage standard set to the desired FS value and a frequency meter; a scope is useful for monitoring output waveshape. Verification of linearity requires the availability of a switchable voltage source (or a DAC) having a linearity error below ±0.005%, and the use of long measurement intervals to minimize count uncertainties. *Every AD537 is automatically tested for linearity*, and it will not usually be necessary to perform this verification, which is both tedious and time-consuming.

Although drifts are small it is good practice to allow the operating environment to attain stable temperature and to ensure that the supply, source and load conditions are proper. Begin by setting the input voltage to 1/10,000 of full scale. Adjust the offset pot until the output frequency is 1/10,000 of full scale (for example 1Hz for FS of 10kHz). This is most easily accomplished using a frequency meter connected to the output. Then apply the FS input voltage and adjust the gain pot until the desired FS frequency is indicated. In applications where the FS input is small, this adjustment will very slightly affect the offset voltage, due to the input bias current of the buffer amplifier. A change of 1kΩ in R will affect the input by approximately 100μV, which is as much as 0.1% of a 100mV FS range. Therefore, it may be necessary to repeat the offset and scale adjustments for the highest accuracy. The design of the input amplifier is such that the input voltage drift after offset nulling is typically below 1μV/°C.

In some cases the signal may be in the form of a negative current source. This can be handled in a similar way to a negative input voltage. However, the scaling resistor is no longer required, eliminating the capability of trimming full scale in this fashion. Since it will usually be impractical to vary the capacitance, an alternative calibration scheme is needed. This is shown in Figure 3. A resistor-potentiometer connected from the V_R output to $-V_S$ will alter the internal operating conditions in a predictable way, providing the necessary adjustment range. With the values shown, a range of ±4% is available; a larger range can be attained by reducing R1. This technique does not degrade the temperature-coefficient of the converter, and the linearity will be as for negative input voltages. The minimum supply voltage may be used.

selected to be 5% below the nominal value; with R2 in its mid-position the output frequency is given by

$$f = \frac{I}{10.5 \times C}$$

where f is in kHz, I is in mA and C is in μF. For example, for a FS frequency of 10kHz at a FS input of 1mA, C = 9500pF. Calibration is effected by applying the full-scale input and adjusting R2 for the correct reading.

This alternative adjustment scheme may also be used when it is desired to present an exact input resistance in the negative-voltage mode. The scaling relationship is then

$$f = \frac{V}{R_{exact}} \cdot \frac{1}{10.5\ C}$$

The calibration procedure is then similar to that used for positive input voltages, except that the scale adjustment is by means of R2.

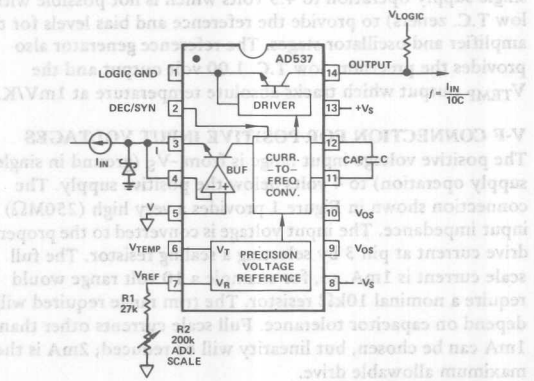


Figure 3. Scale Adjustment for Current Inputs

INPUT PROTECTION

The AD537 was designed to be used with a minimum of additional hardware. However, the successful application of a precision IC involves a good understanding of possible pitfalls and the use of suitable precautions.

The $-V_{IN}$, $+V_{IN}$ and I_{IN} pins should not be driven more than 300mV below $-V_S$. This would cause internal junctions to conduct, possibly damaging the IC. The AD537 can be protected from "below $-V_S$" inputs by a Schottky diode, CR1 (HP5082-2811) as shown in Figure 3. It is also desirable not to drive $+V_{IN}$, $-V_{IN}$ and I_{IN} above $+V_S$. In operation, the converter will become very nonlinear for inputs above ($+V_S$ -3.5V). Control currents above 2mA will also cause nonlinearity.

The 80dB dynamic range of the AD537 guarantees operation from a control current of 1mA (nominal FS) down to 100nA (equivalent to 1mV to 10V FS). Below 100nA improper operation of the oscillator may result, causing a false indication of input amplitude. In many cases this might be due to short-lived noise spikes which become added to the input. For example, when scaled to accept a FS input of 1V, the -80dB level is only 100μV, so when the mean input is only 60dB below FS (1mV), noise spikes of 0.9mV are sufficient to cause momentary malfunction.

This effect can be minimized by using a simple low-pass filter ahead of the converter and a guard ring around the I_{IN} or $-V_{IN}$ pins. For a FS of 10kHz a single-pole filter with a time-constant of 100ms (Figure 2) will be suitable, but the optimum configuration will depend on the application and type of signal processing. Noise spikes are only likely to be a cause of error when the input current remains near its minimum value for long periods of time; above 100nA (1mV) full integration of additive input noise occurs.

The AD537 is somewhat susceptible to interference from other signals. The most sensitive nodes (besides the inputs) are the capacitor terminals and the SYNC pin. The timing capacitor should be located as close as possible to the AD537 to minimize signal pickup in the leads. In some cases, guard rings or shielding may be required. The SYNC pin should be decoupled through a 0.005μF (or larger) capacitor to pin 13 ($+V_S$). This minimizes the possibility that the AD537 will attempt to synchronize to a spurious signal. This precaution is unnecessary on the metal can package since the SYNC function is not brought out to a package pin and is thus not susceptible to pickup.

DECOUPLING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 to 100Ω) in the supply lines to provide a measure of decoupling between the various circuits in a system. Ceramic capacitors of 0.1μF to 1.0μF should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD537.

A decoupling capacitor may also be useful from $+V_S$ to SYNC in those applications where very low cycle-to-cycle period variation (jitter) is demanded. By placing a capacitor across $+V_S$ and SYNC this noise is reduced. On the 10kHz FS range, a 6.8μF capacitor reduces the jitter to one in 20,000 which is adequate for most applications. A tantalum capacitor should be used to avoid errors due to dc leakage.

NONLINEARITY SPECIFICATION

The preferred method for specifying linearity error is in terms of the maximum deviation from the ideal relationship after calibrating the converter at full scale and "zero". This error will vary with the full scale frequency and the mode of operation. The AD537 operates best at a 10kHz full scale frequency with a negative voltage input; the linearity is typically within ±0.05%. Operating at higher frequencies or with positive inputs will degrade the linearity as indicates in the Specifications table. The shape of a typical linearity plot is given in Figure 4.

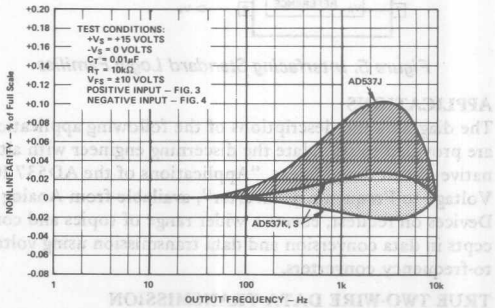


Figure 4a. Typical Nonlinearity Error Envelopes with 10kHz F.S. Output

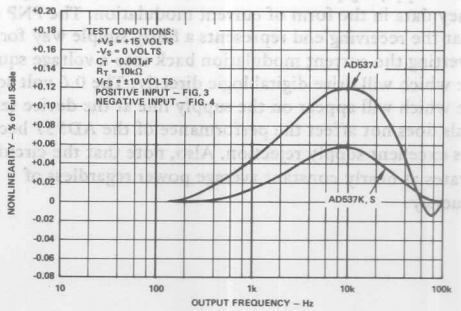
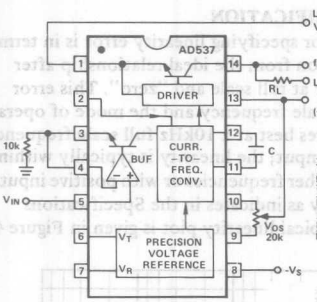


Figure 4b. Typical Nonlinearity Error with 100kHz F.S. Output

OUTPUT INTERFACING CONSIDERATIONS

The design of the output stage allows easy interfacing to all digital logic families. The collector and emitter of the output NPN transistor are both uncommitted; the emitter can be tied to any voltage between $-V_S$ and 4 volts below $+V_S$. The open collector can be pulled up to a voltage 36 volts above the emitter regardless of $+V_S$. The high power output stage can supply up to 20mA (10mA for "H" package) at a maximum saturation voltage of 0.4 volts. The stage limits the output current at 25mA; it can handle this limit indefinitely without damaging the device.

Figure 5 shows the AD537 with a standard 0 to +10 volt input connection and the output stage connections. The values for the logic common voltage, pull-up resistor, positive logic level, and $-V_S$ supply are given in the accompanying chart for several logic forms.



	V_{CC}	V_{EE}	R_L	$-V_S$
TTL/DTL	+5	GND	5k	GND
5V CMOS	+5	GND	20k	GND
15V CMOS/HNIL	+15	GND	10k	GND
ECL 10k	0	-8	5k	-8 to -15
ECL 2.5k	+1.3	-2	5k	-5
PMOS	0	-15	10k	-15

Figure 5. Interfacing Standard Logic Families

APPLICATIONS

The diagrams and descriptions of the following applications are provided to stimulate the discerning engineer with alternative circuit design ideas. "Applications of the AD537 IC Voltage-to-Frequency Converter", available from Analog Devices on request, covers a wider range of topics and concepts in data conversion and data transmission using voltage-to-frequency converters.

TRUE TWO-WIRE DATA TRANSMISSION

Figure 6 shows the AD537 in a true two-wire data transmission scheme. The twisted-pair transmission lines serves the dual purpose of supplying power to the device and also carrying frequency data in the form of current modulation. The PNP circuit at the receiving end represents a fairly simple way for converting the current modulation back into a voltage square wave which will drive digital logic directly. The 0.6 volt square wave which will appear on the supply line at the device terminals does not affect the performance of the AD537 because of its excellent supply rejection. Also, note that the circuit operates at nearly constant average power regardless of frequency.

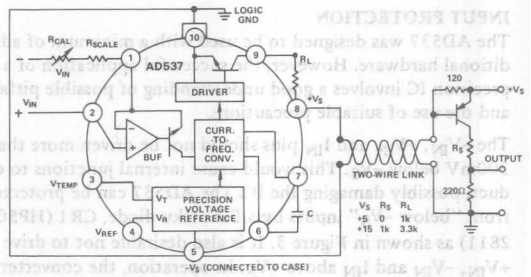


Figure 6. True Two-Wire Operation

F-V CONVERTERS

The AD537 can be used as a high linearity VCO in a phase-locked loop to accomplish frequency-to-voltage conversion. By operating the loop without a low-pass filter in the feedback path (first-order system), it can lock to any frequency from zero to an upper limit determined by the design, responding in three or four cycles to a step change of input frequency. In practice, the overall response time is determined by the characteristics of the averaging filter which follows the PLL.

Figure 7 shows a connection using a low-power TTL quad open-collector nand gate which serves as the phase comparator. The input signal should be a pulse train or square wave with characteristics similar to TTL or 5-volt CMOS outputs. Any duty cycle is acceptable, but the minimum pulse width is 40μs. The output voltage is one volt for a 10kHz input frequency. The output as shown here is at a fairly high impedance level; for many situations an additional buffer may be required.

Trimming is similar to V-F application trimming. First set the V_{OS} trimmer to mid-scale. Apply a 10kHz input frequency and trim the 2kΩ potentiometer for 1.00 volts out. Then apply a 10Hz waveform and trim the V_{OS} for 1mV out. Finally, retrim the full scale output at 10kHz. Other frequency scales can be obtained by appropriate scaling of timing components.

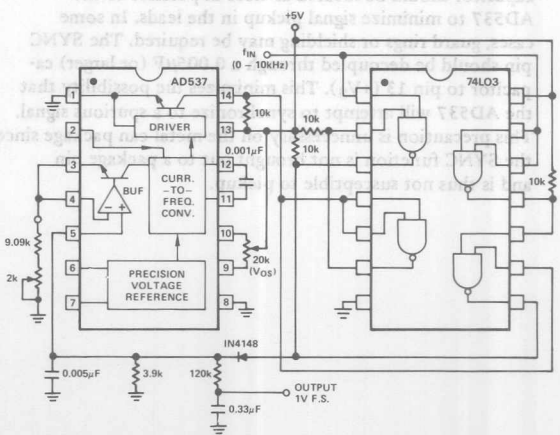


Figure 7. 10kHz F-V Converter

TEMPERATURE-TO-FREQUENCY CONVERSION

The linear temperature-proportional output of the AD537 can be used as shown in these applications to perform various direct temperature-to-frequency conversion functions; it can also be used with other external connections in a temperature sensing or compensation scheme. If the sensor output is used externally, it should be buffered through an op amp since loading that point will cause significant error in the sensor output as well as in the main V-F converter circuitry.

An absolute temperature (Kelvin)-to-frequency converter is very easily accomplished, as shown in Figure 8. The 1mV per K output serves as the input to the buffer amplifier, which then scales the oscillator drive current to a nominal 298μA at +25°C (298K). Use of a 1000pF capacitor results in a corresponding frequency of 2.98kHz. Setting the single 2kΩ trimmer for the correct frequency at a well-defined temperature near +25°C will normally result in an accuracy of ±2°C from -55°C to +125°C (using an AD537S). An NPO ceramic capacitor is recommended to minimize nonlinearity due to capacitance drift.

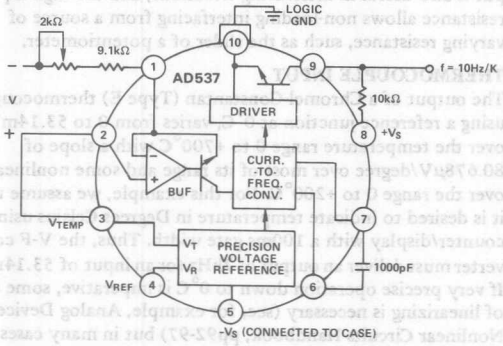


Figure 8. Absolute Temperature to Frequency Converter

OFFSET TEMPERATURE SCALES

Many other temperature scales can be set up by offsetting the temperature output with the voltage reference output. Such a scheme is shown by the Celsius-to-frequency converter in Figure 9. Corresponding component values for a Fahrenheit-to-frequency converter which give 10Hz/°F are given in parentheses.

A simple calibration procedure which will provide ±2°C accuracy requires substitution of a 7.27k resistor for the series combination of the 6.04k with the 2k trimmer; then simply set the 500Ω trimmer to give 250Hz at +25°C.

High accuracy calibration procedure:

1. Measure room temperature in K.
2. Measure temperature output at pin 6 at that temperature.
3. Calculate offset adjustment as follows:

$$\text{Offset Voltage (mV)} = \frac{V_{TEMP}\ (\text{pin 6})\ (\text{mV})}{\text{Room temp (K)}} \times 273.2$$

4. Temporarily disconnect 49Ω resistor (or 500Ω pot) and trim 2kΩ pot to give the offset voltage at the indicated node. Reconnect 49Ω resistor.
5. Adjust slope trimmer to give proper frequency at room temperature (+25°C = 250Hz).
   Adjustment for °F or any other scale is analogous.

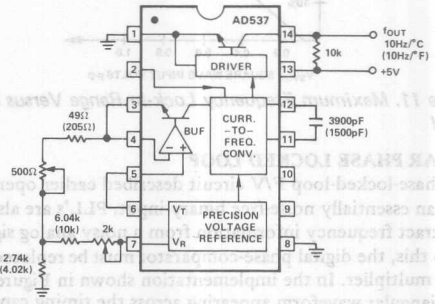


Figure 9. Offset Temperature Scale Converters-Centigrade and (Fahrenheit) to Frequency

SYNCHRONOUS OPERATION

The SYNC terminal at pin 2 of the DIP package can be used to synchronize a free running AD537 to a master oscillator, either at a multiple or a sub-multiple of the primary frequency. The preferred connection is shown in Figure 10. The diodes are used to produce the proper drive magnitude from high level signals. The SYNC terminal can also be used to shut off the oscillator. Shorting the terminal to $+V_S$ will stop the oscillator, and the output will go high (output NPN off).

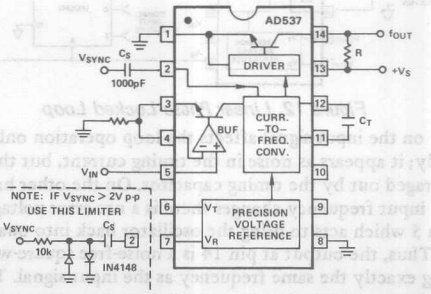


Figure 10. Connection for Synchronous Operation

Figure 11 shows the maximum pull-in range available at a given signal level; the optimum signal is a 0.8 to 1.0 volt square wave; signals below 0.1 volt will have no effect; signals above 2 volts p-p will disable the oscillator. The AD537 can normally be synchronized to a signal which forces it to a higher frequency up to 30% above the nominal free-running frequency, it can only be brought down about 1-2%.

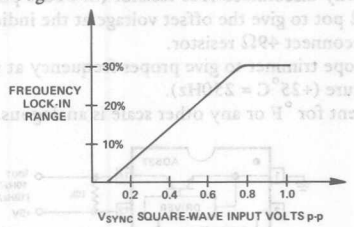


Figure 11. Maximum Frequency Lock-In Range Versus Sync. Signal

LINEAR PHASE LOCKED LOOP

The phase-locked-loop F/V circuit described earlier operates from an essentially noise-free binary input. PLL's are also used to extract frequency information from a noisy analog signal. To do this, the digital phase-comparator must be replaced by a linear multiplier. In the implementation shown in Figure 12, the triangular waveform appearing across the timing capacitor is used as one of the multiplier inputs; the signal provides the other input. It can be shown that the mean value of the multiplier output is zero when the two signals are in quadrature. In this condition, the ripple in the error signal is also quite small. Thus, the voltage at pin 5 is essentially zero, and the frequency is determined primarily by the current in the timing resistor, controlled either manually or by a control voltage.

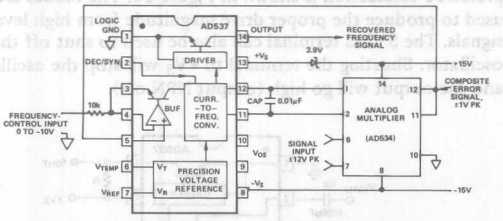


Figure 12. Linear Phase-Locked Loop

Noise on the input signal affects the loop operation only slightly; it appears as noise in the timing current, but this is averaged out by the timing capacitor. On the other hand, if the input frequency changes there is a net error voltage at pin 5 which acts to bring the oscillator back into quadrature. Thus, the output at pin 14 is a noise-free square-wave having exactly the same frequency as the input signal. The effectiveness of this circuit can be judged from Figure 13 which shows the response to an input of 1V rms 1kHz sinusoid plus 1V rms Gaussian noise. The positive supply to the AD537 is reduced by about 4V in order to keep the voltages at pins 11 and 12 within the common-mode range of the AD534.

Since this is also a first-order loop the circuit possesses a very wide capture range. However, even better noise-integrating properties can be achieved by adding a filter between the multiplier output and the VCO input. Details of suitable filter characteristics can be found in the standard texts on the subject.

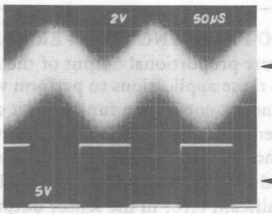


Figure 13. Performance of AD537 Linear Phase-Locked Loop

By connecting the multiplier output to the lower end of the timing resistor and moving the control input to pin 5, a high-resistance frequency-control input is made available. However, due to the reduced supply voltage, this input cannot exceed +6V.

TRANSDUCER INTERFACE

The AD537 was specifically designed to accept a broad range of input signals, particularly small voltage signals, which may be converted directly (unlike many V-F converters which require signal pre-conditioning). The 1.00V stable reference output is also useful in interfacing situations, and the high input resistance allows non-loading interfacing from a source of varying resistance, such as the slider of a potentiometer.

THERMOCOUPLE INPUT

The output of a Chromel-Constantan (Type E) thermocouple, using a reference junction at 0°C, varies from 0 to 53.14mV over the temperature range 0 to +700°C with a slope of 80.678μV/degree over most of its range and some nonlinearity over the range 0 to +200°C. For this example, we assume that it is desired to indicate temperature in Degrees Celsius using a counter/display with a 100ms gate width. Thus, the V-F converter must deliver an output of 7kHz for an input of 53.14mV. If very precise operation down to 0°C is imperative, some sort of linearizing is necessary (see, for example, Analog Devices' Nonlinear Circuits Handbook, pp92-97) but in many cases operation is only needed over part of the range.

The circuit shown in Figure 14 provides good accuracy from +300°C to +700°C. The extrapolation of the temperature-voltage curve back to 0°C shows that an offset of -3.34mV is required to fit the curve most exactly. This small amount of voltage can be introduced without an additional calibration step using the +1.00V output of the AD537. To adjust the scale, the thermocouple should be raised to a known reference temperature near 500°C and the frequency adjusted to value using R1. The error should be within ±0.2% over the range 400°C to 700°C.

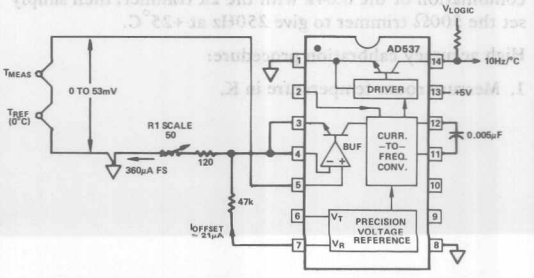


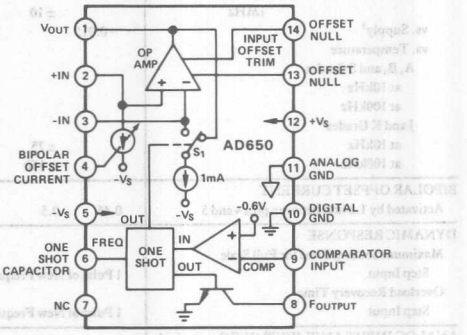
Figure 14. Thermocouple Interface with First-Order Linearization

AD650

FEATURES

- V/F Conversion to 1MHz
- Reliable Monolithic Construction
- Very Low Nonlinearity
  - 0.002% typ at 10kHz
  - 0.005% typ at 100kHz
  - 0.07% typ at 1MHz
- Input Offset Trimmable to Zero
- CMOS or TTL Compatible
- Unipolar, Bipolar, or Differential V/F
- V/F or F/V Conversion
- Available in Surface Mount
- MIL-STD-883-Compliant Versions Available

PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD650 V/F/V (voltage-to-frequency or frequency-to-voltage converter) provides a combination of high frequency operation and low nonlinearity previously unavailable in monolithic form. The inherent monotonicity of the V/F transfer function makes the AD650 useful as a high-resolution analog-to-digital converter. A flexible input configuration allows a wide variety of input voltage and current formats to be used, and an open-collector output with separate digital ground allows simple interfacing to either standard logic families or opto-couplers.

The linearity error of the AD650 is typically 20ppm (0.002% of full scale) and 50ppm (0.005%) maximum at 10kHz full scale. This corresponds to approximately 14-bit linearity in an analog-to-digital converter circuit. Higher full-scale frequencies or longer count intervals can be used for higher resolution conversions. The AD650 has a useful dynamic range of six decades allowing extremely high resolution measurements. Even at 1MHz full scale, linearity is guaranteed less than 1000ppm (0.1%) on the AD650KN, KP, BD and SD grades.

In addition to analog-to-digital conversion, the AD650 can be used in isolated analog signal transmission applications, phased-locked-loop circuits, and precision stepper motor speed controllers. In the F/V mode, the AD650 can be used in precision tachometer and FM demodulator circuits.

The input signal range and full-scale output frequency are user-programmable with two external capacitors and one resistor. Input offset voltage can be trimmed to zero with an external potentiometer.

The AD650JN and AD650KN are offered in a plastic 14-pin DIP package. The AD650JP and AD650KP are available in a 20-pin plastic leaded chip carrier (PLCC). Both plastic packaged versions of the AD650 are specified for the commerical (0 to +70°C) temperature range. For industrial temperature range (−25°C to +85°C) applications, the AD650AD and AD650BD are offered in a ceramic package. The AD650SD is specified for the full −55°C to +125°C extended temperature range.

PRODUCT HIGHLIGHTS

1. In addition to very high linearity, the AD650 can operate at full scale output frequency up to 1MHz. The combination of these two features makes the AD650 an inexpensive solution for applications requiring high resolution monotonic A/D conversion.
2. The AD650 has a very versatile architecture that can be configured to accommodate bipolar, unipolar, or differential input voltages, or unipolar input currents.
3. TTL or CMOS compatibility is achieved using an open collector frequency output. The pullup resistor can be connected to voltages up to +30V, or +15V or +5V for conventional CMOS or TTL logic levels.
4. The same components used for V/F conversion can also be used for F/V conversion by adding a simple logic biasing network and reconfiguring the AD650.
5. The AD650 provides separate analog and digital grounds. This feature allows prevention of ground loops in real-world applications.
6. The AD650 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD650/883B data sheet for detailed specifications.

	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
DYNAMIC PERFORMANCE										
Full Scale Frequency Range			1			1			1	MHz
Nonlinearity[1] f_{max} = 10kHz		0.002	0.005		0.002	0.005		0.002	0.005	%
100kHz		0.005	**0.02**		0.005	**0.02**		0.005	**0.02**	%
500kHz		0.02	0.05		0.02	0.05		0.02	0.05	%
1MHz		0.1			0.05	**0.1**		0.05	**0.1**	%
Full Scale Calibration Error[2], 100kHz		±5			±5			±5		%
1MHz		±10			±10			±5		%
vs. Supply[3]	−0.015		**+0.015**	−0.015		**+0.015**	−0.015		**+0.015**	% of FSR/V
vs. Temperature										
A, B, and S Grades										
at 10kHz			±75			±75			**±75**	ppm/°C
at 100kHz			±150			±150			**±150**	ppm/°C
J and K Grades										
at 10kHz		±75			±75					ppm/°C
at 100kHz		±150			±150					ppm/°C
BIPOLAR OFFSET CURRENT										
Activated by 1.24kΩ between pins 4 and 5	0.45	0.5	0.55	0.45	0.5	0.55	0.45	0.5	0.55	mA
DYNAMIC RESPONSE										
Maximum Settling Time for Full Scale										
Step Input	1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			
Overload Recovery Time										
Step Input	1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			
ANALOG INPUT AMPLIFIER (V/F Conversion)										
Current Input Range (Figure 1)	0		+0.6	0		+0.6	0		+0.6	mA
Voltage Input Range (Figure 5)	−10		0	−10		0	−10		0	V
Differential Impedance		2MΩ‖10pF			2MΩ‖10pF			2MΩ‖10pF		
Common Mode Impedance		1000MΩ‖10pF			1000MΩ‖10pF			1000MΩ‖10pF		
Input Bias Current										
Noninverting Input		40	**100**		40	**100**		40	**100**	nA
Inverting Input		±8	**±20**		±8	**±20**		±8	**±20**	nA
Input Offset Voltage										
(Trimmable to Zero)			**±4**			**±4**			**±4**	mV
vs. Temperature (T_{min} to T_{max})		±30				±30			±30	µV/°C
Safe Input Voltage		$\pm V_S$			$\pm V_S$			$\pm V_S$		C
COMPARATOR (F/V Conversion)										
Logic "0" Level	$-V_S$		−1	$-V_S$		−1	$-V_S$		+1	V
Logic "1" Level	0		$+V_S$	0		$+V_S$	0		$+V_S$	V
Pulse Width Range[4]	0.1		$(0.3 \times t_{OS})$	0.1		$(0.3 \times t_{OS})$	0.1		$(0.3 \times t_{OS})$	µs
Input Impedance		250			250			250		kΩ
OPEN COLLECTOR OUTPUT (V/F Conversion)										
Output Voltage in Logic "0"										
$I_{SINK} \leq 8mA$, T_{min} to T_{max}			0.4			0.4			0.4	V
Output Leakage Current in Logic "1"			**100**			**100**			**100**	nA
Voltage Range[5]	0		+36	0		+36	0		+36	V
AMPLIFIER OUTPUT (F/V Conversion)										
Voltage Range (1500Ω min load resistance)	0		+10	0		+10	0		+10	V
Source Current (750Ω max load resistance)	10			10			10			mA
Capacitive Load (Without Oscillation)			100			100			100	pF
POWER SUPPLY										
Voltage, Rated Performance	±9		**±18**	±9		**±18**	±9		**±18**	V
Quiescent Current			**8**			**8**			**8**	mA
TEMPERATURE RANGE										
Rated Performance – N Package	0		+70	0		+70				°C
D Package	−25		+85	−25		+85	−55		+125	°C
Storage – N Package	−25		+85	−25		+85				°C
D Package	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTIONS[6]										
PLCC (P-20A)		AD650JP			AD650KP					
Plastic DIP (N-14)		AD650JN			AD650KN					
Ceramic DIP (D-14)		AD650AD			AD650BD			AD650SD		

NOTES

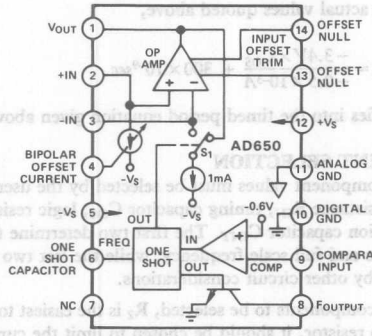
[1]Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a fraction of full scale.
[2]Full scale calibration error adjustable to zero.
[3]Measured at full scale output frequency of 100kHz.
[4]Refer to F/V conversion section of the text.
[5]Referred to digital ground.
[6]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage $+V_S$ to $-V_S$ 36V
Storage Temperature Ceramic . . . . . −55°C to +165°C
Plastic . . . . . −25°C to +125°C
Differential Input Voltage (Pins 2 & 3) . . . . . ±10V
Maximum Input Voltage . . . . . ±V_S
Open Collector Output Voltage Above Digital GND . . 36V
Current 50mA
Amplifier Short Ckt to Ground . . . . . Indefinite
Comparator Input Voltage (Pin 9) . . . . . ±V_S



AD650 Pin Configuration

ORDERING GUIDE

Model[1]	Gain Tempco ppm/°C 100kHz	1MHz Linearity	Specified Temperature Range °C	Package
AD650JN	150 typ	0.1% typ	0 to +70	Plastic DIP
AD650KN	150 typ	0.1% max	0 to +70	Plastic DIP
AD650JP	150 typ	0.1% typ	0 to +70	PLCC
AD650KP	150 typ	0.1% max	0 to +70	PLCC
AD650AD	150 max	0.1% typ	−25 to +85	Ceramic
AD650BD	150 max	0.1% max	−25 to +85	Ceramic
AD650SD	150 max	0.1% max	−55 to +125	Ceramic

NOTE
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD650/883B data sheet.

3

CIRCUIT OPERATION

UNIPOLAR CONFIGURATION

The AD650 is a *charge balance* voltage-to-frequency converter. In the connection diagram shown in Figure 1, or the block diagram of Figure 2a, the input signal is converted into an equivalent current by the input resistance R_{IN}. This current is *exactly* balanced by an internal feedback current delivered in short, timed bursts from the switched 1mA internal current source. These bursts of current may be thought of as precisely defined packets of charge. The required number of charge packets, each producing one pulse of the output transistor, depends upon the amplitude of the input signal. Since the number of charge packets delivered per unit time is dependent on the input signal amplitude, a linear voltage-to-frequency transformation will be accomplished. The frequency output is furnished via an open collector transistor.

A more rigorous analysis demonstrates how the charge balance voltage-to-frequency conversion takes place.

A block diagram of the device arranged as a V to F converter is shown in Figure 2a. The unit is comprised of an input integrator, a current source and steering switch, a comparator and a one-shot. When the output of the one-shot is low, the current steering switch S_1 diverts all the current to the output of the op amp; this is called the Integration Period. When the one-shot has been triggered and its output is high, the switch S_1 diverts all the current to the summing junction of the op amp; this is called the Reset Period. The two different states are shown in Figure 2 along with the various branch currents. It should be noted that the output current from the op amp is the same for either state, thus minimizing transients.

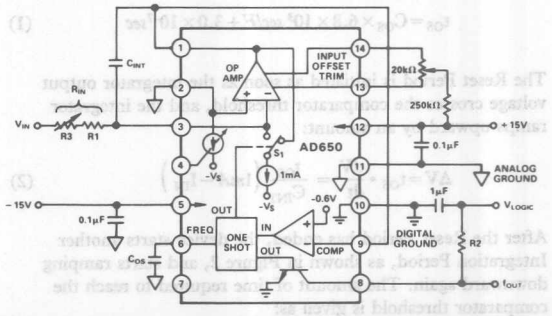


Figure 1. Connection Diagram for V/F Conversion, Positive Input Voltage

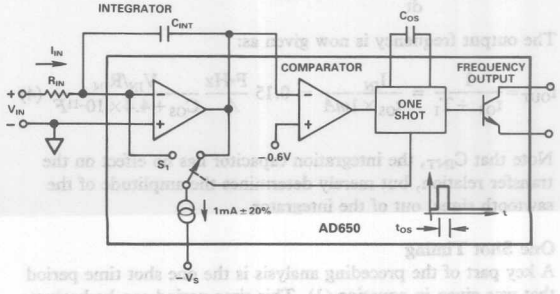


Figure 2a. Block Diagram

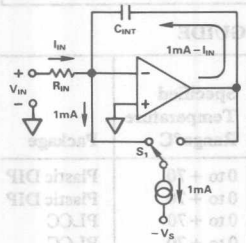


Figure 2b. Reset Mode

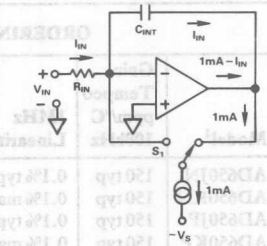


Figure 2c. Integrate Mode

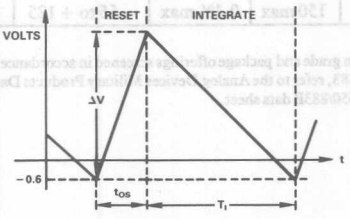


Figure 2d. Voltage Across C_{INT}

The positive input voltage develops a current ($I_{IN} = V_{IN}/R_{IN}$) which charges the integrator capacitor C_{INT}. As charge builds up on C_{INT}, the output voltage of the integrator ramps downward towards ground. When the integrator output voltage (pin 1) crosses the comparator threshold (−0.6 volt) the comparator triggers the one shot, whose time period, t_{OS} is determined by the one shot capacitor C_{OS}.

Specifically, the one shot time period is:

$$t_{OS} = C_{OS} \times 6.8 \times 10^3\ sec/F + 3.0 \times 10^{-7} sec \quad (1)$$

The Reset Period is initiated as soon as the integrator output voltage crosses the comparator threshold, and the integrator ramps upward by an amount:

$$\Delta V = t_{OS} \cdot \frac{dV}{dt} = \frac{t_{OS}}{C_{INT}} \left(1mA - I_{IN}\right) \quad (2)$$

After the Reset Period has ended, the device starts another Integration Period, as shown in Figure 2, and starts ramping downward again. The amount of time required to reach the comparator threshold is given as:

$$T_I = \frac{\Delta V}{\frac{dV}{dt}} = \frac{t_{OS}/C_{INT}(1mA - I_{IN})}{I_{IN}/C_{INT}} = t_{OS}\left(\frac{1mA}{I_{IN}} - 1\right) \quad (3)$$

The output frequency is now given as:

$$f_{OUT} = \frac{1}{t_{OS} + T_I} = \frac{I_{IN}}{t_{OS} \times 1mA} = 0.15\ \frac{F \cdot Hz}{A}\ \frac{V_{IN}/R_{IN}}{C_{OS} + 4.4 \times 10^{-11} F} \quad (4)$$

Note that C_{INT}, the integration capacitor has no effect on the transfer relation, but merely determines the amplitude of the sawtooth signal out of the integrator.

One Shot Timing

A key part of the preceding analysis is the one shot time period that was given in equation (1). This time period can be broken down into approximately 300ns of propagation delay, and a second time segment dependent linearly on timing capacitor C_{OS}. When the one shot is triggered, a voltage switch that holds pin 6 at analog ground is opened allowing that voltage to change. An internal 0.5mA current source connected to pin 6 then draws its current out of C_{OS}, causing the voltage at pin 6 to decrease linearly. At approximately −3.4V, the one shot resets itself, thereby ending the timed period and starting the V/F conversion cycle over again. The total one shot time period can be written mathematically as:

$$t_{OS} = \frac{\Delta V\ C_{OS}}{I_{DISCHARGE}} + T_{GATE\ DELAY} \quad (5)$$

substituting actual values quoted above,

$$t_{OS} = \frac{-3.4V \times C_{OS}}{-0.5 \times 10^{-3} A} + 300 \times 10^{-9} sec \quad (6)$$

This simplifies into the timed period equation given above.

COMPONENT SELECTION

Only four component values must be selected by the user. These are input resistance R_{IN}, timing capacitor C_{OS}, logic resistor R_2, and integration capacitor C_{INT}. The first two determine the input voltage and full scale frequency, while the last two are determined by other circuit considerations.

Of the four components to be selected, R_2 is the easiest to define. As a pull up resistor, it should be chosen to limit the current through the output transistor to 8mA if a TTL maximum V_{OL} of 0.4V is desired. For example, if a 5V logic supply is used, R_2 should be no smaller than 5V/8mA or 625Ω. A larger value can be used if desired.

R_{IN} and C_{OS} are the only two parameters available to set the full scale frequency to accommodate the given signal range. The "swing" variable that is affected by the choice of R_{IN} and C_{OS} is nonlinearity. The selection guide of Figure 3 shows this quite graphically. In general, larger values of C_{OS} and lower full scale input currents (higher values of R_{IN}) provide better linearity. In Figure 3, the implications of four different choices of R_{IN} are shown. Although the selection guide is set up for a unipolar configuration with a zero to 10V input signal range, the results can be extended to other configurations and input signal ranges. For a full scale frequency of 100kHz (corresponding to 10V input), you can see that among the available choices, R_{IN} = 20k and C_{OS} = 620pF gives the lowest nonlinearity, 0.0038%. Also, if you wish to use the highest frequency that will give the 20ppm minimum nonlinearity, it is approximately 33kHz (40.2kΩ and 1000pF).

For input signal spans other than 10V, the input resistance must be scaled proportionately. For example, if 100kΩ is called out for a 0–10V span, 10k would be used with a 0–1V span, or 200kΩ with a ±10V bipolar connection.

The last component to be selected is the integration capacitor C_{INT}. In almost all cases, the best value for C_{INT} can be calculated using the equation:

$$C_{INT} = \frac{10^{-4} F/sec}{f_{MAX}} \quad (1000pF\ minimum) \quad (7)$$

When the proper value for C_{INT} is used, the charge balance architecture of the AD650 provides continuous integration of the input signal, hence large amounts of noise and interference

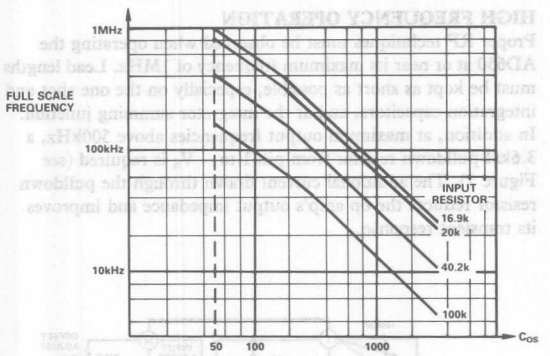


Figure 3a. Full Scale Frequency vs. C_{OS}

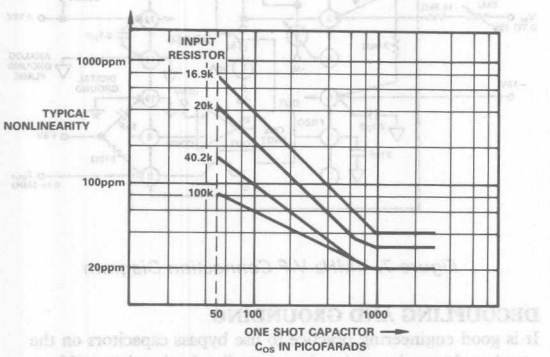


Figure 3b. Typical Nonlinearity vs. C_{OS}

can be rejected. If the output frequency is measured by counting pulses during a constant gate period, the integration provides infinite normal mode rejection for frequencies corresponding to the gate period and its harmonics. However, if the integrator stage becomes saturated by an excessively large noise pulse, the continuous integration of the signal will be interrupted, allowing the noise to appear at the output. If the approximate amount of noise that will appear on C_{INT} is known (V_{NOISE}), the value of C_{INT} can be checked using the following inequality:

$$C_{INT} > \frac{t_{OS} \times 1 \times 10^{-3} A}{+V_S - 3V - V_{NOISE}} \quad (8)$$

For example, consider an application calling for a maximum frequency of 75kHz, a 0–1 volt signal range, and supply voltages of only ±9 volts. The component selection guide of Figure 3 is used to select 2.0kΩ for R_{IN} and 1000pF for C_{OS}. This results in a one shot time period of approximately 7μs. Substituting 75kHz into equation 7 yields a value of 1300pF for C_{INT}. When the input signal is near zero, 1mA flows through the integration capacitor to the switched current sink during the reset phase, causing the voltage across C_{INT} to increase by approximately 5.5 volts. Since the integrator output stage requires approximately 3 volts head room for proper operation, only 0.5 volt margin remains for integrating extraneous noise on the signal line. A negative noise pulse at this time might saturate the integrator, causing an error in signal integration. Increasing C_{INT} to 1500 or 2000pF will provide much more noise margin, thereby eliminating this potential trouble spot.

BIPOLAR V/F

Figure 4 shows how the internal bipolar current sink is used to provide a half-scale offset for a ±5V signal range, while providing a 100kHz maximum output frequency. The nominally 0.5mA (±10%) offset current sink is enabled when a 1.24kΩ resistor is connected between pins 4 and 5. Thus, with the grounded 10kΩ nominal resistance shown, a −5V offset is developed at pin 2. Since pin 3 must also be at −5V, the current through R_{IN} is 10V/40kΩ = +0.25mA at V_{IN} = +5V, and 0mA at V_{IN} = −5V.

Components are selected using the same guidelines outlined for the unipolar configuration with one alteration. The voltage across the total signal range must be equated to the maximum

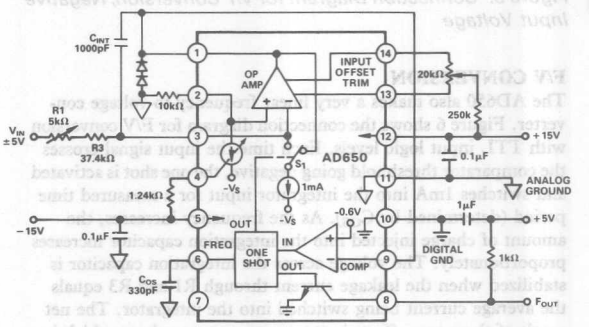


Figure 4. Connections for ±5V Bipolar V/F with 0 to 100kHz TTL Output

input voltage in the unipolar configuration. In other words, the value of the input resistor R_{IN} is determined by the input voltage span, not the maximum input voltage. A diode from pin 1 to ground is also recommended. This is discussed further under "Other Circuit Conditions".

As in the unipolar circuit, R_{IN} and C_{OS} must have low temperature coefficients to minimize the overall gain drift. The 1.24kΩ resistor used to activate the 0.5mA offset current should also have a low temperature coefficient. The bipolar offset current has a temperature coefficient of approximately −200ppm/°C.

UNIPOLAR V/F, NEGATIVE INPUT VOLTAGE

Figure 5 shows the connection diagram for V/F conversion of negative input voltages. In this configuration full scale output frequency occurs at negative full scale input, and zero output frequency corresponds with zero input voltage.

A very high impedance signal source may be used since it only drives the noninverting integrator input. Typical input impedance at this terminal is 1GΩ or higher. For V/F conversion of positive input signals using the connection diagram of Figure 1, the signal generator must be able to source the integration current to drive the AD650. For the negative V/F conversion circuit of Figure 5, the integration current is drawn from ground through R1 and R3, and the active input is high impedance.

Circuit operation for negative input voltages is very similar to positive input unipolar conversion described in a previous section. For best operating results use component equations listed in that section.

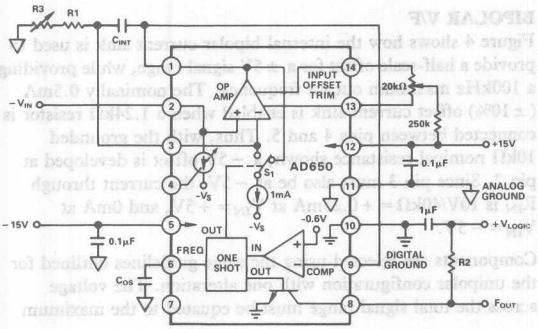


Figure 5. Connection Diagram for V/F Conversion, Negative Input Voltage

F/V CONVERSION

The AD650 also makes a very linear frequency-to-voltage converter. Figure 6 shows the connection diagram for F/V conversion with TTL input logic levels. Each time the input signal crosses the comparator threshhold going negative, the one shot is activated and switches 1mA into the integrator input for a measured time period (determined by C_{OS}). As the frequency increases, the amount of charge injected into the integration capacitor increases proportionately. The voltage across the integration capacitor is stabilized when the leakage current through R1 and R3 equals the average current being switched into the integrator. The net result of these two effects is an average output voltage which is proportional to the input frequency. Optimum performance can be obtained by selecting components using the same guidelines and equations listed in the V/F conversion section.

The circuit of Figure 6 can be biased to accommodate almost any input signal waveform. With a TTL input, the 1000pF coupling capacitor and 2.2kΩ resistor creates a clean negative spike that triggers the one shot on negative going edges. For input signals with slower edges, a larger capacitor and/or resistor may be used as long as the comparator is never exposed to a voltage lower than −0.6V for longer than the one shot time period. If this happens, the one shot will trigger itself more than once per cycle, creating discontinuities in the F/V transfer function. An input pulse greater than 100ns but less than $0.3 \times t_{OS}$ is recommended (t_{OS} is defined by equation 1 in the circuit operation section, unipolar configuration).

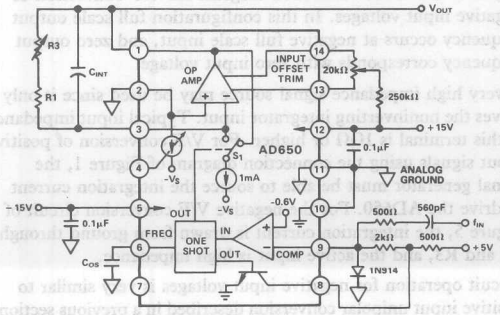


Figure 6. Connection Diagram for F/V Conversion

HIGH FREQUENCY OPERATION

Proper RF techniques must be observed when operating the AD650 at or near its maximum frequency of 1MHz. Lead lengths must be kept as short as possible, especially on the one shot and integration capacitors, and at the integrator summing junction. In addition, at maximum output frequencies above 500kHz, a 3.6kΩ pulldown resistor from pin 1 to $-V_S$ is required (see Figure 7). The additional current drawn through the pulldown resistor reduces the op amp's output impedance and improves its transient response.

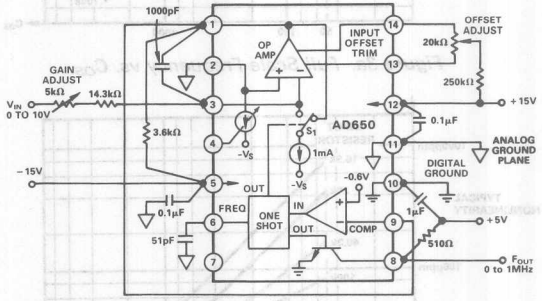


Figure 7. 1MHz V/F Connection Diagram

DECOUPLING AND GROUNDING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 to 100Ω) in the supply lines to provide a measure of decoupling between the various circuits in a system. Ceramic capacitors of 0.1μF to 1.0μF should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD650.

In addition, a larger board level decoupling capacitor of 1μF to 10μF should be located relatively close to the AD650 on each power supply line. Such precautions are imperative in high resolution data acquisition applications where one expects to exploit the full linearity and dynamic range of the AD650. Although some types of circuits may operate satisfactorily with power supply decoupling at only one location on each circuit board, such practice is strongly discouraged in high accuracy analog design.

Separate digital and analog grounds are provided on the AD650. The emitter of the open collector frequency output transistor is the only node returned to the digital ground. All other signals are referred to analog ground. The purpose of the two separate grounds is to allow isolation between the high precision analog signals and the digital section of the circuitry. As much as several hundred millivolts of noise can be tolerated on the digital ground without affecting the accuracy of the VFC. Such ground noise is inevitable when switching the large currents associated with the frequency output signal.

At 1MHz full scale, it is necessary to use a pull-up resistor of about 500Ω in order to get the rise time fast enough to provide well defined output pulses. This means that from a 5 volt logic supply, for example, the open collector output will draw 10mA.

This much current being switched will surely cause ringing on long ground runs due to the self inductance of the wires. For instance, #20 gauge wire has an inductance of about 20nH per inch; a current of 10mA being switched in 50ns at the end of 12 inches of 20 gauge wire will produce a voltage spike of 50mV. The separate digital ground of the AD650 will easily handle these types of switching transients.

A problem will remain from interference caused by radiation of electro-magnetic energy from these fast transients. Typically, a voltage spike is produced by inductive switching transients; these spikes can capacitively couple into other sections of the circuit. Another problem is ringing of ground lines and power supply lines due to the distributed capacitance and inductance of the wires. Such ringing can also couple interference into sensitive analog circuits. The best solution to these problems is proper bypassing of the logic supply at the AD650 package. A 1μF to 10μF tantalum capacitor should be connected directly to the supply side of the pull-up resistor and to the digital ground – pin 10. The pull-up resistor should be connected directly to the frequency output – pin 8. The lead lengths on the bypass capacitor and the pull up resistor should be as short as possible. The capacitor will supply (or absorb) the current transients, and large ac signals will flow in a physically small loop through the capacitor, pull up resistor, and frequency output transistor. It is important that the loop be physically small for two reasons: first, there is less self-inductance if the wires are short, and second, the loop will not radiate RFI efficiently.

The digital ground (pin 10) should be separately connected to the power supply ground. Note that the leads to the digital power supply are only carrying dc current and cannot radiate RFI. There may also be a dc ground drop due to the difference in currents returned on the analog and digital grounds. This will not cause any problem. In fact, the AD650 will tolerate as much as 0.25 volt dc potential difference between the analog and digital grounds. These features greatly ease power distribution and ground management in large systems. Proper technique for grounding requires separate digital and analog ground returns to the power supply. Also, the signal ground must be referred directly to analog ground (pin 11) at the package. All of the signal grounds should be tied directly to pin 11, especially the one-shot capacitor. More information on proper grounding and reduction of interference can be found in reference 1.

TEMPERATURE COEFFICIENTS

The drift specifications of the AD650 do not include temperature effects of any of the supporting resistors or capacitors. The drift of the input resistors R1 and R3 and the timing capacitor C_{OS} directly affect the overall temperature stability. In the application of Figure 2, a 10ppm/°C input resistor used with a 100ppm/°C capacitor may result in a maximum overall circuit gain drift of:

150ppm/°C (AD650A) + 100ppm/°C (C_{OS}) + 10ppm/°C (R_{IN}) = 260ppm/°C

In bipolar configuration, the drift of the 1.24kΩ resistor used to activate the internal bipolar offset current source will directly affect the value of this current. This resistor should be matched to the resistor connected to the op amp noninverting input (pin 2), see Figure 4. That is, the temperature coefficients of these two resistors should be equal. If this is the case, then the effects of the temperature coefficients of the resistors cancel each other, and the drift of the offset voltage developed at the op amp noninverting input will be determined solely by the AD650. Under these conditions the TC of the bipolar offset voltage is typically −200ppm/°C and is a maximum of −300ppm/°C. The offset voltage always decreases in magnitude as temperature is increased.

Other circuit components do not directly influence the accuracy of the VFC over temperature changes as long as their actual values are not so different from the nominal value as to preclude operation. This includes the integration capacitor, C_{INT}. A change in the capacitance value of C_{INT} simply results in a different rate of voltage change across the capacitor. During the Integration Phase (refer to Figure 2), the rate of voltage change across C_{INT} has the opposite effect that it does during the Reset Phase. The result is that the conversion accuracy is unchanged by either drift or tolerance of C_{INT}. The net effect of a change in the integrator capacitor is simply to change the peak to peak amplitude of the sawtooth waveform at the output of the integrator.

The gain temperature coefficient of the AD650 is not a constant value. Rather the gain TC is a function of both the full scale frequency and the ambient temperature. At a low full scale frequency, the gain TC is determined primarily by the stability of the internal reference–a buried zener reference. This low speed gain TC can be quite good; at 10kHz full scale, the gain TC near 25°C is typically 0 ±50ppm/°C. Although the gain TC changes with ambient temperature (tending to be more positive at higher temperatures), the drift remains within a ±75ppm/°C window over the entire military temperature range. At full scale frequencies higher than 10kHz dynamic errors become much more important than the static drift of the dc reference. At a full scale frequency of 100kHz and above, these timing errors dominate the gain TC. For example, at 100kHz full scale frequency (R_{IN} = 40k and C_{OS} = 330pF) the gain TC near room temperature is typically −80 ±50ppm/°C, but at an ambient temperature near +125°C, the gain TC tends to be more positive and is typically +15 ±50ppm/°C. This information is presented in a graphical form in Figure 8. The gain TC always tends to become more positive at higher temperatures. Therefore it is possible to adjust the gain TC of the AD650 by using a one-shot capacitor with an appropriate TC to cancel the drift of the circuit. For example, consider the 100kHz full scale frequency. An average drift of −100ppm/°C means that as temperature is increased, the circuit will produce a lower frequency in reponse to a given input voltage. This means that the one-shot capacitor must decrease in value as temperature increases in order to compensate the gain TC of the AD650; that is, the capacitor must have a TC of −100ppm/°C. Now consider the 1MHz full scale frequency.

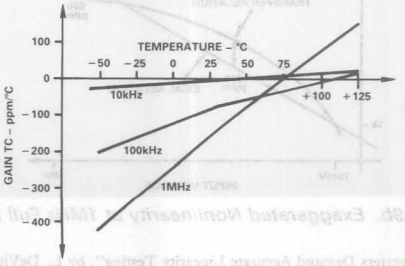


Figure 8. Gain TC vs. Temperature

[1]"Noise Reduction Techniques in Electronic Systems", by H. W. OTT, (John Wiley, 1976).

It is not possible to achieve very much improvement in performance unless the expected ambient temperature range is known. For example, in a constant low temperature application such as gathering data in an Arctic climate (approximately −20°C), a C_{OS} with a drift of −310ppm/°C is called for in order to compensate the gain drift of the AD650. However, if that circuit should see an ambient temperature of +75°C, the C_{OS} cap would change the gain TC from approximately 0ppm to +310ppm/°C.

The temperature effects of the components described above are the same when the AD650 is configured for negative or bipolar input voltages, and for F/V conversion as well.

NONLINEARITY SPECIFICATION

The linearity error of the AD650 is specified by the end point method. That is, the error is expressed in terms of the deviation from the ideal voltage to frequency transfer relation after calibrating the converter at full scale and "zero". The nonlinearity will vary with the choice of one-shot capacitor and input resistor (see Figure 3). Verification of the linearity specification requires the availability of a switchable voltage source (or a DAC) having a linearity error below 20ppm, and the use of very long measurement intervals to minimize count uncertainties. Every AD650 is automatically tested for linearity, and it will not usually be necessary to perform this verification, which is both tedious and time consuming. If it is required to perform a nonlinearity test either as part of an incoming quality screening or as a final product evaluation, an automated "bench-top" tester would prove useful. Such a system based on the Analog Devices' LTS-2010 is described in Reference 2.

The voltage-to-frequency transfer relation is shown in Figure 9 with the nonlinearity exaggerated for clarity. The first step in determining nonlinearity is to connect the end points of the operating range (typically at 10mV and 10V) with a straight line. This straight line is then the ideal relationship which is desired from the circuit. The second step is to find the difference between this line and the actual response of the circuit at a few points between the end points – typically ten intermediate points will suffice. The difference between the actual and the ideal response is a frequency error measured in hertz. Finally, these frequency errors are normalized to the full scale frequency and expressed either as parts per million of full-scale (ppm) or parts per hundred of full scale (%). For example, on a 100kHz full scale, if the maximum frequency error is 5Hz, the nonlinearity would be specified as 50ppm or 0.005%. Typically on the 100kHz scale, the nonlinearity is positive and the maximum value occurs at about midscale (Figure 9a). At higher full scale frequencies, (500kHz to 1MHz), the nonlinearity becomes "S" shaped and the maximum value may be either positive or negative. Typically, on the 1MHz scale (R_{IN} = 16.9k, C_{OS} = 51pF) the nonlinearity is positive below about 2/3 scale and is negative above this point. This is shown graphically in Figure 9b.

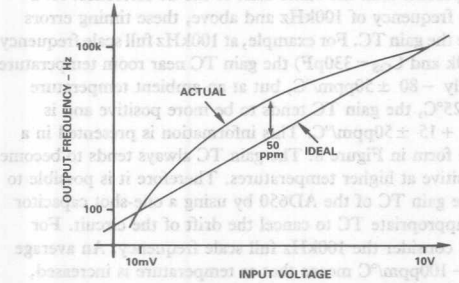


Figure 9a. Exaggerated Nonlinearity at 100kHz Full Scale

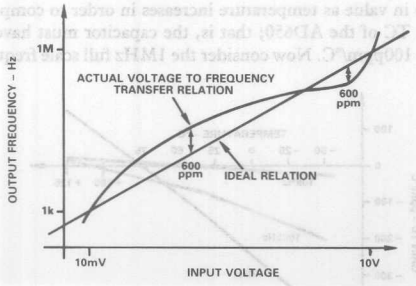


Figure 9b. Exaggerated Nonlinearity at 1MHz Full Scale

[2]"V-F Converters Demand Accurate Linearity Testing", by L. DeVito, (Electronic Design, March 4, 1982)

PSRR

The power supply rejection ratio is a specification of the change in gain of the AD650 as the power supply voltage is changed. The PSRR is expressed in units of parts-per-million change of the gain per percent change of the power supply – ppm/%. For example, consider a VFC with a 10 volt input applied and an output frequency of exactly 100kHz when the power supply potential is ±15 volts. Changing the power supply to ±12.5 volts is a 5 volt change out of 30 volts, or 16.7%. If the output frequency changes to 99.9kHz, the gain has changed 0.1% or 1000ppm. The PSRR is 1000ppm divided by 16.7% which equals 60ppm/%.

The PSRR of the AD650 is a function of the full scale operating frequency. At low full scale frequencies the PSRR is determined by the stability of the reference circuits in the device and can be very good. At higher frequencies there are dynamic errors which become more important than the static reference signals, and consequently the PSRR is not quite as good. The values of PSRR are typically 0 ±20ppm/% at 10kHz full scale frequency (R_{IN} = 40k, C_{OS} = 3300pF). At 100kHz (R_{IN} = 40k, C_{OS} = 330pF) the PSRR is typically +80 ±40ppm/%, and at 1MHz (R_{IN} = 16.9kΩ, C_{OS} = 51pF) the PSRR is +350 ±50ppm/%. This information is summarized graphically in Figure 10.

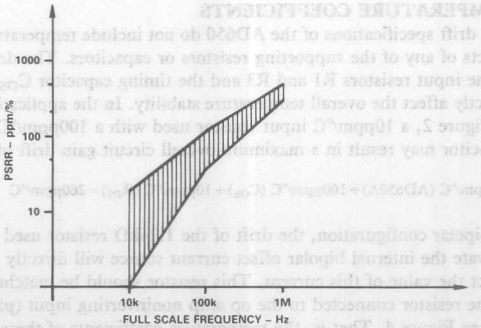


Figure 10. PSRR vs. Full Scale Frequency

OTHER CIRCUIT CONSIDERATIONS

The input amplifier connected to pins 1, 2 and 3 is not a standard operational amplifier. Rather, the design has been optimized for simplicity and high speed. The single largest difference between this amplifier and a normal op amp is the lack of an integrator (or level shift) stage. Consequently the voltage on the output (pin 1) must always be more positive than 2 volts below the inputs (pins 2 and 3). For example, in the F to V conversion mode, see Figure 6, the noninverting input of the op amp (pin 2) is grounded, which means that the output (pin 1) will not be able to go below −2 volts. Normal operation of the circuit as shown in the figure will never call for a negative voltage at the output but one may imagine an arrangement calling for a bipolar output voltage (say ±10 volts) by connecting an extra resistor from pin 3 to a positive voltage. This will not work.

Care should be taken under conditions where a high positive input voltage exists at or before power up. These situations can cause a latch up at the integrator output (pin 1). This is a non-destructive latch and, as such, normal operation can be restored by cycling the power supply. Latch up can be prevented by connecting two diodes (e.g., 1N914 or 1N4148) as shown in Figure 4 thereby preventing pin 1 from swinging below pin 2.

A second major difference is that the output will only sink 1mA to the negative supply. There is no pulldown stage at the output other than the 1mA current source used for the V to F conversion. The op amp will source a great deal of current from the positive supply, and it is internally protected by current limiting. The output of the op amp may be driven to within 3 volts of the positive supply when it is not sourcing external current. When sourcing 10mA the output voltage may be driven to within 6 volts of the positive supply.

A third difference between this op amp and a normal device is that the inverting input, pin 3, is bias current compensated and the noninverting input is not bias current compensated. The bias current at the inverting input is nominally zero, but may be as much as 20nA in either direction. The noninverting input typically has a bias current of 40nA that always flows into the node (an npn input transistor). Therefore, it is not possible to match input voltage drops due to bias currents by matching input resistors.

The op amp has provisions for trimming the input offset voltage. A potentiometer of 20kΩ is connected to pins 13 and 14 and the wiper is connected to the positive supply through a 250kΩ resistor. A potential of about 0.6 volt is established across the 250kΩ resistor, and the 3μA current is injected into the null pins. It is also possible to null the op amp offset voltage by using only one of the null pins and use a bipolar current either into or out of the null pin. The amount of current required will be very small – typically less than 3μA. This technique is shown in the applications section of this data sheet: the auto-zero circuit uses this technique.

The bipolar offset current is activated by connecting a 1.24kΩ resistor between pin 4 and the negative supply. The resultant current delivered to the op amp noninverting input is nominally 0.5mA and has a tolerance of ±10%. This current is then used to provide an offset voltage when pin 2 is tied to ground through a resistor. The 0.5mA which appears at pin 2 is also flowing through the 1.24kΩ resistor and this current may be measured by observing the voltage across the 1.24kΩ resistor. An external resistor is used to activate the bipolar offset current source to provide the lowest tolerance and temperature drift of the resultant offset voltage. It is possible to use other values of resistance between pin 4 and $-V_S$ to obtain a bipolar offset current different than 0.5mA. Figure 11 is a graph of the relationship between the bipolar offset current and the value of the resistor used to activate the source.

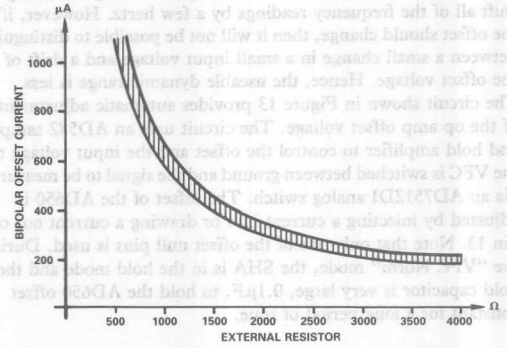


Figure 11. Bipolar Offset Current vs. External Resistor

APPLICATIONS

DIFFERENTIAL VOLTAGE-TO-FREQUENCY CONVERSION

The circuit of Figure 12 accepts a true floating differential input signal. The common mode input, V_{CM}, may be in the range +15 to −5 volts with respect to analog ground. The signal input, V_{IN}, may be ±5 volts with respect to the common mode input. Both inputs are low impedance: the source which drives the common mode input must supply the 0.5mA drawn by the bipolar offset current source and the source which drives the signal input must supply the integration current.

If less common mode voltage range is required, a lower voltage zener may be used. For example, if a 5 volt zener is used, the V_{CM} input may be in the range +10 to −5 volt. If the zener is not used at all, the common mode range will be ±5 volts with repect to analog ground. If no zener is used, the 10k pulldown resistor is not needed and the integrator output (pin 1) is connected directly to the comparator input (pin 9).

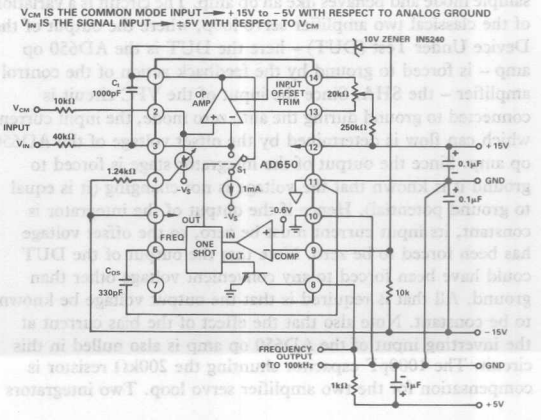


Figure 12. AD650 Differential Input

AUTO ZERO CIRCUIT

In order to exploit the full dynamic range of the AD650 VFC, very small input voltages will need to be converted. For example, a six decade dynamic range based on a full scale of 10 volts will require accurate measurement of signals down to 10μV. In these situations a well-controlled input offset voltage is imperative. A constant offset voltage will not affect dynamic range but simply shift all of the frequency readings by a few hertz. However, if the offset should change, then it will not be possible to distinguish between a small change in a small input voltage and a drift of the offset voltage. Hence, the useable dynamic range is less. The circuit shown in Figure 13 provides automatic adjustment of the op amp offset voltage. The circuit uses an AD582 sample and hold amplifier to control the offset and the input voltage to the VFC is switched between ground and the signal to be measured via an AD7512DI analog switch. The offset of the AD650 is adjusted by injecting a current into or drawing a current out of pin 13. Note that only one of the offset null pins is used. During the "VFC Norm" mode, the SHA is in the hold mode and the hold capacitor is very large, 0.1μF, to hold the AD650 offset constant for a long period of time.

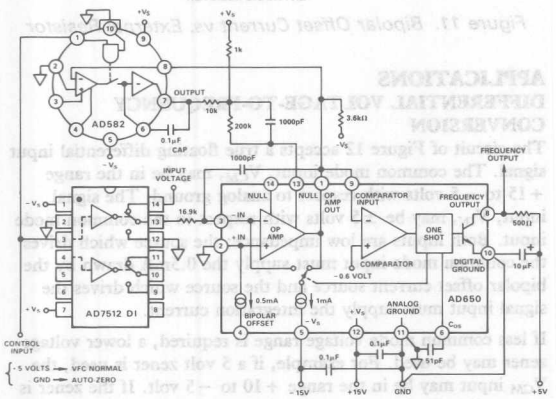


Figure 13. Auto-Zero Circuit for AD650 Voltage-to-Frequency Converter

When the circuit is in the "Auto Zero" mode the SHA is in sample mode and behaves like an op amp. The circuit is a variation of the classical two amplifier servo loop, where the output of the Device Under Test (DUT) – here the DUT is the AD650 op amp – is forced to ground by the feedback action of the control amplifier – the SHA. Since the input of the VFC circuit is connected to ground during the auto zero mode, the input current which can flow is determined by the offset voltage of the AD650 op amp. Since the output of the integrator stage is forced to ground it is known that the voltage is not changing (it is equal to ground potential). Hence if the output of the integrator is constant, its input current must be zero, so the offset voltage has been forced to be zero. Note that the output of the DUT could have been forced to any convenient voltage other than ground. All that is required is that the output voltage be known to be constant. Note also that the effect of the bias current at the inverting input of the AD650 op amp is also nulled in this circuit. The 1000pF capacitor shunting the 200kΩ resistor is compensation for the two amplifier servo loop. Two integrators in a loop requires a single zero for compensation. Note that the 3.6kΩ resistor from pin 1 of the AD650 to the negative supply is *not* part of the auto-zero circuit, but rather it is required for VFC operation at 1MHz.

PHASE LOCKED LOOP F/V CONVERSION

Although the F/V conversion technique shown in Figure 6 is quite accurate and uses only a few extra components, it is very limited in terms of signal frequency response and carrier feedthrough. If the carrier (or input) frequency changes instantaneously, the output cannot change very rapidly due to the integrator time constant formed by C_{INT} and R_{IN}. While it is possible to decrease the integrator time constant to provide faster settling of the F to V output voltage, the carrier feedthrough will then be larger. For signal frequency response in excess of 2kHz, a phase locked F/V conversion technique such as the one shown in Figure 14 is recommended.

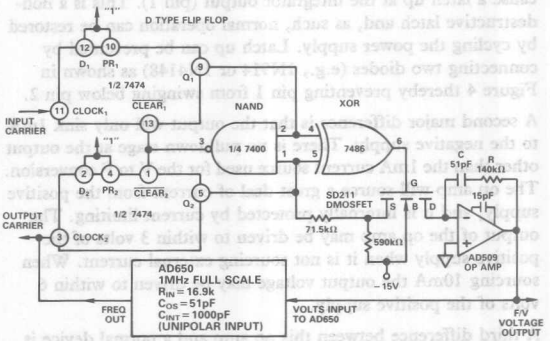


Figure 14. Phase Locked Loop F/V Conversion

In a phase locked loop circuit, the oscillator is driven to a frequency and phase equal to an input reference signal. In applications such as a synthesizer, the oscillator output frequency is first processed through a programmable "divide by N" before being applied to the phase detector as feedback. Here the oscillator frequency is forced to be equal to "N times" the reference frequency and it is this frequency output which is the desired output signal and not a voltage. In this case, the AD650 offers compact size and wide dynamic range.

In signal recovery applications of a PLL, the desired output signal is the voltage applied to the oscillator. In these situations a linear relationship between the input frequency and the output voltage is desired; the AD650 makes a superb oscillator for FM demodulation. The wide dynamic range and outstanding linearity of the AD650 VFC allow simple embodiment of high performance analog signal isolation or telemetry systems. The circuit shown in Figure 14 uses a digital phase detector which also provides proper feedback in the event of unequal frequencies. Such phase-frequency detectors (PFD's) are available in integrated form. For a full discussion of phase lock loop circuits see Reference 3.

An analysis of this circuit must begin at the 7474 dual D flip flop. When the input carrier matches the output carrier in both phase and frequency, the Q outputs of the flip flops will rise at exactly the same time. With two zero's, then two one's on the inputs of the exclusive or (XOR) gate, the output will remain low keeping the DMOS FET switched off. Also, the NAND gate will go low resetting the flip-flops to zero. Throughout the

[3]"Phase lock Techniques", by F.M. Gardner, 2nd Edition, 1979, John Wiley and Sons.

entire cycle just described, the DMOS integrator gate remained off, allowing the voltage at the integrator output to remain unchanged from the previous cycle. However, if the input carrier leads the output carrier by a few degrees, the XOR gate will be turned on for the small time span that the two signals are mismatched. Since Q_2 will be low during the mismatch time, a negative current will be fed into the integrator, causing its output voltage to rise. This in turn will increase the frequency of the AD650 slightly, driving the system towards synchronization. In a similar manner, if the input carrier lags the output carrier, the integrator will be forced down slightly to synchronize the two signals.

Using a mathematical approach, the $\pm 25\mu A$ pulses from the phase detector are incorporated into the phase detector gain, K_d.

$$K_d = \frac{25\mu A}{2\pi} = 4 \times 10^{-6} \quad amperes/radian \tag{9}$$

Also, the V/F converter is configured to produce 1MHz in response to a 10 volt input, so its gain K_o is:

$$K_o = \frac{2\pi \times 1 \times 10^6 Hz}{10V} = 6.3 \times 10^5 \quad \frac{radians}{volt \cdot sec} \tag{10}$$

The dynamics of the phase relationship between the input and output signals can be characterized as a second order system with natural frequency ω_n:

$$\omega_n = \sqrt{\frac{K_o K_d}{C}} \tag{11}$$

and damping factor

$$\zeta = \frac{R\sqrt{C\,K_o K_d}}{2} \tag{12}$$

For the values shown in Figure 14, these relations simplify to a natural frequency of 35kHz with a damping factor of 0.8.

For those desiring a simple approach to determining component values for other PLL frequencies and VFC full scale voltage, the following cookbook steps can be used:

1. Determine K_o (in units of radians per volt second) from the maximum input carrier frequency F_{max} (in hertz) and the maximum output voltage V_{max}.
$$K_o = \frac{2\pi \times F_{max}}{V_{max}} \tag{13}$$
2. Calculate a value for C based upon the desired loop bandwidth, f_n. Note that this is the desired frequency range of the output signal. The loop bandwidth (f_n) is *not* the maximum carrier frequency (f_{max}): the signal may be very narrow even though it is transmitted over a 1MHz carrier.
$$C = \frac{K_o}{f_n^2} \cdot 1 \times 10^{-7} \frac{V \cdot F}{Rad \cdot sec} \quad \begin{matrix} C \text{ units FARADS} \\ f_n \text{ units HERTZ} \\ K_o \text{ units RAD/VOLT•SEC} \end{matrix} \tag{14}$$
3. Calculate R to yield a damping factor of approximately 0.8 using this equation:
$$R = \frac{f_n}{K_o} \cdot 2.5 \times 10^6 \frac{Rad \cdot \Omega}{V} \quad \begin{matrix} R \text{ units OHMS} \\ f_n \text{ units HERTZ} \\ K_o \text{ units RAD/VOLT•SEC} \end{matrix} \tag{15}$$

If in actual operation the PLL overshoots or hunts excessively before reaching a final value, the damping factor may be raised by increasing the value of R. Conversely, if the PLL is overdamped, a smaller value of R should be used.

PLL PERFORMANCE

The performance of the PLL circuit is demonstrated by the system shown in Figure 15; an analog signal is converted into a frequency, and then this frequency is converted back into an analog voltage by the PLL.

The source of the frequency input signal used to drive the PLL is an AD650 with two separate inputs: one for dc to set the carrier frequency, and one for ac to establish a modulation. Note how the summing junction input to the AD650 allows such flexibility. The output frequency is then relayed to the

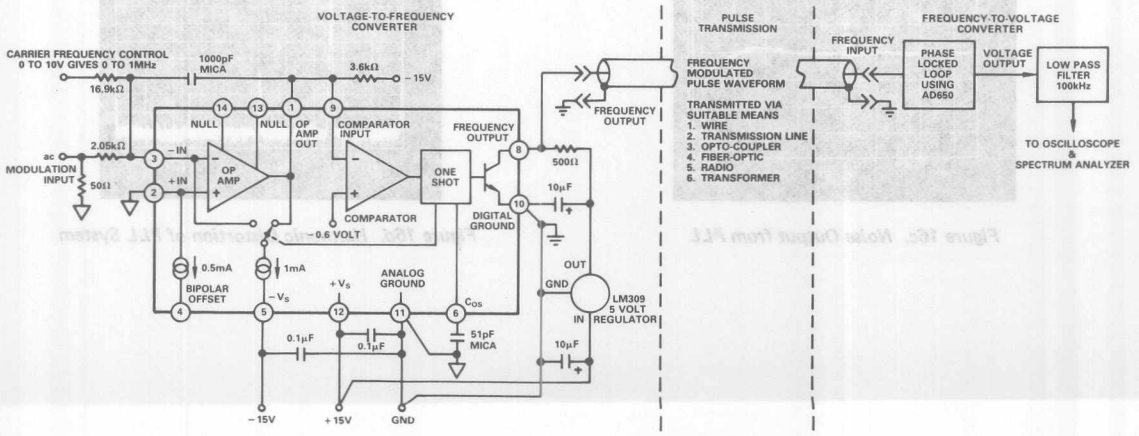


Figure 15.

PLL via a jumper cable. The signal at this point is a 5 volt digital pulse train and as such may be transmitted in any fashion suitable to the application at hand. For example, galvanic isolation is achieved with a simple transformer or opto-isolator; extremely high voltage isolation or transmission through severe RF environments can be accomplished with a fiber-optic link; telemetry can be accomplished with a radio link. The actual method of conveying the pulses is not crucial to the system performance. The PLL is the circuit shown in Figure 14, and the filter shown on the output signal is simply to attenuate carrier feedthrough to allow easy interpretation of the signal with an oscilloscope and spectrum analyzer.

The step response of the system is shown in Figure 16a. The signal output is swinging between 5 volts and 10 volts, for an input step of 500kHz to 1MHz. Note that the AD650 is actually overshooting to 1.1MHz and the response remains well controlled. Note the slight irregularity during the transition: this is caused by cycleslipping during the slew where feedback is lost temporarily and the PLL actually loses phase lock. The frequency response of the system when driven with sinewave excitation is shown in Figure 16b. Here the output level is set to 2 volts peak to peak, and the carrier is 800kHz. Note that the −3dB bandwidth is about 70kHz, which is consistent with a damping factor of 0.8 and a natural frequency of 35kHz[4]. When an unmodulated carrier is applied to the PLL, the noise that appears at the output determines the dynamic range of the system. The spectrum of the noise at the output of the PLL is shown in Figure 16c. By comparing this with Figure 16b, the dynamic range of the system is seen to be 80dB. The harmonic distortion of the system is shown in Figure 16d. The output is a 2V p-p sinewave at 5kHz, and the amplitude of the first harmonic is seen to be 48dB below the fundamental. The harmonic distortion can be improved to the level of 60dB by reducing the amplitude of the modulation, but this is at the expense of dynamic range since the intensity of the noise floor remains constant.

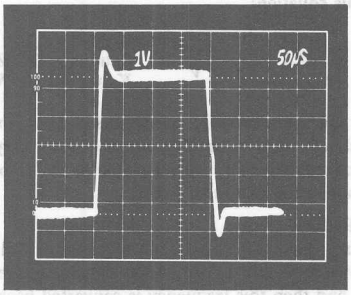


Figure 16a. Step Response

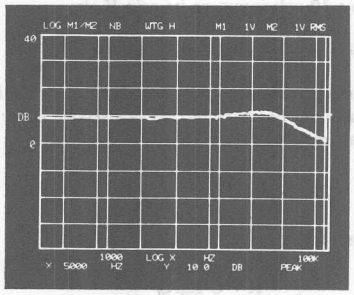


Figure 16b. Frequency Response

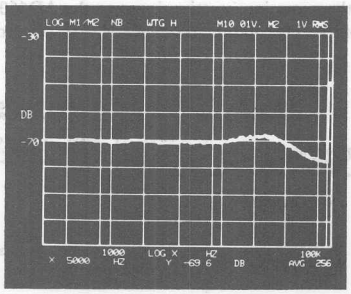


Figure 16c. Noise Output from PLL

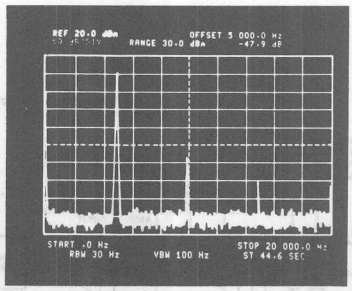


Figure 16d. Harmonic Distortion of PLL System

[4]See page 13 of reference 3.

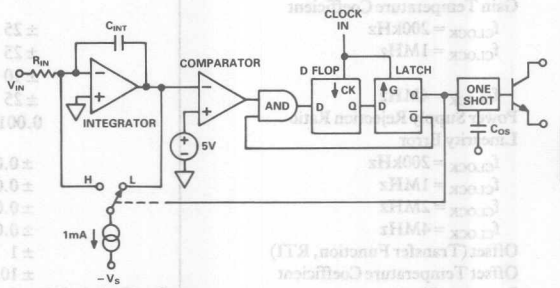
Monolithic Synchronous Voltage-to-Frequency Converter

AD652

FEATURES

- Full-Scale Frequency (Up to 2MHz) Set by External System Clock
- Extremely Low Linearity Error (0.005% max at 1MHz FS, 0.02% max at 2MHz FS)
- No Critical External Components Required
- Accurate 5V Reference Voltage
- Low Drift (25ppm/°C max)
- Dual or Single Supply Operation
- Voltage or Current Input
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD652 Synchronous Voltage-to-Frequency Converter (SVFC) is a powerful building block for precision analog-to-digital conversion, offering typical nonlinearity of 0.002% (0.005% maximum) at a 100kHz output frequency. The inherent monotonicity of the transfer function and wide range of clock frequencies allows the conversion time and resolution to be optimized for specific applications.

The AD652 uses a variation of the popular charge-balancing technique to perform the conversion function. The AD652 uses an external clock to define the full-scale output frequency, rather than relying on the stability of an external capacitor. The result is a more stable, more linear transfer function, with significant application benefits in both single- and multi-channel systems.

Gain drift is minimized using a precision low-drift reference and low-TC on-chip thin-film scaling resistors. Furthermore, the initial gain error is reduced to less than 0.5% by the use of laser-wafer-trimming.

The analog and digital sections of the AD652 have been designed to allow operation from a single-ended power source, simplifying its use with isolated power supplies.

The AD652 is available in five performance grades. The 20-pin PLCC packaged JP and KP grades are specified for operation over the 0 to +70°C commercial temperature range. The 16-pin cerdip-packaged AQ and BQ grades are specified for operation over the −40°C to +85°C industrial temperature range, and the AD652SQ is available for operation over the full −55°C to +125°C extended temperature range.

PRODUCT HIGHLIGHTS

1. The use of an external clock to set the full-scale frequency allows the AD652 to achieve linearity and stability far superior to other monolithic VFCs. By using the same clock to drive the AD652 and (through a suitable divider) also set the counting period, conversion accuracy is maintained independent of variations in clock frequency.
2. The AD652 Synchronous VFC requires only a single external component (a noncritical integrator capacitor) for operation.
3. The AD652 includes a buffered, accurate 5V reference which is available to the user.
4. The clock input of the AD652 is TTL and CMOS compatible and can also be driven by sources referred to the negative power supply. The flexible open-collector output stage provides sufficient current sinking capability for TTL and CMOS logic, as well as for optical couplers and pulse transformers. A capacitor-programmable one-shot is provided for selection of optimum output pulse width for power reduction.
5. The AD652 can also be configured for use as a synchronous F/V converter for isolated analog signal transmission.
6. The AD652 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD652/883B data sheet for detailed specifications.

AD652—SPECIFICATIONS (typical @ T_A = +25°C, V_S = ±15V, unless otherwise noted)

Parameter	AD652JP/AQ/SQ Min	AD652JP/AQ/SQ Typ	AD652JP/AQ/SQ Max	AD652KP/BQ Min	AD652KP/BQ Typ	AD652KP/BQ Max	Units
VOLTAGE-TO-FREQUENCY MODE							
Gain Error							
f_{CLOCK} = 200kHz		±0.5	±1		±0.25	±0.5	%
f_{CLOCK} = 1MHz		±0.5	±1		±0.25	±0.5	%
f_{CLOCK} = 4MHz		±0.5	±1.5		±0.25	±0.75	%
Gain Temperature Coefficient							
f_{CLOCK} = 200kHz		±25	±50		±15	±25	ppm/°C
f_{CLOCK} = 1MHz		±25	±50		±15	±25	ppm/°C
		±10	±50		±10	±30	ppm/°C[1]
f_{CLOCK} = 4MHz		±25	±75		±15	±50	ppm/°C
Power Supply Rejection Ratio		0.001	0.01		0.001	0.01	%/V
Linearity Error							
f_{CLOCK} = 200kHz		±0.002	±0.02		±0.002	±0.005	%
f_{CLOCK} = 1MHz		±0.002	±0.02		±0.002	±0.005	%
f_{CLOCK} = 2MHz		±0.01	±0.02		±0.002	±0.005	%
f_{CLOCK} = 4MHz		±0.02	±0.05		±0.01	±0.02	%
Offset (Transfer Function, RTI)		±1	±3		±1	±2	mV
Offset Temperature Coefficient		±10	±50		±10	±25	µV/°C
Response Time	One Period of New Output Frequency Plus One Clock Period.						
FREQUENCY-TO-VOLTAGE MODE							
Gain Error							
f_{IN} = 100kHz FS		±0.5	±1		±0.25	±0.5	%
Linearity Error							
f_{IN} = 100kHz FS		±0.002	±0.02		±0.002	±0.01	%
INPUT RESISTORS							
Cerdip (Figure 1a.) (0 to +10V FS Range)	19.8	20	20.2	19.8	20	20.2	kΩ
PLCC (Figure 1b.)							
Pin 8 to Pin 7	9.9	10	10.1	9.9	10	10.1	kΩ
Pin 7 to Pin 5 (0 to +5V FS Range)	9.9	10	10.1	9.9	10	10.1	kΩ
Pin 8 to Pin 5 (0 to +10V FS Range)	19.8	20	20.2	19.8	20	20.2	kΩ
Pin 9 to Pin 5 (0 to +8V FS Range)	15.8	16	16.2	15.8	16	16.2	kΩ
Pin 10 to Pin 5 (Auxiliary Input)	19.8	20	20.2	19.8	20	20.2	kΩ
Temperature Coefficient (All)		±50	±100		±50	±100	ppm/°C
INTEGRATOR OP AMP							
Input Bias Current							
Inverting Input (Pin 5)		±5	±20		±5	±20	nA
Noninverting Input (Pin 6)		20	50		20	50	nA
Input Offset Current		20	70		20	70	nA
Input Offset Current Drift		1	3		1	2	nA/°C
Input Offset Voltage		±1	±3		±1	±2	mV
Input Offset Voltage Drift		±10	±25		±10	±15	µV/°C
Open Loop Gain		86			86		dB
Common-Mode Input Range	$-V_S+5$		$+V_S-5$	$-V_S+5$		$+V_S-5$	V
CMRR	80			80			dB
Bandwidth	14	95		14	95		MHz
Output Voltage Range (Referred to Pin 6, R_1 >= 5k)	−1		$(+V_S-4)$	−1		$(+V_S-4)$	V
COMPARATOR							
Input Bias Current		0.5	5		0.5	5	µA
Common-Mode Voltage	$-V_S+4$		$+V_S-4$	$-V_S+4$		$+V_S-4$	V
CLOCK INPUT							
Maximum Frequency	4	5		4	5		MHz
Threshold Voltage (Referred to Pin 12)		1.2			1.2		V
T_{min}-T_{max}	0.8		2.0	0.8		2.0	V
Input Current							
$(-V_S<V_{CLK}<+V_S)$		5	20		5	20	µA
Voltage Range	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Rise Time			2			2	µs

Parameter	AD652JP/AQ/SQ Min	Typ	Max	AD652KP/BQ Min	Typ	Max	Units
OUTPUT STAGE							
V_{OL} (I_{OUT} = 10mA)			**0.4**			**0.4**	V
I_{OL}							
V_{OL}<0.8V			**15**			**15**	mA
V_{OL}<0.4V, T_{min}-T_{max}			**8**			**8**	mA
I_{OH} (Off Leakage)		0.01	**10**		0.01	**10**	µA
Delay Time, Positive Clock Edge to Output Pulse	**150**	200	**250**	**150**	200	**250**	ns
Fall Time (Load = 500pF and I_{SINK} = 5mA)		100			100		ns
Output Capacitance		5			5		pF
OUTPUT ONE-SHOT							
Pulse Width							
C_{OS} = 300pF	**1**	1.5	**2**	**1**	1.5	**2**	µs
C_{OS} = 1000pF	**4**	5	**6**	**4**	5	**6**	µs
REFERENCE OUTPUT							
Voltage	**4.950**	5.0	**5.050**	**4.975**	5.0	**5.025**	V
Drift			**100**			**50**	ppm/°C
Output Current							
Source	**10**			**10**			mA
Sink	**100**	500		**100**	500		µA
Power Supply Rejection							
(Supply Range = ±12.5V to ±17.5V)			0.015			0.015	%/V
Output Impedance (Sourcing Current)		0.3	**2**		0.3	**2**	Ω
POWER SUPPLY							
Rated Voltage		±15			±15		V
Operating Range							
Dual Supplies	±6	±15	±18	±6	±15	±18	V
Single Supply ($-V_S$ = 0)	+12		+36	+12		+36	V
Quiescent Current		±11	**±15**		±11	**±15**	mA
Digital Common	$-V_S$		$+V_S-4$	$-V_S$		$+V_S-4$	V
Analog Common	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
TEMPERATURE RANGE							
Specified Performance							
JP, KP Grade	0		+70	0		+70	°C
AQ, BQ Grade	−40		+85	−40		+85	°C
SQ Grade	−55		+125				°C

NOTES
[1]Referred to internal V_{REF}. In PLCC package, tested on 10V input range only.
Specifications in **boldface** are 100% tested at final test and are used to measure outgoing quality levels.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage $+V_S$ to $-V_S$ 36V
Maximum Input Voltage (Figure 6) 36V
Maximum Output Current (Open Collector Output) . . 50mA
Amplifier Short Circuit to Ground . . . . . Indefinite
Storage Temperature Range: Cerdip . . . . −65°C to +150°C
PLCC . . . . −65°C to +150°C

DEFINITIONS OF SPECIFICATIONS

GAIN ERROR – The gain of a voltage-to-frequency converter is that scale factor setting that provides the nominal conversion relationship, e.g. 1MHz full scale. The "gain error" is the difference in slope between the actual and ideal transfer functions for the V-F converter.

LINEARITY ERROR – The "linearity error" of a V-F is the deviation of the actual transfer function from a straight line passing through the endpoints of the transfer function.

GAIN TEMPERATURE COEFFICIENT – The gain temperature coefficient is the rate of change in full-scale frequency as a function of the temperature from +25°C to T_{min} or T_{max}.

Part Number[1]	Gain Drift ppm/°C 100 kHz	1 MHz Linearity %	Specified Temperature Range °C	Package Options[2]
AD652JP	50 max	0.02 max	0 to +70	PLCC (P-20A)
AD652KP	25 max	0.005 max	0 to +70	PLCC (P-20A)
AD652AQ	50 max	0.02 max	−40 to +85	Cerdip (Q-16)
AD652BQ	25 max	0.005 max	−40 to +85	Cerdip (Q-16)
AD652SQ	50 max	0.02 max	−55 to +125	Cerdip (Q-16)

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD652/883 data sheet.
[2]P = Plastic Leaded Chip Carrier; Q = Cerdip; E = Leadless Ceramic Chip Carrier. For outline information see Package Information section.

PIN	"Q" CERDIP	"P" PLCC
1	$+V_S$	NC
2	TRIM	$+V_S$
3	TRIM	NC
4	OP AMP OUT	OP AMP OUT
5	OP AMP "−"	OP AMP "−"
6	OP AMP "+"	OP AMP "+"
7	10 VOLT INPUT	5 VOLT INPUT
8	$-V_S$	10 VOLT INPUT
9	C_{OS}	8 VOLT INPUT
10	CLOCK INPUT	OPTIONAL 10V INPUT
11	FREQ OUT	$-V_S$
12	DIGITAL GND	C_{OS}
13	ANALOG GND	CLOCK INPUT
14	COMP "−"	FREQ OUT
15	COMP "+"	DIGITAL GROUND
16	COMP REF	ANALOG GND
17		COMP "−"
18		COMP "+"
19		NC
20		COMP REF

THEORY OF OPERATION

A synchronous VFC is similar to other voltage-to-frequency converters in that an integrator is used to perform a charge-balance of the input signal with an internal reference current. However, rather than using a one-shot as the primary timing element which requires a high quality and low drift capacitor, a synchronous voltage-to-frequency converter (SVFC) uses an external clock; this allows the designer to determine the system stability and drift based upon the external clock selected. A crystal oscillator may also be used if desired.

The SVFC architecture provides other system advantages besides low drift. If the output frequency is measured by counting pulses gated to a signal which is derived from the clock, the clock stability is unimportant and the device simply performs as a voltage controlled frequency divider, producing a high resolution A/D. If a large number of inputs must be monitored simultaneously in a system, the controlled timing relationship between the frequency output pulses and the user supplied clock greatly simplifies this signal acquisition. Also, if the clock signal is provided by a VFC, then the output frequency of the SVFC will be proportional to the product of the two input voltages. Hence, multiplication and A-to-D conversion on two signals are performed simultaneously.

The pinouts of the AD652 SVFC are shown in Figure 1. A block diagram of the device configured as a SVFC, along with various system waveforms, is shown in Figure 2.

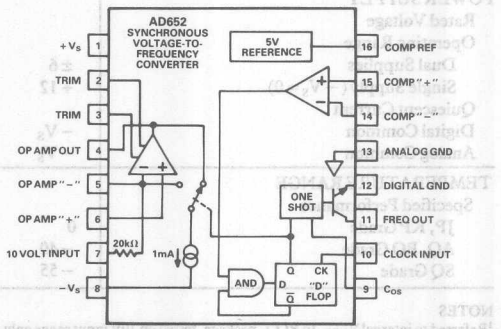


Figure 1a. AD652 Cerdip Pin Configuration

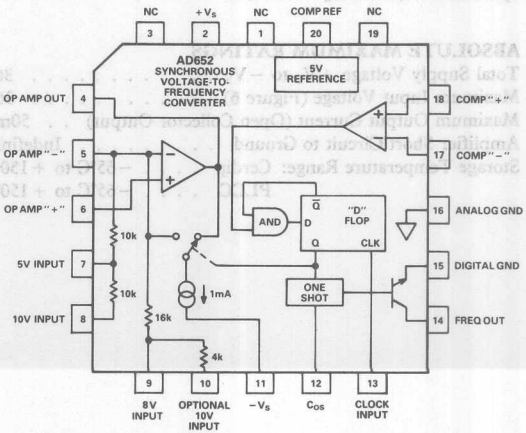


Figure 1b. AD652 PLCC Pin Configuration

Figure 2 shows the typical up-and-down ramp integrator output of a charge-balance VFC. After the integrator output has crossed the comparator threshold and the output of the AND gate has gone high, nothing happens until a negative edge of the clock comes along to transfer the information to the output of the D-FLOP. At this point, the clock level is low, so the latch does not change state. When the clock returns high, the latch output goes high and drives the switch to reset the integrator. At the same time the latch drives the AND gate to a low output state. On the very next negative edge of the clock the low output state of the AND gate is transferred to the output of the D-FLOP and then when the clock returns high, the latch output goes low and drives the switch back into the Integrate Mode. At the same time the latch drives the AND gate to a mode where it will truthfully relay the information presented to it by the comparator.

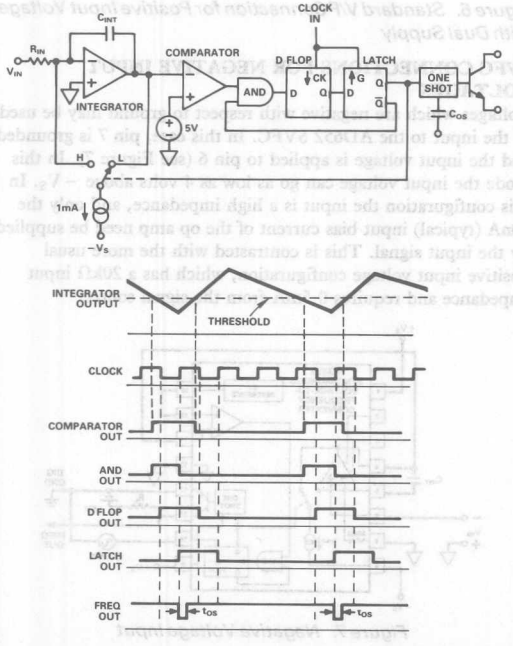


Figure 2. AD652 Block Diagram and System Waveforms

Since the reset pulses applied to the integrator are exactly one clock period long, the only place where drift can occur is in a variation of the symmetry of the switching speed with temperature. Since each reset pulse is identical to every other, the AD652 SVFC produces a very linear voltage to frequency transfer relation. Also, since all of the reset pulses are gated by the clock, there are no problems with dielectric absorption causing the duration of a reset pulse to be influenced by the length of time since the last reset.

Referring to Figure 2, it can be seen that the period between output pulses is constrained to be an exact multiple of the clock period. Consider an input current of exactly one quarter of the value of the reference current. In order to achieve a charge balance, the output frequency will equal the clock frequency divided by four; one clock period for reset and three clock periods of integrate. This is shown in Figure 3. If the input current is increased by a very small amount, the output frequency should also increase by a very small amount. Initially, however, no output change is observed for a very small increase in the input current. The output frequency continues to run at one quarter of the clock, delivering an average of 250μA to the summing junction. Since the input current is slightly larger than this, charge accumulates in the integrator and the sawtooth signal starts to drift downward. As the integrator sawtooth drifts down, the comparator threshold is crossed earlier and earlier in each successive cycle, until finally, a whole cycle is lost. When the cycle is lost, the Integrate Phase lasts for two periods of the clock instead of the usual three periods. Thus, among a long string of divide-by-four's an occasional divide-by-three occurs; the average of the output frequency is very close to one quarter of the clock, but the instantaneous frequency can be very different.

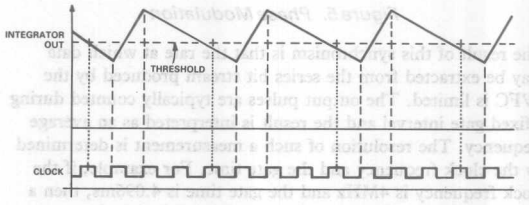


Figure 3. Integrator Output for $I_{IN} = 250\mu A$

Because of this, it is very difficult to observe the waveform on an oscilloscope. During all of this time, the signal at the output of the integrator is a sawtooth wave with an envelope which is also a sawtooth. This is shown in Figure 4.

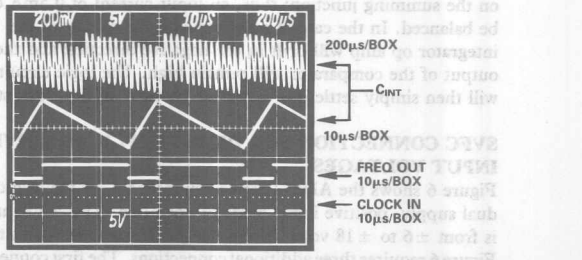


Figure 4. Integrator Output for I_{IN} Slightly Greater than 250μA

Another way to view this is that the output is a frequency of approximately one quarter of the clock that has been phase modulated. A constant frequency can be thought of as accumulating phase linearly with time at a rate equal to $2\pi f$ radians per second. Hence, the average output frequency which is slightly in excess of a quarter of the clock will require phase accumulation at a certain rate. However, since the SVFC is running at exactly one quarter of the clock, it will not accumulate enough phase (see Figure 5). When the difference between the required phase (average frequency) and the actual phase equals 2π, a step in phase is taken where the deficit is made up instantaneously. The output frequency is then a steady carrier which has been phase modulated by a sawtooth signal (see Figure 5). The period of the sawtooth phase modulation is the time required to accumulate a 2π difference in phase between the required average

frequency and one quarter of the clock frequency. The amplitude of the sawtooth phase modulation is 2π.

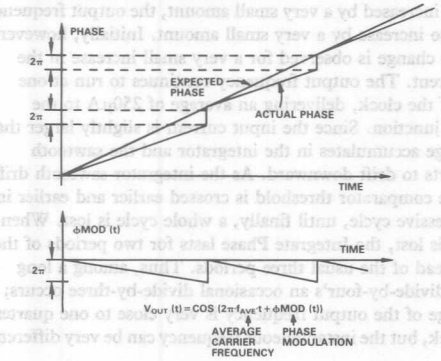


Figure 5. Phase Modulation

The result of this synchronism is that the rate at which data may be extracted from the series bit stream produced by the SVFC is limited. The output pulses are typically counted during a fixed gate interval and the result is interpreted as an average frequency. The resolution of such a measurement is determined by the clock frequency and the gate time. For example, if the clock frequency is 4MHz and the gate time is 4.096ms, then a maximum count of 8,192 is produced by a full-scale frequency of 2MHz. Thus, the resolution is 13 bits.

OVERRANGE

Since each reset pulse is only one clock period in length, the full-scale output frequency is equal to one-half the clock frequency. At full scale the current steering switch spends half of the time on the summing junction; thus, an input current of 0.5mA can be balanced. In the case of an overrange, the output of the integrator op amp will drift in the negative direction and the output of the comparator will remain high. The logic circuits will then simply settle into a "divide-by-two" of the clock state.

SVFC CONNECTION FOR DUAL SUPPLY, POSITIVE INPUT VOLTAGES

Figure 6 shows the AD652 connection scheme for the traditional dual supply, positive input mode of operation. The $\pm V_S$ range is from ± 6 to ± 18 volts. When $+V_S$ is lower than 9.0 volts, Figure 6 requires three additional connections. The first connection is to short pin 13 to pin 8 (Analog Ground to $-V_S$) and add a pull-up resistor to $+V_S$ (as shown in Figure 15). The pull-up resistor is determined by the following equation:

$$R_{PULLUP} = \frac{2\,V_S - 5V}{500\mu A}$$

These connections will ensure proper operation of the 5V reference. Tie pin 16 to pin 6 (as shown in Figure 15) to ensure that the integrator output ramps down far enough to trip the comparator.

The cerdip packaged AD652 accepts either a 0 to 10V or 0 to 0.5mA full-scale input signal. The temperature drift of the AD652 is specified for a 0 to 10V input range using the internal 20kΩ resistor. If a current input is used, the gain drift will be degraded by a maximum of 100ppm/°C (the TC of the 20kΩ resistor). If an external resistor is connected to pin 5 to establish a different input voltage range, drift will be induced to the extent that the external resistor's TC differs from the TC of the internal resistor. The external resistor used to establish a different input voltage range should be selected as to provide a full-scale current of 0.5mA (i.e., 10kΩ for 0 to 5V).

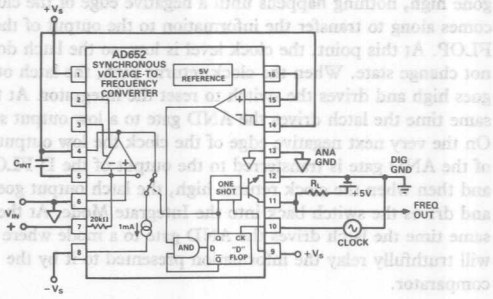


Figure 6. Standard V/F Connection for Positive Input Voltage with Dual Supply

SVFC CONNECTIONS FOR NEGATIVE INPUT VOLTAGES

Voltages which are negative with respect to ground may be used as the input to the AD652 SVFC. In this case, pin 7 is grounded and the input voltage is applied to pin 6 (see Figure 7). In this mode the input voltage can go as low as 4 volts above $-V_S$. In this configuration the input is a high impedance, and only the 20nA (typical) input bias current of the op amp need be supplied by the input signal. This is contrasted with the more usual positive input voltage configuration, which has a 20kΩ input impedance and requires 0.5mA from the signal source.

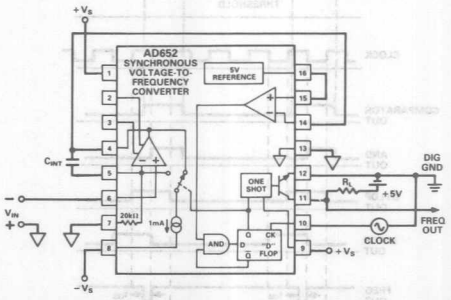


Figure 7. Negative Voltage Input

SVFC CONNECTION FOR BIPOLAR INPUT VOLTAGES

A bipolar input voltage of $\pm 5V$ can be accommodated by injecting a 250μA current into pin 5. This is shown in Figure 8a. A $-5V$ signal will then provide a zero sum current at the integrator summing junction which will result in a zero output frequency, while a $+5V$ signal will provide a 0.5mA (full-scale) sum current which will result in the full-scale output frequency.

The use of an external resistor to inject the offset current will have some effect on the bipolar offset temperature coefficient. The ideal transfer curve with bipolar inputs is shown in Figure 8b. The user actually has four options to use in injecting the bipolar offset current into the inverting input of the op amp: 1) use an external resistor for R_{OS} and the internal 20k resistor for R_{IN} (as shown in Figure 8a); 2) use the internal 20k resistor as R_{OS} and an external R_{IN}; 3) use two external resistors; 4) use two internal resistors for R_{IN} and R_{OS} (available on PLCC version only).

Option #4 provides the closest to the ideal transfer function as diagrammed in Figure 8b. Figure 8c shows the effects on the transfer relation of the other three options. In the first case, the slope of the transfer function is unchanged with temperature. However, V_{ZERO} (the input voltage required to produce an output frequency of 0Hz) and F_{ZERO} (the output frequency when V_{IN} = 0V) changes as the transfer function is displaced parallel to the voltage axis with temperature. In the second case, F_{ZERO} remains constant, but V_{ZERO} changes as the transfer function rotates about F_{ZERO} with temperature changes. In the third case, with two external resistors, the V_{ZERO} point remains invariant while the slope and offset of the transfer function change with temperature. If selecting this third option, the user should select low drift, matched resistors.

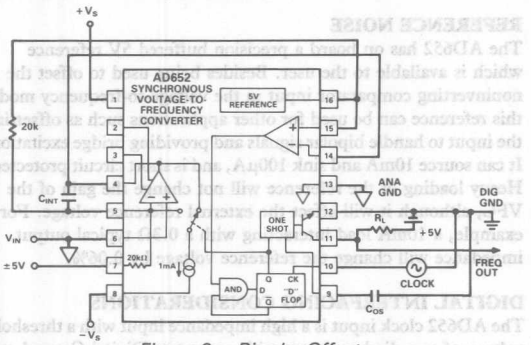


Figure 8a. Bipolar Offset

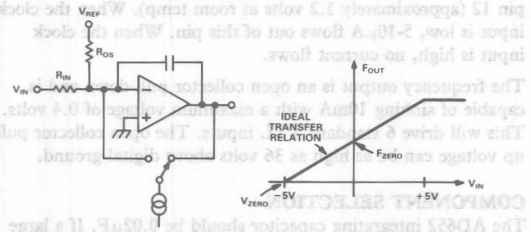


Figure 8b. Ideal Bipolar Input Transver Curve Over Temperature

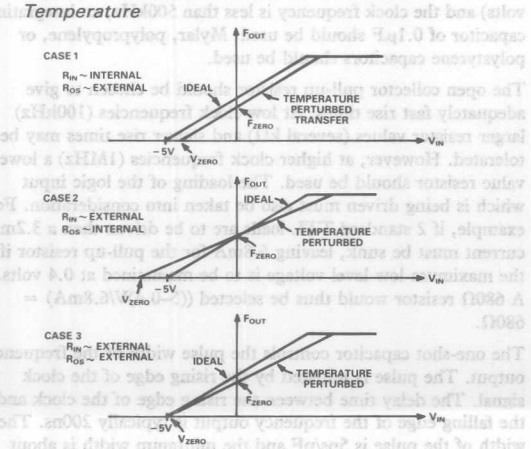
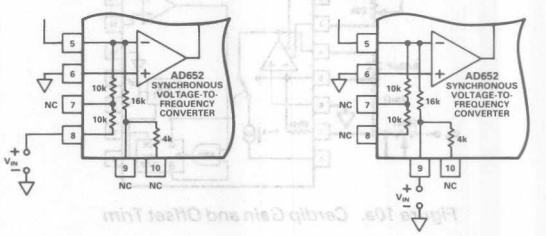


Figure 8c. Actual Bipolar Input Transfer Over Temperature

PLCC CONNECTIONS

The PLCC packaged AD652 offers additional input resistors not found on the cerdip-packaged device. These resistors provide the user with additional input voltage ranges. Besides the 10V range available using the on-chip resistor in the cerdip part, the PLCC device also offers 8V and 5V ranges. Figures 9a-9c show the proper connections for these ranges with positive input voltages. For negative input voltages, the appropriate resistor should be tied to analog ground and the input voltage should be applied to pin 6, the "+" input of the op amp.

Bipolar input voltages can be accommodated by injecting a 250μA into pin 5 with the use of the 5V reference and the input resistors. For ±5V or ±2.5V range the reference output, pin 20, should be tied to pin 10. The input signal should then be applied to pin 8 for a ±5V signal and pin 7 for a ±2.5V signal. The input connections for a ±5V range are shown in Figure 9d. For a ±4V range, the input signal should be applied to pin 9, and pin 20 should be connected to pin 8.



a. PLCC 0 to +10V Input *b. PLCC 0 to +8V Input*

c. PLCC 0 to +5V Input *d. PLCC ±5V Input*

Figure 9.

GAIN AND OFFSET CALIBRATION

The gain error of the AD652 is laser trimmed to within ±0.5%. If higher accuracy is required, the internal 20kΩ resistor must be shunted with a 2MΩ resistor to produce a parallel equivalent which is 1% lower in value than the nominal 20kΩ. Full scale adjustment is then accomplished using a 500Ω series trimmer. See Figures 10a and 10b. When negative input voltages are used, this 500Ω trimmer will be tied to ground and pin 6 will be the input pin.

This gain trim should be done with an input voltage of 9V, and the output frequency should be adjusted to exactly 45% of the clock frequency. Since the device settles into a divide-by-two mode for an input overrange condition, adjusting the gain with a 10V input is impractical; the output frequency would be exactly one-half the clock frequency if the gain were too high and would not change with adjustment until the exact proper scale factor was achieved. Hence, the gain adjustment should be done with a 9V input.

scheme shown in Figures 10a for the cerdip packaged device and Figure 10b for the PLCC packaged device. One way of trimming the offset is by grounding pin 7 (8) of the cerdip (PLCC) packaged device and observing the waveform at pin 4. If the offset voltage of the op amp is positive, then the integrator will have saturated and the voltage will be at the positive rail. If the offset voltage is negative, then there will be a small effective input current that will cause the AD652 to oscillate and a sawtooth waveform will be observed at pin 4. The trimpot should be adjusted until the downward slope of this sawtooth becomes very slow, down to a frequency of 1Hz or less. In an analog-to-digital conversion application, an easier way to trim the offset is to apply a small input voltage, such as 0.01% of the full-scale voltage, and adjust the trimpot until the correct digital output is reached.

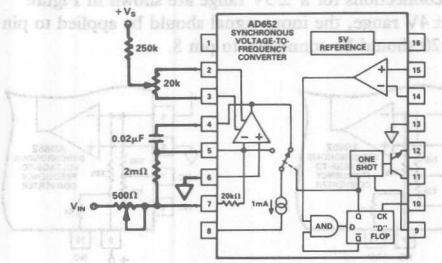


Figure 10a. Cerdip Gain and Offset Trim

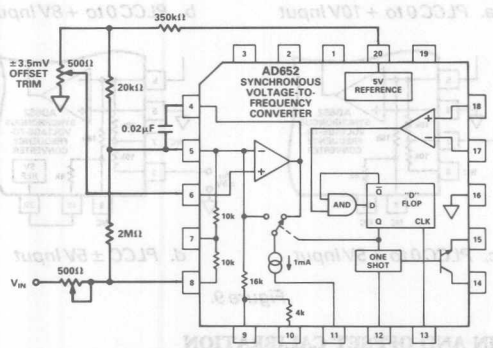


Figure 10b. PLCC Gain and Offset Trim

GAIN PERFORMANCE

The AD652 gain error is specified as the difference in slope between the actual and the ideal transfer function over the full-scale frequency range. Figure 11 shows a plot of the typical gain error changes vs. the clock input frequency, normalized to 100kHz. If after using the AD652 with a full-scale clock frequency of 100kHz it is decided to reduce the necessary gating time by increasing the clock frequency, this plot shows the typical gain changes normalized to the original 100kHz gain.

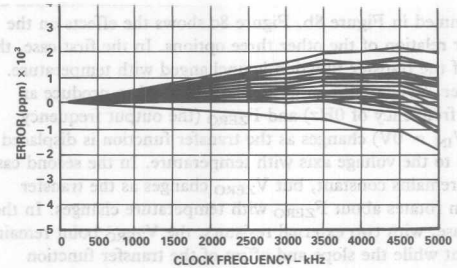


Figure 11. Gain vs. Clock Input

REFERENCE NOISE

The AD652 has on board a precision buffered 5V reference which is available to the user. Besides being used to offset the noninverting comparator input in the voltage-to-frequency mode, this reference can be used for other applications such as offsetting the input to handle bipolar signals and providing bridge excitation. It can source 10mA and sink 100μA, and is short circuit protected. Heavy loading of the reference will not change the gain of the VFC, although it will affect the external reference voltage. For example, a 10mA load interacting with a 0.3Ω typical output impedance will change the reference voltage by 0.06%.

DIGITAL INTERFACING CONSIDERATIONS

The AD652 clock input is a high impedance input with a threshold voltage of two diode voltages with respect to Digital Ground at pin 12 (approximately 1.2 volts at room temp). When the clock input is low, 5-10μA flows out of this pin. When the clock input is high, no current flows.

The frequency output is an open collector pull-down and is capable of sinking 10mA with a maximum voltage of 0.4 volts. This will drive 6 standard TTL inputs. The open collector pull up voltage can be as high as 36 volts above digital ground.

COMPONENT SELECTION

The AD652 integrating capacitor should be 0.02μF. If a large amount of normal mode interference is expected (more than 0.1 volts) and the clock frequency is less than 500kHz, an integrating capacitor of 0.1μF should be used. Mylar, polypropylene, or polystyrene capacitors should be used.

The open collector pull-up resistor should be chosen to give adequately fast rise times. At low clock frequencies (100kHz) larger resistor values (several kΩ) and slower rise times may be tolerated. However, at higher clock frequencies (1MHz) a lower value resistor should be used. The loading of the logic input which is being driven must also be taken into consideration. For example, if 2 standard TTL loads are to be driven then a 3.2mA current must be sunk, leaving 6.8mA for the pull-up resistor if the maximum low level voltage is to be maintained at 0.4 volts. A 680Ω resistor would thus be selected ((5–0.4)V/6.8mA) = 680Ω.

The one-shot capacitor controls the pulse width of the frequency output. The pulse is initiated by the rising edge of the clock signal. The delay time between the rising edge of the clock and the falling edge of the frequency output is typically 200ns. The width of the pulse is 5ns/pF and the minimum width is about 200ns with pin 9 floating. If the one-shot period is accidentally chosen longer than the clock period, the width of the pulse will

default to equal the clock period. The one-shot can be disabled by connecting pin 9 to $+V_S$ (Figure 12); the output pulse width will then be equal to the clock period. The one-shot is activated (Figure 13) by connecting a capacitor from pin 9 to $+V_S$, $-V_S$, or Digital Ground($+V_S$ is preferred).

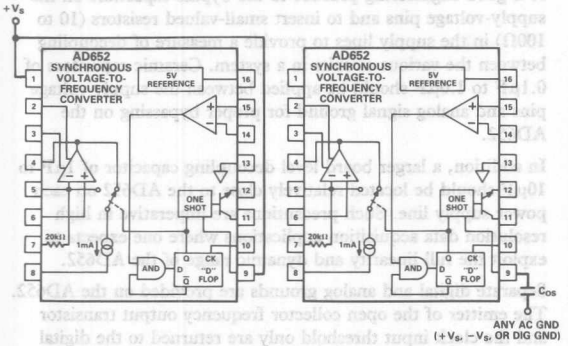


Figure 12. One Shot Disabled

Figure 13. One Shot Enabled

DIGITAL GROUND

Digital Ground can be at any potential between $-V_S$ and ($+V_S$ -4 volts). This can be very useful in a system with derived grounds rather than stiff supplies. For example, in a small isolated power circuit, often only a single supply is generated and the "ground" is set by a divider tap. Such a ground cannot handle the large currents associated with digital signals. With the AD652 SVFC, it is possible to connect the DIG GND to $-V_S$ for a solid logic reference, as shown in Figure 14.

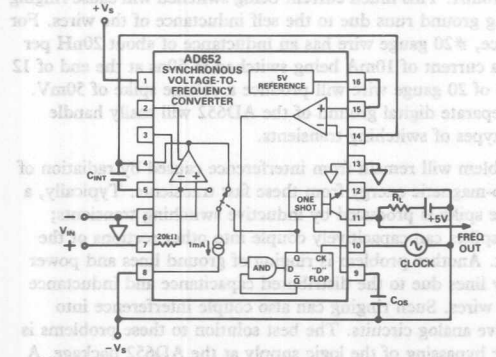


Figure 14. Digital GND at $-V_S$

SINGLE SUPPLY OPERATION

In addition to the Digital Ground being connected to $-V_S$, it is also possible to connect Analog Ground to $-V_S$ of the AD652. Hence, the device is truly operating from a single supply voltage that can range from $+12V$ to $+36V$. This is shown in Figure 15 for a positive voltage input and Figure 16 for a negative voltage input.

In Figure 15, the comparator reference is used as a derived ground, and the input voltage is referred to this point as well as the op amp common mode (pin 6 is tied to pin 16). Since the input signal source must drive 0.5mA of full-scale signal current into pin 7, it must also draw the exact same current from the input reference potential. This current will thus be provided by the 5V reference.

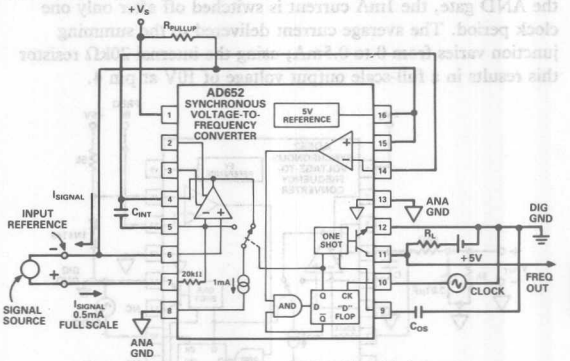


Figure 15. Single Supply Positive Voltage Input

In the single supply operation mode, an external resistor, R_{PULLUP}, is necessary between the power supply, $+V_S$, and the 5V reference output. This resistor should be selected such that a current of approximately 500μA flows during operation. For example, with a power supply voltage of $+15V$, a 20kΩ resistor would be selected ((15V − 5V)/500μA = 20kΩ).

Figure 16 shows the negative voltage input configuration for use of the AD652 in the single supply mode. In this mode the signal source is driving the "+" input of the op amp which requires only 20nA (typical), rather than the 0.5mA required in the positive input voltage configuration. The voltage at pin 6 may go as low as 4 volts above ground ($-V_S$, pin 8). Since the input reference is 5.0 volts above ground, this leaves a 1V window for the input signal. In order to drive the integrating capacitor with a 0.5mA full-scale current, it is necessary to provide an external 2kΩ resistor. This results in a 2kΩ resistor and a 1V input range. The external 2kΩ resistor should be a low-TC metal-film type for lowest drift degradation.

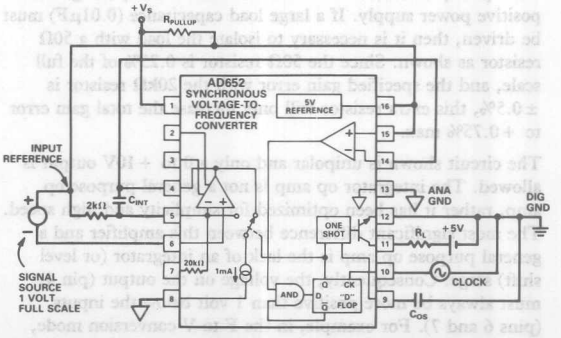


Figure 16. Single Supply Negative Voltage Input

FREQUENCY-TO-VOLTAGE CONVERTER

The AD652 SVFC also works as a frequency-to-voltage converter. Figure 17 shows the connection diagram for F/V conversion. In this case the "−" input of the comparator is fed the input pulses. Either comparator input may be used so that an input pulse of either polarity may be applied to the F/V. In Figure 17 the "+" input is tied to a 1.2V reference and low level TTL pulses are used as the frequency input. The pulse must be low

on the falling edge of the clock. On the subsequent rising edge the 1mA current source is switched to the integrator summing junction and ramps up the voltage at pin 4. Due to the action of the AND gate, the 1mA current is switched off after only one clock period. The average current delivered to the summing junction varies from 0 to 0.5mA; using the internal 20kΩ resistor this results in a full-scale output voltage of 10V at pin 4.

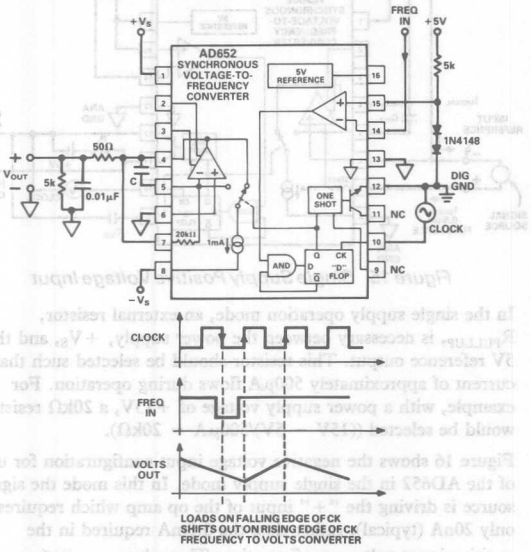


Figure 17. Frequency-to-Voltage Converter

The frequency response of the circuit is determined by the capacitor; the −3dB frequency is simply the RC time constant. A tradeoff exists between ripple and response. If low ripple is desired, a large value capacitor must be used (1μF), if fast response is needed, a small capacitor is used (1nF minimum).

The op amp can drive a 5kΩ resistor load to 10V, using a 15V positive power supply. If a large load capacitance (0.01μF) must be driven, then it is necessary to isolate the load with a 50Ω resistor as shown. Since the 50Ω resistor is 0.25% of the full scale, and the specified gain error with the 20kΩ resistor is ±0.5%, this extra resistor will only increase the total gain error to +0.75% max.

The circuit shown is unipolar and only a 0 to +10V output is allowed. The integrator op amp is not a general purpose op amp, rather it has been optimized for simplicity and high speed. The most significant difference between this amplifier and a general purpose op amp is the lack of an integrator (or level shift) stage. Consequently, the voltage on the output (pin 4) must always be more positive than 1 volt below the inputs (pins 6 and 7). For example, in the F-to-V conversion mode, the noninverting input of the op amp (pin 6) is grounded which means that the output (pin 4) cannot go below −1 volt. Normal operation of the circuit as shown will never call for a negative voltage at the output.

A second difference between this op amp and a general purpose amplifier is that the output will only sink 1.5mA to the negative supply. The only pulldown other than the 1mA current used for voltage-to-frequency conversion is a 0.5mA source. The op amp will source a great deal of current from the positive supply, and it is internally protected by current limiting. The output of the op amp may be driven to within 4 volts of the positive supply when not sourcing external current. When sourcing 10mA, the output voltage may be driven to within 6 volts of the positive supply.

DECOUPLING AND GROUNDING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 to 100Ω) in the supply lines to provide a measure of decoupling between the various circuits in a system. Ceramic capacitors of 0.1μF to 1.0μF should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD652.

In addition, a larger board level decoupling capacitor of 1μF to 10μF should be located relatively close to the AD652 on each power supply line. Such precautions are imperative in high resolution data acquisition applications where one expects to exploit the full linearity and dynamic range of the AD652.

Separate digital and analog grounds are provided on the AD652. The emitter of the open collector frequency output transistor and the clock input threshold only are returned to the digital ground. Only the 5V reference is connected to analog ground. The purpose of the two separate grounds is to allow isolation between the high precision analog signals and the digital section of the circuitry. Much noise can be tolerated on the digital ground without affecting the accuracy of the VFC. Such ground noise is inevitable when switching the large currents associated with the frequency output signal.

At high full-scale frequencies, it is necessary to use a pull-up resistor of about 500Ω in order to get the rise time fast enough to provide well defined output pulses. This means that from a 5 volt logic supply, for example, the open collector output will draw 10mA. This much current being switched will cause ringing on long ground runs due to the self inductance of the wires. For instance, #20 gauge wire has an inductance of about 20nH per inch; a current of 10mA being switched in 50ns at the end of 12 inches of 20 gauge wire will produce a voltage spike of 50mV. The separate digital ground of the AD652 will easily handle these types of switching transients.

A problem will remain from interference caused by radiation of electro-magnetic energy from these fast transients. Typically, a voltage spike is produced by inductive switching transients; these spikes can capacitively couple into other sections of the circuit. Another problem is ringing of ground lines and power supply lines due to the distributed capacitance and inductance of the wires. Such ringing can also couple interference into sensitive analog circuits. The best solution to these problems is proper bypassing of the logic supply at the AD652 package. A 1μF to 10μF tantalum capacitor should be connected directly to the supply side of the pull-up resistor and to the digital ground, pin 12. The pull-up resistor should be connected directly to the frequency output, pin 11. The lead lengths on the bypass capacitor and the pull-up resistor should be as short as possible. The capacitor will supply (or absorb) the current transients, and large ac signals will flow in a physically small loop through the capacitor, pull-up resistor, and frequency output transistor. It is important that the loop be physically small for two reasons: first, there is less inductance if the wires are short, and second, the loop will not radiate RFI efficiently.

The digital ground (pin 12) should be separately connected to the power supply ground. Note that the leads to the digital power supply are only carrying dc current. There may be a dc

ground drop due to the difference in currents returned on the analog and digital grounds. This will not cause a problem. These features greatly ease power distribution and ground management in large systems. Proper technique for grounding requires separate digital and analog ground returns to the power supply. Also, the signal ground must be referred directly to analog ground (pin 6) at the package. More information on proper grounding and reduction of interference can be found in reference 1.

FREQUENCY OUTPUT MULTIPLIER

The AD652 can serve as a frequency output multiplier when used in conjunction with a standard voltage-to-frequency converter. Figure 18 shows the low cost AD654 VFC being used as the clock input to the AD652. Also shown is a second AD652 in the F/V mode. The AD654 is set up to produce an output frequency of 0-500kHz for an input voltage (V_1) range of 0-10V. The use of R4, C1, and the XOR gate doubles this output frequency from 0-500kHz to 0-1MHz.

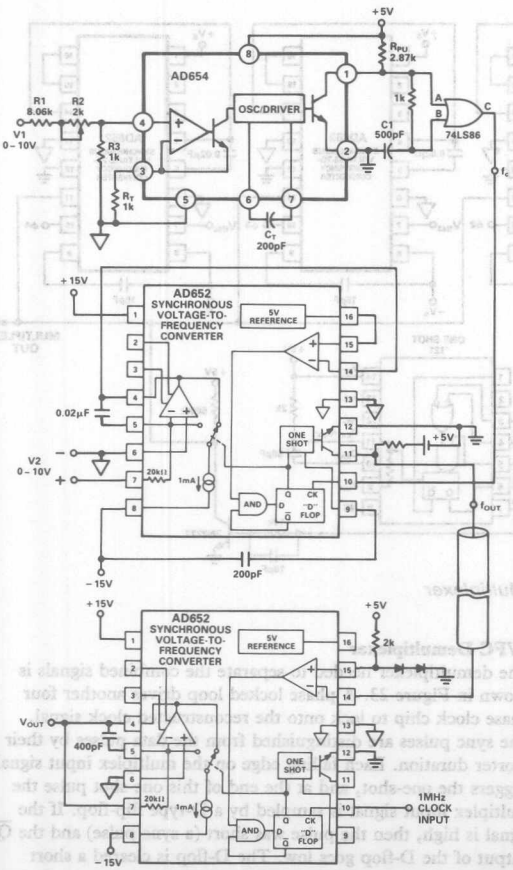


Figure 18. Frequency Output Multiplier

This 1MHz full-scale frequency is then used as the clock input to the AD652 SVFC. Since the AD652 full-scale output frequency is one-half the clock frequency, the 1MHz FS clock frequency establishes a 500kHz maximum output frequency for the AD652 when its input voltage (V_2) is +10V. The user thus has an output frequency range from 0-500kHz which is proportional to the product of V_1 and V_2.

This can be shown in equation form, where f_C is the AD654 output frequency and f_{OUT} is the AD652 output frequency:

$$f_C = V_1 \frac{1MHz}{10V}$$

$$f_{OUT} = V_2 \left(\frac{f_C/2}{10V}\right)$$

$$f_{OUT} = V_1 V_2 \left(\frac{1MHz}{2(10V)\,(10V)}\right)$$

$$f_{OUT} = V_1 \cdot V_2 \cdot 5kHz/V^2$$

The scope photo in Figure 19 shows V_1 and V_2 (top two traces) and the output of the F-V (bottom trace).

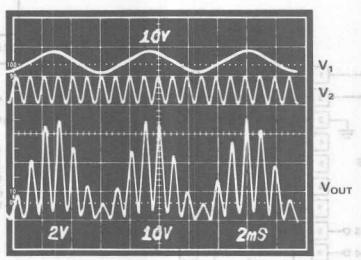


Figure 19. Multiplier Waveforms

SINGLE-LINE MULTIPLEXED DATA TRANSMISSION

It is often necessary to measure several different signals and relay the information to some remote location using a minimum amount of cable. Multiple AD652 SVFC devices may be used with a multiphase clock to combine these measurements for serial transmission and demultiplexing. Figure 20 shows a block diagram of a single-line multiplexed data transmission system with high noise immunity. Figures 21, 22 and 23 show the SVFC multiplexer, a representative means of data transmission, and an SVFC demultiplexer respectively.

Multiplexer

Figure 21 shows the SVFC multiplexer. The clock inputs for the several SVFC channels are generated by a TIM9904A four phase clock driver, and the frequency outputs are combined by strapping all the frequency output pins together (a "wire or" connection). The one-shot in the AD652 sets the pulse width of the frequency output pulses to be slightly shorter than one quarter of the clock period. Synchronization is achieved by applying one of the four available phases to a fixed TTL one-shot ('121) and combining the output with an external transistor. The width of this sync pulse is shorter than the width of the frequency output pulses to facilitate decoding the signal. The RC lag network on the input of the one-shot provides a slight delay between the rising edge of the clock and the sync pulse in

[1]"Noise Reduction Techniques in Electronic Systems," by H.W. Ott, (John Wiley, 1976).

edge of the clock and the output pulse.

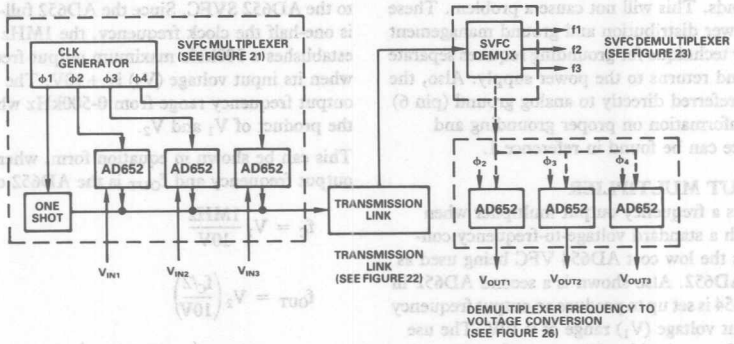


Figure 20. Single Line Multiplexed Data Transmission Block Diagram

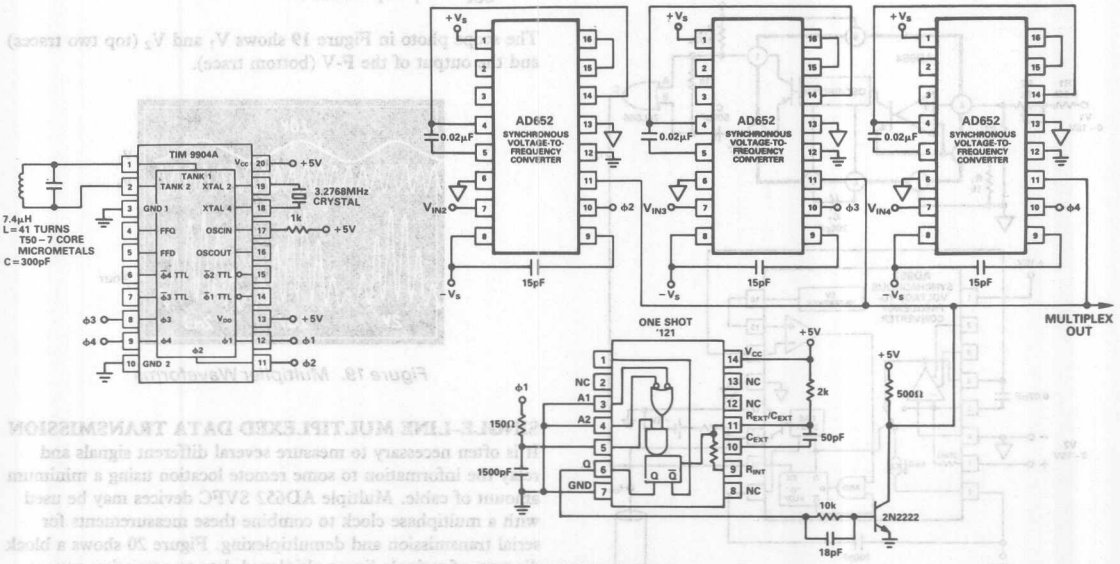


Figure 21. SVFC Multiplexer

Transmitter

The multiplex signal can be transmitted in any manner suitable to the task at hand. A pulse transformer or an opto-isolator can provide galvanic isolation; extremely high voltage isolation or transmission through severe RF environments can be accomplished with a fiber-optic link; telemetry can be accomplished with a radio link. The circuit shown in Figure 22 uses an EIA RS-422 standard for digital data transmission over a balanced line. Figure 24 shows the waveforms of the four clock phases and the multiplex output signal. Note that the sync pulse is present every clock cycle, but the data pulses are no more frequent than every other clock cycle since the maximum output frequency from the SVFC is half the clock frequency. The clock frequency used in this circuit is 819.2 kHz and will provide more than 16 bits of resolution if 100 millisecond gate time is allowed for counting pulses of the decoded output frequencies.

SVFC Demultiplexer

The demultiplexer needed to separate the combined signals is shown in Figure 23. A phase locked loop drives another four phase clock chip to lock onto the reconstructed clock signal. The sync pulses are distinguished from the data pulses by their shorter duration. Each falling edge on the multiplex input signal triggers the one-shot, and at the end of this one-shot pulse the multiplex input signal is sampled by a D-type flip-flop. If the signal is high, then the pulse was short (a sync pulse) and the $\overline{Q}$ output of the D-flop goes low. The D-flop is cleared a short time (two gate delays) later, and the clock is reconstructed as a stream of short, low-going pulses. If the Multiplex input is a data pulse, then when the D-flop samples at the end of the one-shot period, the signal will still be low and no pulse will appear at the reconstructed clock output. These waveforms are shown in Figure 25.

If it is desired to recover the individual frequency signals, then the multiplex input is sampled with a D-flop at the appropriate time as determined by the rising edge of the various phases generated by the clock chip. These frequency signals can be counted as a ratio relative to the reconstructed clock, so it is not even necessary for the transmitter to be crystal controlled as shown here.

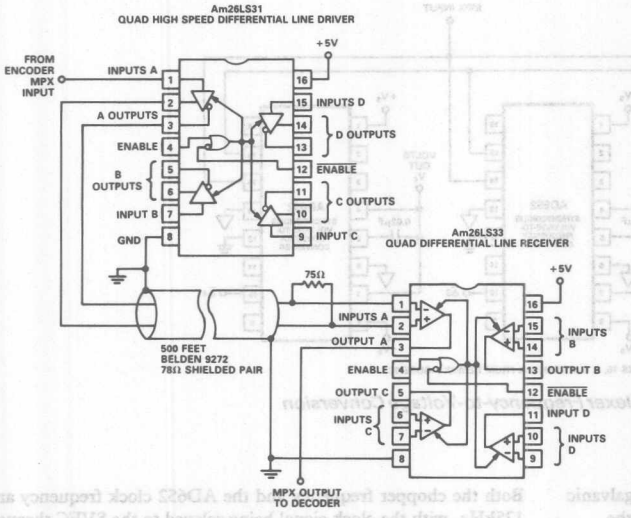


Figure 22. RS-422 Standard Data Transmission

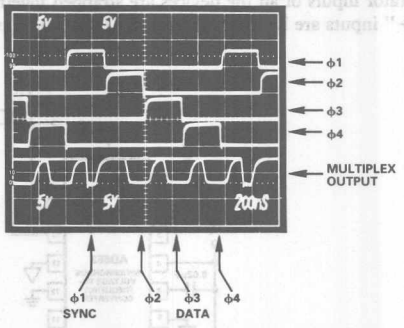


Figure 24. Multiplexer Waveforms

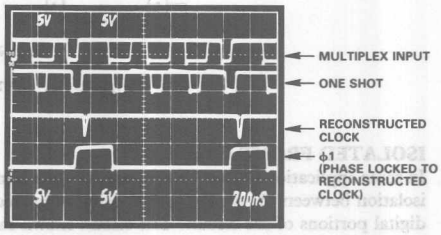


Figure 25. Demultiplexer Waveforms

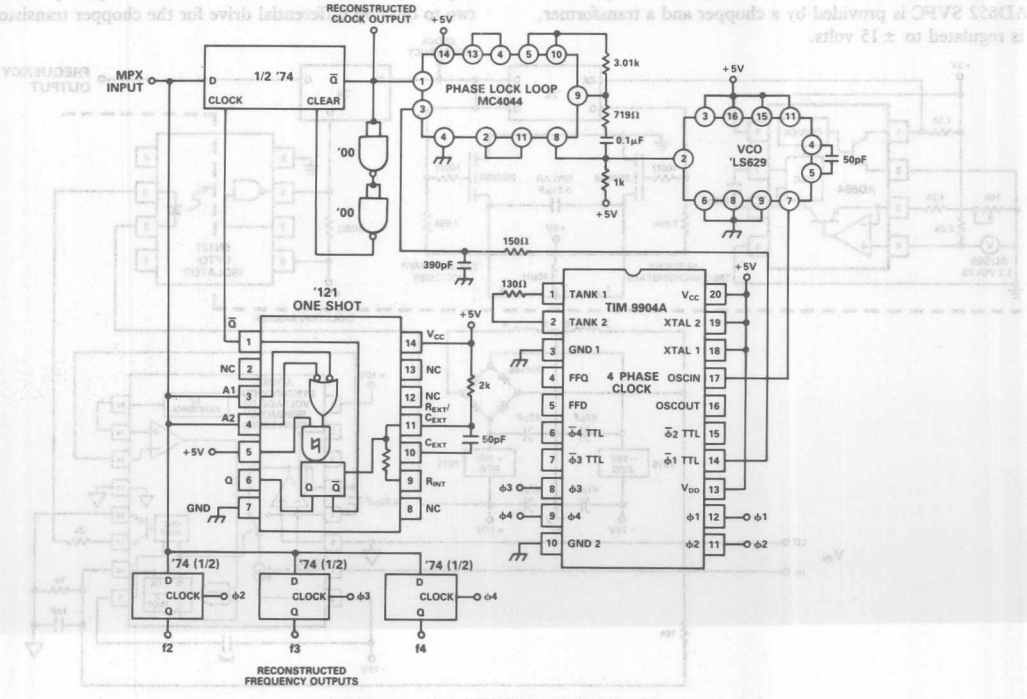


Figure 23. SVFC Demultiplexers

Analog Signal Reconstruction

If it is desired to reconstruct the analog voltages from the multiplex signal, then three more AD652 SVFC devices are used as frequency-to-voltage converters, as shown in Figure 26. The comparator inputs of all the devices are strapped together, and the "+" inputs are held at a 1.2 volt TTL threshold, while the "–" inputs are driven by the multiplex input. The three clock inputs are driven by the $\overline{\phi}$ outputs of the clock chip. Remember that data at the comparator input of the SVFC is loaded on the falling edge of the clock signal and shifted out on the next rising edge. Note that the frequency signals for each data channel are available at the frequency output pin of each FVC.

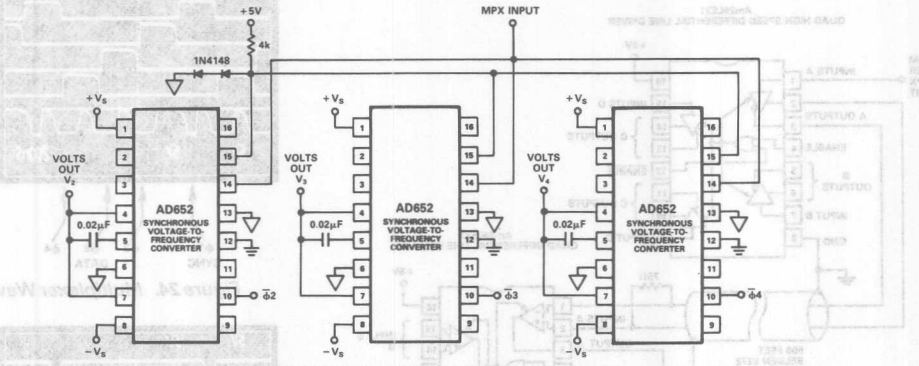


Figure 26. Demultiplexer Frequency-to-Voltage Conversion

ISOLATED FRONT END

In some applications it may be necessary to have complete galvanic isolation between the analog signals being measured and the digital portions of the circuit. The circuit shown in Figure 27 runs off a single 5 volt power supply and provides a self-contained, completely isolated analog measurement system. The power for the AD652 SVFC is provided by a chopper and a transformer, and is regulated to ±15 volts. Both the chopper frequency and the AD652 clock frequency are 125kHz, with the clock signal being relayed to the SVFC through the transformer. The frequency output signal is relayed through an opto-isolator and latched into a D-flop. The chopper frequency is generated from an AD654 VFC and is frequency divided by two to develop differential drive for the chopper transistors, and

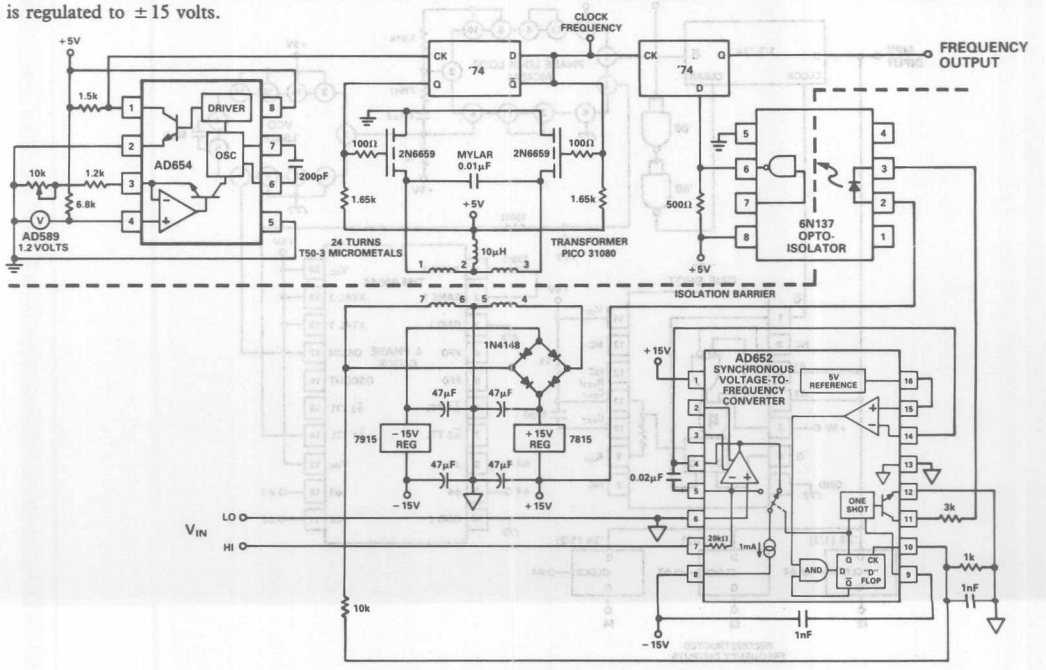


Figure 27. Isolated Synchronous VFC

to ensure an accurate 50 percent duty cycle. The pull-up resistors on the D-flop outputs provide a well defined high level voltage to the choppers to equalize the drive in each direction. The 10μH inductor in the +5V lead of the transformer primary is necessary to equalize any residual imbalance in the drive on each half-cycle and thus prevent saturation of the core. The capacitor across the primary resonates the system so that under light loading conditions on the secondary the wave shape will be sinusoidal and the clock frequency will be relayed to the SVFC. To adjust the chopper frequency, disconnect any load on the secondary and tune the AD654 for a minimum in the supply current drawn from the 5 volt supply.

A-TO-D CONVERSION

In performing an A-to-D conversion, the output pulses of a VFC are counted for a fixed gate interval. To achieve maximum performance with the AD652, the fixed gate interval should be generated using a multiple of the SVFC clock input. Counting in this manner will eliminate any errors due to the clock (whether it be jitter, drift with time or temperature, etc.) since it is the ratio of the clock and output frequencies that is being measured.

The resolution of the A-to-D conversion measurement is determined by the clock frequency and the gate time. If, for instance, a resolution of 12 bits is desired and the clock frequency is 1MHz (resulting in an AD652 FS frequency of 500kHz) the gate time will be:

$$\left(\frac{\text{FS Freq}}{N}\right)^{-1} = \left(\frac{1}{2}\frac{\text{Clock Freq}}{N}\right)^{-1} = \left(\frac{1\text{MHz}}{2(4096)}\right)^{-1}$$

$$= \frac{8192}{1\times10^{6}}\ \text{sec} = 8.192\text{ms}$$

: Where N is the total number of codes for a given resolution.

Figure 28 shows the AD652 SVFC as an A-to-D converter in block diagram form.

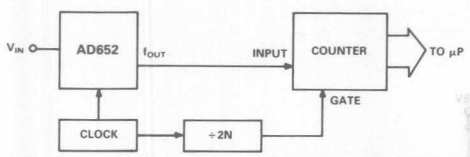


Figure 28. Block Diagram of SVFC A-to-D Converter

To provide the ÷ 2N block a single chip counter such as the 4020B can be used. The 4020B is a 14-stage binary ripple counter which has a clock and master reset for inputs, and buffered outputs from the first stage and the last eleven stages. The output of the first stage is $f_{CLOCK} \div 2^1 = f_{CLOCK}/2$, while the output of the last stage is $f_{CLOCK} \div 2^{14} = f_{CLOCK}/16384$. Hence using this single chip counter as the ÷ 2N block, 13-bit resolution can be achieved. Higher resolution can be achieved by cascading D-type flip-flops or another 4020B with the counter.

Table I shows the relationship between clock frequency and gate time for various degrees of resolution. Note that if the variables are chosen such that the gate times are multiples of 50, 60 or 400Hz, normal-mode rejection (NMR) of those line frequencies will occur.

Table I.

Resolution	N	Clock	Conversion or Gate Time	Typ Lin	Comments
12 Bits	4096	81.92kHz	100ms	0.002%	50, 60, 400Hz NMR
12 Bits	4096	2MHz	4.096ms	0.01%	
12 Bits	4096	4MHz	2.048ms	0.02%	
4 Digits	10000	200kHz	100ms	0.002%	50, 60, 400Hz NMR
14 Bits	16384	327.68kHz	100ms	0.002%	50, 60, 400Hz NMR
14 Bits	16384	1.966MHz	16.66ms	0.01%	60Hz NMR
14 Bits	16384	1.638MHz	20ms	0.01%	50Hz NMR
4 1/2 Digits	20000	400kHz	100ms	0.002%	50, 60, 400Hz NMR
16 Bits	65536	655.36kHz	200ms	0.002%	50, 60, 400Hz NMR
16 Bits	65536	4MHz	32.77ms	0.02%	

DELTA MODULATOR

The circuit of Figure 29 shows the AD652 configured as a delta modulator. A reference voltage is applied to the input of the integrator (pin 7), which sets the steady state output frequency at one-half of the AD652 full-scale frequency (1/4 of the clock frequency). As a 0 to 10V input signal is applied to the comparator (pin 15), the output of the integrator attempts to track this signal. For an input in an idling condition (dc) the output frequency will be one-half full scale. For positive going signals the output frequency will be between one-half full scale and full scale, and for negative going signals the output frequency will be between zero and one-half full scale. The output frequency will correspond to the slope of the comparator input signal.

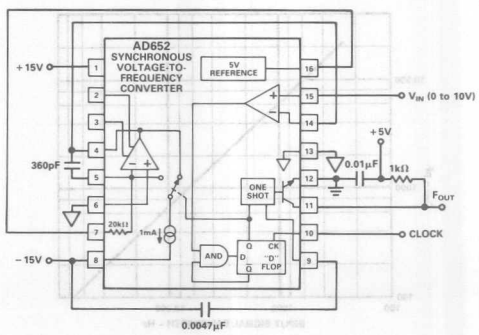


Figure 29. Delta Modulator

Since the output frequency corresponds to the slope of the input signal, the delta modulator acts as a differentiator. A delta modulator is thus a direct way of finding the derivative of a signal. This is useful in systems where, for example, a signal corresponding to velocity exists and it is desired to determine acceleration.

Figure 30 is a scope photo showing a 20kHz, 0 to 10V sine wave used as the input to the comparator and its ramp-wise approximation at the integrator output. The clock frequency used as 2MHz and the integrating capacitor was 360pF. Figure 31 shows the same input signal and its ramp-wise approximation, along with the output frequency corresponding to the derivative of the input signal. In this case the clock frequency was 850kHz.

The choice of an integrating capacitor is primarily dictated by the input signal bandwidth. Figure 32 shows this relationship. It should be noted that as the value of C_{INT} is lowered, the ramp size of the integrator approximation becomes larger. This can be compensated for by increasing the clock frequency. The

in Figures 30 and 31.

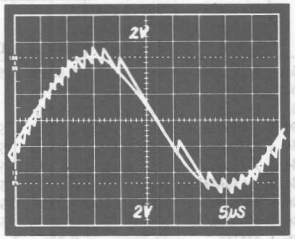


Figure 30. Delta Modulator Input Signal and Ramp-Wise Approximation

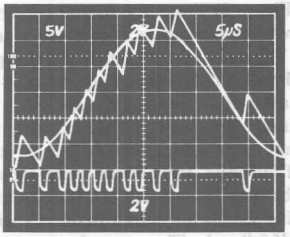


Figure 31. Delta Modulator Input Signal, Ramp-Wise Approximation and Output Frequency

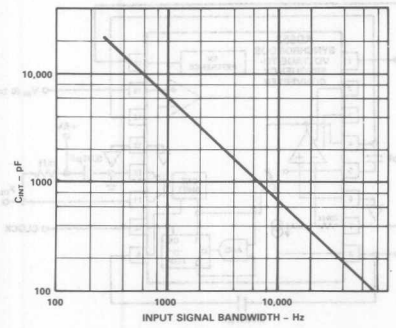


Figure 32. Maximum Integrating Cap Value vs. Input Signal Bandwidth

The circuit of Figure 33 illustrates a simple interface between the AD652 and a bridge-type transducer. The AD652 is an ideal choice because its buffered 5 volt reference can be used as the bridge excitation thereby ratiometrically eliminating the gain drift related errors. This reference will provide a minimum of 10mA of external current, which is adequate for bridge resistance of 600Ω and above. If, for example, the bridge resistance is 120Ω or 350Ω, an external pull-up resistor (R_{PU}) is required and can be calculated using the formula:

$$R_{PU}\,(\max) = \frac{+V_S - 5V}{\frac{5V}{R_{BRIDGE}} - 10mA}$$

An instrumentation amplifier is used to condition the bridge signal before presenting it to the SVFC. The AD625, with its high CMRR, minimizes common-mode errors and also can be set to arbitrary gains between 1 and 10,000 via three resistors, simplifying the scaling for the AD652's calibrated 10 volt input range. These resistors should be selected such that the following equation holds:

$$10V = V_{BRIDGE}\left(\frac{2R_F}{R_G} + 1\right)$$

where $10k\Omega \le R_F \le 20k\Omega$, and V_{BRIDGE} is the maximum output voltage of the bridge.

The bridge output may be unipolar, as is the case for most pressure transducers, or it may be bipolar as in some strain measurements. If the signal is unipolar, the reference input of the AD625 (pin 7) is simply grounded. If the bridge has a bipolar output, however, the AD652 reference can be tied to pin 7, thereby converting a ±5 volt signal (after gain) into a 0 to +10 volt input for the SVFC.

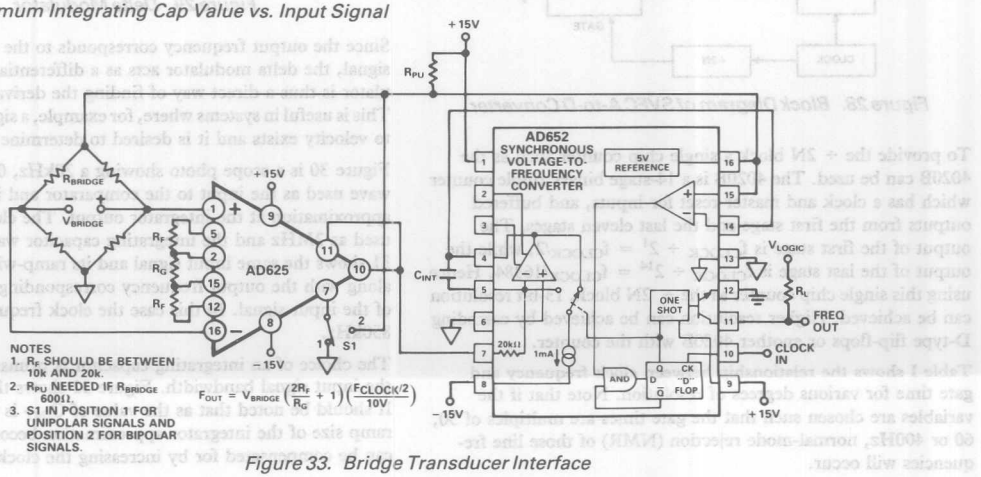


Figure 33. Bridge Transducer Interface

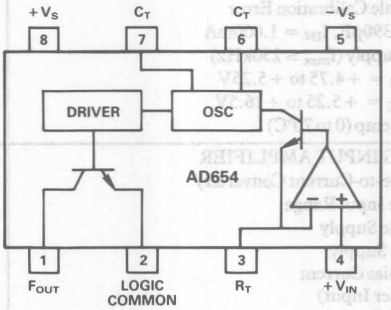
Low Cost Monolithic Voltage-to-Frequency Converter

AD654

FEATURES

- **Low Cost**
- **Single or Dual Supply, 5 to 36 Volts, ±5V to ±18V**
- **Full Scale Frequency Up to 500kHz**
- **Minimum Number of External Components Needed**
- **Versatile Input Amplifier**
  - **Positive or Negative Voltage Modes**
  - **Negative Current Mode**
  - **High Input Impedance, Low Drift**
- **Low Power: 2.0mA Quiescent Current**
- **Low Offset: 1mV**

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD654 is a monolithic V/F converter consisting of an input amplifier, a precision oscillator system, and a high current output stage. A single RC network is all that is required to set up any full scale (F.S.) frequency up to 500kHz and any F.S. input voltage up to ±30V. Linearity error is only 0.03% for a 250kHz F.S., and operation is guaranteed over an 80dB dynamic range. The overall temperature coefficient (excluding the effects of external components) is typically ±50ppm/°C. The AD654 operates from a single supply of 5 to 36V and consumes only 2.0mA quiescent current.

The low drift (4μV/°C typ) input amplifier allows operation directly from small signals such as thermocouples or strain gauges while offering a high (250MΩ) input resistance. Unlike most V/F converters, the AD654 provides a square-wave output, and can drive up to 12 TTL loads, opto-couplers, long cables, or similar loads.

PRODUCT HIGHLIGHTS

1. Packaged in both an 8-pin mini-DIP and an 8-pin SOIC package, the AD654 is a complete V/F converter requiring only an RC timing network to set the desired full scale frequency and a selectable pull-up resistor for the open-collector output stage. Any full scale input voltage range from 100mV to 10 volts (or greater, depending on $+V_S$) can be accommodated by proper selection of the timing resistor. The full scale frequency is then set by the timing capacitor from the simple relationship, f = V/10RC.
2. A minimum number of low cost external components are necessary. A single RC network is all that is required to set up any full scale frequency up to 500kHz and any full scale input voltage up to ±30V.
3. Plastic packaging allows low cost implementation of the standard VFC applications: A/D conversion, isolated signal transmission, F/V conversion, phase-locked loops, and tuning switched-capacitor filters.
4. Power supply requirements are minimal; only 2.0mA of quiescent current is drawn from the single positive supply from 4.5 to 36 volts. In this mode, positive inputs can vary from 0 volts (ground) to $(+V_S - 4)$ volts. Negative inputs can easily be connected for below ground operation.
5. The versatile open-collector output stage can sink more than 10mA with a saturation voltage less than 0.4 volts. The Logic Common terminal can be connected to any level between ground (or $-V_S$) and 4 volts below $+V_S$. This allows easy direct interface to any logic family with either positive or negative logic levels.

AD654 —SPECIFICATIONS

(t_{AMB} = +25°C and V_S (total) = 5 to 16.5V, unless otherwise specified. All testing done @ V_S = +5V).

Model	AD654JN/JR Min	Typ	Max	Units
CURRENT-TO-FREQUENCY CONVERTER				
Frequency Range	0		500	kHz
Nonlinearity[1]				
f_{max} = 250kHz		0.06	**0.1**	%
f_{max} = 500kHz		0.20	0.4	%
Full Scale Calibration Error				
C = 390pF, I_{IN} = 1.000mA	−10		**10**	%
vs. Supply ($f_{max} \leq$ 250kHz)				
V_S = +4.75 to +5.25V		0.20	**0.40**	%/V
V_S = +5.25 to +16.5V		0.05	**0.10**	%/V
vs. Temp (0 to 70°C)		50		ppm/°C
ANALOG INPUT AMPLIFIER				
(Voltage-to-Current Converter)				
Voltage Input Range				
Single Supply	0		(+V_S −4)	V
Dual Supply	−V_S		(+V_S −4)	V
Input Bias Current				
(Either Input)		30	**50**	nA
Input Offset Current		5		nA
Input Resistance (Non-Inverting)		250		MΩ
Input Offset Voltage		0.5	**1.0**	mV
vs. Supply				
V_S = +4.75 to +5.25V		0.1	**0.25**	mV/V
V_S = +5.25 to +16.5V		0.03	**0.1**	mV/V
vs. Temp (0 to 70°C)		4		µV/°C
OUTPUT INTERFACE (Open Collector Output)				
(Symmetrical Square Wave)				
Output Sink Current in Logic "0"[2]				
V_{OUT} = 0.4V max, 25°C	**10**	20		mA
V_{OUT} = 0.4V max, 0 to 70°C	5	10		mA
Output Leakage Current in Logic "1"		10	**100**	nA
0 to 70°C		50	500	nA
Logic Common Level Range	−V_S		(+V_S −4)	V
Rise/Fall Times (C_T = 0.01µF)				
I_{IN} = 1mA		0.2		µs
I_{IN} = 1µA		1		µs
POWER SUPPLY				
Voltage, Rated Performance	4.5		16.5	V
Voltage, Operating Range				
Single Supply	4.5		36	V
Dual Supply	±5		±18	V
Quiescent Current				
V_S (Total) = 5V		1.5	**2.5**	mA
V_S (Total) = 30V		2.0	**3.0**	mA
TEMPERATURE RANGE				
Operating Range	−40		85	°C
PACKAGE OPTIONS[3]				
SOIC		AD654JR		
Plastic DIP		AD654JN		

NOTES

[1]At f_{max} = 250kHz; R_T = 1kΩ, C_T = 390pF, I_{IN} = 0-1mA.
f_{max} = 500kHz; R_T = 1kΩ, C_T = 200pF, I_{IN} = 0-1mA.

[2]The sink current is the amount of current that can flow into Pin 1 of the AD654 while maintaining a maximum voltage of 0.4V between Pin 1 and Logic Common.

[3]N = Plastic DIP; R = SOIC. For outline information see Package Information section.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage $+V_S$ to $-V_S$ 36V
Maximum Input Voltage
(Pins 3, 4) to $-V_S$ . . . . . $-300mV$ to $+V_S$
Maximum Output Current
Instantaneous 50mA
Sustained 25mA
Logic Common to $-V_S$ . . . . . $-500mV$ to $(+V_S - 4)$
Storage Temperature Range . . . . . $-65°C$ to $+150°C$

CIRCUIT OPERATION

The AD654's block diagram appears in Figure 1. A versatile operational amplifier serves as the input stage; its purpose is to convert and scale the input voltage signal to a drive current in the NPN follower. Optimum performance is achieved when, at the full scale input voltage, a 1mA drive current is delivered to the current-to-frequency converter (an astable multivibrator). The drive current provides both the bias levels and the charging current to the externally connected timing capacitor. This "adaptive" bias scheme allows the oscillator to provide low nonlinearity over the entire current input range of 100nA to 2mA. The square wave oscillator output goes to the output driver which provides a floating base drive to the NPN power transistor. This floating drive allows the logic interface to be referenced to a level other than $-V_S$.

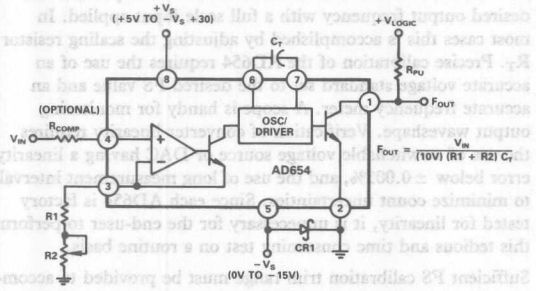


Figure 1. Standard V-F Connection for Positive Input Voltages

V/F CONNECTION FOR POSITIVE INPUT VOLTAGES

In the connection scheme of Figure 1, the input amplifier presents a very high (250MΩ) impedance to the input voltage, which is converted into the proper drive current by the scaling resistors at pin 3. Resistors R1 and R2 are selected to provide a 1mA full scale current with enough trim range to accommodate the AD654's 10% FS error and the components' tolerances. Full scale currents other than 1mA can be chosen, but linearity will be reduced; 2mA is the maximum allowable drive. The AD654's positive input voltage range spans from $-V_S$ (ground in single supply operation) to four volts below the positive supply. Power supply rejection degrades as the input exceeds $(+V_S - 3.75V)$ and at $(+V_S - 3.5V)$ the output frequency goes to zero.

As indicated by the scaling relationship in Figure 1, a 0.01μF timing capacitor will give a 10kHz full scale frequency, and 0.001μF will give 100kHz with a 1mA drive current. Good V/F linearity requires the use of a capacitor with low dielectric absorption (DA), while the most stable operation over temperature calls for a component having a small tempco. Polystyrene, polypropylene, or Teflon* capacitors are preferred for tempco and dielectric absorption; other types will degrade linearity. The capacitor should be wired very close to the AD654. In Figure 1, Schottky diode CR1 (MBD101) prevents logic common from dropping more than 500mV below $-V_S$. This diode is not required if $-V_S$ is equal to logic common.

V/F CONNECTIONS FOR NEGATIVE INPUT VOLTAGE OR CURRENT

The AD654 can accommodate a wide range of negative input voltages with proper selection of the scaling resistor, as indicated in Figure 2. This connection, unlike the buffered positive connection, is not high impedance because the signal source must supply the 1mA F.S. drive current. However, large negative voltages beyond the supply can be handled easily by modifying the scaling resistors appropriately. If the input is a true current source, R1 and R2 are not used. Again, diode CR1 prevents latch-up by insuring Logic Common does not drop more than 500mV below $-V_S$. The clamp diode (MBD101) protects the AD654 input from "below $-V_S$" inputs.

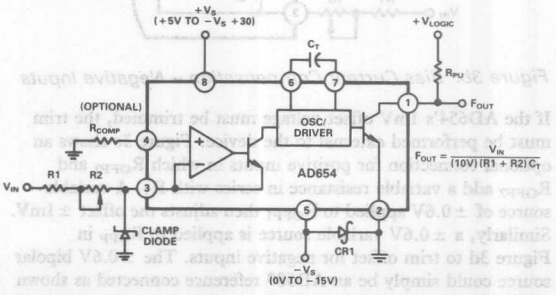


Figure 2. V-F Connections for Negative Input Voltages or Current

*Teflon is a trademark of E. I. Du Pont de Nemours & Co.

OFFSET CALIBRATION

In theory, two adjustments calibrate a V/F: scale and offset. In practice, most applications find the AD654's 1mV max voltage offset sufficiently low to forgo offset calibration. However, the input amplifier's 30nA (typ) bias currents will generate an offset due to the difference in DC source resistance between the input terminals. This offset can be substantial for large values of $R_T = R_1 + R_2$ and will vary as the bias currents drift over temperature. Therefore, to maintain the AD654's low offset, the application may require balancing the DC source resistances at the inputs (pins 3 and 4).

For positive inputs, this is accomplished by adding a compensation resistor nominally equal to R_T in series with the input as shown in Figure 3a. This limits the offset to the product of the 30nA bias current and the mismatch between the source resistance R_T and R_{COMP}. A second, smaller offset arises from the inputs' 5nA offset current flowing through the source resistance R_T or R_{COMP}. For negative input voltage and current connections, the compensation resistor is added at pin 4 as shown in Figure 3b in lieu of grounding the pin directly. For both positive and negative inputs, the use of R_{COMP} may lead to noise coupling at pin 4 and should therefore be bypassed for lowest noise operation.

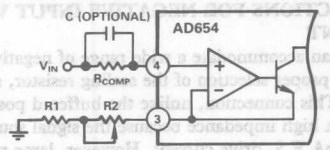


Figure 3a. Bias Current Compensation – Positive Inputs

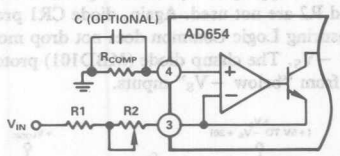


Figure 3b. Bias Current Compensation – Negative Inputs

If the AD654's 1mV offset voltage must be trimmed, the trim must be performed external to the device. Figure 3c shows an optional connection for positive inputs in which R_{OFF1} and R_{OFF2} add a variable resistance in series with R_T. A variable source of ±0.6V applied to R_{OFF1} then adjusts the offset ±1mV. Similarly, a ±0.6V variable source is applied to R_{OFF} in Figure 3d to trim offset for negative inputs. The ±0.6V bipolar source could simply be an AD589 reference connected as shown in Figure 3e.

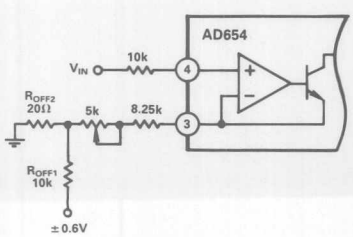


Figure 3c. Offset Trim Positive Input (10V FS)

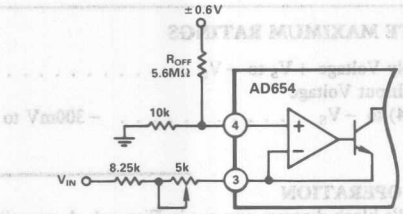


Figure 3d. Offset Trim Negative Input (–10V FS)

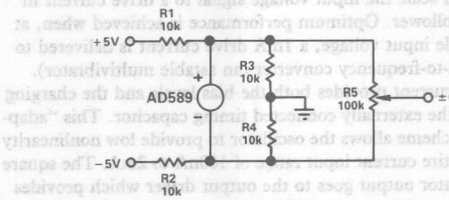


Figure 3e. Offset Trim Bias Network

FULL SCALE CALIBRATION

Full scale trim is the calibration of the circuit to produce the desired output frequency with a full scale input applied. In most cases this is accomplished by adjusting the scaling resistor R_T. Precise calibration of the AD654 requires the use of an accurate voltage standard set to the desired FS value and an accurate frequency meter. A scope is handy for monitoring output waveshape. Verification of converter linearity requires the use of a switchable voltage source or DAC having a linearity error below ±0.005%, and the use of long measurement intervals to minimize count uncertainties. Since each AD654 is factory tested for linearity, it is unnecessary for the end-user to perform this tedious and time consuming test on a routine basis.

Sufficient FS calibration trim range must be provided to accommodate the worst-case sum of all major scaling errors. This includes the AD654's 10% full scale error, the tolerance of the fixed scaling resistor, and the tolerance of the timing capacitor. Therefore, with a resistor tolerance of 1% and a capacitor tolerance of 5%, the fixed part of the scaling resistor should be a maximum of 84% of nominal, with the variable portion selected to allow 116% of the nominal.

If the input is in the form of a negative current source, the scaling resistor is no longer required, eliminating the capability of trimming FS frequency in this fashion. Since it is usually not practical to smoothly vary the capacitance for trimming purposes, an alternative scheme such as the one shown in Figure 4 is needed. Designed for a FS of 1mA, this circuit divides the input into two current paths. One path is through the 100Ω

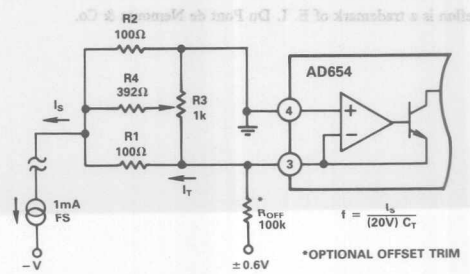


Figure 4. Current Source FS Trim

resistor R1, and flowing into pin 3; it constitutes the signal current I_T to be converted. The second path, through another 100Ω resistor R2, carries the same nominal current. Two equal valued resistors offer the best overall stability, and should be either 1% discrete film units, or a pair from a common array.

Since the 1mA FS input current is divided into two 500μA legs (one to ground and one to pin 3), the total input signal current (I_S) is divided by a factor of two in this network. To achieve the same conversion scale factor, C_T must be reduced by a factor of two. This results in a transfer unique to this hookup:

$$f = \frac{I_S}{(20V)\ C_T}$$

For calibration purposes, resistors R3 and R4 are added to the network, allowing a ±15% trim of scale factor with the values shown. By varying R4's value the trim range can be modified to accommodate wider tolerance components or perhaps the calibration tolerance on a current output transducer such as the AD592 temperature sensor. Although the values of R1 – R4 shown are valid for 1mA FS signals only, they can be scaled upward proportionately for lower FS currents. For instance, they should be increased by a factor of ten for a FS current of 100μA.

In addition to the offsets generated by the input amplifier's bias and offset currents, an offset voltage induced parasitic current arises from the current fork input network. These effects are minimized by using the bias current compensation resistor R_{OFF} and offset trim scheme shown in Figure 3e.

Although device warmup drifts are small, it is good practice to allow the devices operating environment to stabilize before trim, and insure the supply, source and load are appropriate. If provision is made to trim offset, begin by setting the input to 1/10,000 of full scale. Adjust the offset pot until the output is 1/10,000 of full scale (for example, 25Hz for a FS of 250kHz). This is most easily accomplished using a frequency meter connected to the output. The FS input should then be applied and the gain pot should be adjusted until the desired FS frequency is indicated.

INPUT PROTECTION

The AD654 was designed to be used with a minimum of additional hardware. However, the successful application of a precision IC involves a good understanding of possible pitfalls and the use of suitable precautions. Thus $+V_{IN}$ and R_T pins should not be driven more than 300mV below $-V_S$. Likewise, Logic Common should not drop more than 500mV below $-V_S$. This would cause internal junctions to conduct, possibly damaging the IC. In addition to the diode shown in Figures 1 and 2 protecting Logic Common, a second Schottky diode (MBD101) can protect the AD654's inputs from "below $-V_S$" inputs as shown in Figure 5. It is also desirable not to drive $+V_{IN}$ and R_T above $+V_S$. In operation, the converter will exhibit a zero output for inputs above ($+V_S$ – 3.5V). Also, control currents above 2mA will increase nonlinearity.

The AD654's 80dB dynamic range guarantees operation from a control current of 1mA (nominal FS) down to 100nA (equivalent to 1mV to 10V FS). Below 100nA improper operation of the oscillator may result, causing a false indication of input amplitude. In many cases this might be due to short-lived noise spikes which become added to input. For example, when scaled to accept an FS input of 1V, the −80dB level is only 100μV, so when the mean input is only 60dB below FS (1mV), noise spikes

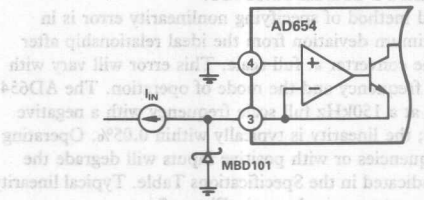


Figure 5. Input Protection

of 0.9mV are sufficient to cause momentary malfunction.

This effect can be minimized by using a simple low-pass filter ahead of the converter or a guard ring around the R_T pin. The filter can be assembled using the bias current compensation resistor discussed in the previous section. For an FS of 10kHz, a single-pole filter with a time constant of 100ms will be suitable, but the optimum configuration will depend on the application and the type of signal processing. Noise spikes are only likely to be a cause of error when the input current remains near its minimum value for long periods of time; above 100nA full integration of additive input noise occurs. Like the inputs, the capacitor terminals are sensitive to interference from other signals. The timing capacitor should be located as close as possible to the AD654 to minimize signal pickup in the leads. In some cases, guard rings or shielding may be required.

DECOUPLING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 to 100Ω) in the supply lines to provide a measure of decoupling between the various circuits in the system. Ceramic capacitors of 0.1μF to 1.0μF should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD654. A proper ground scheme appears in Figure 6.

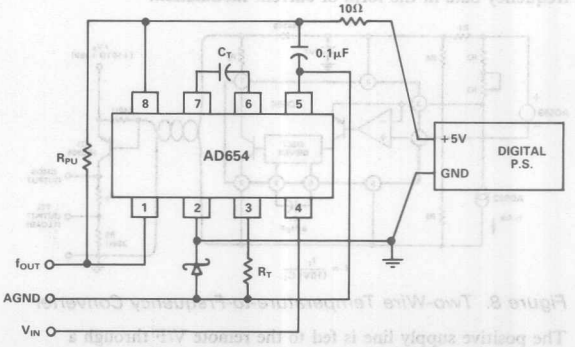


Figure 6. Proper Ground Scheme

OUTPUT INTERFACING CONSIDERATIONS

The output stage's design allows easy interfacing to all digital logic families. The output NPN transistor's emitter and collector are both uncommitted. The emitter can be tied to any voltage between $-V_S$ and 4 volts below $+V_S$, and the open collector can be pulled up to a voltage 36 volts above the emitter regardless of $+V_S$. The high power output stage can sink over 10mA at a maximum saturation voltage of 0.4V. The stage limits the output current at 25mA and can handle this limit indefinitely without damaging the device.

calibrating the converter at full scale. This error will vary with the full scale frequency and the mode of operation. The AD654 operates best at a 150kHz full scale frequency with a negative voltage input; the linearity is typically within 0.05%. Operating at higher frequencies or with positive inputs will degrade the linearity as indicated in the Specifications Table. Typical linearity at various temperatures is shown in Figure 7.

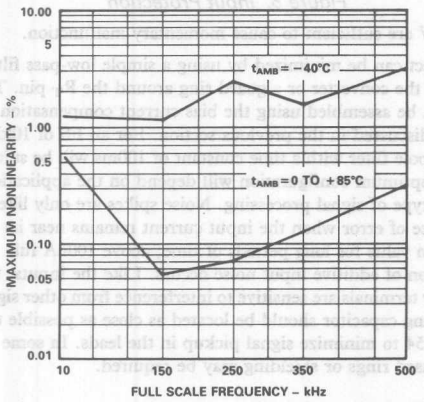


Figure 7. Typical Nonlinearities at Different Full-Scale Frequencies

TWO-WIRE TEMPERATURE-TO-FREQUENCY CONVERSION

Figure 8 shows the AD654 in a two-wire temperature-to-frequency conversion scheme. The twisted pair transmission line serves the dual purpose of supplying power to the device and also carrying frequency data in the form of current modulation.

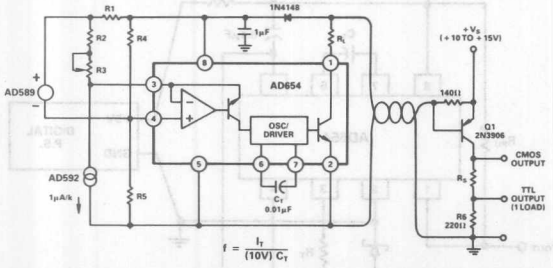


Figure 8. Two-Wire Temperature-to-Frequency Converter

The positive supply line is fed to the remote V/F through a 140Ω resistor. This resistor is selected such that the quiescent current of the AD654 will cause less than one V_{BE} to be dropped. As the V/F oscillates, additional switched current is drawn through R_L when pin 1 goes low. The peak level of this additional current causes Q1 to saturate, and thus regenerates the AD654's output square wave at the collector. The supply voltage to the AD654 then consists of a DC level, less the resistive line drop, plus a one V_{BE} p-p square wave at the output frequency of the AD654. This ripple is reduced by the diode/capacitor combination.

To set up the receiver circuit for a given voltage, the R_S and R_L resistances are selected as shown in Table I. CMOS logic stages

$+V_S$	R_S	R_L
10V	270Ω	1.8k
15V	680Ω	2.7k

Table I.

	$(+V_S)$	R1	R2	R3	R4	R5	
K	10V	–	–	–	100k	127k	F = 10Hz/K
	15V	–	–	–	100k	127k	
°C	10V	6.49k	4.02k	1k	95.3k	22.6k	F = 10Hz/°C
	15V	12.7k	4.02k	1k	78.7k	36.5k	
°F	10V	6.49k	4.42k	1k	154k	22.6k	F = 5.55Hz/°F
	15V	12.7k	4.42k	1k	105k	36.5k	

Table II.

At the V/F end, the AD592C temperature transducer is interfaced with the AD654 in such a manner that the AD654 output frequency is proportional to temperature. The output frequency can be scaled and offset from K to °C or °F using the resistor values shown in Table II. Since temperature is the parameter of interest, an NPO ceramic capacitor is used as the timing capacitor for low V/F TC.

When scaling per K, resistors R1 – R3 and the AD589 voltage reference are not used. The AD592 produces a 1μA/K current output which drives pin 3 of the AD654. With the timing capacitor of 0.01μF this produces an output frequency scaled to 10Hz/K. When scaling per °C and °F, the AD589 and resistors R1 – R3 offset the drive current at pin 3 by 273.2μA for scaling per °C and 255.42μA for scaling per °F. This will result in frequencies scaled at 10Hz/°C and 5.55Hz/°F, respectively.

OPTOISOLATOR COUPLING

A popular method of isolated signal coupling is via optoelectronic isolators, or optocouplers. In this type of device, the signal is coupled from an input LED to an output photo-transistor, with light as the connecting medium. This technique allows DC to be transmitted, is extremely useful in overcoming ground loop problems between equipment, and is applicable over a wide range of speeds and power.

Figure 9 shows a general purpose isolated V/F circuit using a low cost 4N37 optoisolator. A +5V power supply is assumed for both the isolated (+5V isolated) and local (+5V local) supplies. The input LED of the isolator is driven from the collector output of the AD654, with a 9mA current level established by R1 for high speed, as well as for a 100% current transfer ratio.

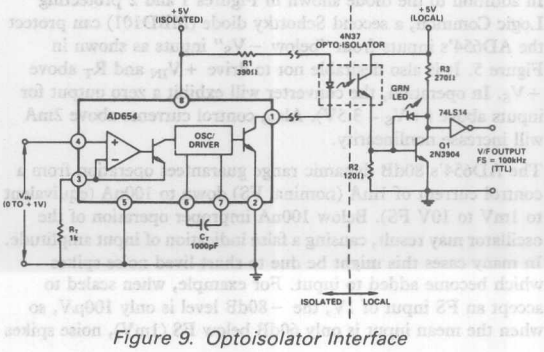


Figure 9. Optoisolator Interface

At the receiver side, the output transistor is operated in the photo-transistor mode; that is with the base lead (pin 6) open. This allows the highest possible output current. For reasonable speed in this mode, it is imperative that the load impedance be as low as possible. This is provided by the single transistor stage current-to-voltage converter, which has a dynamic load impedance of less than 10 ohms and interfaces with TTL at the output.

USING A STAND-ALONE FREQUENCY COUNTER/LED DISPLAY DRIVER FOR VOLTMETER APPLICATIONS

Figure 10 shows the AD654 used with a stand-alone frequency counter/LED display driver. With C_T = 1000pF and R_T = 1kΩ the AD654 produces an FS frequency of 100kHz when V_{IN} = +1V. This signal is fed into the ICM7226A, a universal counter system that drives common anode LED's. With the FUNCTION pin tied to D1 through a 10kΩ resistor the ICM7226A counts the frequency of the signal at A_{IN}. This count period is selected by the user and can be 10ms, 100ms, 1s, or 10 seconds, as shown on pin 21. The longer the period selected, the more resolution the count will have. The ICM7226A then displays the frequency on the LED's, driving them directly as shown. Refreshing of the LED's is handled automatically by the ICM7226. The entire circuit operates on a single +5V supply and gives a meter with 3, 4, or 5 digit resolution.

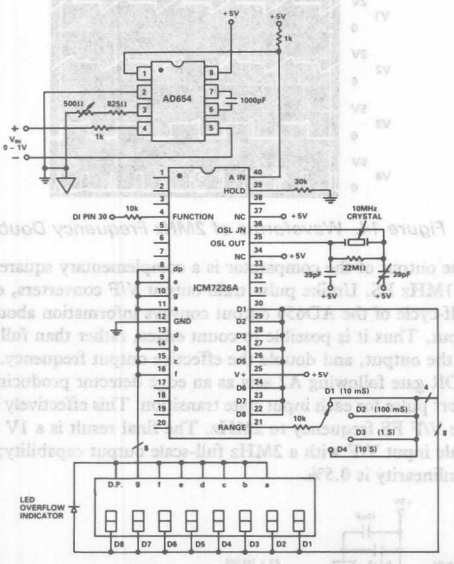


Figure 10. AD654 With Stand-Alone Frequency Counter/LED Display Driver

Longer count periods not only result in the count having more resolution, they also serve as an integration of noisy analog signals. For example, a normal-mode 60Hz sine wave riding on the input of the AD654 will result in the output frequency increasing on the positive half of the sine wave and decreasing on the negative half of the sine wave. This effect is cancelled by selecting a count period equal to an integral number of noise signal periods. A 100ms count period is effective because it not only has an integral number of 60Hz cycles (6), it also has an integral number of 50Hz cycles (5). This is also true of the 1 second and 10 second count period.

AD654-BASED ANALOG-TO-DIGITAL CONVERSION USING A SINGLE CHIP MICROCOMPUTER

The AD654 can serve as an analog-to-digital converter when used with a single component microcomputer that has an interval timer/event counter such as the 8048. Figure 11 shows the AD654, with a full scale input voltage of +1V and a full scale output frequency of 100kHz, connected to the timer/counter input pin T1 of the 8048. Such a system can also operate on a single +5V supply.

The 8748 counter is negative edge triggered; after the STRT CNT instruction is executed subsequent high to low transitions on T1 increment the counter. The maximum rate at which the counter may be incremented is once per three instruction cycles; using a 6MHz crystal, this corresponds to once every 7.5μs, or a maximum frequency of 133kHz. Because the counter overflows every 256 counts (8 bits), the timer interrupt is enabled. Each overflow then causes a jump to a subroutine where a register is incremented. After the STOP TCNT instruction is executed, the number of overflows that have occurred will be the number in this register. The number in this register multiplied by 256 plus the number in the counter will be the total number of negative edges counted during the count period. The count period is handled simply by decrementing a register the number of times necessary to correspond to the desired count time. After the register has been decremented the required number of times, the STOP TCNT instruction is executed.

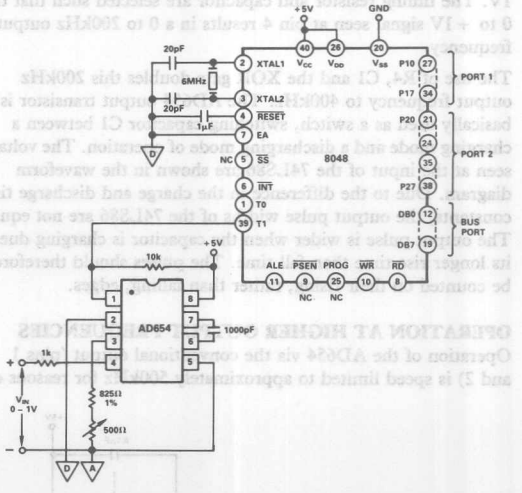


Figure 11. AD654 VFC as an ADC

The total number of negative edges counted during the count period is proportional to the input voltage. For example, if a 1V full-scale input voltage produces a 100kHz signal and the count period is 100ms, then the total count will be 10,000. Scaling from this maximum is then used to determine the input voltage, i.e., a count of 5000 corresponds to an input voltage of 0.5V. As with the ICM7226, longer count times result in counts having more resolution; and they result in the integration of noisy analog signals.

FREQUENCY DOUBLING

Since the AD654's output is a square-wave rather than a pulse train, information about the input signal is carried on both halves of the output waveform. The circuit in Figure 12 converts the output into a pulse train, effectively doubling the output frequency, while preserving the better low frequency linearity of the AD654. This circuit also accommodates an input voltage that is greater than the AD654 supply voltage.

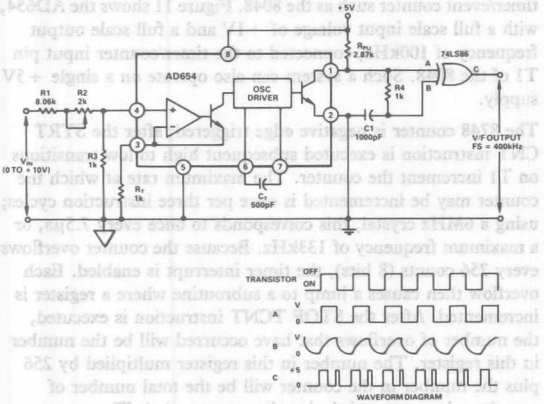


Figure 12. Frequency Doubler

Resistors R1 – R3 are used to scale the 0 to +10V input voltage down to 0 to +1V as seen at pin 4 of the AD654. Recall that V_{IN} must be less than V_{SUPPLY} −4V, or in this case less than 1V. The timing resistor and capacitor are selected such that this 0 to +1V signal seen at pin 4 results in a 0 to 200kHz output frequency.

The use of R4, C1 and the XOR gate doubles this 200kHz output frequency to 400kHz. The AD654 output transistor is basically used as a switch, switching capacitor C1 between a charging mode and a discharging mode of operation. The voltages seen at the input of the 74LS86 are shown in the waveform diagram. Due to the difference in the charge and discharge time constants, the output pulse widths of the 74LS86 are not equal. The output pulse is wider when the capacitor is charging due to its longer rise time than fall time. The pulses should therefore be counted on their rising, rather than falling, edges.

OPERATION AT HIGHER OUTPUT FREQUENCIES

Operation of the AD654 via the conventional output (pins 1 and 2) is speed limited to approximately 500kHz for reasons of TTL logic compatibility. Although the output stage may become speed limited, the multivibrator core itself is able to oscillate to 1MHz or more. The designer may take advantage of this feature in order to operate the device at frequencies in excess of 500kHz.

Figure 13 illustrates this with a circuit offering 2MHz full scale. In this circuit the AD654 is operated at a full scale (FS) of 1mA, with a C_T of 100pF. This achieves a basic device FS frequency of 1MHz across C_T. The P channel JFETs, Q1 and Q2, buffer the differential timing capacitor waveforms to a low impedance level where the push-pull signal is then AC coupled to the high speed comparator A2. Hysteresis is used, via R7, for non-ambiguous switching and to eliminate the oscillations which would otherwise occur at low frequencies.

The net result of this is a very high-speed circuit which does not compromise the AD654 dynamic range. This is a result of the FET buffers typically having only a few pA of bias current. The high end dynamic range is limited, however, by parasitic package and layout capacitances in shunt with C_T, as well as those from each node to AC ground. Minimizing the lead length between A2–6/A2–7 and Q1/Q2 in PC layout will help. A ground plane will also help stability. Figure 14 shows the waveforms V1 – V4 found at the respective points shown in Figure 13.

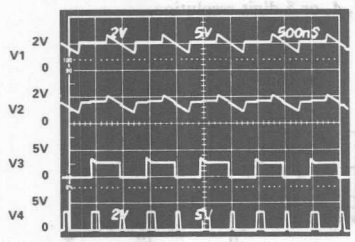


Figure 14. Waveforms of 2MHz Frequency Doubler

The output of the comparator is a complementary square wave at 1MHz FS. Unlike pulse train output V/F converters, each half-cycle of the AD654 output conveys information about the input. Thus it is possible to count edges, rather than full cycles of the output, and double the effective output frequency. The XOR gate following A2 acts as an edge detector producing a short pulse for each input state transition. This effectively doubles the V/F FS frequency to 2MHz. The final result is a 1V full scale input V/F with a 2MHz full-scale output capability; typical nonlinearity is 0.5%.

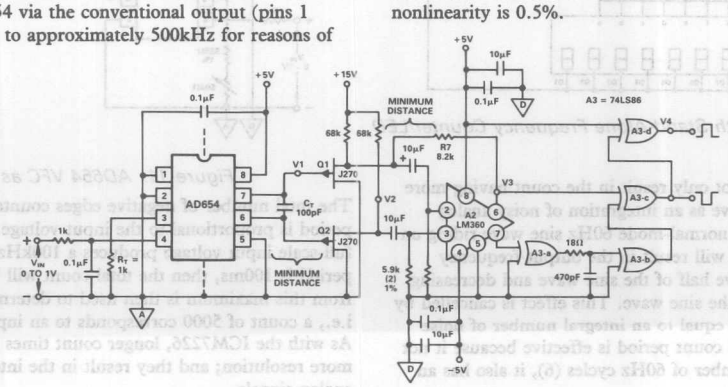


Figure 13. 2MHz, Frequency Doubling V/F

Voltage-to-Frequency and Frequency-to-Voltage Converter

ADVFC32

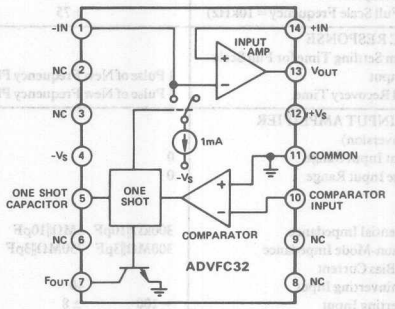
FEATURES

High Linearity
- **±0.01% max at 10kHz FS**
- **±0.05% max at 100kHz FS**
- **±0.2% max at 500kHz FS**

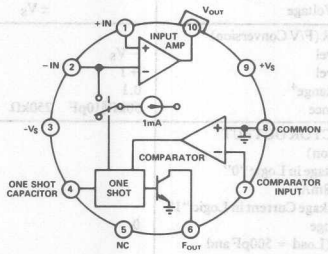
Output TTL/CMOS Compatible
V/F or F/V Conversion
6 Decade Dynamic Range
Voltage or Current Input
Reliable Monolithic Construction
MIL-STD-883 Compliant Versions Available

PIN CONFIGURATION
(TOP VIEW)

"N" PACKAGE



"H" PACKAGE – TO-100



PRODUCT DESCRIPTION

The industry standard ADVFC32 is a low cost monolithic voltage-to-frequency (V/F) converter or frequency-to-voltage (F/V) converter with good linearity (0.01% max error at 10kHz) and operating frequency up to 0.5MHz. In the V/F configuration, positive or negative input voltages or currents can be converted to a proportional frequency using only a few external components. For F/V conversion, the same components are used with a simple biasing network to accommodate a wide range of input logic levels.

TTL or CMOS compatibility is achieved in the V/F operating mode using an open collector frequency output. The pullup resistor can be connected to voltages up to 30 volts, or to +15V or +5V for conventional CMOS or TTL logic levels. This resistor should be chosen to limit current through the open collector output to 8mA. A larger resistance can be used if driving a high impedance load.

Input offset drift is only 3ppm of full scale per °C, and full scale calibration drift is held to a maximum of 100ppm/°C (ADVFC32BH) due to a low T.C. zener diode.

The ADVFC32 is available in commercial, industrial, and extended temperature grades. The commercial grade is packaged in a 14-pin plastic DIP while the two wider temperature range parts are packaged in hermetically sealed TO-100 cans.

PRODUCT HIGHLIGHTS

1. The ADVFC32 uses a charge balancing circuit technique (see Functional Block Diagram) which is well suited to high accuracy voltage-to-frequency conversion. The full-scale operating frequency is determined by only one precision resistor and capacitor. The tolerance of other support components (including the integration capacitor) is not critical. Inexpensive ±20% resistors and capacitors can be used without affecting linearity or temperature drift.
2. The ADVFC32 is easily configured to satisfy a wide range of system requirements. Input voltage scaling is set by selecting the input resistor which sets the input current to 0.25mA at the maximum input voltage.
3. The same components used for V/F conversion can also be used for F/V conversion by adding a simple logic biasing network and reconfiguring the ADVFC32.
4. The ADVFC32 is intended as a pin-for-pin replacement for VFC32 devices from other manufacturers.
5. The ADVFC32 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current ADVFC32/883B data sheet for detailed specifications.

DYNAMIC PERFORMANCE										
Full Scale Frequency Range	0		500	0		500	0		500	kHz
Nonlinearity[1]										
f_{max} = 10kHz	−0.01		±0.01	−0.01		+0.01	−0.01		+0.01	%
f_{max} = 100kHz	**−0.05**		**+0.05**	**−0.05**		**+0.05**	**−0.05**		**+0.05**	%
f_{max} = 0.5MHz	−0.20	±0.05	+0.20	−0.20	±0.05	+0.20	−0.20	±0.05	+0.20	%
Full Scale Calibration Error										
(Adjustable to Zero)		±5			±5			±5		%
vs. Supply										
(Full Scale Frequency = 100kHz)	**−0.015**		**+0.015**	**−0.015**		**+0.015**	**−0.015**		**+0.015**	% of FSR/%
vs. Temperature										
(Full Scale Frequency = 10kHz)		±75		−100		+100	**+150**		**+150**	ppm/°C
DYNAMIC RESPONSE										
Maximum Settling Time for Full Scale										
Step Input	1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			
Overload Recovery Time	1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			
ANALOG INPUT AMPLIFIER										
(V/F Conversion)										
Current Input Range	0		+0.25	0		+0.25	0		+0.25	mA
Voltage Input Range	0		−10	0		−10	0		−10	V[2]
			0.25 × R_{IN}[3]			0.25 × R_{IN}[3]			0.25 × R_{IN}[3]	mA
Differential Impedance	300kΩ‖10pF	2MΩ‖10pF		300kΩ‖10pF	2MΩ‖10pF		300kΩ‖10pF	2MΩ‖10pF		
Common-Mode Impedance	300MΩ‖3pF	750MΩ‖3pF		300MΩ‖3pF	750MΩ‖10pF		300MΩ‖3pF	750MΩ‖10pF		
Input Bias Current										
Noninverting Input		40	**250**		40	**250**		40	**250**	nA
Inverting Input	**−100**	±8	**+100**	**−100**	±8	**+100**	**−100**	±8	**+100**	nA
Input Offset Voltage										
(Trimmable to Zero)[2,3]			**4**			**4**			**4**	mV
vs. Temperature (T_{min} to T_{max})			30			30			**30**	µV/°C
Safe Input Voltage		±V_S			±V_S			±V_S		
COMPARATOR (F/V Conversion)										
Logic "0" Level	−V_S		−0.6	−V_S		−0.6	−V_S		−0.6	V
Logic "1" Level	+1		+V_S	+1		+V_S	+1		+V_S	V
Pulse Width Range[4]	0.1		0.15/f_{max}	0.1		0.15/f_{max}	0.1		0.15/f_{max}	µs
Input Impedance	50kΩ‖10pF	250kΩ		50kΩ‖10pF	250kΩ		50kΩ‖10pF	250kΩ		
OPEN COLLECTOR OUTPUT										
(V/F Conversion)										
Output Voltage in Logic "0"										
I_{SINK} = 8mA			**0.4**			**0.4**			**0.4**	V
Output Leakage Current in Logic "1"			**1**			**1**			**1**	µA
Voltage Range	0		+30	0		+30	0		+30	V
Fall Times (Load = 500pF and										
I_{SINK} = 5mA)			400			400			400	ns
AMPLIFIER OUTPUT (F/V Conversion)										
Voltage Range (0mA≤I_O≤7mA)	0		+10	0		+10	0		+10	V
Source Current (0≤V_O≤7V)	10			10			10			mA
Capacitive Load (Without Oscillation)			100			100			100	pF
Closed Loop Output Impedance			1			1			1	Ω
POWER SUPPLY										
Rated Voltage		±15			±15			±15		V
Voltage Range	±9		±18	±9		±18	±9		±18	V
Quiescent Current		6	8		6	8		6	8	mA
TEMPERATURE RANGE										
Specified Range	0		+70	−25		+85	−55		+125	°C
Operating Range	−25		+85	−55		+125	−55		+125	°C
Storage	−25		+85	−65		+150	−65		+150	°C
PACKAGE OPTIONS[5,6]										
Plastic DIP (N-14)	ADVFC32KN									
TO-100 (H-10A)				ADVFC32BH			ADVFC32SH			

NOTES

[1]Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a percentage of full scale.

[2]See Figure 3.

[3]See Figure 1.

[4]f_{max} expressed in units of MHz.

[5]N = Plastic DIP; H = Hermetic Metal Can. For outline information see Package Information section.

[6]For ADVFC32/883B specifications, refer to Analog Devices Military Products Databook.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ORDERING GUIDE

Model[1]	Gain Tempco ppm/°C	Temp Range °C	Package
ADVFC32KN	±75 typ	0 to +70	14-Pin Plastic DIP
ADVFC32BH	±100 max	−25 to +85	TO-100
ADVFC32SH	±150 max	−55 to +125	TO-100

NOTE
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current ADVFC32/883B data sheet.

3

UNIPOLAR V/F, POSITIVE INPUT VOLTAGE

When operated as a V/F converter, the transformation from voltage to frequency is based on a comparison of input signal magnitude to the 1mA internal current source.

A more complete understanding of the ADVFC32 requires a close examination of the internal circuitry of this part. Consider the operation of the ADVFC32 when connected as shown in Figure 1. At the start of a cycle, a current proportional to the

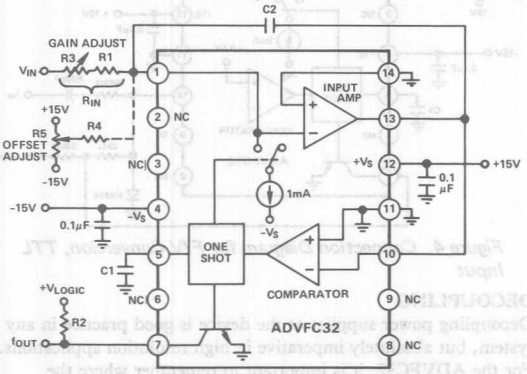


Figure 1. Connection Diagram for V/F Conversion, Positive Input Voltage

input voltage flows through R3 and R1 to charge integration capacitor C2. As charge builds up on C2, the output voltage of the input amplifier decreases. When the amplifier output voltage (pin 13) crosses ground (see Figure 2 at time t_1), the comparator

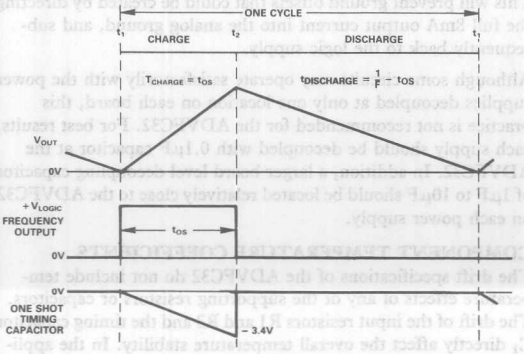


Figure 2. Voltage-to-Frequency Conversion Waveforms

triggers a one shot whose time period is determined by capacitor C1. Specifically, the one shot time period (in nanoseconds) is:

$$t_{OS} \cong (C_1 + 44pF) \times 6.7k\Omega$$

During this period, a current of $(1mA - I_{IN})$ flows out of the integration capacitor. The total amount of charge depleted during one cycle is, therefore $(1mA - I_{IN}) \times t_{OS}$. This charge is replaced during the remainder of the cycle to return the integrator to its original voltage. Since the charge taken out of C2 is equal to the charge that is put on C2 every cycle,

$$(1mA - I_{IN}) \times t_{OS} = I_{IN} \times \left(\frac{1}{F_{OUT}} - t_{OS} \right)$$

or, rearranging terms,

$$F_{OUT} = \frac{I_{IN}}{1mA \times t_{OS}}$$

The complete transfer equation can now be derived by substituting $I_{IN} = V_{IN}/R_{IN}$ and the equation relating C1 and t_{OS}. The final equation describing ADVFC32 operation is:

$$F_{OUT} = \frac{V_{IN}/R_{IN}}{1mA \times (C_1 + 44pF) \times 6.7k\Omega}$$

Components should be selected to optimize performance over the desired input voltage and output frequency range using the equations listed below:

$$C_1 = \frac{3.7 \times 10^7 pF/sec}{F_{OUT\ FS}} - 44pF$$

$$C_2 = \frac{10^{-4}\ Farads/sec}{F_{OUT\ FS}} \quad (1000pF\ minimum)$$

$$R_{IN} = \frac{V_{IN\ FS}}{0.25mA}$$

$$R_2 \geq \frac{+V_{LOGIC}}{8mA}$$

Both R_{IN} and C_1 should have very low temperature coefficients as changes in their values will result in a proportionate change in the V/F transfer function. Other component values and temperature coefficients are not critical.

Table I. Suggested Values for C_1, R_{IN} and C_2

$V_{IN\ FS}$	$F_{OUT\ FS}$	C_1	R_{IN}	C_2
1V	10kHz	3650pF	4.0kΩ	0.01μF
10V	10kHz	3650pF	40kΩ	0.01μF
1V	100kHz	330pF	4.0kΩ	1000pF
10V	100kHz	330pF	40kΩ	1000pF

Input resistance R_{IN} is composed of a fixed resistor (R1) and a variable resistor (R3) to allow for initial gain error compensation. To cover all possible situations, R3 should be 20% of R_{IN}, and R1 should be 90% of R_{IN}. This allows a ±10% gain adjustment to compensate for the ADVFC32 full-scale error and the tolerance of C1.

If more accurate initial offset is required, the circuit of R4 and R5 can be added. R5 can have a value between 10kΩ and 100kΩ, and R4 should be approximately 10MΩ. The amount of current required to trim zero offset will be relatively small, so the temperature coefficients of these resistors are not critical. If large offsets are added using this circuit, temperature drift of both of these resistors is much more important.

BIPOLAR V/F

By adding another resistor from pin 1 (pin 2 of TO-100 can) to a stable positive voltage, the ADVFC32 can be operated with a bipolar input voltage. For example, an 80kΩ resistor to +10V causes an additional current of 0.125mA to flow into the integrator so that the net current flow to the integrator is positive even for negative input voltages. At negative full scale input voltage, 0.125mA will flow into the integrator from V_{IN} cancelling out the 0.125mA from the offset resistor, resulting in an output frequency of zero. At positive full scale, the sum of the two currents will be 0.25mA and the output will be at its maximum frequency.

UNIPOLAR V/F, NEGATIVE INPUT VOLTAGE

Figure 3 shows the connection diagram for V/F conversion of negative input voltages. In this configuration full scale output frequency occurs at negative full scale input, and zero output frequency corresponds to zero input voltage.

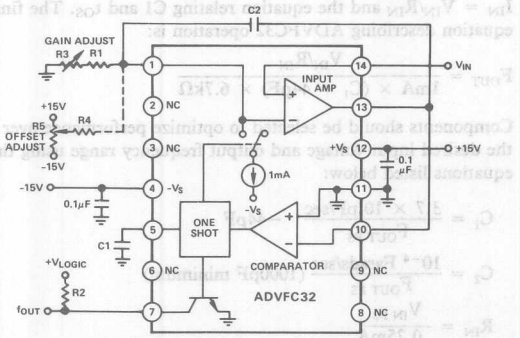


Figure 3. Connection Diagram for V/F Conversion, Negative Input Voltage

A very high impedance signal source may be used since it only drive the noninverting integrator input. Typical input impedance at this terminal is 250MΩ or higher. For V/F conversion of positive input signals the signal generator must be able to source 0.25mA to properly drive the ADVFC32, but for negative V/F conversion the 0.25mA integration current is drawn from ground through R1 and R3.

Circuit operation for negative input voltages is very similar to positive input unipolar conversion described in the previous section. For best operating results use component equations listed in that section.

F/V CONVERSION

Although the mathematics of F/V conversion can be very complex, the basic principle is easy to understand. Figure 4 shows the connection diagram for F/V conversion with TTL input logic levels. Each time the input signal crosses the comparator threshold going negative, the one shot is activated and switches 1mA into the integrator input for a measured time period (determined by C1). As the frequency increases, the amount of charge injected into the integration capacitor increases proportionately. The voltage across the integration capacitor is stabilized when the leakage current through R1 and R3 equals the average current being switched into the integrator. The net result of these two effects is an average output voltage which is proportional to the input frequency. Optimum performance can be obtained by selecting components using the same guidelines and equations listed in the V/F conversion section.

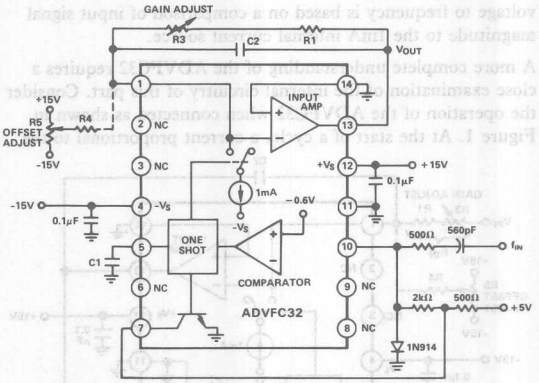


Figure 4. Connection Diagram for F/V Conversion, TTL Input

DECOUPLING

Decoupling power supplies at the device is good practice in any system, but absolutely imperative in high resolution applications. For the ADVFC32, it is important to remember where the voltage transients and ground currents flow. For example, the current drawn through the output pulldown transistor originates from the logic supply, and is directed to ground through pin 11 (pin 8 of TO-100). Therefore, the logic supply should be decoupled near the ADVFC32 to provide a low impedance return path for switching transients. Also, if there is a separate digital ground it should be connected to the analog ground at the ADVFC32. This will prevent ground offsets that could be created by directing the full 8mA output current into the analog ground, and subsequently back to the logic supply.

Although some circuits may operate satisfactorily with the power supplies decoupled at only one location on each board, this practice is not recommended for the ADVFC32. For best results, each supply should be decoupled with 0.1µF capacitor at the ADVFC32. In addition, a larger board level decoupling capacitor of 1µF to 10µF should be located relatively close to the ADVFC32 on each power supply.

COMPONENT TEMPERATURE COEFFICIENTS

The drift specifications of the ADVFC32 do not include temperature effects of any of the supporting resistors or capacitors. The drift of the input resistors R1 and R3 and the timing capacitor C_1 directly affect the overall temperature stability. In the application of Figure 2, a 10ppm/°C input resistor used with a

100ppm/°C capacitor may result in a maximum overall circuit gain drift of:

100ppm/°C (ADVFC32BH) + 100ppm/°C (C1) + 10ppm/°C (R_{IN}) = 210ppm/°C

Although R_{IN} and C_1 have the most pronounced effect on temperature stability, the offset circuit of resistors R4 and R5 may also have a slight effect on the offset temperature drift of the circuit. The offset will change with variations in the resistance of R4 and supply voltage changes. In most applications the offset adjustment is very small, and the offset drift attributable to this circuit will be negligible. In the bipolar mode, however, both the positive reference and the resistor used to offset the signal range will have a pronounced effect on offset drift. A high quality reference and resistor should be used to minimize offset drift errors.

Other circuit components do not directly influence temperature performance as long as their actual values are not so different from nominal value as to preclude operation. This includes integration capacitor C2. A change in the capacitance value of C2 results in a different rate of voltage change across C2, but this is compensated by an equal effect when C2 is discharged by the switched 1mA current source so that no net effect occurs.

The temperature effects of the components described above are the same when the ADVFC32 is configured for negative or bipolar input ranges, or F/V conversion.

OTHER CIRCUIT CONSIDERATIONS

The input amplifier connected to pins 1, 13, and 14 is not a standard operational amplifier. Although it operates like an op amp in most applications, two key differences should be noted. First, the bias current of the positive input is typically 40nA while the bias current of the inverting input is ±8nA. Therefore, any attempt to cancel input offset voltage due to bias currents by matching input resistors will create worse offsets. Second, the output of this amplifier will sink only 1mA, even though it will source as much as 10mA. When used in the F/V mode, the amplifier must be buffered if large sink currents are required.

MICROPROCESSOR OPERATED A/D CONVERTER

With the addition of a few external components the ADVFC32 can be used as a ±10V A/D microprocessor front end. Although the nonlinearity of the ADVFC32 is only 0.05% maximum (0.01% typ), the resolution is much higher, allowing it to be used in 16-bit measurement and control systems where a monotonic transfer function is essential. The resolution of the circuit shown in Figure 5 is dependent on the amount of time allowed to count the ADVFC32 frequency output. Using a full scale frequency of 100kHz, an 8-bit conversion can be made in about 10ms, and a 2 second time period allows a 16-bit measurement, including offset and gain calibration cycles.

As shown in Figure 5, the input signal is selected via the AD7590 input multiplexer. Positive and negative references as well as a ground input are provided to calibrate the A/D. This is very important in systems subject to moderate or extreme temperature changes since the gain temperature coefficient of the ADVFC32 is as high as ±150ppm/°C. By using the calibration cycles, the A/D conversion will be as accurate as the references provided. The AD542 following the input multiplexer provides a high impedance input (10^{12} ohms) and buffers the switch resistance from the relatively low impedance ADVFC32 input.

If higher linearity is required, the ADVFC32 can be operated at 10kHz, but this will require a proportionately longer conversion time. Conversely, the conversion time can be decreased at the expense of nonlinearity by increasing the maximum frequency to as high as 500kHz.

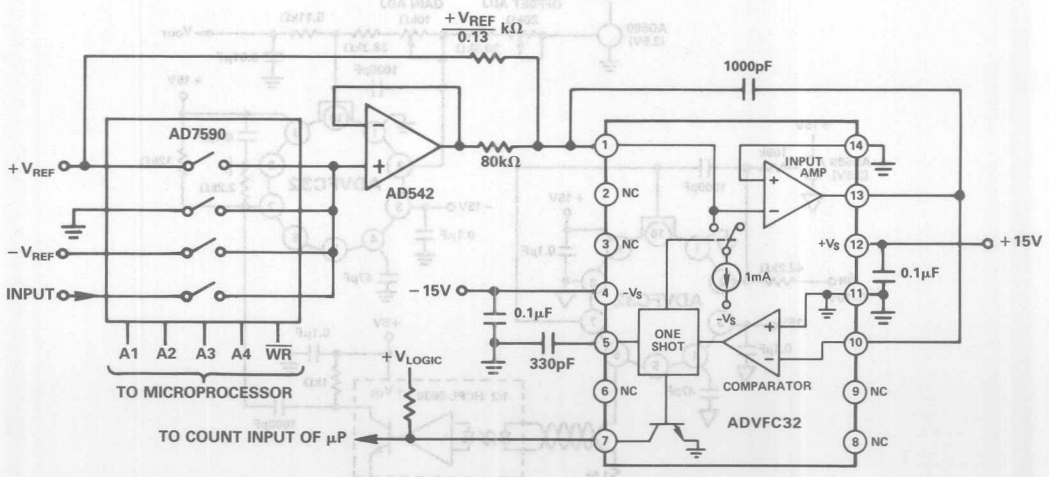


Figure 5. High Resolution, Self-Calibrating, Microprocessor Operated A/D Converter

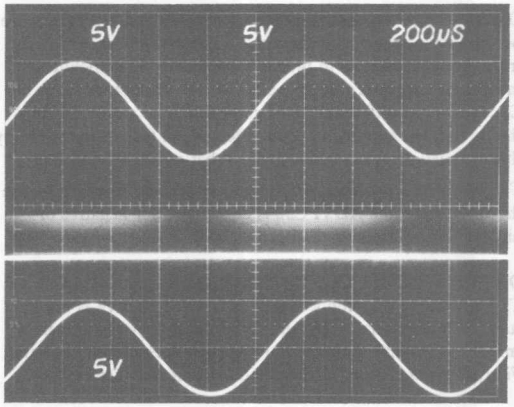
LINK

In many applications, a signal must be sensed at a remote site and sent through a very noisy environment to a central location for further processing. In these cases, even a shielded cable may not protect the signal from noise pickup. The circuit of Figure 6 provides a solution in these cases. Due to the optocoupler and voltage-to-frequency conversion, this data link is extremely insensitive to noise and common mode voltage interference. For even more protection, an optical fiber link substituted for the HCPL2630 will provide common mode rejection of more than several hundred kilovolts and virtually total immunity to electrical noise. For most applications, however, the frequency modulated signal has sufficient noise immunity without using an optical fiber link, and the optocoupler provides common mode isolation up to 3000V dc.

The data link input voltage is changed in a frequency modulated signal by the first ADVFC32. A 42.2kΩ input resistor and a 100kΩ offset resistor set the scaling so that a 0V input signal corresponds to 50kHz, and a 10V input results in the maximum output frequency of 500kHz. A high frequency optocoupler is then used to transmit the signal across any common mode voltage potentials to the receiving ADVFC32. The optocoupler is not necessary in systems where common mode noise is either very small or a constant low level dc voltage. In systems where common mode voltage may present a problem, the connection between the two locations should be through the optocoupler; no power or ground connections need to be made.

The output of the optocoupler drives an ADVFC32 hooked up in the F/V configuration. Since the reconstructed signal at pin 10 has a considerable amount of carrier feedthrough, it is desirable to filter out any frequencies in the carrier range of 50kHz to 500kHz. The frequency response of the F/V converter is only 3kHz due to the pole made by the integrator, so a second 3kHz filter will not significantly limit the bandwidth. With the simple one pole filter shown in Figure 6, the input to output 3dB point is approximately 2kHz, and the output noise is less than 15mV. If a lower output impedance drive is needed, a two pole active filter is recommended as an output stage.

Although the F/V conversion technique used in this circuit is quite simple, it is also very limited in terms of its frequency response and output ripple. The frequency response is limited by the integrator time constant and while it is possible to decrease that time constant, either signal range or output ripple must be sacrificed. The performance of the circuit of Figure 6 is shown in the photograph below. The top trace is the input signal, the middle trace is the frequency-modulated signal at the optocoupler's output, and the bottom trace is the recovered signal at the output of the F/V converter.



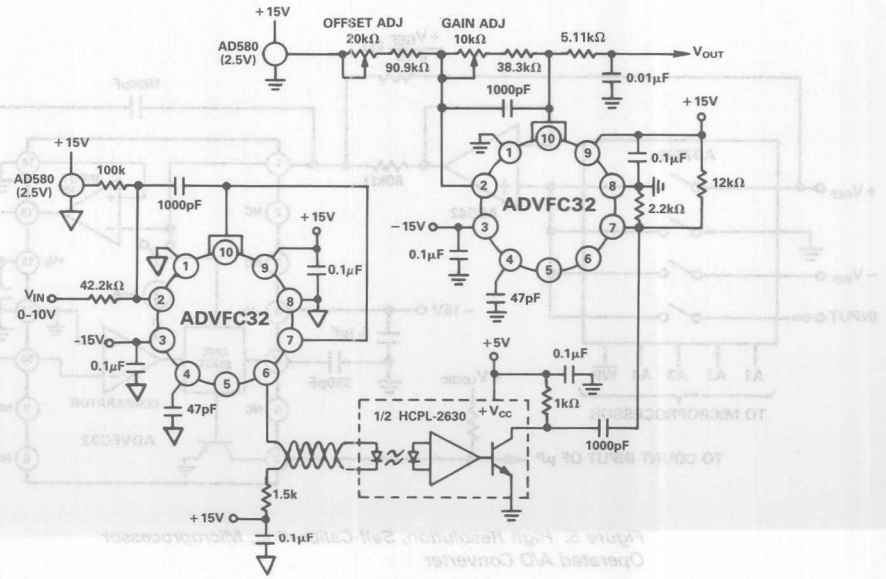


Figure 6. High Noise Immunity Data Link

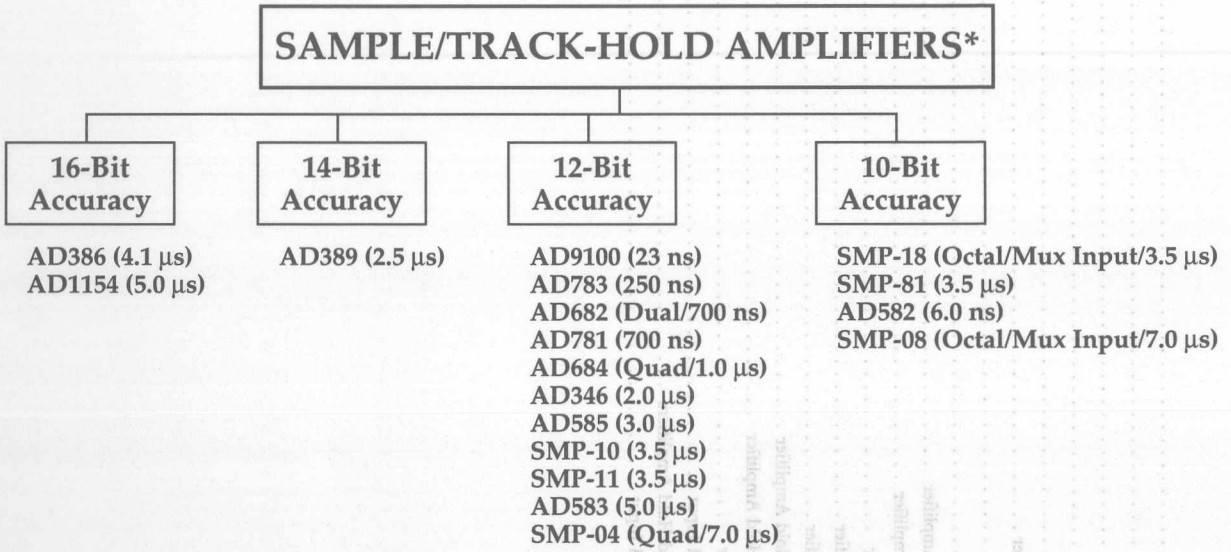
Sample/Track-Hold Amplifiers
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4

Selection Tree
Sample and Hold Amplifiers



*Times noted are acquisition times to rated accuracy

Selection Guide
Sample/Track-Hold Amplifiers

Model	Specified Accuracy %	Acquisition Time µs max	Aperture Time ns typ	Aperture Jitter ns typ	Droop Rate µV/µs max	Package Options[1]	Temp Range[2]	Page	Comments
AD1154	**0.00076**	**5.0**	**80**	**0.15**	**0.1**	**13**	**C, I**	**C II 4–69**	**Low Cost 16-Bit Accurate, High Speed Amplifier**
AD386	**0.00076**	**4.1**	**12**	**0.04**	**0.1**	**1**	**C, M**	**C II 4–11**	**High Resolution, High Speed Track-and-Hold Amplifier**
AD389	**0.003**	**2.5**	**30**	**0.4**	**0.1**	**1**	**C, I**	**C II 4–25**	**High Resolution Track-and-Hold Amplifier**
***AD9100**	**0.01**	**0.023**	**0.8**	**<0.001**	**6000**	**1, 14**	**C, I, M**	**C II 4–75**	**Ultrahigh Speed Monolithic T/H, Low Distortion**
***AD783**	**0.01**	**0.25**	**15**	**0.01**	**1**	**2, 3**	**C, I, M**	**C II 4–65**	**Complete 250 ns Sample-and-Hold Amplifier**
***AD781**	**0.01**	**0.7**	**25**	**0.05**	**1**	**2, 3**	**C, I, M**	**C II 4–57**	**Complete 700 ns Sample-and-Hold Amplifier**
***AD682**	**0.01**	**0.7**	**25**	**0.05**	**1**	**2, 3**	**C, I, M**	**C II 4–41**	**Two-Channel 700 ns Sample-and-Hold Amplifier**
AD684	**0.01**	**1.0**	**20**	**0.1**	**1**	**3**	**C, I, M**	**C II 4–49**	**Quad, Monolithic 1 µs SHA**
AD346	0.01	2.0	60	0.4	0.5	1	C, M	C II 4–7	High Speed Sample-and-Hold, Industry Standard
AD585	**0.01**	**3.0**	**35**	**0.5**	**1**	**3, 4, 5**	**C, I, M**	**C II 4–35**	**High Speed, Precision, On-Board Hold Cap**
SMP-10	**0.01**	**3.5**	**50**	**1**	**0.02**	**3**	**C, M**	**C II 4–109**	**Low Droop Rate, High Sample/Hold Current Ratio**
SMP-11	**0.01**	**3.5**	**50**	**1**	**0.2**	**2, 3**	**C, I, M**	**C II 4–109**	**Low Droop Rate, Fast Hold Mode Settling Time**
***SMP-18**	**0.01**	**3.5**	**—**	**—**	**0.04**	**2, 3, 6**	**I**	**C II 4–119**	**Fast SMP-08**
AD583	0.01	5.0	50	5		1	C	C II 4–33	5 µs SHA
SMP-04	**0.01**	**7.0**	**—**	**—**	**0.025**	**2, 3, 6**	**I, M**	**C II 4–87**	**CMOS, Quad Sample-and-Hold Amplifier**
SMP-81	0.045	3.5	50	1	2.0	3	I	C II 12–4	High Accuracy, Fast Acquisition for PCM Encodes
AD582	0.1	6.0	200	15		1, 8	C, M	C II 4–29	Low Cost, 15 µs
SMP-08	**0.1**	**7.0**	**—**	**—**	**0.02**	**2, 3, 6**	**I, M**	**C II 4–101**	**Octal, Sample-and-Hold with Multiplexed Input**

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-In-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92.
[2]Temperature Ranges: C = Commercial, 0 to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.
*New product since the publication of the most recent Databooks.

Sample-and-Hold Amplifiers

A sample-and-hold amplifier (SHA) is a device that samples an analog input signal then holds the instantaneous value upon the command of a logic control signal. This device is basically an analog memory where a capacitor serves as the storage element. The most prevalent application is in data acquisition in which the SHA is used to capture the last instantaneous sampled analog input voltage prior to a conversion and hold this sample with minimal degradation during the conversion process. In signal processing applications using A/D converters with a subranging or successive approximation architecture, a SHA is used with the A/D converter to maximize the system's full potential bandwidth. Significant improvement in dynamic performance can be made by placing a fast SHA with low aperture jitter ahead of flash A/D converters. Other applications for a SHA include D/A deglitchers, simultaneous sampling systems, peak detectors, pulse stretchers, delay lines, and data distribution systems.

Most SHAs and track-and-holds are identical in both function and circuit implementation. The only distinction between them is in how they are used in the system. A sample-and-hold (SHA) implies that the device samples a signal for a short time and remains in the hold mode for the remainder of the cycle. Conversely, a track-and-hold will spend the majority of the time in the track mode and be switched into the hold mode for brief intervals. Some SHAs compromise their TRACK mode performance in order to improve their HOLD mode performance, and are not recommended for track-and-hold applications. At throughput rates greater than a 1 MHz, this distinction between the two definitions becomes less obvious.

SHA CIRCUITRY AND HARDWARE

The four major functional blocks common to all SHAs are shown in Figure 1. They are the input amplifier, the energy storage device (hold capacitor), the output amplifier, and the switching circuits. The input amplifier serves as a buffer to the signal source, as well as providing current gain to charge the hold capacitor. The hold capacitor usually determines the frequency response of the SHA and retains the last sampled voltage. The output buffer amplifier provides a high impedance to the hold capacitor to minimize the output voltage droop rate. The switching circuit and its driver form the mechanism by which the hold capacitor is alternately switched between the sample and the hold mode of operation. The actual analog switch may be a FET switch or a diode bridge.

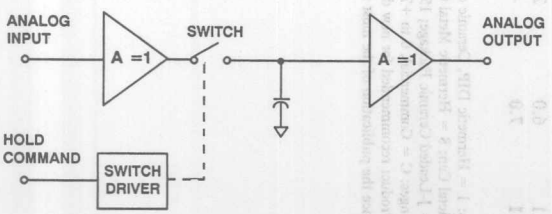


Figure 1. Basic Sample-and-Hold Amplifier

SHA design topologies fall into two categories: open- or closed-loop circuits. Closed-loop SHAs usually contain a high performance input amplifier, a switch, and an output buffer amplifier. The output buffer can be configured as either a voltage follower (i.e., AD583), or as an integrating amplifier (i.e., AD585) which decreases leakage currents by referencing the analog switch to ground. The closed-loop configuration exploits such advantages as gain flexibility, higher accuracy and higher linearity due to overall loop feedback. A tradeoff in accuracy versus speed (i.e., bandwidth, acquisition time, settling time) exists due to overall loop dynamics in which the hold capacitor value helps determine the frequency response and acquisition time. A derivative of this closed-loop topology which is used in the AD680 and AD780 series contains a unique "self correcting" architecture to improve the overall speed and accuracy by nulling out many of the errors accumulated in the sample mode. This particular architecture compromises the performance in the sample mode to achieve high performance in the hold mode.

Conversely, open-loop circuits exploit the characteristics of high-speed unity gain buffer amplifiers and high speed diode bridges to achieve high speed specifications at the expense of overall accuracy (due to the lack of overall loop feedback). A derivative of this topology, used in the AD9100, integrates the high speed diode bridge, a major source of distortion, into the buffer amplifier. This configuration improves upon the overall distortion specifications and provides 10-bit performance at ultrahigh speeds. Another extension of this topology implemented in the SMP-10 and SMP-11 use a super-charger circuit to enhance the slew rate. The super-charger circuit supplements the capacitor charging current whenever the difference between the input and output levels exceeds a given threshold.

PERFORMANCE

The performance of a SHA is described by dynamic and static specifications pertaining to both the sample and the hold mode of operation as well as the transition states between these two modes. Figure 2 displays a complete cycle from the sample-to-hold mode and back with the various error sources exaggerated for tutorial purposes. These groups which define the state of operation of the SHA can be described by both static and dynamic specification. Table I provides an outline of the various dynamic and static specifications associated with the SHA's two modes and transition states. Since a SHA in the sample mode is simply a limited bandwidth amplifier, both the dynamic and static specifications listed in this mode are similar to those of any amplifier. The error sources in the hold mode are due to

Table I. Sample-and-Hold Specifications

Sample Mode	Sample-to-Hold Transition	Hold Mode	Sample-to-Track Transition
STATIC Offset Nonlinearity	STATIC Pedestal (Sample-to-Hold Offset) Pedestal Nonlinearity	STATIC Droop Dielectric Absorption	
DYNAMIC Settling Time Bandwidth Harmonic Distortion Slew Rate	DYNAMIC Switch Aperture Time Effective Aperture Delay Time Aperture Jitter Switch Delay Time Switching Transient	DYNAMIC Feedthrough Distortion + Noise	DYNAMIC Acquisition Time Switching Transient

imperfections in the switch, the output amplifier, and the hold capacitor. Some SHAs specify ac distortion specifications in the hold mode, which provide a simple means of characterizing a particular SHA's performance in a sampled data system.

The specifications of the sample-and-hold transition are particularly relevant in understanding the sources of nonlinearity and thus distortion, as well as in determining the precise time to strobe the device with respect to the input signal. The key specification in the hold-to-sample transition is the acquisition time to a specified percent since this affects the overall achievable throughput rate of a particular sampled data system. Another important specification is the total output noise, which is the rms sum of the output noise of the output amplifier in the hold mode and the dc sampled uncertainty due to aperture jitter. This error source will lower the S/N of the system and thus degrade overall system accuracy. The following definitions of specifications represent a culmination and combination of the various error sources discussed.

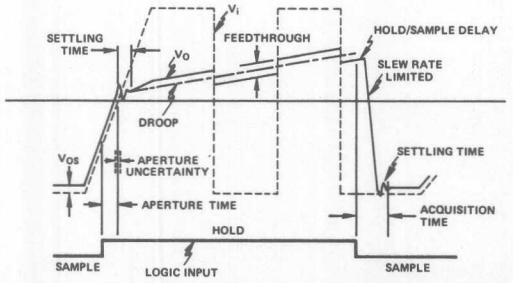


Figure 2. Complete SHA Cycle

DEFINITIONS

Acquisition Time (t_{AQ})
The minimum time for the output voltage to begin tracking the input voltage, to within a specified error band, after the beginning of the sample command. Included are switch-delay time, the slewing interval and settling time for a specified output-voltage change.

Aperture (Delay) Time (t_{AP})
The time required after the hold command for the switch to open fully. The sample is in effect delayed by this interval and the hold command would have to be advanced by this amount for precise timing.

Aperture Jitter or Aperture Uncertainty
The maximum amount of deviation in aperture time from sample to sample, due to noise modulating the phase of the hold command. This deviation manifests itself as an aperture error which is proportional to the slew rate of the sampled analog input signal.

Charge Transfer or Offset Step (Q_T)
The charge transferred to the storage capacitor via stray capacitance when switching to the hold mode. The associated voltage error (Q_T/C) which contributes to pedestal may be reduced by using greater capacitance for storage, but this increases response time.

Droop Rate (dV_{CH}/dt)
The change of the output voltage during the hold mode as a result of leakage or bias currents flowing through the storage capacitor. Its polarity depends on the sources of leakage current or droop current (I_{DR}) within a given device and its magnitude is equal to I_{DR}/C_H.

Feedthrough (F_A)
The fraction of the input signal variation or ac input waveform that appears at the output in the hold mode. It is caused by stray capacitive coupling from the input to the storage capacitor, principally across the open switch.

Full Power Bandwidth (F_P)
The maximum frequency at which rated output voltage E_P can be supplied without significant distortion.

Gain Error
The voltage difference between input and output voltages measured over a specified voltage range, assuming the ideal gain is unity.

Hold Capacitor Charging Current (I_{CH})
The current which charges, or discharges the hold capacitor C_H while the circuit is in the sample mode.

Hold Mode Distortion
Signal-to-Noise Ratio Plus Distortion (S/N+D), Total Harmonic Distortion (THD), Intermodulation Distortion (IMD), and Spurious Free Dynamic Range (SFDR) are all specifications that measure a SHA's performance in the hold mode and its effect on system accuracy.

Hold Mode or Sample-to-Hold Settling Time (t_{HM})
The time for all output transients to settle within a specified error band. Measured from the inception of the hold command.

Hold Step (V_{HS})
Magnitude of step caused in the output voltage by switching the circuit from the sample mode to hold mode.

Input Bias Current (I_B)
Input terminal current with input voltage held at zero volts.

Input Resistance or Impedance (R_{IN})
AC impedance measured as a ratio of input voltage V_{IN} to input current.

Leakage (Droop) Current (I_{DR})
The current which flows out of the hold capacitor C_H while the circuit is operating in the hold mode. In general, droop current is defined positive when its direction is into the C_H pin.

Linearity Error
The maximum deviation from an ideal straight line drawn between the output voltage when V_{IN} = maximum analog voltage, expressed as a percentage of the maximum analog voltage.

Output Resistance (R_O)
An ac change in output voltage as a result of an ac change in load current.

Sample Hold Current Ratio (I_{CH}/I_{DR})
The ratio of the peak charging current available to the droop current.

Sample-to-Hold Offset or Pedestal
A shift in level between the last value in the sample mode and the value to which the output settles in the hold output mode, is the residual step error after the charge transfer is accounted for and/or cancelled. Since it is unpredictable in magnitude and may be a function of the signal, it is also known as offset nonlinearity.

Signal Transfer Nonlinearity
The total input to output hold mode error caused by gain nonlinearity, feedthrough, thermal transient, charge transfer and droop rate. These error terms cannot be corrected by offset and gain adjustments.

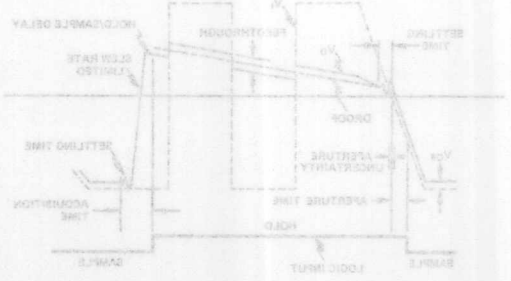
Slew Rate (SR)
The maximum possible rate of change of the output voltage when supplying the rated output. For a SHA, slew rate must be defined with a specified value of holding capacitor C_H.

Total Error
The algebraic sum of the following factors:

i. Zero-Scale Error
ii. Gain Error
iii. Hold Step Change versus $dV_{(S/H)}/dt$
iv. Hold Step Change versus V_{IN}

Voltage Gain (A_V)
The ratio of the output voltage to the input voltage with the circuit operating in the sample mode.

Zero-Scale Error (V_{ZS})
The magnitude of the output voltage when the circuit is switched from sample mode to hold mode while holding the input at zero volts. Zero-Scale Error V_{ZS} is the algebraic sum of the offset voltage and the charge transfer hold step voltage. V_{ZS} can be adjusted to zero.



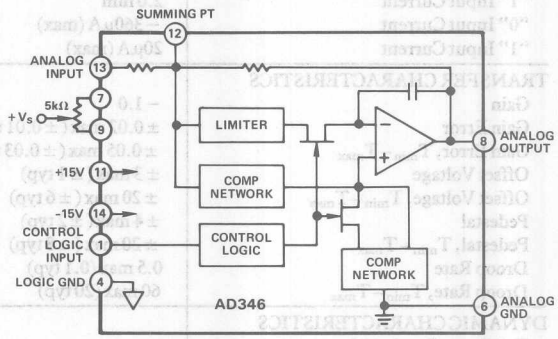
High Speed Sample-and-Hold Amplifier

AD346

FEATURES

Fast 2.0μs Acquisition Time to ±0.01%
Low Droop Rate: 0.5mV/ms
Low Offset
Low Glitch: <40mV
Aperture Jitter: 400ps
Extended Temperature Range: −55°C to +125°C
Internal Hold Capacitor
MIL-STD-883B Processing Available

FUNCTIONAL BLOCK DIAGRAM



4

PRODUCT DESCRIPTION

The AD346 is a high speed (2μs to 0.01%), adjustment free sample-and-hold amplifier designed for high throughput rate data acquisition applications. The fast acquisition time (2μs to 0.01%) and low aperture jitter (400ps) make it suitable for use with fast A/D converters to digitize signals up to 97kHz.

The AD346 is complete with an internal hold capacitor and it incorporates a compensation network which minimizes the sample to hold charge offset. The AD346 is also laser trimmed to eliminate the need for external trimming potentiometers.

Typical applications for the AD346 include sampled data systems, D/A deglitchers, peak hold functions, strobed measurement systems and simultaneous sampling converter systems.

The device is available in two versions: the "J" specified for operation over the 0 to +70°C commercial temperature range and the "S" specified over the extended temperature range, −55°C to +125°C.

ORDERING GUIDE

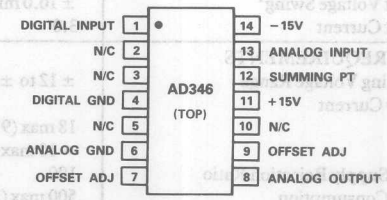
Model	Temperature Range	Package Option*
AD346JD	0 to +70°C	DH-14A
AD346SD	−55°C to +125°C	DH-14A
AD346SD/883B	−55°C to +125°C	DH-14A

*DH-14A = Ceramic DIP. For outline information see Package Outline section.

PRODUCT HIGHLIGHTS

1. The AD346 is an improved second source for other sample and holds of the same pin configuration.
2. The AD346 provides separate analog and digital grounds, thus improving the device's immunity to ground and switching transients.
3. The droop rate is only 0.5mV/ms so that it may be used in slower high accuracy systems without the loss of accuracy.
4. The fast acquisition time and low aperture make it suitable for very high speed data acquisition systems.

PIN CONFIGURATION



AD346—SPECIFICATIONS (typical @ +25°C, V_S = ±15V unless otherwise noted)

Model	AD346JD	AD346SD	Units
ANALOG INPUT			
Voltage Range	±10.0	*	Volts
Input Impedance	3.0	*	kΩ
DIGITAL INPUT			
"0" Input Threshold Voltage (Hold)	+0.8 max	*	Volts
"1" Input Current	2.0 min	*	Volts
"0" Input Current	−360μA (max)	*	μA
"1" Input Current	20μA (max)	*	μA
TRANSFER CHARACTERISTICS			
Gain	−1.0	*	V/V
Gain Error	±0.02 max (±0.01 typ)	*	% FSR
Gain Error, $T_{min}-T_{max}$	±0.05 max (±0.03 typ)	*	% FSR
Offset Voltage	±3 max (±1 typ)	*	mV
Offset Voltage, $T_{min}-T_{max}$	±20 max (±6 typ)	*	mV
Pedestal	±4 max (±2 typ)	*	mV
Pedestal, $T_{min}-T_{max}$	±20 max (±8 typ)	±20 max (±10 typ)	mV
Droop Rate	0.5 max (0.1 typ)	*	mV/ms
Droop Rate, $T_{min}-T_{max}$	60 max (20 typ)	650 max (200 typ)	mV/ms
DYNAMIC CHARACTERISTICS			
Full Power Bandwidth			
V_{OUT} = +10V, −3dB	1.4	*	MHz
Output Slew Rate	50	*	V/μs
Acquisition Time			
To ±0.01% 10V Step	2.0 max (1.0 typ)	*	μs
To ±0.01% 20V Step	2.5 max (1.6 typ)	*	μs
Aperture Delay	60 max (30 typ)	*	ns
Aperture Jitter	0.4	*	ns
Settling Time			
Sample Mode (10V Step)	2.0 max (1.0 typ)	*	μs
Sample to Hold	500	*	ns
Feedthrough (Hold Mode)			
at 1kHz	0.02 max (0.005 typ)	*	% FSR
Transient Peak Amplitude			
Sample/Hold/Sample	40	*	mV
ANALOG OUTPUT			
Output Voltage Swing[1]	±10.0 min	*	Volts
Output Current	3.0	*	mA
POWER REQUIREMENTS			
Operating Voltage Range	±12 to ±18	*	Volts
Supply Current			
+V	18 max (9 typ)	*	mA
−V	−10 max (−3 typ)	*	mA
Power Supply Rejection Ratio	100	*	μV/V
Power Consumption	500 max (200 typ)	*	mW

NOTES
[1]Maximum output swing is 4V less than $+V_S$.
*Specifications same as AD346JD.
Specifications subject to change without notice.

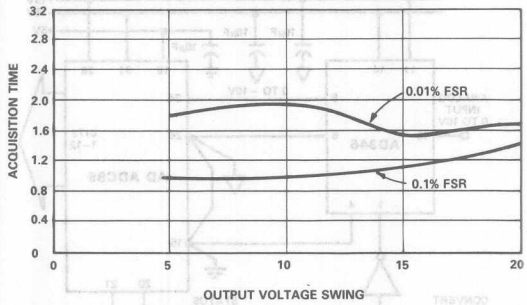


Figure 1. Acquisition Time vs. Output Voltage

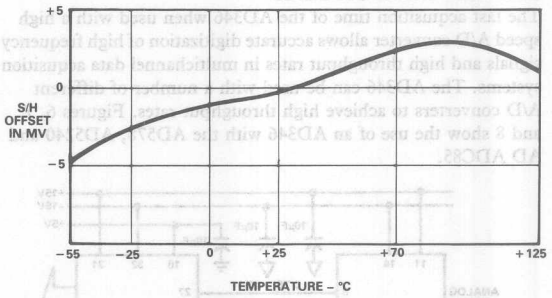


Figure 3. S/H Offset Drift (Typical)

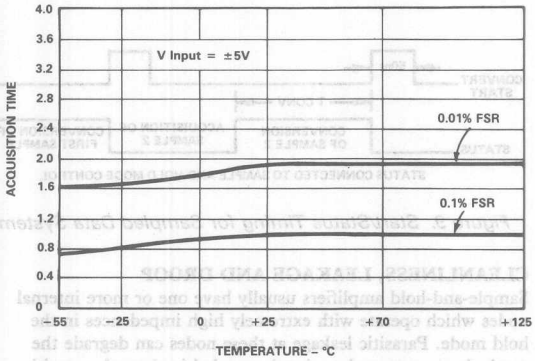
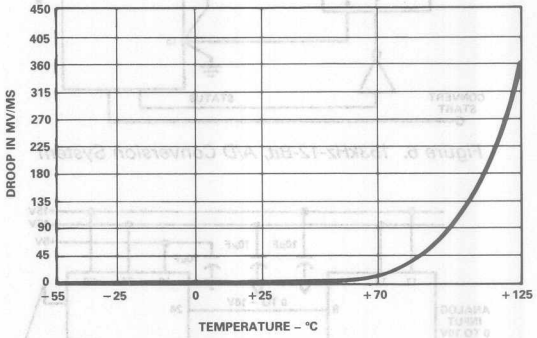


Figure 2. Acquisition Time vs. Temperature



Figue 4. Droop vs. Temperature (±5 Volts)

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pins of the AD346. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

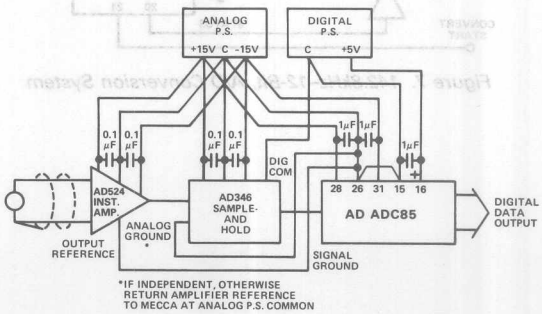


Figure 5. Basic Grounding Practice

speed A/D converter allows accurate digitization of high frequency signals and high throughput rates in multichannel data acqusition systems. The AD346 can be used with a number of different A/D converters to achieve high throughput rates. Figures 6, 7 and 8 show the use of an AD346 with the AD578, AD5240 and AD ADC85.

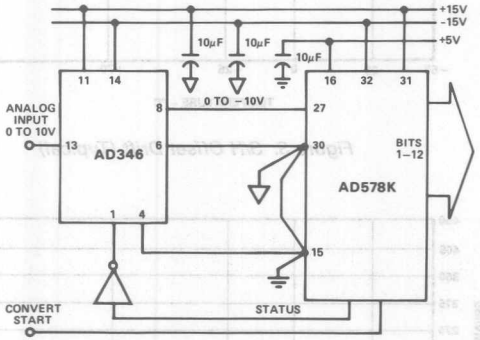


Figure 6. 153kHz-12-Bit, A/D Conversion System

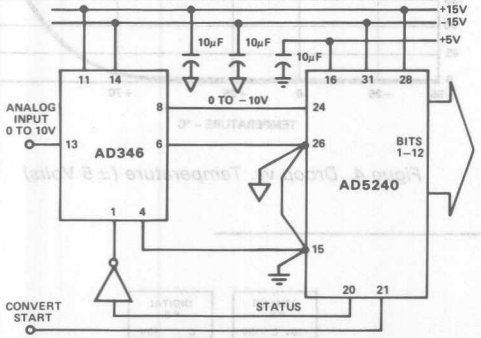


Figure 7. 142.8kHz–12-Bit, A/D Conversion System

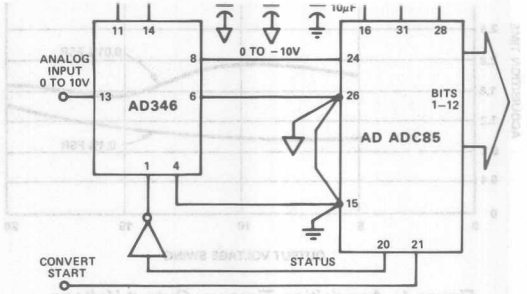


Figure 8. 83.3kHz–12-Bit, A/D Conversion System

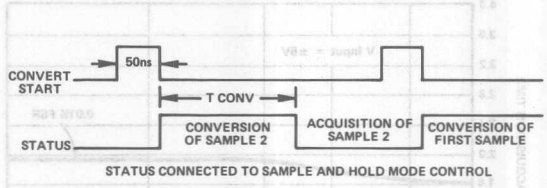


Figure 9. Start/Status Timing for Sampled Data System

CLEANLINESS, LEAKAGE AND DROOP

Sample-and-hold amplifiers usually have one or more internal nodes which operate with extremely high impedances in the hold mode. Parasitic leakage at these nodes can degrade the part's droop rate, and ac signals coupled in through parasitic capacitance can introduce noise onto the held output. One such dc leakage path can be produced by the residual oils left on the package after it has been handled with bare fingers. Most normal board cleaning and flux removal procedures will remove these contaminants. For best results finger cots should be used when handling the AD346.

Track-and-Hold Amplifier

AD386

FEATURES

Companion to True 16-Bit A/D Converters
16-Bit Linear (−40°C to +85°C)
14-Bit Linear (−55°C to +125°C)
Fast Acquisition Time: 3.6 μs to 0.00076%
Low Droop Rate: 20 μV/ms
Differential Amplifier for Ground Sense
Low Aperture Jitter: 40 ps

APPLICATIONS

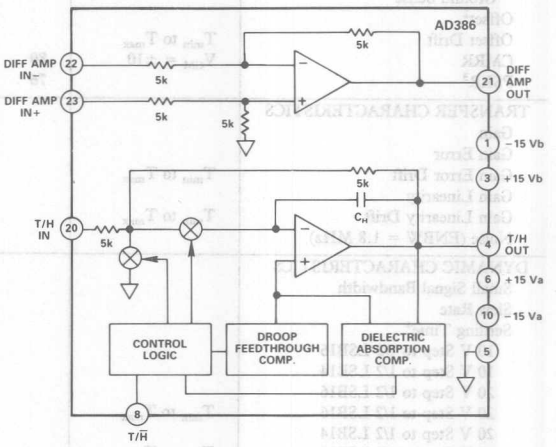
Medical and Analytical Instrumentation
Signal Processing
Multichannel Data Acquisition Systems
Automatic Test Equipment
Guidance and Control
Sonar

PRODUCT DESCRIPTION

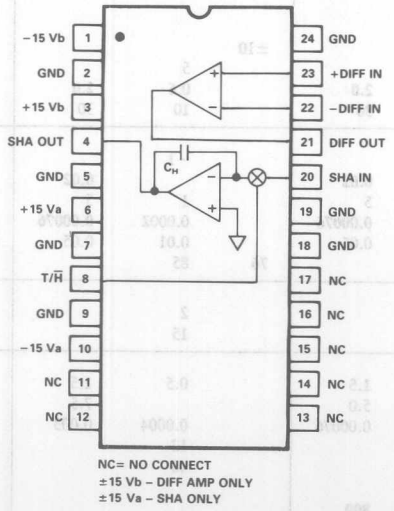
The AD386 is a high accuracy, adjustment free track-and-hold amplifier designed for high resolution data acquisition applications. The fast acquisition time (3.6 μs to 75 μV) and low aperture jitter (40 ps) make it ideal for use with fast A/D converters.

The AD386 is complete with an internal hold capacitor, and it incorporates a compensation network which minimizes the track-to-hold charge offset and dielectric absorption. The AD386 also includes an internal differential amplifier for very high accuracy applications.

FUNCTIONAL BLOCK DIAGRAM



Typical applications for the AD386 include sampled data system, peak hold function, strobe measurement system and simultaneous sampling converter systems. When used with autozero and autocalibration techniques, this T/H combined with a high linearity A/D will offer true 16-bit performance (0.00076% linearity) over the industrial temperature range, and 14-bit performance (0.003% linearity) over the military temperature range.



AD386 Pin Configuration

ORDERING GUIDE

Model	Max Linearity Error	Temperature Range	Package Option*
AD386BD	0.00076% FSR	−40°C to +85°C	DH-24B
AD386TD	0.003% FSR	−55°C to +125°C	DH-24B
AD386TD/883B	0.003% FSR	−55°C to +125°C	DH-24B

*DH-24B = Ceramic DIP. For outline information see Package Information section.

AD386—SPECIFICATIONS (@ +25°C unless otherwise noted, V_S = ±15 V ± 10%)

Model	Conditions	AD386BD Min	AD386BD Typ	AD386BD Max	AD386TD Min	AD386TD Typ	AD386TD Max	Units
DIFFERENTIAL AMPLIFIER								
INPUT CHARACTERISTICS								
Input Range		±10			±10			V
Common-Mode Range		±10			±10			V
Input Resistance[1]								
Signal			5			5		kΩ
Ground Sense			10			10		kΩ
Offset[2]			0.6	**2.0**		0.6	**2.0**	mV
Offset Drift	T_{min} to T_{max}		10	30		10	30	µV/°C
CMRR	V_{CM} = ±10	**80**	90		**80**	90		dB
PSRR[3]		**76**	85		**76**	85		dB
TRANSFER CHARACTERISTICS								
Gain			−1			−1		V/V
Gain Error				**0.02**			**0.02**	%
Gain Error Drift	T_{min} to T_{max}		1	5		1	5	ppm/°C
Gain Linearity			0.0002	**0.00076**		0.0002	**0.00076**	%
Gain Linearity Drift	T_{min} to T_{max}		0.01	0.05		0.01	0.05	ppm/°C
Noise (ENBW = 1.8 MHz)			32	45		32	45	µV rms
DYNAMIC CHARACTERISTICS								
Small Signal Bandwidth			6			6		MHz
Slew Rate			65			65		V/µs
Settling Time[4]								
10 V Step to 1/2 LSB16			2.0	3.0				µs
10 V Step to 1/2 LSB14			0.8	1.5		0.8	1.5	µs
20 V Step to 1/2 LSB16			2.0	**3.0**				µs
20 V Step to 1/2 LSB16	T_{min} to T_{max}		2.0	3.0				µs
20 V Step to 1/2 LSB14			0.8	**1.5**		0.8	**1.5**	µs
20 V Step to 1/2 LSB14	T_{min} to T_{max}		0.8	1.5		0.8	1.5	µs
OUTPUT								
Voltage	R_{LOAD}>3.5 kΩ, T_{min} to T_{max}	±10			±10			V
Current	Short Circuit		15			15		mA
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		±5		±18	±5		±18	V
Quiescent Current			4.2	**5.0**		4.2	**5.0**	mA
TRACK-AND-HOLD								
INPUT CHARACTERISTICS								
Input Range		±10			±10			V
Input Resistance[1]			5			5		kΩ
Offset[2]			0.6	**2.0**		0.6	**2.0**	mV
Offset Drift	T_{min} to T_{max}		10	30		10	30	µV/°C
TRANSFER CHARACTERISTICS								
Gain			−1			−1		V/V
Gain Error				**0.02**			**0.02**	%
Gain Error Drift	T_{min} to T_{max}		1	5		1	5	ppm/°C
Gain Linearity			0.0002	**0.00076**		0.0002	**0.00076**	%
Gain Linearity Drift	T_{min} to T_{max}		0.01	0.05		0.01	0.05	ppm/°C
PSRR[3]		**76**	85		**76**	85		dB
DYNAMIC CHARACTERISTICS								
Small Signal Bandwidth			2			2		MHz
Slew Rate			15			15		V/µs
TRACK-TO-HOLD SWITCHING								
Pedestal + Offset			0.5	**1.5**		0.5	**1.5**	mV
Pedestal + Offset	T_{min} to T_{max}			5.0			7.5	mV
Pedestal Linearity	T_{min} to T_{max}		0.0004	0.00076		0.0004	0.003	%
Aperture Delay			12			12		ns
Aperture Jitter			40			40		ps
Transient Settling[4]								
to 1/2 LSB16	T_{min} to T_{max}		600	**800**				ns
to 1/2 LSB14	T_{min} to T_{max}		400	**500**		400	**500**	ns

Model	Conditions	AD386BD Min	AD386BD Typ	AD386BD Max	AD386TD Min	AD386TD Typ	AD386TD Max	Units
HOLD MODE								
Droop Rate			20	**100**		20	**100**	mV/s
Droop Rate	T_{max}		0.2	1.0		3.6	18	V/s
Feedthrough[5]			−99	**−94**		−99	**−94**	dB
Noise (ENBW = 1.7 MHz)			32	50		32	50	μV rms
PSRR[3]		**60**	66		**60**	66		dB
Dielectric Absorption[6]			7	**10**		7	**10**	ppm
HOLD-TO-TRACK DYNAMICS								
Acquisition Time[4]								
10 V Step to 1/2 LSB16			3.6	4.1				μs
10 V Step to 1/2 LSB14			3.1	3.6		3.1	3.6	μs
20 V Step to 1/2 LSB16			3.6	**4.1**				μs
20 V Step to 1/2 LSB16	T_{min} to T_{max}		4.0	4.5				μs
20 V Step to 1/2 LSB14			3.1	**3.6**		3.1	**3.6**	μs
20 V Step to 1/2 LSB14	T_{min} to T_{max}		3.5	4.0		4.0	4.5	μs
DIGITAL INPUTS								
V_{IH}	T_{min} to T_{max}	**3.5**			**3.5**			V
V_{IL}	T_{min} to T_{max}			**0.9**			**0.9**	V
I_{IH}	T_{min} to T_{max}	**−10**		**+10**	**−10**		**+10**	μA
I_{IL}	T_{min} to T_{max}	**−10**		**+10**	**−10**		**+10**	μA
OUTPUT								
Voltage	R_{LOAD}>3.5 kΩ, T_{min} to T_{max}	±10			±10			V
Current	Short Circuit		15			15		mA
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		±8		±18	±8		±18	V
Quiescent Current								
Positive Supply			8.0	**12.0**		8.0	**12.0**	mA
Negative Supply		**−6.0**	−5.4		**−6.0**	−5.4		mA
SYSTEM								
Gain Linearity	T_{min} to T_{max}		0.0003	0.0012		0.0003	0.0012	%
Acquisition Time[4, 7]								
20 V Step to 1/2 LSB16			4.1	5.1				μs
20 V Step to 1/2 LSB16	T_{min} to T_{max}		4.5	5.4				μs
20 V Step to 1/2 LSB14			3.2	3.9		3.2	3.9	μs
20 V Step to 1/2 LSB14	T_{min} to T_{max}		3.6	4.3		4.1	4.8	μs
Power Dissipation			312	435		312	435	mW
TEMPERATURE RANGE								
Operating		−40		+85	−55		+125	°C
Storage		−60		+150	−60		+150	°C

NOTES
[1]Typical resistance tolerance is ±25%.
[2]After 5 minute warmup at +25°C.
[3]Test conditions: $+V_S$ = +15 V, $-V_S$ = −16 V to −14 V and $+V_S$ = +14 V to +16 V, $-V_S$ = −15 V.
[4]R_{LOAD} = 5 kΩ, C_{LOAD} = 10 pF, settling measured to 1/2 LSB at output.
[5]Measured at 1 kHz.
[6]Dielectric Absorption represents the magnitude of long-term settling artifacts for hold times up to 80 μs as a fraction of the difference in voltages between two successive held samples.
[7]Specifications also apply for 10 V step.

Specifications subject to change without notice.
Specifications in **bold** are 100% production tested.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation . . . . . .800 mW
Input Voltage[2] . . . . . ±18 V
T/$\overline{H}$ Input Voltage . . . . . −0.5 V, +16 V
Output Short Circuit Duration . . . . . .Indefinite
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range
AD386B . . . . . −40°C to +85°C
AD386T . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

AD386—Typical Performance Characteristics

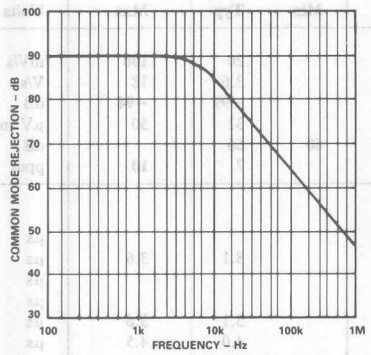


Figure 1. Differential Amplifier Common Mode Rejection vs. Frequency

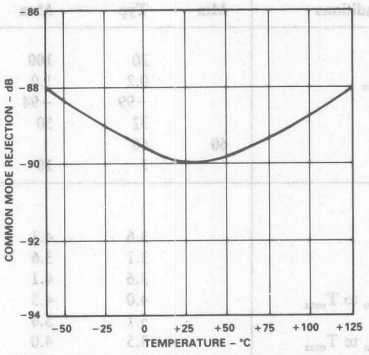


Figure 2. Differential Amplifier Common Mode Rejection vs. Temperature (100 Hz)

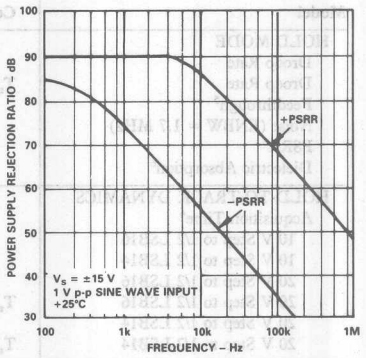


Figure 3. Differential Amplifier Power Supply Rejection vs. Frequency

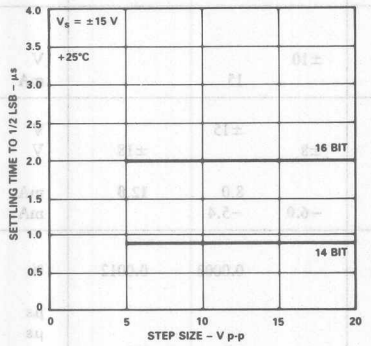


Figure 4. Differential Amplifier Settling Time vs. Step Size

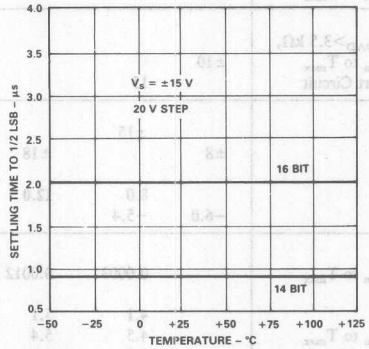


Figure 5. Differential Amplifier Settling Time vs. Temperature

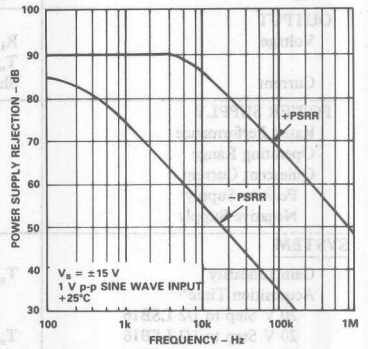


Figure 6. T/H Power Supply Rejection vs. Frequency, Track Mode

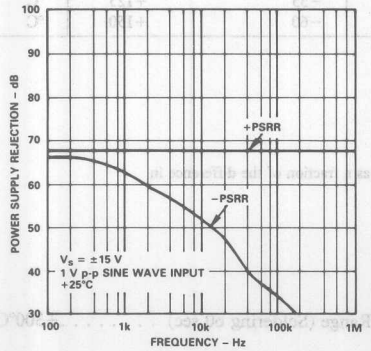


Figure 7. T/H Power Supply Rejection vs. Frequency, Hold Mode

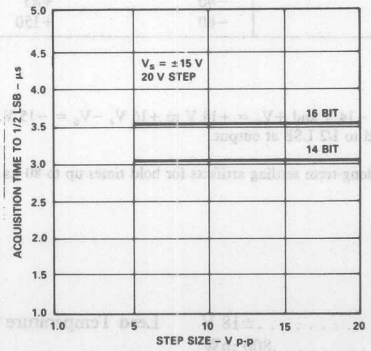


Figure 8. T/H Acquisition Time vs. Step Size

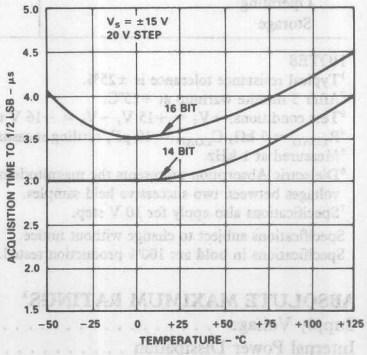


Figure 9. T/H Acquisition Time vs. Temperature

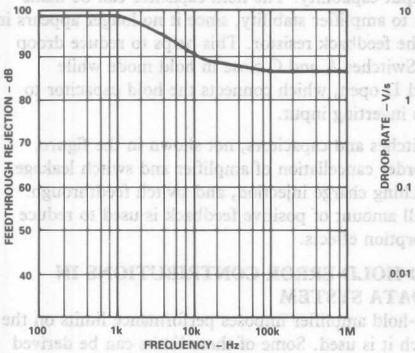


Figure 10. Feedthrough vs. Frequency

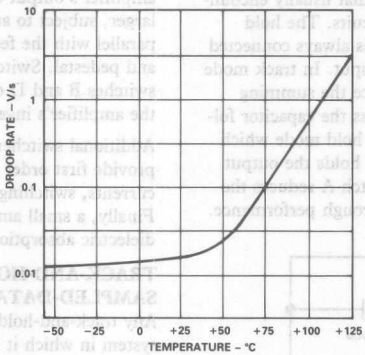


Figure 11. Droop Rate vs. Temperature

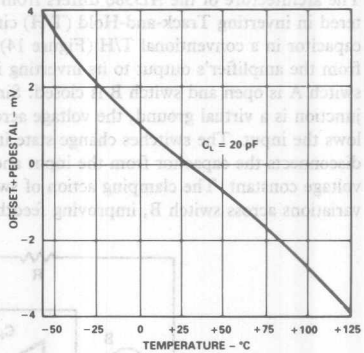


Figure 12. (Pedestal + Offset) vs. Temperature

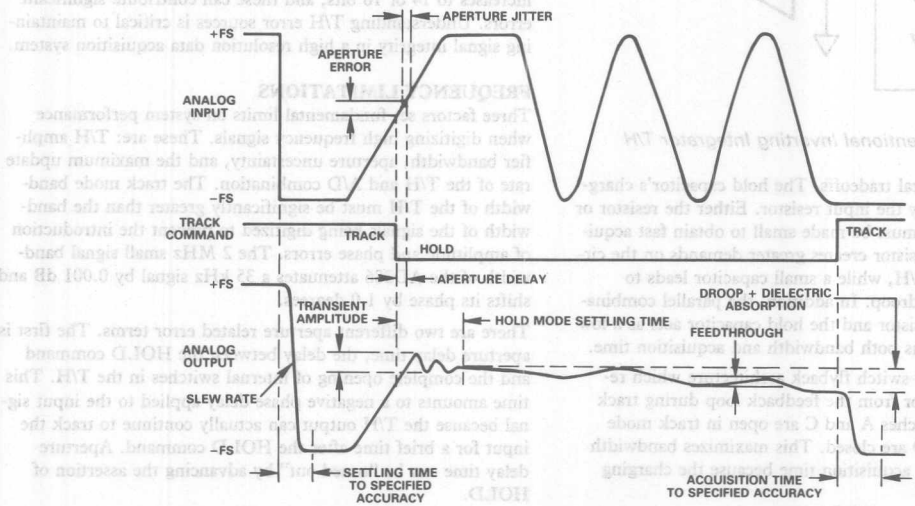


Figure 13. T/H Characteristic Features

TERMINOLOGY

Aperture Delay: the time required by the internal switch(es) to disconnect the hold capacitor from the input, which produces an effective delay in the sample timing.

Aperture Jitter: the uncertainty in Aperture Delay caused by internal noise and the variation of switching thresholds with signal level. The error caused by aperture jitter depends on the rate of change of the input and as such determines the maximum input frequency which can be sampled without error.

Pedestal: a step change in the output voltage which occurs when switching from track mode to hold mode.

Hold Mode Settling Time: the time required for the pedestal to reach its final value to within a specified fraction of full scale.

Droop: the change in the held output voltage resulting from leakage currents.

Feedthrough: the fraction of input signal variation which appears at the output in hold mode as a result of capacitive coupling.

Dielectric Absorption: the tendency of charges within a capacitor to redistribute themselves over time, resulting in "creep" in the voltage of an open circuit capacitor after a large rapid change.

Acquisition Time: the time required after entering track mode for the voltage on the hold capacitor to settle to within a specified fraction of full scale. This is usually specified for a full-scale step change in output voltage.

Settling Time: the time required in track mode for the output to reach its final value within a specified fraction of full scale following a step change in the input voltage.

Nonlinearity: the degree to which a plot of output versus input deviates from the straight line defined by the end points. It is usually specified as a percentage of full scale.

THEORY OF OPERATION

The architecture of the AD386 differs from that usually encountered in inverting Track-and-Hold (T/H) circuits. The hold capacitor in a conventional T/H (Figure 14) is always connected from the amplifier's output to its inverting input. In track mode switch A is open and switch B is closed. Since the summing junction is a virtual ground, the voltage across the capacitor follows the input. The switches change state in hold mode which disconnects the capacitor from the input and holds the output voltage constant. The clamping action of switch A reduces the variations across switch B, improving feedthrough performance.

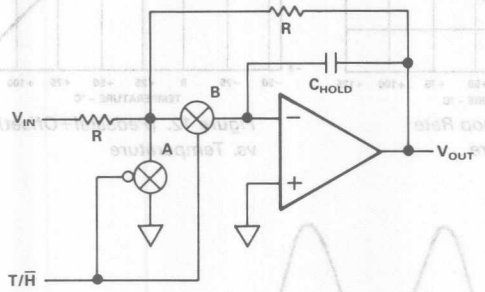


Figure 14. Conventional Inverting Integrator T/H

This circuit forces several tradeoffs. The hold capacitor's charging current is limited by the input resistor. Either the resistor or the capacitor, or both, must be made small to obtain fast acquisition times. A small resistor creates greater demands on the circuit which drives the T/H, while a small capacitor leads to increased pedestal and droop. In addition, the parallel combination of the feedback resistor and the hold capacitor acts as a low pass filter and constrains both bandwidth and acquisition time.

The AD386 uses a four-switch flyback architecture which removes the hold capacitor from the feedback loop during track mode (Figure 15). Switches A and C are open in track mode while switches B and D are closed. This maximizes bandwidth and provides minimum acquisition time because the charging current delivered to the hold capacitor is limited only by the amplifier's output capability. The hold capacitor can be made larger, subject to amplifier stability, since it no longer appears in parallel with the feedback resistor. This helps to reduce droop and pedestal. Switches A and C close in hold mode while switches B and D open, which connects the hold capacitor to the amplifier's inverting input.

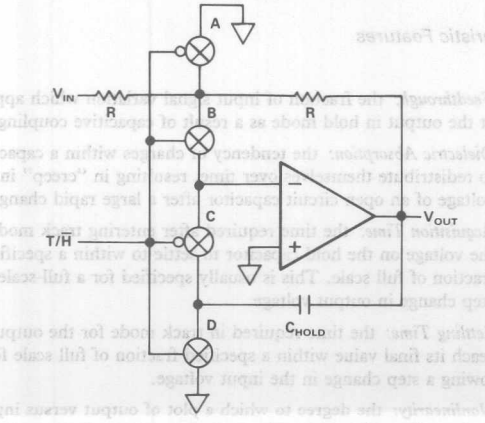


Figure 15. Four-Switch Inverting Flyback T/H

Additional switches and capacitors, not shown in the figure, provide first order cancellation of amplifier and switch leakage currents, switching charge injection, and switch feedthrough. Finally, a small amount of positive feedback is used to reduce dielectric absorption effects.

TRACK-AND-HOLD ERROR CONTRIBUTIONS IN SAMPLED-DATA SYSTEM

Any track-and-hold amplifier imposes performance limits on the system in which it is used. Some of these limits can be derived from the theory of sampled-data systems, some are intrinsic to the T/H, and some depend on details of the system design. Many subtle effects come into play as system resolution increases to 14 or 16 bits, and these can contribute significant errors. Understanding T/H error sources is critical to maintaining signal integrity in a high resolution data acquisition system.

FREQUENCY LIMITATIONS

Three factors set fundamental limits on system performance when digitizing high frequency signals. These are: T/H amplifier bandwidth, aperture uncertainty, and the maximum update rate of the T/H and A/D combination. The track mode bandwidth of the T/H must be significantly greater than the bandwidth of the signals being digitized to prevent the introduction of amplitude and phase errors. The 2 MHz small signal bandwidth of the AD386 attenuates a 35 kHz signal by 0.001 dB and shifts its phase by 1.0 degrees.

There are two different aperture related error terms. The first is aperture delay time, the delay between the HOLD command and the complete opening of internal switches in the T/H. This time amounts to a negative phase delay applied to the input signal because the T/H output can actually continue to track the input for a brief time after the HOLD command. Aperture delay time can be "tuned out" by advancing the assertion of HOLD.

Aperture jitter, the random variations in aperture delay time, causes errors which are directly related to the rate of change of the input signal and which cannot be eliminated by circuit adjustments.

A simple calculation provides the frequency at which aperture jitter produces an error of 1/2 LSB when the input is a full-scale sinusoid. The general result for an N-bit A/D converter is

$$F_{max} = \frac{V_{FS}}{V_{PP}} \times \frac{1}{2^{N+1} \times \pi \times Aperture\ Jitter}$$

where V_{FS} is the A/D converter's input range and V_{PP} is the peak-to-peak value of the input sinusoid. The worst case (minimum) value of F_{max} occurs when V_{PP} is equal to V_{FS}. If the T/H has an aperture jitter of 100 ps and is used with a 16-bit linear A/D, the maximum input frequency is 24.3 kHz.

The same T/H, when used with a 14-bit linear A/D, permits the processing of signals up to 97.1 kHz before aperture jitter-errors become observable. Figure 16 shows these errors as a function of frequency, assuming a full scale input sinusoid, for several values of aperture jitter.

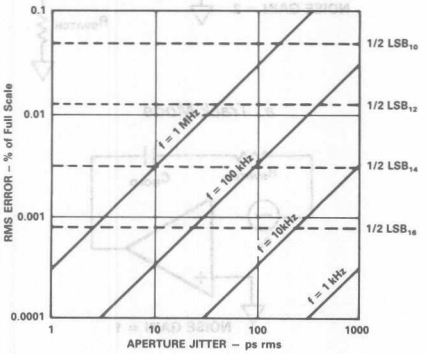


Figure 16. T/H Error vs. Aperture Jitter and Input Frequency

Aperture jitter is often expressed as an rms number. "Peak-to-peak" aperture jitter is usually defined as 6 times this rms value. This comes from probability theory, where 99.7% of the measurements of a random variable will be within 3 standard deviations of the variable's average value. Aperture jitter arises from broadband electrical noise, which is very nearly an ideal random process with a standard deviation equal to its rms value, so multiplication by 6 gives a good approximation to the noise's peak-to-peak value.

A second limit on the input frequency is imposed by the finite time required for signal acquisition and conversion. It is possible to reconstruct any uniformly sampled signal without loss of information provided the sampling rate is at least twice the bandwidth of the input signal; this is the Nyquist criterion, a fundamental result in sampling theory. This limits input frequency to

$$F_{max} = \frac{1}{2 \times (t_{ACQ} + t_{CONV} + t_{AP})}$$

where t_{ACQ} is the T/H acquisition time, T_{CONV} is the time required for the A/D conversion, and T_{AP} is the aperture delay of the T/H. The last term is usually very small and can be ignored. A system composed of a 3.6 μs T/H and a 10 μs A/D can be used successfully to digitize signals with frequency components up to 36.76 kHz. This limit is independent of input signal amplitude. Throughput rates and input frequency ranges for the AD386 in combination with various A/D converters are shown in Table I.

A/D	Conversion Time	Minimum Throughput
ADADC71	50 μs max	18.7 kHz
AD1376/78	17 μs max	48.8 kHz
AD1377	10 μs max	73.5 kHz

Table I. Throughput for AD386 with Various A/D Converters

NONLINEARITIES

Two phenomena directly affect the fidelity of a T/H's transfer function and can degrade system linearity. One of these error sources is track mode nonlinearity. It arises primarily from gain nonlinearity in the T/H's internal amplifier(s). Mismatches in the temperature coefficients of internal resistors may also contribute, but usually do so only for very low frequency signals. The AD386's track mode nonlinearity is about 1/6 16-bit LSB (Figure 17), as is the nonlinearity of the AD386's differential amplifier.

System linearity will also be reduced if the pedestal varies nonlinearly with signal level. Pedestal nonlinearity in the AD386 is below 8 microvolts per volt of input signal, or about 1/2 16-bit LSB.

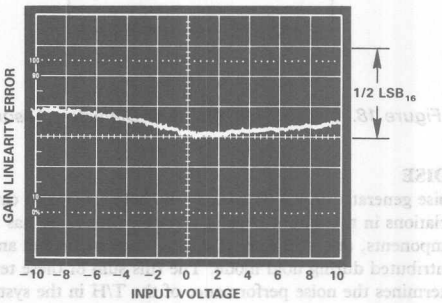


Figure 17. AD386 Track Mode Nonlinearity

FEEDTHROUGH, DROOP, AND DIELECTRIC ABSORPTION

Errors resulting from signal feedthrough and droop must be less than 1/2 LSB in order for the system's linearity to be maintained. The AD386 uses a symmetrical, compensated architecture to minimize both these effects. Feedthrough varies slightly with input frequency from −100 dB below 1 kHz to −86 dB above 100 kHz (Figure 10). This provides 16-bit accuracy for full-scale inputs up to at least 5 kHz and 14-bit performance to beyond 100 kHz.

The circuit's symmetry causes the droop rate to depend on differences in leakage currents between identical junctions under nearly identical bias conditions. The resulting droop is less than 1/2 16-bit LSB (10 V scale) at temperatures up to 85°C and 1/2 14-bit LSB (10 V scale) over the full military temperature range for hold times up to 100 μs.

Capacitors exhibit a memory phenomenon, dielectric absorption (DA), in fast charge, long hold applications. This arises from nonideal behavior of the dielectric material which allows charge storage in the bulk of the dielectric. This bulk charge cannot be removed rapidly because of the long time constant associated with the dielectric's high resistance. A capacitor with dielectric absorption can be modeled as an ideal capacitor in parallel with a series R-C circuit as shown in Figure 18. When such a capacitor is used as the hold capacitor in a T/H the held voltage will tend to creep back towards the voltage held for the previous conversion cycle. The degree and time constant of this behavior depends on the capacitor's dielectric material, as well as on the charge and hold time of the circuit.

4

This causes an apparently nonlinear pedestal because the difference between the currently measured voltage and the previously measured voltage determines the magnitude of the DA error. The AD386 uses a high quality hold capacitor with low intrinsic DA. Residual DA errors are further reduced by laser trimming a compensation network during the manufacturing process. The trimming is performed under typical system timing conditions of 5 μs track, 45 μs hold. The post-trim dielectric absorption error is less than 1/2 16-bit LSB for full-scale changes between samples and hold times between 10 μs and 100 μs.

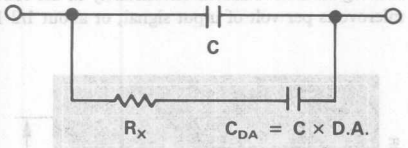


Figure 18. Capacitor Model with Dielectric Absorption

NOISE

Noise generated in a T/H adds to the held signal and causes variations in the output code of an A/D. This noise has two components, one which arises during track mode and another contributed during hold mode. The rms sum of these terms determines the noise performance of the T/H in the system.

Track noise is the noise which gets sampled when entering hold mode. An inverting T/H architecture such as that used in the AD386 has a noise gain of 2. This noise is low pass filtered in the R-C network comprised of the hold capacitor and the switch on resistance (see Figure 19a). The rms value of the track noise is

$$\langle e_{nT} \rangle = (op\ amp\ noise) \times (noise\ gain) \times (ENBW)^{1/2}$$

Op amp noise is the rms sum of the amplifier's broadband voltage noise and the thermal noise contributions of the input and feedback resistors, about 17 nV/$\sqrt{\text{Hz}}$. Other noise sources, including amplifier current noise and switch thermal noise, are negligible. ENBW, the equivalent noise bandwidth, is

$$ENBW = \frac{\pi}{2} \times \frac{BW1 \times BW2}{BW1 + BW2}$$

where BW1 is the small signal bandwidth of the T/H in track mode (2 MHz for the AD386) and BW2 is the corner frequency of the R_{SWITCH}–C_{HOLD} combination (2.7 MHz). The resulting track noise in the AD386 is at most 46 μV rms.

Noise gain is reduced to 1 in hold mode, and input and feedback resistor thermal noise makes no contribution (Figure 19b). The equivalent noise bandwidth now depends on the T/H's small signal bandwidth and the characteristics of the A/D converter used in the system. This is because the signal at the input

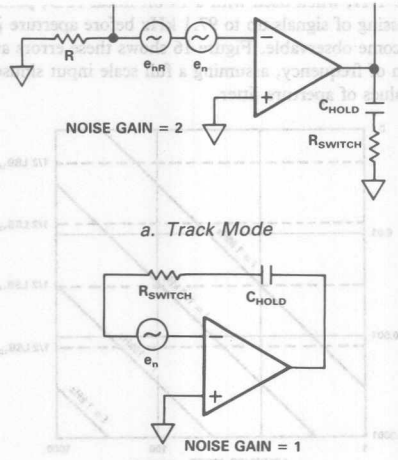


Figure 19. Dominant AD386 Noise Sources

of the comparator in a successive approximation A/D converter is filtered by the converter's input resistance and the summing junction capacitance. ENBW is calculated as before, but now BW1 is the T/H's small signal bandwidth in hold mode (4 MHz for the AD386), and BW2 is the bandwidth of the A/D's input R-C. BW2 is about 700 kHz in the AD ADC71 and AD1376 and roughly 1.7 MHz in the AD1377 and AD1378 (assuming a 10 V span). The respective values of ENBW are 940 kHz and 1.9 MHz. The hold noise contribution of the AD386 is about 16 μV rms when used with the AD ADC71 or AD1376 and 22 μV rms when used with the AD1377 or AD1378; this noise is 30% less for a 20 V span and 40% greater for a 5 V span because changes in the A/D's input resistance cause changes in BW2.

The total noise is the rms sum of these two results:

$$\langle e_n \rangle = [\langle e_{nT}^2 \rangle + \langle e_{nH}^2 \rangle]^{1/2}$$

This yields 49 μV rms and 51 μV rms for the two cases. Track noise dominates in both instances.

When the AD386's differential amplifier is used, its noise contribution will be band limited and sampled by the T/H. The equivalent bandwidth for this noise is also 1.8 MHz and the contribution to the track noise is 46 μV rms. The total track noise is the rms sum of 46 μV and 46 μV, or 65 μV rms, and the overall noise for the complete AD386 used with any of the above A/D converters is at most 70 μV rms.

The rms value represents one standard deviation if the noise has a Gaussian distribution, which is usually the case for wideband electrical noise. If a constant noise-free voltage is sampled a large number of times, the held result will be within one standard deviation of the ideal value 32% of the time, within two standard deviations 95% of the time, and within three standard deviations 99.7% of the time. The entries in Table II were calculated using three standard deviations as the definition of the peak-to-peak noise.

Span	No. Bits	rms Noise LSBs	p-p Noise LSBs
10 V	14	0.11	0.66
20 V	14	0.06	0.36
10 V	16	0.45	2.7
20 V	16	0.23	1.4

Table II. AD386 Noise Contribution as a Function of A/D Span and Resolution

POWER SUPPLY REJECTION

Variations on the power supply lines, both dc and ac, can lead to unwanted changes in the voltage acquired by a T/H. Power supply variations in track mode cause the output voltage, and hence the voltage across the hold capacitor, to vary. PSRR decreases with increasing frequency, making well regulated, low noise linear power supplies and proper bypassing essential in a high resolution data acquisition system.

Equally important, but usually forgotten or omitted, is hold PSRR. This is frequently much worse than track PSRR because parasitic capacitances which are not significant in track mode couple into the extremely high impedance nodes which exist in a T/H during hold mode. This specification is essential to the system designer, as hold mode PSRR often determines the performance required from the system's power supplies. The power supply rejection of the AD386 is specified and characterized in both track and hold modes.

Pedestal arises from the transfer of charge from the internal switching circuitry to the hold capacitor during the transition from track mode to hold mode. Pedestal in some T/H circuits is extremely sensitive to changes in the high and low levels of the external control signal. The AD386 uses an internal +5 V supply and logic buffers to prevent this behavior.

GROUNDING

All voltage measurements in a data acquisition system are eventually referenced to ground. Variations in the "ground" potential through the system resulting from resistive drops of power supply and signal return currents as well as from interference from external sources may add to the signal being digitized and produce false results. The grounding scheme in a high resolution system cannot be left to chance and must be planned as carefully as any other aspect of the system's design. Proper grounding and the reduction of externally induced ground noise are discussed at length in the following Applications section.

Applications

GROUNDING. DECOUPLING, AND LAYOUT CONSIDERATIONS

Many data acquisition systems have two or more ground pins which are not connected together within the device(s). These "grounds" may be referred to as Logic Power Return, Digital Return, Analog Ground, Analog Power Return, Signal Ground, etc., and they must be connected together somewhere within the system to establish a measurement reference point. Good grounding practice dictates that these grounds be tied at a single point, sometimes called a star or "Mecca" ground. In high resolution systems the star point is often located at the A/D, with a single, short, low impedance trace leading from there to the analog supply "common" terminal. The ideal is to use a solid analog ground plane beneath the T/H and A/D as the star point.

Because circuit traces have resistance and inductance, currents in the various ground runs can create voltage differences of hundreds of millivolts between "'ground" in different parts of the system. Power supply and signal ground traces should be separate to prevent summing power supply return currents with analog signal currents, which would lead to measurement errors. It is also important to avoid closed circuit loops in system ground connections. A loop can act as a very effective antenna, coupling voltages created by stray magnetic fields into the measurement system.

Each of the AD386's power supply terminals should be capacitively bypassed to the ground plane as closely as possible to the device. This is best done using 0.01 μF to 0.1 μF ceramic capacitors. High frequency supply noise rejection may be further improved by placing small (4.7 Ω to 10 Ω) carbon composition resistors in series with the supply leads. These resistors, in combination with the ceramic capacitors, act as local low pass filters and prevent crosstalk between system components. The bypassing scheme should also include solid Tantalum capacitors of 1 μF to 10 μF from each supply to ground in the critical areas of the board. Proper grounding and bypassing techniques are shown in Figure 20.

All AD386 ground pins (Pins 2, 5, 7, 9, 18, 19, and 24) should be connected to the analog ground plane.

WARNING: Improper bypassing can result in poor settling performance or high frequency oscillations.

The metal cover of the AD386 is internally grounded to provide additional shielding. Do not make any external connection to the cover.

DIFFERENTIAL AMPLIFIER

Many high resolution applications require the ability to sense ground at the signal source. This is especially true in systems with physical or thermal constraints that make it necessary to locate the T/H and A/D at some distance from the transducer. Under these conditions stray electromagnetic fields may cause "ground" at the signal source to be at a different potential from "ground" at the A/D despite the designer's best efforts. This will give rise to measurement errors because the potential difference will appear to be added to the true signal. The AD386's differential amplifier may be used to eliminate this type of ground noise as shown in Figure 21.

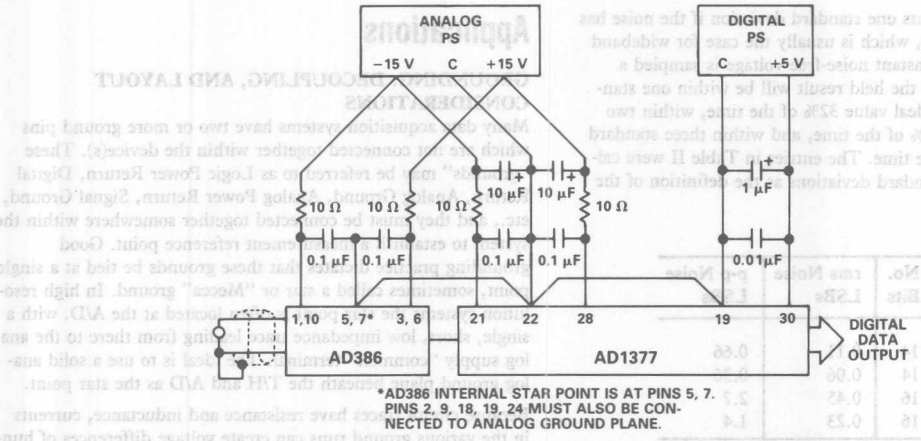
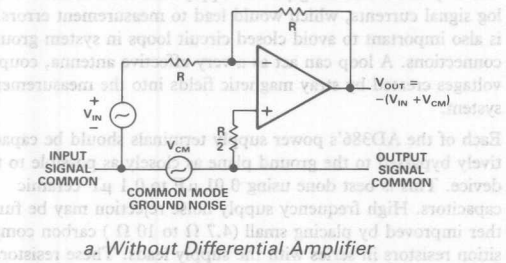
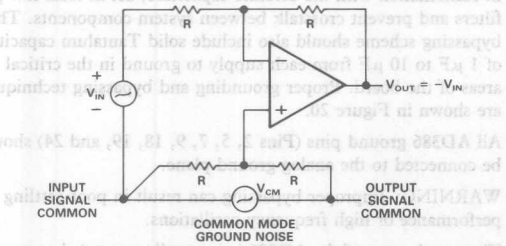


Figure 20. Proper Grounding and Supply Bypassing Techniques for a High Resolution Data Acquisition System



a. Without Differential Amplifier



b. With Differential Amplifier

Figure 21. Effects of Common Mode Noise

In extremely noisy environments it may be necessary to connect the differential amplifier to the signal source with shielded twisted pair cable. The shield should be connected to ground at the transducer and should be left floating at the AD386. This shielding technique is shown in Figure 22. The cable presents a capacitive load, and the signal source must be capable of driving this load without ringing or oscillations. The differential amplifier's noninverting input should be connected to Pin 24 if ground sensing is not required.

Another use of the differential amplifier is to restore signal polarity. Like most high resolution T/H amplifiers, the T/H in the AD386 operates in the inverting mode. The differential amplifier may be used to provide a second inversion so that the T/H output has the same polarity as the sensor output.

The differential amplifier also provides a low dynamic source impedance to the T/H section. This absorbs transients produced when the T/H switches from hold mode to track mode, providing optimal settling performance.

The T/H and differential amplifier have independent power supply connections. This permits a reduction in system power dissipation when the differential amplifier function is not needed.

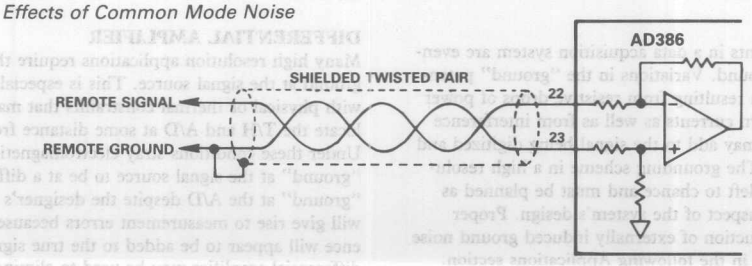


Figure 22. Remote Ground Sensing in a Noisy Environment

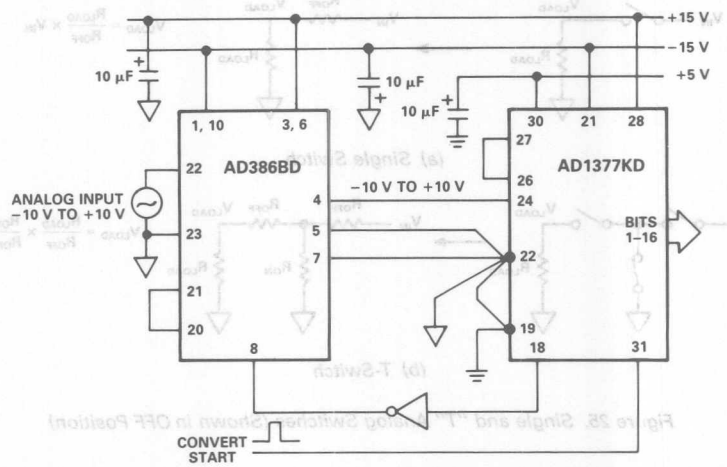


Figure 23. Basic Data Acquisition System (Some Supply Bypassing Omitted for Clarity)

GAIN AND OFFSET ADJUSTMENT

The usual practice in the design of data acquisition systems is to incorporate a single system level trim for offsets and a second for gain errors, rather than to trim each element in the signal processing chain. Traditionally these trims involve potentiometers or fixed resistors. The trims should be designed so that nulling static errors does not introduce new errors such as noise, increased thermal drift, or nonlinearity.

The offset, drift, and gain errors of the AD386 are laser trimmed during manufacture and no external adjustment capabilities are provided. This prevents the introduction of noise through offset adjust terminals and preserves the excellent gain linearity and drift performance. Most A/Ds provide for nulling gain and offset errors with a range sufficient to include the contributions of the AD386. Of course, it is also possible to include calibration routines in the system's software to eliminate mechanical adjustments.

HIGH RESOLUTION DATA ACQUISITION SYSTEM

The essential details of a high resolution data acquisition system using the AD386 are shown in Figure 23. Conversion is initiated by the falling edge of the CONVERT START pulse. This edge drives the A/D's STATUS line high. The inverter then drives the AD386 into hold mode. STATUS remains high throughout the conversion and returns low once the conversion is completed. This allows the AD386 to reenter track mode. The throughputs given in Table I were calculated based upon this circuit configuration.

One drawback of this connection becomes apparent if the system's grounding is marginal. The falling edge of CONVERT-START resets the successive approximation register within the A/D, causing transient currents in both the analog and digital return paths. These transients vary depending on the input signal and the prior conversion result. The same edge also drives the T/H into hold mode. The exact timing relationship of these two events depends upon differences in propagation delays. The T/H's held value may be affected if the A/D reset transient begins before the T/H has fully entered hold mode. The end result is system nonlinearity.

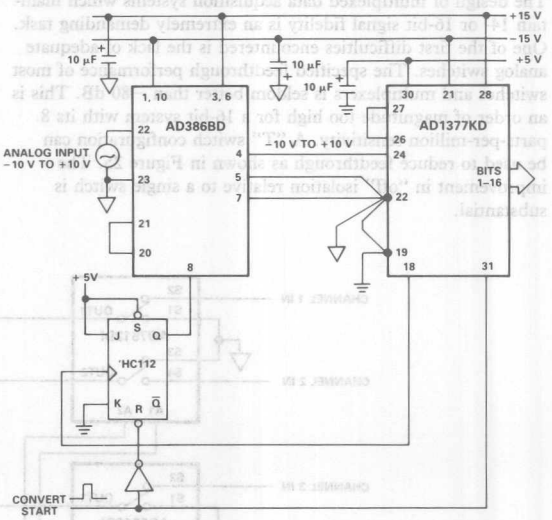


Figure 24. Improved Data Acquisition System (Some Supply Bypassing Omitted for Clarity)

This problem can be avoided with the addition of a flip flop as shown in Figure 24. The rising edge of CONVERT START places the T/H into hold mode before the A/D reset transients begin. The falling edge of STATUS places the AD386 back into track mode. System throughput will be reduced if a long CONVERT START pulse is used. Throughput can be calculated from

$$Throughput = \frac{1}{T_{ACQ} + T_{CONV} + T_{CS}}$$

where T_{ACQ} is the T/H acquisition time, T_{CONV} is the time required for the A/D conversion, and T_{CS} is the duration of CONVERT START. No significant T/H droop error will be introduced provided the width of CONVERT START is small compared with the A/D's conversion time.

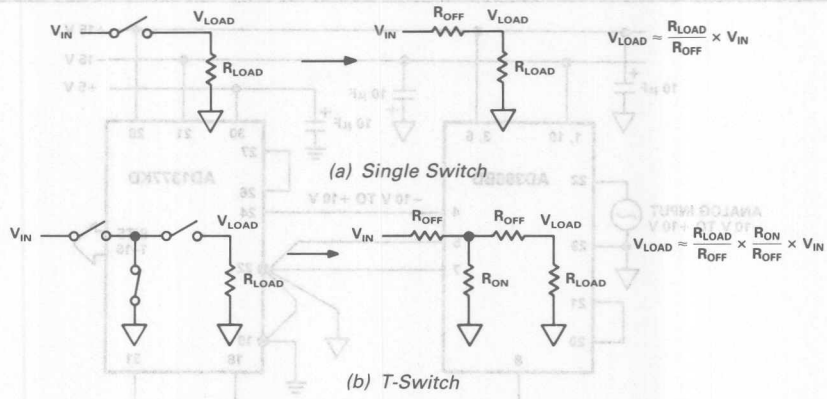


Figure 25. Single and "T" Analog Switches (Shown in OFF Position)

MULTICHANNEL SYSTEMS

The design of multiplexed data acquisition systems which maintain 14- or 16-bit signal fidelity is an extremely demanding task. One of the first difficulties encountered is the lack of adequate analog switches. The specified feedthrough performance of most switches and multiplexers is seldom better than −80 dB. This is an order of magnitude too high for a 16-bit system with its 8 parts-per-million sensitivity. A "T" switch configuration can be used to reduce feedthrough as shown in Figure 25. The improvement in "off" isolation relative to a single switch is substantial.

A few monolithic video T-switch ICs are now available and provide the necessary isolation in the dc-50 kHz frequency range. Unfortunately, these devices have voltage limitations which restrict their utility. It will usually be necessary to design a multiplexer using analog multiplexer and switch ICs. Figure 26 shows a simple 4-channel single-ended T-switch multiplexer and includes a high performance buffer (see below).

The on-resistance of analog switches and multiplexers is a nonlinear function of signal voltage. This will produce severe nonlinearity in a system in which a multiplexer supplies signals

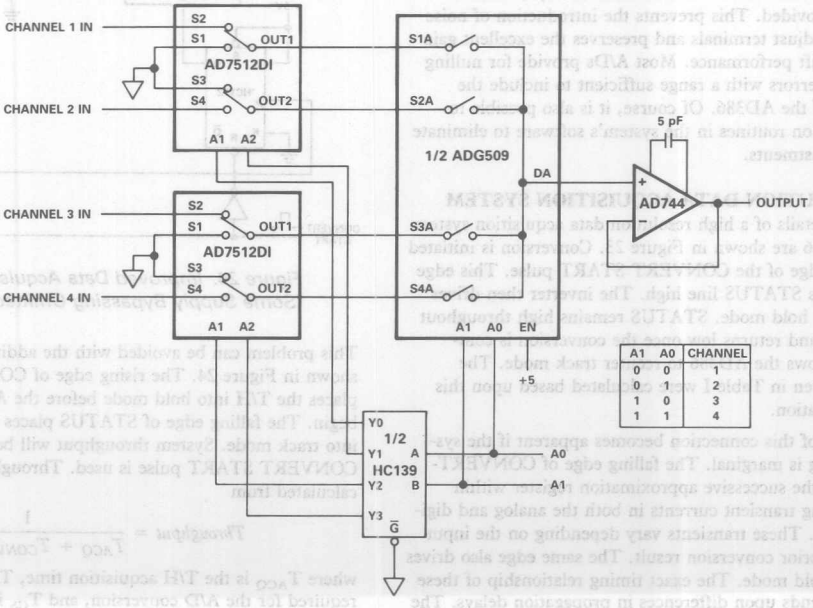


Figure 26. Four-Channel T-Switch Multiplexer (Power Supply Connections Not Shown)

directly to an AD386. A high-impedance buffer between the multiplexer and the T/H's input can solve this problem but may introduce several others.

An op amp in the noninverting gain-of-1 configuration is the obvious candidate for a buffer. The amplifier must settle quickly to maximize system throughput and must be extremely linear to maintain system performance. The linearity of this configuration depends upon the linearity of both the amplifier's open loop gain and common-mode rejection (linear errors in these parameters result only in system gain error, but nonlinear gain and CMRR produce system nonlinearity). Neither of these parameters is specified by most amplifier manufacturers.

A buffer may also increase system noise. Applications which require ground- sensing will require two buffers, resulting in 40% more noise than a one-buffer system.

Finally, a buffer will add its own offset to the signal being measured. Software calibration of the error and its drift is possible using a permanently grounded multiplexer channel.

The AD744 is a nearly ideal buffer for multiplexed systems. This amplifier provides offsets as low as 250 μV and an offset drift of 3 μV/°C while maintaining 16-bit linearity over the −40°C to +85°C temperature range. Typical settling times at room temperature are 2.3 μs (14 bits) and 3.5 μs (16 bits) for the AD744 combined with the AD386's differential amplifier. The increase in noise at the differential amplifier's output will be about 6 μV rms in a one-buffer system and roughly 12 μV rms in a two buffer system (recall that a 16-bit LSB in a 20 volt system is 305 μV). The AD744 is not unity-gain stable, and compensation is required. A 5 pF compensating capacitor is sufficient to ensure stability. The settling times listed above were measured using a 9 pF compensation capacitor which provides greater stability with moderate capacitive loads.

The NE5534 can also be used as a buffer to deliver 16-bit linearity. This amplifier also requires slight compensation to achieve unity-gain stability; 10 pF is sufficient. Settling is somewhat slower than the AD744, about 5 μs to 14 bits and 6 μs to 16 bits, including the AD386's differential amplifier when measured at room temperature. The 5534 has lower voltage noise and will cause only a 1 or 2 μV rms increase in the total noise at the differential amplifier's output. The NE5534 lacks the precision offset and drift performance of the AD744.

Multiplexed throughput can be improved with the proper choice of system timing. If the new input channel is selected while the AD386 is in Hold mode, then multiplexer, buffer, and differential amplifier settling can occur during the A/D conversion. In this case throughput is determined only by the sum of the T/H acquisition and A/D conversion times. The effects of T/H feedthrough must be considered when using this type of overlap in system timing.

There is another solution to many of the problems of multiplexed systems when the speed of channel switching is not critical: relays. Relays should be selected for good shielding, low thermal EMF, and low on-resistance. The only significant drawback of this approach, other than switching speed and size, is power dissipation. In all other respects relays offer a near-perfect solution to the problems of high resolution system design discussed above.

DYNAMIC PERFORMANCE

Dynamic characteristics such as signal-to-noise ratio (SNR) and total harmonic distortion (THD) are important in many signal processing applications. SNR and THD are affected by both the T/H and A/D. The errors contributed by the T/H are generally dependent upon the input signal frequency, while those contributed by the A/D converter usually are not. The dynamic performance of a T/H-A/D pair is characterized using Fast Fourier Transform (FFT) techniques.

Figures 27–31 show the results of several 1024-point FFTs which demonstrate the exceptional distortion and noise performance of the AD386 when combined with the AD1377. These FFTs were obtained using a circuit similar to that of Figure 24. The input signal was processed by both the differential amplifier and T/H sections of the AD386 and was sampled at an 83.333 kHz rate. The AD1377's clock was adjusted to yield an 8.0 μs conversion time, which provided 4.0 μs for the AD386 to acquire each new sample. The vertical scale for these figures is based on a full-scale input referenced as 0 dB. The system was configured for a 10 volt span.

Figures 27 and 28 illustrate the system's low frequency noise and distortion performance. The input frequency is 1.546 kHz. When the input is −0.3 dB, nearly full scale, the largest harmonic component is −102.8 dB (Figure 27). Total harmonic distortion, the rms sum of the second through fifth harmonics, is −99.9 dB. The signal to noise ratio is 89.9 dB. The ultimate noise floor can be determined using a lower level input. Reducing the input level about 20 dB, as in Figure 28, decreases the

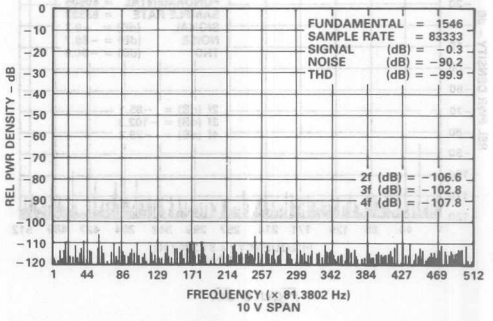


Figure 27.

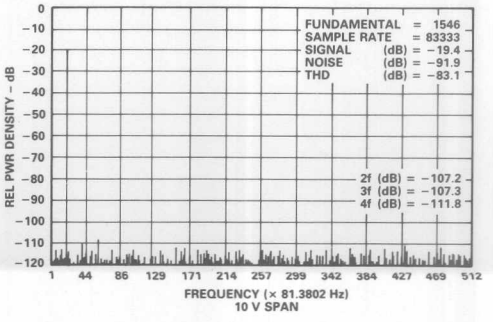


Figure 28.

AD386 noise contribution of about 45 μV rms. The FFT noise floor would improve about 2 dB with the system configured for a 20 volt span because the effect of noise contributed by the AD386 is reduced as a result of the increased LSB size.

System performance just beyond the high end of the audio band is shown in Figure 29. Here the input is a −0.3 dB sinusoid at 21.24 kHz. The only significant harmonic component, the second harmonic, is −91.9 dB with respect to the fundamental, and THD is −91.1 dB. The noise floor is 0.5 dB greater than in Figure 27. The additional noise is contributed by higher-order harmonics, the second through fifth harmonics have been excluded from the noise floor calculations, but higher harmonics are considered to be "noise". These harmonics arise from the AD386's aperture jitter. The additional noise is consistent with an rms jitter of 40 ps.

In Figures 30 and 31, −0.3 dB and −20.1 dB inputs at 40.61 kHz show system performance near the Nyquist frequency. Even at this high frequency a full-scale input produces THD of only −84.6 dB, dominated by the second harmonic at −85.1 dB (Figure 31). In Figure 31 the harmonics have been eliminated by reducing the input level by a factor of 10.

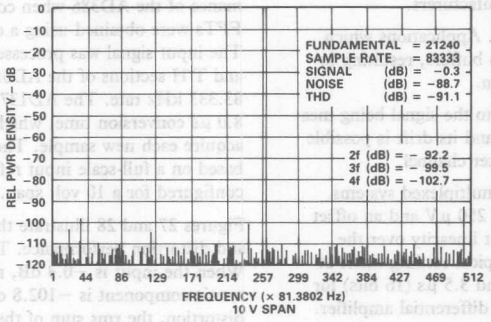


Figure 29.

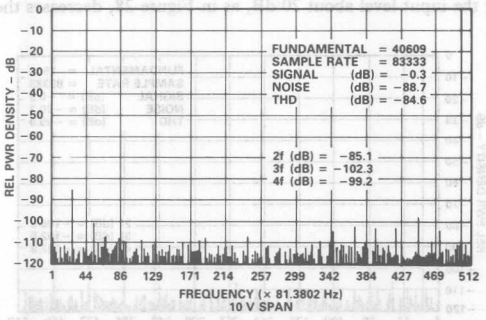


Figure 30.

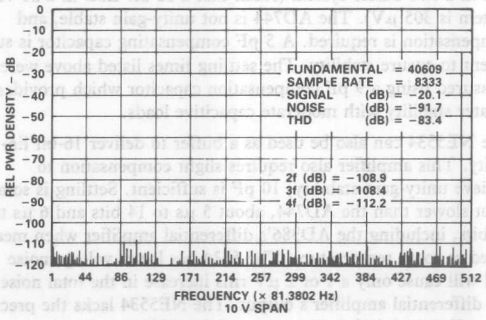


Figure 31.

ANALOG DEVICES

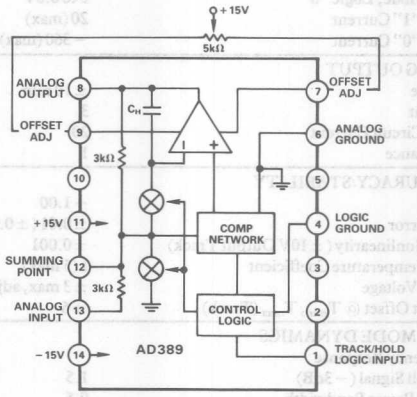
High Resolution Track-and-Hold Amplifier

AD389

FEATURES

Companion to High Resolution A/D Converters
Fast Acquisition Time: 2.5μs to ±0.003%
Low Droop Rate: 0.1μV/μs
Aperture Jitter: 400ps
Internal Hold Capacitor
Unity Gain Inverter
Low Power Dissipation: 300mW

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD389 is a high accuracy, adjustment free track-and-hold amplifier designed for high resolution data acquisition applications. The fast acquisition time (2.5μs to ±0.003%) and low aperture jitter (400ps) make it suitable for use with fast A/D converters to digitize signals up to 40kHz.

The AD389 is complete with an internal hold capacitor and it incorporates a compensation network which minimizes the sample to hold charge offset.

Typical applications for the AD389 include sampled data systems, peak hold functions, strobed measurement systems and simultaneous sampling converter systems. When used with autozero and autocalibration techniques, this T/H combined with a high linearity A/D will offer 14-bit performance over the converter's full no-missing-code temperature range.

The device is available in two versions: the "K" specified for operation over the 0 to +70°C commercial temperature range and the "B" specified over the full industrial temperature range, −25°C to +85°C. High reliability processing is available; contact factory for information.

PRODUCT HIGHLIGHTS

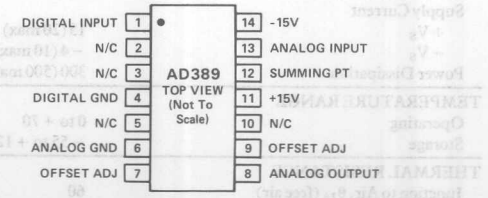
1. The AD389 is the ideal companion track-and-hold amplifier to 14-bit accurate A/D converters.
2. The AD389 provides separate analog and digital grounds, thus improving the device's immunity to ground and switching transients.
3. The droop rate is only 0.1μV/μs so that it may be used in slower high resolution systems without the loss of accuracy.
4. The fast acquisition time and low aperture make it suitable for high speed data acquisition systems and digital audio recording.
5. The AD389 T/H amplifier is ideal for applications requiring wide dynamic range.
6. Clever circuit design eliminates any measurable thermal tail (see Figures 1a and 1b).

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD389KD	0 to +70°C	DH-14A
AD389BD	−25°C to +85°C	DH-14A

*DH-14A = Ceramic DIP. For outline information see Package Information section.

PIN CONFIGURATION



AD389—SPECIFICATIONS (typical @ +25°C and nominal power supply voltage of ±15 V unless otherwise noted)

Model	AD389KD	AD389BD	Units
ANALOG INPUT			
Voltage Range	±10 min	*	V
Overvoltage, no damage	±15 max	*	V
Impedance	3000	*	Ω
DIGITAL INPUT (TTL Compatible)			
Track Mode, Logic "1"	2 to 5.5V	*	V
Hold Mode, Logic "0"	0 to 0.8V	*	V
Logic "1" Current	20 (max)	*	μA
Logic "0" Current	−360 (max)	*	μA
ANALOG OUTPUT			
Voltage	±10 min	*	V
Current	3	*	mA
Short Circuit Current	20	*	mA
Impedance	1	*	Ω
DC ACCURACY/STABILITY			
Gain	−1.00	*	V/V
Gain Error	±0.01 (±0.02 max)	*	%
Gain Nonlinearity (±10V Output Track)	±0.001	*	%
Gain Temperature Coefficient	1 (5 max)	*	ppm/°C
Offset Voltage	±3 max, adjustable to zero	*	mV
Output Offset @ T_{min}, T_{max} (Track)	±6	*	mV
TRACK MODE DYNAMICS			
Frequency Response			
Small Signal (−3dB)	1.5	*	MHz
Full Power Bandwidth	0.5	*	MHz
Slew Rate	30	*	V/μs
Noise in Track Mode, dc to 1.0MHz	200	*	μV rms
TRACK-TO-HOLD SWITCHING			
Aperture Time	30	*	ns
Aperture Uncertainty (Jitter)	0.4	*	ns
Offset Step (Pedestal)	±2 (4 max)	*	mV
Pedestal with Temperature	±4	±6	mV
Switching Transient			
Amplitude	200	*	mV
Settling to 1mV	0.5 (2 max)	*	μs
Settling to 0.3mV	1.0 (3 max)	*	μs
HOLD MODE DYNAMICS			
Droop Rate	0.1 (1 max)	*	μV/μs
Droop Rate at T_{max}	10 max	40 max	μV/μs
Feedthrough Rejection (10V p-p @ 20kHz)	86 (74 min)	*	dB
HOLD-TO-TRACK DYNAMICS			
Acquisition Time to ±0.01% of 20V	1.5 (3 max)	*	μs
Acquisition Time to ±0.003% of 20V	2.5 (5 max)	*	μs
POWER REQUIREMENTS			
Nominal Voltages for Rated Performance	±15 (±3%)	*	V
Operating Range[1]	±11 to ±18	*	V
Power Supply Rejection	100	*	μV/V
Supply Current			
$+V_S$	15 (20 max)	*	mA
$-V_S$	−4 (10 max)	*	mA
Power Dissipation	300 (500 max)	*	mW
TEMPERATURE RANGE			
Operating	0 to +70	−25 to +85	°C
Storage	−55 to +125	*	°C
THERMAL RESISTANCE			
Junction to Air, θ_{JA} (free air)	60	*	°C/W
Junction to Case, θ_{JC}	20	*	°C/W

NOTES

[1]Operating to derated performance with $|V_{IN}| < |V_S - 5V|$.

*Specifications same as AD389KD.

Specifications subject to change without notice.

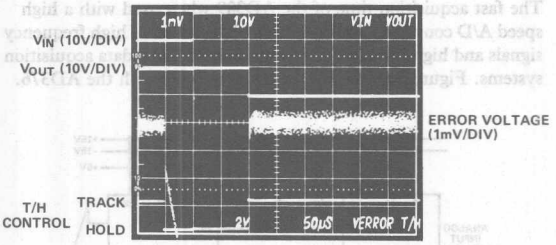


Figure 1a. Acquisition Time after 100μs in the Hold Mode. The AD389 shows No "Thermal Tail."

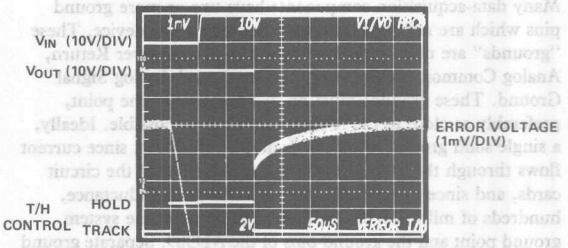


Figure 1b. Typical Thermal Tail and Acquisition Time of Other 12-Bit T/Hs Make Them Unsuitable for High Resolution Applications

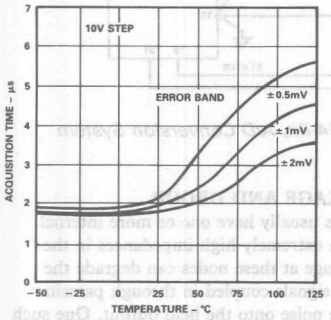


Figure 2. Acquisition Time vs. Temperature

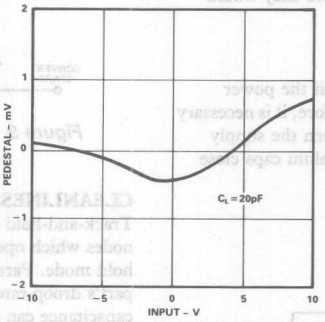


Figure 3. Pedestal vs. Input Voltage

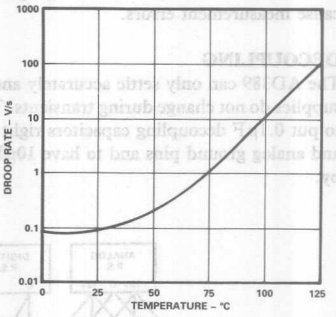


Figure 4. Droop Rate vs. Temperature

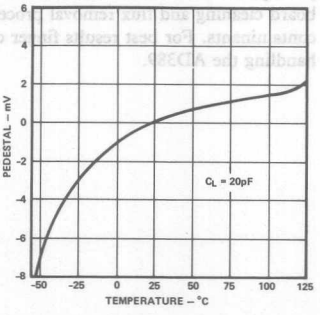


Figure 5. Pedestal vs. Temperature

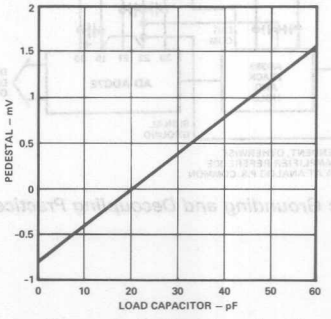


Figure 6. Pedestal vs. Load Capacitor

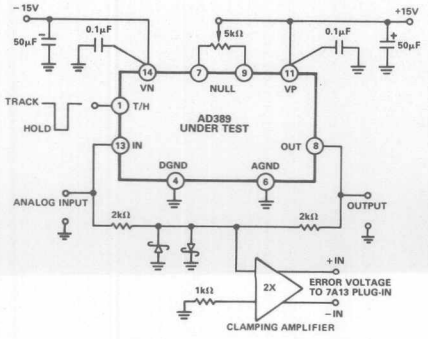


Figure 7. Pedestal and Acquisition Time Test Circuit

OFFSET ADJUST TRIM

In most data acquisition systems only one offset adjustment is made. In many cases it is the offset adjust of the ADC that is used to cancel all other accumulated system offsets. The offset or pedestal of the AD389 can be nulled by means of 5kΩ potentiometer between pins 7, 9, and 11. If the offset of the AD389 is not adjusted, then connect pins 7 and 9 to pin 14, the negative supply. Otherwise the high impedance of the null pin together with parasitic capacitances can cause tail effects.

pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, preferably as close to the A-to-D converter as possible. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pins of the AD389. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

DECOUPLING

The AD389 can only settle accurately and fast if the power supplies do not change during transients. Therefore, it is necessary to put 0.1μF decoupling capacitors right between the supply and analog ground pins and to have 10μF tantalum caps close by.

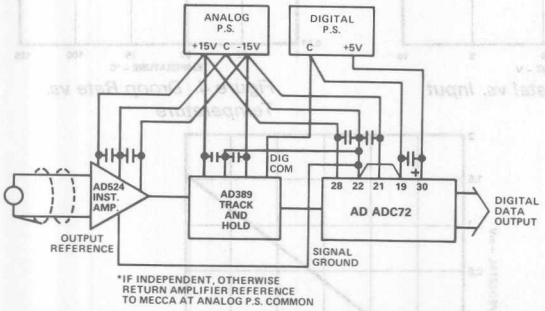


Figure 8. Basic Grounding and Decoupling Practice

speed A/D converter allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. Figure 9 shows the use of an AD389 with the AD376.

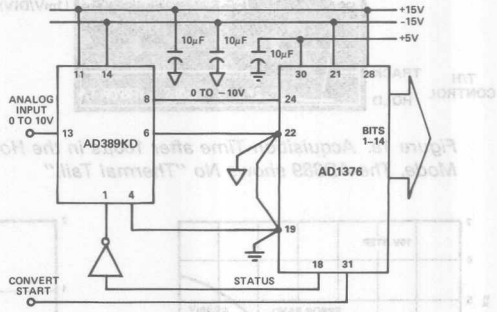


Figure 9. 20kHz-14-Bit, A/D Conversion System

CLEANLINESS, LEAKAGE AND DROOP

Track-and-hold amplifiers usually have one or more internal nodes which operate with extremely high impedances in the hold mode. Parasitic leakage at these nodes can degrade the part's droop rate, and ac signals coupled in through parasitic capacitance can introduce noise onto the held output. One such dc leakage path can be produced by the residual oils left on the package after it has been handled with bare fingers. Most normal board cleaning and flux removal procedures will remove these contaminants. For best results finger cots should be used when handling the AD389.

Sample-and-Hold Amplifier

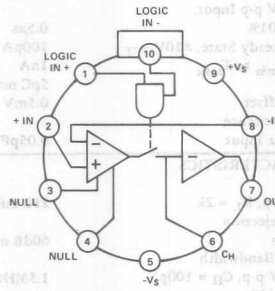
AD582

FEATURES

Suitable for 12-Bit Applications
High Sample/Hold Current Ratio: 10^7
Low Acquisition Time: 6μs to 0.1%
Low Charge Transfer: <2pC
High Input Impedance in Sample-and-Hold Modes
Connect in Any Op Amp Configuration
Differential Logic Inputs
MIL-STD-883 Compliant Versions Available

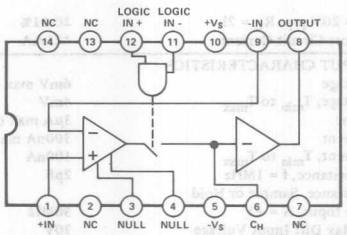
PIN CONFIGURATIONS

10-Pin TO-100



TOP VIEW

14-Pin DIP TO-116



TOP VIEW

PRODUCT DESCRIPTION

The AD582 is a low-cost integrated circuit sample-and-hold amplifier consisting of a high performance operational amplifier, a low leakage analog switch and a JFET integrating amplifier – all fabricated on a single monolithic chip. An external holding capacitor, connected to the device, completes the sample-and-hold function.

With the analog switch closed, the AD582 functions like a standard op amp; any feedback network may be connected around the device to control gain and frequency response. With the switch open, the capacitor holds the output at its last level, regardless of input voltage.

Typical applications for the AD582 include sampled data systems, D/A deglitchers, analog de-multiplexers, auto null systems, strobed measurement systems and A/D speed enhancement.

The device is available in two versions: the "K" specified for operation over the 0 to +70°C commercial temperature range and the "S" specified over the extended temperature range, –55°C to +125°C. All versions may be obtained in either the hermetic sealed, TO-100 can or the TO-116 DIP.

PRODUCT HIGHLIGHTS

1. The specially designed input stage presents a high impedance to the signal source in both sample and hold modes (up to ±12V). Even with signal levels up to $\pm V_S$, no undesirable signal inversion, peaking or loss of hold voltage occurs.
2. The AD582 may be connected in any standard op amp configuration to control gain or frequency response and provide signal inversion, etc.
3. The AD582 offers a high, sample-to-hold current ratio: 10^7. The ratio of the available charging current to the holding leakage current is often used as a figure of merit for a sample and hold circuit.
4. The AD582 has a typical charge transfer less than 2pC. A low charge transfer produces less offset error and permits the use of smaller hold capacitors for faster signal acquisition.
5. The AD582 provides separate analog and digital grounds, thus improving the device's immunity to ground and switching transients.
6. The AD582 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD582/883B data sheet for detailed specifications.

AD582—SPECIFICATIONS (typical @ +25°C, V_S = ±15V and C_H = 1000pF, A = +1 unless otherwise specified)

MODEL	AD582K	AD582S
SAMPLE/HOLD CHARACTERISTICS		
Acquisition Time, 10V Step to 0.1%, C_H = 100pF	6μs	*
Acquisition Time, 10V Step to 0.01%, C_H = 1000pF	25μs	*
Aperture Delay, 20V p-p Input, Hold 0V	200ns	*
Aperture Jitter, 20V p-p Input, Hold 0V	15ns	*
Settling Time, 20V p-p Input, Hold 0V, to 0.01%	0.5μs	*
Droop Current, Steady State, ±10V_{OUT}	100pA max	*
Droop Current, T_{min} to T_{max}	1nA	150nA max
Charge Transfer	5pC max (1.5pC typ)	*
Sample to Hold Offset	0.5mV	*
Feedthrough Capacitance 20V p-p, 10kHz Input	0.05pF	*
TRANSFER CHARACTERISTICS		
Open Loop Gain V_{OUT} = 20V p-p, R_L = 2k	25k min (50k typ)	*
Common Mode Rejection V_{CM} = 20V p-p	60dB min (70dB typ)	*
Small Signal Gain Bandwidth V_{OUT} = 100mV p-p, C_H = 100pF	1.5MHz	*
Full Power Bandwidth V_{OUT} = 20V p-p, C_H = 100pF	70kHz	*
Slew Rate V_{OUT} = 20V p-p, C_H = 100pF	3V/μs	*
Output Resistance Hold Mode, I_{OUT} = ±5mA	12Ω	*
Linearity V_{OUT} = 20V p-p, R_L = 2k	±0.01%	*
Output Short Circuit Current	±25mA	*
ANALOG INPUT CHARACTERISTICS		
Offset Voltage	6mV max (2mV typ)	*
Offset Voltage, T_{min} to T_{max}	4mV	8mV max (5mV typ)
Bias Current	3μA max (1.5μA typ)	*
Offset Current	300nA max (75nA typ)	*
Offset Current, T_{min} to T_{max}	100nA	400nA max (100nA typ)
Input Capacitance, f = 1MHz	2pF	*
Input Resistance, Sample or Hold 20V p-p Input, A = +1	30MΩ	*
Absolute Max Diff Input Voltage	30V	*
Absolute Max Input Voltage, Either Input	±V_S	*
DIGITAL INPUT CHARACTERISTICS		
+Logic Input Voltage		
Hold Mode, T_{min} to T_{max}, -Logic @ 0V	+2V min	*
Sample Mode, T_{min} to T_{max}, -Logic @ 0V	+0.8V max	*
+Logic Input Current		
Hold Mode, +Logic @ +5V, -Logic @ 0V	1.5μA	*
Sample Mode, +Logic @ 0V, -Logic @ 0V	1nA	*
-Logic Input Current		
Hold Mode, +Logic @ +5V, -Logic @ 0V	24μA	*
Sample Mode, +Logic @ 0V, -Logic @ 0V	4μA	*
Absolute Max Diff Input Voltage, +L to -L	+15V/-6V	*
Absolute Max Input Voltage, Either Input	±V_S	*
POWER SUPPLY CHARACTERISTICS		
Operating Voltage Range	±9V to ±18V	±9V to ±22V
Supply Current, R_L = ∞	4.5mA max (3mA typ)	*
Power Supply Rejection, ΔV_S = 5V, Sample Mode (see next page)	60dB min (75dB typ)	*
TEMPERATURE RANGE		
Specified Performance	0 to +70°C	−55°C to +125°C
Operating	−25°C to +85°C	−55°C to +125°C
Storage	−65°C to +150°C	*
Lead Temperature (Soldering, 15 sec)	+300°C	*
PACKAGE OPTION[1,2]		
TO-100 (H-10A)	AD582KH	AD582SH
TO-116 (D-14)	AD582KD	AD582SD

NOTES
*Specifications same as AD582K.
[1]D = Ceramic DIP; H = Hermetic Metal Can. For outline information see Package Information section.
[2]For AD582/883B specifications, refer to Analog Devices Military Products Databook.
Specifications subject to change without notice.

APPLYING THE AD582

Both the inverting and non-inverting inputs are brought out to allow op amp type versatility in connecting and using the AD582. Figure 1 shows the basic non-inverting unity gain connection requiring only an external hold capacitor and the usual power supply bypass capacitors. An offset null pot can be added for more critical applications.

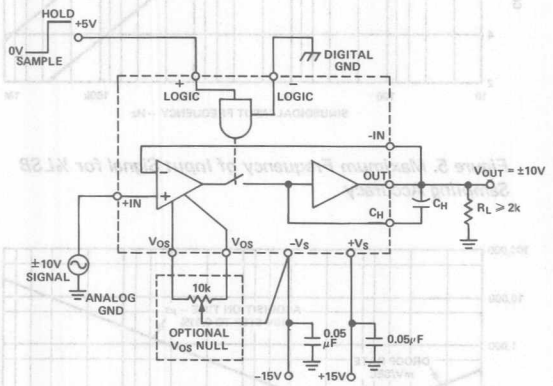


Figure 1. Sample and Hold with A = +1

Figure 2 shows a non-inverting configuration where voltage gain, A_V, is set by a pair of external resistors. Frequency shaping or non-linear networks can also be used for special applications.

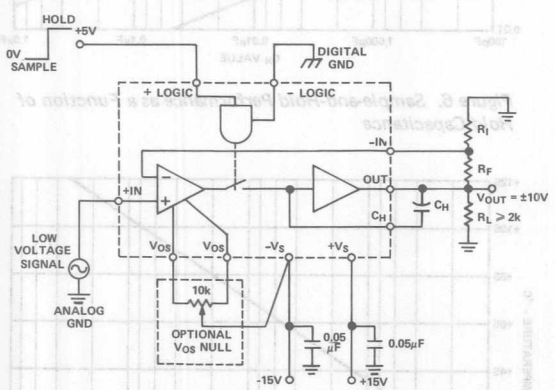


Figure 2. Sample and Hold with A = (1 + R_F/R_I)

The hold capacitor, C_H, should be a high quality polystyrene (for temperatures below +85°C) or Teflon type with low dielectric absorption. For high speed, limited accuracy applications, capacitors as small as 100pF may be used. Larger values are required for accuracies of 12 bits and above in order to minimize feedthrough, sample to hold offset and droop errors (see Figure 6). Care should be taken in the circuit layout to minimize coupling between the hold capacitor and the digital or signal inputs.

In the hold mode, the output voltage will follow any change in the $-V_S$ supply. Consequently, this supply should be well regulated and filtered.

Biasing the +Logic Input anywhere between -6V to +0.8V with respect to the -Logic will set the sample mode. The hold mode will result from any bias between +2.0V and ($+V_S$ - 3V). The sample and hold modes will be controlled differentially with the absolute voltage at either logic input ranging from $-V_S$ to within 3V of $+V_S$ (V_S - 3V). Figure 3 illustrates some examples of the flexibility of this feature.

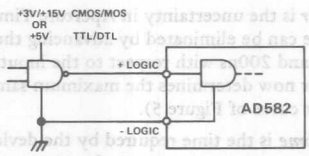


Figure 3A. Standard Logic Connection

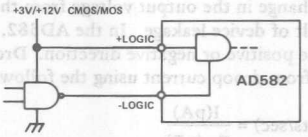


Figure 3B. Inverted Logic Sense Connection

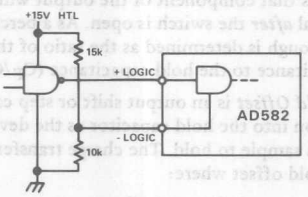


Figure 3C. High Threshold Logic Connection

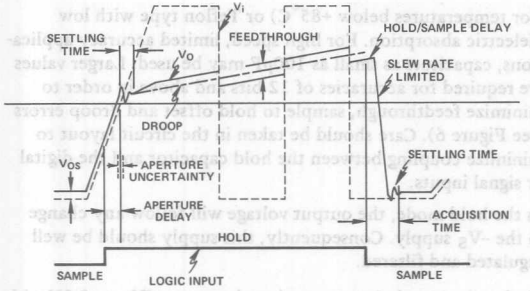


Figure 4. Pictorial Showing Various S/H Characteristics

Aperture Delay is the time required after the "hold" command until the switch is fully open and produces a delay in the effective sample timing. Figure 5 is a plot giving the maximum frequency at which the AD582 can sample an input with a given accuracy (lower curve).

Aperture Jitter is the uncertainty in Aperture Time. The Aperture Time can be eliminated by advancing the sample-to-hold command 200ns with respect to the input signal. The Aperture Jitter now determines the maximum sampling frequency (upper curve of Figure 5).

Acquisition Time is the time required by the device to reach its final value within a given error band after the sample command has been given. This includes switch delay time, slewing time and settling time for a given output voltage change.

Droop is the change in the output voltage from the "held" value as a result of device leakage. In the AD582, droop can be in either the positive or negative direction. Droop rate may be calculated from droop current using the following formula:

$$\frac{\Delta V}{\Delta T}\,(\text{Volts/sec}) = \frac{I(\text{pA})}{C_H(\text{pF})}$$

(See also Figure 6.)

Feedthrough is that component of the output which follows the input signal *after* the switch is open. As a percentage of the input, feedthrough is determined as the ratio of the feedthrough capacitance to the hold capacitance (C_F/C_H).

Sample-to-Hold Offset is an output shift or step caused by charge injection into the hold capacitor as the device is switched from sample to hold. The charge transfer generates a sample-to-hold offset where:

$$\text{S/H Offset (V)} = \frac{\text{Charge (pC)}}{C_H\,(\text{pF})}$$

This offset also has a dc component as shown in Figure 6.

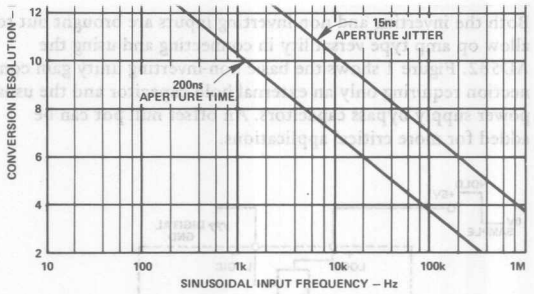


Figure 5. Maximum Frequency of Input Signal for ½LSB Sampling Accuracy

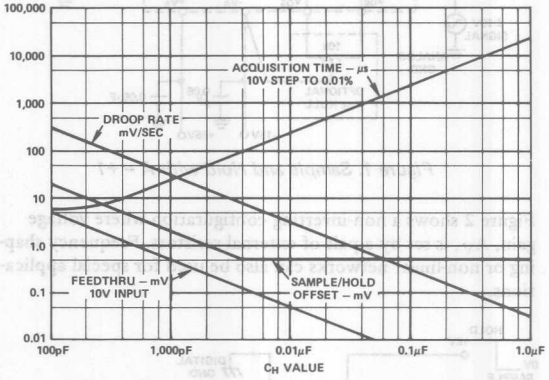


Figure 6. Sample-and-Hold Performance as a Function of Hold Capacitance

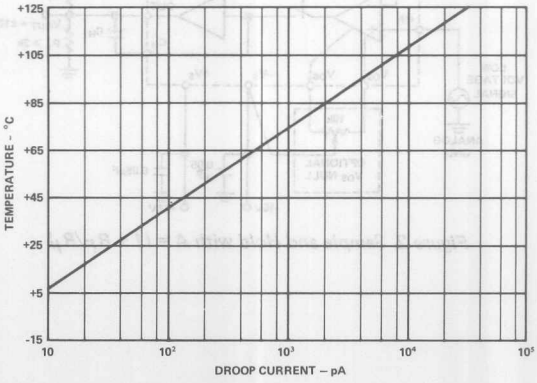


Figure 7. Droop Current vs. Temperature

ANALOG DEVICES

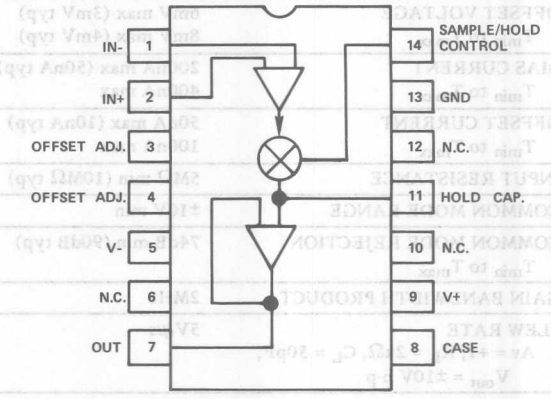
Sample-and-Hold Amplifier

AD583

FEATURES

High Sample-to-Hold Current Ratio: 10^6
High Slew Rate: 5V/μs
High Bandwidth: 2MHz
Low Aperture Time: 50ns
Low Charge Transfer: 10pC
DTL/TTL Compatible
May Be Used as Gated Op Amp

PIN CONFIGURATION



PRODUCTION DESCRIPTION

The AD583 is a monolithic sample-and hold circuit consisting of a high performance operational amplifier in series with a low leakage analog switch and unity gain amplifier. An external hold capacitor, connected to the switch output, completes the sample-and-hold or track-and-hold function.

With the analog switch closed, the AD583 functions like a standard op amp; any feedback network may be connected around the device to control gain and frequency response. With the switch open the capacitor holds the output at its previous level.

The AD583 may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.

PRODUCT HIGHLIGHTS

1. Sample-and-hold operation is obtained with the addition of one external capacitor.
2. Low charge transfer (10pC) and high sample-to-hold current ratio insure accurate tracking.
3. Any gain or frequency response is available using standard op amp feedback networks.
4. High slew rate and low aperture time permit sampling of rapidly changing signals.
5. Output, gated through a low leakage analog switch, also makes the AD583 useful for applications such as analog switches, peak holding circuits, etc.

SPECIFICATIONS (typical @ +25°C, hold capacitor of 1000pF and ±15V dc unless otherwise specified)

MODEL	AD583KD
OPEN LOOP GAIN R_L = 2kΩ, T_{min} to T_{max}	25k min (50k typ)
OUTPUT VOLTAGE SWING R_L = 2kΩ, T_{min} to T_{max}	±10V min
OUTPUT CURRENT	±10mA min
OUTPUT RESISTANCE	5Ω
OFFSET VOLTAGE T_{min} to T_{max}	6mV max (3mV typ) 8mV max (4mV typ)
BIAS CURRENT T_{min} to T_{max}	200nA max (50nA typ) 400nA max
OFFSET CURRENT T_{min} to T_{max}	50nA max (10nA typ) 100nA max
INPUT RESISTANCE	5MΩ min (10MΩ typ)
COMMON MODE RANGE	±10V min
COMMON MODE REJECTION T_{min} to T_{max}	74dB min (90dB typ)
GAIN BANDWIDTH PRODUCT	2MHz
SLEW RATE Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = ±10V p-p	5V/μs
RISE TIME Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = 400mV p-p	100ns
OVERSHOOT Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = 400mV p-p	20%
DIGITAL INPUT CURRENT V_{in} = 0, T_{min} to T_{max} V_{in} = +5.0V, T_{min} to T_{max}	 0.8mA max (Logic "Sample") 20μA max (Logic "Hold")
DIGITAL INPUT VOLTAGE Low T_{min} to T_{max} High T_{min} to T_{max}	 0.8V max 2.0V min
ACQUISITION TIME Av = +1, R_L = 2kΩ, C_L = 50pF to 0.1% of final value: to 0.01% of final value:	 4μs 5μs
APERTURE TIME	50ns
APERTURE JITTER	5ns
DRIFT CURRENT[1] T_{min} to T_{max}	50pA max (5pA typ) 1.0nA max (0.05nA typ)
CHARGE TRANSFER	20pC max (10pC typ)
SUPPLY CURRENT	5.0mA max (2.5mA typ)
POWER SUPPLY REJECTION[2]	74dB min (90dB typ)
OPERATING TEMP	0 to +70°C
STORAGE TEMP	–65°C to +150°C
PACKAGE OPTION[3] D-14	 AD583KD

ABSOLUTE MAXIMUM RATINGS

Voltage between V+ and V- Terminals	40V
Differential Input Voltage	±30V
Digital Voltage (Pin 14)	+8V, -15V
Output Current	Short Circuit Protected
Internal Power Dissipation	30mW (Derate power dissipation by 4.3mW/°C above +150°C ambient temperature)

NOTES
[1] Voltage on hold is zero.
[2] Sample mode only.
[3] D = Ceramic DIP. For outline information see Package Information section.

Specifications subject to change without notice.

High Speed, Precision Sample-and-Hold Amplifier

AD585

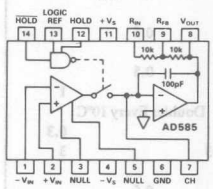
FEATURES

3.0μs Acquisition Time to ±0.01% max
Low Droop Rate: 1.0mV/ms max
Sample/Hold Offset Step: 3mV max
Aperture Jitter: 0.5ns
Extended Temperature Range: −55°C to +125°C
Internal Hold Capacitor
Internal Application Resistors
±12V or ±15V Operation
Available in Surface Mount

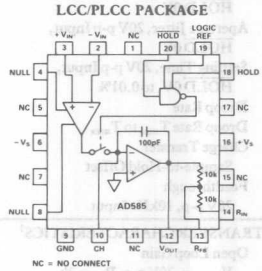
APPLICATIONS

Data Acquisition Systems
Data Distribution Systems
Analog Delay & Storage
Peak Amplitude Measurements
MIL-STD-883 Compliant Versions Available

DIP



LCC/PLCC PACKAGE



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD585 is a complete monolithic sample-and-hold circuit consisting of a high performance operational amplifier in series with an ultralow leakage analog switch and a FET input integrating amplifier. An internal holding capacitor and matched applications resistors have been provided for high precision and applications flexibility.

The performance of the AD585 makes it ideal for high speed 10- and 12-bit data acquisition systems, where fast acquisition time, low sample-to-hold offset, and low droop are critical. The AD585 can acquire a signal to ±0.01% in 3μs maximum, and then hold that signal with a maximum sample-to-hold offset of 3mV and less than 1mV/ms droop, using the on-chip hold capacitor. If lower droop is required, it is possible to add a larger external hold capacitor.

The high-speed analog switch used in the AD585 exhibits aperture jitter of 0.5ns, enabling the device to sample full-scale (20V peak-to-peak) signals at frequencies up to 78kHz with 12-bit precision.

The AD585 can be used with any user-defined feedback network to provide any desired gain in the sample mode. On-chip precision thin-film resistors can be used to provide gains of +1, −1, or +2. Output impedance in the hold mode is sufficiently low to maintain an accurate output signal even when driving the dynamic load presented by a successive-approximation A/D converter. However, the output is protected against damage from accidental short circuits.

The control signal for the HOLD command can be either active high or active low. The differential HOLD signal is compatible with all logic families, if a suitable reference level is provided. An on-chip TTL reference level is provided for TTL compatibility.

The AD585 is available in three performance grades. The JP grade is specified for the 0 to +70°C commercial temperature range and packaged in a 20-pin PLCC. The AQ grade is specified for the −25°C to +85°C industrial temperature range and is packaged in a 14-pin cerdip. The SQ and SE grades are specified for the −55°C to +125°C military temperature range and are packaged in a 14-pin cerdip and 20-pin LCC.

PRODUCT HIGHLIGHTS

1. The fast acquisition time (3μs) and low aperture jitter (0.5ns) make it the first choice for very high speed data acquisition systems.
2. The droop rate is only 1.0mV/ms so that it may be used in slower high accuracy systems without the loss of accuracy.
3. The low charge transfer of the analog switch keeps sample-to-hold offset below 3mV with the on-chip 100pF hold capacitor, eliminating the trade-off between acquisition time and S/H offset required with other SHAs.
4. The AD585 has internal pretrimmed application resistors for applications versatility.
5. The AD585 is complete with an internal hold capacitor for ease of use. Capacitance can be added externally to reduce the droop rate when long hold times and high accuracy are required.
6. The AD585 is recommended for use with 10- and 12-bit successive-approximation A/D converters such as AD573, AD574A, AD674A, AD7572 and AD7672.
7. The AD585 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD585/883B data sheet for detailed specifications.

Model	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
SAMPLE/HOLD CHARACTERISTICS										
Acquisition Time, 10V Step to 0.01%			3			3			3	µs
20V Step to 0.01%			5			5			5	µs
Aperture Time, 20V p-p Input, $\overline{HOLD}$ 0V		35			35			35		ns
Aperture Jitter, 20V p-p Input, $\overline{HOLD}$ 0V		0.5			0.5			0.5		ns
Settling Time, 20V p-p Input, $\overline{HOLD}$ 0V, to 0.01%		0.5			0.5			0.5		µs
Droop Rate			1			1			1	mV/ms
Droop Rate T_{min} to T_{max}		Doubles Every 10°C			Doubles Every 10°C			Doubles Every 10°C		
Charge Transfer			0.3			0.3			0.3	pC
Sample-to-Hold Offset	−3		3	−3		3	−3		3	mV
Feedthrough 20V p-p, 10kHz Input		0.5			0.5			0.5		mV
TRANSFER CHARACTERISTICS[1]										
Open Loop Gain V_{OUT} = 20V p-p, R_L = 2k		200,000			200,000			200,000		V/V
Application Resistor Mismatch			0.3			0.3			0.3	%
Common Mode Rejection V_{CM} = ± 10V	80			80			80			dB
Small Signal Gain Bandwidth V_{OUT} = 100mV p-p		2.0			2.0			2.0		MHz
Full Power Bandwidth V_{OUT} = 20V p-p		160			160			160		kHz
Slew Rate V_{OUT} = 20V p-p		10			10			10		V/µs
Output Resistance (Sample Mode) I_{OUT} = ± 10mA			0.05			0.05			0.05	Ω
Output Short Circuit Current		50			50			50		mA
Output Short Circuit Duration		Indefinite			Indefinite			Indefinite		
ANALOG INPUT CHARACTERISTICS										
Offset Voltage			5			2			2	mV
Offset Voltage, T_{min} to T_{max}			6			3			3	mV
Bias Current			2			2			2	nA
Bias Current T_{min} to T_{max}			5			5			50[2]	nA
Input Capacitance, f = 1MHz		10			10			10		pF
Input Resistance, Sample or Hold 20V p-p Input, A = +1		10^{12}			10^{12}			10^{12}		Ω
DIGITAL INPUT CHARACTERISTICS										
TTL Reference Output	1.2	1.4	1.6	1.2	1.4	1.6	1.2	1.4	1.6	V
Logic Input High Voltage T_{min} to T_{max}	2.0			2.0			2.0			V
Logic Input Low Voltage T_{min} to T_{max}			0.8			0.8			0.7	V
Logic Input Current (Either Input)			50			50			50	µA
POWER SUPPLY CHARACTERISTICS										
Operating Voltage Range	+5, −10.8		±18	+5, −10.8		±18	+5, −10.8		±18	V
Supply Current, R_L = ∞	6		10	6		10	6		10	mA
Power Supply Rejection, Sample Mode	70			70			70			dB
TEMPERATURE RANGE Specified Performance	0		+70	−25		+85	−55		+125	°C
PACKAGE OPTIONS[3,4]										
Cerdip (Q-14)					AD585AQ			AD585SQ		
LCC (E-20A)								AD585SE		
PLCC (P-20A)		AD585JP								
PRICES (100s)		9.15			9.90			26.85 (SQ) 30.08 (SE)		$

NOTES

[1]Maximum input signal is the minimum supply minus a headroom voltage of 2.5V.

[2]Not tested at −55°C.

[3]E = Leadless Ceramic Chip Carrier; P = Plastic Leaded Chip Carrier; Q = Cerdip.

[4]For AD585/883B specifications, refer to Analog Devices Military Products Databook.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supplies ($+V_S$, $-V_S$)	±18V
Logic Inputs	$\pm V_S$
Analog Inputs	$\pm V_S$
R_{IN}, R_{FB} Pins	$\pm V_S$
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering)	300°C
Output Short Circuit to Ground	Indefinite
TTL Logic Reference Short Circuit to Ground	Indefinite

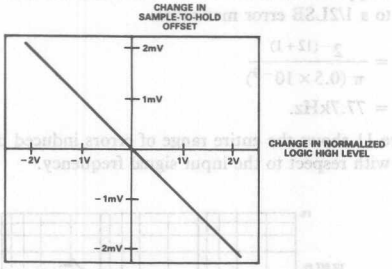


Figure 1. Sample-to-Hold Offset vs. Logic Level (HOLD Active)

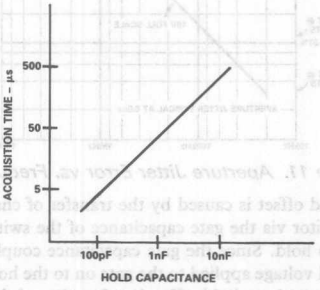


Figure 2. Acquisition Time vs. Hold Capacitance (10V Step to 0.01%)

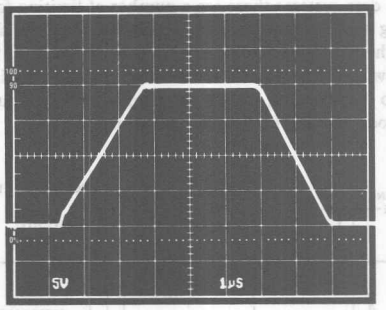


Figure 3. Large Signal Response, Sample Mode

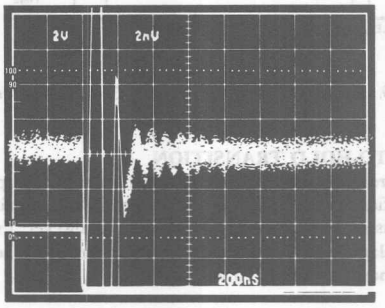


Figure 4. Sample-to-Hold Settling Time (HOLD Active)

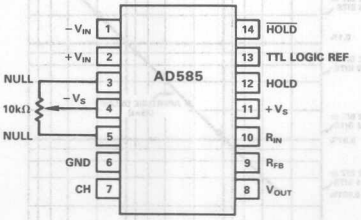


Figure 5. DIP Pin Configuration

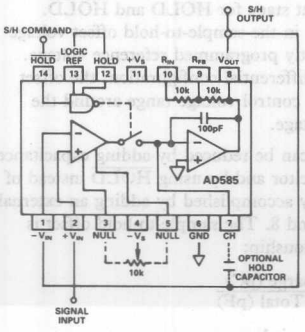


Figure 6. Connection Diagram, Gain = +1, HOLD Active

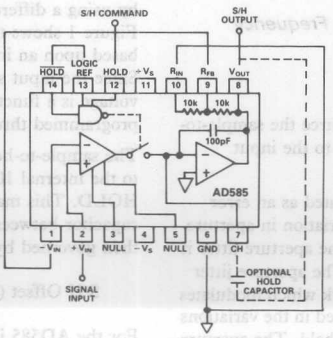


Figure 7. Connection Diagram, Gain = +2, HOLD Active

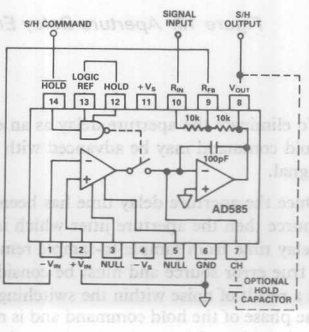


Figure 8. Connection Diagram, Gain = −1, HOLD Active

SAMPLED DATA SYSTEMS

In sampled data systems there are a number of limiting factors in digitizing high frequency signals accurately. Figure 9 shows pictorially the sample-and-hold errors that are the limiting factors. In the following discussions of error sources the errors will be divided into the following groups: 1. Sample-to-Hold Transition, 2. Hold Mode and 3. Hold-to-Sample Transition.

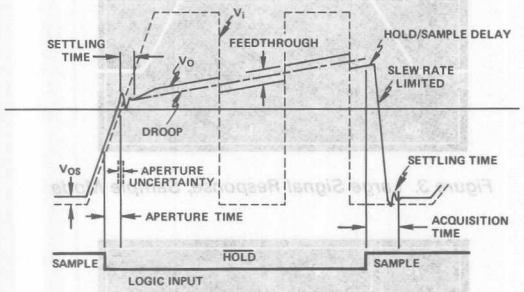


Figure 9. Pictorial Showing Various S/H Characterstics

SAMPLE-TO-HOLD TRANSITION

The aperture delay time is the time required for the sample-and-hold amplifier to switch from sample to hold. Since this is effectively a constant then it may be tuned out. If however, the aperture delay time is not accounted for then errors of the magnitude as shown in Figure 10 will result.

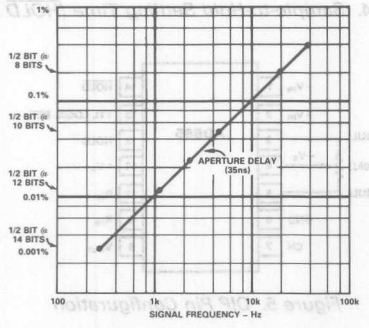


Figure 10. Aperture Delay Error vs. Frequency

To eliminate the aperture delay as an error source the sample-to-hold command may be advanced with respect to the input signal.

Once the aperture delay time has been eliminated as an error source then the aperture jitter which is the variation in aperture delay time from sample-to-sample remains. The aperture jitter is a true error source and must be considered. The aperture jitter is a result of noise within the switching network which modulates the phase of the hold command and is manifested in the variations in the value of the analog input that has been held. The aperture error which results from this jitter is directly related to the dV/dT of the analog input.

The error due to aperture jitter is easily calculated as shown below. The error calculation takes into account the desired accuracy corresponding to the resolution of the N-bit A/D converter.

$$F_{max} = \frac{2^{-(N+1)}}{\pi\ (\text{Aperture Jitter})}$$

For an application with a 10-bit A/D converter with a 10V full scale to a 1/2LSB error maximum.

$$F_{max} = \frac{2^{-(10+1)}}{\pi\ (0.5 \times 10^{-9})}$$

$$F_{max} = 310.8\text{kHz}.$$

For an application with a 12-bit A/D converter with a 10V full scale to a 1/2LSB error maximum:

$$F_{max} = \frac{2^{-(12+1)}}{\pi\ (0.5 \times 10^{-9})}$$

$$F_{max} = 77.7\text{kHz}.$$

Figure 11 shows the entire range of errors induced by aperture jitter with respect to the input signal frequency.

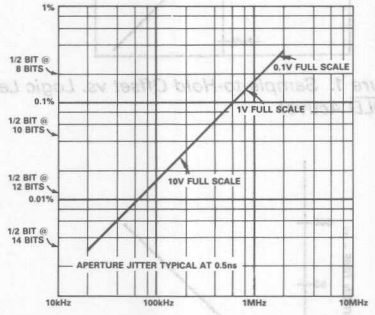


Figure 11. Aperture Jitter Error vs. Frequency

Sample-to-hold offset is caused by the transfer of charge to the holding capacitor via the gate capacitance of the switch when switching into hold. Since the gate capacitance couples the switch-control voltage applied to the gate on to the hold capacitor, the resulting sample-to-hold offset is a function of the logic level.

The logic inputs were designed for application flexibility and, therefore, a wide range of logic thresholds. This was achieved by using a differential input stage for HOLD and $\overline{\text{HOLD}}$. Figure 1 shows the change in the sample-to-hold offset voltage based upon an independently programmed reference voltage. Since the input stage is a differential configuration, the offset voltage is a function of the control voltage range around the programmed threshold voltage.

The sample-to-hold offset can be reduced by adding capacitance to the internal 100pF capacitor and by using $\overline{\text{HOLD}}$ instead of HOLD. This may be easily accomplished by adding an external capacitor between Pins 7 and 8. The sample-to-hold offset is then governed by the relationship:

$$\text{S/H Offset (V)} = \frac{\text{Charge (pC)}}{C_H\ \text{Total (pF)}}$$

For the AD585 in particular it becomes:

$$\text{S/H Offset (V)} = \frac{0.3\ \text{pC}}{100\text{pF} + (C_{EXT})}$$

The addition of an external hold capacitor also affects the acquisition time of the AD585. The change in acquisition time with respect to the C_{EXT} is shown graphically in Figure 2.

HOLD MODE

In the hold mode there are two important specifications that must be considered; feedthrough and the droop rate. Feedthrough errors appear as an attenuated version of the input at the output while in the hold mode. Hold-Mode feedthrough varies with frequency, increasing at higher frequencies. Feedthrough is an important specification when a sample and hold follows an analog multiplexer that switches among many different channels.

Hold-mode droop rate is the change in output voltage per unit of time while in the hold mode. Hold mode droop originates as leakage from the hold capacitor, of which the major leakage current contributors are switch leakage current and bias current. The rate of voltage change on the capacitor dV/dT is the ratio of the total leakage current I_L to the hold capacitance C_H.

$$\text{Droop Rate} = \frac{dV_{OUT}}{dT}\ (\text{Volts/Sec}) = \frac{I_L(\text{pA})}{C_H(\text{pF})}$$

For the AD585 in particular;

$$\text{Droop Rate} = \frac{100\text{pA}}{100\text{pF} + (C_{EXT})}$$

Additionally the leakage current doubles for every 10°C increase in temperature above 25°C; therefore, the hold-mode droop rate characteristic will also double in the same fashion. The hold-mode droop rate can be traded-off with acquisition time to provide the best combination of droop error and acquisition time. The tradeoff is easily accomplished by varying the value of C_{EXT}.

Since a sample and hold is used typically in combination with an A/D converter, then the total droop in the output voltage has to be less than 1/2LSB during the period of a conversion. The maximum allowable signal change on the input of an A/D converter is:

$$\Delta V \text{ max} = \frac{\text{Full Scale Voltage}}{2^{(N+1)}}$$

Once the maximum ΔV is determined then the conversion time of the A/D converter (T_{CONV}) is required to calculate the maximum allowable dV/dT.

$$\frac{dV \text{ max}}{dt} = \frac{\Delta V \text{ max}}{T_{CONV}}$$

The maximum $\frac{dV \text{ max}}{dT}$ as shown by the previous equation is the limit not only at 25°C but at the maximum expected operating temperature range. Therefore, over the operating temperature range the following criteria must be met ($T_{OPERATION} - 25°C$) $= \Delta T$.

$$\frac{dV\ 25°C}{dT} \times 2^{\frac{(\Delta T°C)}{10°C}} \leq \frac{dV \text{ max}}{dT}$$

NYQUIST THEOREM

The Nyquist theorem states that a band-limited signal which is sampled at a rate at least twice the maximum signal frequency can be reconstructed without loss of information. This means that a sampled data system must sample, convert and acquire the next point at a rate at least twice the signal frequency. Thus the maximum input frequency is equal to

$$f_{MAX} = \frac{1}{2(T_{ACQ} + T_{CONV} + T_{AP})}$$

Where T_{ACQ} is the acquisition time of the sample-to-hold amplifier, T_{AP} is the maximum aperture time (small enough to be ignored) and T_{CONV} is the conversion time of the A/D converter.

DATA ACQUISITION SYSTEMS

The fast acquisition time of the AD585 when used with a high speed A/D converter allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. The AD585 can be used with a number of different A/D converters to achieve high throughput rates. Figures 12 and 13 show the use of an AD585 with the AD578 and AD574A.

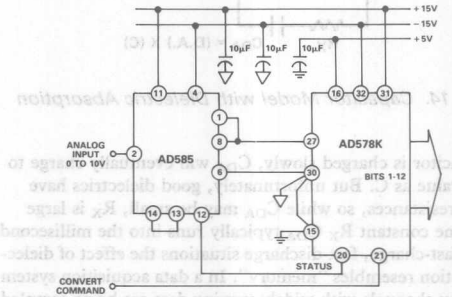


Figure 12. A/D Conversion System, 117.6kHz Throughput 58.8kHz max Signal Input

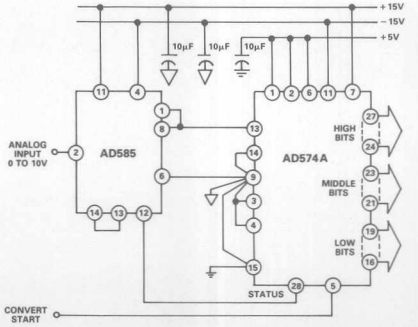


Figure 13. 12 Bit A/D Conversion System, 26.3kHz Throughput Rate, 13.1kHz max Signal Input

LOGIC INPUT

The sample-and-hold logic control was designed for versatile logic interfacing. The HOLD and $\overline{\text{HOLD}}$ inputs may be used with both low and high level CMOS, TTL and ECL logic systems. Logic threshold programmability was achieved by using a differential amplifier as the input stage for the digital inputs. A predictable logic threshold may be programmed by referencing either HOLD or $\overline{\text{HOLD}}$ to the appropriate threshold voltage. For example, if the internal 1.4V reference is applied to $\overline{\text{HOLD}}$ an input signal to HOLD between +1.8V and $+V_S$ will place the AD585 in the hold mode. The AD585 will go into the sample mode for this case when the input is between $-V_S$ and +1.0V. The range of references which may be applied is from ($-V_S$ +4V) to ($+V_S$ −3V).

OPTIONAL CAPACITOR SELECTION

If an additional capacitor is going to be used in conjunction with the internal 100pF capacitor it must have a low dielectric absorption. Dielectric absorption is just that; it is the charge absorbed into the dielectric that is not immediately added to or removed from the capacitor when rapidly charged or discharged. The capacitor with dielectric absorption is modeled in Figure 14.

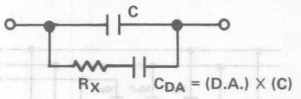


Figure 14. Capacitor Model with Dielectric Absorption

If the capacitor is charged slowly, C_{DA} will eventually charge to the same value as C. But unfortunately, good dielectrics have very high resistances, so while C_{DA} may be small, R_X is large and the time constant R_X C_{DA} typically runs into the millisecond range. In fast-charge, fast-discharge situations the effect of dielectric absorption resembles "memory". In a data acquisition system where many channels with widely varying data are being sampled the effect is to have an ever changing offset which appears as a very nonlinear sample-to-hold offset since the difference between the voltage being measured and the voltage previously measured determines the fraction by which the dielectric absorption figure is multiplied. It is impossible to readily correct for this error source. The only solution is to use a capacitor with dielectric absorption less than the maximum tolerable error. Capacitor types such as polystyrene, polypropylene or Teflon are recommended.

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD585. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

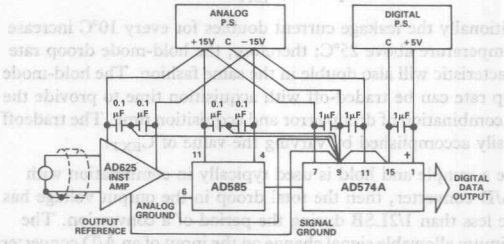


Figure 15. Basic Grounding Practice

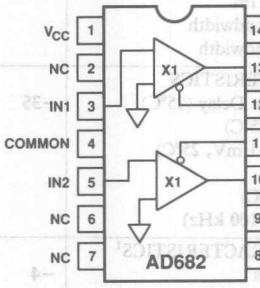
Two-Channel 700 ns Sample-and-Hold Amplifier

AD682*

FEATURES

- Two Matched Sample-and-Hold Amplifiers
- Fully Specified and Tested Hold Mode Distortion
- Acquisition Time to 0.01%: 700 ns Maximum
- Independent Inputs, Outputs and Control Pins
- Low Power Dissipation: 190 mW
- Low Droop Rate: 0.01 μV/μs
- Total Harmonic Distortion: −80 dB Maximum
- Aperture Jitter: 75 ps Maximum
- Internal Hold Capacitors
- Self-Correcting Architecture
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



NC = NO CONNECT

4

PRODUCT DESCRIPTION

The AD682 is a two-channel high speed monolithic sample-and-hold amplifier (SHA). The AD682 guarantees a maximum acquisition time of 700 ns to 0.01% over temperature. Interchannel characteristics are fully specified and tested. The AD682 is also specified and tested for hold mode total harmonic distortion and hold mode signal-to-noise and distortion. The AD682 is configured as two independent unity gain amplifiers. The AD682 uses a self-correcting architecture that minimizes hold mode errors and insures accuracy over temperature. The AD682 is self-contained and requires no external components or adjustments.

The AD682 is ideal for systems demanding interchannel and hold mode characteristic requirements, such as in data acquisition systems and in-phase (I) and quadrature (Q) modulated systems. The independent inputs, outputs and controls allow maximum user configuration flexibility. The AD682 is ideal for 12- and 14-bit high speed analog-to-digital converters.

The AD682 is manufactured on a BiMOS process which merges high performance bipolar circuitry with low power CMOS to provide an accurate, high speed, low power SHA.

The AD682 is specified for three temperature ranges. The J grade device is specified for operation from 0°C to 70°C, the A grade from −40°C to +85°C and the S grade from −55°C to +125°C. The J and A grades are available in 14-pin plastic DIPs. The S grade is available in a 14-pin cerdip package.

PRODUCT HIGHLIGHTS

1. Fast acquisition time (700 ns) and low aperture jitter (75 ps) make the AD682 the best choice for multiple channel data acquisition systems.
2. Monolithic construction insures excellent interchannel matching, while testing guarantees the fully specified performance.
3. Independent inputs, outputs and sample-and-hold controls allow user flexibility.
4. Low droop (0.01 μV/μs) and internally compensated hold mode error results in superior system accuracy.
5. Fully specified and tested hold mode distortion and signal-to-noise and distortion guarantees the AD682's performance in sampled data systems.
6. The AD682's fast settling time and low output impedance make it ideal for driving high speed analog-to-digital converters such as the AD578, AD674B, AD774B, AD7572 and the AD7672.
7. The AD682 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD682/883B data sheet for detailed specifications.

*Protected by Patent Number 4,962,325.

AD682—SPECIFICATIONS

DC SPECIFICATIONS (T_{min} to T_{max} with V_{CC} = +12 V ± 10%, V_{EE} = −12 V ± 10%, C_L = 20 pF, unless otherwise specified)

Parameter	AD682J Min	AD682J Typ	AD682J Max	AD682A Min	AD682A Typ	AD682A Max	AD682S Min	AD682S Typ	AD682S Max	Units
SAMPLING CHARACTERISTICS										
Acquisition Time										
10 V Step to 0.01%		600	700		600	700		600	700	ns
10 V Step to 0.1%		500	600		500	600		500	600	ns
Small Signal Bandwidth		4			4			4		MHz
Full Power Bandwidth		1			1			1		MHz
HOLD CHARACTERISTICS										
Effective Aperture Delay (25°C)	−35	−25	−15	−35	−25	−15	−35	−25	−15	ns
Aperture Jitter (25°C)		50	75		50	75		50	75	ps
Hold Settling (to 1 mV, 25°C)		250	500		250	500		250	500	ns
Droop Rate		0.01	1		0.01	1		0.01	1	μV/μs
Feedthrough (25°C)										
(V_{IN} = ±5 V, 100 kHz)		−90			−90			−90		dB
ACCURACY CHARACTERISTICS[1]										
Hold Mode Offset	−4	−1	+3	−4	−1	+3	−4	−1	+3	mV
Hold Mode Offset Drift		10			10			10		μV/°C
Sample Mode Offset		50	200		50	200		50	200	mV
Nonlinearity		±0.002	±0.003		±0.002	±0.003		±0.003	±0.005	% FS
Gain Error		±0.03	±0.05		±0.03	±0.05		±0.03	±0.05	% FS
OUTPUT CHARACTERISTICS										
Output Drive Current	−5		+5	−5		+5	−5		+5	mA
Output Resistance, DC		0.3	0.5		0.3	0.5		0.3	0.5	Ω
Total Output Noise (DC to 5 MHz)		150			150			150		μV rms
Sampled DC Uncertainty		85			85			85		μV rms
Hold Mode Noise (DC to 5 MHz)		125			125			125		μV rms
Short Circuit Current										
Source		20			20			20		mA
Sink		10			10			10		mA
INPUT CHARACTERISTICS										
Input Voltage Range	−5		+5	−5		+5	−5		+5	V
Bias Current		100	250		100	250		100	250	nA
Input Impedance		50			50			50		MΩ
Input Capacitance		2			2			2		pF
DIGITAL CHARACTERISTICS										
Input Voltage Low			0.8			0.8			0.8	V
Input Voltage High	2.0			2.0			2.0			V
Input Current High (V_{IN} = 5 V)		2	10		2	10		2	10	μA
POWER SUPPLY CHARACTERISTICS										
Operating Voltage Range	±10.8	±12	±13.2	±10.8	±12	±13.2	±10.8	±12	±13.2	V
Supply Current		8	12.5		8	12.5		8	13	mA
+PSRR (+12 V ± 10%)	70	80		70	80		70	80		dB
−PSRR (−12 V ± 10%)	65	75		65	75		65	75		dB
Power Consumption		190	300		190	300		190	320	mW
TEMPERATURE RANGE										
Specified Performance	0		+70	−40		+85	−55		+125	°C

NOTE
[1]Specified and tested over an input range of ±5 V.
Specifications subject to change without notice.

INTERCHANNEL SPECIFICATIONS unless otherwise specified)

Parameter	AD682J Min	AD682J Typ	AD682J Max	AD682A Min	AD682A Typ	AD682A Max	AD682S Min	AD682S Typ	AD682S Max	Units
INTERCHANNEL ISOLATION (V_{IN} = ±5 V, 100 kHz)	90	96		90	96		90	96		dB
INTERCHANNEL APERTURE OFFSET		150	300		150	300		150	300	ps
INTERCHANNEL OFFSET		0.1	1.5		0.1	1.5		0.1	1.5	mV

HOLD MODE AC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ±10%, V_{EE} = −12 V ±10%, C_L = 20 pF, unless otherwise specified)[1]

Parameter	AD682J Min	AD682J Typ	AD682J Max	AD682A Min	AD682A Typ	AD682A Max	AD682S Min	AD682S Typ	AD682S Max	Units
TOTAL HARMONIC DISTORTION										
F_{IN} = 10 kHz		−90	−80		−90	−80		−90	−80	dB
F_{IN} = 50 kHz		−73			−73			−73		dB
F_{IN} = 100 kHz		−68			−68			−68		dB
SIGNAL-TO-NOISE AND DISTORTION										
F_{IN} = 10 kHz	72	78		72	78		72	78		dB
F_{IN} = 50 kHz		73			73			73		dB
F_{IN} = 100 kHz		67			67			67		dB
INTERMODULATION DISTORTION										
F_{IN1} = 49 kHz, F_{IN2} = 50 kHz										
2nd Order Products		−77			−77			−77		dB
3rd Order Products		−78			−78			−78		dB

NOTE
[1]F_{IN} amplitude = 0 dB and F_{SAMPLE} = 500 kHz unless otherwise indicated.

Specifications shown in **boldface** are tested on all devices at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed although only those shown in **boldface** are tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Spec	With Respect to	Min	Max	Unit
V_{CC}	Common	−0.3	+15	V
V_{EE}	Common	−15	+0.3	V
Control Inputs	Common	−0.5	+7	V
Analog Inputs	Common	−12	+12	V
Output Short Circuit to Ground, V_{CC}, or V_{EE}		Indefinite		
Maximum Junction Temperature			+175	°C
Storage		−65	+150	°C
Lead Temperature (10 sec max)			+300	°C
Power Dissipation			340	mW

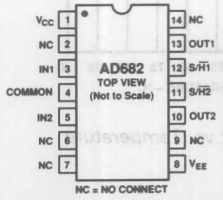
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
AD682JN	0°C to +70°C	14-Pin Plastic DIP	N-14
AD682AN	−40°C to +85°C	14-Pin Plastic DIP	N-14
AD682SQ	−55°C to +125°C	14-Pin Cerdip	Q-14

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD682/883B data sheet.
[2]N = Plastic DIP; Q = Cerdip. For outline information see Package Information section.

PIN CONFIGURATION

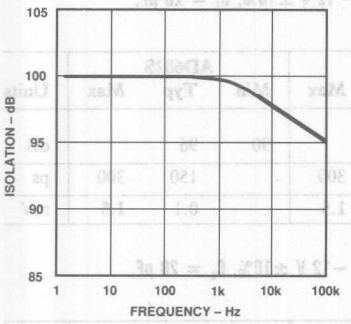


CAUTION

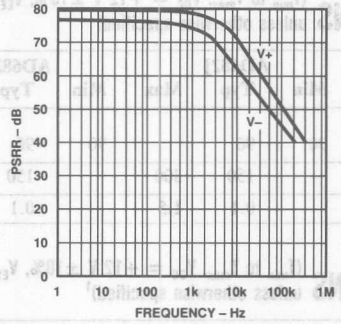
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.



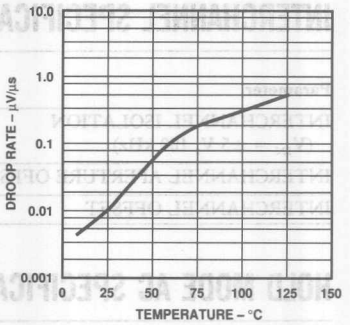
AD682—Typical Characteristics



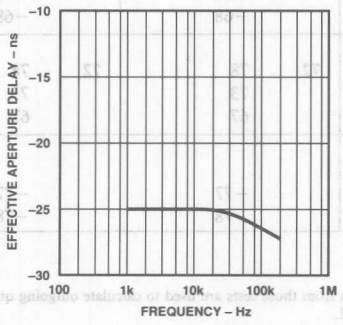
Interchannel Isolation vs. Frequency



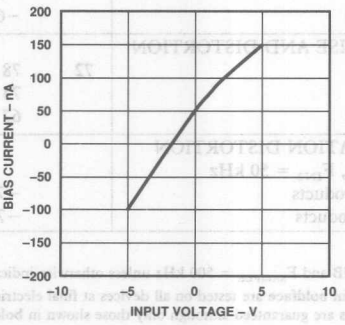
Power Supply Rejection Ratio vs. Frequency



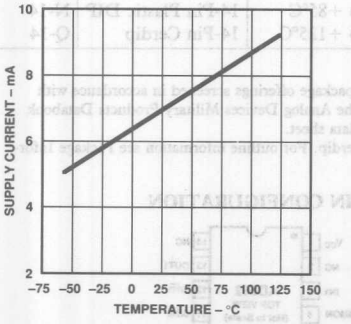
Droop Rate vs. Temperature, V_{IN} = 0 V



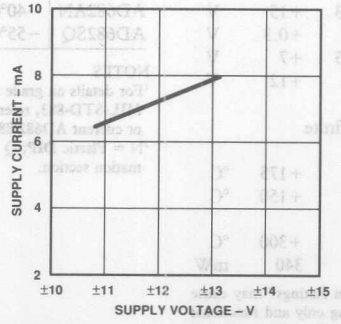
Effective Aperture Delay vs. Frequency



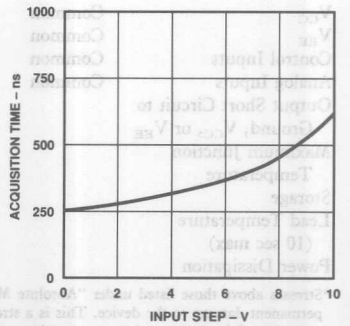
Bias Current vs. Input Voltage



Supply Current vs. Temperature



Supply Current vs. Supply Voltage



Acquisition Time (to 0.01%) vs. Input Step Size

DEFINITIONS OF SPECIFICATIONS

Acquisition Time – The length of time that the SHA must remain in the sample mode in order to acquire a full scale input step to a given level of accuracy.

Small Signal Bandwidth – The frequency at which the held output amplitude is 3 dB below the input amplitude, under an input condition of a 100 mV p–p sine wave.

Full Power Bandwidth – The frequency at which the held output amplitude is 3 dB below the input amplitude, under an input condition of a 10 V p–p sine wave.

Effective Aperture Delay – The difference between the switch delay and the analog delay of the SHA channel. A negative number indicates that the analog portion of the overall delay is greater than the switch portion. This effective delay represents the point in time, relative to the hold command, that the input signal will be sampled.

Aperture Jitter – The variations in delay for successive samples. Aperture jitter puts an upper limit on the maximum frequency that can be accurately sampled.

Hold Settling Time – The time required for the output to settle to within a specified level of accuracy of its final held value after the hold command has been given.

Droop Rate – The drift in output voltage while in the hold mode.

Feedthrough – The attenuated version of a changing input signal that appears at the output when the SHA is in the hold mode.

Hold Mode Offset – The difference between the input signal and the held output. This offset term applies only in the hold mode and includes the error caused by charge injection and all other internal offsets. It is specified for an input of 0 V.

Tracking Mode Offset – The difference between the input and output signals when the SHA is in the track mode.

Nonlinearity – The deviation from a straight line on a plot of input vs. (held) output as referenced to a straight line drawn between end points, over an input range of –5 V and +5 V.

Gain Error – Deviation from a gain of +1 on the transfer function of input vs. held output.

Interchannel Isolation – The level of crosstalk between adjacent channels while in the sample (track) mode with a full-scale 100 kHz input signal.

Interchannel Aperture Offset – The variation in aperture time between the two channels for a simultaneous hold command.

Interchannel Offset – The difference in hold mode offset between the two SHA channels.

Power Supply Rejection Ratio – A measure of change in the held output voltage for a specified change in the positive or negative supply.

Sampled DC Uncertainty – The internal rms SHA noise that is sampled onto the hold capacitor.

Hold Mode Noise – The rms noise at the output of the SHA while in the hold mode, specified over a given bandwidth.

Total Output Noise – The total rms noise that is seen at the output of the SHA while in the hold mode. It is the rms summation of the sampled dc uncertainty and the hold mode noise.

Output Drive Current – The maximum current the SHA can source (or sink) while maintaining a change in hold mode offset of less than 2.5 mV.

Signal-to-Noise and Distortion (S/N+D) Ratio – S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

Total Harmonic Distortion (THD) – THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal.

Intermodulation Distortion (IMD) – With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequency of mfa±nfb, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa+fb) and (fa−fb), and the third order terms are (2fa+fb), (2fa−fb), (fa+2fb) and (fa−2fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals are of equal amplitude, and peak value of their sums is −0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

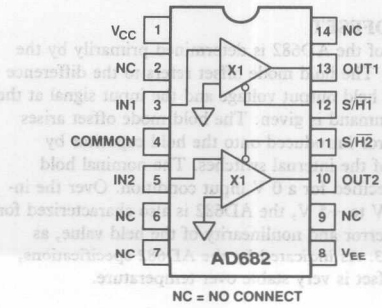
FUNCTIONAL DESCRIPTION

The AD682 is a complete dual sample-and-hold amplifier that provides high speed sampling to 12-bit accuracy in less than 700 ns.

The AD682 is completely self-contained, including on-chip hold capacitors, and requires no external components or adjustments to perform the sampling function. Each SHA channel can operate independently, having its own input, output and sample/hold command. Both inputs and outputs are treated as single-ended signals, referred to common.

The AD682 utilizes a proprietary circuit design which includes a self-correcting architecture. This sample-and-hold circuit corrects for internal errors after the hold command has been given, by compensating for amplifier gain and offset errors, and charge injection errors. Due to the nature of the design, the SHA output in the sample mode is not intended to provide an accurate representation of the input. However, in hold mode, the internal circuitry is reconfigured to produce an accurately held version of the input signal. Below is a block diagram of the AD682.

FUNCTIONAL BLOCK DIAGRAM



NC = NO CONNECT

DYNAMIC PERFORMANCE

The AD682 is compatible with 12-bit A-to-D converters in terms of both accuracy and speed. The fast acquisition time, fast hold settling time and good output drive capability allow the AD682 to be used with high speed, high resolution A-to-D converters like the AD674B, AD774B and AD7672. The AD682's fast acquisition time provides high throughput rates for multichannel data acquisition systems. Typically, the sample and hold can acquire a 10 V step in less than 600 ns. Figure 1 shows the settling accuracy as a function of acquisition time.

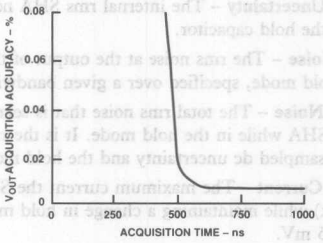


Figure 1. V_{OUT} Settling vs. Acquisition Time

The hold settling determines the required time, after the hold command is given, for the output to settle to its final specified accuracy. The typical settling behavior of the AD682 is shown in Figure 2. The settling time of the AD682 is sufficiently fast to allow the SHA, in most cases, to directly drive an A-to-D converter without the need for an added "start convert" delay.

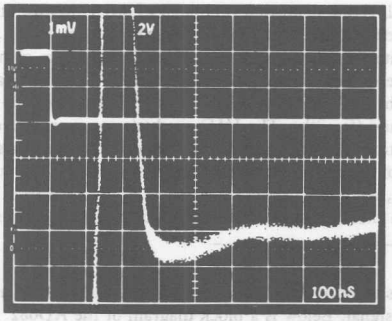


Figure 2. Typical AD682 Hold Mode

HOLD MODE OFFSET

The dc accuracy of the AD682 is determined primarily by the hold mode offset. The hold mode offset refers to the difference between the final held output voltage and the input signal at the time the hold command is given. The hold mode offset arises from a voltage error introduced onto the hold capacitor by charge injection of the internal switches. The nominal hold mode offset is specified for a 0 V input condition. Over the input range of −5 V to +5 V, the AD682 is also characterized for an effective gain error and nonlinearity of the held value, as shown in Figure 3. As indicated by the AD682 specifications, the hold mode offset is very stable over temperature.

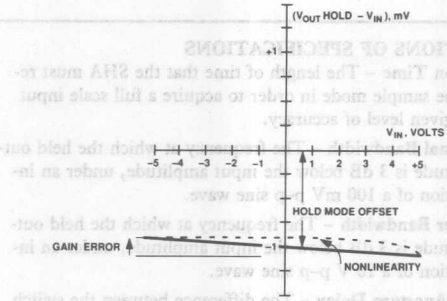


Figure 3. Hold Mode Offset, Gain Error and Nonlinearity

For applications where it is important to obtain zero offset, the hold mode offset may be nulled externally at the input to the A-to-D converter. Adjustment of the offset may be accomplished through the A-to-D itself or by an external amplifier with offset nulling capability (e.g., AD711). The offset will change less than 0.5 mV over the specified temperature range.

SUPPLY DECOUPLING AND GROUNDING CONSIDERATIONS

As with any high speed, high resolution data acquisition system, the power supplies should be well regulated and free from excessive high frequency noise (ripple). The supply connection to the AD682 should also be capable of delivering transient currents to the device. To achieve the specified accuracy and dynamic performance, decoupling capacitors must be placed directly at both the positive and negative supply pins to common. Ceramic type 0.1 μF capacitors should be connected from V_{CC} and V_{EE} to common.

The AD682 does not provide separate analog and digital ground leads as is the case with most A-to-D converters. The common pin is the single ground terminal for the device. It is the reference point for the sampled input voltage and the held output voltage and also the digital ground return path. The common pin should be connected to the reference (analog) ground of the A-to-D converter with a separate ground lead. Since the analog and digital grounds in the AD682 are connected internally, the common pin should also be connected to the digital ground, which is usually tied to analog common at the A-to-D converter. Figure 4 illustrates the recommended decoupling and grounding practice.

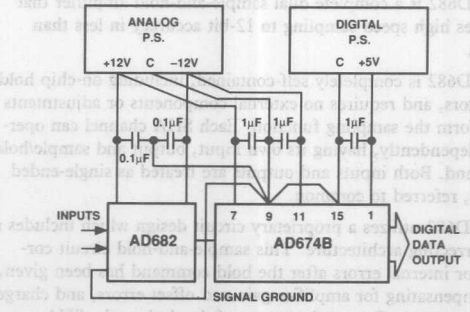


Figure 4. Basic Grounding and Decoupling Diagram

NOISE CHARACTERISTICS

Designers of data conversion circuits must also consider the effect of noise sources on the accuracy of the data acquisition system. A sample-and-hold amplifier that precedes the A-to-D converter introduces some noise and represents another source of uncertainty in the conversion process. The noise from the AD682 is specified as the total output noise, which includes both the sampled wideband noise of the SHA in addition to the band limited output noise. The total output noise is the rms sum of the sampled dc uncertainty and the hold mode noise. A plot of the total output noise vs. the equivalent input bandwidth of the converter being used is given in Figure 5.

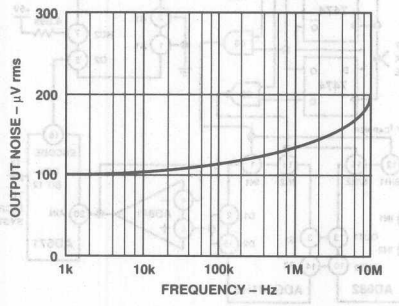


Figure 5. RMS Noise vs. Input Bandwidth of ADC

DRIVING THE ANALOG INPUTS

For best performance, it is important to drive the AD682 analog input from a low impedance signal source. This enhances the sampling accuracy by minimizing the analog and digital crosstalk. Signals which come from higher impedance sources (e.g., over 5 kΩ) will have a relatively higher level of crosstalk. For applications where signals have high source impedance, an operational amplifier buffer in front of the AD682 is required. The AD712 (precision BiFET op amp) is recommended for these applications.

HIGH FREQUENCY SAMPLING

Aperture jitter and distortion are the primary factors which limit frequency domain performance of a sample-and-hold amplifier. Aperture jitter modulates the phase of the hold command and produces an effective noise on the sampled analog input. The magnitude of the jitter induced noise is directly related to the frequency of the input signal.

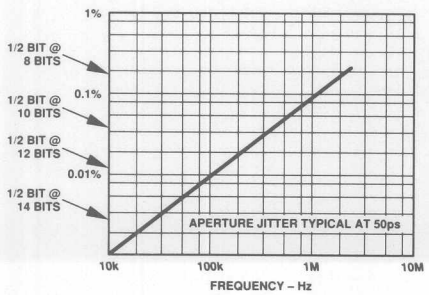


Figure 6. Error Magnitude vs. Frequency

A graph showing the magnitude of the jitter induced error vs. frequency of the input signal is given in Figure 6.

The accuracy in sampling high frequency signals is also constrained by the distortion and noise created by the sample-and-hold. The level of distortion increases with frequency and reduces the "effective number of bits" of the conversion.

Measurements of Figures 7 and 8 were made using a 14-bit A-to-D converter with V_{IN} = 10 V p–p and a sample frequency of 100 kSPS.

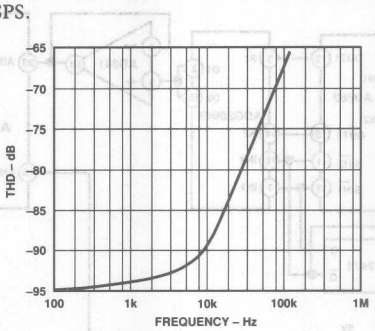


Figure 7. Total Harmonic Distortion vs. Frequency

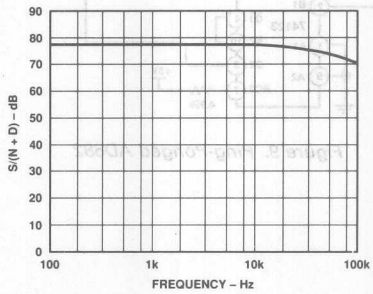


Figure 8. Signal/(Noise and Distortion) vs. Frequency

THE AD682 IN A PING-PONG ARRANGEMENT

In a ping-pong arrangement two sample-and-hold amplifiers are connected to the same analog input source. While one channel is sampling the analog input, the other is in the hold mode. Depending upon the ADC conversion time, a ping-pong circuit can increase data throughput rates by as much as 100%. The AD682's excellent interchannel aperture delay, gain and offset errors make it ideal to use in a ping-pong arrangement.

Figure 9 shows the AD682 in a ping-pong arrangement with the AD671 12-bit, 500 ns A/D converter. A high speed switch (ADG201HS) directs the appropriate AD682 output to the AD671. In this system the data throughput rate is increased by up to 80% as compared to a system using only one channel of the AD682.

THE AD682 FOR IN-PHASE (I) AND QUADRATURE (Q) DEMODULATION

The AD682 can be used to demodulate digital data that has been I and Q modulated. Using two SHAs for the signal acqui-

sition allows the use of slower and lower cost SHAs and A/D converters as compared to a system using one SHA.

Figure 10 shows the AD682 being used as a I and Q demodulator. If the carrier frequency is represented by f and w = 2 πf, the incoming signal can be represented by s(t) = I(n) × cos(wt) + Q(n) × sin(wt), where I(n) and Q(n) (the nth I– Q pair sent) only take on discrete values and must stay constant for at least one carrier period (2 π/w).

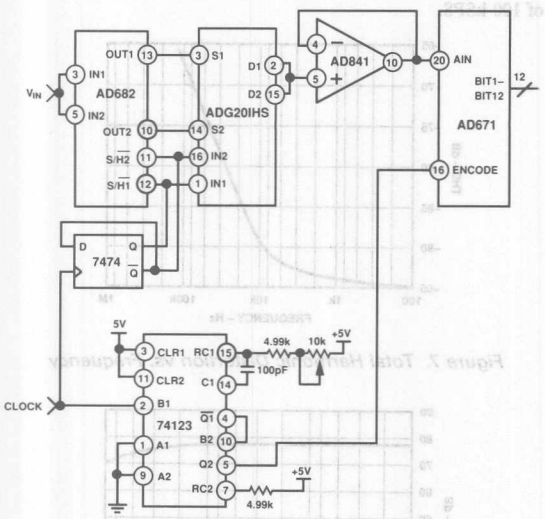


Figure 9. Ping-Ponged AD682

The clock source from which the AD682's control signals are derived must be coherent with the input signal carrier. To recover I(n), s(t) must be sampled when the in-phase carrier component is 1 and the quadrature component is 0 (when t is integer multiples of 2 π/W). Similarly to recover Q(n) s(t) must be sampled when the in-phase carrier component is 0 and the quadrature component is 1 (when t is integer multiples of 2 π/w + π/2).

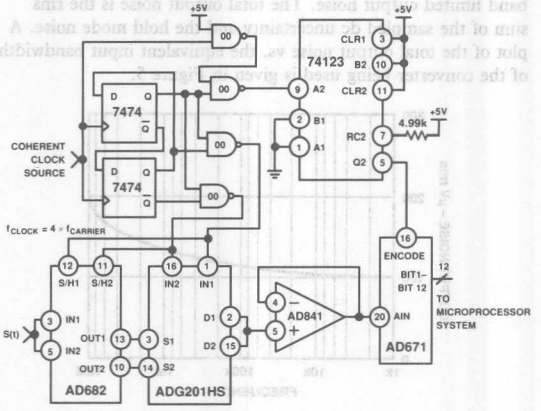


Figure 10. The AD682 Used for I and Q Demodulation

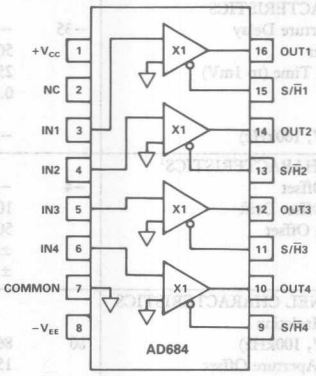
Four-Channel Sample-and-Hold Amplifier

AD684*

FEATURES

Four Matched Sample-and-Hold Amplifiers
Independent Inputs, Outputs and Control Pins
500ns Hold Mode Settling
1μs Maximum Acquisition Time to 0.01%
Low Droop Rate: 0.01μV/μs
Internal Hold Capacitors
75ps Maximum Aperture Jitter
Low Power Dissipation: 430mW
0.3″ Skinny DIP Package
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD684 is a monolithic quad sample-and-hold amplifier (SHA). It features four complete sampling channels, each controlled by an independent hold command. Each SHA is complete with an internal hold capacitor. The high accuracy SHA channels are self-contained and require no external components or adjustments. The AD684 is manufactured on a BiMOS process which provides a merger of high performance bipolar circuitry and low power CMOS logic.

The AD684 is ideal for high performance, multichannel data acquisition systems. Each SHA channel can acquire a signal in less than 1μs and retain the held value with a droop rate of less than 0.01μV/μs. Excellent linearity and ac performance make the AD684 an ideal front end for high speed 12- and 14-bit ADCs.

The AD684 has a self-correcting architecture that minimizes hold mode errors and insures accuracy over temperature. Each channel of the AD684 is capable of sourcing 5mA and incorporates output short circuit protection.

The AD684 is specified for three temperature ranges. The J grade device is specified for operation from 0 to 70°C, the A grade from −40°C to +85°C and the S grade from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Fast acquisition time (1μs) and low aperture jitter (75ps) make the AD684 the best choice for multiple channel data acquisition systems.
2. Monolithic construction insures excellent interchannel matching in terms of timing and accuracy, as well as high reliability.
3. Independent inputs, outputs and sample-and-hold controls allow user flexibility in system architecture.
4. Low droop (0.01μV/μs) and internally compensated hold mode error results in superior system accuracy.
5. The AD684's fast settling time and low output impedance make it ideal for driving high speed analog to digital converters such as the AD578, AD674, AD7572 and the AD7672.
6. The AD684 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current AD684/883B data sheet for detailed specifications.

***Protected by U.S. Patent Number 4,962,325.**

Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
SAMPLING CHARACTERISTICS										
Acquisition Time										
10V Step to 0.01%		0.75	1.0		0.75	1.0		0.75	1.0	µs
10V Step to 0.1%		0.5	0.6		0.5	0.6		0.5	0.6	µs
Small Signal Bandwidth		4			4			4		MHz
Full Power Bandwidth		1			1			1		MHz
HOLD CHARACTERISTICS										
Effective Aperture Delay	−35	−25	−15	−35	−25	−15	−35	−25	−15	ns
Aperture Jitter		50	75		50	75		50	75	ps
Hold Settling Time (to 1mV)		250	500		250	500		250	500	ns
Droop Rate[1]		0.01	**1**		0.01	**1**		0.01	**1**	µV/µs
Feedthrough										
(V_{IN} = ±5V, 100kHz)		−90			−90			−90		dB
ACCURACY CHARACTERISTICS[1]										
Hold Mode Offset	**−4**	−1	**+3**	**−4**	−1	**+3**	**−4**	−1	**+3**	mV
Hold Mode Offset Drift		10			10			10		µV/°C
Sample Mode Offset		50	**200**		50	**200**		50	**200**	mV
Nonlinearity		±0.002	±0.003		±0.002	±0.003		±0.003	±0.005	% FS
Gain Error		±0.03	**±0.05**		±0.03	**±0.05**		±0.03	**±0.05**	% FS
INTERCHANNEL CHARACTERISTICS										
Interchannel Isolation										
(V_{IN} = ±5V, 100kHz)	80	86		80	86		80	86		dB
Interchannel Aperture Offset		150	300		150	300		150	300	ps
Interchannel Offset		0.4	**1.5**		0.4	**2.0**		0.4	**2.0**	mV
OUTPUT CHARACTERISTICS										
Output Drive Current[2]	**−5**		**+5**	**−5**		**+5**	**−5**		**+5**	mA
Output Resistance, dc		0.3	0.5		0.3	0.5		0.3	0.5	Ω
Total Output Noise										
(dc to 5MHz)		150			150			150		µV rms
Sampled dc Uncertainty		85			85			85		µV rms
Hold Mode Noise										
(dc to 5MHz)		125			125			125		µV rms
Short Circuit Current[3]										
Source		20			20			20		mA
Sink		10			10			10		mA
INPUT CHARACTERISTICS										
Input Voltage Range	−5		+5	−5		+5	−5		+5	V
Bias Current[4]		100	**250**		100	**250**		100	**250**	nA
			400			500			500	nA
Input Impedance		50			50			50		MΩ
Input Capacitance		2			2			2		pF
DIGITAL CHARACTERISTICS										
Input Voltage Low			**0.8**			**0.8**			**0.8**	V
Input Voltage High	**2.0**			**2.0**			**2.0**			V
Input Current (V_{IN} = 5V)		2	**10**		2	**10**		2	**10**	µA
POWER SUPPLY CHARACTERISTICS										
Operating Voltage Range (V_{CC}, V_{EE})	±10.8	±12	±13.2	±10.8	±12	±13.2	±10.8	±12	±13.2	V
Supply Current		18	**25**		18	**25**		18	**26**	mA
+ PSRR	**65**	70		**65**	70		**65**	70		dB
−PSRR	**60**	65		**60**	65		**60**	65		dB
Power Consumption		430	600		430	600		430	625	mW
TEMPERATURE RANGE										
Specified Performance	0		+70	−40		+85	−55		+125	°C
PACKAGE OPTIONS										
16-Pin Cerdip (Q)		AD684JQ			AD684AQ			AD684SQ		

NOTES

[1]Specified and tested over an input range of ±5V.

[2]Maximum current the AD684 can source (or sink). Testing guarantees that the accuracy of the held signal remains within 2.5mV of its initial value.

[3]The output is protected for a short circuit to common, V_{CC} and V_{EE}.

[4]V_{CC} and V_{EE} at nominal voltage levels.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

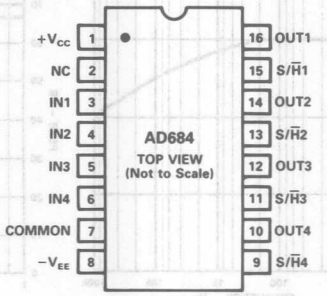
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Spec	With Respect to	Min	Max	Unit
V_{CC}	Common	−0.3	+15	V
V_{EE}	Common	−15	+0.3	V
Control Inputs	Common	−0.5	+7	V
Analog Inputs	Common	−12	+12	V
Output Short Circuit to Ground, V_{CC}, or V_{EE}		Indefinite		
Max Junction Temperature			+175	°C
Storage		−65	+150	°C
Lead Temperature (10sec max)			+300	°C
Power Dissipation			640	mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

PIN CONFIGURATION



NC = NO CONNECT

4

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.

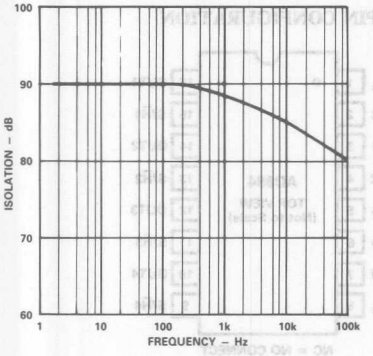


ORDERING GUIDE

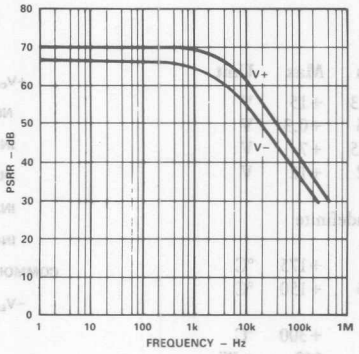
Model[1]	Temperature Range	Package Option[2]
AD684JQ	0 to +70°C	Q-16
AD684AQ	−40°C to +85°C	Q-16
AD684SQ	−55°C to +125°C	Q-16

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD684/883B data sheet.
[2]Q = Cerdip. For outline information see Package Information section.

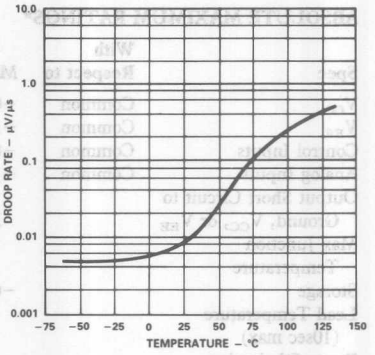
AD684 — Typical Characteristics



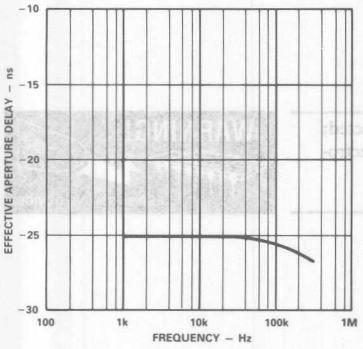
Interchannel Isolation vs. Frequency



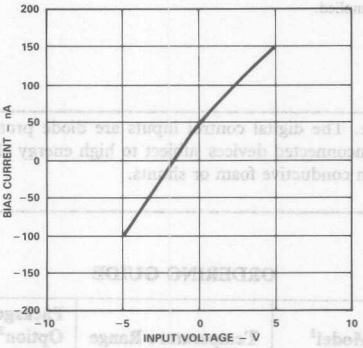
Power Supply Rejection Ratio vs. Frequency



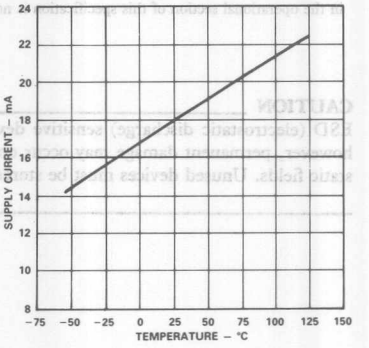
Droop Rate vs. Temperature, V_{IN} = 0V



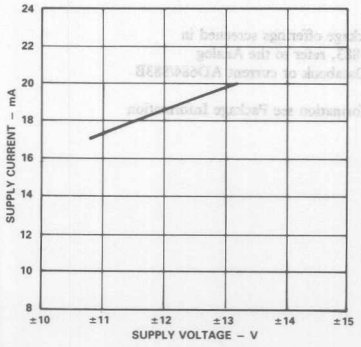
Effective Aperture Delay vs. Frequency



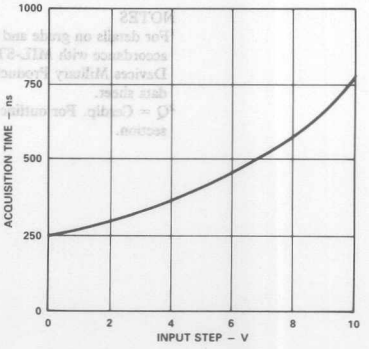
Bias Current vs. Input Voltage



Supply Current vs. Temperature



Supply Current vs. Supply Voltage



Acquisition Time (to 0.01%) vs. Input Step Size

DEFINITIONS OF SPECIFICATIONS

Acquisition Time — The length of time that the SHA must remain in the sample mode in order to acquire a full scale input step to a given level of accuracy.

Small Signal Bandwidth — The frequency at which the held output amplitude is 3dB below the input amplitude, under an input condition of a 100mV p-p sine wave.

Full Power Bandwidth — The frequency at which the held output amplitude is 3dB below the input amplitude, under an input condition of a 10V p-p sine wave.

Effective Aperture Delay — The difference between the switch delay and the analog delay of the SHA channel. A negative number indicates that the analog portion of the overall delay is greater than the switch portion. This effective delay represents the point in time, relative to the hold command, that the input signal will be sampled.

Aperture Jitter — The variations in aperture delay for successive samples. Aperture jitter puts an upper limit on the maximum frequency that can be accurately sampled.

Hold Settling Time — The time required for the output to settle to within a specified level of accuracy of its final held value after the hold command has been given.

Droop Rate — The drift in output voltage while in the hold mode.

Feedthrough — The attenuated version of a changing input signal that appears at the output when the SHA is in the hold mode.

Hold Mode Offset — The difference between the input signal and the held output. This offset term applies only in the hold mode and includes the error caused by charge injection and all other internal offsets. It is specified for an input of 0V.

Tracking Mode Offset — The difference between the input and output signals when the SHA is in the track mode.

Nonlinearity — The deviation from a straight line on a plot of input vs. (held) output as referenced to a straight line drawn between endpoints, over an input range of −5V and +5V.

Gain Error — Deviation from a gain of +1 on the transfer function of input vs. held output.

Interchannel Isolation — The level of crosstalk between adjacent channels while in the sample (track) mode with a full scale 100kHz input signal.

Interchannel Aperture Offset — The variation in aperture time between the four channels for a simultaneous hold command.

Differential Offset — The difference in hold mode offset between the four SHA channels.

Power Supply Rejection Ratio — A measure of change in the held output voltage for a specified change in the positive or negative supply.

Sampled dc Uncertainty — The internal rms SHA noise that is sampled onto the hold capacitor.

Hold Mode Noise — The rms noise at the output of the SHA while in the hold mode, specified over a given bandwidth.

Total Output Noise — The total rms noise that is seen at the output of the SHA while in the hold mode. It is the rms summation of the sampled dc uncertainty and the hold mode noise.

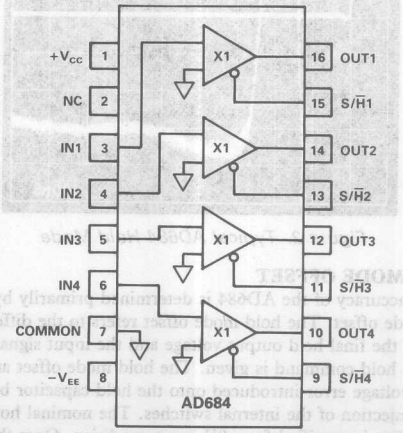
Output Drive Current — The maximum current the SHA can source (or sink) while maintaining a change in hold mode offset of less than 2.5mV.

FUNCTIONAL DESCRIPTION

The AD684 is a complete quad sample-and hold amplifier that provides high speed sampling to 12-bit accuracy in less than 1μs.

The AD684 is completely self-contained, including on-chip hold capacitors, and requires no external components or adjustments to perform the sampling function. Each SHA channel can operate independently, having its own input, output and sample/hold command. Both inputs and outputs are treated as single ended signals, referred to common.

The AD684 utilizes a proprietary circuit design which includes a self-correcting architecture. This sample-and-hold circuit corrects for internal errors after the hold command has been given, by compensating for amplifier gain and offset errors, and charge injection errors. Due to the nature of the design, the SHA output in the sample mode is not intended to provide an accurate representation of the input. However, in hold mode, the internal circuitry is reconfigured to produce an accurately held version of the input signal. To the right is a block diagram of the AD684.



Functional Block Diagram

DYNAMIC PERFORMANCE

The AD684 is compatible with 12-bit A-to-D converters in terms of both accuracy and speed. The fast acquisition time, fast hold settling time and good output drive capability allow the AD684 to be used with high speed, high resolution A-to-D converters like the AD674 and AD7672. The AD684's fast acquisition time provides high throughput rates for multichannel data acquisition systems. Typically, the sample and hold can acquire a 10V step in less than 750ns. Figure 1 shows the settling accuracy as a function of acquisition time.

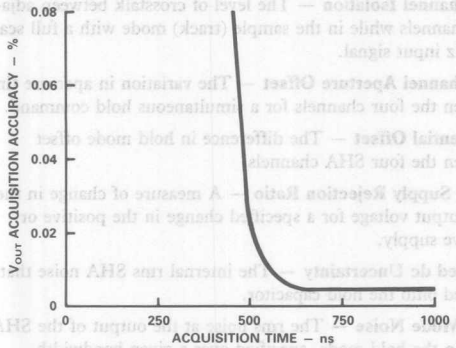


Figure 1. V_{OUT} Settling vs. Acquisition Time

The hold settling determines the required time, after the hold command is given, for the output to settle to its final specified accuracy. The typical settling behavior of the AD684 is shown in Figure 2. The settling time of the AD684 is sufficiently fast to allow the SHA, in most cases, to directly drive an A-to-D converter without the need for an added "start convert" delay.

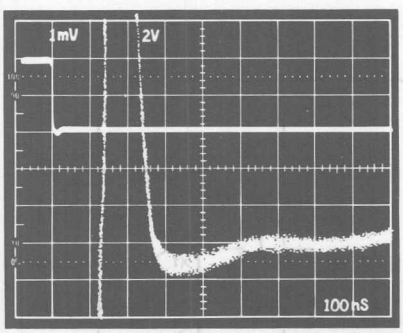


Figure 2. Typical AD684 Hold Mode

HOLD MODE OFFSET

The dc accuracy of the AD684 is determined primarily by the hold mode offset. The hold mode offset refers to the difference between the final held output voltage and the input signal at the time the hold command is given. The hold mode offset arises from a voltage error introduced onto the hold capacitor by charge injection of the internal switches. The nominal hold mode offset is specified for a 0V input condition. Over the input range of −5V to +5V, the AD684 is also characterized for an effective gain error and nonlinearity of the held value, as shown in Figure 3. As indicated by the AD684 specifications, the hold mode offset is very well matched between channels and stable over temperature.

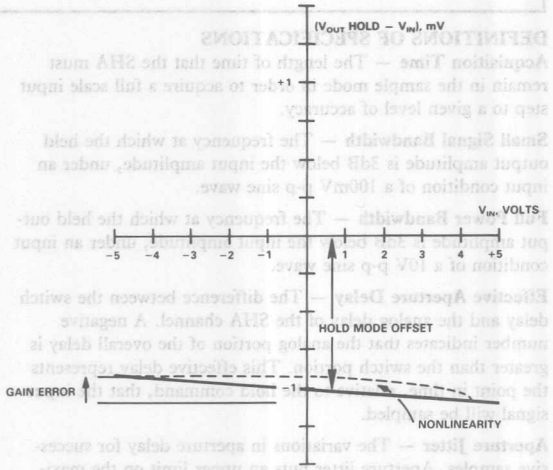


Figure 3. Hold Mode Offset, Gain Error and Nonlinearity

For applications where it is important to obtain zero offset, the hold mode offset may be nulled externally at the input to the A-to-D converter. Adjustment of the offset may be accomplished through the A-to-D itself or by an external amplifier with offset nulling capability (e.g., AD711). Only a single adjustment of the offset is necessary for the four SHA channels as a result of the excellent matching among them. The offset will change less than 0.5mV over the specified temperature range.

SUPPLY DECOUPLING AND GROUNDING CONSIDERATIONS

As with any high speed, high resolution data acquisition system, the power supplies should be well regulated and free from excessive high frequency noise (ripple). The supply connection to the AD684 should also be capable of delivering transient currents to the device. To achieve the specified accuracy and dynamic performance, decoupling capacitors must be placed directly at both the positive and negative supply pins to common. Ceramic type 0.1μF capacitors should be connected from V_{CC} and V_{EE} to common.

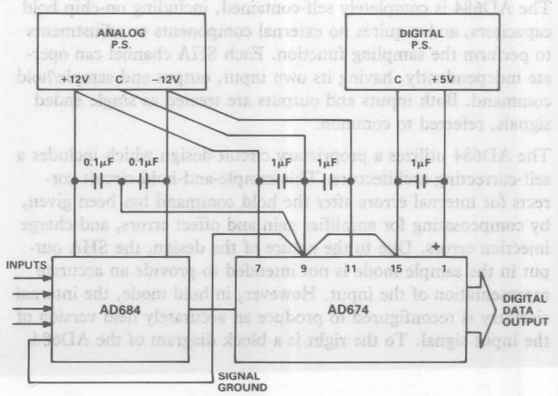


Figure 4. Basic Grounding and Decoupling Diagram

The AD684 does not provide separate analog and digital ground leads as is the case with most A-to-D converters. The common pin is the single ground terminal for the device. It is the reference point for the sampled input voltage and the held output voltage and also the digital ground return path. The common pin should be connected to the reference (analog) ground of the A-to-D converter with a separate ground lead. Since the analog and digital grounds in the 684 are connected internally, the common pin should also be connected to the digital ground, which is usually tied to analog common at the A-to-D converter. Figure 4 illustrates the recommended decoupling and grounding practice.

NOISE CHARACTERISTICS

Designers of data conversion circuits must also consider the effect of noise sources on the accuracy for the data acquisition system. A sample-and-hold amplifier that precedes the A-to-D converter introduces some noise and represents another source of uncertainty in the conversion process. The noise from the AD684 is specified as the total output noise, which includes both the sampled wideband noise of the SHA in addition to the band limited output noise. The total output noise is the rms sum of the sampled dc uncertainty and the hold mode noise. A plot of the total output noise vs. the equivalent input bandwidth of the converter being used is given in Figure 5.

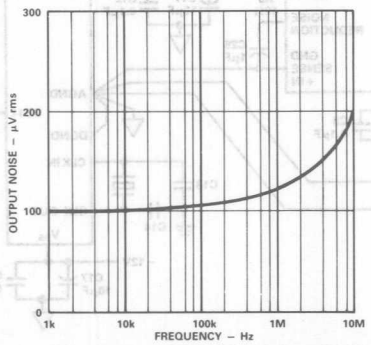


Figure 5. RMS Noise vs. Input Bandwidth of ADC

DRIVING THE ANALOG INPUTS

For best performance, it is important to drive the AD684 analog inputs from a low impedance signal source. This enhances the sampling accuracy by minimizing the analog and digital crosstalk. Signals which come from higher impedance sources (e.g., over 5k ohms) will have a relatively higher level of crosstalk. For applications where signals have high source impedance, an operational amplifier buffer in front of the AD684 is required. The AD713 (precision quad BiFET op amp) is recommended for these applications.

HIGH FREQUENCY SAMPLING

Aperture jitter and distortion are the primary factors which limit frequency domain performance of a sample-and-hold amplifier. Aperture jitter modulates the phase of the hold command and produces an effective noise on the sampled analog input. The magnitude of the jitter induced noise is directly related to the frequency of the input signal.

A graph showing the magnitude of the jitter induced error vs. frequency of the input signal is given in Figure 6.

The accuracy in sampling high frequency signals is also constrained by the distortion and noise created by the sample-and-hold. The level of distortion increases with frequency and reduces the "effective number of bits" of the conversion.

Measurements of Figures 7 and 8 were made using a 14-bit A-to-D converter with $V_{IN} = 10V$ p-p and a sample frequency of 100kSPS.

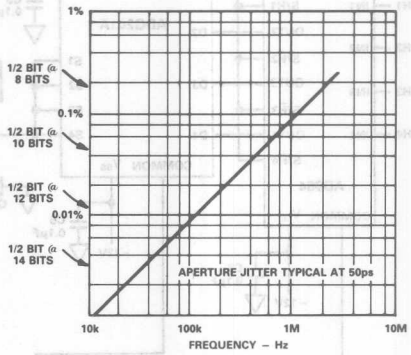


Figure 6. Error Magnitude vs. Frequency

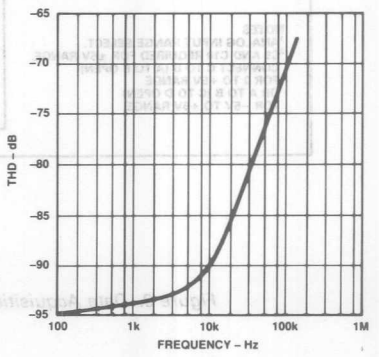


Figure 7. Total Harmonic Distortion vs. Frequency

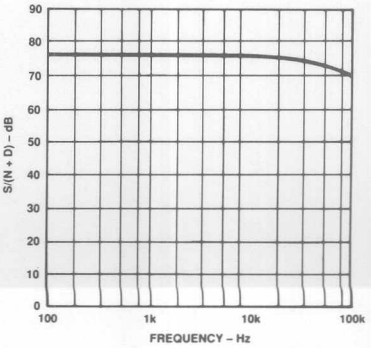


Figure 8. Signal/(Noise and Distortion) vs. Frequency

DATA ACQUISITION APPLICATIONS

Figure 9 shows a typical data acquisition circuit using the AD684 and the high speed 12-bit A-to-D converter, the AD7672. Four input signals are simultaneously sampled by the AD684 as the $\overline{HOLD}$ command is given. One of the four held outputs is selected by the ADG201, quad CMOS switch, and buffered by the AD711. The AD588 provides the reference voltage with switches A–B and C–D selecting a −5V to +5V or 0 to +5V input range.

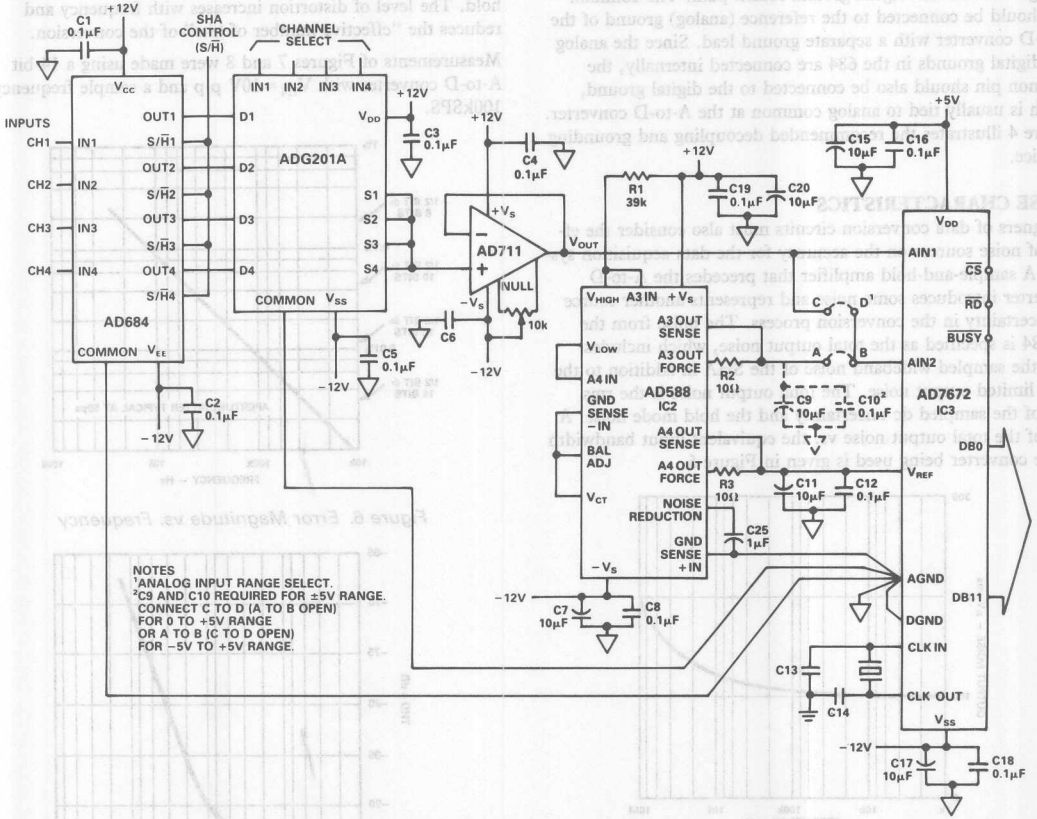


Figure 9. Data Acquisition System Using the AD684 and the AD7672

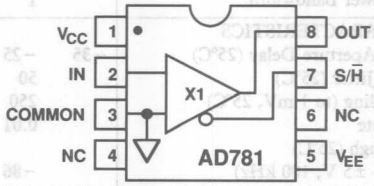
Complete 700 ns Sample-and-Hold Amplifier

AD781*

FEATURES

Acquisition Time to 0.01%: 700 ns Maximum
Low Power Dissipation: 95 mW
Low Droop Rate: 0.01 μV/μs
Fully Specified and Tested Hold Mode Distortion
Total Harmonic Distortion: −80 dB Maximum
Aperture Jitter: 75 ps Maximum
Internal Hold Capacitor
Self-Correcting Architecture
8-Pin Mini Cerdip and Plastic Package
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



4

PRODUCT DESCRIPTION

The AD781 is a high speed monolithic sample-and-hold amplifier (SHA). The AD781 guarantees a maximum acquisition time of 700 ns to 0.01% over temperature. The AD781 is specified and tested for hold mode total harmonic distortion and hold mode signal-to-noise and distortion. The AD781 is configured as a unity gain amplifier and uses a self-correcting architecture that minimizes hold mode errors and insures accuracy over temperature. The AD781 is self-contained and requires no external components or adjustments.

The low power dissipation, 8-pin mini-DIP package and completeness make the AD781 ideal for highly compact board layouts. The AD781 will acquire a full-scale input in less than 700 ns and retain the held value with a droop rate of 0.01 μV/μs. Excellent linearity and hold mode dc and dynamic performance make the AD781 ideal for 12- and 14-bit high speed analog-to-digital converters.

The AD781 is manufactured on Analog Devices' BiMOS process which merges high performance, low noise bipolar circuitry with low power CMOS to provide an accurate, high speed, low power SHA.

The AD781 is specified for three temperature ranges. The J grade device is specified for operation from 0°C to 70°C, the A grade from −40°C to +85°C and the S grade from −55°C to +125°C. The J and A grades are available in 8-pin plastic DIP packages. The S grade is available in an 8-pin cerdip package.

***Protected by U.S. Patent No. 4,962,325.**

PRODUCT HIGHLIGHTS

1. Fast acquisition time (700 ns), low aperture jitter (75 ps) and fully specified hold mode distortion make the AD781 an ideal SHA for sampling systems.
2. Low droop (0.01 μV/μs) and internally compensated hold mode error results in superior system accuracy.
3. Low power (95 mW typical), complete functionality and small size make the AD781 an ideal choice for a variety of high performance, low power applications.
4. The AD781 requires no external components or adjustments.
5. Excellent choice as a front-end SHA for high speed analog-to-digital converters such as the AD671, AD7586, AD674B, AD774B, AD7572 and AD7672.
6. Fully specified and tested hold mode distortion guarantees the performance of the SHA in sampled data systems.
7. The AD781 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD781/883B data sheet for detailed specifications.

AD781—SPECIFICATIONS

DC SPECIFICATIONS (T_{min} to T_{max} with V_{CC} = +12 V ± 10%, V_{EE} = −12 V ± 10%, C_L = 20 pF, unless otherwise specified)

Parameter	AD781J Min	AD781J Typ	AD781J Max	AD781A Min	AD781A Typ	AD781A Max	AD781S Min	AD781S Typ	AD781S Max	Units
SAMPLING CHARACTERISTICS										
Acquisition Time										
10 V Step to 0.01%		600	700		600	700		600	700	ns
10 V Step to 0.1%		500	600		500	600		500	600	ns
Small Signal Bandwidth		4			4			4		MHz
Full Power Bandwidth		1			1			1		MHz
HOLD CHARACTERISTICS										
Effective Aperture Delay (25°C)	**−35**	−25	**−15**	**−35**	−25	**−15**	**−35**	−25	**−15**	ns
Aperture Jitter (25°C)		50	75		50	75		50	75	ps
Hold Settling (to 1 mV, 25°C)		250	**500**		250	**500**		250	**500**	ns
Droop Rate		0.01	**1**		0.01	**1**		0.01	**1**	µV/µs
Feedthrough (25°C)										
(V_{IN} = ±5 V, 100 kHz)		−86			−86			−86		dB
ACCURACY CHARACTERISTICS[1]										
Hold Mode Offset	**−4**	−1	**+3**	**−4**	−1	**+3**	**−4**	−1	**+3**	mV
Hold Mode Offset Drift		10			10			10		µV/°C
Sample Mode Offset		50	**200**		50	**200**		50	**200**	mV
Nonlinearity		±0.002	±0.003		±0.002	±0.003		±0.003	±0.005	% FS
Gain Error		±0.01	**±0.025**		±0.01	**±0.025**		±0.01	**±0.025**	% FS
OUTPUT CHARACTERISTICS										
Output Drive Current	**−5**		**+5**	**−5**		**+5**	**−5**		**+5**	mA
Output Resistance, DC		0.3	**0.5**		0.3	**0.5**		0.3	**0.5**	Ω
Total Output Noise (DC to 5 MHz)		150			150			150		µV rms
Sampled DC Uncertainty		85			85			85		µV rms
Hold Mode Noise (DC to 5 MHz)		125			125			125		µV rms
Short Circuit Current										
Source		20			20			20		mA
Sink		10			10			10		mA
INPUT CHARACTERISTICS										
Input Voltage Range	−5		+5	−5		+5	−5		+5	V
Bias Current		50	**250**		50	**250**		50	**250**	nA
Input Impedance		50			50			50		MΩ
Input Capacitance		2			2			2		pF
DIGITAL CHARACTERISTICS										
Input Voltage Low			**0.8**			**0.8**			**0.8**	V
Input Voltage High	**2.0**			**2.0**			**2.0**			V
Input Current High (V_{IN} = 5 V)		2	**10**		2	**10**		2	**10**	µA
POWER SUPPLY CHARACTERISTICS										
Operating Voltage Range	±10.8	±12	±13.2	±10.8	±12	±13.2	±10.8	±12	±13.2	V
Supply Current		4	**6.5**		4	**6.5**		4	**7**	mA
+PSRR (+12 V ± 10%)	**70**	80		**70**	80		**70**	80		dB
−PSRR (−12 V ± 10%)	**65**	75		**65**	75		**65**	75		dB
Power Consumption		95	175		95	175		95	185	mW
TEMPERATURE RANGE										
Specified Performance	0		+70	−40		+85	−55		+125	°C

NOTE

[1]Specified and tested over an input range of ±5 V.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all devices at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed although only those shown in **boldface** are tested.

HOLD MODE AC SPECIFICATIONS

(T_{min} to T_{max}, V_{CC} = +12 V ±10%, V_{EE} = −12 V ±10%, C_L = 20 pF, unless otherwise specified)[1]

Parameter	AD781J Min	AD781J Typ	AD781J Max	AD781A Min	AD781A Typ	AD781A Max	AD781S Min	AD781S Typ	AD781S Max	Units
TOTAL HARMONIC DISTORTION										
F_{IN} = 10 kHz		−90	−80		−90	−80		−90	−80	dB
F_{IN} = 50 kHz		−73			−73			−73		dB
F_{IN} = 100 kHz		−68			−68			−68		dB
SIGNAL-TO-NOISE AND DISTORTION										
F_{IN} = 10 kHz	72	78		72	78		72	78		dB
F_{IN} = 50 kHz		73			73			73		dB
F_{IN} = 100 kHz		67			67			67		dB
INTERMODULATION DISTORTION										
F_{IN1} = 49 kHz, F_{IN2} = 50 kHz										
2nd Order Products		−77			−77			−77		dB
3rd Order Products		−78			−78			−78		dB

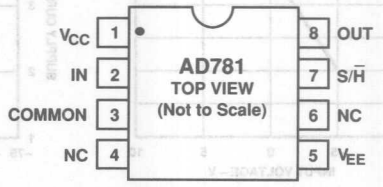
NOTE
[1]F_{IN} amplitude = 0 dB and F_{SAMPLE} = 500 kHz unless otherwise indicated.
Specifications shown in **boldface** are tested on all devices at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed although only those shown in **boldface** are tested.

ABSOLUTE MAXIMUM RATINGS*

Spec	With Respect to	Min	Max	Unit
V_{CC}	Common	−0.3	+15	V
V_{EE}	Common	−15	+0.3	V
Control Input	Common	−0.5	+7	V
Analog Input	Common	−12	+12	V
Output Short Circuit to Ground, V_{CC}, or V_{EE}		Indefinite		
Maximum Junction Temperature			+175	°C
Storage		−65	+150	°C
Lead Temperature (10 sec max)			+300	°C
Power Dissipation			195	mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

PIN CONFIGURATION



ORDERING GUIDE

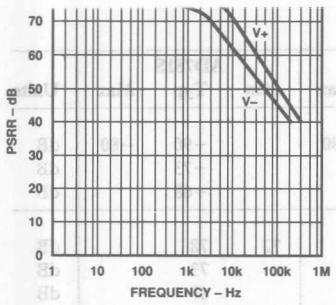
Model[1]	Temperature Range	Description	Package Options[2]
AD781JN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD781AN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD781SQ	−55°C to +125°C	8-Pin Cerdip	Q-8

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD781/883B data sheet.
[2]N = Plastic DIP; Q = Cerdip. For outline information see Package Information section.

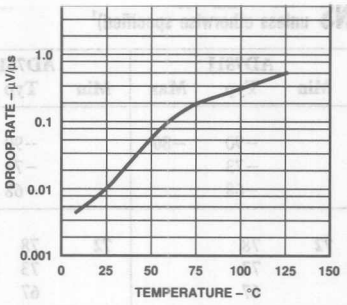
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.

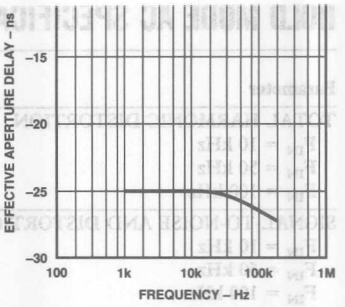




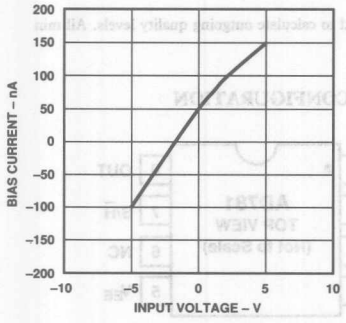
Power Supply Rejection Ratio vs. Frequency



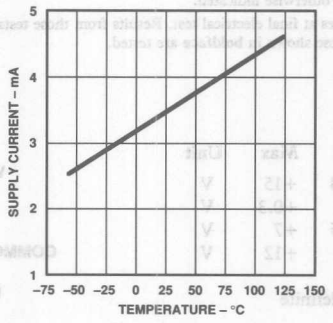
Droop Rate vs. Temperature, V_{IN} = 0 V



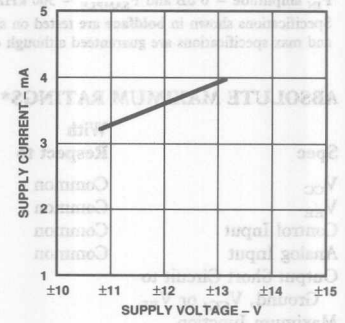
Effective Aperture Delay vs. Frequency



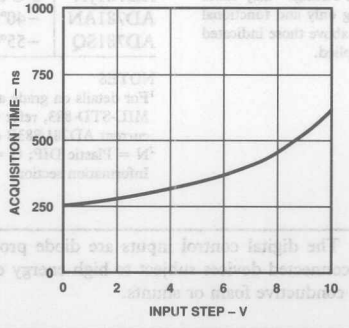
Bias Current vs. Input Voltage



Supply Current vs. Temperature



Supply Current vs. Supply Voltage



Acquisition Time (to 0.01%) vs. Input Step Size

DEFINITIONS OF SPECIFICATIONS

Acquisition Time—The length of time that the SHA must remain in the sample mode in order to acquire a full-scale input step to a given level of accuracy.

Small Signal Bandwidth—The frequency at which the held output amplitude is 3 dB below the input amplitude, under an input condition of a 100 mV p–p sine wave.

Full Power Bandwidth—The frequency at which the held output amplitude is 3 dB below the input amplitude, under an input condition of a 10 V p–p sine wave.

Effective Aperture Delay—The difference between the switch delay and the analog delay of the SHA channel. A negative number indicates that the analog portion of the overall delay is greater than the switch portion. This effective delay represents the point in time, relative to the hold command, that the input signal will be sampled.

Aperture Jitter—The variations in aperture delay for successive samples. Aperture jitter puts an upper limit on the maximum frequency that can be accurately sampled.

Hold Settling Time—The time required for the output to settle to within a specified level of accuracy of its final held value after the hold command has been given.

Droop Rate—The drift in output voltage while in the hold mode.

Feedthrough—The attenuated version of a changing input signal that appears at the output when the SHA is in the hold mode.

Hold Mode Offset—The difference between the input signal and the held output. This offset term applies only in the hold mode and includes the error caused by charge injection and all other internal offsets. It is specified for an input of 0 V.

Tracking Mode Offset—The difference between the input and output signals when the SHA is in the track mode.

Nonlinearity—The deviation from a straight line on a plot of input vs. (held) output as referenced to a straight line drawn between endpoints, over an input range of −5 V and +5 V.

Gain Error—Deviation from a gain of +1 on the transfer function of input vs. held output.

Power Supply Rejection Ratio—A measure of change in the held output voltage for a specified change in the positive or negative supply.

Sampled DC Uncertainty—The internal rms SHA noise that is sampled onto the hold capacitor.

Hold Mode Noise—The rms noise at the output of the SHA while in the hold mode, specified over a given bandwidth.

Total Output Noise—The total rms noise that is seen at the output of the SHA while in the hold mode. It is the rms summation of the sampled dc uncertainty and the hold mode noise.

Output Drive Current—The maximum current the SHA can source (or sink) while maintaining a change in hold mode offset of less than 2.5 mV.

Signal-To-Noise and Distortion (S/N+D) Ratio—S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

Total Harmonic Distortion (THD)—THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

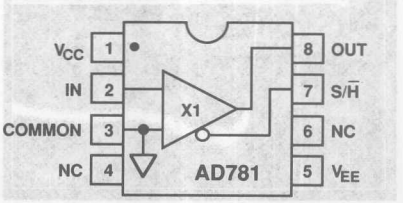
Intermodulation Distortion (IMD)—With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequency of mfa±nfb, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa+fb) and (fa−fb), and the third order terms are (2fa+fb), (2fa−fb), (fa+2fb) and (fa−2fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals are of equal amplitude, and peak value of their sums is −0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

FUNCTIONAL DESCRIPTION

The AD781 is a complete sample-and-hold amplifier that provides high speed sampling to 12-bit accuracy in less than 700 ns.

The AD781 is completely self-contained, including an on-chip hold capacitor, and requires no external components or adjustments to perform the sampling function. Both input and output are treated as a single-ended signal, referred to common.

The AD781 utilizes a proprietary circuit design which includes a self-correcting architecture. This sample-and-hold circuit corrects for internal errors after the hold command has been given, by compensating for amplifier gain and offset errors, and charge injection errors. Due to the nature of the design, the SHA output in the sample mode is not intended to provide an accurate representation of the input. However, in hold mode, the internal circuitry is reconfigured to produce an accurately held version of the input signal. Below is a block diagram of the AD781.



Functional Block Diagram

DYNAMIC PERFORMANCE

The AD781 is compatible with 12-bit A-to-D converters in terms of both accuracy and speed. The fast acquisition time, fast hold settling time and good output drive capability allow the AD781 to be used with high speed, high resolution A-to-D converters like the AD674 and AD672. The AD781's fast acquisition time provides high throughput rates for multichannel data acquisition systems. Typically, the sample and hold can acquire a 10 V step in less than 600 ns. Figure 1 shows the settling accuracy as a function of acquisition time.

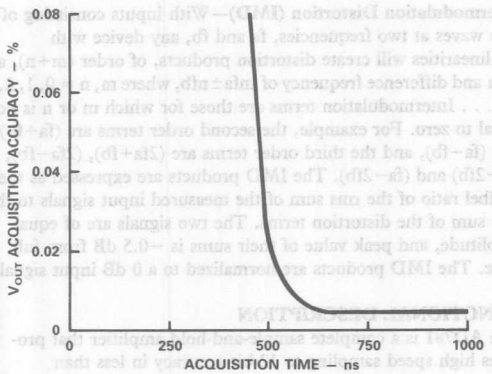


Figure 1. V_{OUT} Settling vs. Acquisition Time

The hold settling determines the required time, after the hold command is given, for the output to settle to its final specified accuracy. The typical settling behavior of the AD781 is shown in Figure 2. The settling time of the AD781 is sufficiently fast to allow the SHA, in most cases, to directly drive an A-to-D converter without the need for an added "start convert" delay.

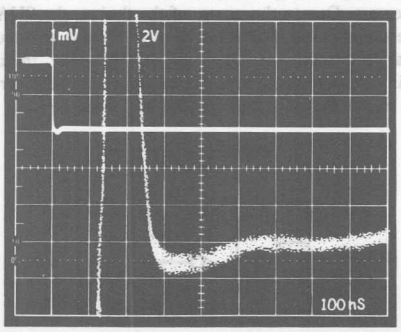


Figure 2. Typical AD781 Hold Mode

HOLD MODE OFFSET

The dc accuracy of the AD781 is determined primarily by the hold mode offset. The hold mode offset refers to the difference between the final held output voltage and the input signal at the time the hold command is given. The hold mode offset arises from a voltage error introduced onto the hold capacitor by charge injection of the internal switches. The nominal hold mode offset is specified for a 0 V input condition. Over the input range of −5 V to +5 V, the AD781 is also characterized for

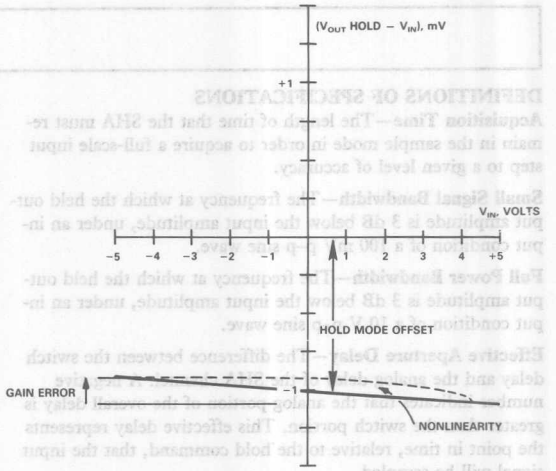


Figure 3. Hold Mode Offset, Gain Error and Nonlinearity

an effective gain error and nonlinearity of the held value, as shown in Figure 3. As indicated by the AD781 specifications, the hold mode offset is very stable over temperature.

For applications where it is important to obtain zero offset, the hold mode offset may be nulled externally at the input to the A-to-D converter. Adjustment of the offset may be accomplished through the A-to-D itself or by an external amplifier with offset nulling capability (e.g., AD711). The offset will change less than 0.5 mV over the specified temperature range.

SUPPLY DECOUPLING AND GROUNDING CONSIDERATIONS

As with any high speed, high resolution data acquisition system, the power supplies should be well regulated and free from excessive high frequency noise (ripple). The supply connection to the AD781 should also be capable of delivering transient currents to the device. To achieve the specified accuracy and dynamic performance, decoupling capacitors must be placed directly at both the positive and negative supply pins to common. Ceramic type 0.1 μF capacitors should be connected from V_{CC} and V_{EE} to common.

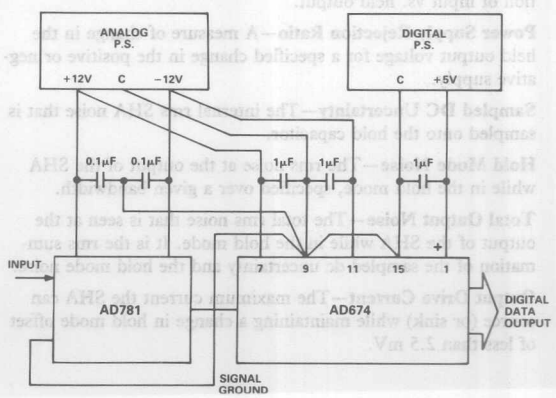


Figure 4. Basic Grounding and Decoupling Diagram

The AD781 does not provide separate analog and digital ground leads as is the case with most A-to-D converters. The common pin is the single ground terminal for the device. It is the reference point for the sampled input voltage and the held output voltage and also the digital ground return path. The common pin should be connected to the reference (analog) ground of the A-to-D converter with a separate ground lead. Since the analog and digital grounds in the AD781 are connected internally, the common pin should also be connected to the digital ground, which is usually tied to analog common at the A-to-D converter. Figure 4 illustrates the recommended decoupling and grounding practice.

NOISE CHARACTERISTICS

Designers of data conversion circuits must also consider the effect of noise sources on the accuracy of the data acquisition system. A sample-and-hold amplifier that precedes the A-to-D converter introduces some noise and represents another source of uncertainty in the conversion process. The noise from the AD781 is specified as the total output noise, which includes both the sampled wideband noise of the SHA in addition to the band limited output noise. The total output noise is the rms sum of the sampled dc uncertainty and the hold mode noise. A plot of the total output noise vs. the equivalent input bandwidth of the converter being used is given in Figure 5.

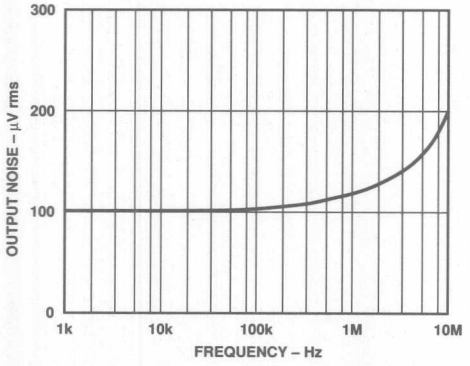


Figure 5. RMS Noise vs. Input Bandwidth of ADC

DRIVING THE ANALOG INPUTS

For best performance, it is important to drive the AD781 analog input from a low impedance signal source. This enhances the sampling accuracy by minimizing the analog and digital crosstalk. Signals which come from higher impedance sources (e.g., over 5 kΩ) will have a relatively higher level of crosstalk. For applications where signals have high source impedance, an operational amplifier buffer in front of the AD781 is required. The AD711 (precision BiFET op amp) is recommended for these applications.

HIGH FREQUENCY SAMPLING

Aperture jitter and distortion are the primary factors which limit frequency domain performance of a sample-and-hold amplifier. Aperture jitter modulates the phase of the hold command and produces an effective noise on the sampled analog input. The magnitude of the jitter induced noise is directly related to the frequency of the input signal.

A graph showing the magnitude of the jitter induced error vs. frequency of the input signal is given in Figure 6.

The accuracy in sampling high frequency signals is also constrained by the distortion and noise created by the sample-and-hold. The level of distortion increases with frequency and reduces the "effective number of bits" of the conversion.

Measurements of Figures 7 and 8 were made using a 14-bit A/D converter with V_{IN} = 10 V p–p and a sample frequency of 100 kSPS.

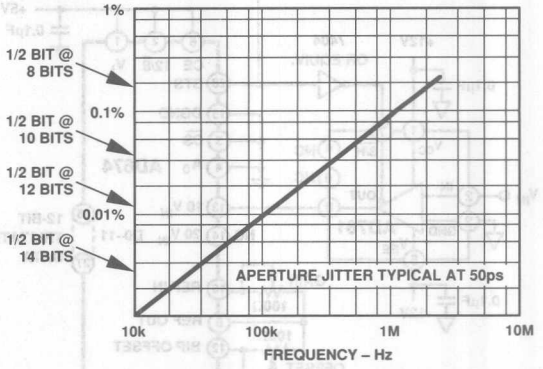


Figure 6. Error Magnitude vs. Frequency

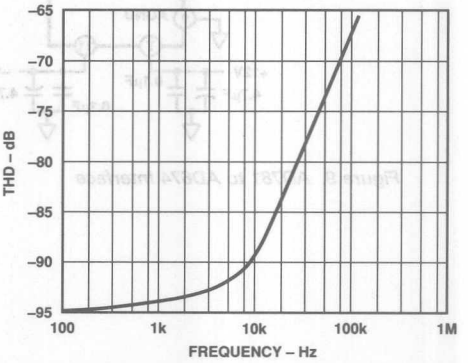


Figure 7. Total Harmonic Distortion vs. Frequency

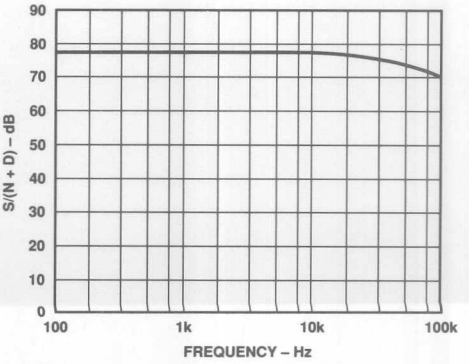


Figure 8. Signal/(Noise and Distortion) vs. Frequency

AD781, a high linearity, low aperture jitter SHA and the AD674 a 12-bit high speed ADC. The time between the AD674 status line going high and the actual start of conversion allows the AD781 to settle to 0.01%. As a result, the AD674 status line can be used to control the AD781; only an inverter is needed to interface the two devices.

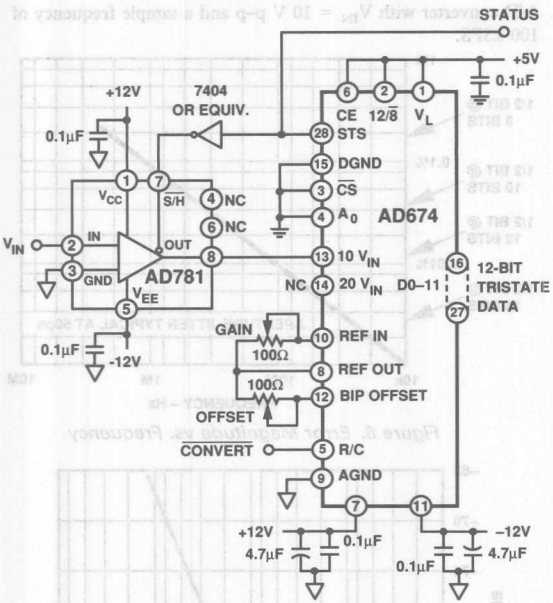


Figure 9. AD781 to AD674 Interface

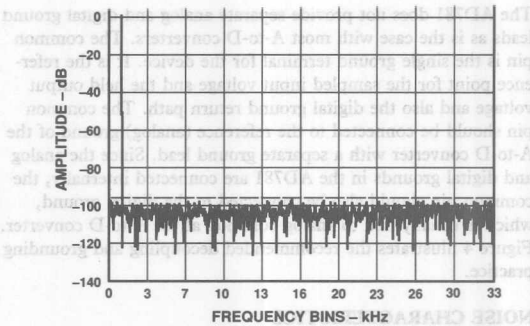


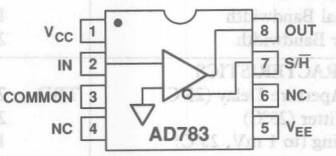
Figure 10. FFT Plot of AD781 to AD674 Interface, F_{IN} = 1 kHz

Complete 250 ns Sample-and-Hold Amplifier

AD783*

FEATURES
- Acquisition Time to 0.01%: 250 ns Maximum
- Low Power Dissipation: 95 mW
- Low Droop Rate: 0.02 μV/μs
- Fully Specified and Tested Hold Mode Distortion
- Total Harmonic Distortion: −85 dB
- Aperture Jitter: 50 ps Maximum
- Internal Hold Capacitor
- Self-Correcting Architecture
- 8-Pin Mini Cerdip and Plastic Packages

FUNCTIONAL BLOCK DIAGRAM



NC = NO CONNECT

4

PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

The AD783 is a high speed, monolithic sample-and-hold amplifier (SHA). The AD783 guarantees a maximum acquisition time of 250 ns to 0.01% over temperature. The AD783 is specified and tested for hold mode total harmonic distortion with input frequencies up to 500 kHz. The AD783 is configured as a unity gain amplifier and uses a self-correcting architecture that minimizes hold mode errors and ensures accuracy over temperature. The AD783 is self-contained and requires no external components or adjustments.

The AD783 will acquire a full-scale input in less than 250 ns and will retain the held value with a droop rate of 0.02 μV/μs. Excellent linearity and hold mode dc and dynamic performance make the AD783 ideal for high speed 12- and 14-bit analog-to-digital converters.

The AD783 is manufactured on Analog Devices' ABCMOS process which merges high performance, low noise bipolar circuitry with low power CMOS to provide an accurate, high speed, low power SHA.

The AD783 is specified for three temperature ranges. The J grade device is specified for operation from 0°C to +70°C, the A grade from −40°C to +85°C and the S grade from −55°C to +125°C. The J and A grades are available in 8-pin plastic DIP packages. The S grade is available in an 8-pin cerdip package.

*Protected by U.S. Patent Number 4,962,325.

PRODUCT HIGHLIGHTS

1. Fast acquisition time (250 ns), low aperture jitter (50 ps) and fully specified hold mode distortion make the AD783 an ideal SHA for sampling systems.
2. Low droop (0.02 μV/μs) and internally compensated hold mode error result in superior system accuracy.
3. Low power (95 mW typical), complete functionality and small size make the AD783 an ideal choice for a variety of high performance applications.
4. The AD783 requires no external components or adjustments.
5. The AD783 is an excellent choice as a front-end SHA for high speed analog-to-digital converters such as the AD671, AD7586, AD674B, AD774B, AD7572 and AD7672.
6. Fully specified and tested hold mode distortion guarantees the performance of the SHA in sampled data systems.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD783—SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5%, V_{EE} = −5 V ± 5%, C_L = 50 pF, unless otherwise noted)

Parameter	AD783J			AD783A			AD783S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SAMPLING CHARACTERISTICS										
Acquisition Time										
5 V Step to 0.01%		155	250		150	250		150	250	ns
5 V Step to 0.1%		100	TBD		100	TBD		100	TBD	ns
Small Signal Bandwidth		15			15			15		MHz
Full Power Bandwidth		2			2			2		MHz
HOLD CHARACTERISTICS										
Effective Aperture Delay (25°C)	TBD	20	TBD	TBD	20	TBD	TBD	20	TBD	ns
Aperture Jitter (25°C)		20	50		20	50		20	50	ps
Hold Settling (to 1 mV, 25°C)		150	200		150	200		150	200	ns
Droop Rate		0.02	1		0.02	1		0.02	1	μV/μs
Feedthrough (25°C)										
(V_{IN} = ±2.5 V, 500 kHz)		−80			−80			−80		dB
ACCURACY CHARACTERISTICS[1]										
Hold Mode Offset	−4	0	+4	−4	0	+4	−4	0	+4	mV
Hold Mode Offset Drift		10			10			10		μV/°C
Sample Mode Offset		50	200		50	200		50	200	mV
Nonlinearity		±0.005	±0.01		±0.005	±0.01		±0.005	±0.01	% FS
Gain Error		±0.03	±0.05		±0.03	±0.05		±0.03	±0.05	% FS
OUTPUT CHARACTERISTICS										
Output Drive Current	−5		+5	−5		+5	−5		+5	mA
Output Resistance, DC		0.3	0.6		0.3	0.6		0.3	0.6	Ω
Total Output Noise										
(DC to 5 MHz)		150			150			150		μV rms
Sampled DC Uncertainty		85			85			85		μV rms
Hold Mode Noise										
(DC to 5 MHz)		125			125			125		μV rms
Short Circuit Current										
Source			20			20			20	mA
Sink			13			13			13	mA
INPUT CHARACTERISTICS										
Input Voltage Range	−2.5		+2.5	−2.5		+2.5	−2.5		+2.5	V
Bias Current		100	250		100	250		100	250	nA
Input Impedance		10			10			10		MΩ
Input Capacitance		2			2			2		pF
DIGITAL CHARACTERISTICS										
Input Voltage Low			0.8			0.8			0.8	V
Input Voltage High	2.0			2.0			2.0			V
Input Current High (V_{IN} = 5 V)		2	10		2	10		2	10	μA
POWER SUPPLY CHARACTERISTICS										
Operating Voltage Range	±4.75	±5	±5.25	±4.75	±5	±5.25	±4.75	±5	±5.25	V
Supply Current		9.5	14		9.5	14		9.5	14	mA
+PSRR (+5 V ± 5%)	60	65		60	65		60	65		dB
−PSRR (−5 V ± 5%)	60	65		60	65		60	65		dB
Power Consumption		95	150		95	150		95	150	μW
TEMPERATURE RANGE										
Specified Performance	0		+70	−40		+85	−55		+125	°C

NOTE
[1]Specified and tested over an input range of ±2.5 V.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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HOLD MODE AC SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5%, V_{EE} = −5 V ± 5%, C_L = 50 pF, unless otherwise noted)[1]

Parameter	AD783J Min	AD783J Typ	AD783J Max	AD783A Min	AD783A Typ	AD783A Max	AD783S Min	AD783S Typ	AD783S Max	Units
TOTAL HARMONIC DISTORTION										
F_{IN} = 50 kHz		−85	TBD		−85	TBD		−85	TBD	dB
F_{IN} = 100 kHz		−83	TBD		−83	TBD		−83	TBD	dB
F_{IN} = 250 kHz		−79			−79			−79		dB
F_{IN} = 500 kHz		−72			−72			−72		dB
SIGNAL-TO-NOISE AND DISTORTION										
F_{IN} = 50 kHz	TBD	80		TBD	80		TBD	80		dB
F_{IN} = 100 kHz	TBD	77		TBD	77		TBD	77		dB
F_{IN} = 200 kHz		72			72			72		dB
F_{IN} = 500 kHz		70			70			70		dB
INTERMODULATION DISTORTION (F1 = 99 kHz, F2 = 100 kHz)										
Second Order Products		−80			−80			−80		dB
Third Order Products		−85			−85			−85		dB

NOTE

[1]F_{IN} amplitude = −0.5 dB and t_{ACQ} = 250 ns unless otherwise indicated.

Specifications shown in **boldface** are tested on all devices at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed although only those shown in boldface are tested.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS*

Spec	With Respect to	Min	Max	Units
V_{CC}	COM	−0.5	+6.5	V
V_{EE}	COM	−6.5	+0.5	V
Analog Input	COM	−6.5	+6.5	V
Digital Input	COM	−0.5	+6.5	V
Output Short Circuit to Ground, V_{CC}, or V_{EE}		Indefinite		
Maximum Junction Temperature			+175	°C
Storage		−65	+150	°C
Lead Temperature (10 sec max)			+300	°C
Power Dissipation			195	mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

ORDERING GUIDE

Model	Temperature Range	Package Options*
AD783JN	0°C to +70°C	N-8
AD783AN	−40°C to +85°C	N-8
AD783SQ	−55°C to +125°C	Q-8

*N = Plastic DIP; Q = Cerdip. For outline information see Package Information section.

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DEFINITIONS OF SPECIFICATIONS

Acquisition Time—The length of time that the SHA must remain in the sample mode in order to acquire a full-scale input step to a given level of accuracy.

Small Signal Bandwidth—The frequency at which the held output amplitude is 3 dB below the input amplitude, under an input condition of a 100 mV p–p sine wave.

Full Power Bandwidth—The frequency at which the held output amplitude is 3 dB below the input amplitude, under an input condition of a 5 V p–p sine wave.

Effective Aperture Delay—The difference between the switch delay and the analog delay of the SHA channel. A negative number indicates that the analog portion of the overall delay is greater than the switch portion. This effective delay represents the point in time, relative to the hold command, that the input signal will be sampled.

Aperture Jitter—The variations in delay for successive samples. Aperture jitter puts an upper limit on the maximum frequency that can be accurately sampled.

Hold Settling Time—The time required for the output to settle to within a specified level of accuracy of its final held value after the hold command has been given.

Droop Rate—The drift in output voltage while in the hold mode.

Feedthrough—The attenuated version of a changing input signal that appears at the output when the SHA is in the hold mode.

Hold Mode Offset—The difference between the input signal and the held output. This offset term applies only in the hold mode and includes the error caused by charge injection and all other internal offsets. Hold mode offset is specified with an input of 0 V.

Sample Mode Offset—The difference between the input and output signals when the SHA is in the sample mode.

Nonlinearity—The deviation from a straight line on a plot of input vs. (held) output as referenced to a straight line drawn between endpoints, over an input range of −2.5 V and +2.5 V.

Gain Error—Deviation from a gain of +1 on the transfer function of input vs. held output.

Power Supply Rejection Ratio—A measure of change in the held output voltage for a specified change in the positive or negative supply.

Sampled DC Uncertainty—The internal rms SHA noise that is sampled onto the hold capacitor.

Hold Mode Noise—The rms noise at the output of the SHA while in the hold mode, specified over a given bandwidth.

Total Output Noise—The total rms noise that is seen at the output of the SHA while in the hold mode. It is the rms summation of the sampled dc uncertainty and the hold mode noise.

Output Drive Current—The maximum current the SHA can source (or sink) while maintaining a change in hold mode offset of less than 2.5 mV.

Total Harmonic Distortion (THD)—THD is the ratio of the rms sum of the first six harmonic components to the rms value of a full-scale input signal and is expressed as a percentage or in decibels.

Signal-to-Noise and Distortion Ratio (S/N+D)—S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

Intermodulation Distortion (IMD)—With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb) and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (2 fb − fa). The IMD products are expressed as the decibel ratio of the RMS sum of the measured input signals to the RMS sum of the distortion terms. The two signals are of equal amplitude and the peak value of their sums is −0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD1154

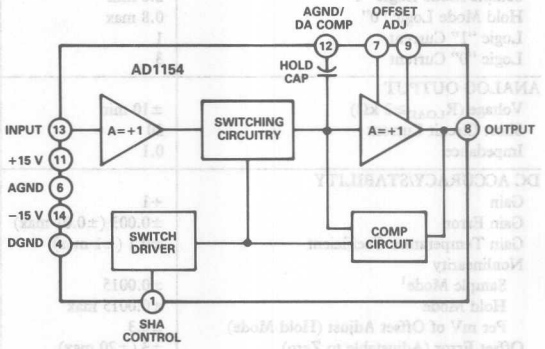
FEATURES

- Low Nonlinearity: ±7.6 ppm max (1/2 LSB @ 16-Bit Accuracy)
- Fast Acquisition Time to ±0.00076%: 3.5 μs
- Low Droop Rate: 0.02 μV/μs
- Aperture Jitter: 150 ps
- ±10 V Input Range
- Hold Mode Feedthrough Rejection of −106 dB
- 14-Pin Metal DIP
- Gain of +1 V/V
- Low Cost

APPLICATIONS

- Medical and Analytical Instrumentation
- Automatic Test Equipment
- Data Acquisition for Signal Processing
- Simultaneous Sample-and-Hold
- Peak Measurement Detection
- Event Analysis

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD1154 is a high accuracy, low cost sample-and-hold amplifier (SHA) designed to be used in high resolution data acquisition systems. It is complete with internal hold capacitor and proprietary capacitor trimmed compensation circuitry. Its accuracy (0.00076% of full scale range) and dynamic performance allow it to be used with high speed 16-bit A/D converters. The AD1154's low price enables users to upgrade the front end performance of 14-bit systems without increasing system cost. Its gain accuracy and droop rate in "hold" mode also allow accurate conversion by slower 16-bit A/D converters having conversion times of up to 7.6 ms.

The AD1154 is a hybrid noninverting sample-and-hold amplifier (SHA) with a gain of +1 V/V. It can be utilized in most inverting SHA applications by inverting the digital data. The AD1154 is packaged in a compact 14-pin metal DIP.

Typical applications for the AD1154 include data acquisition systems, strobed measurement systems, peak hold circuits and simultaneous sample-and-hold functions. The AD1154 is available in two grades, both operating over the −25°C to +85°C temperature range. The "A" grade is specified for 15-bit accurate systems, while the "B" grade offers superior performance for true 16-bit applications.

PRODUCT HIGHLIGHTS

1. Fast acquisition and low jitter make it the right choice for high speed, high accuracy data acquisition.
2. Its low droop rate (0.02 μV/μs) allows it to be used in slower systems without noticeable performance degradation.
3. The AD1154 is ideal for systems requiring wide dynamic range.
4. Low price reduces overall system cost.
5. Unity gain buffer architecture allows ease of use.

4

AD1154—SPECIFICATIONS (typical @ 25°C and nominal power supply of ±15 V unless otherwise noted)

Model	AD1154AW	AD1154BW	Units
ANALOG INPUT			
Voltage Range	±10 min	*	V
Overvoltage (No Damage)	$\pm V_S$	*	V
Input Impedance	10^{12}	*	Ω
Input Capacitance	10	*	pF
DIGITAL INPUT (TTL COMPATIBLE)			
Sample Mode Logic "1"	2.0 min	*	V
Hold Mode Logic "0"	0.8 max	*	V
Logic "1" Current	1	*	μA
Logic "0" Current	3	*	μA
ANALOG OUTPUT			
Voltage ($R_{LOAD} \geq 2$ kΩ)	±10 min	*	V
Short Circuit Current	20	*	mA
Impedance	0.1	*	Ω @ 1 kHz
DC ACCURACY/STABILITY			
Gain	+1	*	V/V
Gain Error	±0.003 (±0.01 max)	*	%
Gain Temperature Coefficient	±0.1 (±1 max)	*	ppm/°C
Nonlinearity			
Sample Mode[1]	±0.0015	*	%
Hold Mode	±0.0015 max	±0.00076 max	%
Per mV of Offset Adjust (Hold Mode)	±0.3	*	ppm/mV
Offset Error (Adjustable to Zero)	±3 (±20 max)	*	mV
Offset Error @ T_{min}, T_{max}[2]	±0.6	*	mV
Offset Tempco per mV of Offset Adjust	±0.5	*	μV/°C/mV
SAMPLE MODE DYNAMICS			
Small Signal Bandwidth (−3 dB)	1	*	MHz
Full Power Bandwidth	120	*	kHz
Slew Rate	10	*	V/μs
Noise (dc to 1 MHz)	40	*	μV rms
SAMPLE-TO-HOLD SWITCHING			
Aperture Delay	80	*	ns
Aperture Uncertainty (Jitter)	150	*	ps
Offset Step (Pedestal)	±8	*	mV
Switching Transient			
Amplitude	±75	*	mV
Settling to ±0.003%	0.4	*	μs
Settling to ±0.00076%	1	*	μs
Dielectric Absorption Error (Uncompensated)	0.003	*	%
HOLD MODE DYNAMICS			
Droop Rate	0.2 (0.7 max)	0.1 (0.35 max)	μV/μs
Droop Rate @ T_{max}	5	2.5	μV/μs
Feedthrough Rejection (20 V p-p @ 10 kHz)	−106 (−96 max)	*	dB
HOLD-TO-TRACK SWITCHING			
Acquisition Time to ±0.00076% of 20 V[3]	5 (8 max)	3.5 (5 max)	μs
POWER REQUIREMENTS			
Nominal Voltage for Rated Performance (V_S)	±15 (±3%)	*	V
Power Supply Rejection	20	*	μV/V
Supply Current			
$+V_S$	10	*	mA
$-V_S$	10	*	mA
Power Dissipation	300	*	mW
TEMPERATURE RANGE			
Rated Performance	−25 to +85	*	°C
Storage	−40 to +125	*	°C
PACKAGE	14-Pin DIP	*	

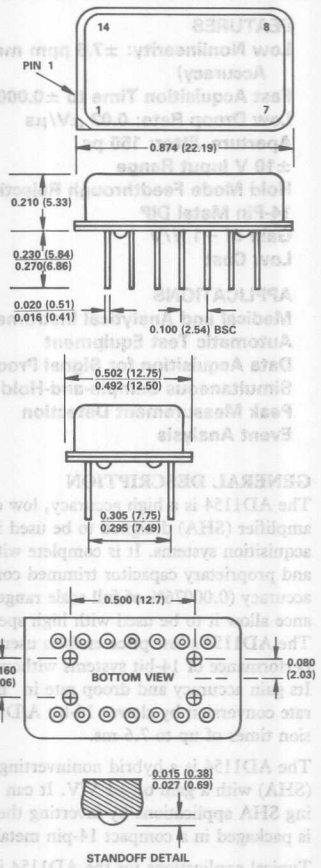
NOTE
[1]The AD1154 was designed specifically for 16-bit accurate sample/hold applications (tailored for hold mode performance), but it may be used as a track-and-hold amplifier with 15-bit accurate tracking performance.
[2]Error at +25°C adjusted to zero.
[3]Tested with 5 kΩ load.
*Specification same as AD1154AW.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions are shown in inches and (mm).

14-LEAD METAL PLATFORM DIP



PIN DESIGNATIONS

PIN	DESCRIPTION	PIN	DESCRIPTION
1	SHA CONTROL	8	SHA OUTPUT
2	NO CONNECTION	9	OFFSET ADJUST
3	NO CONNECTION	10	NO CONNECTION
4	DIGITAL GROUND	11	+15 V
5	NO CONNECTION	12	ANA GND/DA COMP
6	ANALOG GROUND	13	SHA INPUT
7	OFFSET ADJUST	14	−15 V

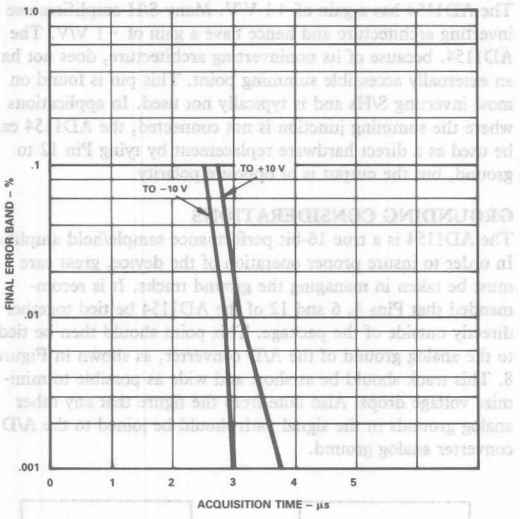


Figure 1. Acquisition Time vs. Final Error Band for 20 Volt Step

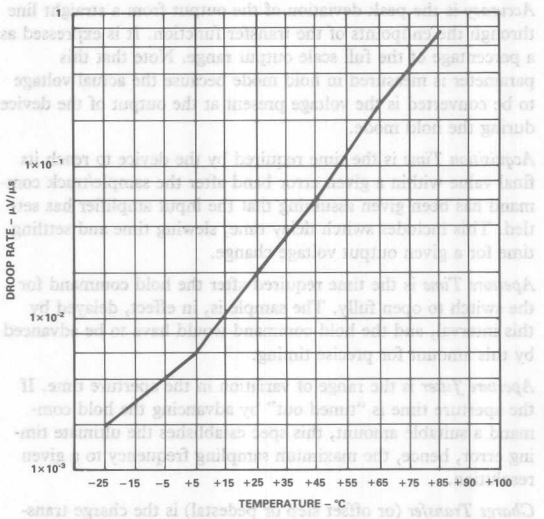


Figure 2. Droop Rate vs. Temperature

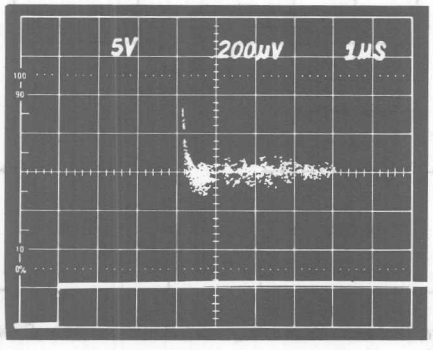


Figure 3. Hold-to-Sample Acquisition Time

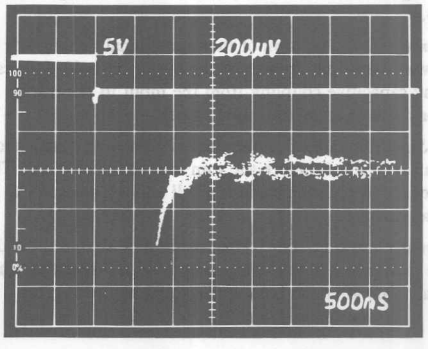


Figure 4. Sample-to-Hold Settling Time

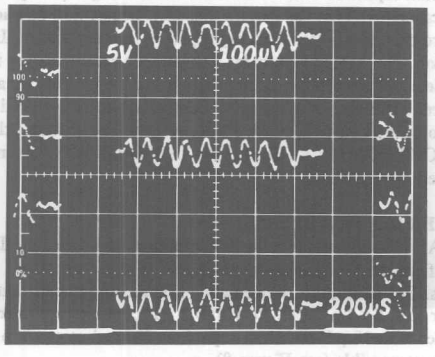


Figure 5. Input Feedthrough

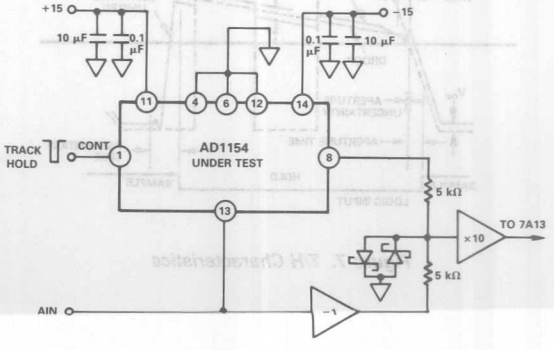


Figure 6. Acquisition Time Test Circuit

TERMINOLOGY

Accuracy is the peak deviation of the output from a straight line through the endpoints of the transfer function. It is expressed as a percentage of the full scale output range. Note that this parameter is measured in hold mode because the actual voltage to be converted is the voltage present at the output of the device during the hold mode.

Acquisition Time is the time required by the device to reach its final value within a given error band after the sample/track command has been given assuming that the input amplifier has settled. This includes switch delay time, slewing time and settling time for a given output voltage change.

Aperture Time is the time required after the hold command for the switch to open fully. The sample is, in effect, delayed by this interval, and the hold command would have to be advanced by this amount for precise timing.

Aperture Jitter is the range of variation in the aperture time. If the aperture time is "tuned out" by advancing the hold command a suitable amount, this spec establishes the ultimate timing error, hence, the maximum sampling frequency to a given resolution.

Charge Transfer (or offset step or pedestal) is the charge transferred to the storage capacitor when switching to the hold mode.

Droop Rate is the rate of change in output voltage over time while in the hold mode. The droop rate will determine how long a signal can be accurately held before it changes more than 1 LSB.

Feedthrough is the fraction of the input signal variation or ac input waveform that appears at the output in hold. It is caused by stray capacitive coupling from the input to the storage capacitor, principally across the open switch.

Small Signal Bandwidth is the maximum analog signal frequency that can be tracked before the gain is reduced by 3 dB. This assumes the signal amplitude is small enough so as not to be slew rate limited.

Switching Transient Settling Time is the time required for the device to stabilize in the hold mode to within specified limits of its final value after the hold mode signal has been given.

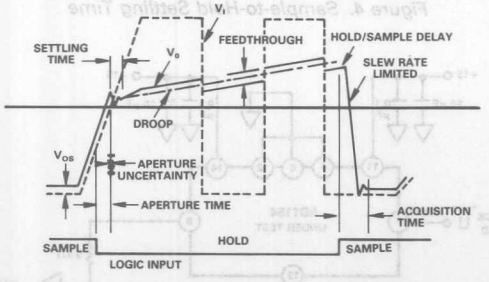


Figure 7. T/H Characteristics

INVERTING VS. NONINVERTING ARCHITECTURE

The AD1154 has a gain of +1 V/V. Many S/H amplifiers use an inverting architecture and hence have a gain of −1 V/V. The AD1154, because of its noninverting architecture, does not have an externally accessible summing point. This pin is found on most inverting S/Hs and is typically not used. In applications where the summing junction is not connected, the AD1154 can be used as a direct hardware replacement by tying Pin 12 to ground, but the output is of opposite polarity.

GROUNDING CONSIDERATIONS

The AD1154 is a true 16-bit performance sample/hold amplifier. In order to insure proper operation of the device, great care must be taken in managing the ground tracks. It is recommended that Pins 4, 6 and 12 of the AD1154 be tied together directly outside of the package. This point should then be tied to the analog ground of the A/D converter, as shown in Figure 8. This track should be as short and wide as possible to minimize voltage drops. Also note from the figure that any other analog grounds in the signal path should be joined to the A/D converter analog ground.

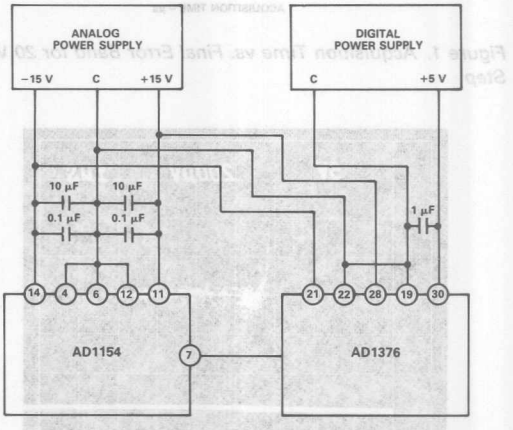


Figure 8. Basic Grounding and Power Supply Bypassing Practice

DIELECTRIC ABSORPTION COMPENSATION

The hold capacitor used in the AD1154 is a high quality ceramic chip capacitor. This capacitor's dielectric absorption characteristics are typically better than high quality film capacitors. In addition, the AD1154 provides a means for compensating for the dielectric absorption of the capacitor if better performance is required. If dielectric absorption compensation is not used, Pin 12 should be tied to ground. Please refer to the section titled "DISCUSSION OF DIELECTRIC ABSORPTION" for more detailed information.

POWER SUPPLY BYPASSING

The AD1154 utilizes high speed amplifiers in its design. These amplifiers require quiet power supplies that are free from spikes. For maximum performance it is recommended that both power supplies be bypassed with 0.1 µF ceramic capacitors in parallel with 10 µF tantalum capacitors located as close to the device as possible (see Figure 8).

DISCUSSION OF DIELECTRIC ABSORPTION

The hold capacitor of the AD1154 was chosen for its low dielectric absorption (D.A.) characteristics. D.A. is directly affected by the sample/hold mode switching durations and input levels. The AD1154 provides the user with a pin for external D.A. compensation circuitry. The AD1154's uncompensated D.A. performance is inherently superior, and in most applications the D.A. compensation pin should be connected to ground. Where additional compensation is desired to tailor the AD1154 to a specific user's application, only three resistors and a capacitor are required to optimize the AD1154's D.A. performance (see Figure 11).

If a capacitor is charged to a voltage, discharged for a moderate period of time, and then open circuited, the voltage on the capacitor will begin to creep back towards its initial value. This creep voltage is known as dielectric absorption. Dielectric absorption occurs because the dielectric material doesn't polarize instantly, the molecules need time to align themselves. As a result, not all of the energy stored in a capacitor can be quickly recovered upon discharge.

A first order model of the hold capacitor to include dielectric absorption effects is shown in Figure 9. In addition to the main capacitance, C_M, and the insulation resistance, R_I, there is an

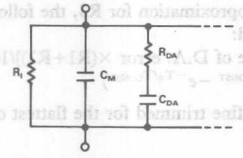


Figure 9. First Order Model of D. A. Effects

R_{DA} and a C_{DA}. When the capacitor is charged to some value, C_{DA} is also charged. When the capacitor is discharged, C_{DA} also discharges. But it must discharge through R_{DA}, and, if the capacitor is not discharged for a long enough period of time, C_{DA} will not completely discharge. As a result, when the capacitor is open circuited, C_{DA} will discharge into C_M causing the voltage across it to creep back towards its initial value. The actual model of the capacitor should contain additional R_{DA}s and C_{DA}s with increasing time constants in parallel with the one shown.

Figure 10 shows a circuit suitable for measuring the dielectric absorption of sample/hold amplifiers. The circuit operates as follows: R1 and C1 set the frequency of the SHA control; R2 and C2 set the amount of acquisition time allowed for the SHA. See the timing diagram of Figure 10.

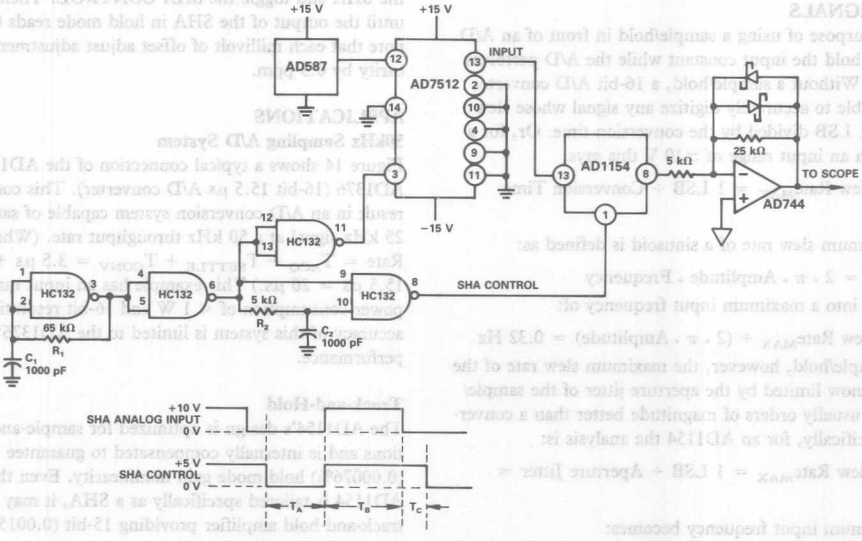


Figure 10. Dielectric Absorption Measurement Circuit

During T_B, the CONTROL line is high, the AD1154 is in the sample mode and the analog input charges the hold capacitor to +10 V. During T_C the analog input to the SHA is switched to ground, effectively shorting the hold capacitor for the remainder of the sample period. During T_A, the SHA is switched into hold mode and the hold capacitor is open circuited. The dielectric rebound can be observed on the oscilloscope during T_A. Refer to Figure 12.

Note that the dielectric absorption error is dependent on several factors: it is a function of how long the capacitor is charged (T_B), how long it is discharged (T_C) and how long it is observed while open circuited (T_A). These parameters can be modified by changing R1, R2, C1 and C2.

The AD1154 provides a pin to compensate for dielectric absorption. To use it, the circuit of Figure 11 must be employed.

To find the optimum values for R1, R2, R3 and C1 follow this procedure:

1. Adjust the D.A. measurement circuit (see Figure 10) to represent a typical sampling rate.
2. Observe the dielectric absorption error on the oscilloscope.
3. Pick (R1||R2) • C1 to be equal to the approximate time constant (T_{const}) of the dielectric rebound on the oscilloscope (see photo in Figure 12).

4. R3 is used to adjust the magnitude of the compensation. To find an initial approximation for R3, the following relationship can be used:
   $R3 = [\text{Magnitude of D.A. error} \times (R1+R2)]/10 \times 1/(e^{-T_C/T_{CONST}} - e^{-T_A/T_{CONST}})$
5. R3 can then be fine trimmed for the flattest output during hold.

Using this method it is possible to reduce the effect of dielectric absorption by a factor of four or five. The typical values for resistors and capacitor given in Figure 11 are for a sample time of 20 μs, acquisition time of 5 μs and a hold time of 20 μs. When determining the values, R3 should be less than 10 Ω, and C1 should be as small as possible.

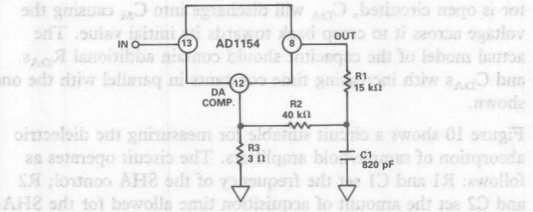


Figure 11. D/A Compensation Circuit with Typical Values

DYNAMIC SIGNALS

The primary purpose of using a sample/hold in front of an A/D converter is to hold the input constant while the A/D performs its conversion. Without a sample/hold, a 16-bit A/D converter would not be able to accurately digitize any signal whose slew rate exceeded 1 LSB divided by the conversion time. Or, for a 15 μs A/D with an input range of ±10 V this says:

$\text{Input Signal Slew Rate}_{MAX}$ = 1 LSB ÷ Conversion Time
= 20.3 V/S

Since the maximum slew rate of a sinusoid is defined as:

$\text{Slew Rate}_{MAX} = 2 \cdot \pi \cdot \text{Amplitude} \cdot \text{Frequency}$

This translates into a maximum input frequency of:

$F_{IN\ MAX}$ = $\text{Slew Rate}_{MAX} \div (2 \cdot \pi \cdot \text{Amplitude})$ = 0.32 Hz

By using a sample/hold, however, the maximum slew rate of the input signal is now limited by the aperture jitter of the sample/hold, which is usually orders of magnitude better than a conversion time. Specifically, for an AD1154 the analysis is:

$\text{Input Signal Slew Rate}_{MAX}$ = 1 LSB ÷ Aperture Jitter = 2.035 V/μs.

Now the maximum input frequency becomes:

$F_{IN\ MAX}$ = $\text{Slew Rate}_{MAX} \div (2 \cdot \pi \cdot \text{Amplitude})$ = 32.4 kHz.

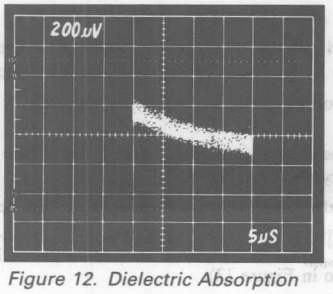


Figure 12. Dielectric Absorption

This represents a dramatic improvement over using the A/D converter by itself. The AD1154's 222 kHz throughput ($1/(T_{ACQ} + T_{SETT})$) and 150 ps aperture jitter allow it to digitize input signals of up to 32 kHz to 16-bit accuracy or up to a 128 kHz signal to 14-bits.

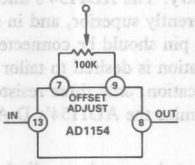


Figure 13. Offset Adjust Circuit

OPERATING INSTRUCTIONS

Offset Adjust

In most data acquisition systems only one offset adjustment is made. Usually the offset adjust of the A/D converter is used to null the combined system offsets. However, the offset or pedestal of the AD1154 can be nulled by connecting a trim potentiometer between Pins 7 and 9, and tying the wiper to +15 V (refer to Figure 13.) To null the pedestal, ground the input of the SHA and toggle the SHA CONTROL. Then adjust the pot until the output of the SHA in hold mode reads 0 V. Please note that each millivolt of offset adjust adjustment degrades linearity by 0.3 ppm.

APPLICATIONS

50kHz Sampling A/D System

Figure 14 shows a typical connection of the AD1154 to the AD1376 (16-bit 15.5 μs A/D converter). This combination will result in an A/D conversion system capable of sampling a 25 kHz signal at a 50 kHz throughput rate. (Where Throughput Rate = $T_{ACQ} + T_{SETTLE} + T_{CONV}$ = 3.5 μs + 1 μs + 15.5 μs = 20 μs.) This example has an input range of ±10 V, power consumption of < 1 W and 16-bit resolution. The accuracy of this system is limited to the AD1376's 14-bit performance.

Track-and-Hold

The AD1154's design is optimized for sample-and-hold applications and is internally compensated to guarantee 16-bit (0.00076%) hold mode gain nonlinearity. Even though the AD1154 is tailored specifically as a SHA, it may be used as a track-and-hold amplifier providing 15-bit (0.0015%) track mode gain nonlinearity.

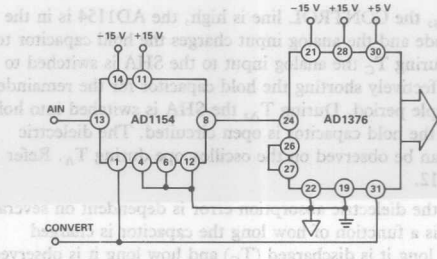


Figure 14. 50 kHz Sampling A/D Conversion System

Ultrahigh Speed Monolithic Track-and-Hold

AD9100*

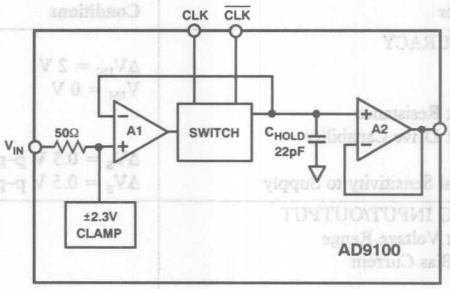
FEATURES

Excellent Hold Mode Distortion
−88 dB @ 30 MSPS (2.3 MHz V_{IN})
−83 dB @ 30 MSPS (12.1 MHz V_{IN})
−74 dB @ 30 MSPS (19.7 MHz V_{IN})
16 ns Acquisition Time to 0.01%
<1 ps Aperture Jitter
250 MHz Tracking Bandwidth
83 dB Feedthrough Rejection @ 20 MHz
3.3 nV/$\sqrt{Hz}$ Spectral Noise Density

APPLICATIONS

A/D Conversion
Direct IF Sampling
Imaging/FLIR Systems
Peak Detectors
Radar/EW/ECM
Spectrum Analysis
CCD ATE

FUNCTIONAL BLOCK DIAGRAM



4

GENERAL DESCRIPTION

The AD9100 is a monolithic track-and-hold amplifier which sets a new standard for high speed and high dynamic range applications. It is fabricated in a mature high speed complementary bipolar process. In addition to innovative design topologies, a custom package is utilized to minimize parasitics and optimize dynamic performance.

Acquisition time (hold to track) is 13 ns to 0.1% accuracy, and 16 ns to 0.01%. The AD9100 boasts superlative hold-mode frequency domain performance; when sampling at 30 MSPS hold mode distortion is less than −83 dBfs for analog frequencies up to 12 MHz; and −74 dBfs at 20 MHz. The AD9100 can also drive capacitive loads up to 100 pF with little degradation in acquisition time; it is therefore well suited to drive 8- and 10-bit flash converters at clock speeds to 50 MSPS. With a spectral noise density of 3.3 nV/$\sqrt{Hz}$ and feedthrough rejection of 83 dB at 20 MHz, the AD9100 is well suited to enhance the dynamic range of many 8- to 16-bit systems.

*Patent pending.

The AD9100 is "user friendly" and easy to apply: (1) it requires +5 V/−5.2 V power supplies; (2) the hold capacitor and switch power supply decoupling capacitors are built into the DIP package; (3) the encode clock is differential ECL to minimize clock jitter; (4) the input resistance is typically 800 kΩ; (5) the analog input is internally clamped to prevent damage from voltage transients.

The AD9100 is available in a 20-lead side-brazed "skinny DIP" package. Commercial, industrial, and military temperature grade parts are available. Consult the factory for information about the availability of surface mount packages and 883-qualified devices.

PRODUCT HIGHLIGHTS

1. Hold Mode Distortion is guaranteed.
2. Monolithic construction.
3. Analog input is internally clamped to protect against overvoltage transients and ensure fast recovery.
4. Output is short circuit protected.
5. Drives capacitive loads to 100 pF.
6. Differential ECL clock inputs.

AD9100—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±6 V
Continuous Output Current . . . . . 70 mA
Analog Input Voltage[2] . . . . . ±5 V
Junction Temperature . . . . . +175°C
Storage Temperature . . . . . −65°C to +150°C
Lead Soldering Temperature (10 sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (unless otherwise noted, $+V_S = +5$ V; $-V_S = -5.2$ V; $R_{LOAD} = 100\ \Omega$; $R_{IN} = 50\ \Omega$)

Parameter	Conditions	Temp	Test Level	AD9100JD/AD/SD[3] Min	Typ	Max	Units
DC ACCURACY							
Gain	$\Delta V_{IN} = 2$ V	Full	VI	0.989	0.994		V/V
Offset	$V_{IN} = 0$ V	Full	VI	−5	±1	+5	mV
Output Resistance		25°C	V		0.4		Ω
Output Drive Capability		Full	VI	±40	±60		mA
PSRR	$\Delta V_S = 0.5$ V p–p	Full	VI	48	55		dB
Pedestal Sensitivity to Supply	$\Delta V_S = 0.5$ V p–p	Full	VI		0.9	3	mV/V
ANALOG INPUT/OUTPUT							
Output Voltage Range		Full	VI	+2	±2.2	−2	V
Input Bias Current		25°C	VI	−8	±3	+8	μA
		Full	VI	−16		+16	μA
Input Overdrive Current[4]	$V_{IN} = \pm 4$ V	25°C	V		±22		mA
Input Capacitance		25°C	V		1.2		pF
Input Resistance		25°C, T_{max}	VI	350	800		kΩ
		T_{min}	VI	200			kΩ
CLOCK/$\overline{\text{CLOCK}}$ INPUTS							
Input Bias Current	CL/$\overline{\text{CL}}$ = −1.0 V	Full	VI		4	5	mA
Input Low Voltage (V_{IL})		Full	VI	−1.8		−1.5	V
Input High Voltage (V_{IH})		Full	VI	−1.0		−0.8	V
TRACK MODE DYNAMICS							
Bandwidth (−3 dB)	$V_{OUT} \leq 0.4$ V p–p	Full	IV	150	250		MHz
Slew Rate	4-Volt Step	25°C	IV	550	850		V/μs
	4-Volt Step	T_{min}, T_{max}	IV	500	700		V/μs
Overdrive Recovery Time[4] (to 0.1%)	$V_{IN} = \pm 4$ V to 0 V	25°C	V		21		ns
2nd Harm. Dist. (20 MHz, 2 V p–p)		Full	V		−65		dBc
3rd Harm. Dist. (20 MHz, 2 V p–p)		Full	V		−75		dBc
Integrated Output Noise (1–200 MHz)		25°C	V		45		μV
RMS Spectral Noise @ 10 MHz		25°C	V		3.3		nV/$\sqrt{\text{Hz}}$
HOLD MODE DYNAMICS							
Worst Harmonic (2.3 MHz, 30 MSPS)	$V_{OUT} = 2$ V p–p	25°C	V		−83		dBfs
Worst Harmonic (12.1 MHz, 30 MSPS)	$V_{OUT} = 2$ V p–p	25°C	IV		−81	−72	dBfs
Worst Harmonic (12.1 MHz, 30 MSPS)	$V_{OUT} = 2$ V p–p	T_{max}	IV		−76	−70	dBfs
Worst Harmonic (12.1 MHz, 30 MSPS)	$V_{OUT} = 2$ V p–p	T_{min}	IV		−73	−68	dBfs
Worst Harmonic (19.7 MHz, 30 MSPS)	$V_{OUT} = 2$ V p–p	25°C	V		−74		dBfs
Hold Noise[5]		25°C	V		300 × t_H		V/s rms
Droop Rate[6]	$V_{IN} = 0$ V	25°C	VI		1	6	±mV/μs
		T_{min}	VI		7	40	±mV/μs
		T_{max}	VI		5	30	±mV/μs
Feedthrough Rejection (20 MHz)	$V_{IN} = 2$ V p–p	Full	V		83		dB
TRACK-TO-HOLD SWITCHING							
Aperture Delay		25°C	V		+800		ps
Aperture Jitter		25°C	V		<1		ps
Pedestal Offset	$V_{IN} = 0$ V	25°C	VI	−5	±1	+5	mV
		Full	VI	−10		+10	mV
Transient Amplitude	$V_{IN} = 0$ V	Full	V		±6		mV
Settling Time to 1 mV		Full	IV		7	10	ns
Glitch Product	$V_{IN} = 0$ V	25°C	V		15		pV-s
HOLD-TO-TRACK SWITCHING							
Acquisition Time to 0.1%	2 V Step	25°C	V		13		ns
Acquisition Time to 0.01%	2 V Step	Full	IV		16	23	ns
Acquisition Time to 0.01%	4 V Step	25°C	V		20		ns

Parameter	Conditions	Temp	Test Level	AD9100JD/AD/SD[3] Min	Typ	Max	Units
POWER SUPPLY							
Power Dissipation		Full	VI		1.05	1.25	W
$+V_S$ Current		Full	VI		96	118	mA
$-V_S$ Current		Full	VI		116	132	mA

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Analog input voltage should not exceed $\pm V_S$.
[3]The "Full" temperature specifications refer to the ambient temperature for the DIP package only after a power soak. AD9100JD: 0°C to +70°C. AD9100AD: −40°C to +85°C. AD9100SD: −55°C to +125°C. θ_{JA} = 38°C/W; this is valid with the device mounted flush to a grounded 2-oz copper clad board with 16 sq. inches of surface area and no air flow.
[4]The input to the AD9100 is internally clamped at ±2.3 V. The internal input series resistance is nominally 50 Ω.
[5]Hold mode noise is proportional to the length of time a signal is held. For example, if the hold time (t_H) is 20 ns, the accumulated noise is typically 6 μV (300 V/s × 20 ns). This value must be combined with the track mode noise to obtain total noise.
[6]Min and max droop rates are based on the military temperature range (−55°C to +125°C). Refer to the "Droop Rate vs Temperature" chart for min/max limits over the commercial and industrial ranges.
Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Periodically sample tested.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
AD9100JD	0°C to +70°C	D-20
AD9100AD	−40°C to +85°C	D-20
AD9100SD	−55°C to +125°C	D-20

NOTES
[1]Consult factory about availability of parts in LCC packages, as well as parts screened to MIL-STD-883.
[2]D = Ceramic DIP. For outline information see Package Information section.

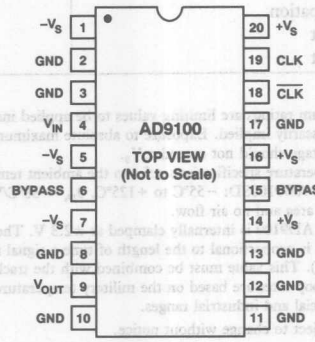
DIP PIN DESCRIPTIONS/CONNECTIONS

Pin No.	Description	Connection
1	$-V_S$	−5.2 V Power Supply
2	GND	Common Ground Plane
3	GND	Common Ground Plane
4	V_{IN}	Analog Input Signal
5	$-V_S$	−5.2 V Power Supply
6	BYPASS	0.1 μF to Ground
7	$-V_S$	−5.2 V Power Supply
8	GND	Common Ground Plane
9	V_{OUT}	Track-and-Hold Output
10	GND	Common Ground Plane
11	GND	Common Ground Plane
12	GND	Common Ground Plane
13	GND	Common Ground Plane
14	$+V_S$	+5 V, Power Supply
15	BYPASS	0.1 μF to Ground
16	$+V_S$	+5 V, Power Supply
17	GND	Common Ground Plane
18	$\overline{CLK}$	Complement ECL Clock
19	CLK	"True" ECL Clock
20	$+V_S$	+5 V Power Supply

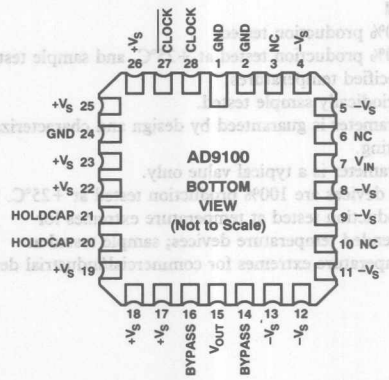
LCC PIN DESCRIPTIONS/CONNECTIONS

Pin No.	Description	Connection
1	GND	Common Ground Plane
2	GND	Common Ground Plane
3	NC	None
4	$-V_S$	−5.2 V Power Supply
5	$-V_S$	−5.2 V Power Supply
6	NC	None
7	V_{IN}	Analog Input Supply
8	$-V_S$	−5.2 V Power Supply
9	$-V_S$	−5.2 V Power Supply
10	NC	None
11	$-V_S$	−5.2 V Power Supply
12	$-V_S$	−5.2 V Power Supply
13	$-V_S$	−5.2 V Power Supply
14	BYPASS	0.1 μF to Pin 16
15	V_{OUT}	Track-and-Hold Output
16	BYPASS	0.1 μF to Pin 14
17	$+V_S$	+5 V Power Supply
18	$+V_S$	+5 V Power Supply
19	$+V_S$	+5 V Power Supply
20	HOLDCAP	External Hold Capacitor
21	HOLDCAP	External Hold Capacitor
22	$+V_S$	+5 V Power Supply
23	$+V_S$	+5 V Power Supply
24	GND	Common Ground Plane
25	$+V_S$	+5 V Power Supply
26	$+V_S$	+5 V Power Supply
27	$\overline{CLOCK}$	Complement ECL Clock
28	CLOCK	"True" ECL Clock

DIP PINOUTS



LCC PINOUTS



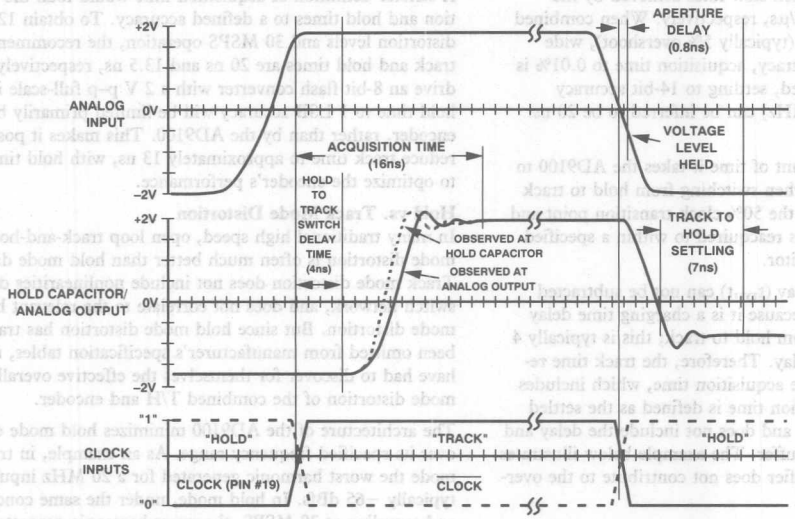
Acquisition Time is the amount of time it takes the AD9100 to reacquire the analog input when switching from hold to track mode. The interval starts at the 50% clock transition point and ends when the input signal is reacquired to within a specified error band at the hold capacitor.

Analog Delay is the time required for an analog input signal to propagate from the device input to output.

Aperture Delay tells when the input signal is actually sampled. It is the time difference between the analog propagation delay of the front-end buffer and the control switch delay time. (The time from the hold command transition to when the switch is opened.) For the AD9100, this is a positive value which means that the switch delay is longer than the analog delay.

Aperture Jitter is the random variation in the aperture delay. This is measured in ps-rms and results in phase noise on the held signal.

Droop Rate is the change in output voltage as a function of time (dV/dt). It is measured at the AD9100 output with the device in hold mode and the input held at a specified dc value; the measurement starts immediately after the T/H switches from track to hold.



AD9100 Timing Diagram

Feedthrough Rejection is the ratio of the input signal to the output signal when in hold mode. This is a measure of how well the switch isolates the input signal from feeding through to the output.

Hold to Track Switch Delay is the time delay from the track command to the point when the output starts to change and acquire a new signal.

Pedestal Offset is the offset voltage step measured immediately after the AD9100 is switched from track to hold with the input held at zero volts. It manifests itself as an added offset during the hold time.

Track to Hold Settling Time is the time necessary for the track to hold switching transient to settle to within 1 mV of its final value.

Track to Hold Switching Transient is the maximum peak switch induced transient voltage which appears at the AD9100 output when it is switched from track to hold.

THEORY OF OPERATION

The AD9100 utilizes a new track and hold architecture. Previous commercially available high speed track and holds used a front end open loop input buffer, followed by a diode bridge, hold capacitor, and output buffer (closed or open loop) with a FET device connected to the hold capacitor. This architecture required mixed device technology and, usually, hybrid construction. The sampling rate of these hybrids has been limited to 20 MSPS for 12-bit accuracy. Distortion generated in the front-end amplifier/bridge limited the dynamic range performance to the "mid-70 dBfs" for analog input signals of less than 10 MHz. Broadband and switch-generated noise limited the SNR of previous track and holds to about 70 dB.

The AD9100 is a monolithic device using a high frequency complementary bipolar process to achieve new levels of high speed precision. Its patent pending architecture breaks from the traditional architecture described above. (See the block diagram on the first page.) The switching type bridge has been integrated into the first stage closed loop input amplifier. This innovation provides error (distortion) correction for both the switch and amplifier, while still achieving slew rates representative of an open-loop design. In addition, acquisition slew current for the hold capacitor is higher than standard diode bridge and switch configurations, removing a main contributor to the limits of maximum sampling rate and input frequency.

Switching circuits in the device use current steering (versus voltage switching) to provide improved isolation between the switch and analog sections. This results in low aperture time sensitivity to the analog input signal, and reduced power supply and analog switching noise. Track to hold peak switching transient is typically only 6 mV and settles to less than 1 mV in 7 ns. In addition, pedestal sensitivity to analog input voltage is very low (0.6 mV/V) and being first order linear does not significantly affect distortion.

The closed-loop output buffer includes zero voltage bias current cancellation, which results in high-temperature droop rates equivalent to those found in FET type inputs. The buffer also provides first order quasistatic bias correction resulting in an extremely high input resistance and very low droop sensitivity vs. input voltage level (typically less than 1.5 mV/V−μs.) This closed-loop architecture inherently provides high speed loop correction and results in low distortion under heavy loads.

The extremely fast time constant linearity (7 ns to 0.01% for a 2 V step) ensures that the output buffer does not limit the AD9100 sampling rate or analog input frequency. (The acquisition and settling time are primarily limited only by the input amplifier and switch.) The output is transparent to the overall AD9100 hold mode distortion levels for loads as low as 250 Ω.

Full-scale track and acquisition slew rates achieved by the AD9100 are 800 and 1000 V/μs, respectively. When combined with excellent phase margin (typically 5% overshoot), wide bandwidth, and dc gain accuracy, acquisition time to 0.01% is only 16 ns. Though not tested, settling to 14-bit accuracy (−88 dB distortion @ 2.3 MHz) can be inferred to be 20 ns.

Acquisition Time

Acquisition time is the amount of time it takes the AD9100 to reacquire the analog input when switching from hold to track mode. The interval starts at the 50% clock transition point and ends when the input signal is reacquired to within a specified error band at the hold capacitor.

The hold to track switch delay ($t_{DH}t$) can not be subtracted from this acquisition time because it is a charging time delay that occurs when moving from hold to track; this is typically 4 to 6 ns and is the longest delay. Therefore, the track time required for the AD9100 is the acquisition time, which includes t_{DHT}. Note that the acquisition time is defined as the settled voltage at the hold capacitor and does not include the delay and settling time of the output buffer. The example below illustrates why the output buffer amplifier does not contribute to the overall AD9100 acquisition time.

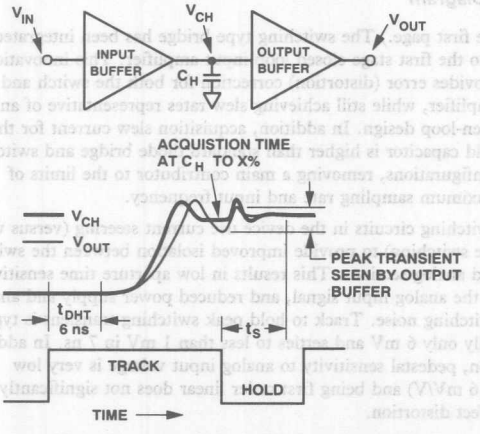


Figure 1. Acquisition Time Diagram

The exaggerated illustration in Figure 1 shows that V_{CH} has settled to within x% of its final value, but V_{OUT} (due to slew rate limitations, finite BW, power supply ringing, etc.) has not settled during the track time. However, since the output buffer always "tracks" the front end circuitry, it "catches up" during the hold time and directly superimposes itself (less about 600 ps of analog delay) to V_{CH}. Since the small-signal settling time of the output buffer is about 1.8 ns to ±1 mV and is significantly less than the specified hold time, acquisition time should be referenced to the hold capacitor.

Note that most of the hold settling time and output acquisition time are due to the input buffer and the switch network. For output acquisition time, the output buffer contributes only about 5 ns of the total; in hold mode, it contributes only 1.8 ns (as stated above).

A stricter definition of acquisition time would total the acquisition and hold times to a defined accuracy. To obtain 12 bit + distortion levels and 30 MSPS operation, the recommended track and hold times are 20 ns and 13.5 ns, respectively. To drive an 8-bit flash converter with a 2 V p–p full-scale input, hold time to 1 LSB accuracy will be limited primarily by the encoder, rather than by the AD9100. This makes it possible to reduce track time to approximately 13 ns, with hold time chosen to optimize the encoder's performance.

Hold vs. Track Mode Distortion

In many traditional high speed, open loop track-and-holds, track mode distortion is often much better than hold mode distortion. Track mode distortion does not include nonlinearities due to the switch network, and does not correlate to the relevant hold mode distortion. But since hold mode distortion has traditionally been omitted from manufacturer's specification tables, users have had to discover for themselves the effective overall hold mode distortion of the combined T/H and encoder.

The architecture of the AD9100 minimizes hold mode distortion over its specified frequency range. As an example, in track mode the worst harmonic generated for a 20 MHz input tone is typically −65 dBfs. In hold mode, under the same conditions and sampling at 30 MSPS, the worst harmonic generated is −74 dBfs. The reason is the output buffer in hold mode has only dc distortion relevancy. With its inherent linearity (7 ns settling to 0.01%), the output buffer has essentially settled to its dc distortion level even for track plus hold times as short as 30 ns. For a traditional open-loop output buffer, the ac (track mode) and dc (hold mode) distortion levels are often the same.

Droop Rate

Droop rate does not necessarily affect a track and hold's distortion characteristics. If the droop rate is constant versus the input voltage for a given hold time, it manifests itself as a dc offset to the encoder. For the AD9100, the droop rate is typically ±1 mV/μs. If a signal is held for 1 μs, a subsequent encoder would see a 1 mV offset voltage. If there is no droop sensitivity to the held voltage value, the 1 mV offset would be constant and "ride" on the input signal and introduce no hold-mode nonlinearities.

In instances in which droop rate varies proportionately to the magnitude of the held voltage signal level, a gain error only is introduced to the A/D encoder. The AD9100 has a droop sensitivity to the input level of 1.5 mV/V−μsec. For a 2 V p–p input signal, this translates to a 0.15%/μs gain error and does not cause additional distortion errors.

For the AD9100, droop sensitivity to input level is insignificant. However, *hold times longer than about 2 μs can cause distortion* due to the R × C_H time constant at the hold capacitor. In addition, hold mode noise will increase linearly vs. hold time and thus degrade SNR performance.

Layout Considerations

For best performance results, good high speed design techniques must be applied. The component (top) side ground plane should be as large as possible; two-ounce copper cladding is preferable. All runs should be as short as possible, and decoupling capacitors must be used.

Figure 2 is the schematic of a recommended AD9100 evaluation board. (Contact factory concerning availability of assembled boards.) All 0.01 μF decoupling capacitors should be low induc-

tance surface mount devices (P/N 05085C103MT050 from AVX) and connected on the component side within 30 mils of the designated pins; with the other sides soldered directly to the top ground plane.

The 10 μF low frequency power supply tantalum decoupling capacitors should be located within 1.5 inches of the AD9100. The common 0.01 μF supply capacitors can be wired together. The common power supply bus (connected to the 10 μF capacitor and power supply source) can be routed to the underside of the board to the daisy chain wired 0.01 μF supply capacitors.

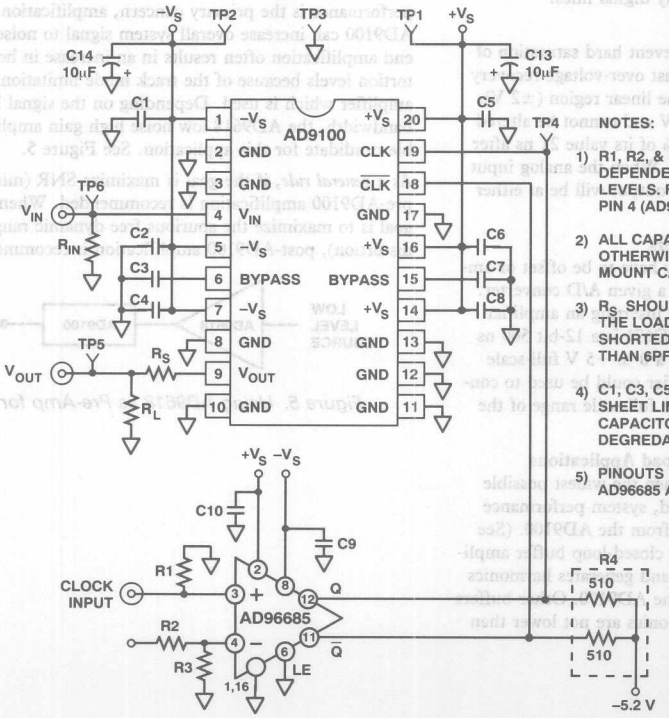
For remote input and/or output drive applications, controlled impedances are required to minimize line reflections which will reduce signal fidelity. When capacitive and/or high impedance levels are present, the load and/or source should be physically located within approximately one inch of the AD9100. Note that a series resistance, R_S, is required if the load is greater than 6 pF. (The Recommended R_S vs. CL chart in the "Typical Performance Section" shows values of R_S for various capacitive loads which result in no more than a 20% increase in settling time for loads up to 80 pF.) As much of the ground plane as possible should be removed from around the V_{IN} and V_{OUT} pins to minimize coupling onto the analog signal path.

While a single ground plane is recommended, the analog signal and differential ECL clock ground currents follow a narrow path directly under their common voltage signal line. To reduce reflections, especially when terminations are used for transmission line efficiency, the clock, V_{IN}, and V_{OUT} signals and respective ground paths should not cross each other; if they do, unwanted coupling can result.

High current ground transients via the high frequency decoupling capacitors can also cause unwanted coupling to the V_{IN} and V_{OUT} current loops. Therefore, these analog terminations should be kept as far as possible from the power supply decoupling capacitors to minimize feedthrough.

Using Sockets

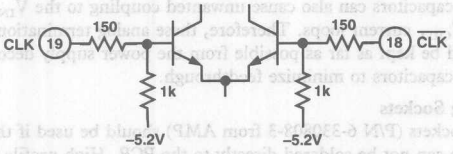
Pin sockets (P/N 6-330808-3 from AMP) should be used if the device can not be soldered directly to the PCB. High profile or wire wrap type sockets will dramatically reduce the dynamic performance of the device in addition to increasing the case-to-ambient thermal resistance.



Driving the Encode Clock

The AD9100 requires a differential ECL clock command. Due to the high gain bandwidth of the AD9100 internal switch, the input clock should have a slew rate of at least 100 V/μs.

To obtain maximum signal to noise performance, especially at high analog input frequencies, a low jitter clock source is required. The AD9100 clock can be driven by an AD96685, an ultrahigh speed ECL comparator with very low jitter.



Clock/$\overline{\text{Clock}}$ Input Stage

Driving the Analog Input

Special care must be taken to ensure that the analog input signal is not compromised before it reaches the AD9100. To obtain maximum signal to noise performance, a very low phase noise analog source is required. In addition, input filtering and/or a low harmonic signal source is necessary to maximize the spurious free dynamic range. Any required filtering should be done close to the AD9100 and away from any digital lines.

Overdriving the Analog Input

The AD9100 has input clamps that prevent hard saturation of the output buffer, thereby providing fast over-voltage recovery when the analog input transitions to the linear region (±2 V). The clamps are set internally at ±2.3 V and cannot be altered by the user. The output settles to 0.1% of its value 21 ns after the over-voltage condition is alleviated. When the analog input is outside the linear region, the analog output will be at either +2.2 V or −2.2 V.

Matching the AD9100 to A/D Encoders

The AD9100's analog output level may have to be offset or amplified to match the full-scale range of a given A/D converter. This can generally be accomplished by inserting an amplifier after the AD9100. For example, the AD671 is a 12-bit 500 ns monolithic ADC encoder that requires a 0 to +5 V full-scale analog input. An AD84X series amplifier could be used to condition the AD9100 output to match the full-scale range of the AD671.

Ultralow Distortion/Low Resistive Load Applications

When driving low resistive loads or when the widest possible spurious free dynamic range is required, system performance can be improved by isolating the load from the AD9100. (See Figure 3.) The AD9620 low distortion closed-loop buffer amplifier has an input resistance of 800 kΩ and generates harmonics that are less than those generated by the AD9100. Other buffers should not be considered if their harmonics are not lower than those of the AD9100.

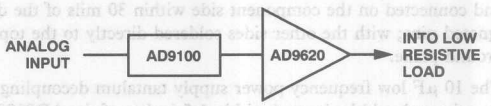


Figure 3. Using AD9620 as Isolation Amplifier

Super Nyquist Signals/Low Distortion

The AD9100 can be used to sample super-Nyquist signals, making high fidelity direct IF sampling practical. For applications in which the analog input signal is >20 MHz, some improvement in system level performance may be achieved if the analog input to the AD9100 is reduced, then gained up at the output by a low distortion amplifier such as the AD9617. See Figure 4.

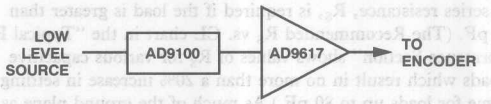


Figure 4. Using AD9617 as Post-Amp for AD9100

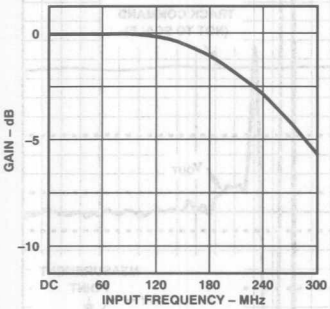
Low Noise Applications

When processing low level single event signals in which noise performance is the primary concern, amplification ahead of the AD9100 can increase overall system signal to noise ratio. Front-end amplification often results in an increase in hold mode distortion levels because of the track mode limitations of the amplifier which is used. Depending on the signal levels and bandwidth, the AD9618 low noise high gain amplifier is a possible candidate for this application. See Figure 5.

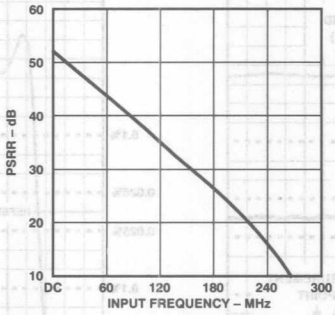
As a general rule, if the goal is maximize SNR (minimize noise), pre-AD9100 amplification is recommended. When the system goal is to maximize the spurious free dynamic range (minimize distortion), post-AD9100 amplification is recommended.



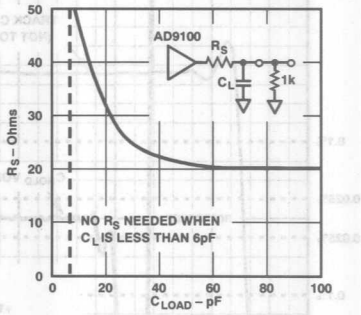
Figure 5. Using AD9618 as Pre-Amp for AD9100



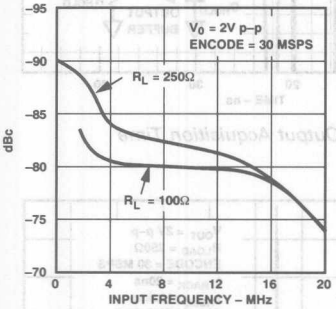
Gain vs. Frequency (Track Mode)



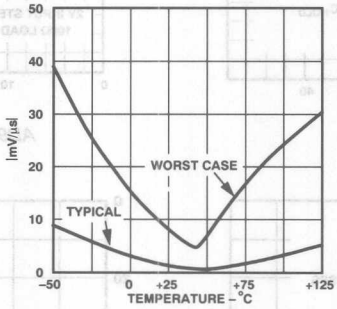
Power Supply Rejection Ratio vs. Frequency



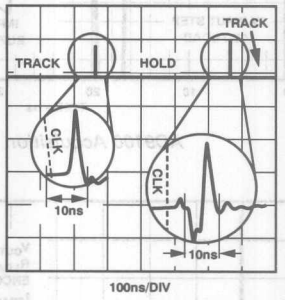
Recommended R_S vs. C_{LOAD} for Optimal Settling Times



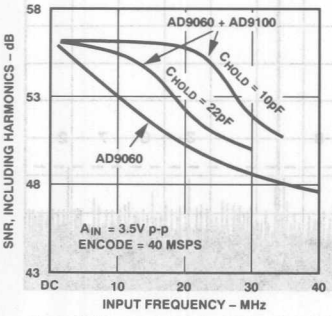
Worst Hold Mode Harmonic vs. Analog Input Frequency



Magnitude of Droop Rate vs. Temperature



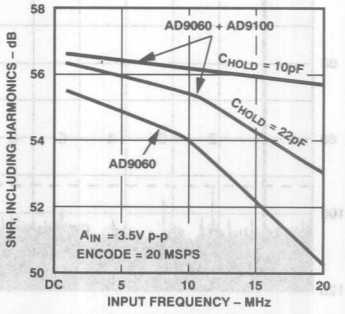
Track-to-Hold-to-Track Switch Transients



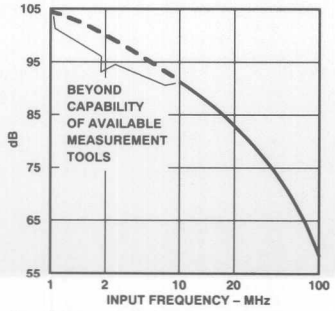
SNR vs. Analog Input



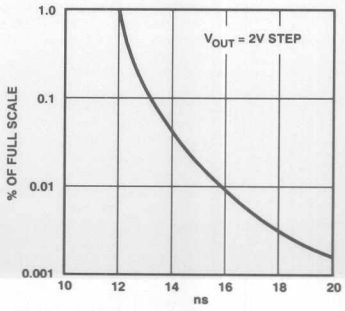
THE AD9060 IS A 10-BIT, 75MSPS MONOLITHIC ADC FROM ANALOG DEVICES.
* THE AD9100XD (DIP) HAS AN INTERNAL 22pF HOLD CAPACITOR. CONTACT FACTORY REGARDING AVAILABILITY OF AD9100 IN A 28-PIN LEADED CHIP CARRIER PACKAGE WITH EXTERNAL HOLD CAPACITOR.



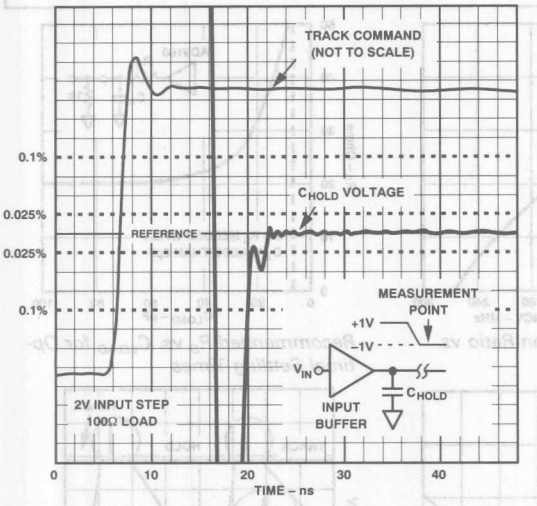
SNR vs. Analog Input



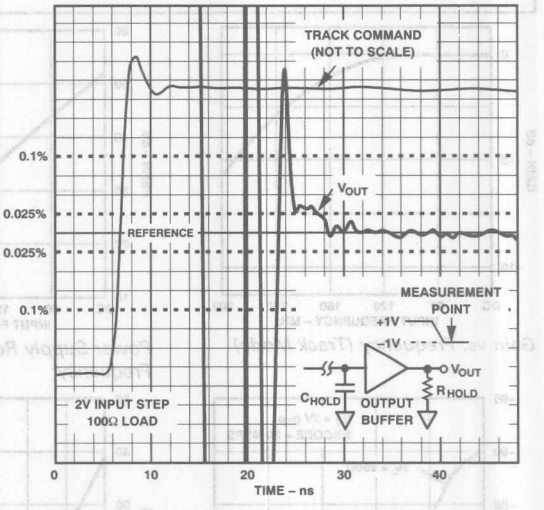
Feedthrough Rejection vs. Input Frequency



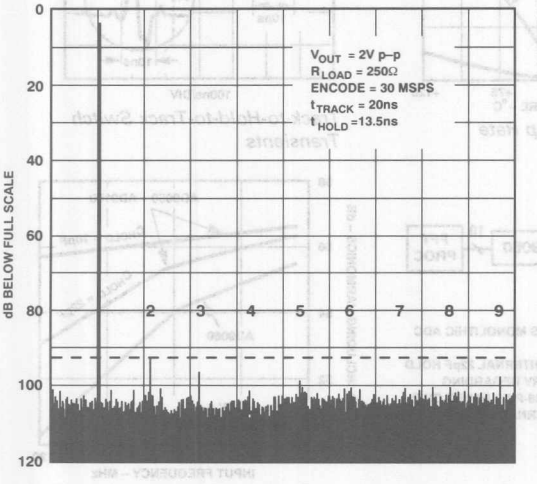
Settling Tolerance vs. Acquisition Time



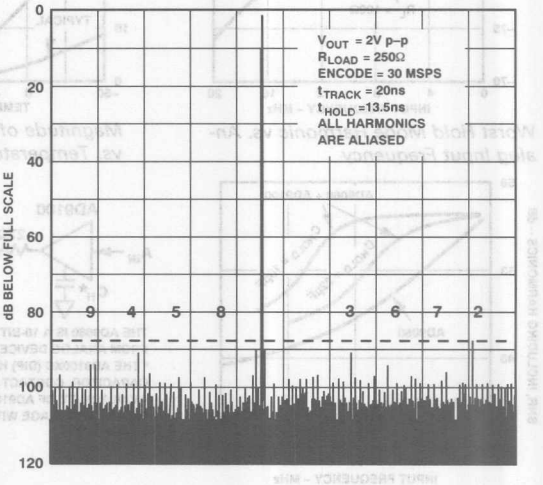
AD9100 Acquisition Time



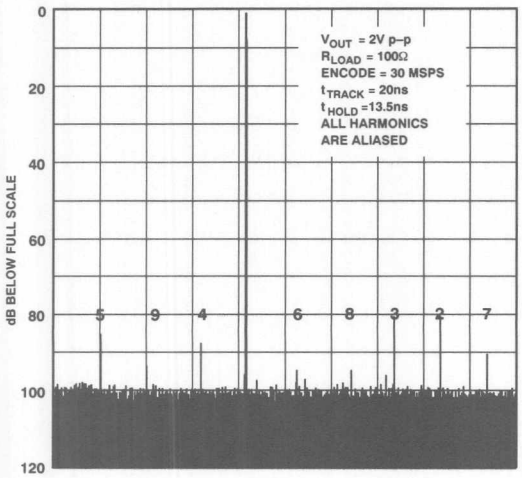
AD9100 Output Acquisition Time



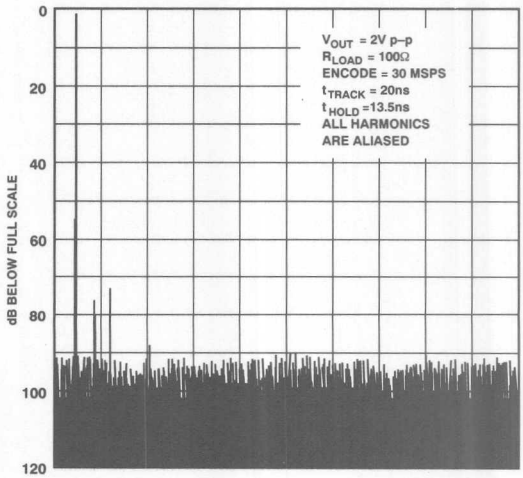
Frequency (500 kHz/Division) Analog Input = 540 kHz



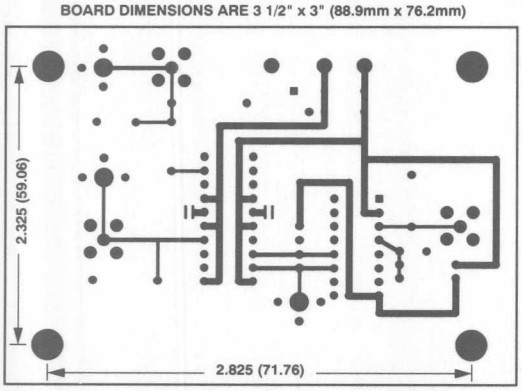
Frequency (500 kHz/Division) Analog Input = 2.3 MHz



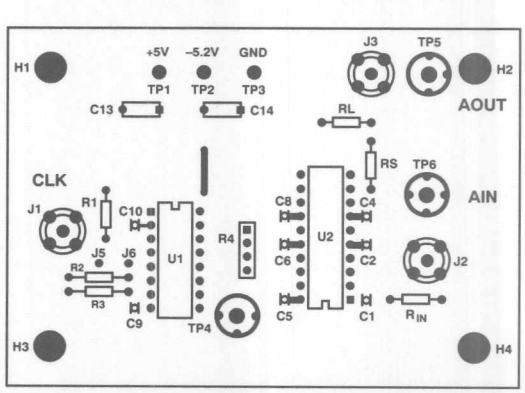
Frequency (500 kHz/Division) Analog Input = 12.1 MHz



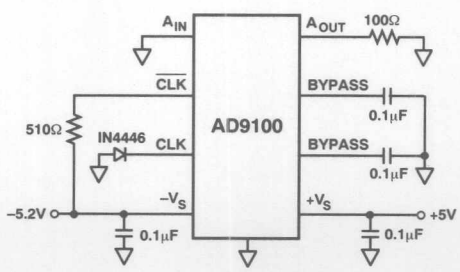
Frequency (500 kHz/Division) Analog Input = 19.8 MHz



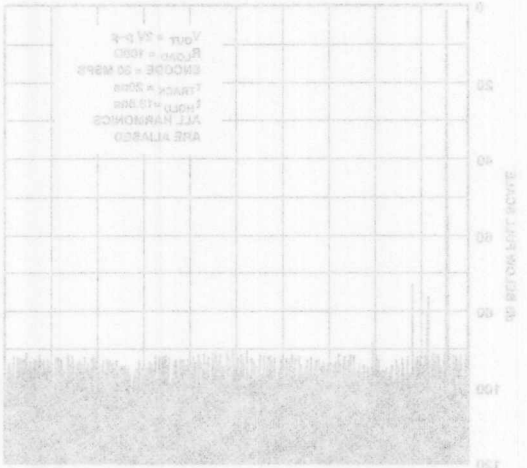
AD9100 Evaluation Board (Solder Side Viewed from Bottom)

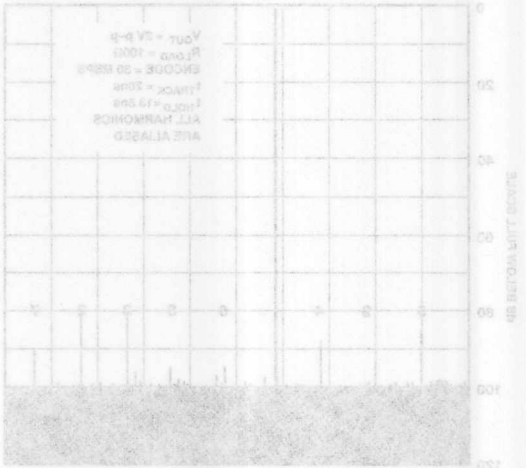


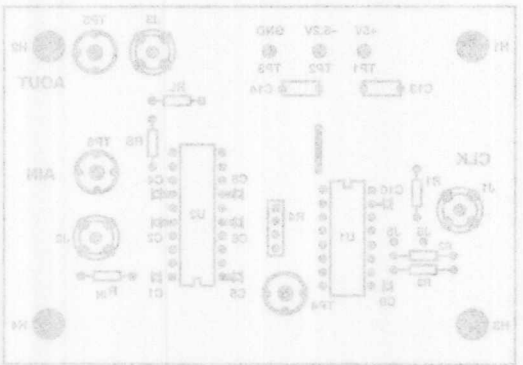
AD9100 Evaluation Board (Component Side Viewed from Top)

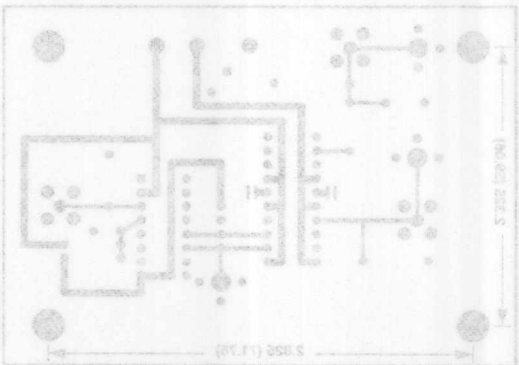


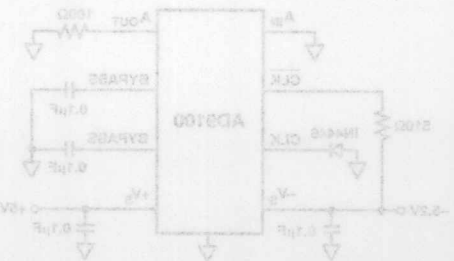
AD9100 Burn-in Circuit











CMOS Quad Sample-and-Hold Amplifier

SMP-04

FEATURES

- **Four Independent Sample-and-Holds**
- **Internal Hold Capacitors**
- **High Accuracy – 12-Bit**
- **Very Low Droop Rate (2mV/s Typ)**
- **Output Buffers Stable for $C_L \leq 500pF$**
- **TTL/CMOS Compatible Logic Inputs**
- **Single or Dual Supply Applications**
- **Monolithic Low Power CMOS Design**

APPLICATIONS

- **Signal Processing Systems**
- **Multichannel Data Acquisition Systems**
- **Automatic Test Equipment**
- **Medical and Analytical Instrumentation**
- **Event Analysis**
- **DAC Deglitching**

ORDERING INFORMATION †

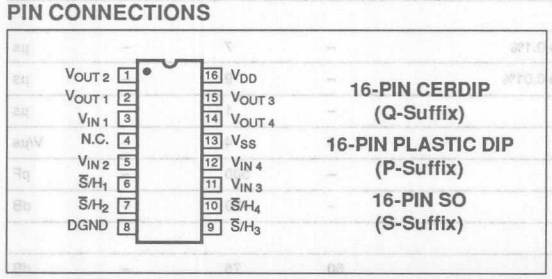
PACKAGE		OPERATING TEMPERATURE RANGE
PLASTIC 16-PIN	CERDIP 16-PIN	
—	SMP04AQ/883*	MIL
SMP04EP	SMP04EQ	XIND
SMP04ES††	—	XIND

* Consult factory for 883 data sheet.

† Burn-in is available on extended industrial temperature range parts in CerDIP and plastic DIP packages.

†† For availability and burn-in information on SO packages, contact your local sales office.

PIN CONNECTIONS



16-PIN CERDIP (Q-Suffix)

16-PIN PLASTIC DIP (P-Suffix)

16-PIN SO (S-Suffix)

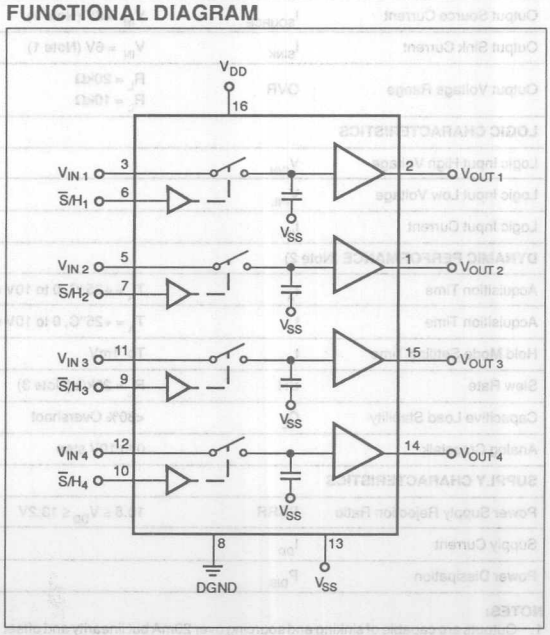
GENERAL DESCRIPTION

The SMP-04 is a monolithic quad sample-and-hold; it has four internal precision buffer amplifiers and internal hold capacitors. It is manufactured in PMI's advanced oxide isolated CMOS technology to obtain high accuracy, low droop rate and fast acquisition time required by data acquisition and signal processing systems. The device can acquire an 8-bit input signal to ±1/2 LSB in less than seven microseconds. The SMP-04 can operate from single or dual power supplies with TTL/CMOS logic compatibility. Its output swing includes the negative supply.

The SMP-04 is ideally suited for a wide variety of sample-and-hold applications including amplifier offset or VCA gain adjustments. One or more can be used with a single or multiple DACs to provide multiple set points within a system.

The SMP-04 offers significant cost and size reduction over equivalent module or discrete designs. It is available in a 16-pin hermetic or plastic DIP and surface mount SOIC packages. It is specified over the extended industrial temperature range of –40°C to +85°C. See SMP-04/883 data sheet for –55°C to +125°C specifications.

FUNCTIONAL DIAGRAM



Manufactured under the following U.S. patent: 4,739,281

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

V_{DD} to DGND ..... –0.3V, 17V
V_{DD} to V_{SS} ..... –0.7V, 17V
V_{LOGIC} to DGND ..... –0.3V, V_{DD}
V_{IN} to DGND ..... V_{SS}, V_{DD}
V_{OUT} to DGND ..... V_{SS}, V_{DD}
Analog Output Current ..... ±20mA
(Not short-circuit protected)
Digital Input Voltage to DGND ..... –0.3V, V_{DD} +0.3V
Operating Temperature Range
EQ, EP, ES ..... –40°C to +85°C
AQ ..... –55°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
16-Pin CerDIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SO (S)	92	27	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

CAUTION:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and function operation at or above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.
2. Digital inputs and outputs are protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam or packaging at all times until ready to use. Use proper anti-static handling procedures.
3. Remove power before inserting or removing units from their sockets.

ELECTRICAL CHARACTERISTICS at V_{DD} = +12.0V, V_{SS} = DGND = 0V, R_L = No Load, T_A = Operating Temperature Range specified in Absolute Maximum Ratings, unless otherwise specified.

			SMP-04			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Linearity Error			–	0.01	–	%
Buffer Offset Voltage	V_{OS}	V_{IN} = 6V	–10	±2.5	+10	mV
Hold Step	V_{HS}	V_{IN} = 6V	–	1	±4	mV
Droop Rate	ΔV/Δt	V_{IN} = 6V, T_A = +25°C	–	2	25	mV/s
Output Source Current	I_{SOURCE}	V_{IN} = 6V (Note 1)	1.2	–	–	mA
Output Sink Current	I_{SINK}	V_{IN} = 6V (Note 1)	0.5	–	–	mA
Output Voltage Range	OVR	R_L = 20kΩ R_L = 10kΩ	0.06 0.06	– –	10.0 9.5	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4	–	–	V
Logic Input Low Voltage	V_{INL}		–	–	0.8	V
Logic Input Current	I_{IN}		–	0.5	1	µA
DYNAMIC PERFORMANCE (Note 2)						
Acquisition Time	t_A	T_A = +25°C, 0 to 10V step to 0.1%	–	7	–	µs
Acquisition Time	t_A	T_A = +25°C, 0 to 10V step to 0.01%	–	9	–	µs
Hold Mode Settling Time	t_H	To 1mV	–	1	–	µs
Slew Rate	SR	R_L = 20kΩ (Note 3)	3	4	–	V/µs
Capacitive Load Stability	C_L	<30% Overshoot	–	500	–	pF
Analog Crosstalk		0 to 10V step	–	–80	–	dB
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	10.8 ≤ V_{DD} ≤ 13.2V	60	75	–	dB
Supply Current	I_{DD}		–	4	7	mA
Power Dissipation	P_{DIS}		–	–	84	mW

NOTES:
1. Outputs are capable of sinking and sourcing over 20mA but linearity and offset are guaranteed at specified load levels.
2. All input control signals are specified with $t_r = t_f$ = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
3. Slew rate is measured in the sample mode with a 0 to 10 volt step from 20 to 80%.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5.0V, V_{SS} = –5.0V, DGND = 0.0V, R_L = No Load, T_A = Operating Temperature Range specified in Absolute Maximum Ratings, unless otherwise specified.

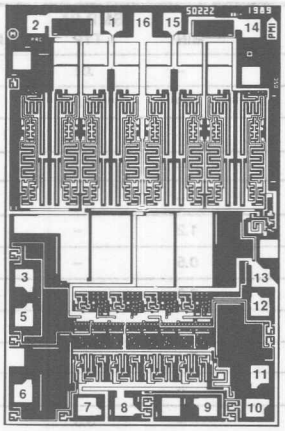
			SMP-04			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Linearity Error			–	.01	–	%
Buffer Offset Voltage	V_{OS}	V_{IN} = 0V	–10	±2.5	+10	mV
Hold Step	V_{HS}	V_{IN} = 0V	–	–1	±4	mV
Droop Rate	$\Delta V/\Delta t$	V_{IN} = 0V, T_A = +25°C	–	2	25	mV/s
Output Resistance	R_{OUT}		–	1	–	Ω
Output Source Current	I_{SOURCE}	V_{IN} = 0V (Note 1)	1.2	–	–	mA
Output Sink Current	I_{SINK}	V_{IN} = 0V (Note 1)	0.5	–	–	mA
Output Voltage Range	OVR	R_L = 20kΩ	–3.0	–	+3.0	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4	–	–	V
Logic Input Low Voltage	V_{INL}		–	–	0.8	V
Logic Input Current	I_{IN}		–	0.5	1	µA
DYNAMIC PERFORMANCE (Note 2)						
Acquisition Time	t_A	–3 to +3V step to 0.1%	–	7	–	µs
Acquisition Time	t_A	–3 to +3V step to 0.01%	–	9	–	µs
Hold Mode Settling Time	t_H	To 1mV	–	1	–	µs
Slew Rate	SR	R_L = 20kΩ (Note 3)	–	3	–	V/µs
Capacitive Load Stability	C_L	<30% Overshoot	500	–	–	pF
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	±5 ≤ V_{DD} ≤ ±6V	60	75	–	dB
Supply Current	I_{DD}		–	3.5	5.5	mA
Power Dissipation	P_{DIS}		–	–	55	mW

NOTES:

1. Outputs are capable of sinking and sourcing over 20mA but linearity and offset are guaranteed at specified load levels.
2. All input control signals are specified with $t_r = t_f$ = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
3. Slew rate is measured in the sample mode with a –3 to +3 volt step from 20 to 80%.

4

DICE CHARACTERISTICS



DIE SIZE 0.080 x 0.120 inch, 9,600 sq. mils
(2.032 x 3.048 mm, 6.193 sq. mm)

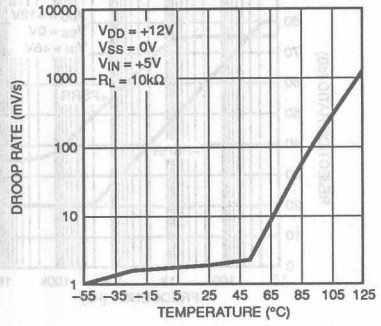
1. $V_{OUT\,2}$
2. $V_{OUT\,1}$
3. $V_{IN\,1}$
4. N.C.
5. $V_{IN\,2}$
6. S/H_1
7. S/H_2
8. DGND
9. S/H_3
10. S/H_4
11. $V_{IN\,3}$
12. $V_{IN\,4}$
13. V_{SS}
14. $V_{OUT\,4}$
15. $V_{OUT\,3}$
16. V_{DD}

WAFER TEST LIMITS at V_{DD} = +12.0V, V_{SS} = DGND = 0V, R_L = No Load, T_A = +25°C, unless otherwise specified.

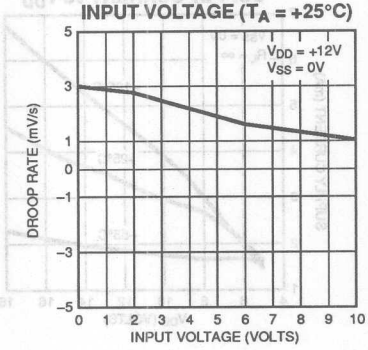
PARAMETER	SYMBOL	CONDITIONS	SMP-04G LIMITS	UNITS
Buffer Offset Voltage	V_{OS}	V_{IN} = 6V	±10	mV MAX
Hold Step	V_{HS}	V_{IN} = 6V	±4	mV MAX
Droop Rate	$\Delta V/\Delta t$	V_{IN} = 6V	25	mV/s MAX
Output Source Current	I_{SOURCE}	V_{IN} = 6V	1.2	mA MIN
Output Sink Current	I_{SINK}	V_{IN} = 6V	0.5	mA MIN
Output Voltage Range	OVR	R_L = 20kΩ R_L = 10kΩ	0.06/10.0 0.06/9.5	V MIN/MAX
LOGIC CHARACTERISTICS				
Logic Input High Voltage	V_{INH}		2.4	V MIN
Logic Input Low Voltage	V_{INL}		0.8	V MAX
Logic Input Current	I_{IN}		1	µA MAX
SUPPLY CHARACTERISTICS				
Power Supply Rejection Ratio	PSRR	$10.8 \le V_{DD} \le 13.2V$	60	dB MIN
Supply Current	I_{DD}		7	mA MAX
Power Dissipation	P_{DIS}		84	mW MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

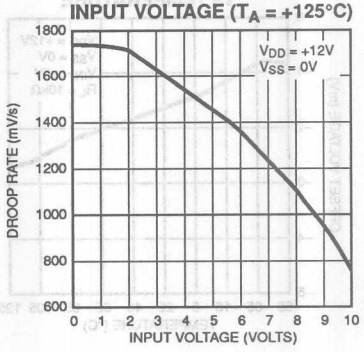
DROOP RATE vs TEMPERATURE



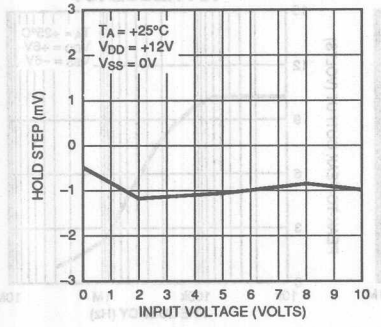
DROOP RATE vs INPUT VOLTAGE (T_A = +25°C)



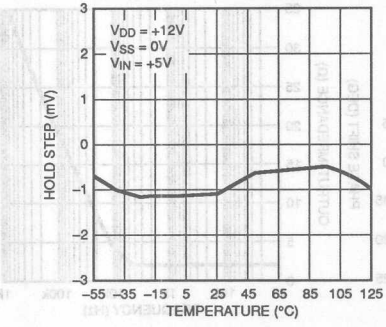
DROOP RATE vs INPUT VOLTAGE (T_A = +125°C)



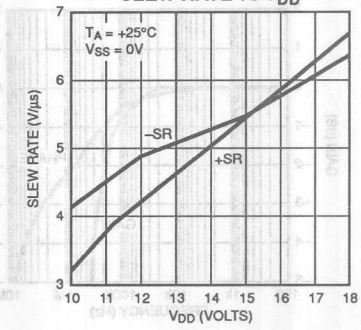
HOLD STEP vs INPUT VOLTAGE



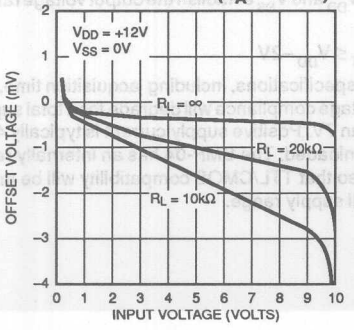
HOLD STEP vs TEMPERATURE



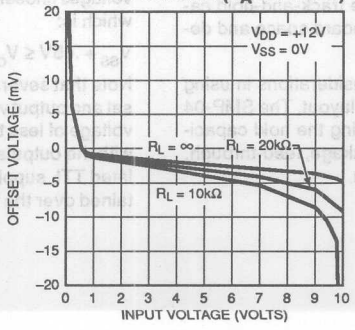
SLEW RATE vs V_{DD}



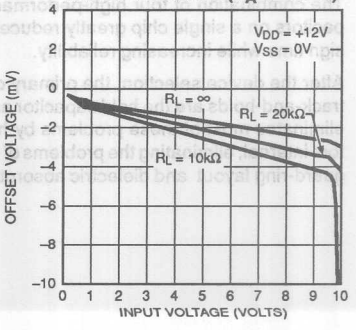
OFFSET VOLTAGE VS INPUT VOLTAGE (T_A = +25°C)



OFFSET VOLTAGE vs INPUT VOLTAGE (T_A = +125°C)

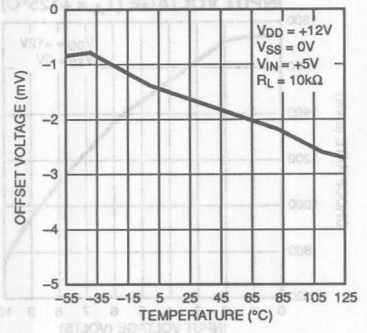


OFFSET VOLTAGE vs INPUT VOLTAGE (T_A = –55°C)

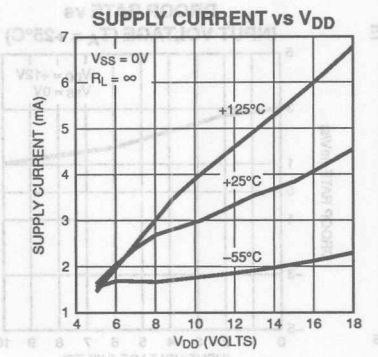


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

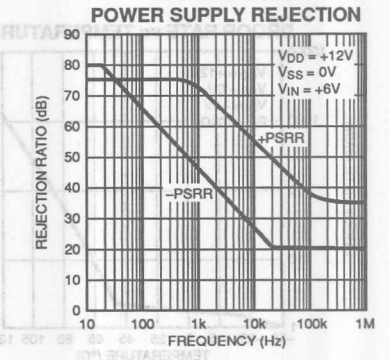
OFFSET VOLTAGE vs TEMPERATURE



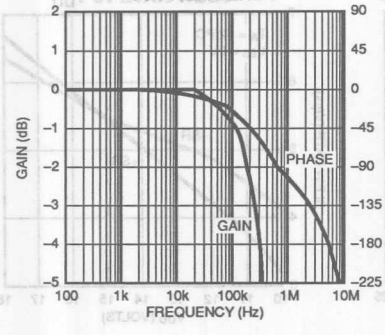
SUPPLY CURRENT vs V_{DD}



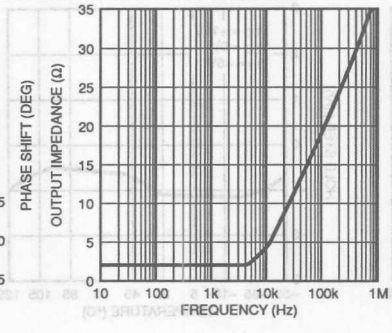
SAMPLE MODE POWER SUPPLY REJECTION



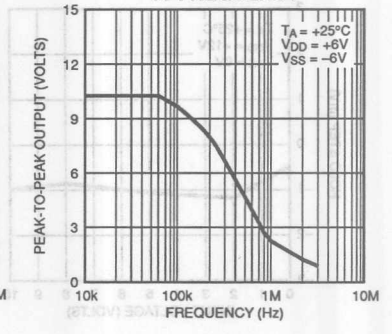
GAIN, PHASE SHIFT vs FREQUENCY



OUTPUT IMPEDANCE vs FREQUENCY



MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



GENERAL INFORMATION

The SMP-04 is a quad sample-and-hold with each track-and-hold having its own input, output, control, and on-chip hold capacitor. The combination of four high-performance track-and-hold capacitors on a single chip greatly reduces board space and design time while increasing reliability.

After the device selection, the primary considerations in using track-and-holds are the hold capacitor and layout. The SMP-04 eliminates most of these problems by having the hold capacitors internal, eliminating the problems of leakage, feed-through, guard-ring layout and dielectric absorption.

POWER SUPPLIES

The SMP-04 is capable of operating with either single or dual supplies over a voltage range of 7 to 15 volts. Based on the supply voltages chosen, V_{DD} and V_{SS} establish the output voltage range, which is:

$$V_{SS} + .05V \leq V_{OUT} \leq V_{DD} - 2V$$

Note that several specifications, including acquisition time, offset and output voltage compliance will degrade for a total supply voltage of less than 7V. Positive supply current is typically 4mA with the outputs unloaded. The SMP-04 has an internally regulated TTL supply so that TTL/CMOS compatibility will be maintained over the full supply range.

Single Supply Operation Grounding Considerations – In single supply applications, it is extremely important that the V_{SS} (negative supply) pin be connected to a clean ground. This is because the hold capacitor is internally tied to V_{SS}. Any noise or disturbance in the ground will directly couple to the output of the sample-and-hold, degrading the signal-to-noise performance. It is advisable that the analog and digital ground traces on the circuit board be physically separated to reduce digital switching noise from entering the analog circuitry.

Power Supply Bypassing – For optimum performance, the V_{DD} supply pin must also be bypassed with a good quality, high-frequency ceramic capacitor. The recommended value is 0.1µF. In the case where dual supplies are used, V_{SS} (negative supply) bypassing is particularly important. Again this is because the internal hold capacitor is tied to V_{SS}. Good bypassing prevents high frequency noise from entering the sample-and-hold amplifier. A 0.1µF ceramic bypass capacitor is generally sufficient. For high noise environments, adding a 10µF tantalum capacitor in parallel with the 0.1µF provides additional protection.

Power Supply Sequencing – It may be advisable to have the V_{DD} turn on prior to having logic levels on the inputs. The SMP-04 has been designed to be resistant to latch-up, but standard precautions should still be taken.

OUTPUT BUFFERS (Pins 1, 2, 14, and 15)
The buffer offset specification is ±10mV; this is less than 1/2 LSB of an 8-bit DAC with 10V full scale. Change in offset over the output range is typically 3mV. The hold step is the magnitude of the voltage step caused when switching from sample-to-hold mode. This error is sometimes referred to as the pedestal error or sample-to-hold offset, and is about 1mV with little variation. The droop rate of a held channel is 2µV/ms typical and ±25µV/ms maximum.

The buffers are designed primarily to drive loads connected to ground. The outputs can source more than 1.2mA each, over the full voltage range and maintain specified accuracy. In split supply operation, symmetrical output swings can be obtained by restricting the output range to 2V from either supply.

On-chip SMP-04 buffers eliminate potential stability problems associated with external buffers; outputs are stable with capacitive loads up to 500pF. However, since the SMP-04's buffer outputs are not short-circuit protected, care should be taken to avoid shorting any output to the supplies or ground.

SIGNAL INPUT (Pins 3, 5, 11, and 12)
The signal inputs should be driven from a low impedance voltage source such as the output of an op amp. The op amp should have a high slew rate and fast settling time if the SMP-04's fast acquisition time characteristics are to be maintained. As with all CMOS devices, all input voltages should be kept within range of the supply rails ($V_{SS} \leq V_{IN} \leq V_{DD}$) to avoid the possibility of setting up a latch-up condition.

The internal hold capacitance is typically 60pF and the internal switch ON resistance is 4kΩ.

If single supply operation is desired, op amps such as the OP-21, OP-80, or OP-90 that have input and output voltage compliances including ground, can be used to drive the inputs. Split supplies, such as ±7.5V, can be used with the SMP-04 and the above mentioned op amps.

APPLICATION TIPS
All unused digital inputs should be connected to logic LOW and the analog inputs connected to analog ground. For connector-driven analog inputs that may become temporarily disconnected, a resistor to V_{SS} or analog ground should be used with a value ranging from 0.2 to 1MΩ.

Do not apply signals to the SMP-04 with power off unless the input current's value is limited to less than 10mA.

Track-and-holds are sensitive to layout and physical connections. For the best performance, the SMP-04 should not be socketed.

FREQUENCY DOMAIN PERFORMANCE
The SMP-04 has been characterized in the frequency domain for those applications that require capture of dynamic signals. See Figure 1a for typical 86.1kHz sample rate and an 8kHz input signal. Typically, the SMP-04 can sample at rates up to 85kHz. In addition to the maximum sample rate, a minimum sample pulse width will also be acceptable for a given design. Our testing shows a drop in performance as the sample pulse width becomes less than 4µs.

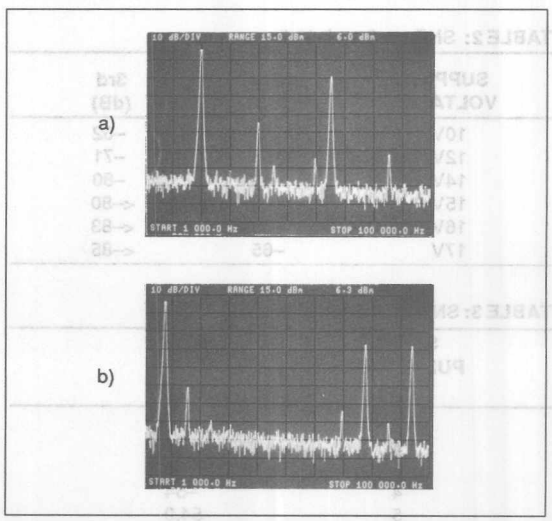


FIGURE 1: *Spectral response at a sampling frequency of 86kHz. Photo (a) shows a 20kHz carrier frequency, and photo (b) shows an 8kHz frequency.*

Optimizing Dynamic Performance of the SMP-04 – Various operating parameters such as input voltage amplitude, sampling pulse width and, as mentioned before, supply bypassing and grounding all have an effect on the signal-to-noise ratio. Table 1 shows the SNR versus input level for the SMP-04.
Distortion of the SMP-04 is reduced by increasing the supply voltage. This has the effect of increasing the positive slew rate. Table 2 shows data taken at 12.3kHz sample rate and 2kHz input frequency. Total harmonic distortion is dominated by the second and third harmonics.

Table 3 shows the effect of sampling pulse width on the SNR of the SMP-04. The recommended operating pulse width should be a minimum of 5 µs to achieve a good balance between acquisition time and SNR for the 1.4V_{p-p} signal shown. For larger swings the pulse width will need to be larger to account for the time required for the signal to slew the additional voltage. This could be used as a method of measuring acquisition time indirectly.

TABLE 1: SNR vs. V_{IN}

INPUT VOLTAGE (V_{p-p})	SNR (dB)
1	–61
2	–53
3	–50
4	–47
5	–45
6	–44

Conditions: V_S = ±6V, f_S = 14.4kHz, f_{IN} = 1.8kHz, t_{PW} = 10 µs.

TABLE 2: SNR vs. Supply Voltage

SUPPLY VOLTAGE	2nd (dB)	3rd (dB)
10V	–49	–62
12V	–55	–71
14V	–60	–80
15V	–62	<–80
16V	–63	<–83
17V	–65	<–85

TABLE 3: SNR vs. Sample Pulse Width

SAMPLE PULSE WIDTH (µs)	SNR (dB)
1	–37
2	–44
3	–50
4	–54
5	–54.9
6	–55
7	–55.3

Conditions: V_S = ±6V, V_{IN} = 1.4V_{p-p}, f_S =14.4kHz, f_{IN} = 1.8kHz

Sample-Mode Distortion Characteristics – Although designed as a sample-and-hold, the SMP-04 may be used as a straight buffer amplifier by configuring it in a continuous sample mode. This is done by connecting the $\overline{S/H}$ control pin to a logic LOW. Its buffer bandwidth is primarily limited by the distortion content as the signal frequency increases. Figure 2 shows the distortion characteristics of the SMP-04 versus frequency. It maintains less than 1% total harmonic distortion over a voiceband of 8kHz.

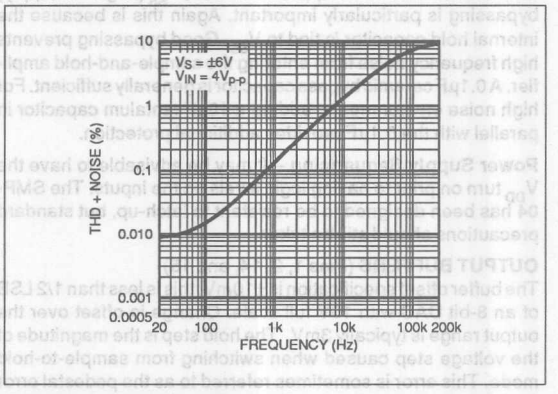


FIGURE 2: *THD+N vs. Frequency*

Sampled Data Dynamic Performance – In continuous sampled data applications such as voice digitization or communication circuits, it is important to analyze the spectral response of a sample-and-hold. Figures 1a and b show the SMP-04 sampling at a frequency of 86kHz with a 1.4V_{p-p} pure sine wave input of 20kHz and 8kHz respectively. The photos include the sampling carrier frequency as well as its multiplying frequencies. In the case of the 20kHz carrier frequency, the second harmonic measures 41dB down from the fundamental, because the second is dominant, the signal-to-noise ratio is –40.9dB. The 8kHz case produces an improved S/N performance of –48 dB.

In the V.32 and V.33 modem environment, where a 1.8kHz carrier signal frequency is applied to the SMP-04, Figure 3 compares the spectral responses of the SMP-04 under three different sampling frequencies of 14.4kHz, 9.6kHz and 7.2kHz. The signal-to-noise ratios measure to be 58.2dB, 59.3dB and 60dB respectively.

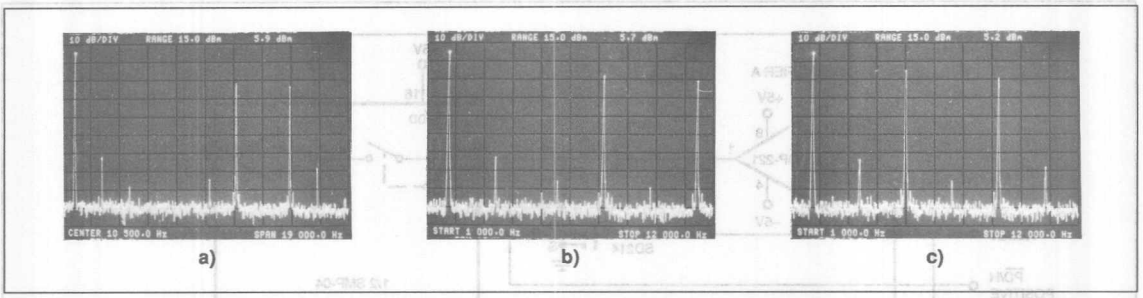


FIGURE 3: *SMP-04 spectral response with a 1.8kHz carrier frequency. (a) shows the sampling frequency at 14.4kHz; it exhibits a S/N ratio of 58.2dB. (b) shows a 59.3dB S/N at a sampling frequency of 8.6kHz. (c) shows a 60dB S/N at 7.2kHz.*

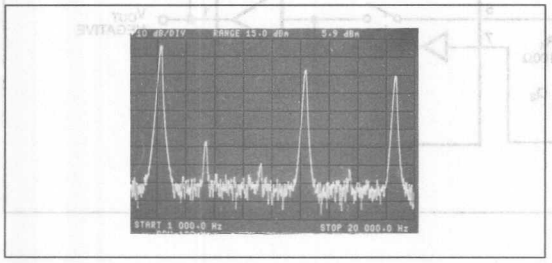


FIGURE 4: *SMP-04 spectral response with an input carrier frequency of 3kHz and the sampling frequency of 15.7kHz.*

Figure 4 depicts SMP-04's spectral response operating with voice frequency of 3kHz sampling at a 15.7kHz rate. Under this condition, the signal-to-noise measures 53dB.

4

APPLICATIONS

MULTIPLEXED QUAD DAC (Figure 5)

The SMP-04 can be used to demultiplex a single DAC converter's output into four separate analog outputs. The circuit is greatly simplified by using a voltage output DAC such as the DAC-8228. To minimize output voltage perturbation, 5µs should be allowed to settle to its final voltage before a sample signal is asserted. Each sample-and-hold amplifier must be refreshed every second or less in order to assure the droop does not exceed 10mV or 1/2 LSB.

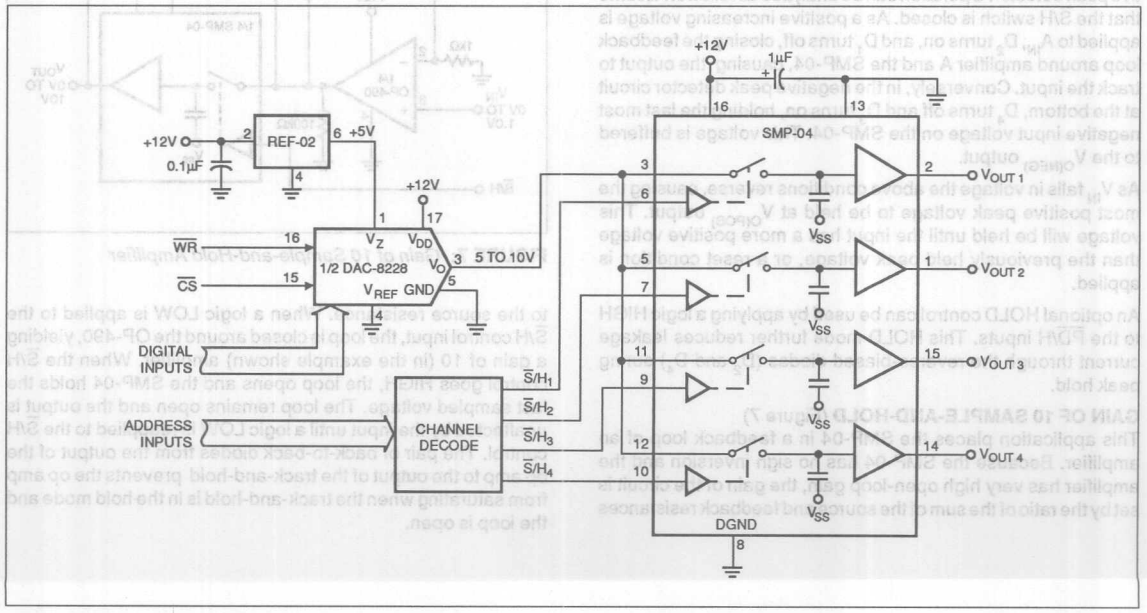


FIGURE 5: *Multiplexed Quad DAC*

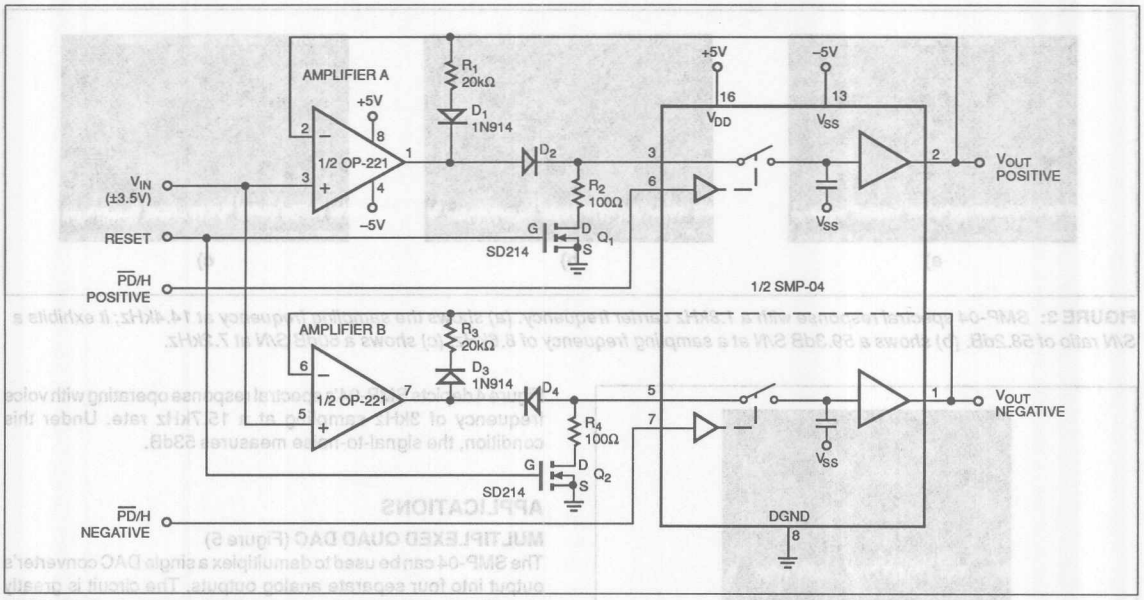


FIGURE 6: *Positive and Negative Peak Detector with Hold Control*

POSITIVE AND NEGATIVE PEAK DETECTOR WITH HOLD CONTROL (Figure 6)

In this application the top amplifier (amplifier A) is the positive peak detector and the bottom amplifier (amplifier B) is the negative peak detector. Operation can be analyzed as follows: Assume that the $\overline{S}$/H switch is closed. As a positive increasing voltage is applied to A_{IN}, D_2 turns on, and D_1 turns off, closing the feedback loop around amplifier A and the SMP-04, causing the output to track the input. Conversely, in the negative peak detector circuit at the bottom, D_4 turns off and D_3 turns on, holding the last most negative input voltage on the SMP-04. This voltage is buffered to the $V_{O(NEG)}$ output.

As V_{IN} falls in voltage the above conditions reverse, causing the most positive peak voltage to be held at $V_{O(POS)}$ output. This voltage will be held until the input has a more positive voltage than the previously held peak voltage, or a reset condition is applied.

An optional HOLD control can be used by applying a logic HIGH to the $\overline{PD}$/H inputs. This HOLD mode further reduces leakage current through the reverse-biased diodes (D_2 and D_4) during peak hold.

GAIN OF 10 SAMPLE-AND-HOLD (Figure 7)

This application places the SMP-04 in a feedback loop of an amplifier. Because the SMP-04 has no sign inversion and the amplifier has very high open-loop gain, the gain of the circuit is set by the ratio of the sum of the source and feedback resistances

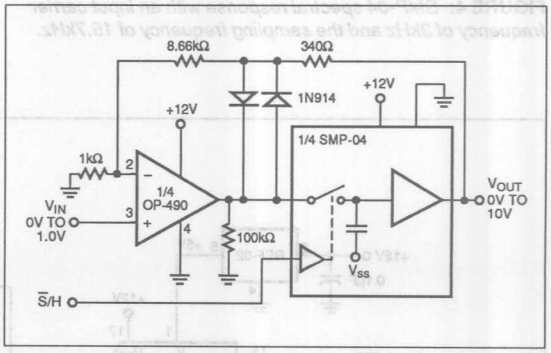


FIGURE 7: *Gain of 10 Sample-and-Hold Amplifier*

to the source resistance. When a logic LOW is applied to the $\overline{S}$/H control input, the loop is closed around the OP-490, yielding a gain of 10 (in the example shown) amplifier. When the $\overline{S}$/H control goes HIGH, the loop opens and the SMP-04 holds the last sampled voltage. The loop remains open and the output is unaffected by the input until a logic LOW is reapplied to the $\overline{S}$/H control. The pair of back-to-back diodes from the output of the op amp to the output of the track-and-hold prevents the op amp from saturating when the track-and-hold is in the hold mode and the loop is open.

SAMPLE AND DIFFERENCE AMPLIFIER (Figure 8)
This circuit uses two sample-and-holds to measure the voltage difference of a signal between two time points, t_1 and t_2. The sampled voltages are fed into the differential inputs of the AMP-02 instrumentation amplifier. A single resistor R_G sets the gain of this instrumentation amplifier. Using two of the SMP-04s in this application has the advantage of matched sample-and-hold performance, since they are both on the same chip.

SINGLE SUPPLY, SAMPLING, INSTRUMENTATION AMPLIFIER (Figure 9)
This application again uses two channels of the SMP-04 and an instrumentation amplifier to provide a sampled difference signal. The sample-and-hold signals in this circuit are tied together to sample at the same point in time. The other two parts of the SMP-04 are used as amplifiers by grounding their control lines so that they are always sampling. One section is used to drive a guard to the common-mode voltage and the other to generate a +6V reference to serve as an offset for single supply operation.

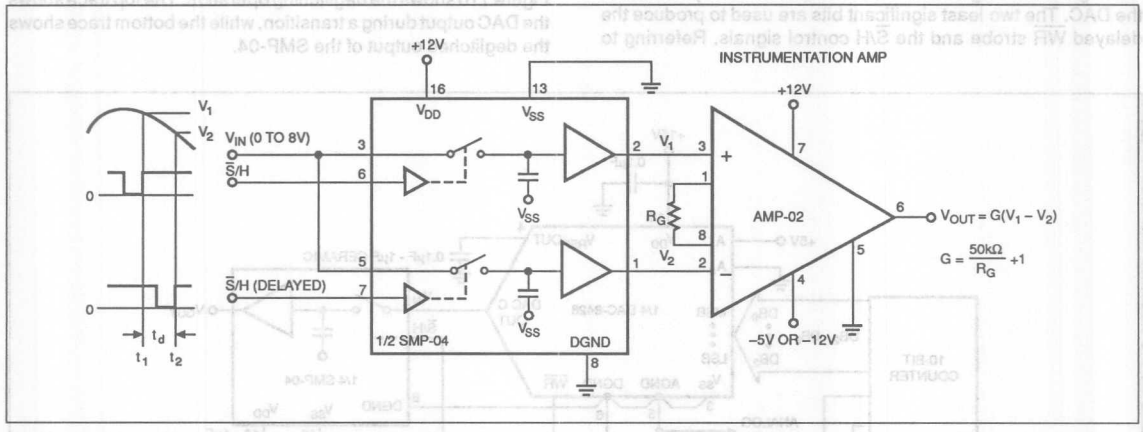


FIGURE 8: *Time Delta Sample-and-Difference Measurement*

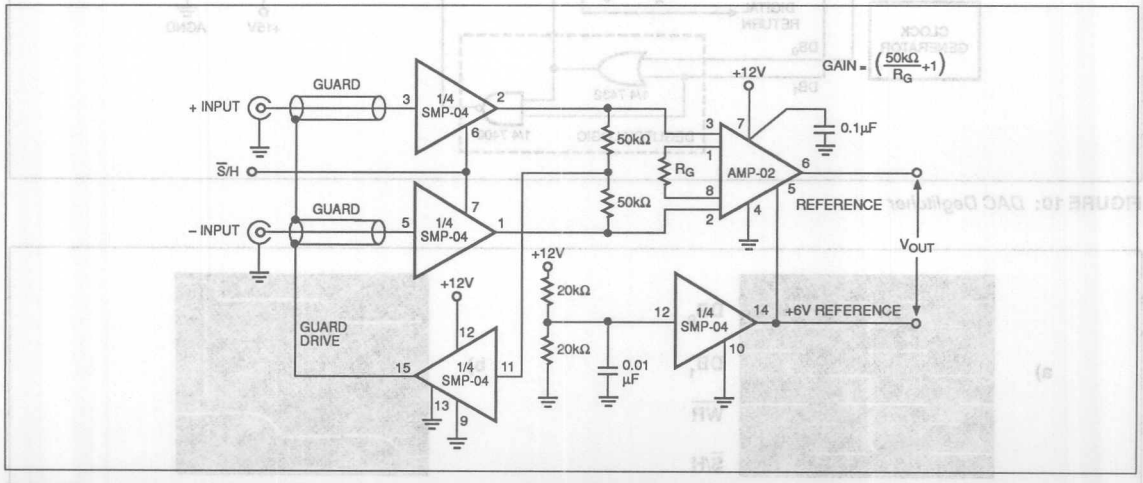


FIGURE 9: *+12V Single Supply Sampling Instrumentation Amplifier with Guard Drive*

Most D/A converters output an appreciable amount of glitch energy during a transition from one code to another. The glitch amplitude can range from several millivolts to hundreds of millivolts. This may become unacceptable in many applications. By selectively delaying the DAC's output transition, the SMP-04 can be used to smooth the output waveform. Figure 10 shows the schematic diagram of such a deglitcher circuit. Two simple logic gates (an OR and a NAND gate) provide the proper timing sequence for the DAC $\overline{WR}$ strobe and the $\overline{S}$/H control signal to the SMP-04. In this example a linear ramp signal is generated by feeding the most significant 8-bits of the 10-bit binary counter to the DAC. The two least significant bits are used to produce the delayed $\overline{WR}$ strobe and the $\overline{S}$/H control signals. Referring to the timing diagram, Figure 11a, the DAC's output changes on the falling edge, but the DAC output does not change yet until a $\overline{WR}$ strobe goes active. During this period, the SMP-04 is in a sample mode whose output tracks the DAC output. When $\overline{S}$/H goes HIGH, the current DAC output voltage is held by the SMP-04. After 1.2µs settling, the $\overline{WR}$ strobe goes LOW to allow the DAC output to change. Any glitch that occurs at the DAC output is effectively blocked by the SMP-04. As soon as the $\overline{WR}$ strobe goes HIGH, the digital data is latched; at the same time the $\overline{S}$/H goes LOW, allowing the SMP-04 to track to the new DAC output voltage.

Figure 11b shows the deglitching operation. The top trace shows the DAC output during a transition, while the bottom trace shows the deglitched output of the SMP-04.

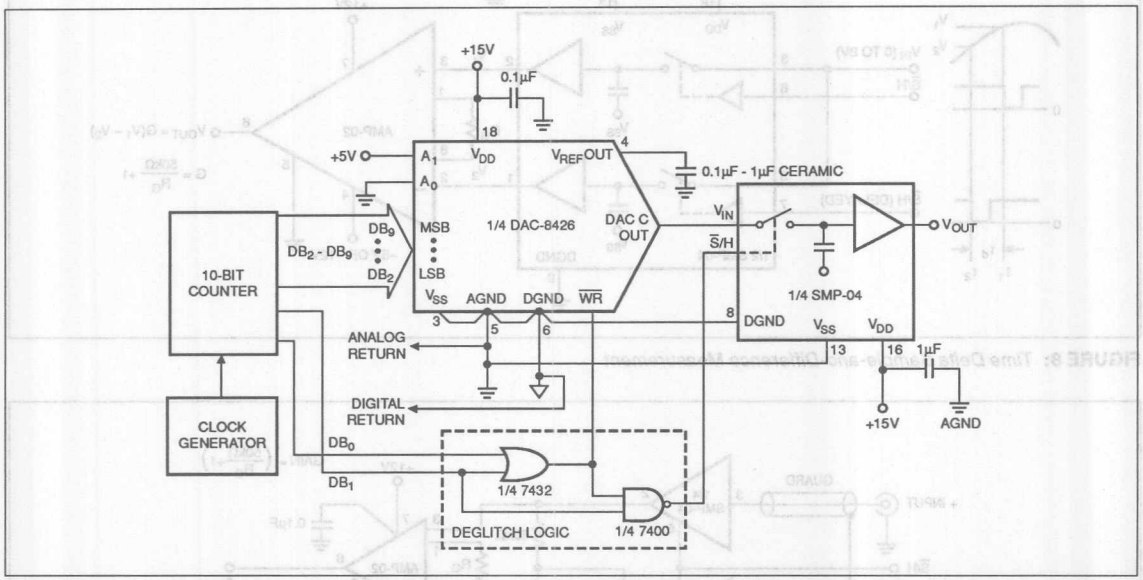


FIGURE 10: *DAC Deglitcher*

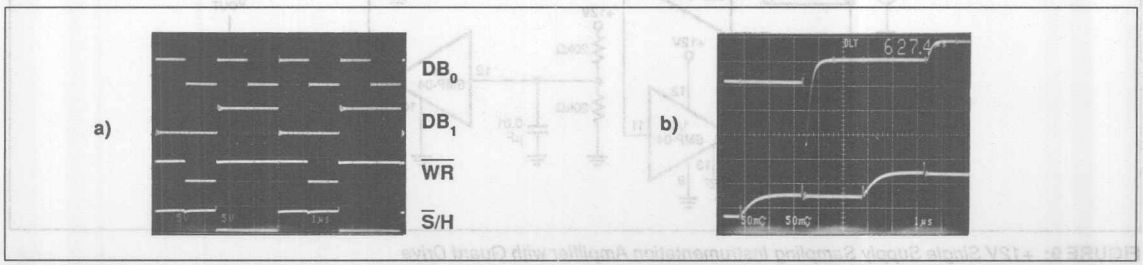
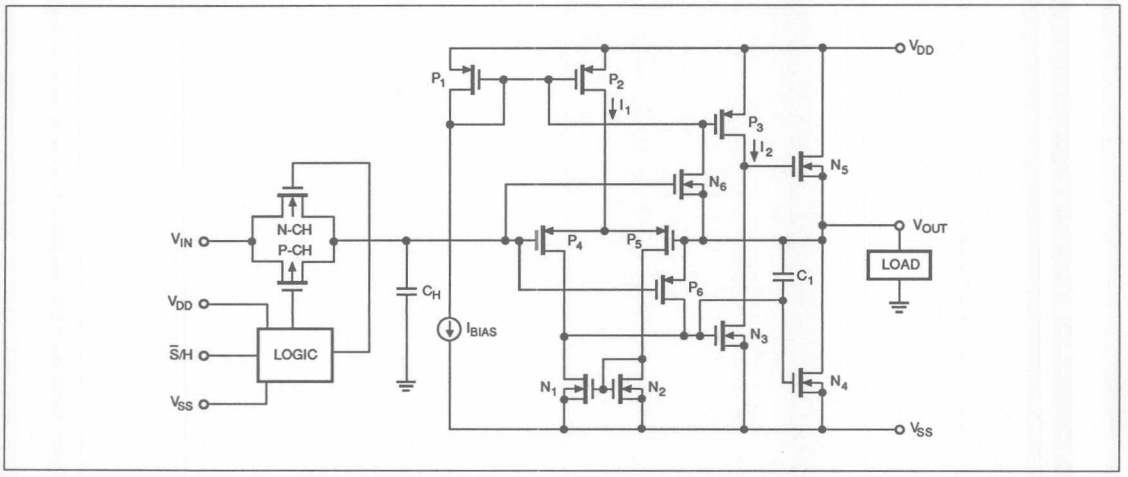
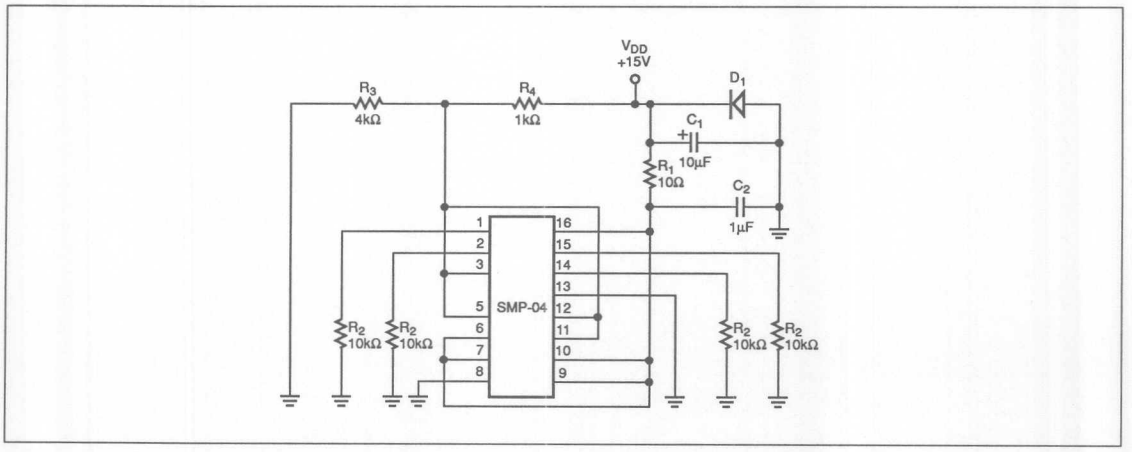


FIGURE 11: *(a) shows the logic timing of the deglitcher. The top two traces are the two least significant bits, DB_0 and DB_1, respectively. These are used to generate the $\overline{WR}$ and $\overline{S}$/H signals which are shown in the bottom two traces. (b) shows the typical glitch amplitude of a DAC (top trace) and the deglitched output of the AMP-04 (bottom trace).*

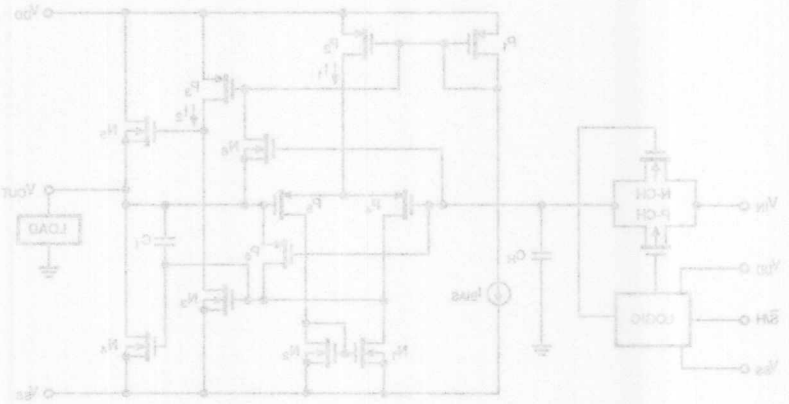
SIMPLIFIED SCHEMATIC



BURN-IN CIRCUIT



SIMPLIFIED SCHEMATIC



BURN-IN CIRCUIT

Octal Sample-and-Hold with Multiplexed Input

SMP-08

FEATURES

- Internal Hold Capacitors
- Low Droop Rate
- TTL/CMOS Compatible Logic Inputs
- Single or Dual Supply Operation
- Break-Before-Make Channel Addressing
- Compatible With CD4051 Pinout
- Low Cost

APPLICATIONS

- Multiple Path Timing Deskew for A.T.E.
- Memory Programmers
- Mass Flow/Process Control Systems
- Multichannel Data Acquisition Systems
- Robotics and Control Systems
- Medical and Analytical Instrumentation
- Event Analysis
- Stage Lighting Control

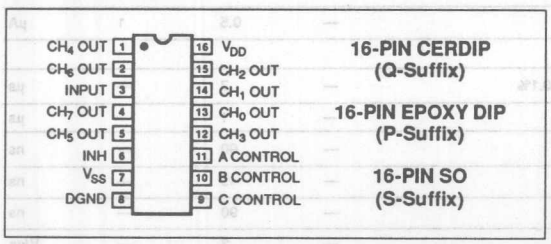
ORDERING INFORMATION †

PACKAGE: 16-PIN DIP/SO		OPERATING TEMPERATURE RANGE
CERDIP 16-PIN	PLASTIC 16-PIN	
TBA*	–	MIL
SMP08FQ	SMP08FP	XIND
–	SMP08FS	XIND

* Consult factory for 883 data sheet.

† Burn-in is available on industrial temperature range parts in CerDIP and plastic DIP packages.

PIN CONNECTIONS



16-PIN CERDIP (Q-Suffix)

16-PIN EPOXY DIP (P-Suffix)

16-PIN SO (S-Suffix)

GENERAL DESCRIPTION

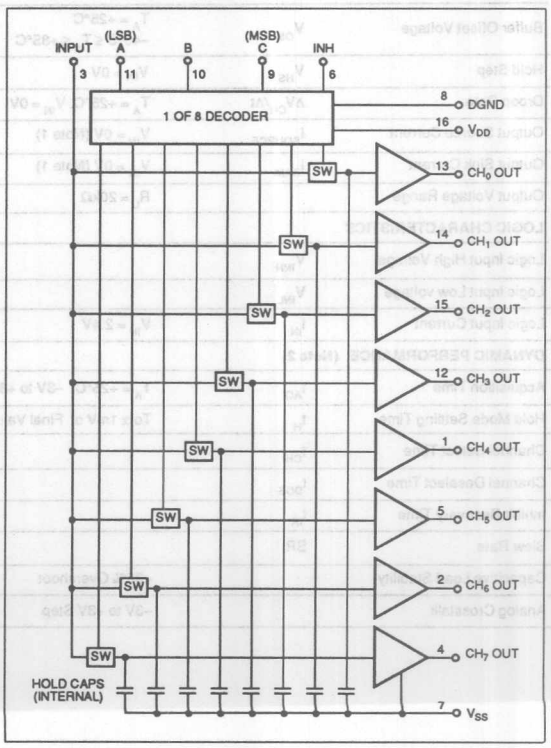
The SMP-08 is a monolithic octal sample-and-hold; it has eight internal buffer amplifiers, input multiplexer, and internal hold capacitors. It is manufactured in an advanced oxide isolated CMOS technology to obtain high accuracy, low droop rate, and fast acquisition time. The SMP-08 has a typical linearity error of only 0.01% and can accurately acquire a 10-bit input signal to ±1/2 LSB in less than seven microseconds. The SMP-08's output swing includes the negative supply in both single and dual supply operation.

The SMP-08 was specifically designed for systems that use a calibration cycle to adjust a multiple of system parameters. The low cost and high level of integration makes the SMP-08 ideal for calibration requirements that have previously required an ASIC, or high cost multiple D/A converters.

The SMP-08 is also ideally suited for a wide variety of sample-and-hold applications including amplifier offset or VCA gain adjustments. One or more SMP-08s can be used with single or multiple DACs to provide multiple set points within a system.

The SMP-08 offers significant cost and size reduction over discrete designs. It is available in a 16-pin hermetic or plastic DIP, or surface mount SOIC package.

FUNCTIONAL DIAGRAM



Manufactured under the following U.S. patent: 4,739,281

ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{DD} to DGND ..... –0.3V, 17V
V_{DD} to V_{SS} ..... –0.3V, 17V
V_{LOGIC} to DGND ..... –0.3V, V_{DD}
V_{IN} to DGND ..... V_{SS}, V_{DD}
V_{OUT} to DGND ..... V_{SS}, V_{DD}
Analog Output Current ..... ±20mA
(Not short-circuit protected)
Operating Temperature Range
FP, FS ..... –40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

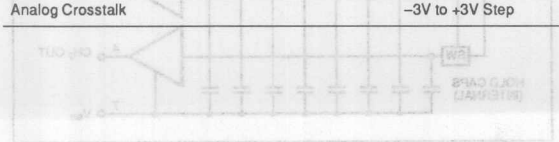
PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SO (S)	92	27	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

CAUTION:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.
2. Digital inputs and outputs are protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam or packaging at all times until ready to use. Use proper anti-static handling procedures.
3. Remove power before inserting or removing units from their sockets.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, V_{SS} = –5V, DGND = 0V, R_L = No Load, T_A = –40°C to +85°C for SMP-08F, unless otherwise noted.

			SMP-08F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Linearity Error		–3V ≤ V_{IN} ≤ +3V	—	0.01	—	%
Buffer Offset Voltage	V_{OS}	T_A = +25°C	—	2.5	10	mV
		–40°C ≤ T_A ≤ +85°C	—	3.5	20	
Hold Step	V_{HS}	V_{IN} = 0V	—	1	4	mV
Droop Rate	$\Delta V_{CH}/\Delta t$	T_A = +25°C, V_{IN} = 0V	—	2	20	mV/s
Output Source Current	I_{SOURCE}	V_{IN} = 0V (Note 1)	1.2	—	—	mA
Output Sink Current	I_{SINK}	V_{IN} = 0V (Note 1)	0.5	—	—	mA
Output Voltage Range		R_L = 20kΩ	–3.0	—	+3.0	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4	—	—	V
Logic Input Low voltage	V_{INL}		—	—	0.8	V
Logic Input Current	I_{IN}	V_{IN} = 2.4V	—	0.5	1	µA
DYNAMIC PERFORMANCE (Note 2)						
Acquisition Time	t_{AQ}	T_A = +25°C, –3V to +3V to 0.1%	—	7	—	µs
Hold Mode Settling Time	t_H	To ± 1mV of Final Value	—	1	—	µs
Channel Select Time	t_{CH}		—	90	—	ns
Channel Deselect Time	t_{DCS}		—	45	—	ns
Inhibit Recovery Time	t_{IR}		—	90	—	ns
Slew Rate	SR		—	3	—	V/µs
Capacitive Load Stability		<30% Overshoot	—	500	—	pF
Analog Crosstalk		–3V to +3V Step	—	–72	—	dB



ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, V_{SS} = –5V, DGND = 0V, R_L = No Load, T_A = –40°C to +85°C for SMP-08F, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	SMP-08F MIN	SMP-08F TYP	SMP-08F MAX	UNITS
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±6V	60	75	—	dB
Supply Current	I_{DD}	T_A = +25°C –40°C ≤ T_A ≤ +85°C	— —	5.5 7.5	7.5 9.5	mA

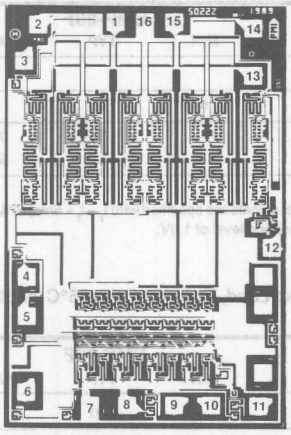
NOTES:
1. Outputs are capable of sinking and sourcing over 20mA but offset is guaranteed at specified load levels.
2. All input control signals are specified with $t_r = t_f$ = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.

ELECTRICAL CHARACTERISTICS at V_{DD} = +12V, V_{SS} = 0V, DGND = 0V, R_L = No Load, T_A = –40°C to +85°C for SMP-08F, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SMP-08F MIN	SMP-08F TYP	SMP-08F MAX	UNITS
Linearity Error		60mV ≤ V_{IN} ≤ 10V	—	0.01	—	%
Buffer Offset Voltage	V_{OS}	T_A = +25°C –40°C ≤ T_A ≤ +85°C	— —	2.5 3.5	10 20	mV
Hold Step	V_{HS}	V_{IN} = 6V	—	1	4	mV
Droop Rate	$\Delta V_{CH}/\Delta t$	T_A = +25°C, V_{IN} = 6V	—	2	20	mV/s
Output Source Current	I_{SOURCE}	V_{IN} = 6V (Note 1)	1.2	—	—	mA
Output Sink Current	I_{SINK}	V_{IN} = 6V (Note 1)	0.5	—	—	mA
Output Voltage Range		R_L = 20kΩ R_L = 10kΩ	0.06 0.06	— —	10.0 9.5	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4	—	—	V
Logic Input Low voltage	V_{INL}		—	—	0.8	V
Logic Input Current	I_{IN}	V_{IN} = 2.4V	—	0.5	1	µA
DYNAMIC PERFORMANCE (Note 2)						
Acquisition Time	t_{AQ}	T_A = +25°C, 0 to 10V to 0.1%	—	9	—	µs
Hold Mode Settling Time	t_H	To ± 1mV of Final Value	—	1	—	µs
Channel Select Time	t_{CH}		—	90	—	ns
Channel Deselect Time	t_{DCS}		—	45	—	ns
Inhibit Recovery Time	t_{IR}		—	90	—	ns
Slew Rate	SR	R_L = 20kΩ (Note 3)	3	4	—	V/µs
Capacitive Load Stability		<30% Overshoot	—	500	—	pF
Analog Crosstalk		0 to 10V Step	—	–72	—	dB
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	10.8V ≤ V_{DD} ≤ 13.2V	60	75	—	dB
Supply Current	I_{DD}	T_A = +25°C –40°C ≤ T_A ≤ +85°C	— —	6.0 8.0	8.0 10.0	mA

NOTES:
1. Outputs are capable of sinking and sourcing over 20mA but offset is guaranteed at specified load levels.
2. All input control signals are specified with $t_r = t_f$ = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
3. Slew rate is measured in the sample mode with a 0 to 10V step from 20% to 80%.

DICE CHARACTERISTICS



DIE SIZE 0.080 x 0.120 inch, 9,600 sq. mils
(2.032 x 3.048 mm, 6.193 sq. mm)

1. CH_4 OUT
2. CH_5 OUT
3. INPUT
4. CH_7 OUT
5. CH_5 OUT
6. INH
7. V_{SS}
8. DGND
9. C CONTROL
10. B CONTROL
11. A CONTROL
12. CH_3 OUT
13. CH_0 OUT
14. CH_1 OUT
15. CH_2 OUT
16. V_{DD}

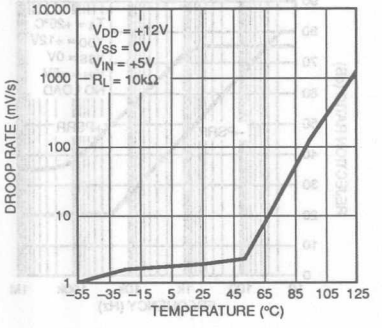
WAFER TEST LIMITS at V_{DD} = +12V, V_{SS} = DGND = 0V, R_L = No Load, T_A = +25°C, unless otherwise specified.

			SMP-08GBC	
PARAMETER	SYMBOL	CONDITIONS	LIMITS	UNITS
Buffer Offset Voltage	V_{OS}	V_{IN} = +6V	20	mV MAX
Droop Rate	$\Delta V_{CH}/\Delta t$	V_{IN} = +6V	20	mV/s MAX
Output Source Current	I_{SOURCE}	V_{IN} = +6V	1.2	mA MIN
Output Sink Current	I_{SINK}	V_{IN} = +6V	0.5	mA MIN
Output Voltage Range		R_L = 20kΩ R_L = 10kΩ	0.06/10.0 0.06/9.5	V MAX/MIN
LOGIC CHARACTERISTICS				
Logic Input High Voltage	V_{INH}		2.4	V MIN
Logic Input Low Voltage	V_{INL}		0.8	V MAX
Logic Input Current	I_{IN}	V_{IN} = 2.4V	1	µA MAX
SUPPLY CHARCTERISTICS				
Power Supply Rejection Ratio	PSRR	$10.8V \le V_{DD} \le 13.2$	60	dB MIN
Supply Current	I_{DD}		8.0	mA MAX

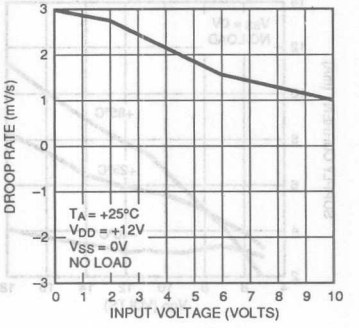
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

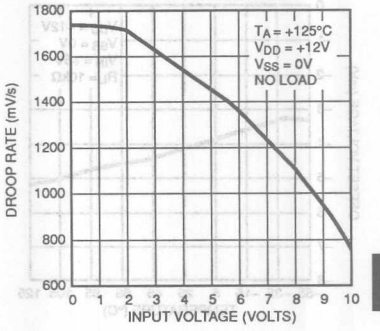
DROOP RATE vs TEMPERATURE



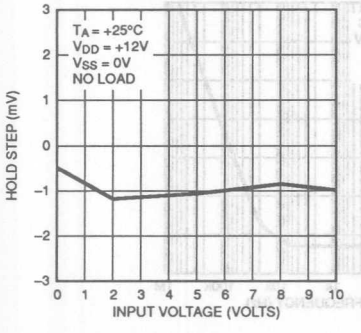
DROOP RATE vs INPUT VOLTAGE



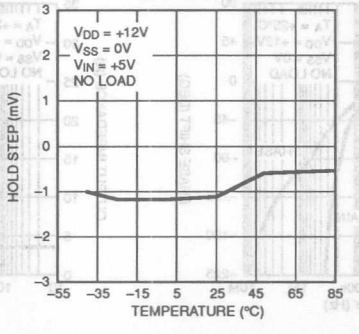
DROOP RATE vs INPUT VOLTAGE



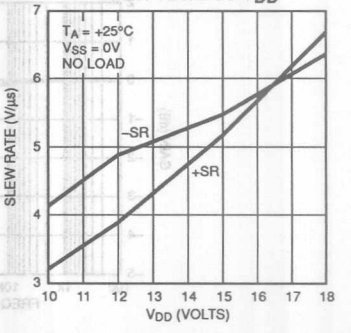
HOLD STEP vs INPUT VOLTAGE



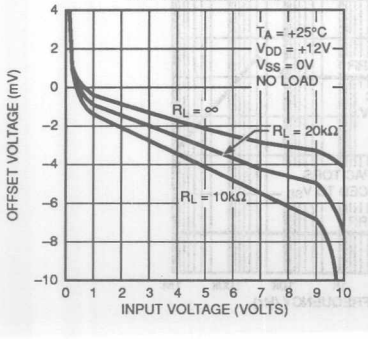
HOLD STEP vs TEMPERATURE



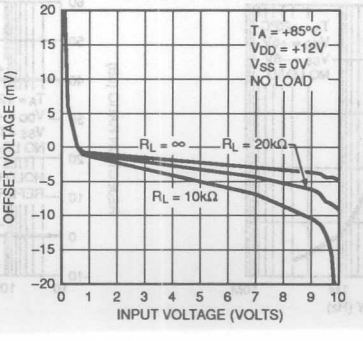
SLEW RATE vs V_{DD}



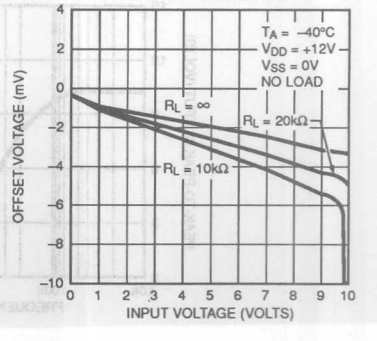
OFFSET VOLTAGE vs INPUT VOLTAGE



OFFSET VOLTAGE vs INPUT VOLTAGE

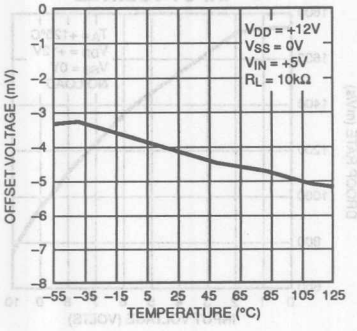


OFFSET VOLTAGE vs INPUT VOLTAGE

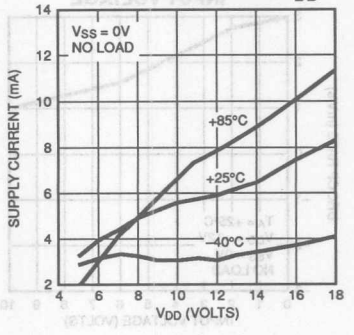


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

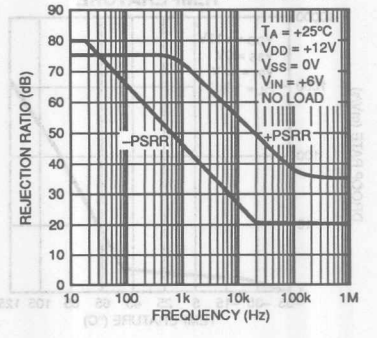
OFFSET VOLTAGE vs TEMPERATURE



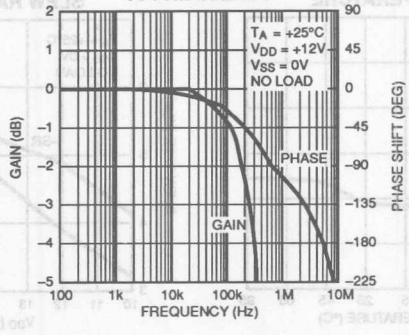
SUPPLY CURRENT vs V_{DD}



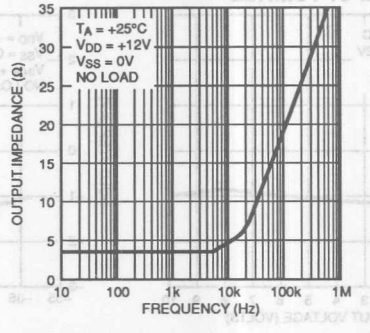
SAMPLE MODE POWER SUPPLY REJECTION



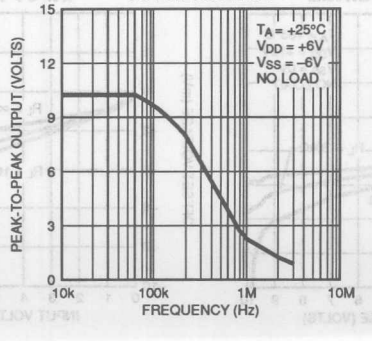
GAIN, PHASE SHIFT vs FREQUENCY



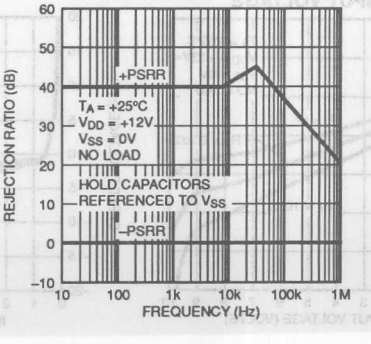
OUTPUT IMPEDANCE vs FREQUENCY



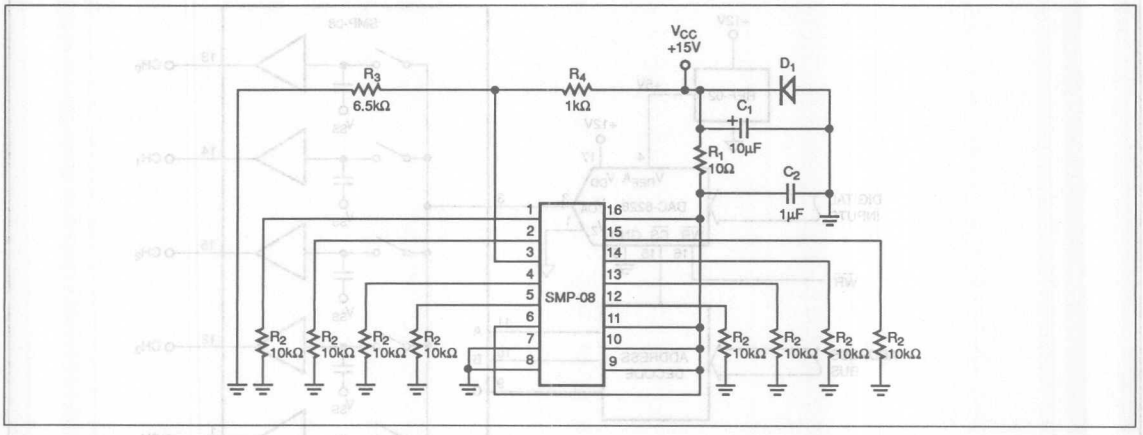
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



HOLD MODE POWER SUPPLY REJECTION



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

The SMP-08, a multiplexed octal S/H, minimizes board space in systems requiring cycled calibration or an array of control voltages. When used in conjunction with a low cost 10-bit D/A, the SMP-08 can easily be integrated into microprocessor based systems. Since the SMP-08 features break-before-make switching and an internal decoder, no external logic is required. The SMP-08 has an internally regulated TTL supply so that TTL/CMOS compatibility is maintained over the full supply range. See Figure 1 for channel decode address information.

POWER SUPPLIES

The SMP-08 is capable of operating with either single or dual supplies, over a voltage range of 7 to 15 volts. Based on the supply voltages chosen, V_{DD} and V_{SS} establish the input and output voltage range, which is:

$(V_{SS} + 0.06V) \leq V_{OUT/IN} \leq (V_{DD} - 2V)$

Note that several specifications, including acquisition time, offset and output voltage compliance will degrade for supply voltages of less than 7V.

If split supplies are used, the negative supply should be bypassed with a 0.1µF capacitor in parallel with a 10µF to ground. The internal hold capacitors are connected to this supply pin and any noise will appear at the outputs.

In single supply applications, it is extremely important that the V_{SS} (negative supply) pin is connected to a clean ground. The hold capacitors are internally tied to the V_{SS} (negative) rail. Any ground noise or disturbance will directly couple to the output of the sample-and-hold, degrading the signal-to-noise performance. The analog and digital ground traces on the circuit board should be physically separated to reduce digital switching noise from entering the analog circuitry.

POWER SUPPLY SEQUENCING

V_{DD} should be applied to the SMP-08 before the logic input signals. The SMP-08 has been designed to be immune to latch-up, but standard precautions should still be taken.

OUTPUT BUFFERS (Pins 1, 2, 4, 5, 12, 13, 14, 15)

The buffer offset specification is 10mV; this is less than 1/2 LSB of an 8-bit DAC with 10V full scale. The hold step (magnitude of step caused in the output voltage when switching from sample-to-hold mode, also referred to as the pedestal error or sample-to-hold offset), is about 2mV with little variation over the full output voltage range. The droop rate of a held channel is 2mV/s typical and 20mV/s maximum.

The buffers are designed to drive loads connected to ground. The outputs can source more than 20mA, over the full voltage range, but have limited current sinking capability near V_{SS}. In split supply operation, symmetrical output swings can be obtained by restricting the output range to 2V from either supply.

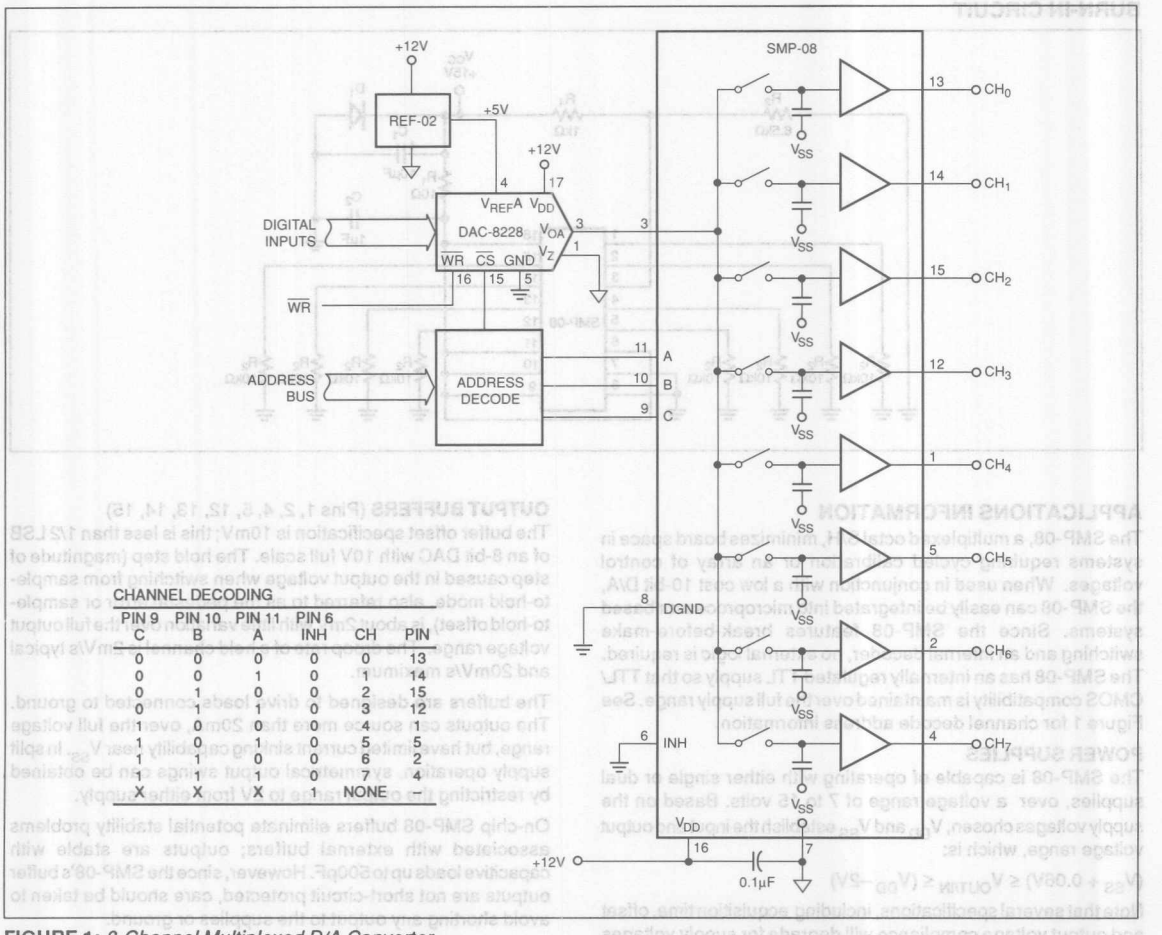
On-chip SMP-08 buffers eliminate potential stability problems associated with external buffers; outputs are stable with capacitive loads up to 500pF. However, since the SMP-08's buffer outputs are not short-circuit protected, care should be taken to avoid shorting any output to the supplies or ground.

SIGNAL INPUT (Pin 3)

The signal input should be driven from a low impedance voltage source such as the output of an op amp. The op amp should have a high slew rate and fast settling time if the SMP-08's acquisition time characteristics are to be maintained. As with all CMOS devices, all input voltages should be kept within range of the supply rails ($V_{SS} \leq V_{IN} \leq V_{DD}$) to avoid the possibility of latch-up. If single supply operation is desired, op amps such as the OP-21, OP-80, or OP-90 that have input and output voltage compliances including ground, can be used to drive the inputs. Split supplies, such as ±7.5V, can be used with the SMP-08.

APPLICATION TIPS

All unused digital inputs should be connected to logic LOW and unused analog inputs connected to analog ground. For connector-driven analog inputs that may become temporarily disconnected, a resistor to V_{DD}, V_{SS} or analog ground should be used with a value ranging from 200kΩ to 1MΩ.



CHANNEL DECODING

PIN 9 C	PIN 10 B	PIN 11 A	PIN 6 INH	CH	PIN
0	0	0	0	0	13
0	0	1	0	1	14
0	1	0	0	2	15
0	1	1	0	3	12
1	0	0	0	4	1
1	0	1	0	5	5
1	1	0	0	6	2
1	1	1	0	7	4
X	X	X	1	NONE	–

FIGURE 1: *8-Channel Multiplexed D/A Converter*

Do not apply signals to the SMP-08 with power off unless the input current is limited to less than 10mA.

TYPICAL APPLICATIONS

AN 8-CHANNEL MULTIPLEXED D/A CONVERTER

Figure 1 illustrates a typical multiplexing function of the SMP-08. It is used to sample-and-hold eight different output voltages corresponding to eight different digital codes from a D/A converter. The SMP-08's droop rate of 20mV/s requires a refresh once every 500ms, before the voltage drifts beyond 1/2 LSB accuracy (1 LSB of an 8-bit DAC is equivalent to 19.5mV, out of a full-scale voltage of 5V). For a 10-bit DAC, the refresh rate must be less than 120ms, and, for a 12-bit system, 31ms. This implementation is very cost-effective compared to using multiple DACs as the number of output channels increases.

FEATURES

SMP-10

- Low Droop Rate 5.0μV/ms
- Linearity Error 0.005%
- High Sample/Hold Current Ratio ..... 2×10^9

SMP-11

- Low Droop Rate Over Temperature 2400μV/ms
- High Sample/Hold Current Ratio ..... 1.7×10^8

BOTH SMP-10 AND SMP-11

- Fast Acquisition Time, 10V Step to 0.1% 3.5μs
- High Slew Rate 10V/μs
- Low Aperture Time 50ns
- Trimmed for Minimum Zero-Scale Error 0.45mV
- Feedthrough Attenuation Ratio 96dB
- Low Power Dissipation 160mW
- DTL, TTL & CMOS Compatible Logic Input
- HA-2420, HA-2425, SHM-IC-1, and AD583 Socket Compatible
- Available in Die Form

ORDERING INFORMATION †

$T_A = +25°C$

V_{ZS} (mV)	DROOP RATE IN μV/ms	PACKAGE 14-PIN DIP HERMETIC	PACKAGE LCC	OPERATING TEMPERATURE RANGE
1.5	20	SMP10AY*	–	MIL
1.5	20	SMP10EY	–	COM
3.0	50	SMP10FY	–	COM
1.5	200	SMP11AY*	–	MIL
3.0	500	SMP11BY*	SMP11BRC/883	MIL
1.5	200	SMP11EY	–	COM
3.0	500	SMP11FY	–	COM
7.0	900	SMP11GY	–	COM
7.0	900	SMP11GS	–	XIND
7.0	900	SMP11GP	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The SMP-10/11 are precision sample-and-hold amplifiers that provide the high accuracy, the low droop rate and the fast acquisition time required in data acquisition and signal processing systems. Both devices are essentially noninverting unity gain circuits consisting of two very high input impedance buffer amplifiers connected together by a diode bridge switch.

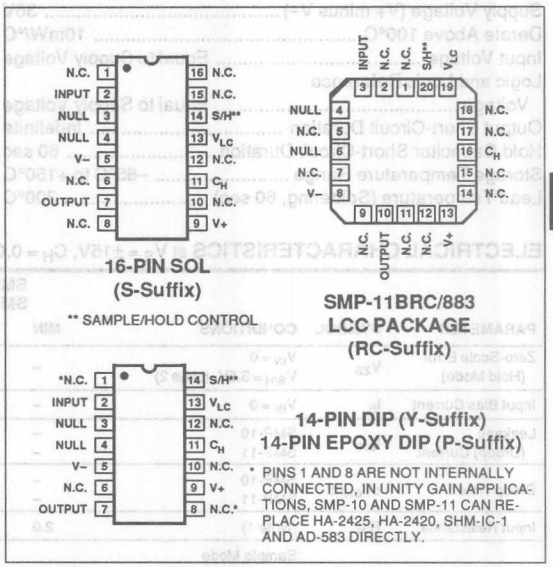
HIGH ACCURACY AND LOW DROOP RATE

The high input impedance and the low droop rates of the SMP-10 and the SMP-11 are achieved by using bipolar Darlington circuits and an ion implant process that creates "super beta" transistors.

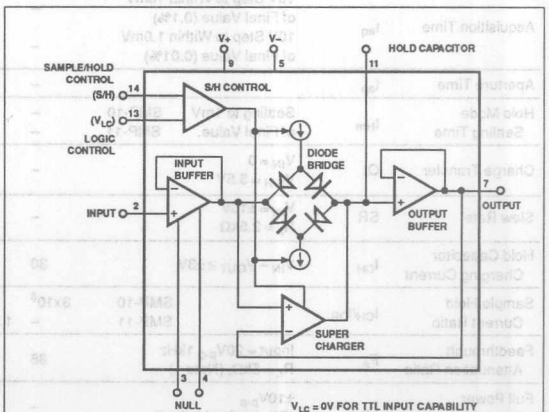
The output buffer's input stage converts to a super beta Darlington configuration during the hold mode, which results in a very low droop rate with no penalty in acquisition time. The use of bipolar transistors achieves a low change in droop rate over the operating temperature range.

Continued

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



S/H	MODE
0	Sample
1	Hold

Manufactured under the following patents: 4,109,215 and 4,142,117.

GENERAL DESCRIPTION *Continued*

FAST ACQUISITION

A unique super charger provides up to 50mA of charging current to the hold capacitor, which results in smooth, fast charging with minimum noise. As the hold capacitor voltage nears its final value, the low current diode bridge controls the final settling time. This unique combination of linear functions in a monolithic circuit enables the system designer to achieve superior performance.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V+ minus V–) 36V
Derate Above 100°C ..... 10mW/°C
Input Voltage ..... Equal to Supply Voltage
Logic and Logic Reference Voltage ..... Equal to Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Hold Capacitor Short-Circuit Duration ..... 60 sec
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Operating Temperature Range
SMP-10AY ..... –55°C to +125°C
SMP-10EY, FY ..... 0°C to +70°C
SMP-11AY, BY, BRC ..... –55°C to +125°C
SMP-11EY, FY, GY ..... 0°C to +70°C
SMP11GS, GP ..... –40°C to +85°C
Junction Temperature (T_j) ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	108	16	°C/W
14-Pin Epoxy DIP (P)	83	39	°C/W
16-Pin SOL (S)	98	30	°C/W
20-Contact LCC (RC)	98	38	°C/W

NOTES:
1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and LCC packages.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $T_A = +25°C$, unless otherwise noted.

				SMP-10A/E SMP-11A/E			SMP-10F SMP-11B/F			SMP-11G			
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Zero-Scale Error (Hold Mode)	V_{ZS}	$V_{IN} = 0$ $V_{S/H} = 3.5V$, (Note 2)		–	0.45	1.5	–	0.60	3.0	–	1.5	7.0	mV
Input Bias Current	I_B	$V_{IN} = 0$		–	35	65	–	55	90	–	90	160	nA
Leakage (Droop) Current	I_{DR}	SMP-10 SMP-11		– –	– –	0.10 1.00	– –	– –	0.25 2.50	– –	– –	– 4.5	nA
Droop Rate	dV_{CH}/dt	SMP-10 SMP-11		– –	5 60	20 200	– –	5 70	50 500	– –	– 80	– 900	µV/ms
Input Resistance	R_{IN}	(Note 1)		2.0	3.0	–	1.4	2.5	–	–	2.0	–	GΩ
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm10V$, $R_L = 5k\Omega$ or $V_{IN} = \pm5V$, $R_L = 2.5k\Omega$		0.99963	0.99983	–	0.99953	0.99978	–	0.99940	0.99975	–	V/V
Acquisition Time	t_{aq}	10V Step to Within 10mV of Final Value (0.1%)		–	3.5	–	–	3.5	–	–	3.5	–	µs
		10V Step to Within 1.0mV of Final Value (0.01%)		–	5.0	–	–	5.0	–	–	5.0	–	µs
Aperture Time	t_{ap}			–	50	–	–	50	–	–	50	–	ns
Hold Mode Settling Time	t_{Hm}	Settling to 1mV of Final Value.	SMP-10	–	7	–	–	7	–	–	7	–	µs
			SMP-11	–	1.5	–	–	1.5	–	–	1.5	–	
Charge Transfer	Qt	$V_{IN} = 0$ $V_{S/H} = 3.5V$		–	5	–	–	5	–	–	5	–	pC
Slew Rate	SR	$V_{IN} = \pm10V$ $R_L = 2.5k\Omega$		–	10	–	–	10	–	–	10	–	V/µs
Hold Capacitor Charging Current	I_{CH}	$V_{IN} - V_{OUT} \geq \pm3V$		30	50	–	20	50	–	–	50	–	mA
Sample/Hold Current Ratio	I_{CH}/I_{DR}		SMP-10	$3x10^8$	$2x10^9$	–	$8x10^7$	$8x10^8$	–	–	–	–	mA/mA
			SMP-11	–	$1.7x10^8$	–	–	$1.5x10^8$	–	–	$1.5x10^8$	–	
Feedthrough Attenuation Ratio	F_A	Input = $20V_{p-p}$ 1kHz $R_L = 5k\Omega$, (Note 1)		86	98	–	80	90	–	–	90	–	dB
Full Power Bandwidth	F_p	$\pm10V_{p-p}$ (Dissipation Limited)		–	100	–	–	100	–	–	100	–	kHz

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $T_A = +25°C$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	SMP-10A/E SMP-11A/E MIN	SMP-10A/E SMP-11A/E TYP	SMP-10A/E SMP-11A/E MAX	SMP-10F SMP-11B/F MIN	SMP-10F SMP-11B/F TYP	SMP-10F SMP-11B/F MAX	SMP-11G MIN	SMP-11G TYP	SMP-11G MAX	UNITS
Input Voltage Range and/or Output Voltage Swing		$R_L = 2.5k\Omega$	±11	±11.5	–	±10.5	±11.5	–	±10.5	±11.5	–	V
Output Resistance	R_O		–	0.15	–	–	0.15	–	–	0.15	–	Ω
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm9V$ to ±18V	82	92	–	77	92	–	72	92	–	dB
Power Consumption (DC)	P_D	Sample Mode $V_{IN} = 0$	–	160	180	–	170	210	–	180	240	mW

NOTES:
1. Guaranteed by design.
2. Measured 500µs after hold command.

ELECTRICAL CHARACTERISTICS – SMP-10 ONLY at $V_S = \pm15V$, $C_H = 0.005\mu F$, $V_{LC} = 0V$, $T_A = +25°C$, device fully warmed up, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SMP-10A/E MIN	SMP-10A/E TYP	SMP-10A/E MAX	SMP-10F MIN	SMP-10F TYP	SMP-10F MAX	UNITS
Hold Step	V_{HS}	$V_{IN} = 0$	–1.0	+1.5	+4.0	–3.0	+1.5	+6.0	mV
Linearity Error	NL	$V_{IN} = \pm10V$, $R_L = 5k\Omega$	–	0.005	–	–	0.007	–	% of 10V
Output Noise	$E_{N\ (RMS)}$	Wideband Noise 100Hz to 100kHz Sample Mode	–	40	–	–	50	–	μV_{RMS}

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $0°C \le T_A \le +70°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SMP-10E SMP-11E MIN	SMP-10E SMP-11E TYP	SMP-10E SMP-11E MAX	SMP-10F SMP-11F MIN	SMP-10F SMP-11F TYP	SMP-10F SMP-11F MAX	SMP-11G MIN	SMP-11G TYP	SMP-11G MAX	UNITS
Zero-Scale Error	V_{ZS}	$V_{IN} = 0$, $V_{S/H} = 3.5V$, (Note 1)	–	0.75	2.0	–	1.0	4.0	–	2.7	10	mV
Input Bias Current	I_B	$V_{IN} = 0V$	–	50	90	–	80	140	–	120	250	nA
Leakage (Droop) Current	I_{DR}	SMP-10	–	0.05	0.25	–	0.080	0.65	–	–	–	nA
		SMP-11	–	0.5	1.8	–	0.6	2.8	–	0.7	5	
Droop Rate	dV_{CH}/dt	SMP-10	–	10	50	–	16	130	–	–	–	µV/ms
		SMP11	–	100	360	–	120	560	–	140	1000	
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm10V$, $R_L = 5k\Omega$ or $V_{IN} = \pm5V$, $R_L = 2.5k\Omega$	0.99955	0.99976	–	0.99950	0.99972	–	0.99930	0.99970	–	V/V
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm9V$ to ±18V	80	90	–	75	80	–	70	90	–	dB
Logic Control Input Current	I_{LC}	$V_{LC} = 0V$	–	–1	–2	–	–1	–3	–	–1	–4	µA
Logic Input	$I_{S/H}$	Sample Mode $V_{S/H} = 0.6V$	–	–5	–15	–	–5	–15	–	–5	–15	µA
		Hold Mode $V_{S/H} = 5.0V$	–	0.2	–	–	0.2	–	–	0.2	–	nA
Differential Logic Threshold	V_{TH}		0.8	1.3	2.0	0.8	1.3	2.0	0.8	1.3	2.0	V

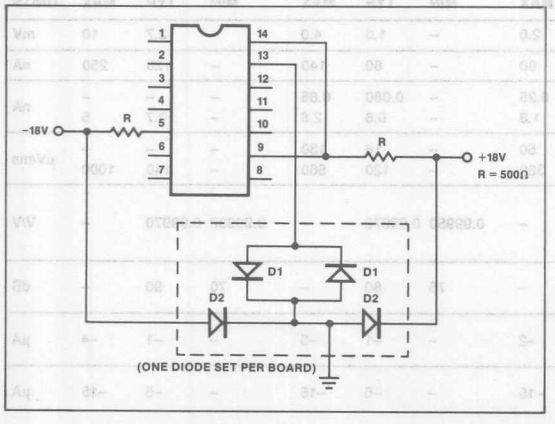
NOTE:
1. Measured 500µs after hold command.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $-55°C \le T_A \le +125°C$, unless otherwise noted.

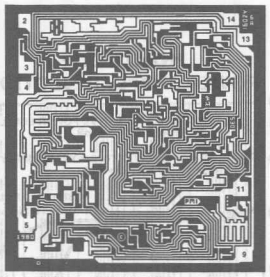
PARAMETER	SYMBOL	CONDITIONS		SMP-10A SMP-11A MIN	SMP-10A SMP-11A TYP	SMP-10A SMP-11A MAX	SMP-10 SMP-11B MIN	SMP-10 SMP-11B TYP	SMP-10 SMP-11B MAX	UNITS
Zero-Scale Error	V_{ZS}	$V_{IN} = 0$, $V_{S/H} = 3.5V$, (Note 1)		—	1.25	3.0	—	1.60	5.5	mV
Input Bias Current	I_B	$V_{IN} = 0V$		—	90	180	—	160	280	nA
Leakage (Droop) Current	I_{DR}	$T_A = -55°C$	SMP-10	—	0.050	0.50	—	0.080	1.22	nA
		$T_A = +125°C$	SMP-10	—	12	20	—	16	25	
		T_A = Full Range	SMP-11	—	12	20	—	16	25	
Droop Rate	dV_{CH}/dt	$T_A = -55°C$	SMP-10	—	10	100	—	16	250	μV/ms
		$T_A = +125°C$	SMP-10	—	2400	4000	—	3200	5000	
		T_A = Full Range	SMP-11	—	2400	4000	—	3200	5000	
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$, $R_L = 5k\Omega$ or $V_{IN} = \pm 5V$, $R_L = 2.5k\Omega$		0.99950	0.99972	—	0.99940	0.99968	—	V/V
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$		78	88	—	72	90	—	dB
Logic Control Input Current	I_{LC}	$V_{LC} = 0V$		—	−1	−3	—	−1	−5	μA
Logic Input	$I_{S/H}$	Sample Mode $V_{S/H} = 0.6V$		—	−5	−15	—	−5	−15	μA
		Hold Mode $V_{S/H} = 5.0V$		—	0.2	—	—	0.2	—	nA
Differential Logic Threshold	V_{TH}			0.6	1.3	2.0	0.6	1.3	2.0	V

NOTES:
1. Measured 500μs after hold command.

BURN-IN CIRCUIT



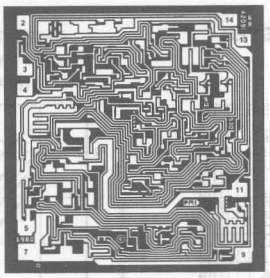
DICE CHARACTERISTICS



SMP-10

2. INPUT
3. NULL
4. NULL
5. NEGATIVE SUPPLY (SUBSTRATE)
7. OUTPUT
9. POSITIVE SUPPLY
11. HOLD CAPACITOR (C_H)
13. LOGIC THRESHOLD CONTROL (V_{LC})
14. SAMPLE/HOLD COMMAND

DIE SIZE 0.088 × 0.083 inch, 7304 sq. mils
(2.235 × 2.108 mm, 4.711 sq. mm)



SMP-11

2. INPUT
3. NULL
4. NULL
5. NEGATIVE SUPPLY (SUBSTRATE)
7. OUTPUT
9. POSITIVE SUPPLY
11. HOLD CAPACITOR (C_H)
13. LOGIC THRESHOLD CONTROL (V_{LC})
14. SAMPLE/HOLD COMMAND

WAFER TEST LIMITS at $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SMP-10N SMP-11N LIMIT	SMP-10G SMP-11G LIMIT	UNITS
Zero-Scale Error	V_{ZS}	$V_{IN} = 0$, $V_{S/H} = 3.5V$ Hold Mode, (Note 2)	1.5	3.0	mV MAX
Input Bias Current	I_B	$V_{IN} = 0V$	60	90	nA MAX
Leakage (Droop) Current	I_{DR}	SMP-10 SMP-11	0.10 1	0.25 2.5	nA MAX
Droop Rate	dV_{CH}/dt	SMP-10 SMP-11	20 200	50 500	μV/ms MAX
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$ or $V_{IN} = \pm 5V$	0.99963	0.99953	V/V MIN
Hold Capacitor Charging Current	I_{CH}	$V_{IN} - V_{OUT} \geq \pm 3V$	30	20	mA MIN
Input Voltage Range and/or Output Voltage Swing		$R_L = 2.5k\Omega$	±11	±10.5	V MIN
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$	82	77	dB MIN
Power Consumption	P_D	Sample Mode $V_{IN} = 0$	180	210	mW MAX
Logic Control Input Current	I_{LC}	$V_{LC} = 0V$	−2	−3	μA MAX
Logic Input	$I_{S/H}$	Sample Mode $V_{S/H} = 0.6V$ Hold Mode $V_{S/H} = 5V$	−15 0	−15 0	μA MAX nA MAX
Differential Logic Threshold	V_{TH}	$V_{LC} = 0$	2.0 0.8	2.0 0.8	V MAX V MIN

NOTES:
1. Measured 500μs after hold command.

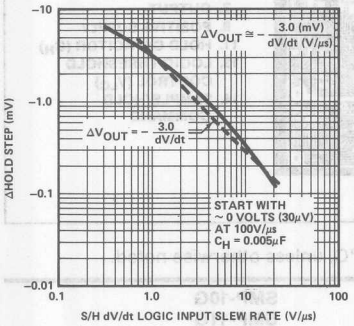
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $T_A = 25°C$, unless otherwise noted.

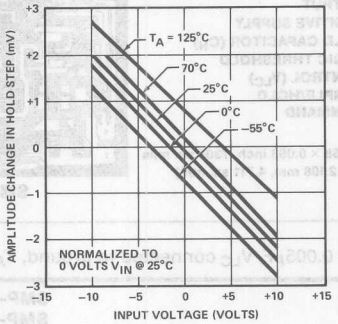
PARAMETER	SYMBOL	CONDITIONS	SMP-10N SMP-11N TYPICAL	SMP-10G SMP-11G TYPICAL	UNITS
Acquisition Time	t_{aq}	10V step to 0.1% of final value	3.5	3.5	μs
Aperture Time	t_{ap}		50	50	ns
Charge Transfer	Q_t	$V_{IN} = 0$, $V_{S/H} = 3.5V$	5	5	pC
Slew Rate	SR	$V_{IN} = \pm 10V$, $R_L = 2.5k\Omega$	10	10	V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

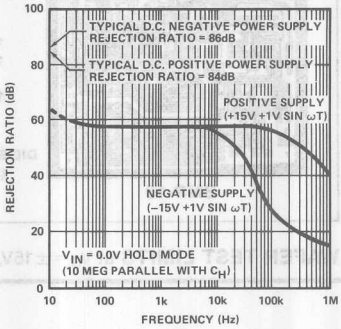
CHANGE IN HOLD STEP vs S/H $\frac{dV}{dt}$



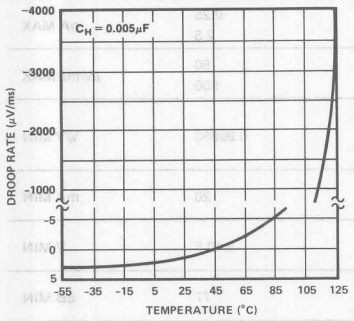
AMPLITUDE CHANGE IN HOLD STEP vs INPUT VOLTAGE



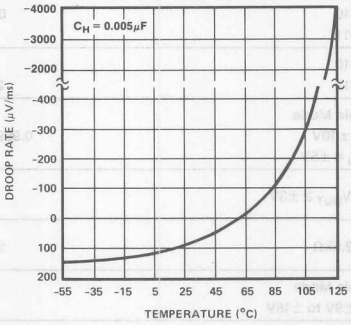
HOLD MODE POWER SUPPLY REJECTION



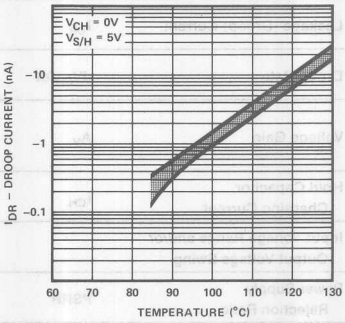
SMP-10 DROOP RATE vs TEMPERATURE



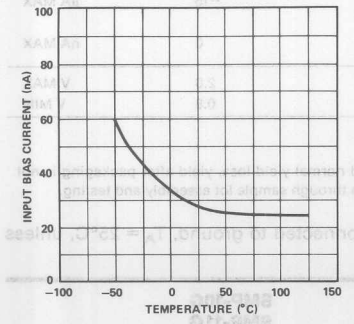
SMP-11 DROOP RATE vs TEMPERATURE



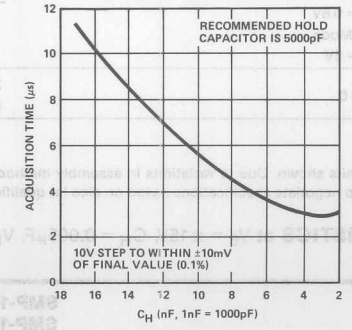
DROOP CURRENT vs TEMPERATURE



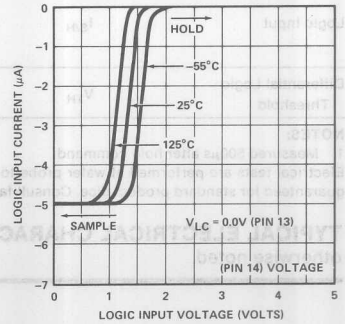
INPUT BIAS CURRENT vs TEMPERATURE



ACQUISITION TIME vs HOLD CAPACITOR

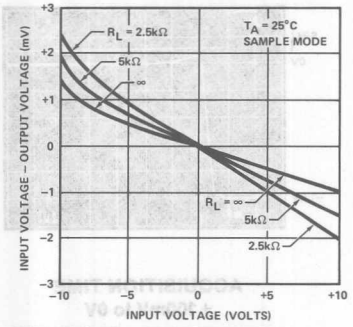


LOGIC INPUT CURRENT

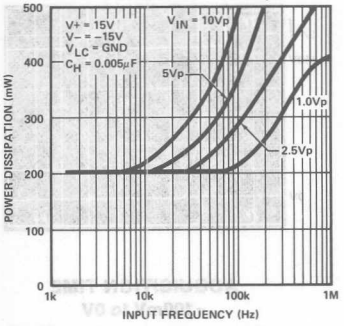


TYPICAL PERFORMANCE CHARACTERISTICS

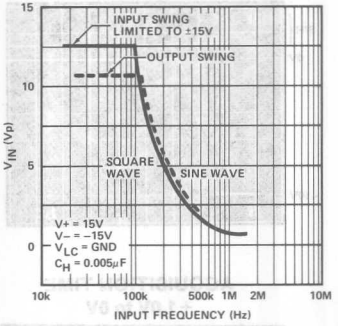
GAIN ERROR



POWER DISSIPATION vs INPUT FREQUENCY = V_p SIN ωT

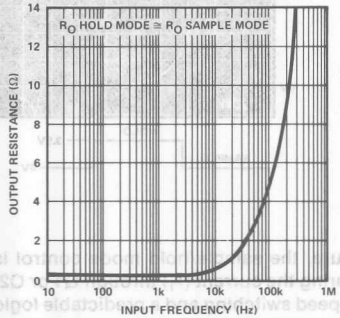


MAXIMUM INPUT SIGNAL AMPLITUDE vs FREQUENCY

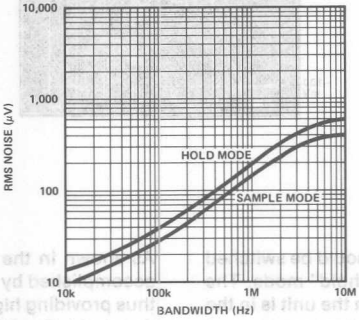


4

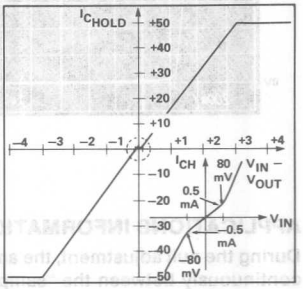
OUTPUT RESISTANCE vs FREQUENCY



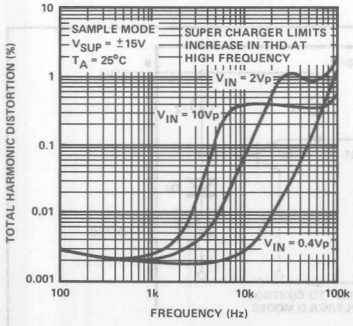
OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



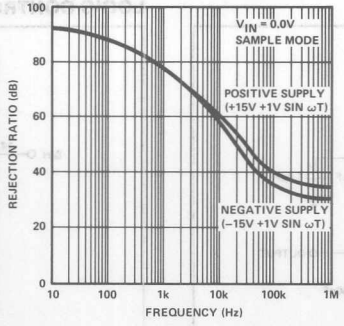
HOLD CAPACITOR CHARGING CURRENT vs INPUT OUTPUT VOLTAGE



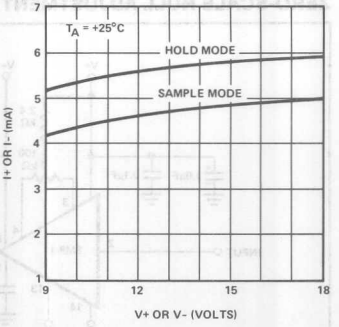
TOTAL HARMONIC DISTORTION vs FREQUENCY



SAMPLE MODE POWER SUPPLY REJECTION

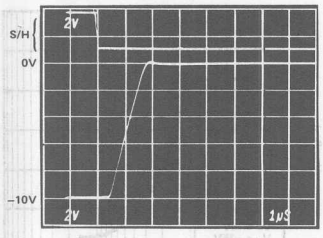


POWER SUPPLY CURRENT vs POWER SUPPLY VOLTAGE

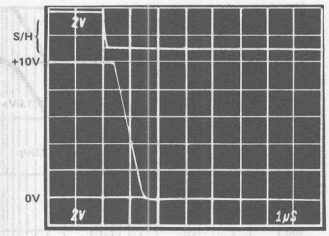


SMP-10/SMP-11 ACQUISITION TIMES

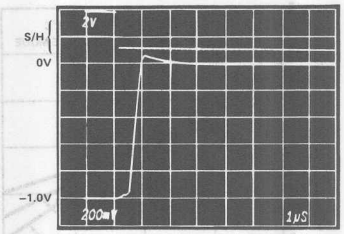
ACQUISITION TIME −10V to 0V



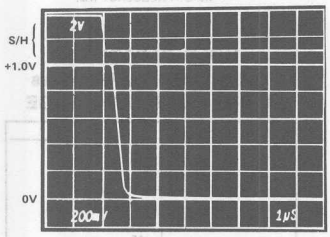
ACQUISITION TIME +10V to 0V



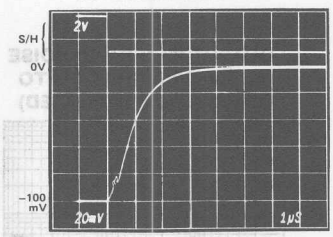
ACQUISITION TIME −1.0V to 0V



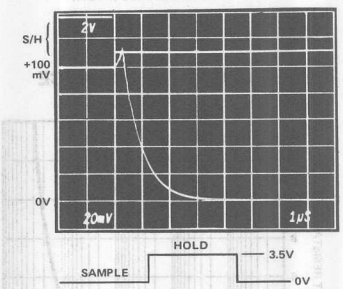
ACQUISITION TIME +1.0V to 0V



ACQUISITION TIME −100mV to 0V



ACQUISITION TIME +100mV to 0V

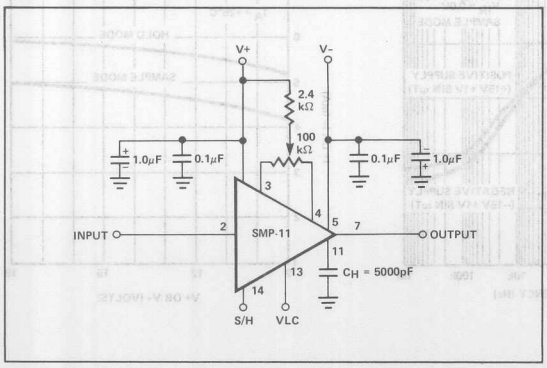


APPLICATIONS INFORMATION

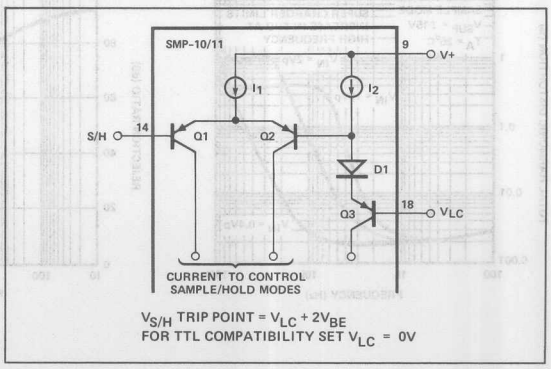
During the null adjustment, the amplifier should be switched continuously between the "sample" and "hold" mode. The error should be adjusted to read zero when the unit is in the "hold" mode. In this way, both offset voltage errors and charge transfer errors are adjusted to zero.

As shown in the Figure, the sample/hold mode control is accomplished by steering the current (I_1) through Q1 or Q2, thus providing high-speed switching and a predictable logic threshold. For TTL and DTL interface, simply ground V_{LC} (Pin 13). For CMOS, HTL and HNIL interface, the appropriate

ZERO-SCALE NULL ADJUSTMENT



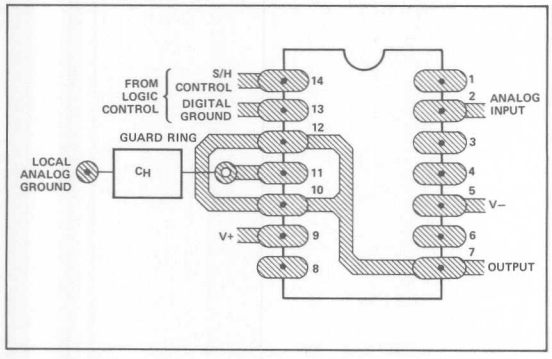
LOGIC CONTROL



threshold voltage, allowing for 2 diode drops for D1 and V_{BE} of Q3, should be applied to V_{LC}.

For proper operation, the V_{LC} (logic control) must always be at least 3.5V below the positive supply and 2.0V above the negative supply.

Sample-and-hold control voltage (S/H) must always be at least 2.8V above the negative supply.



GUARDING AND GROUNDING LAYOUT

The use of a ground plane is strongly recommended to minimize ground path resistances. Separate analog and digital grounds should be used, and it is advisable to keep these two ground systems isolated until they are tied back to the common system ground. Digital currents should not flow back to the system ground through the analog ground path.

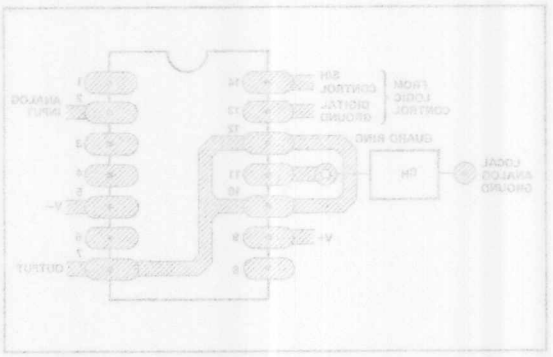
HOLD CAPACITOR RECOMMENDATIONS

The hold capacitor (C_H) acts as a memory element and also as a compensating capacitor for the sample-and-hold amplifier. For stable operation, a minimum value of 2000pF is recommended, with no limit set for the maximum value. The devices have been internally trimmed for C_H=5000pF. Other values of C_H will cause a zero-scale shift, which can be calculated from the following equation:

$$\Delta V_{ZS}(mV) = \frac{5\,(pC) \times 10^3}{C_H\,(pF)} - 1$$

The hold capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85°C, polystyrene capacitors are recommended, while teflon capacitors are recommended for higher temperature applications.

4



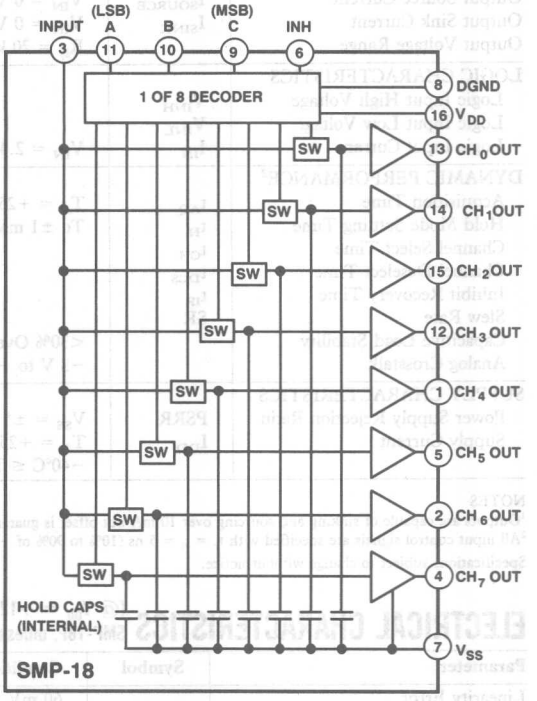
Octal Sample-and-Hold with Multiplexed Input

SMP-18

FEATURES
- High Speed Version of SMP-08
- Internal Hold Capacitors
- Low Droop Rate
- TTL/CMOS Compatible Logic Inputs
- Single or Dual Supply Operation
- Break-Before-Make Channel Addressing
- Compatible With CD4051 Pinout
- Low Cost

APPLICATIONS
- Multiple Path Timing Deskew for A.T.E.
- Memory Programmers
- Mass Flow/Process Control Systems
- Multichannel Data Acquisition Systems
- Robotics and Control Systems
- Medical and Analytical Instrumentation
- Event Analysis
- Stage Lighting Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The SMP-18 is a monolithic octal sample-and-hold; it has eight internal buffer amplifiers, input multiplexer, and internal hold capacitors. It is manufactured in an advanced oxide isolated CMOS technology to obtain high accuracy, low droop rate, and fast acquisition time. The SMP-18 has a typical linearity error of only 0.01% and can accurately acquire a 10-bit input signal to ±1/2 LSB in less than 2.5 microseconds. The SMP-18's output swing includes the negative supply in both single and dual supply operation.

The SMP-18 was specifically designed for systems that use a calibration cycle to adjust a multiple of system parameters. The low cost and high level of integration make the SMP-18 ideal for calibration requirements that have previously required an ASIC, or high cost multiple D/A converters.

The SMP-18 is also ideally suited for a wide variety of sample-and-hold applications including amplifier offset or VCA gain adjustments. One or more SMP-18s can be used with single or multiple DACs to provide multiple set points within a system.

The SMP-18 offers significant cost and size reduction over discrete designs. It is available in a 16-pin hermetic or plastic DIP or surface mount SOIC package. The SMP-18 is a higher speed direct replacement for the SMP-08.

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +15 V, V_{SS} = −5 V, DGND = 0 V, R_L = No Load, T_A = −40°C to +85°C for SMP-18F, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Linearity Error		−3 V ≤ V_{IN} ≤ +3 V		0.01		%
Buffer Offset Voltage	V_{OS}	T_A = +25°C, V_{IN} = 0 V		2.5	10	mV
		−40°C ≤ T_A ≤ +85°C, V_{IN} = 0 V		3.5	20	mV
Hold Step	V_{HS}	V_{IN} = 0 V		4	6	mV
Droop Rate	$\Delta V_{CH}/\Delta t$	T_A = +25°C, V_{IN} = 0 V		2	40	mV/s
Output Source Current	I_{SOURCE}	V_{IN} = 0 V[1]	1.2			mA
Output Sink Current	I_{SINK}	V_{IN} = 0 V[1]	0.5			mA
Output Voltage Range		R_L = 20 kΩ	−3.0		+3.0	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4			V
Logic Input Low Voltage	V_{INL}				0.8	V
Logic Input Current	I_{IN}	V_{IN} = 2.4 V		0.5	1	μA
DYNAMIC PERFORMANCE[2]						
Acquisition Time	t_{AQ}	T_A = +25°C, −3 V to +3 V to 0.1%		3.5		μs
Hold Mode Settling Time	t_H	To ±1 mV of Final Value		1		μs
Channel Select Time	t_{CH}			90		ns
Channel Deselect Time	t_{DCS}			45		ns
Inhibit Recovery Time	t_{IR}			90		ns
Slew Rate	SR			6		V/μs
Capacitive Load Stability		<30% Overshoot		500		pF
Analog Crosstalk		−3 V to +3 V Step		−72		dB
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	V_{SS} = ±5 V to ±6 V	60	75		dB
Supply Current	I_{DD}	T_A = +25°C		5.5	7.5	mA
		−40°C ≤ T_A ≤ +85°C		7.5	9.5	mA

NOTES
[1]Outputs are capable of sinking and sourcing over 10 mA but offset is guaranteed at specified load levels.
[2]All input control signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +12 V, V_{SS} = 0 V, DGND = 0 V, R_L = No Load, T_A = −40°C to +85°C for SMP-18F, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Linearity Error		60 mV ≤ V_{IN} ≤ 10 V		0.01		%
Buffer Offset Voltage	V_{OS}	T_A = +25°C, V_{IN} = 6 V		2.5	10	mV
		−40°C ≤ T_A ≤ +85°C, V_{IN} = 6 V		3.5	20	mV
Hold Step	V_{HS}	V_{IN} = 6 V		4	6	mV
Droop Rate	$\Delta V_{CH}/\Delta t$	T_A = +25°C, V_{IN} = 6 V		2	40	mV/s
Output Source Current	I_{SOURCE}	V_{IN} = 6 V[1]	1.2			mA
Output Sink Current	I_{SINK}	V_{IN} = 6 V[1]	0.5			mA
Output Voltage Range		R_L = 20 kΩ	0.06		10.0	V
		R_L = 10 kΩ	0.06		9.5	
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4			V
Logic Input Low Voltage	V_{INL}				0.8	V
Logic Input Current	I_{IN}	V_{IN} = 2.4 V		0.5	1	μA
DYNAMIC PERFORMANCE[2]						
Acquisition Time	t_{AQ}	T_A = +25°C, 0 to 10 V to 0.1%		2.5		μs
Hold Mode Settling Time	t_H	To ±1 mV of Final Value		1		μs
Channel Select Time	t_{CH}			90		ns
Channel Deselect Time	t_{DCS}			45		ns
Inhibit Recovery Time	t_{IR}			90		ns
Slew Rate[3]	SR			7		V/μs
Capacitive Load Stability		<30% Overshoot		500		pF
Analog Crosstalk		0 to 10 V Step		−72		dB

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	$10.8\ V \le V_{DD} \le 13.2\ V$	60	75		dB
Supply Current	I_{DD}	$T_A = +25°C$		6.0	8.0	mA
		$-40°C \le T_A \le +85°C$		8.0	10.0	mA

NOTES
[1]Outputs are capable of sinking and sourcing over 10 mA but offset is guaranteed at specified load levels.
[2]All input control signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[3]Slew rate is measured in the sample mode with a 0 to 10 V step from 20% to 80%.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to DGND . . . . . −0.3 V, 17 V
V_{DD} to V_{SS} . . . . . −0.3 V, 17 V
V_{LOGIC} to DGND . . . . . −0.3 V, V_{DD}
V_{IN} to DGND . . . . . V_{SS}, V_{DD}
V_{OUT} to DGND . . . . . V_{SS}, V_{DD}
Analog Output Current . . . . . ±20 mA
(Not short-circuit protected)
Operating Temperature Range
FQ, FP, FS . . . . . −40°C to +85°C
Junction Temperature . . . . . +150°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
16-Pin Hermetic DIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOIC (S)	92	27	°C/W

NOTES
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and plastic DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

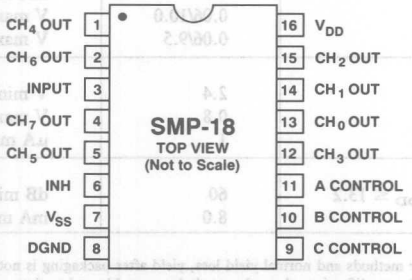
4

CAUTION

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.
2. Digital inputs and outputs are protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam or packaging at all times until ready to use. Use proper antistatic handling procedures.
3. Remove power before inserting or removing units from their sockets.



PIN CONNECTIONS



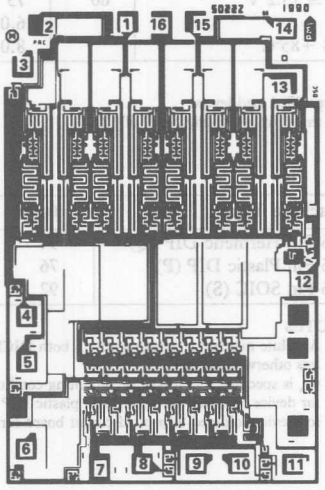
ORDERING GUIDE*

Package: 16-Pin DIP/SOIC		Operating
Cerdip 16-Pin	Plastic 16-Pin	Temperature Range
TBA†		MIL
SMP-18FQ	SMP-18FP	XIND
	SMP-18FS	XIND

NOTES
*Burn-in is available on industrial temperature range parts in cerdip and plastic DIP packages.
†Consult factory for 883 data sheet.

SMP-18

DICE CHARACTERISTICS



1. CH_4 OUT
2. CH_6 OUT
3. INPUT
4. CH_7 OUT
5. CH_5 OUT
6. INH
7. V_{SS}
8. DGND
9. C CONTROL
10. B CONTROL
11. A CONTROL
12. CH_3 OUT
13. CH_0 OUT
14. CH_1 OUT
15. CH_2 OUT
16. V_{DD}

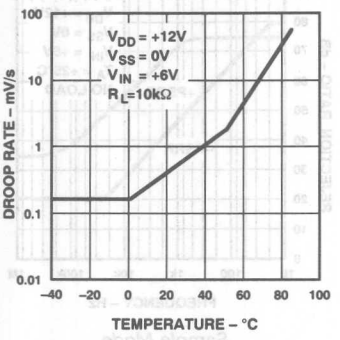
DIE SIZE 0.080 x 0.120 INCH, 9,600 sq. mils
(2.032 x 3.048 mm, 6.193 sq. mm)

WAFER TEST LIMITS (@ V_{DD} = +12 V, V_{SS} = DGND = 0 V, R_L = No Load, T_A = +25°C for SMP-18GBC, unless otherwise specified)

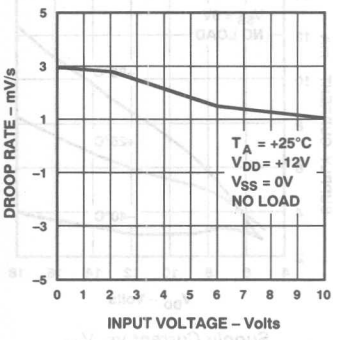
Parameter	Symbol	Conditions	Limits	Units
Buffer Offset Voltage	V_{OS}	V_{IN} = +6 V	20	mV max
Droop Rate	$\Delta V_{CH}/\Delta t$	V_{IN} = +6 V	40	mV/s max
Output Source Current	I_{SOURCE}	V_{IN} = +6 V	1.2	mA min
Output Sink Current	I_{SINK}	V_{IN} = +6 V	0.5	mA min
Output Voltage Range		R_L = 20 kΩ	0.06/10.0	V max/min
		R_L = 10 kΩ	0.06/9.5	V max/min
LOGIC CHARACTERISTICS				
Logic Input High Voltage	V_{INH}		2.4	V min
Logic Input Low Voltage	V_{INL}		0.8	V max
Logic Input Current	I_{IN}	V_{IN} = 2.4 V	1	μA max
SUPPLY CHARACTERISTICS				
Power Supply Rejection Ratio	PSRR	10.8 V ≤ V_{DD} ≤ 13.2	60	dB min
Supply Current	I_{DD}		8.0	mA max

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

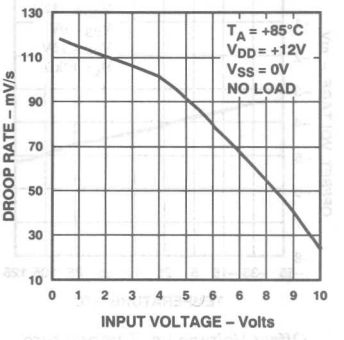
Typical Performance Characteristics—SMP-18



Droop Rate vs. Temperature

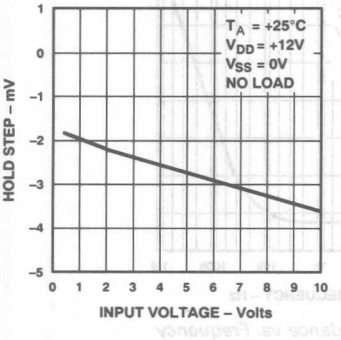


Droop Rate vs. Input Voltage

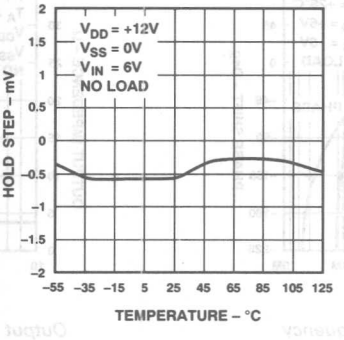


Droop Rate vs. Input Voltage

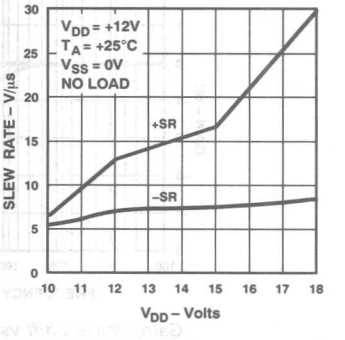
4



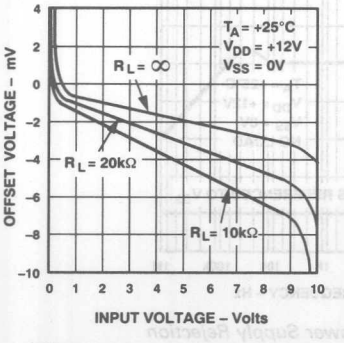
Hold Step vs. Input Voltage



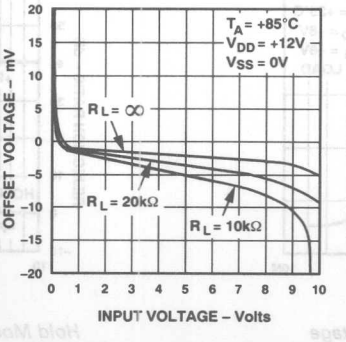
Hold Step vs. Temperature



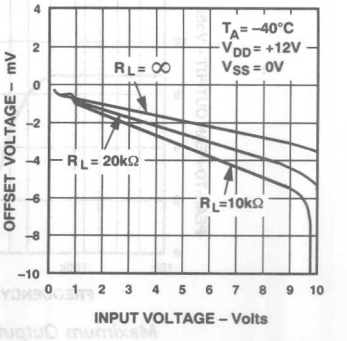
Slew Rate vs. V_{DD}



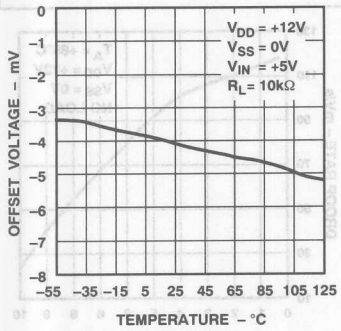
Offset Voltage vs. Input Voltage



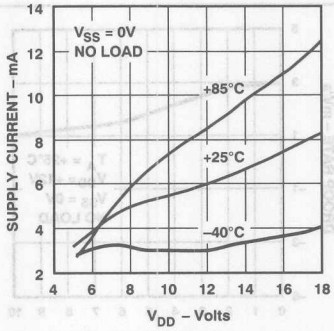
Offset Voltage vs. Input Voltage



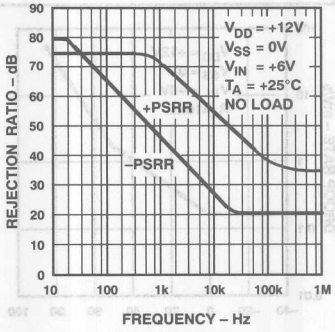
Offset Voltage vs. Input Voltage



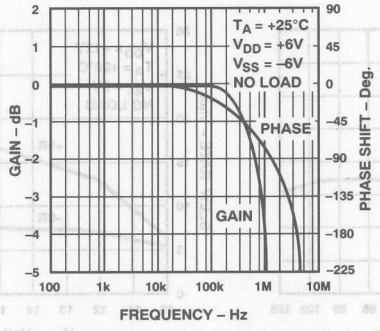
Offset Voltage vs. Temperature



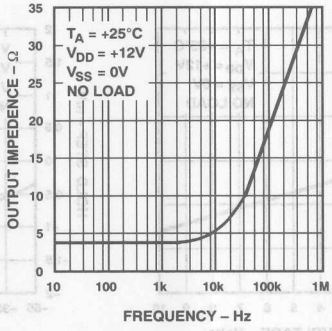
Supply Current vs. V_{DD}



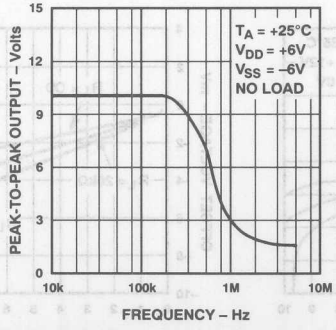
Sample Mode Power Supply Rejection



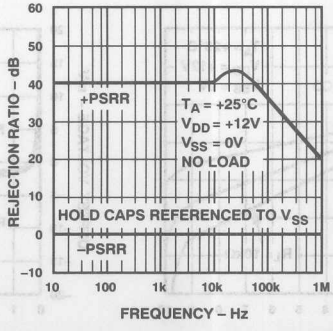
Gain, Phase Shift vs. Frequency



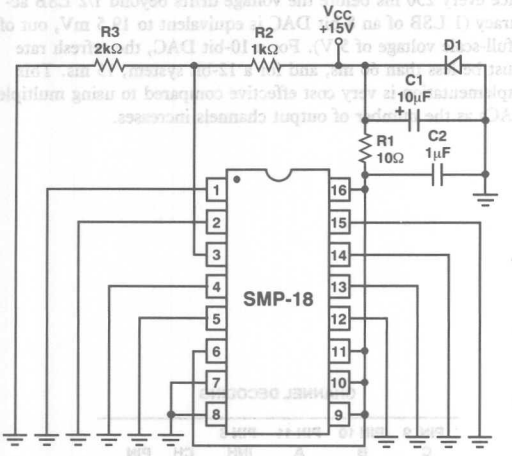
Output Impedance vs. Frequency



Maximum Output Voltage vs. Frequency



Hold Mode Power Supply Rejection



Burn-in Circuit

APPLICATIONS INFORMATION

The SMP-18, a multiplexed octal S/H, minimizes board space in systems requiring cycled calibration or an array of control voltages. When used in conjunction with a low cost 10-bit D/A, the SMP-18 can easily be integrated into microprocessor based systems. Since the SMP-18 features break-before-make switching and an internal decoder, no external logic is required. The SMP-18 has an internally regulated TTL supply so that TTL/CMOS compatibility is maintained over the full supply range. See Figure 1 for channel decode address information.

POWER SUPPLIES

The SMP-18 is capable of operating with either single or dual supplies, over a voltage range of 7 to 15 volts. Based on the supply voltages chosen, V_{DD} and V_{SS} establish the output voltage range, which is:

$$(V_{SS} + 0.06\ V) \leq V_{OUT} \leq (V_{DD} - 2\ V)$$

Note that several specifications, including acquisition time, offset and output voltage, compliance will degrade for supply voltages of less than 7 V.

If split supplies are used, the negative supply should be bypassed with a 0.1 µF capacitor in parallel with a 10 µF to ground. The internal hold capacitors are connected to this supply pin and any noise will appear at the outputs.

In single supply applications, it is extremely important that the V_{SS} (negative supply) pin is connected to a clean ground. The hold capacitors are internally tied to the V_{SS} (negative) rail. Any ground noise or disturbance will directly couple to the output of the sample-and-hold, degrading the signal-to-noise performance. The analog and digital ground traces on the circuit board should be physically separated to reduce digital switching noise from entering the analog circuitry.

POWER SUPPLY SEQUENCING

V_{DD} should be applied to the SMP-18 before the logic input signals. The SMP-18 has been designed to be immune to latch-up, but standard precautions should still be taken.

OUTPUT BUFFERS (Pins 1, 2, 4, 5, 12, 13, 14, 15)

The buffer offset specification is 10 mV; this is less than 1/2 LSB of an 8-bit DAC with 10 V full scale. The hold step (magnitude of step caused in the output voltage when switching from sample-to-hold mode, also referred to as the pedestal error or sample-to-hold offset) is about 4 mV with little variation over the full output voltage range. The droop rate of a held channel is 2 mV/s typical and 40 mV/s maximum.

The buffers are designed to drive loads connected to ground. The outputs can source more than 20 mA, over the full voltage range, but have limited current sinking capability near V_{SS}. In split supply operation, symmetrical output swings can be obtained by restricting the output range to 2 V from either supply.

On-chip SMP-18 buffers eliminate potential stability problems associated with external buffers; outputs are stable with capacitive loads up to 500 pF. However, since the SMP-18's buffer outputs are not short circuit protected, care should be taken to avoid shorting any output to the supplies or ground.

SIGNAL INPUT (Pin 3)

The signal input should be driven from a low impedance voltage source such as the output of an op amp. The op amp should have a high slew rate and fast settling time if the SMP-18's acquisition time characteristics are to be maintained. As with all CMOS devices, all input voltages should be kept within range of the supply rails ($V_{SS} \leq V_{IN} \leq V_{DD}$) to avoid the possibility of latch-up. If single supply operation is desired, op amps such as the OP-21, OP-80, or OP-90 that have input and output voltage compliances including ground, can be used to drive the inputs. Split supplies, such as ±7.5 V, can be used with the SMP-18.

APPLICATION TIPS

All unused digital inputs should be connected to logic LOW. For analog inputs that may become temporarily disconnected, a resistor to V_{DD}, V_{SS} or analog ground should be used with a value ranging from 200 kΩ to 1 MΩ.

Do not apply signals to the SMP-18 with power off unless the input current is limited to less than 10 mA.

TYPICAL APPLICATIONS

An 8-Channel Multiplexed D/A Converter

Figure 1 illustrates a typical multiplexing function of the SMP-18. It is used to sample-and-hold eight different output voltages corresponding to eight different digital codes from a D/A converter. The SMP-18's droop rate of 40 mV/s requires a refresh once every 250 ms before the voltage drifts beyond 1/2 LSB accuracy (1 LSB of an 8-bit DAC is equivalent to 19.5 mV, out of a full-scale voltage of 5 V). For a 10-bit DAC, the refresh rate must be less than 60 ms, and for a 12-bit system, 15 ms. This implementation is very cost effective compared to using multiple DACs as the number of output channels increases.

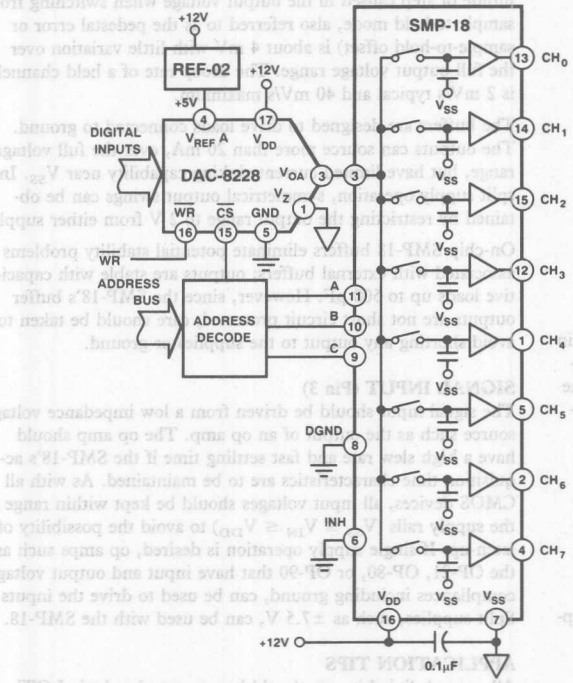


Figure 1. 8-Channel Multiplexed D/A Converter

CHANNEL DECODING

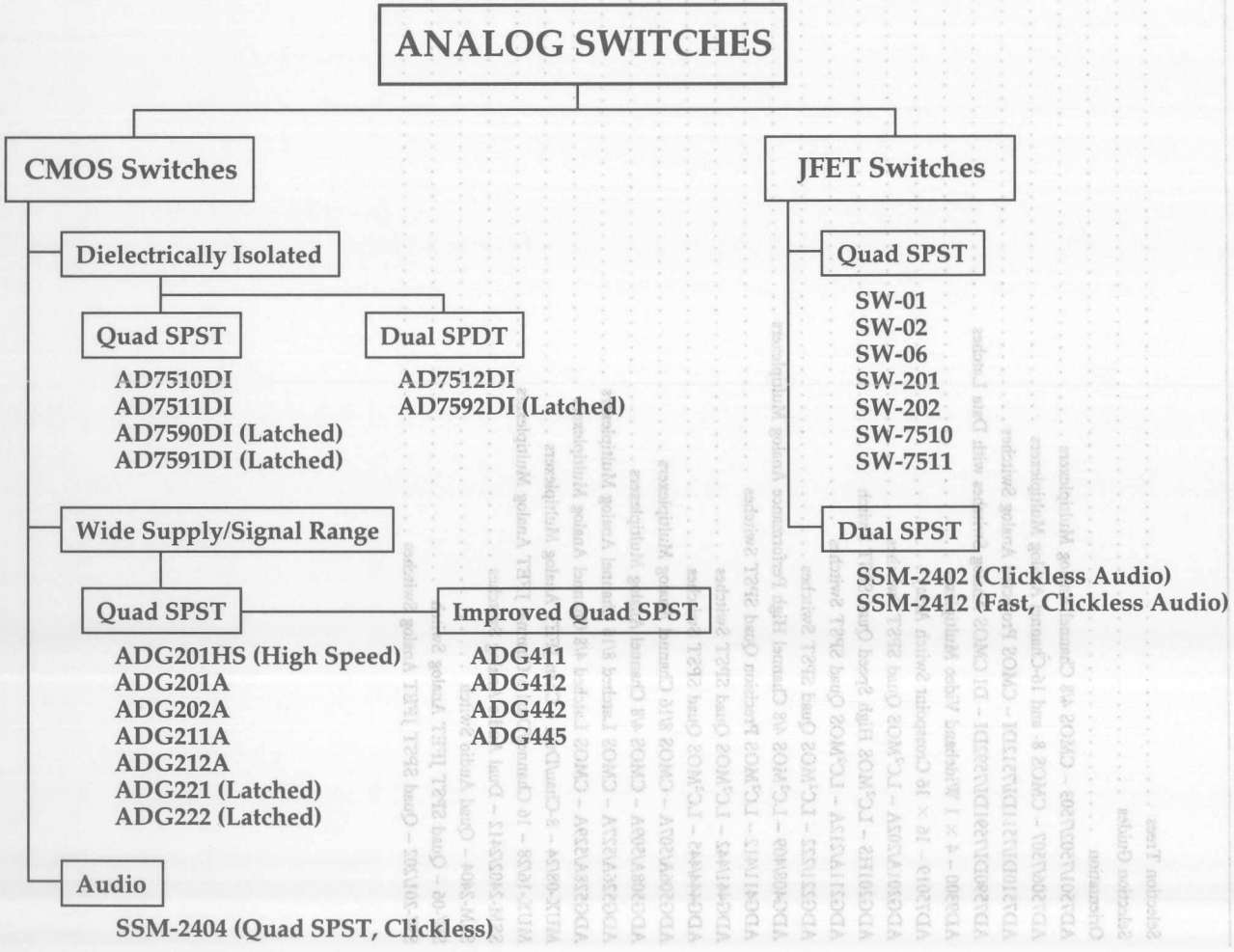
PIN 9 C	PIN 10 B	PIN 11 A	PIN 6 INH	CH	PIN
0	0	0	0	0	13
0	0	1	0	1	14
0	1	0	0	2	15
0	1	1	0	3	12
1	0	0	0	4	1
1	0	1	0	5	5
1	1	0	0	6	2
1	1	1	0	7	4
X	X	X	1	NONE	–

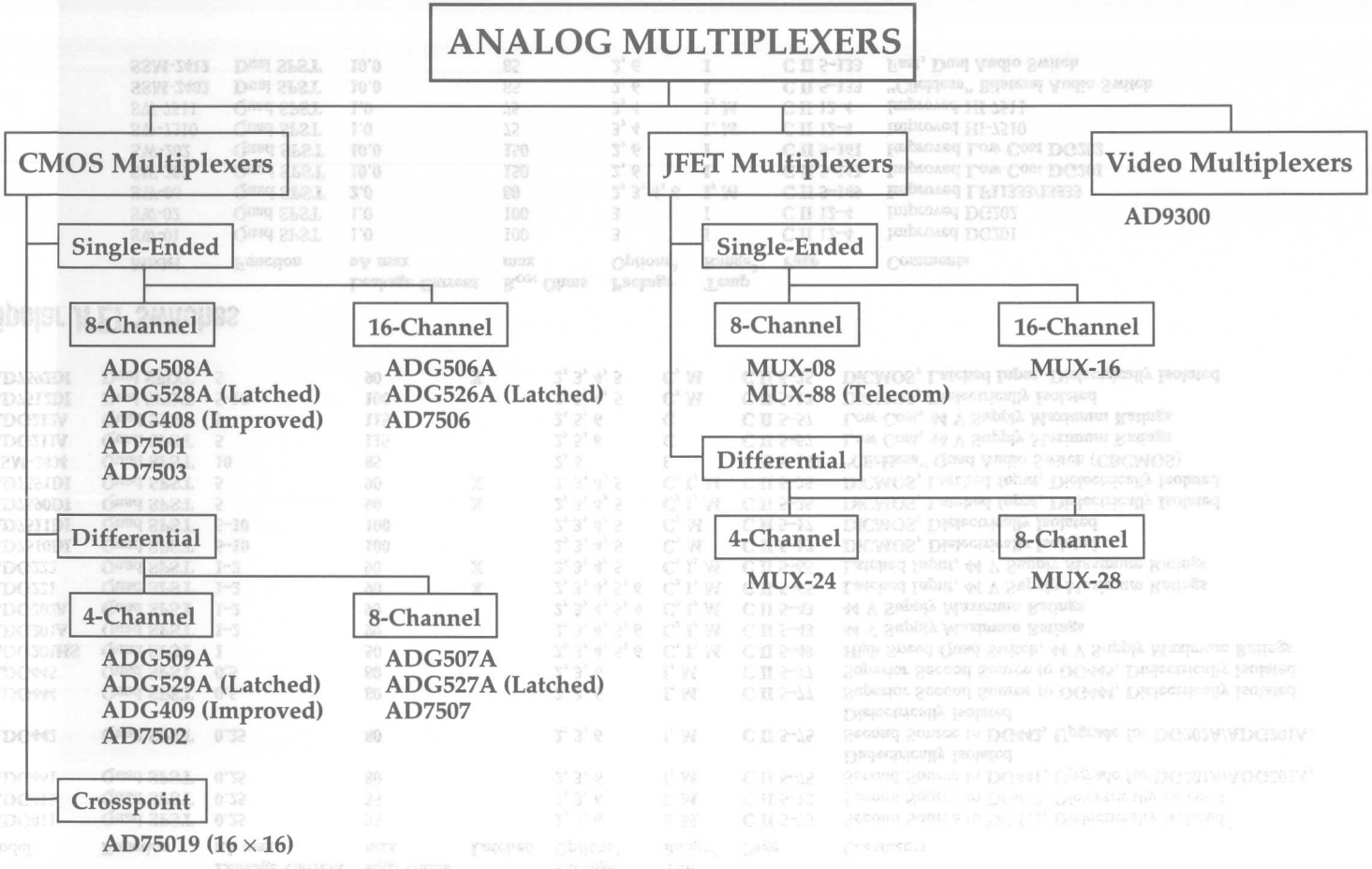
Switches & Multiplexers
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AD7590DI/7591DI/7592DI – DI CMOS Analog Switches with Data Latches	5–25
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ADG201A/202A – LC²MOS Quad SPST Switches	5–43
ADG201HS – LC²MOS High Speed Quad SPST Switch	5–49
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ADG221/222 – LC²MOS Quad SPST Switches	5–65
ADG408/409 – LC²MOS 4/8 Channel High Performance Analog Multiplexers	5–71
ADG411/412 – LC²MOS Precision Quad SPST Switches	5–73
ADG441/442 – LC²MOS Quad SPST Switches	5–75
ADG444/445 – LC²MOS Quad SPST Switches	5–77
ADG506A/507A – CMOS 8/16 Channel Analog Multiplexers	5–79
ADG508A/509A – CMOS 4/8 Channel Analog Multiplexers	5–87
ADG526A/527A – CMOS Latched 8/16 Channel Analog Multiplexers	5–95
ADG528A/529A – CMOS Latched 4/8 Channel Analog Multiplexers	5–103
MUX-08/24 – 8-Chan/Dual 4-Chan JFET Analog Multiplexers	5–111
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SW-06 – Quad SPST JFET Analog Switch	5–149
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5

Selection Tree
Switches & Multiplexers




ANALOG MULTIPLEXERS
CMOS Multiplexers
Single-Ended
8-Channel
ADG508A
ADG528A (Latched)
ADG408 (Improved)
AD7501
AD7503
16-Channel
ADG506A
ADG526A (Latched)
AD7506
Differential
4-Channel
ADG509A
ADG529A (Latched)
ADG409 (Improved)
AD7502
8-Channel
ADG507A
ADG527A (Latched)
AD7507
Crosspoint
AD75019 (16 × 16)
JFET Multiplexers
Single-Ended
8-Channel
MUX-08
MUX-88 (Telecom)
16-Channel
MUX-16
Differential
4-Channel
MUX-24
8-Channel
MUX-28
Video Multiplexers
AD9300

Selection Guide
Switches & Multiplexers

CMOS Switches

Model	Function	Leakage Current nA max	R_{ON} Ohms max	Latched	Package Options[1]	Temp Range[2]	Page	Comments
*ADG411	Quad SPST	0.25	35		2, 3, 6	I, M	C II 5–73	Second Source to DG411, Dielectrically Isolated
*ADG412	Quad SPST	0.25	35		2, 3, 6	I, M	C II 5–73	Second Source to DG412, Dielectrically Isolated
*ADG441	Quad SPST	0.25	80		2, 3, 6	I, M	C II 5–75	Second Source to DG441, Upgrade for DG201A/ADG201 Dielectrically Isolated
*ADG442	Quad SPST	0.25	80		2, 3, 6	I, M	C II 5–75	Second Source to DG442, Upgrade for DG202A/ADG201 Dielectrically Isolated
*ADG444	Quad SPST	0.5	80		2, 3, 6	I, M	C II 5–77	Superior Second Source to DG444, Dielectrically Isolated
*ADG445	Quad SPST	0.5	80		2, 3, 6	I, M	C II 5–77	Superior Second Source to DG445, Dielectrically Isolated
ADG201HS	Quad SPST	1	50		2, 3, 4, 5, 6	C, I, M	C II 5–49	High Speed Quad Switch, 44 V Supply Maximum Ratings
ADG201A	Quad SPST	1–2	90		2, 3, 4, 5, 6	C, I, M	C II 5–43	44 V Supply Maximum Ratings
ADG202A	Quad SPST	1–2	90		2, 3, 4, 5, 6	C, I, M	C II 5–43	44 V Supply Maximum Ratings
ADG221	Quad SPST	1–2	90	X	2, 3, 4, 5, 6	C, I, M	C II 5–65	Latched Input, 44 V Supply Maximum Ratings
ADG222	Quad SPST	1–2	90	X	2, 3, 4, 5	C, I, M	C II 5–65	Latched Input, 44 V Supply Maximum Ratings
AD7510DI	Quad SPST	5–10	100		2, 3, 4, 5	C, M	C II 5–17	DiCMOS, Dielectrically Isolated
AD7511DI	Quad SPST	5–10	100		2, 3, 4, 5	C, M	C II 5–17	DiCMOS, Dielectrically Isolated
AD7590DI	Quad SPST	5	90	X	2, 3, 4, 5	C, I, M	C II 5–25	DiCMOS, Latched Input, Dielectrically Isolated
AD7591DI	Quad SPST	5	90	X	2, 3, 4, 5	C, I, M	C II 5–25	DiCMOS, Latched Input, Dielectrically Isolated
*SSM-2404	Quad SPST	10	85		2, 6	I	C II 5–147	"Clickless" Quad Audio Switch (CBCMOS)
ADG211A	Quad SPST	5	115		2, 5, 6	C	C II 5–57	Low Cost, 44 V Supply Maximum Ratings
ADG212A	Quad SPST	5	115		2, 5, 6	C	C II 5–57	Low Cost, 44 V Supply Maximum Ratings
AD7512DI	Dual SPDT	5–10	100		2, 3, 4, 5	C, M	C II 5–17	DiCMOS, Dielectrically Isolated
AD7592DI	Dual SPDT	5	90	X	2, 3, 4, 5	C, M	C II 5–25	DiCMOS, Latched Input, Dielectrically Isolated

Bipolar JFET Switches

Model	Function	Leakage Current nA max	R_{ON} Ohms max	Package Options[1]	Temp Range[2]	Page	Comments
SW-01	Quad SPST	1.0	100	3	I	C II 12–4	Improved DG201
SW-02	Quad SPST	1.0	100	3	I	C II 12–4	Improved DG202
SW-06	Quad SPST	2.0	80	2, 3, 4, 6	I, M	C II 5–149	Improved LF11333/13333
SW-201	Quad SPST	10.0	150	2, 6	I	C II 5–161	Improved Low Cost DG201
SW-202	Quad SPST	10.0	150	2, 6	I	C II 5–161	Improved Low Cost DG202
SW-7510	Quad SPST	1.0	75	3, 4	I, M	C II 12–4	Improved HI-7510
SW-7511	Quad SPST	1.0	75	3, 4	I, M	C II 12–4	Improved HI-7511
SSM-2402	Dual SPST	10.0	85	2, 6	I	C II 5–133	"Clickless" Bilateral Audio Switch
SSM-2412	Dual SPST	10.0	85	2, 6	I	C II 5–133	Fast, Dual Audio Switch

Analog CMOS Multiplexers

Model	Function	Leakage Current nA max	R_{ON} Ohms max	Latched	Package Options[1]	Temp Range[2]	Page	Comments
*AD75019	16:16	10	300		5	C, I	C II 5–39	16 × 16 Analog Crosspoint, Serial Interface
ADG506A	16:1	1	280		2, 3, 4, 5, 6	C, I, M	C II 5–79	Superior Second Source to DG506A
ADG526A	16:1	1	280	X	2, 3, 4, 5, 6	C, I, M	C II 5–95	Superior Second Source to DG526A
*AD7506	16:1	1-5	300		2, 3, 4	C, M	C II 5–13	
ADG507A	Diff. 8:1	1	280		2, 3, 4, 5, 6	C, I, M	C II 5–79	Superior Second Source to DG507A
ADG527A	Diff. 8:1	1	280	X	2, 3, 4, 5, 6	C, I, M	C II 5–95	Superior Second Source to DG527A
*AD7507	Diff. 8:1	1-5	300		2, 3, 4	C, M	C II 5–13	
*ADG408	8:1	0.5	100		2, 3, 6	C, I, M	C II 5–71	Superior Second Source to DG408
ADG508A	8:1	1	300		2, 3, 4, 5, 6	C, I, M	C II 5–87	Superior Second Source to DG508A
ADG528A	8:1	1	300	X	2, 3, 4, 5	C, I, M	C II 5–103	Superior Second Source to DG528A
AD7501	8:1	1–5	300		2, 3, 4	C, M	C II 5–9	
AD7503	8:1	1–5	300		2, 3, 4	C, M	C II 5–9	
*ADG409	Diff. 4:1	0.5	100		2, 3, 6	C, I, M	C II 5–71	Superior Second Source to DG409
ADG509A	Diff. 4:1	1	300		2, 3, 4, 5, 6	C, I, M	C II 5–87	Superior Second Source to DG509A
ADG529A	Diff. 4:1	1	300	X	2, 3, 4, 5	C, I, M	C II 5–103	Superior Second Source to DG529A
AD7502	Diff. 4:1	1–5	300		2, 3, 4	C, M	C II 5–9	

Analog Bipolar JFET Multiplexers

Model	Function	Leakage Current nA max	R_{ON} Ohms max	Package Options[1]	Temp Range[2]	Page	Comments
MUX-08	8:1	1.0	300	2, 3, 4, 6	C, I, M	C II 5–111	Improved DG508
MUX-16	16:1	1.0	380	2, 3, 4, 5	I, M	C II 5–123	Improved DG506
MUX-24	Diff. 4:1	1.0	300	2, 3, 4, 6	C, I, M	C II 5–111	Improved DG509
MUX-28	Diff. 8:1	1.0	380	2, 3, 4, 5	I, M	C II 5–123	Improved DG507
MUX-88	8:1	100	400	3	I	C II 12–4	8-Channel Telecom Multiplexer

Video Multiplexer

Model	Function	Full Power BW MHz min	Crosstalk Rejection f = 10 MHz dB	Package Options[1]	Temp Range[2]	Page	Comments
AD9300	4:1	30	75	3, 4	C, M	C II 5–31	Wideband Video Mux

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-in-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92.

[2]Temperature Ranges: C = Commercial, 0 to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.

Boldface Type: Product recommended for new design.

*New product since the publication of the most recent Databooks

Orientation
Switches & Multiplexers

Solid-state analog multiplexers and switches have become an essential and ubiquitous component in the design of many electronic systems which require the ability to control and select a specified transmission path for an analog signal. These semiconductor devices are utilized in a wide range of applications including data acquisition, process control, instrumentation, video systems, and telephony systems. Analog Devices offers a complete line of monolithic analog multiplexers and switches in the commercial, industrial, and military grades which are well suited for these applications and environments.

In selecting analog multiplexers and switches, attention must be paid to several key specifications which affect a system's performance. The acquisition of an analog input signal within a specified time and error band is a primary concern affected by the on-channel resistance (R_{ON}) and the effective output capacitance ($C_{D(ON)}$) specifications in conjunction with the effective load impedance. The total output capacitance, consisting of both the multiplexer/switch output and load capacitance, will form an R-C constant with R_{ON}, thus affecting both the bandwidth and the settling time to within a specified error band. A low R_{ON} which remains relatively constant over the analog input range will ensure minimum signal attenuation and distortion. High crosstalk and off-isolation specifications prevent unselected signals from affecting the signal path, thus maintaining a high signal-to-noise ratio. Break-before-make switching ensures that no two channel inputs are simultaneously connected, thus avoiding potential damage to the input signal sources. Switching time and settling time will determine the maximum handling frequency of the multiplexer as determined by the sampling theorem. Voltage offset contributions from a multiplexer/switch are a result of the effective leakage currents flowing through R_{ON}, R_{SOURCE}, and R_{LOAD}.

Our product line can be categorized by the particular fabrication process employed into the following three distinct product families: CMOS, bipolar-JFET, and advanced bipolar (video). An understanding of the advantages and limitations of each of these processes is beneficial in selecting the best analog switch or multiplexer for a particular application. Devices fabricated on a CMOS or a bipolar-JFET process are bidirectional, and their input and output may be transposed, thus allowing a multiplexer to be configured as a demultiplexer.

The CMOS process utilizes both N- and P-channel MOSFETs in the design of the analog switch, digital control logic, and switch driver circuits. These bidirectional analog switches consist of a parallel combination of P- and N-channel MOSFETs, allowing the analog input voltage range to extend to the supply rails while maintaining a fairly constant ON channel resistance (R_{ON}). This process and architecture allow these devices to operate over a +5.0 V to +16.5 V single and dual supply range with the tradeoff being an increase in R_{ON} and switching time for decreasing supply ranges. Low power consumption and leakage currents are some of the intrinsic characteristics and advantages of CMOS processes. Various parasitic device capacitances in conjunction with the load resistance can adversely affect both crosstalk and off isolation, thus limiting the effective bandwidth of these devices to below 100 kHz for a 12-bit system.

Our current portfolio of CMOS multiplexers and switches are fabricated on either a low cost, enhanced LC^{2}MOS junction-isolated or a dielectrically isolated process. The LC^{2}MOS process features high breakdown voltages and very low parasitic capacitances which increase both the switching time and isolation. These junction-isolated devices are designed to restrict the incidence of SCR latch-up to conditions of excessive misuse. The dielectrically isolated process eliminates the parasitic junctions which cause SCR latch-up, thus extending the overvoltage protection at the analog ports to ±25 V above the power supplies while maintaining low R_{ON} and low leakage currents.

Analog multiplexers and switches fabricated on the bipolar-JFET process consist of high quality ion-implanted P-Channel JFET switches. The digital control logic and switch driver circuits for these switches consist of both bipolar and JFET devices. JFET switches tend to exhibit slightly lower R_{ON}, R_{ON} variation over the analog input range and parasitic device capacitance, resulting in improved bandwidth, isolation, crosstalk, and harmonic distortion specifications when compared to CMOS devices. The analog input range extends from the negative supply to approximately 4 volts ($V_{PINCH-OFF}$) below the positive supply. This radiation-hard process is not plagued by the SCR latch-up tendency, and is less susceptible to both ESD and analog over-voltage destruction, unlike traditional CMOS processes. The limitations of this process, when compared to CMOS, are an increase in power consumption, a lower analog input range, and a restricted power supply operating range.

The advanced bipolar process exhibits a minimum full-power bandwidth of 30 MHz and provides fast, wideband switching capabilities while maintaining crosstalk rejection of 75 dB at 10 MHz. As these specifications suggest, this process is best suited for video applications. Some other key specifications include gain flatness and tolerance, differential gain and phase, settling time, and input impedance. The AD9300 4 × 1 video multiplexer uses this process to achieve the high performance characteristics required for video applications which are unattainable through the other processes.

DEFINITIONS OF SPECIFICATIONS

Analog Input Leakage Current—$I_{S(OFF)}$
The algebraic sum of leakage currents into or out of an OFF-channel source input due to parasitic reverse-bias diode junctions.

Analog Output Leakage Current—I_{OUT} or $I_{D(OFF)}$
The algebraic sum of leakage currents into or out of an OFF-channel "D" output due to parasitic reverse-bias diode junctions.

Analog Output-to-Input Capacitance—$C_{DS(OFF)}$
The equivalent capacitance which shunts an open switch effectively between "S" and "D" output. This will determine a switch's isolation over frequency.

Analog Input/Output ON Capacitance—$C_{S(ON)}$, $C_{D(ON)}$
The capacitance between the analog "S" input or "D" output and ground with the channel ON.

Analog Input OFF Capacitance—$C_{S(OFF)}$
The capacitance between an analog "S" input and ground with the channel OFF.

Analog Output OFF Capacitance—$C_{D(OFF)}$
The capacitance between the analog "D" output and ground with the channel OFF. High frequency transmission and output settling time characteristics are highly influenced by this parameter in conjunction with R_{ON}.

Break-Before-Make Delay—(t_{OPEN})
The elapsed time between the turn-off of one analog input and the subsequent turn-on of another input as determined by the appropriate instantaneous change in the digital input code for both inputs measured between the outputs' 50% transition points.

Channel Capacitance—$C_{SS(OFF)}$, $C_{DD(OFF)}$
The capacitance between the "D" ("S") terminals of any two channels.

Charge Transfer—Q
Charge transfer appears as a voltage step (pedestal) on the output capacitance after switch turn-OFF due to charge coupling from the switch driver to the analog switch.

Crosstalk—CT
The proportionate amount of cross-coupling from an analog input channel to another output channel, expressed in dB. It is measured by driving the source of any channel with a specified input signal and observing the voltage which appears at the output with a specified load.

Digital Input Capacitance—C_{DIG} or C_{IN}
The capacitance between a digital input and ground.

Digital Input Current —(I_{INL} or I_{INH})
The current flowing into a digital input when a specified low level or high level voltage is applied to that input.

Digital Input Voltage—(V_{INL} and V_{INH})
The maximum threshold input voltage for Logic "0" and the minimum threshold input voltage for Logic "1."

Negative/Positive Voltage Supply—(V−, V_{SS} and V+, V_{DD})
The most negative and most positive voltage supply with respect to ground.

Off Isolation—$I_{SO(OFF)}$
The proportionate amount of a high frequency analog input signal which is coupled through the channel of an OFF device. This feedthrough is transmitted through the $C_{DS(OFF)}$ to a load comprised of $C_{D(OFF)}$ in parallel with an external load. Isolation generally decreases by 6 dB/octave with increasing frequency.

ON Resistance—R_{ON}
The series ON-channel resistance measured between "S" input and "D" output terminals under specified conditions.

ON Resistance Match—$R_{ON\ Match}$ or R_{ON} Between Switches
The channel-to-channel matching of ON resistance when channels are operated under identical conditions.

ON Resistance Variation—R_{ON} or R_{ON} vs. V_S
The variation of ON resistance produced by the specified analog input voltage change with a constant load current.

ON Channel Analog Leakage Current —$I_{D(ON)}$ + $I_{S(ON)}$ or $I_{OUT}-I_S$
Current loss (or gain) through an ON-channel resistance creating a voltage offset across the device. Specified as an absolute value since the direction of the current flow is unpredictable.

Output Enable Delay Time OFF—$t_{OFF(EN)}$
The required time for a multiplexer to disconnect the analog output from the selected analog input. It is measured from the 50% point of ENABLE input logic change to the time the output reaches 10% of the initial value.

Output Enable Delay Time ON—$t_{ON(EN)}$
The required time for a multiplexer to connect the analog output to the selected analog input. It is measured from the 50% point of ENABLE input logic change to the time the output reaches 90% of the final value.

Output OFF Switching Time—t_{OFF}
The time required to disconnect the analog output from the analog input. The time is measured from the 50% point of the logic input change to the time the output reaches 10% of the initial value.

Output ON Switching Time—t_{ON}
The time required to connect the analog output to the analog input. The time is measured from the 50% of the logic input change to the time the output reaches 10% of the final value.

Output Settling Time—t_S
The elapsed time for the analog output to reach its final value within a specified error band after the corresponding digital input code has been changed. It is measured from the 50% point of the logic input change to the time the output reaches a final value within a specified error band.

Power Supply Rejection—PSSR
The ratio of the change in switch contact voltage (V_D) to the change in voltage supply (V+ or V−) that causes it.

Switching Time— $t_{TRANSITION}$
The time required to switch and slew from one analog input channel to another analog input with a full-scale differential between inputs with a high impedance output load. The time is measured from the 50% point of the logic input change to the time the output reaches 80% of the final value.

Total Harmonic Distortion—THD
The ratio of the signal power at the fundamental frequency to the signal power of all harmonics observed at the switch output (V_D) with a pure sinusoid applied to the switch input (V_S).

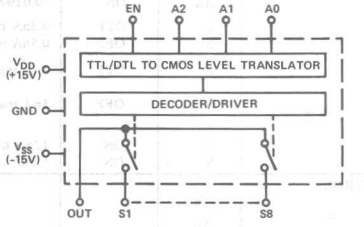
CMOS 4/8 Channel Analog Multiplexers

AD7501/AD7502/AD7503

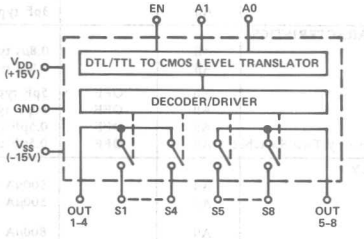
FEATURES
DTL/TTL/CMOS Direct Interface
Power Dissipation: 30μW
R_{ON}: 170Ω
Standard 16-Pin DIPs and 20-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAMS

AD7501/AD7503



AD7502



5

GENERAL DESCRIPTION

The AD7501 and AD7503 are monolithic CMOS, 8-channel analog multiplexers which switches one of 8 inputs to a common output depending on the state of three binary address lines and an "enable" input. The AD7503 is identical to the AD7501 except its "enable" logic is inverted. All digital inputs are TTL/DTL and CMOS logic compatible.

The AD7502 is a monolithic CMOS dual 4-channel analog multiplexer. Depending on the state of 2 binary address inputs and an "enable", it switches two output buses to two of 8 inputs.

TRUTH TABLES

AD7501				
A_2	A_1	A_0	E_N	"ON"
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8
X	X	X	0	None

AD7503				
A_2	A_1	A_0	E_N	"ON"
0	0	0	0	1
0	0	1	0	2
0	1	0	0	3
0	1	1	0	4
1	0	0	0	5
1	0	1	0	6
1	1	0	0	7
1	1	1	0	8
X	X	X	1	None

AD7502			
A_1	A_0	E_N	"ON"
0	0	1	1 & 5
0	1	1	2 & 6
1	0	1	3 & 7
1	1	1	4 & 8
X	X	0	None



AD7501/AD7502/AD7503 — SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V unless otherwise noted.)

PARAMETER	VERSION[1]	SWITCH CONDITION	@25°C AD7501, AD7503	@25°C AD7502	OVER SPECIFIED TEMP. RANGE AD7501, AD7503	OVER SPECIFIED TEMP. RANGE AD7502	TEST CONDITIONS
ANALOG SWITCH							
R_{ON}	All	ON	170Ω typ, 300Ω max	*			$-10V \leq V_S \leq +10V$
R_{ON} vs. V_S	All	ON	20% typ	*			I_S = 1.0mA
R_{ON} vs. Temperature	All	ON	0.5%/°C typ	*			V_S = 0V, I_S = 1.0mA
ΔR_{ON} Between Switches	All	ON	4% typ	*			
R_{ON} vs. Temperature Between Switches	All	ON	±0.01%/°C	*			
I_S	K	OFF	0.2nA typ, 2nA max	*	50nA max	*	V_S = −10V, V_{OUT} = +10V and
	S	OFF	0.5nA max	*	50nA max	*	V_S = +10V, V_{OUT} = −10V
I_{OUT}	K	OFF	1nA typ, 10nA max	0.6nA typ, 5nA max	250nA max	125nA max	V_S = −10V, V_{OUT} = +10V and
	S	OFF	5nA max	3nA max	250nA max	125nA max	V_S = +10V, V_{OUT} = −10V AD7501/02: Enable LOW AD7503: Enable HIGH
$\lvert I_{OUT} - I_S \rvert$	K	ON	12nA max	7nA max	300nA max	175nA max	V_S = 0
	S	ON	5.5nA max	3.5nA max	300nA max	175nA max	
DIGITAL CONTROL							
V_{INL}	All				0.8V max	*	
V_{INH}	All				2.4V min	*	
I_{INL} or I_{INH}	All		10nA typ	*			
C_{IN}	All		3pF typ	*			
DYNAMIC CHARACTERISTICS							
t_{ON}	All		0.8μs typ	*			V_{IN} = 0 to +5.0V
t_{OFF}	All		0.8μs typ	*			(See Test Circuit 2)
C_S	All	OFF	5pF typ	*			
C_{OUT}	All	OFF	30pF typ	15pF typ			
C_{S-OUT}	All	OFF	0.5pF typ	*			
C_{SS} Between Any Two Switches	All	OFF	0.5pF typ	*			
POWER SUPPLY							
I_{DD}	All		500μA max	*	500μA max	*	All Digital Inputs Low
I_{SS}	All		500μA max	*	500μA max	*	
I_{DD}	All		800μA max	*	800μA max	*	All Digital Inputs High
I_{SS}	All		800μA max	*	800μA max	*	

NOTES
*Same specifications as AD7501 and AD7503.
[1]KN version specified for 0 to +70°C, KQ version for −25°C to +85°C; and SQ, SE versions for −55°C to +125°C.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . +17V
V_{SS} to GND . . . . . −17V
V Between Any Switch Terminals (see Note 1) 25V
Digital Input Voltage Range . . . . . V_{DD} to GND
Overvoltage at V_{OUT} (V_S) . . . . . V_{SS}, V_{DD}
Switch Current (I_S, Continuous One Channel) 35mA
Switch Current (I_S, Surge One Channel)
1ms Duration, 10% Duty Cycle 50mA
Power Dissipation (Any Package)
Up to +75°C 450mW
Derates above +75°C by . . . . . 6mW/°C

Operating Temperature
Commercial (KN Version) . . . . . 0 to +70°C
Industrial (KQ Version) . . . . . −25°C to +85°C
Extended (SQ, SE Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C

CAUTION
1. Do not apply voltages higher than V_{DD} and V_{SS} to any other terminal, especially when V_{SS} = V_{DD} = 0V all other pins should be at 0V.
2. The digital control inputs are diode protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

CAUTION:
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

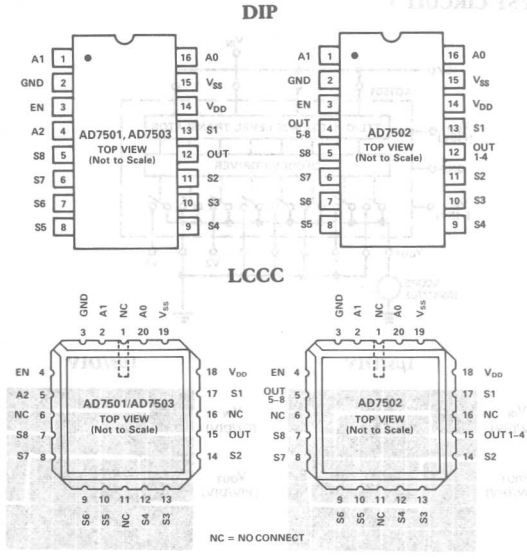


ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
AD7501KN	0°C to +70°C	N-16
AD7501KQ	−25°C to +85°C	Q-16
AD7501SQ	−55°C to +125°C	Q-16
AD7501SE	−55°C to +125°C	E-20A
AD7502KN	0°C to +70°C	N-16
AD7502KQ	−25°C to +85°C	Q-16
AD7502SQ	−55°C to +125°C	Q-16
AD7502SE	−55°C to +125°C	E-20A
AD7503KN	0°C to +70°C	N-16
AD7503KQ	−25°C to +85°C	Q-16
AD7503SQ	−55°C to +125°C	Q-16
AD7503SE	−55°C to +125°C	E-20A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. See the Analog Devices' 1990 Military Databook for military data sheet.
[2]E = Leadless Ceramic Chip Carrier; N = Narrow Plastic DIP; Q = Cerdip. For outline information see Package Information section.

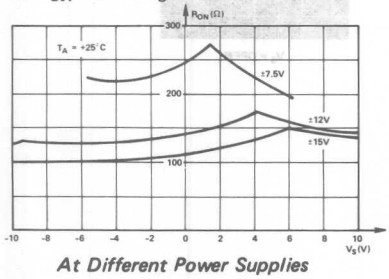
PIN CONFIGURATIONS



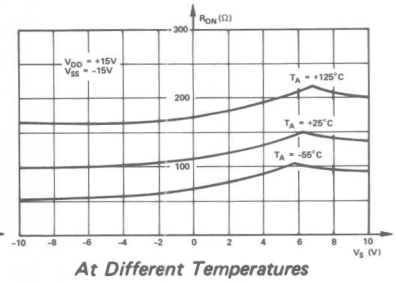
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Typical Performance Characteristics

1. R_{ON} Versus V_S

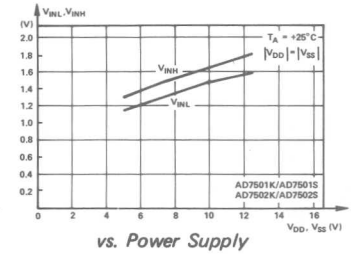


At Different Power Supplies



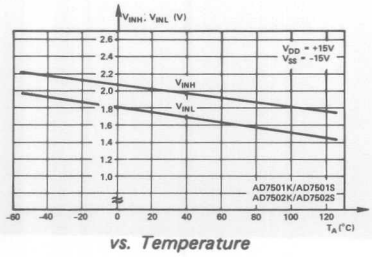
At Different Temperatures

2. Digital Threshold Voltage (V_{INH}, V_{INL})

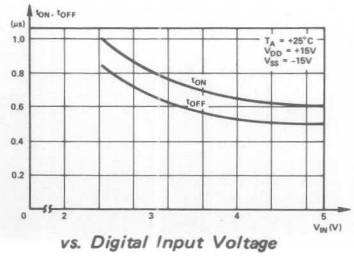


vs. Power Supply

3. t_{ON}, t_{OFF}

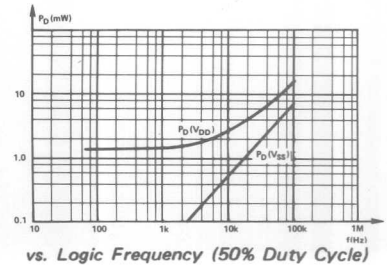


vs. Temperature



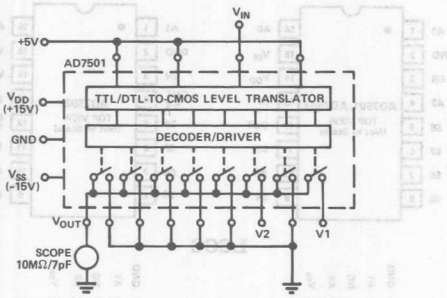
vs. Digital Input Voltage

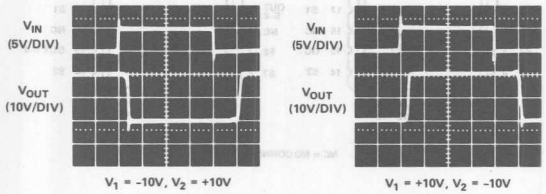
4. Power Dissipation



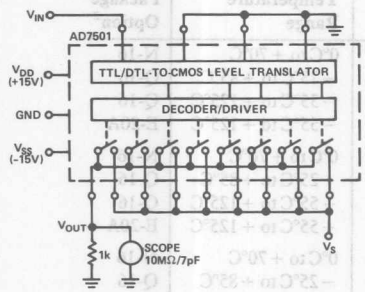
vs. Logic Frequency (50% Duty Cycle)

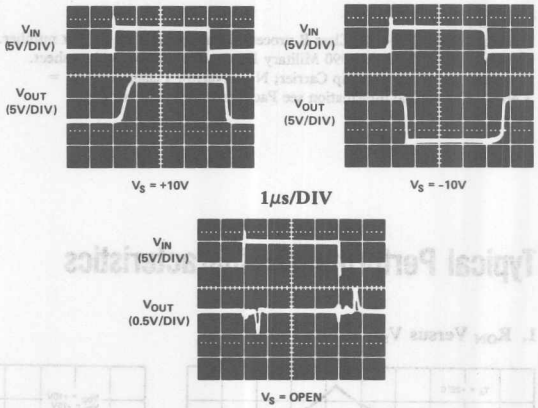
TEST CIRCUIT 1





TEST CIRCUIT 2



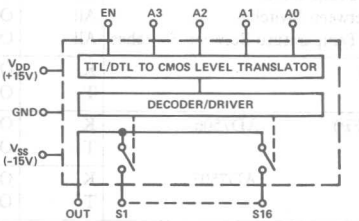


8- and 16-Channel Analog Multiplexers

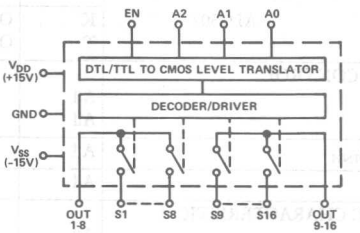
AD7506/AD7507

FEATURES
R_{ON}: 300Ω
Power Dissipation: 1.5mW
TTL/DTL/CMOS Direct Interface
Break-Before-Make Switching
Standard 28-Pin DIPs and 28-Terminal Surface Mount Packages

FUNCTIONAL DIAGRAMS



AD7506



AD7507

GENERAL DESCRIPTION

The AD7506 is a monolithic CMOS 16-channel analog multiplexer packaged in a 28-pin DIP or a 28-terminal surface mount package. It switches a common output to one of 16 inputs, depending on the state of four address lines and an "enable." The AD7507 is identical to the AD7506 except it has two outputs switched to two of 16 inputs depending on three binary address states and an "enable."

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} – GND	+17V
V_{SS} – GND	–17V
V Between Any Switch Terminals (see Note 1)	25V
Digital Input Voltage Range	V_{DD} to GND
Overvoltage at V_{OUT} (V_S)	V_{SS}, V_{DD}
Switch Current (I_S, Continuous One Channel)	20mA
Switch Current (I_S, Surge One Channel)	
1ms Duration, 10% Duty Cycle	35mA
Power Dissipation (Any Package)	
Up to +50°C	1000mW
Derates above +50°C by	10mW/°C
Operating Temperature	
Commercial (KN Versions)	0 to +70°C
Industrial (KQ Versions)	–25°C to +85°C
Extended (TQ, TE Versions)	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

CAUTION:

[1]Do not apply voltage higher than V_{DD} and V_{SS} to any other terminal, especially when $V_{SS} = V_{DD} = 0V$ all other pins should be at 0V.

[2]The digital control inputs are diode protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
AD7506KN	0°C to +70°C	N-28
AD7506KQ	–25°C to +85°C	Q-28
AD7506TQ	–55°C to +125°C	Q-28
AD7506TE	–55°C to +125°C	E-28A
AD7507KN	0°C to +70°C	N-28
AD7507KQ	–25°C to +85°C	Q-28
AD7507TQ	–55°C to +125°C	Q-28
AD7507TE	–55°C to +125°C	E-28A

NOTES

[1]To order MIL-STD-883, Class B, processed parts, add/883B to part number. See Analog Devices Military Products Databook (1990) for military data sheet.

[2]N = Plastic DIP; Q = Cerdip; E = Leadless Ceramic Chip Carrier (LCCC). For outline information see Package Information section.

AD7506/AD7507—SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V unless otherwise noted.)

Parameter	Version[1]	Switch Condition	@ +25°C	Over Specified Temperature Range	Test Conditions
ANALOG SWITCH					
R_{ON}	K	ON	300Ω typ, 450Ω max	550Ω max	V_S=−10V to +10V, I_S=1mA
	T	ON	400Ω max	500Ω max	
R_{ON} vs. V_S	All	ON	15% typ		V_S=0V, I_S=1mA
R_{ON} vs. Temperature	All	ON	0.5%/°C typ		
ΔR_{ON} Between Switches	All	ON	4% typ		
R_{ON} vs. Temperature Between Switches	All	ON	0.05%/°C typ		
I_S (OFF)	K	OFF	0.05nA typ, 5nA max	50nA max	V_S=−10V, V_{OUT}=+10V
	T	OFF	0.05nA typ, 1nA max	50nA max	and
I_{OUT} (OFF) AD7506	K	OFF	0.3nA typ, 20nA max	500nA max	V_S=+10V, V_{OUT}=−10V
	T	OFF	0.3nA typ, 10nA max	500nA max	"Enable" Low
AD7507	K	OFF	0.3nA typ, 10nA max	250nA max	
	T	OFF	0.3nA typ, 5nA max	250nA max	
I_{OUT}–I_S AD7506 (Any Switch ON)	K	ON	0.3nA typ, 20nA max	500nA max	V_S=0V
	T	ON	0.3nA typ, 10nA max	500nA max	
AD7507	K	ON	0.3nA typ, 10nA max	250nA max	
	T	ON	0.3nA typ, 5nA max	250nA max	
DIGITAL CONTROL					
V_{INL}	All			0.8V max	
V_{INH}	All			2.4V min	
I_{INL} or I_{INH}	All		10μA max	30μA max	
C_{IN}	All		3pF typ		
DYNAMIC CHARACTERISTICS[2]					
$t_{TRANSITION}$	All		700ns typ, 1000ns max		V_{IN}: 0 to 3.0V
t_{OPEN}	All		100ns typ		
t_{ON} (En)	All		1.5μs max		V_{EN}: 0 to 3.0V
t_{OFF} (En)	All		1μs max		
"OFF" Isolation	All		70dB typ		V_{EN}=0, R_L=200Ω, C_L=3.0pF, V_S=3.0V rms, f=50kHz
C_S	All	OFF	5pF typ		
C_{OUT} AD7506	All	OFF	40pF typ		
AD7507	All	OFF	20pF typ		
C_{S-OUT}	All	OFF	0.5pF typ		
C_{SS} Between Any Two Switches	All	OFF	0.5pF typ		
POWER SUPPLY					
I_{DD}	K	OFF	0.05mA typ, 1mA max		All Digital Inputs Low
	T	OFF	0.05mA typ, 1mA max	2mA max	
I_{SS}	K	OFF	0.05mA typ, 1mA max		
	T	OFF	0.05mA typ, 1mA max	2mA max	
I_{DD}	K	ON	0.3mA typ, 1mA max		All Digital Inputs High
	T	ON	0.3mA typ, 1mA max	2mA max	
I_{SS}	K	ON	0.05mA typ, 1mA max		
	T	ON	0.05mA typ, 1mA max	2mA max	

NOTES
[1]KN Version specified for 0 to +70°C; KQ Version for −25°C to +85°C; and TQ, TE Versions for −55°C to +125°C.
[2]Sample tested to ensure compliance.
Specifications subject to change without notice.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



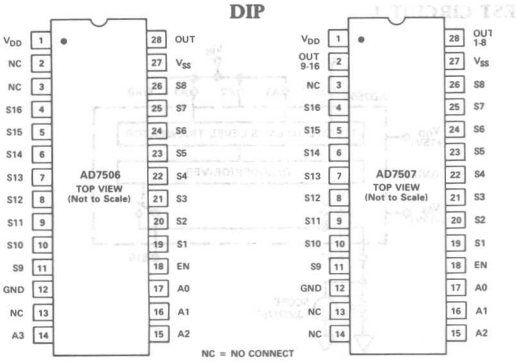
TRUTH TABLES

AD7506					
A_3	A_2	A_1	A_0	E_N	"ON"
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16
X	X	X	X	0	None

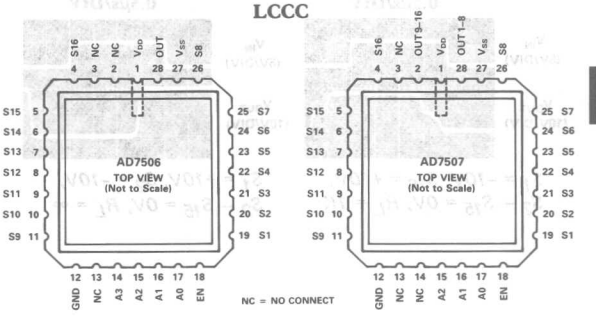
AD7507				
A_2	A_1	A_0	E_N	"ON"
0	0	0	1	1 & 9
0	0	1	1	2 & 10
0	1	0	1	3 & 11
0	1	1	1	4 & 12
1	0	0	1	5 & 13
1	0	1	1	6 & 14
1	1	0	1	7 & 15
1	1	1	1	8 & 16
X	X	X	0	None

PIN CONFIGURATIONS

DIP



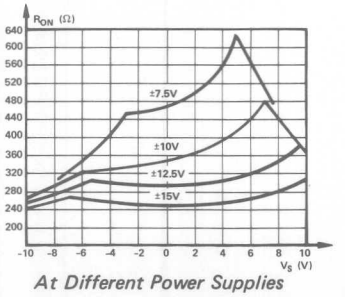
LCCC



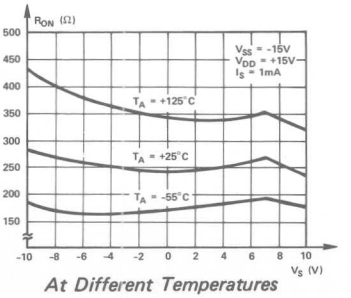
5

Typical Performance Characteristics

1. R_{ON} vs. V_S

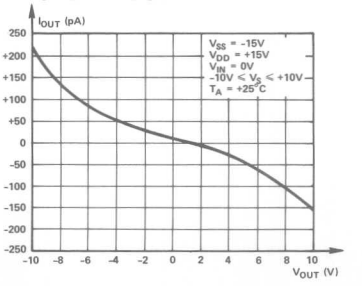


At Different Power Supplies

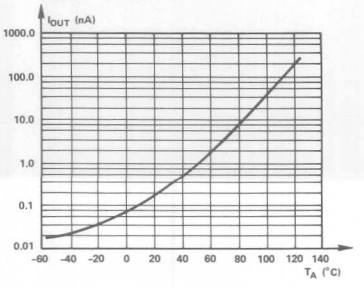


At Different Temperatures

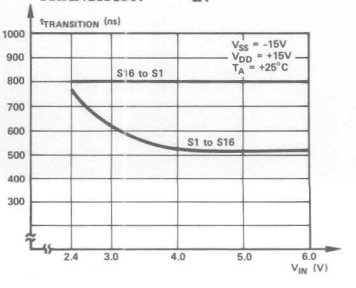
2. I_{OUT} vs. V_{OUT}



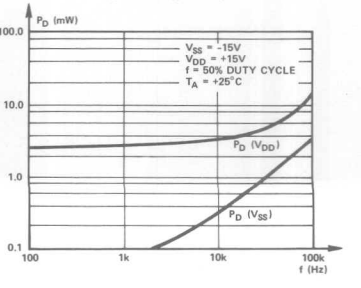
3. I_{OUT} vs. T_A



4. $t_{TRANSITION}$ vs. V_{IN}

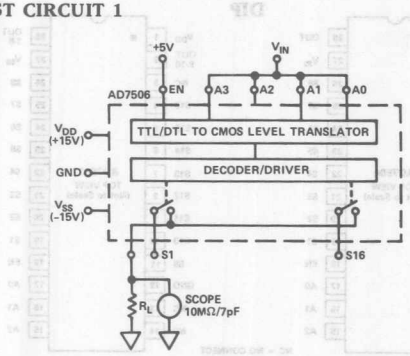


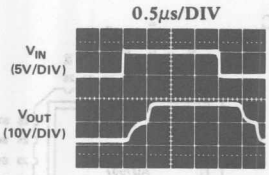
5. P_D vs. Logic Frequency



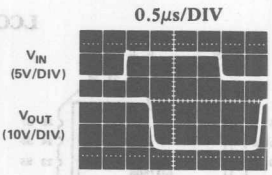
TYPICAL SWITCHING CHARACTERISTICS

TEST CIRCUIT 1



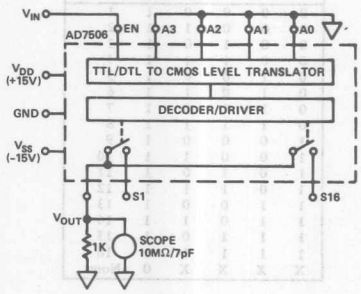


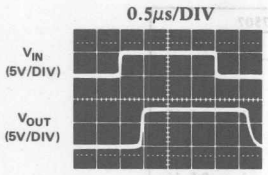
S_1 = -10V, S_{16} = +10V, S_2 – S_{15} = 0V, R_L = 1K



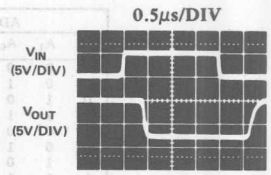
S_1 = +10V, S_2 = -10V, S_2 – S_{15} = 0V, R_L = ∞

TEST CIRCUIT 2

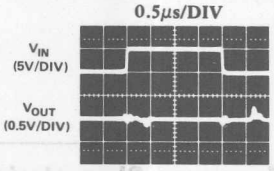




S_1 through S_{16} = +10V



S_1 through S_{16} = -10V

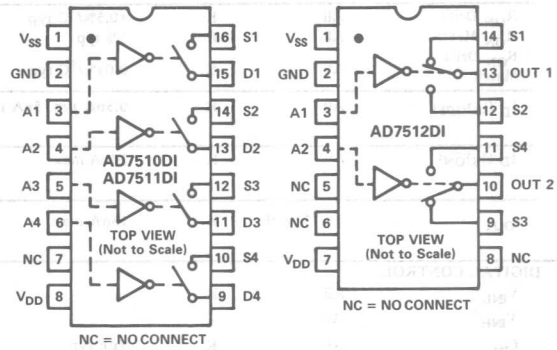


S_1 through S_{16} = 0V

AD7510DI/AD7511DI/AD7512DI

FEATURES
Latch-Proof
Overvoltage-Proof: ±25V
Low R_{ON}: 75Ω
Low Dissipation: 3mW
TTL/CMOS Direct Interface
Silicon-Nitride Passivated
Monolithic Dielectrically-Isolated CMOS
Standard 14-/16-Pin DIPs and
20-Terminal Surface Mount Packages

DIP FUNCTIONAL DIAGRAMS



5

GENERAL DESCRIPTION

The AD7510DI, AD7511DI and AD7512DI are a family of latch proof dielectrically isolated CMOS switches featuring overvoltage protection up to ±25V above the power supplies. These benefits are obtained without sacrificing the low "ON" resistance (75Ω) or low leakage current (500pA), the main features of an analog switch.

The AD7510DI and AD7511DI consist of four independent SPST analog switches packaged in either a 16-pin DIP or a 20-terminal surface mount package. They differ only in that the digital control logic is inverted. The AD7512DI has two independent SPDT switches packaged either in a 14-pin DIP or a 20-terminal surface mount package.

Very low power dissipation, overvoltage protection and TTL/CMOS direct interfacing are achieved by combining a unique circuit design and a dielectrically isolated CMOS process. Silicon nitride passivation ensures long term stability while monolithic construction provides reliability.

CONTROL LOGIC

AD7510DI: Switch "ON" for Address "HIGH"

AD7511DI: Switch "ON" for Address "LOW"

AD7512DI: Address "HIGH" makes S1 to Out 1 and S3 to Out 2

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
AD7510DIKN	0 to +70°C	N-16
AD7510DIKP	0 to +70°C	P-20A
AD7510DIKQ	−25°C to +85°C	Q-16
AD7510DISQ	−55°C to +125°C	Q-16
AD7510DISE	−55°C to +125°C	E-20A
AD7511DIKN	0 to +70°C	N-16
AD7511DIKP	0 to +70°C	P-20A
AD7511DIKQ	−25°C to +85°C	Q-16
AD7511DISQ	−55°C to +125°C	Q-16
AD7511DITE	−55°C to +125°C	E-20A
AD7512DIKN	0 to +70°C	N-14
AD7512DIKP	0 to +70°C	P-20A
AD7512DIKQ	−25°C to +85°C	Q-14
AD7512DITQ	−55°C to +125°C	Q-14
AD7512DITE	−55°C to +125°C	E-20A

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add/883B to part number. See Analog Devices Military Products Databook (1990) for military data sheet.
[2]E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information section.

AD7510DI/AD7511DI/AD7512DI—SPECIFICATIONS

(V_{DD} = +15V, V_{SS} = −15V, unless otherwise noted.)

INDUSTRIAL VERSION (K)

PARAMETER	MODEL	VERSION	+25°C (N, P, Q)	0 to +70°C (N, P) −25°C to +85°C (Q)	TEST CONDITIONS
ANALOG SWITCH					
R_{ON}[1]	All	K	75Ω typ, 100Ω max	175Ω max	−10V ≤ V_D ≤ +10V
R_{ON} vs V_D (V_S)	All	K	20% typ		I_{DS} = 1.0mA
R_{ON} Drift	All	K	+0.5%/°C typ		
R_{ON} Match	All	K	1% typ		V_D = 0, I_{DS} = 1.0mA
R_{ON} Drift Match	All	K	0.01%/°C typ		
I_D (I_S)$_{OFF}$[1]	All	K	0.5nA typ, 5nA max	500nA max	V_D = −10V, V_S = +10V and V_D = +10V, V_S = −10V
I_D (I_S)$_{ON}$[1]	All	K	10nA max		V_S = V_D = +10V
					V_S = V_D = −10V
I_{OUT}[1]	AD7512DI	K	15nA max	1500nA max	V_{S1} = V_{OUT} = ±10V, V_{S2} = ∓10V and V_{S2} = V_{OUT} = ±10V, V_{S1} = ∓10V
DIGITAL CONTROL					
V_{INL}[1]	All	K		0.8V max	
V_{INH}[1]	All			2.4V min	
C_{IN}	All	K	7pF typ		
I_{INH}[1]	All	K	10nA max		V_{IN} = V_{DD}
I_{INL}[1]	All	K	10nA max		V_{IN} = 0
DYNAMIC CHARACTERISTICS					
t_{ON}	AD7510DI	K	180ns typ		
	AD7511DI	K	350ns typ		
t_{OFF}	AD7510DI	K	350ns typ		V_{IN} = 0 to +3.0V
	AD7511DI	K	180ns typ		
$t_{TRANSITION}$	AD7512DI	K	300ns typ		
C_S (C_D)$_{OFF}$	All	K	8pF typ		
C_S (C_D)$_{ON}$	All	K	17pF typ		
C_{DS} (C_{S-OUT})	All	K	1pF typ		V_D (V_S) = 0V
C_{DD} (C_{SS})	All	K	0.5pF typ		
C_{OUT}	AD7512DI	K	17pF typ		
Q_{INJ}	All	K	30pC typ		Measured at S or D terminal. C_L = 1000pF, V_{IN} = 0 to 3V, V_D (V_S) = +10V to −10V
POWER SUPPLY					
I_{DD}[1]	All	K	800μA max	800μA max	All digital inputs = V_{INH}
I_{SS}[1]	All	K	800μA max	800μA max	
I_{DD}[1]	All	K	500μA max	500μA max	All digital inputs = V_{INL}
I_{SS}[1]	All	K	500μA max	500μA max	

NOTES

[1] 100% tested.

Specifications subject to change without notice.

EXTENDED VERSIONS (S, T)

PARAMETER	MODEL	VERSION	+25°C	-55°C to +125°C	TEST CONDITIONS
ANALOG SWITCH					
R_{ON}[1]	All	S, T	100Ω max	175Ω max	$-10V \leq V_D \leq +10V$ I_{DS} = 1mA
I_D $(I_S)_{OFF}$[1]	All	S, T	3nA max	200nA max	V_D = -10V, V_S = +10V and V_D = +10V, V_S = -10V
I_D $(I_S)ON$[1]	All	S, T	10		$V_S = V_D$ = +10V and $V_S = V_D$ = -10V
I_{OUT}[1]	AD7512DI	S, T	9nA max	600nA max	$V_{S1} = V_{OUT} = \pm 10V$ $V_{S2} = \mp 10V$ and $V_{S2} = V_{OUT} = \pm 10V$ $V_{S1} = \mp 10V$
DIGITAL CONTROL					
V_{INL}[1]	All	S, T		0.8V max	
V_{INH}[1,2]	AD7510DI	S		2.4V min	
	AD7511DI	T		2.4V min	
	AD7512DI	T		2.4V min	
	AD7511DI	S		3.0V min	
	AD7512DI	S		3.0V min	
I_{INH}[1]	All	S, T	10nA max		$V_{IN} = V_{DD}$
I_{INL}[1]	All	S, T	10nA max		V_{IN} = 0
DYNAMIC CHARACTERISTICS					
t_{ON}[3]	AD7510DI	S,	1.0μs max		V_{IN} = 0 to +3V
	AD7511DI	S, T	1.0μs max		
t_{OFF}[3]	AD7510DI	S, T	1.0μs max		
	AD7511DI	S, T	1.0μs max		
$t_{TRANSITION}$[3]	AD7512DI	S, T	1.0μs max		
POWER SUPPLY					
I_{DD}[1]	All	S, T		800μA max	All digital inputs = V_{INH}
I_{SS}[1]	All	S, T		800μA max	
I_{DD}[1]	All	S, T		500μA max	All digital inputs = V_{INL}
I_{SS}[1]	All	S, T		500μA max	

NOTES
[1] 100% tested.
[2] A pullup resistor, typically 1-2kΩ is required to make AD7511DISQ and AD7512DISQ TTL compatible.
[3] Guaranteed, not production tested.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND . . . . . +17V
V_{SS} to GND . . . . . -17V
Overvoltage at V_D (V_S)
(1 second surge) . . . . . V_{DD} +25V
or V_{SS} -25V
(Continuous) . . . . . V_{DD} +20V
or V_{SS} -20V
or 20mA, Whichever Occurs First
Switch Current (I_{DS}, Continuous) 50mA
Switch Current (I_{DS}, Surge)
1ms Duration, 10% Duty Cycle 150mA
Digital Input Voltage Range . . . . . 0V to V_{DD} +0.3V
Power Dissipation (Any Package)
Up to +75°C 450mW
Derates above +75°C by . . . . . 6mW/°C

Lead Temperature (Soldering, 10sec) . . . . . +300°C
Storage Temperature . . . . . -65°C to +150°C
Operating Temperature
Commercial (KN, KP Versions) . . . . . 0 to +70°C
Industrial (KQ Versions) . . . . . -25°C to +85°C
Extended (SQ, TQ, SE, TE Versions) . . -55°C to +125°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



5

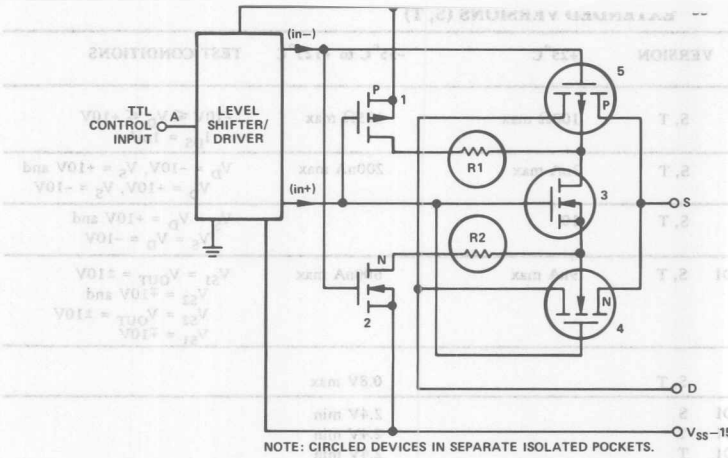


Figure 1. Typical Output Switch Circuitry of AD7510DI Series

CIRCUIT DESCRIPTION

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenon necessitated protection circuitry. These protection circuits, however, either caused degradation of important switch parameters such as R_{ON} or leakage, or provided only limited protection in the event of overvoltage.

The AD7510DI series switches utilize a dielectrically isolated CMOS fabrication process to eliminate the four-layer substrate found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 2. The output switching element is comprised of device numbers 4 and 5. Operation is as follows: for an "ON" switch, (in+) is V_{DD} and (in−) is V_{SS} from the driver circuits. Device numbers 1 and 2 are "OFF" and number 3 in "ON". Hence, the backgates of the P- and N-channel output devices (numbers 4 and 5) are tied together and floating. The circled devices are located in separate dielectrically isolated pockets. Floating the output switch backgates with the signal input increases the effective threshold voltage for an applied analog signal, thus providing a flatter R_{ON} versus V_S response.

For an "OFF" switch, device number 3 is "OFF," and the backgates of devices 4 and 5 are tied through 1kΩ resistors (R1 and R2) to the respective supply voltages through the "ON" devices 1 and 2.

If a voltage is applied to the S or D (OUT) terminal which exceeds V_{DD} or V_{SS}, the S- or D-to-backgate diode is forward biased; however, R1 and R2 provide current limiting action to the supplies.

An equivalent circuit of the output switch element in Figure 3 shows that, indeed, the 1kΩ limiting resistors are in series with the backgates of the P- and N-channel output devices – *not* in series with the signal path between the S and D terminals.

It is possible to turn on an "OFF" switch by applying a voltage in excess of V_{DD} or V_{SS} to the S or D terminal. If a positive stress voltage is applied to the S or D terminal which exceeds V_{DD} by a threshold, then the P-channel (device 5) will turn on creating a low impedance path between the S and D terminals. A similar situation exists for negative stress voltages which exceed V_{SS}. In this case the N-channel provides the low impedance path between the S and D terminals. The limiting factor on the overvoltage protection is the power dissipation of the package and is ±20V continuous (or 20mA whichever occurs first) above the supply voltages.

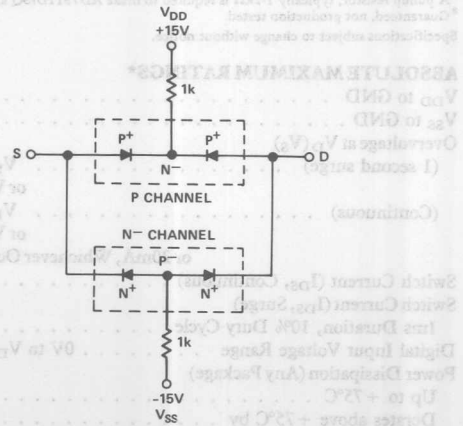
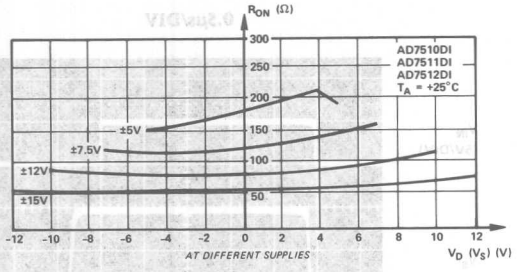
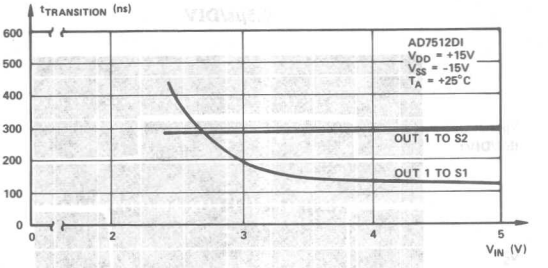


Figure 2. AD7510DI Series Output Switch Diode Equivalent Circuit

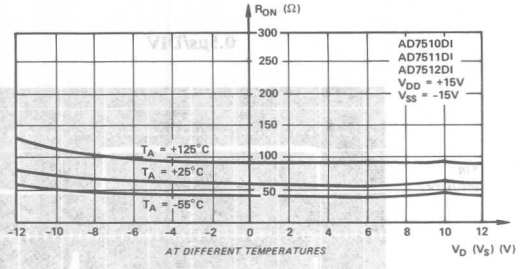
Typical Performance Characteristics—AD7510DI/AD7511DI/AD7512DI



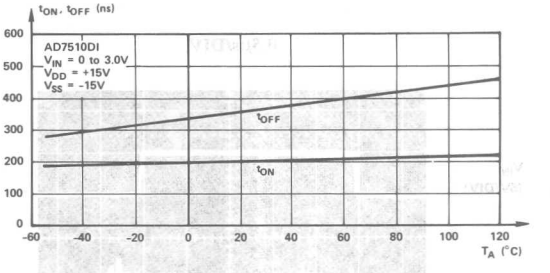
R_{ON} as a Function of V_D (V_S)



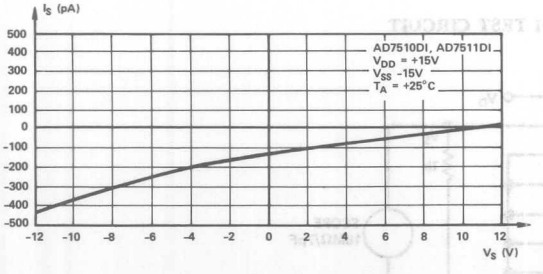
$t_{TRANSITION}$ as a Function of Digital Input Voltage



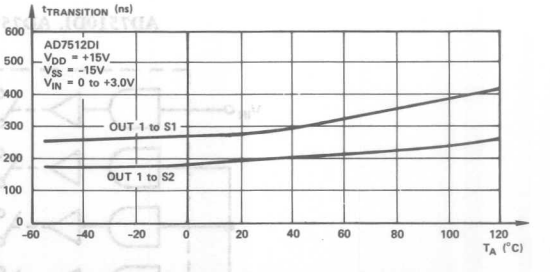
R_{ON} as a Function of V_D (V_S)



t_{ON}, t_{OFF} as a Function of Temperature

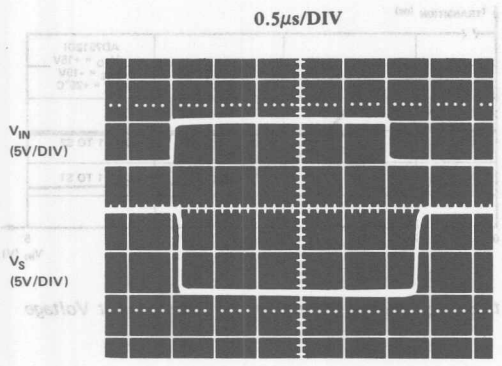


I_S, $(I_D)_{OFF}$ vs V_S

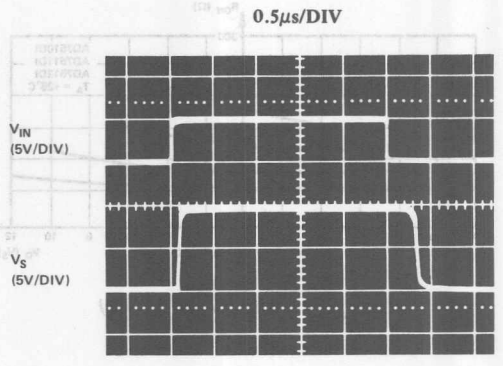


$t_{TRANSITION}$ as a Function of Temperature

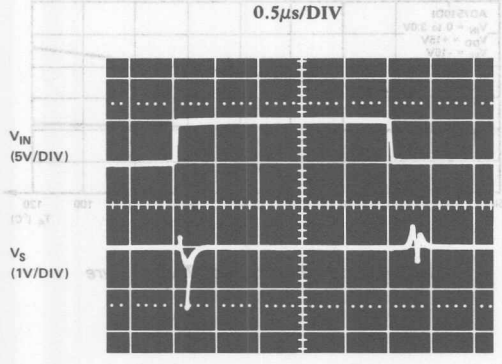
TYPICAL SWITCHING CHARACTERISTICS — AD7510DI, AD7511DI



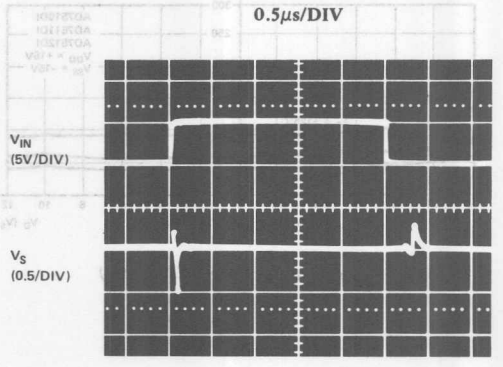
Switching Waveforms for V_D = -10V



Switching Waveforms for V_D = +10V

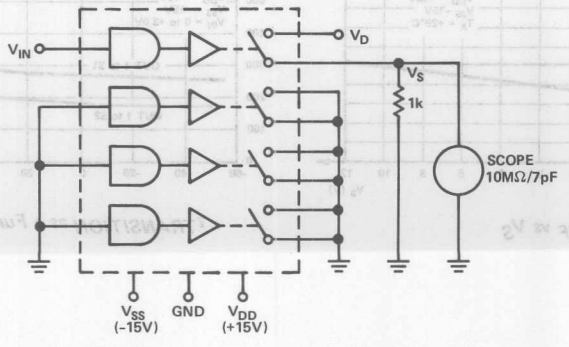


Switching Waveforms for V_D = Open



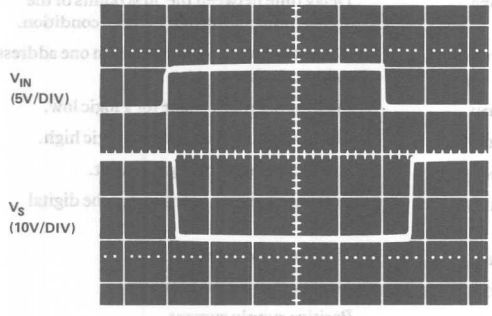
Switching Waveforms for V_D = 0V

AD7510DI, AD7511DI TEST CIRCUIT



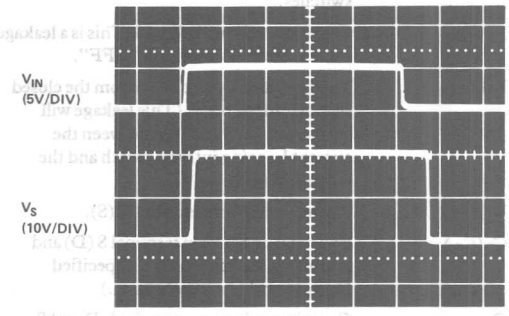
AD7512DI

0.5μs/DIV



Switching Waveforms for
V_{S1} = -10V, V_{S2} = +10V, R_L = 1k

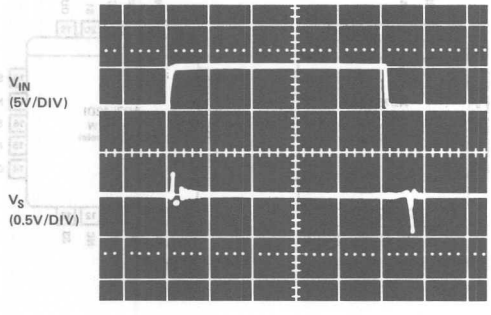
0.5μs/DIV



Switching Waveforms for
V_{S1} = +10V, V_{S2} = -10V, R_L = ∞

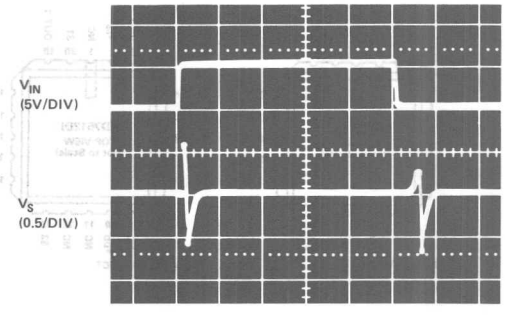
5

0.5μs/DIV



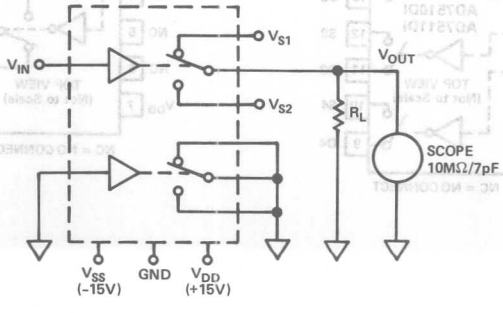
Switching Waveforms for
V_{S1} and V_{S2} = 0V, R_L = ∞

0.5μs/DIV



Switching Waveforms for
V_{S1} and V_{S2} = Open, R_L = 1k

AD7512DI TEST CIRCUIT

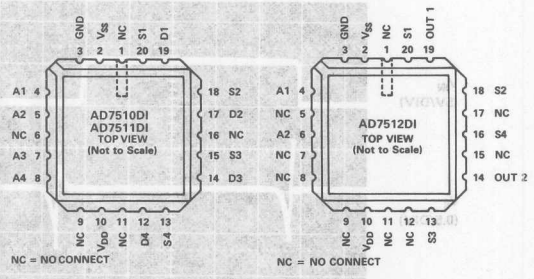


TERMINOLOGY

R_{ON}	Ohmic resistance between terminals D and S.
R_{ON} Drift Match	Difference between the R_{ON} drift of any two switches.
R_{ON} Match	Difference between the R_{ON} of any two switches.
$I_D (I_S)_{OFF}$	Current at terminals D or S. This is a leakage current when the switch is "OFF".
$I_D (I_S)_{ON}$	Leakage current that flows from the closed switch into the body. (This leakage will show up as the difference between the current I_D going into the switch and the outgoing current I_S.)
$V_D (V_S)$	Analog voltage on terminal D (S).
$C_S (C_D)$	Capacitance between terminal S (D) and ground. (This capacitance is specified for the switch open and closed.)
C_{DS}	Capacitance between terminals D and S. (This will determine the switch isolation over frequency.)
$C_{DD} (C_{SS})$	Capacitance between terminals D (S) of any two switches. (This will determine the cross coupling between switches vs. frequency.)
t_{ON}	Delay time between the 50% points of the digital input and switch "ON" condition.
t_{OFF}	Delay time between the 50% points of the digital input and switch "OFF" condition.
$t_{TRANSITION}$	Delay time when switching from one address state to another.
V_{INL}	Maximum input voltage for a logic low.
V_{INH}	Minimum input voltage for a logic high.
$I_{INL} (I_{INH})$	Input current of the digital input.
C_{IN}	Input capacitance to ground of the digital input.
V_{DD}	Most positive voltage supply.
V_{SS}	Most negative voltage supply.
I_{DD}	Positive supply current.
I_{SS}	Negative supply current.

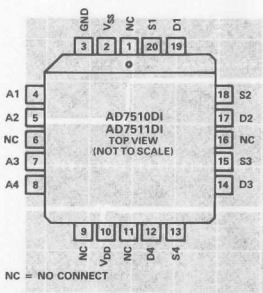
PIN CONFIGURATIONS

LCCC

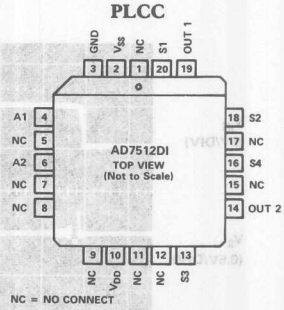


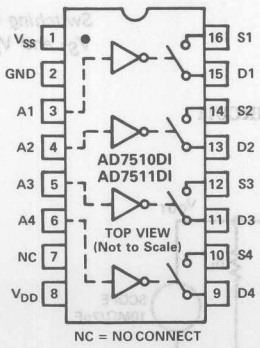
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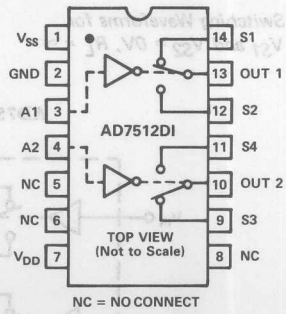
PLCC



PLCC







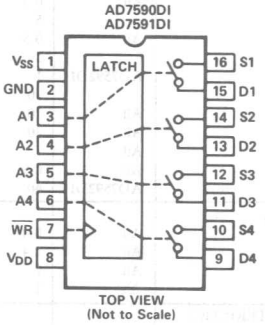
DI CMOS
Analog Switches with Data Latches

AD7590DI/AD7591DI/AD7592DI

FEATURES
SCR Latch-Proof
Overvoltage-Proof: ±25V
Low R_{ON}: 60Ωtyp
Buffered Switch Logic
TTL, CMOS Compatible
Monolithic Dielectrically-Isolated CMOS
Pin Compatible with AD7510DI Series

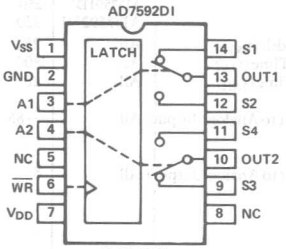
FUNCTIONAL BLOCK DIAGRAMS

16-Pin DIP



TOP VIEW
(Not to Scale)

14-Pin DIP



TOP VIEW
(Not to Scale)

NC = NO CONNECT

GENERAL DESCRIPTION

The AD7590DI, AD7591DI and AD7592DI are a family of protected (latch-proof) dielectrically isolated CMOS switches featuring overvoltage protection up to ±25V above the power supplies. Microprocessor interfacing is facilitated by the provision of on-chip data latches.

The AD7590DI and AD7591DI consist of four independent SPST analog switches packaged in a 16-pin DIP. They differ only in that the switch control logic is inverted. The AD7592DI has two independent SPDT switches packaged in a 14-pin DIP.

CONTROL LOGIC ($\overline{WR}$ HELD LOW)

AD7590DI: Switch "ON" for Address "HIGH"

AD7591DI: Switch "ON" for Address "LOW"

AD7592DI: Address "HIGH" makes S1 to Out 1 and S3 to Out 2

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Parameter						
ANALOG SWITCH						
Analog Signal Range	All	±10	±10	±10	Volts	
R_{ON}[1]	All	60			Ω typ	$-10V \leq V_S \leq +10V$, $I_{DS} = 1mA$;
	All	90	120	150	Ω max	Test Circuit 1
R_{ON} Match[2]	All	2			Ω typ	$V_S = 0$, $I_{DS} = 1mA$
R_{ON} Match Drift[2]	All	0.01			Ω/°C typ	$V_S = 0$, $I_{DS} = 1mA$
I_D OFF[1]	AD7590DI	0.5			nA typ	Test Circuit 2
	AD7591DI	5	50	200	nA max	
I_S OFF[1]	All	0.5			nA typ	Test Circuits 2 & 4
		5	50	200	nA max	
I_D (I_S) ON[1]	All	0.5			nA typ	Test Circuit 3
		5	50	200	nA max	
I_{OUT}[1]	AD7592DI	1			nA typ	Test Circuit 4
		10	100	400	nA max	
C_S (C_D) OFF[3]	All	10			pF typ	
C_S (C_D) ON[3]	All	30			pF typ	
C_{DS} (C_{S-OUT})	All	1			pF typ	
C_{DD} (C_{SS})[3]	All	0.5			pF typ	
C_{OUT}[3]	AD7592DI	40			pF typ	
DIGITAL CONTROL						
V_{INL}[1]	All	0.8	0.8	0.8	V max	
V_{INH}[1]	All	2.4	2.4	2.4	V min	
C_{IN}[3]	All	7	7	7	pF typ	
I_{INL} or I_{INH}[1,4]	All	1	1	1	μA max	$V_{IN} = 0$ or V_{DD}
DYNAMIC CHARACTERISTICS						
t_{ON}[2]	AD7590DI	250	380	380	ns max	Test Circuit 5
	AD7591DI	400	500	500	ns max	
t_{OFF}[2]	AD7590DI	400	500	500	ns max	Test Circuit 5
	AD7591DI	250	380	380	ns max	
$t_{TRANSITION}$[2]	AD7592DI	350	450	450	ns max	Test Circuit 6
Write Pulse-Width (t_{WR})[2]	All	250	300	400	ns min	See Figure 1
Address Setup Time (t_{AS})[2]	All	300	300	400	ns min	See Figure 1
Address Hold Time (t_{AH})[2]	All	20	30	40	ns min	See Figure 1
Off Isolation[3] (Analog Input to Analog Output)	All	−85			dB typ	A, $\overline{WR} = 0.8V$; $V_S = 10V$ (Pk-Pk); $f = 1kHz$, $R_L = 10k\Omega$
Crosstalk[3] (Digital Input to Analog Output)	All	5			mV peak, typ	$R_L = 1M\Omega$, $C_L = 15pF$; $V_{INH} = 3V$, $V_{INL} = 0V$; $t_{RISE} = t_{FALL} = 20ns$; $\overline{WR}$ held HIGH
Q_{INJ}[3] (Charge Injection)	All	55			pC typ	Test Circuit 7
POWER SUPPLY						
I_{DD}[1]	All	1	1.5	2	mA max	Digital Inputs = V_{INL} or V_{INH}
I_{SS}[1]	All	1	1	1	mA max	

NOTES
[1]100% tested.
[2]Guaranteed, not production tested.
[3]Typical values for information only, not subject to test.
[4]Inputs are MOS gates typical current less than 10nA.
Specifications subject to change without notice.

TIMING AND CONTROL SEQUENCE

Figure 1 shows the timing sequence for latching the switch address inputs. The latches are level sensitive and, therefore, while $\overline{WR}$ is held low the latches are transparent and the switches respond to the address inputs. The digital inputs are latched on the rising edge of $\overline{WR}$.

NOTE: All digital input signals rise and fall times measured from 10% to 90% of 3V. $t_R = t_F = 20ns$.

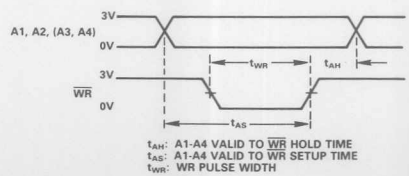


Figure 1. Timing and Control Sequence

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . +17V
V_{SS} to GND . . . . . −17V
Overvoltage at V_D (V_S), One Switch Only
(1sec surge) . . . . . V_{DD} +25V
or V_{SS} −25V
(Continuous) . . . . . V_{DD} +20V
or V_{SS} −20V
or 20mA, Whichever Occurs First
Switch Current (I_{DS}, Continuous) 50mA
Switch Current (I_{DS}, Surge)
1ms Duration, 10% Duty Cycle 150mA
Digital Input Voltage Range . . . . . −0.3V to V_{DD} +0.3V
Power Dissipation (Any Package)
Up to +75°C 450mW
Derates above +75°C by . . . . . 6mW/°C
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature
Plastic (KN Versions) . . . . . 0 to +70°C
Cerdip (BQ Versions) . . . . . −25°C to +85°C
Cerdip (TQ Versions) . . . . . −55°C to +125°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
AD7590DIKN	0°C to +70°C	N-16
AD7590DIKP	0°C to +70°C	P-20A
AD7590DIBQ	−25°C to +85°C	Q-16
AD7590DITQ	−55°C to +125°C	Q-16
AD7591DIKN	0°C to +70°C	N-16
AD7591DIKP	0°C to +70°C	P-20A
AD7591DIBQ	−25°C to +85°C	Q-16
AD7591DITQ	−55°C to +125°C	Q-16
AD7592DIKN	0°C to +70°C	N-14
AD7592DIKP	0°C to +70°C	P-20A
AD7592DIBQ	−25°C to +85°C	Q-14
AD7592DITQ	−55°C to +125°C	Q-14

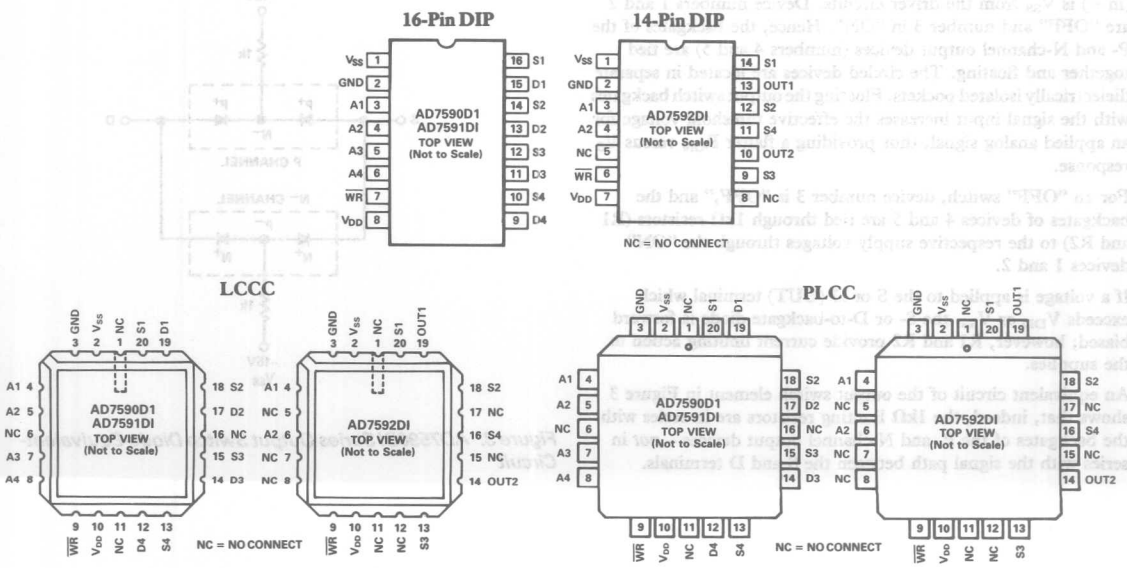
NOTES
[1]To order MIL-STD-883C, Class B processed parts, add /883B to part number. Refer to the Analog Devices Military Products Databook (1990) for military data sheet.
[2]N = Narrow Plastic DIP; P = Plastic Leaded Chip Carrier Q = Cerdip. For Hermetic Surface Mount package, contact your local sales office. For outline information see Package Information section.

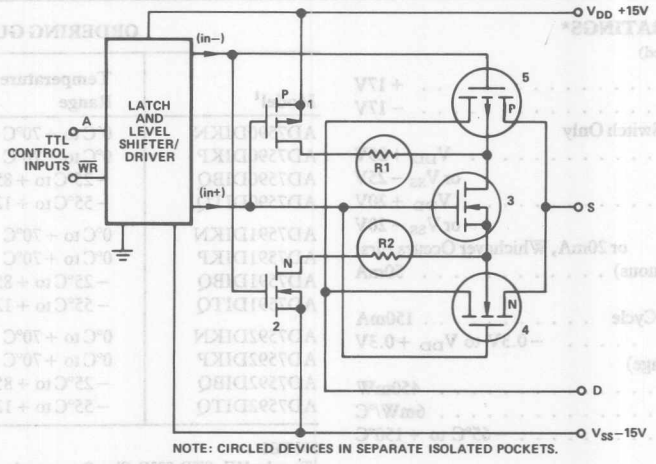
5

CAUTION:
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



PIN CONFIGURATIONS





NOTE: CIRCLED DEVICES IN SEPARATE ISOLATED POCKETS.

Figure 2. Typical Output Switch Circuitry of AD7590DI Series

CIRCUIT DESCRIPTION

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenon necessitated protection circuitry. These protection circuits, however, either caused degradation of important switch parameters such as R_{ON} or leakage, or provided only limited protection in the event of overvoltage.

The AD7590DI series switches utilize a dielectrically-isolated CMOS fabrication process to eliminate the four-layer substrate found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 2. The output switching element is comprised of device numbers 4 and 5. Operation is as follows: for an "ON" switch, (in+) is V_{DD} and (in−) is V_{SS} from the driver circuits. Device numbers 1 and 2 are "OFF" and number 3 in "ON". Hence, the backgates of the P- and N-channel output devices (numbers 4 and 5) are tied together and floating. The circled devices are located in separate dielectrically isolated pockets. Floating the output switch backgates with the signal input increases the effective threshold voltage for an applied analog signal, thus providing a flatter R_{ON} versus V_S response.

For an "OFF" switch, device number 3 is "OFF," and the backgates of devices 4 and 5 are tied through 1kΩ resistors (R1 and R2) to the respective supply voltages through the "ON" devices 1 and 2.

If a voltage is applied to the S or D (OUT) terminal which exceeds V_{DD} or V_{SS}, the S- or D-to-backgate diode is forward biased; however, R1 and R2 provide current limiting action to the supplies.

An equivalent circuit of the output switch element in Figure 3 shows that, indeed, the 1kΩ limiting resistors are in series with the backgates of the P- and N-channel output devices – *not* in series with the signal path between the S and D terminals.

It is possible to turn on an "OFF" switch by applying a voltage in excess of V_{DD} or V_{SS} to the S or D terminal. If a positive stress voltage is applied to the S or D terminal which exceeds V_{DD} by a threshold, then the P-channel (device 5) will turn on creating a low impedance path between the S and D terminals. A similar situation exists for negative stress voltages which exceed V_{SS}. In this case the N-channel provides the low impedance path between the S and D terminals. The limiting factor on the overvoltage protection is the power dissipation of the package and is ±20V continuous (or 20mA whichever occurs first) above the supply voltages.

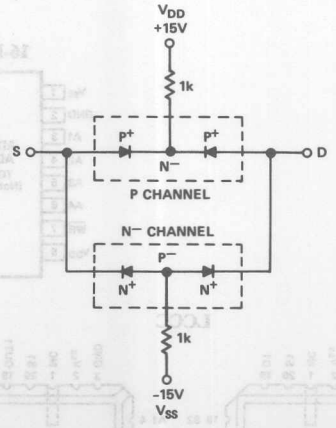
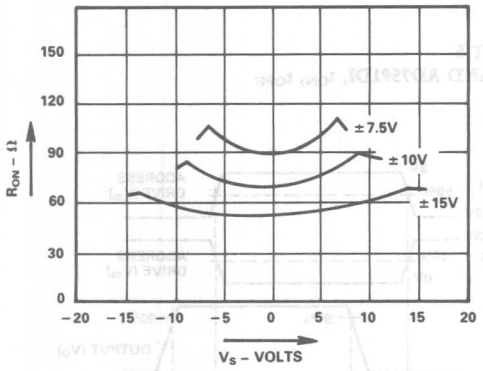
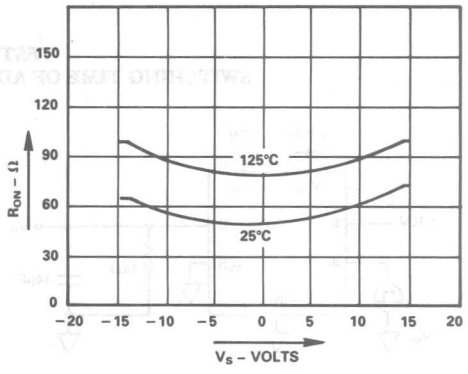


Figure 3. AD7590DI Series Output Switch Diode-Equivalent-Circuit



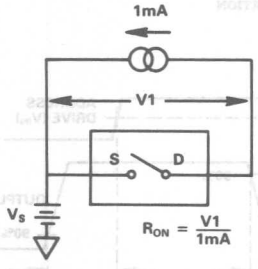
R_{ON} AS A FUNCTION OF V_D (V_S)
FOR DIFFERENT SUPPLY VOLTAGES



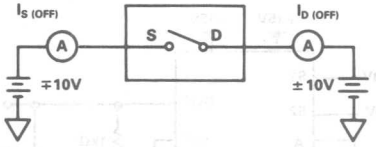
R_{ON} AS A FUNCTION OF V_S (V_D)
FOR DIFFERENT TEMPERATURES

5

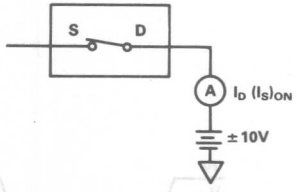
TEST CIRCUIT 1



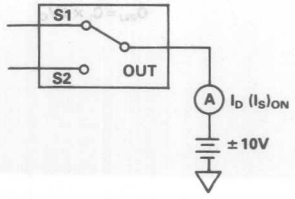
TEST CIRCUIT 2
(AD7590DI, AD7591DI)



TEST CIRCUIT 3

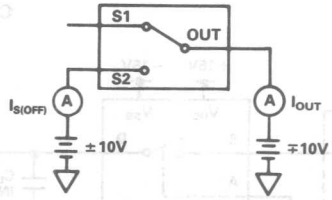


a. AD7590DI, AD7591DI



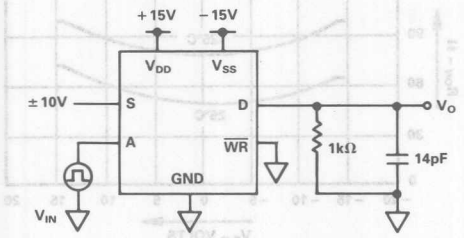
b. AD7592

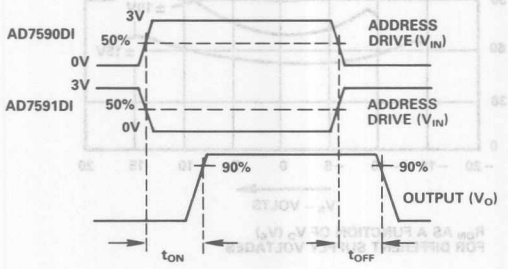
TEST CIRCUIT 4
(AD7592DI ONLY)



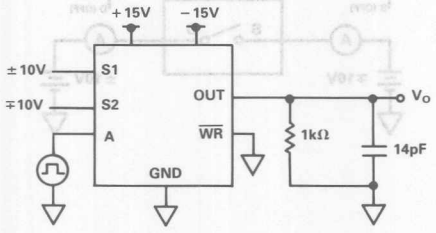
Note: All digital input signal rise and fall times measured from 10% to 90% of 3V. tr = tf = 20ns.

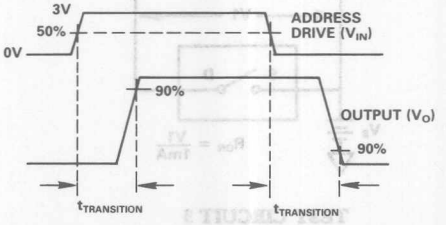
TEST CIRCUIT 5
SWITCHING TIME OF AD7590DI AND AD7591DI, t_{ON}, t_{OFF}



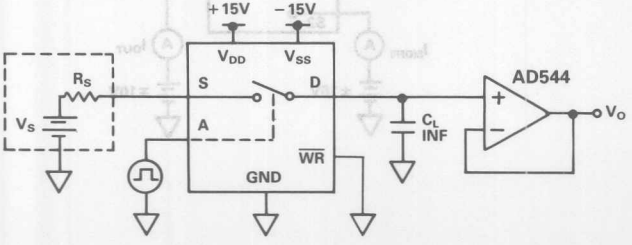


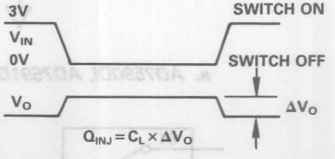
TEST CIRCUIT 6
SWITCHING TIME OF AD7592DI, $t_{TRANSITION}$





TEST CIRCUIT 7
CHARGE INJECTION





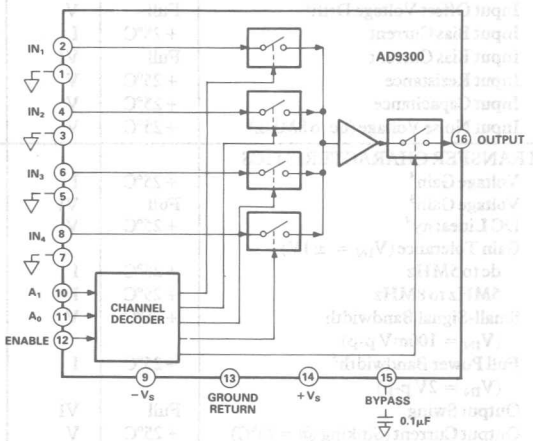
4 × 1 Wideband Video Multiplexer

AD9300

FEATURES
- 34MHz Full Power Bandwidth
- ±0.1dB Gain Flatness to 8MHz
- 72dB Crosstalk Rejection @ 10MHz
- 0.03°/0.01% Differential Phase/Gain
- Cascadable for Switch Matrices
- MIL-STD-883 Compliant Versions Available

APPLICATIONS
- Video Routing
- Medical Imaging
- Electro-Optics
- ECM Systems
- Radar Systems
- Data Acquisition

FUNCTIONAL BLOCK DIAGRAM
(Based on Cerdip)



5

GENERAL DESCRIPTION

The AD9300 is a monolithic high-speed video signal multiplexer useable in a wide variety of applications.

Its four channels of video input signals can be randomly switched at megahertz rates to the single output. In addition, multiple devices can be configured in either parallel or cascade arrangements to form switch matrices. This flexibility in using the AD9300 is possible because the output of the device is in a high-impedance state when the chip is not enabled; when the chip is enabled, the unit acts as a buffer with a high input impedance and low output impedance.

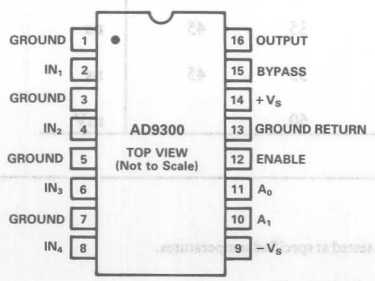
An advanced bipolar process provides fast, wideband switching capabilities while maintaining crosstalk rejection of 72dB at 10MHz. Full power bandwidth is a minimum 27MHz. The device can be operated from ±10V to ±15V power supplies.

The AD9300K is available in a 16-pin ceramic DIP and a 20-pin PLCC and is designed to operate over the commercial temperature range of 0 to +70°C. The AD9300TQ is a hermetic 16-pin ceramic DIP for military temperature range (−55°C to +125°C) applications. This part is also available processed to MIL-STD-883. The AD9300 is available in a 20-pin LCC as the model AD9300TE, which operates over a temperature range of −55°C to +125°C.

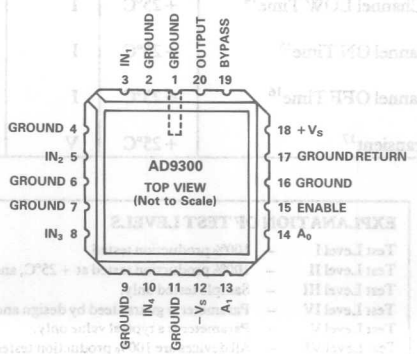
The AD9300 Video Multiplexer is available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current AD9300/883B data sheet for detailed specifications.

PIN DESIGNATIONS

DIP



LCC and PLCC



(PLCC PINOUTS SAME AS LCC)

AD9300–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($\pm V_S = \pm 12V \pm 5\%$; $C_L = 10pF$; $R_L = 2k\Omega$, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	COMMERCIAL 0°C to +70°C AD9300KQ/KP Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Input Offset Voltage	+25°C	I		3	10	mV
Input Offset Voltage	Full	VI			14	mV
Input Offset Voltage Drift[2]	Full	V		75		µV/°C
Input Bias Current	+25°C	I		15	37	µA
Input Bias Current	Full	VI			55	µA
Input Resistance	+25°C	V		3.0		MΩ
Input Capacitance	+25°C	V		2		pF
Input Noise Voltage (dc to 8MHz)	+25°C	V		16		µV rms
TRANSFER CHARACTERISTICS						
Voltage Gain[3]	+25°C	I	0.990	0.994		V/V
Voltage Gain[3]	Full	VI	0.985			V/V
DC Linearity[4]	+25°C	V		0.01		%
Gain Tolerance ($V_{IN} = \pm 1V$)						
dc to 5MHz	+25°C	I		0.05	0.1	dB
5MHz to 8MHz	+25°C	I		0.1	0.3	dB
Small-Signal Bandwidth (V_{IN} = 100mV p-p)	+25°C	V		350		MHz
Full Power Bandwidth[5] (V_{IN} = 2V p-p)	+25°C	I	27	34		MHz
Output Swing	Full	VI	±2			V
Output Current (Sinking @ = 25°C)	+25°C	V		5		mA
Output Resistance	+25°C	IV, V		9	15	Ω
DYNAMIC CHARACTERISTICS						
Slew Rate[6]	+25°C	I	170	215		V/µs
Settling Time (to 0.1% on ±2V Output)	+25°C	IV		70	100	ns
Overshoot						
To T-Step[7]	+25°C	V		<0.1		%
To Pulse[8]	+25°C	V		<10		%
Differential Phase[9]	+25°C	IV		0.03	0.1	°
Differential Gain[9]	+25°C	IV		0.01	0.1	%
Crosstalk Rejection						
Three Channels[10]	+25°C	IV	68	72		dB
One Channel[11]	+25°C	IV	70	76		dB
SWITCHING CHARACTERISTICS[12]						
A_X Input to Channel HIGH Time[13] (t_{HIGH})	+25°C	I		40	50	ns
A_X Input to Channel LOW Time[14] (t_{LOW})	+25°C	I		35	45	ns
Enable to Channel ON Time[15] (t_{ON})	+25°C	I		35	45	ns
Enable to Channel OFF Time[16] (t_{OFF})	+25°C	I		35	45	ns
Switching Transient[17]	+25°C	V		60		mV

EXPLANATION OF TEST LEVELS

Test Level I – 100% production tested.
Test Level II – 100% production tested at + 25°C, and sample tested at specified temperatures.
Test Level III – Sample tested only.
Test Level IV – Parameter is guaranteed by design and characterization testing.
Test Level V – Parameter is a typical value only.
Test Level VI – All devices are 100% production tested at + 25°C. 100% production tested at temperature extremes for military temperature devices; sample tested at temperature extremes for commercial/industrial devices.

Parameter (Conditions)	Temp	Test Level	COMMERCIAL 0°C to +70°C AD9300KQ/KP Min	Typ	Max	Units
DIGITAL INPUTS						
Logic "1" Voltage	Full	VI	2			V
Logic "0" Voltage	Full	VI			0.8	V
Logic "1" Current	Full	VI			5	μA
Logic "0" Current	Full	VI			1	μA
POWER SUPPLY						
Positive Supply Current (+12V)	+25°C	I		13	16	mA
Positive Supply Current (+12V)	Full	VI		13	16	mA
Negative Supply Current (−12V)	+25°C	I		12.5	15	mA
Negative Supply Current (−12V)	Full	VI		12.5	16	mA
Power Supply Rejection Ratio ($\pm V_S = \pm 12V \pm 5\%$)	Full	VI	67	75		dB
Power Dissipation (±12V)[18]	+25°C	V		306		mW

NOTES
[1]Permanent damage may occur if any one absolute maximum rating is exceeded. Functional operation is not implied, and device reliability may be impaired by exposure to higher-than-recommended voltages for extended periods of time.
[2]Measured at extremes of temperature range.
[3]Measured as slope of V_{OUT} versus V_{IN} with $V_{IN} = \pm 1V$.
[4]Measured as worst deviation from end-point fit with $V_{IN} = \pm 1V$.
[5]Full Power Bandwith (FPBW) based on Slew Rate (SR). FPBW = $SR/2\pi V_{PEAK}$
[6]Measured between 20% and 80% transition points of ±1V output.
[7]T-Step = Sin^2X Step, when Step between 0V and +700mV points has 10%-to-90% risetime = 125ns.
[8]Measured with a pulse input having slew rate >250V/μs.
[9]Measured at output between 0.28Vdc and 1.0Vdc with V_{IN} = 284mV p–p at 3.58MHz and 4.43MHz.
[10]This specification is critically dependent on circuit layout. Value shown is measured with selected channel grounded and 10MHz 2V p–p signal applied to remaining three channels. If selected channel is grounded through 75Ω, value is approximately 6dB higher.
[11]This specification is critically dependent on circuit layout. Value shown is measured with selected channel grounded and 10MHz 2V p–p signal applied to one other channel. If selected channel is grounded through 75Ω, value is approximately 6dB higher. Minimum specification in ( ) applies to DIPs.
[12]Consult system timing diagram.
[13]Measured from address change to 90% point of −2V to +2V output LOW-to-HIGH transition.
[14]Measured from address change to 90% point of +2V to −2V output HIGH-to-LOW transition.
[15]Measured from 50% transition point of ENABLE input to 90% transition of 0V to −2V and 0V to +2V output.
[16]Measured from 50% transition point of ENABLE input to 10% transition of +2V to 0V and −2V to 0V output.
[17]Measured while switching between two grounded channels.
[18]Maximum power dissipation is a package-dependent parameter related to the following typical thermal impedances:
16-Pin Ceramic θ_{JA} = 87°C/W; θ_{JC} = 25°C/W
20-Pin LCC θ_{JA} = 74°C/W; θ_{JC} = 10°C/W
20-Pin PLCC θ_{JA} = 71°C/W; θ_{JC} = 26°C/W

Specifications subject to change without notice.

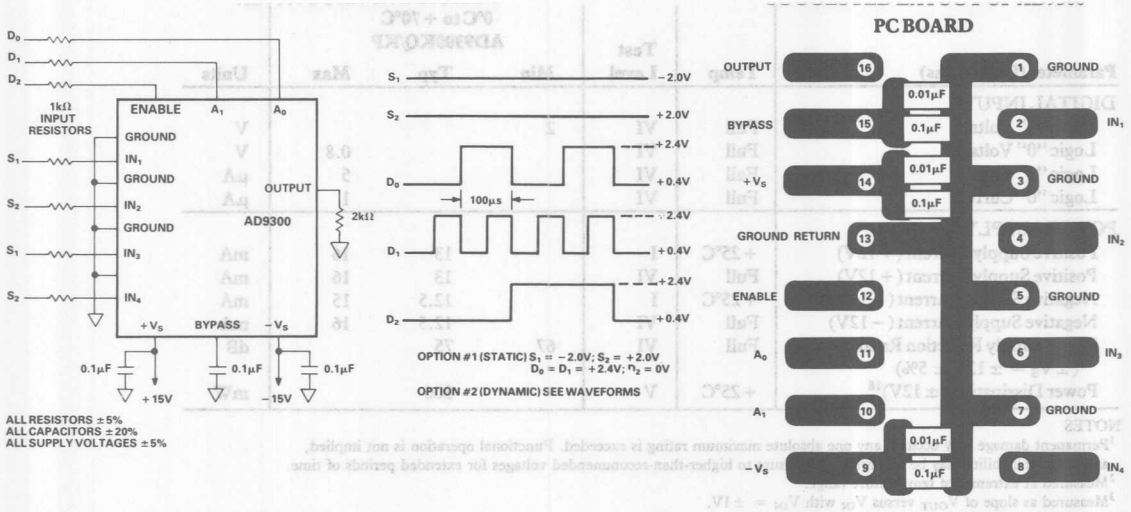
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±16V
Analog Input Voltage Each Input (IN_1 thru IN_4) . . . . . ±3.5V
Differential Voltage Between Any Two Inputs (IN_1 thru IN_4) 5V
Digital Input Voltages (A_0, A_1, ENABLE) . −0.5V to +5.5V
Output Current
Sinking 6.0mA
Sourcing 6.0mA
Operating Temperature Range
AD9300KQ/KP . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering (10sec) . . . . . +300°C

ORDERING GUIDE

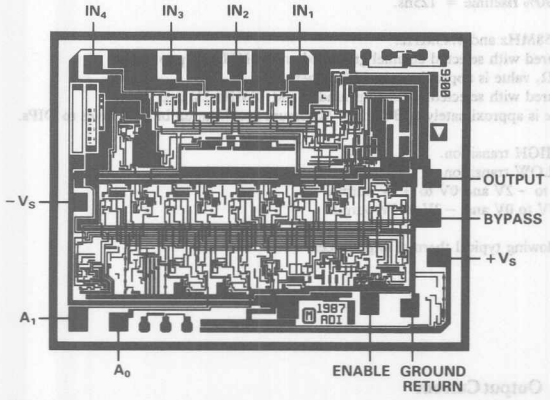
Device	Temperature Range	Description	Package Option[1]
AD9300KQ	0 to +70°C	16-Pin Cerdip, Commercial	Q-16
AD9300TE/883B[2]	−55°C to +125°C	20-Pin LCC, Military Temperature	E-20A
AD9300TQ/883B[2]	−55°C to +125°C	16-Pin Cerdip, Military Temperature	Q-16
AD9300KP	0 to +70°C	20-Pin PLCC, Commercial	P-20A

NOTES
[1]E = Ceramic Leadless Chip Carrier; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.
[2]For specifications, refer to Analog Devices *Military Products Databook*.



Suggested Layout of AD9300 PC Board
(Bottom View – Not to Scale)
Component Side Should be Ground Plane

METALIZATION PHOTOGRAPH



MECHANICAL INFORMATION

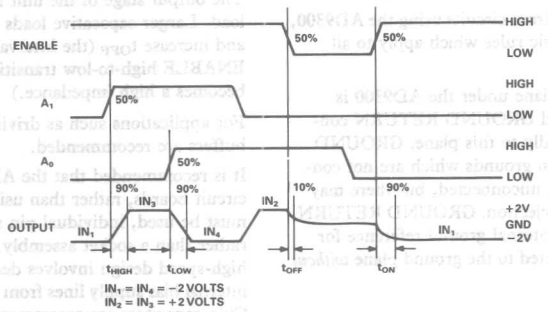
Die Dimensions	84 × 104 × 18 (max) mils
Pad Dimensions	4 × 4 (min) mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil, Aluminum; Ultrasonic Bonding or 1 mil, Gold; Gold Ball Bonding

FUNCTIONAL DESCRIPTION

$IN_1 - IN_4$	Four analog input channels.
GROUND	Analog input shielding grounds, not internally connected. Connect each to external low-impedance ground as close to device as possible.
A_0	One of two TTL decode control lines required for channel selection. See Logic Truth Table.
A_1	One of two TTL decode control lines required for channel selection. See Logic Truth Table.
ENABLE	TTL-compatible chip enable. In enabled mode (logic HIGH), output signal tracks selected input channel; in disabled mode (logic LOW), output is high impedance and no signal appears at output.
$-V_S$	Negative supply voltage; nominally −10V dc to −15V dc.
$+V_S$	Positive supply voltage; nominally +10V dc to +15V dc.
OUTPUT	Analog output. Tracks selected input channel when enabled.
BYPASS	Bypass terminal for internal bias line; must be decoupled externally to ground through 0.1µF capacitor.
GROUND RETURN	Analog signal and power supply ground return.

LOGIC TRUTH TABLE

ENABLE	A_1	A_0	OUTPUT
0	X	X	High Z
1	0	0	IN_1
1	0	1	IN_2
1	1	0	IN_3
1	1	1	IN_4



AD9300 Timing

THEORY OF OPERATION

Refer to the functional block diagram of the AD9300.

As shown on the drawing, this diagram is based on the pinouts of the DIP packaging of the models AD9300KQ and AD9300TQ. The AD9300KP and AD9300TE are packaged in 20-pin surface mount packages. The extra pins are used for ground connections; the theory of operation remains the same.

The AD9300 Video Multiplexer allows the user to connect any one of four analog input channels ($IN_1 - IN_4$) to the output of the device, and to switch between channels at megahertz rates.

The input channel which is connected to the output is determined by a 2-bit TTL digital code applied to A_0 and A_1. The selected input will not appear at the output unless a digital "1" is also applied to the ENABLE input pin; unless the output is enabled, it is a high impedance. Necessary combinations to accomplish channel selection are shown in the Logic Truth Table.

Bipolar construction used in the AD9300 insures that the input impedance of the device remains high, and will not vary with power supply voltages. This characteristic makes the AD9300, in effect, a switchable-input buffer. An on-board bias network makes the performance of the AD9300 independent of applied supply voltages, which can have any nominal value from ±10V dc to ±15V dc.

Although the primary application for the AD9300 is the routing of video signals, the harmonic and dynamic attributes of the device make it appropriate for other applications. The AD9300 has exceptional performance when switching video signals, but can also be used for switching other analog signals requiring greater dynamic range and/or precision than those in video.

As shown in Figure 1, Input and Output Equivalent Circuits, each analog input is connected to the base of a bipolar transistor. If Channel 1 is selected, a current switch is closed and routes current through the input transistor for Channel 1.

If Channel 2 is then selected by the digital inputs, the current switch for Channel 1 is opened and the current switch for Channel 2 is closed. This causes current to be routed away from the Channel 1 transistor and into the Channel 2 input transistor. Whenever a channel's input device is carrying current, the analog input applied to that channel is passed to the output stage.

The operation of the output stage is similar to that of the input stages. Whenever the output stage is enabled with a HIGH digital "1" signal at the ENABLE pin, the output transistor will carry current and pass the selected analog input.

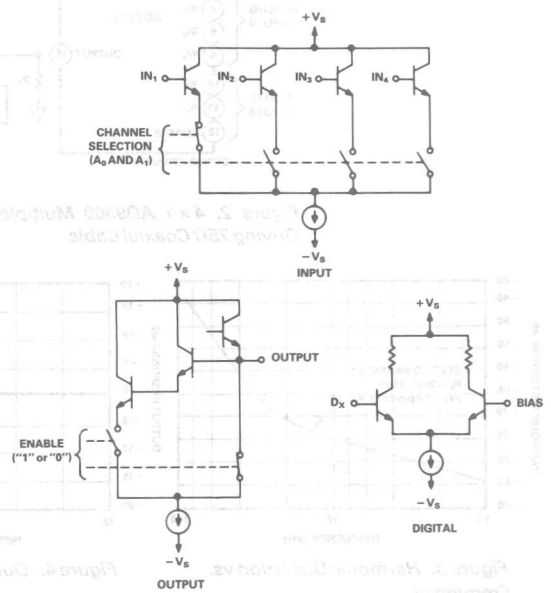


Figure 1. Input and Output Equivalent Circuits

When the output stage is disabled (by virtue of the ENABLE pin being driven LOW with a digital "0"), the output current switch is opened. This routes the current to other circuits within the AD9300 which keep the output transistor biased "off". These circuits require approximately 1μA of bias current from the load connected to the output of the multiplexer. In the absence of a terminating load and the resulting dc bias, the output of the AD9300 "floats" at −2.5V.

In summary, when the AD9300 is enabled by the ENABLE pin being driven HIGH with a digital "1", the selected analog input channel acts as a buffer for the input; and the output of the multiplexer is a low impedance. When the AD9300 is disabled with a digital "0" LOW signal, the selected channel acts as an open switch for the input; and the output of the unit becomes a high impedance. This characteristic allows the user to wire-or several AD9300 Analog Multiplexers together to form switch matrices.

AD9300 APPLICATIONS

To ensure optimum performance from circuits using the AD9300, it is important to follow a few basic rules which apply to all high-speed devices.

A large, low-impedance ground plane under the AD9300 is critical. Generally, GROUND and GROUND RETURN connections should be connected solidly to this plane. GROUND pin connections are signal isolation grounds which are not connected internally; they can be left unconnected, but there may be some degradation in crosstalk rejection. GROUND RETURN, on the other hand, serves as the internal ground reference for the AD9300 and should be connected to the ground plane *without exception*.

The output stage of the unit is capable of driving a 2kΩ‖10pF load. Larger capacative loads may limit full power bandwidth and increase t_{OFF} (the interval between the 50% point of the ENABLE high-to-low transition and the instant the output becomes a high impedance.)

For applications such as driving cables (See Figure 2), output buffers are recommended.

It is recommended that the AD9300 be soldered directly into circuit boards, rather than using socket assemblies. If sockets must be used, individual pin sockets are the preferred choice, rather than a socket assembly. A second requirement for proper high-speed design involves decoupling the power supply and internal bias supply lines from ground to improve noise immunity. Chip capacitors are recommended for connecting 0.1μF and 0.01μF capacitors between ground and the $\pm V_S$ supplies (Pins 9 and 14), and the BYPASS connection (Pin 15).

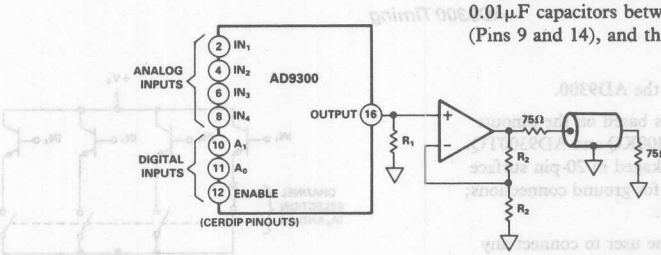


Figure 2. 4×1 AD9300 Multiplexer with Buffered Output Driving 75Ω Coaxial Cable

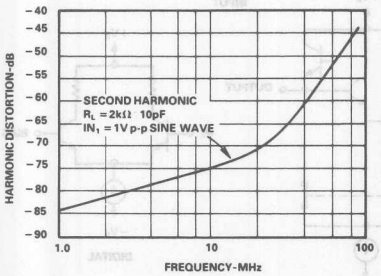


Figure 3. Harmonic Distortion vs. Frequency

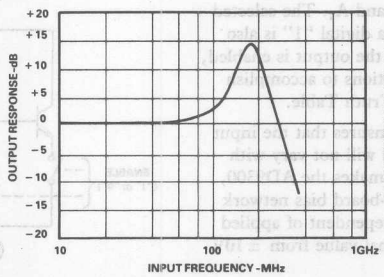


Figure 4. Output vs. Frequency

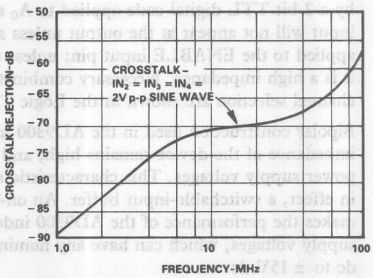


Figure 5. Crosstalk vs. Frequency

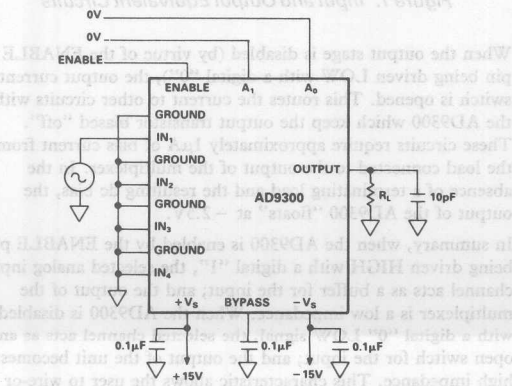


Figure 6. Test Circuit for Harmonic Distortion, Pulse Response, T-Step Response and Disable Characteristics

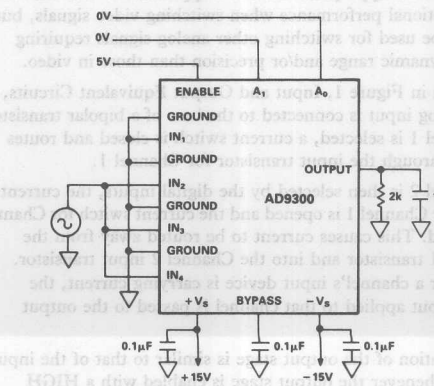


Figure 7. Crosstalk Rejection Test Circuit

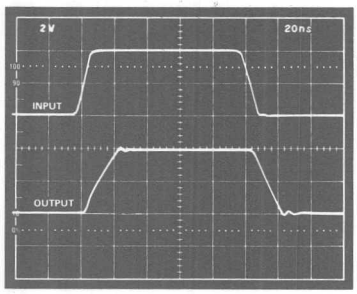


Figure 8. Pulse Response

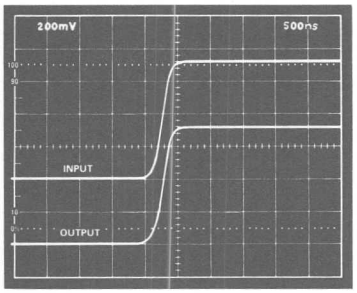


Figure 9. T-Step Response

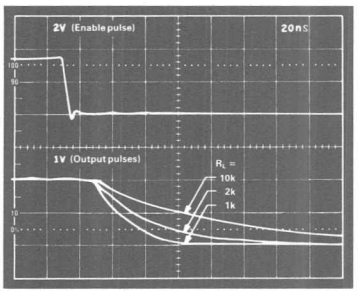


Figure 10. Enable to Channel "Off" Response

CROSSPOINT CIRCUIT APPLICATIONS

Four AD9300 multiplexers can be used to implement an 8×2 crosspoint, as shown in Figure 11. The circuit is modular in concept, with each pair of multiplexers (#1 and #2; #3 and #4) forming an 8×1 crosspoint. When the inputs to all four units are connected as shown, the result is an 8×2 crosspoint circuit.

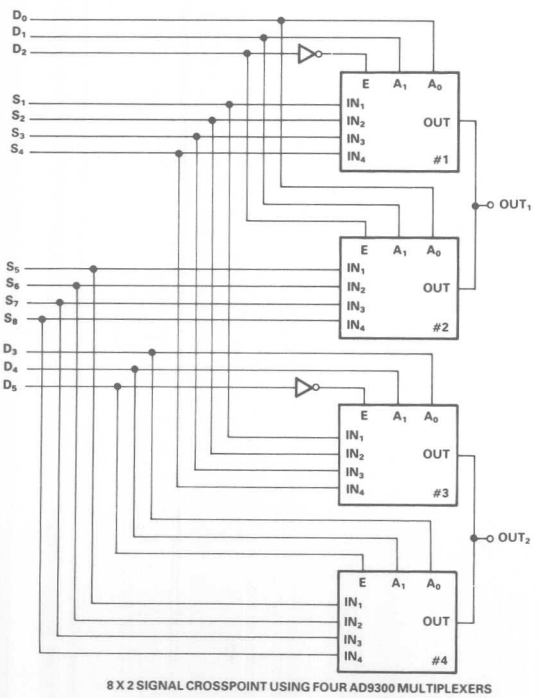


Figure 11. 8×2 Signal Crosspoint Using Four AD9300 Multiplexers

The truth table describes the relationships among the digital inputs (D_0 – D_5) and the analog inputs (S_1 – S_8); and which signal input is selected at the outputs (OUT_1 and OUT_2). The number of crosspoint modules that can be connected in parallel is limited by the drive capabilities of the input signal sources. High input impedance (3MΩ) and low input capacitance (2pF) of the AD9300 help minimize this limitation.

8 × 2 Crosspoint Truth Table

D_2 or D_5	D_1 or D_4	D_0 or D_3	OUT_1 or OUT_2
0	0	0	S_1
0	0	1	S_2
0	1	0	S_3
0	1	1	S_4
1	0	0	S_5
1	0	1	S_6
1	1	0	S_7
1	1	1	S_8

Adding to the number of inputs applied to each crosspoint module is simply a matter of adding AD9300 multiplexers in parallel to the module. Eight devices connected in parallel result in a 32×1 crosspoint which can be used with input signals having 30MHz bandwidth and 1V peak-to-peak amplitude. Even more AD9300 units can be added if input signal amplitude and/or bandwidth are reduced; if they are not, distortion of the output signals can result.

When an AD9300 is enabled, its low output impedance causes the "off" isolation of disabled parallel devices to be greater than the crosstalk rejection of a single unit.

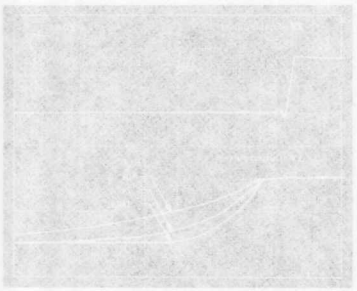


Figure 8. Pulse Response

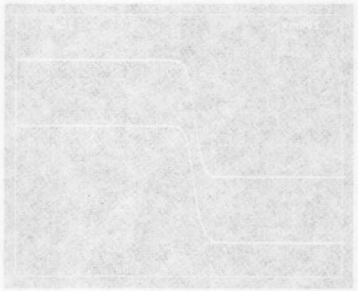


Figure 9. T-Step Response

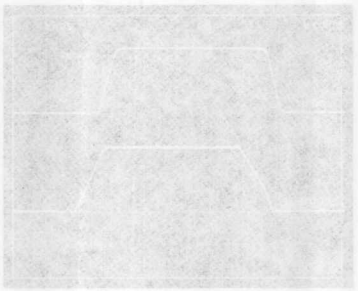


Figure 10. Enable to Channel "Off" Response

CROSSPOINT CIRCUIT APPLICATIONS

Four AD9300 multiplexers can be used to implement an 8 × 2 crosspoint, as shown in Figure 11. The circuit is modular in concept, with each pair of multiplexers (#1 and #2; #3 and #4) forming an 8 × 1 crosspoint. When the inputs to all four units are connected as shown, the result is an 8 × 2 crosspoint circuit.

Figure 11. 8 × 2 Signal Crosspoint Using Four AD9300 Multiplexers

The truth table describes the relationship among the digital inputs (D_0 – D_2) and the analog inputs (S_1 – S_8); and which signal input is selected at the outputs (OUT_1 and OUT_2). The number of crosspoint modules that can be connected in parallel is limited by the drive capabilities of the input signal sources. High input impedance (3MΩ) and low input capacitance (2pF) of the AD9300 help minimize this limitation.

8 × 2 Crosspoint Truth Table

D_2 or D_5	D_1 or D_4	D_0 or D_3	OUT_1 or OUT_2
0	0	0	S_1
0	0	1	S_2
0	1	0	S_3
0	1	1	S_4
1	0	0	S_5
1	0	1	S_6
1	1	0	S_7
1	1	1	S_8

Adding to the number of inputs applied to each crosspoint module is simply a matter of adding AD9300 multiplexers in parallel to the module. Eight devices connected in parallel result in a 32 × 1 crosspoint which can be used with input signals having 30MHz bandwidth and 1V peak-to-peak amplitude. Even more AD9300 units can be added if input signal amplitude and/or bandwidth are reduced; if they are not, distortion of the output signals can result.

When an AD9300 is enabled, its low output impedance causes the "off" isolation of disabled parallel devices to be greater than the crosstalk rejection of a single unit.

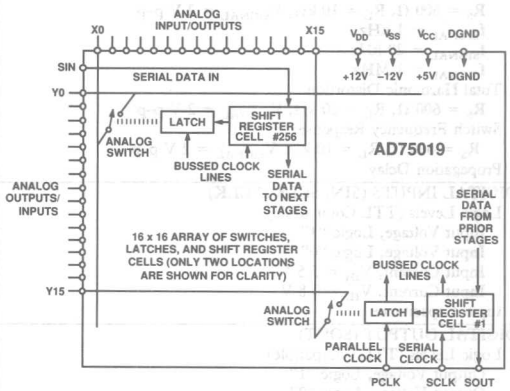
16 × 16 Crosspoint Switch Array

AD75019

FEATURES

256 Switches in a 16 × 16 Array
Wide Signal Range: to Supply Rails of 24 V or ±12 V
Low On-Resistance: 200 Ω typ
TTL/CMOS/Microprocessor-Compatible Control Lines
Serial Input Simplifies Interface
Serial Output Allows Cascading for More Channels
Low Power Consumption: 2 mW Quiescent
Compact 44-Pin Package

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD75019 contains 256 analog switches in a 16 × 16 array. Any of the X or Y pins may serve as an input or output. Any or all of the X terminals may be programmed to connect to any or all of the Y terminals. The switches can accommodate signals with amplitudes up to the supply rails and have a typical on-resistance of 150 Ω.

Data is loaded serially via the SIN input and clocked into an on-board 256-bit shift register via SCLK. When all the switch settings have been programmed, data is transferred into a set of 256 latches via PCLK. The serial shift register is dynamic, so there is a minimum clock rate of 20 kHz. The maximum clock rate of 5 MHz allows loading times as short as 52 µs. The switch control latches are static and will hold their data as long as power is applied.

To extend the number of switches in the array, you may cascade multiple AD75019s. The SOUT output is the end of the shift register, and may be connected to the SIN input of the next AD75019.

The AD75019 is fabricated in Analog Devices' BiMOS II process. This epitaxial BiCMOS process features CMOS devices for low-distortion switches and bipolar devices for ESD protection.

5

AD75019	Symbol	Min	Typ	Max	Units
MULTIPLEXER					
Input Signal Range	V_{IN}	V_{SS} − 0.5		V_{DD} + 0.5	V
Switch ON Resistance, V_{DD} & V_{SS} = ±12 V, V_{SIGNAL} = ±12 V	R_{ON}		150	**300**	Ω
Switch ON Resistance, V_{DD} & V_{SS} = ±5 V, V_{SIGNAL} = ±5 V	R_{ON}		300	500	Ω
Switch ON Resistance Matching [2], V_{SIGNAL} = ±12 V	ΔR_{ON}		20	**30**	Ω
Leakage Current, V_{SIGNAL} = ±10 V			2	10	nA
Input/Output Capacitance	C_{IN}			25	pF
Isolation Between Any Two Channels					
R_S = 600 Ω, R_L = 10 kΩ, V_{SIGNAL} = 2 V p–p					
f_{SIGNAL} = 1 kHz		92			dB
f_{SIGNAL} = 20 kHz		69			dB
f_{SIGNAL} = 1 MHz		38			dB
Total Harmonic Distortion					
R_S = 600 Ω, R_L = 10 kΩ, V_{SIGNAL} = 2 V p–p				0.01	%
Switch Frequency Response, − 3 dB					
R_S = 600 Ω, R_L = 10 kΩ, V_{SIGNAL} = 2 V p–p		20			MHz
Propagation Delay			4	8	ns
DIGITAL INPUTS (SIN, SCLK, PCLK)					
Logic Levels (TTL Compatible)					
Input Voltage, Logic "1"	V_{IH}	**2.4**		5.5	V
Input Voltage, Logic "0"	V_{IL}	0		**0.8**	V
Input Current, V_{IH} = 5.5 V	I_{IH}			±1	μA
Input Current, V_{IL} = 0.8 V	I_{IL}			±1	μA
Input Capacitance	C_{IN}			10	pF
DIGITAL OUTPUT (SOUT)					
Logic Levels (TTL Compatible)					
Output Voltage, Logic "1"	V_{DH}	2.8			V
Output Voltage, Logic "0"	V_{OL}			0.4	V
Output Current, V_{OH} = 2.8 V	I_{OH}	3.2			μA
Output Current, V_{OL} = 0.4 V	I_{OL}	3.2			μA
POWER SUPPLY REQUIREMENTS					
Voltage Range, Total Analog	V_{DD}–V_{SS}	9.0		25.2	V
Voltage Range, Positive Analog	V_{DD} − V_{DGND}	(V_{CC} − 0.5)		25.2	V
Voltage Range, Negative Analog	V_{SS} − V_{DGND}	−20.7		0	V
Voltage Range, Digital	V_{CC} − V_{DGND}	4.5	5	5.5	V
Supply Current, SCLK = 5 MHz,	I_{DD}, I_{SS}			±1	mA
V_{IL} = 0.8 V, V_{IH} = 2.4 V	I_{CC}			500	μA
Supply Current, Quiescent,	I_{DD}, I_{SS}	—		**±400**	μA
V_{IL} = 0.8 V, V_{IH} = 2.4 V	I_{CC}	—		**100**	μA
TEMPERATURE RANGE					
Operating	T_{min}, T_{max}	−25		+85	°C
Storage		−65		+150	°C

NOTES

[1]All minimum and maximum specifications are guaranteed, and specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

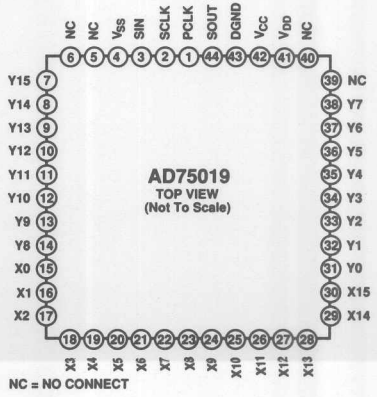
[2]Switch resistance matching is measured with zero volts at each analog input and refers to the difference between the maximum and minimum values.

Specifications subject to change without notice.

PIN DESCRIPTION

Pin	Name	Description
1	PCLK	Parallel Clock Input
2	SCLK	Serial Clock Input
3	SIN	Serial Data Input
4	V_{SS}	Negative Analog Power Supply
5	NC	No Internal Connection
6	NC	No Internal Connection
7	Y15	Analog Output (or Input)
8	Y14	Analog Output (or Input)
9	Y13	Analog Output (or Input)
10	Y12	Analog Output (or Input)
11	Y11	Analog Output (or Input)
12	Y10	Analog Output (or Input)
13	Y9	Analog Output (or Input)
14	Y8	Analog Output (or Input)
15	X0	Analog Input (or Output)
16	X1	Analog Input (or Output)
17	X2	Analog Input (or Output)
18	X3	Analog Input (or Output)
19	X4	Analog Input (or Output)
20	X5	Analog Input (or Output)
21	X6	Analog Input (or Output)
22	X7	Analog Input (or Output)
23	X8	Analog Input (or Output)
24	X9	Analog Input (or Output)
25	X10	Analog Input (or Output)
26	X11	Analog Input (or Output)
27	X12	Analog Input (or Output)
28	X13	Analog Input (or Output)
29	X14	Analog Input (or Output)
30	X15	Analog Input (or Output)
31	Y0	Analog Output (or Input)
32	Y1	Analog Output (or Input)
33	Y2	Analog Output (or Input)
34	Y3	Analog Output (or Input)
35	Y4	Analog Output (or Input)
36	Y5	Analog Output (or Input)
37	Y6	Analog Output (or Input)
38	Y7	Analog Output (or Input)
39	NC	No Internal Connection
40	NC	No Internal Connection
41	V_{DD}	Positive Analog Power Supply
42	V_{CC}	Digital Power Supply
43	DGND	Digital Ground
44	SOUT	Serial Data Output: Positive True

PIN CONFIGURATION

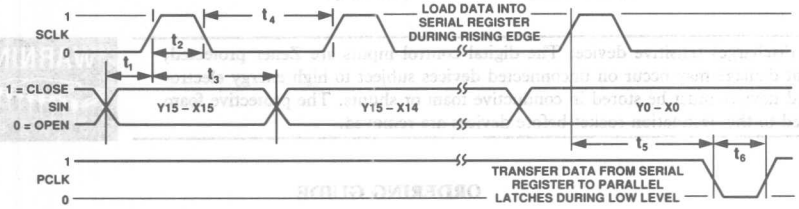


TIMING CHARACTERISTICS[1] ($T_A = T_{min}$ to T_{max}, rated power supplies unless otherwise noted)

Parameter	Symbol	Value	Units	Condition
Data Setup Time	t_1	0	ns	min
SCLK Pulse Width	t_2	100	ns	min
Data Hold Time	t_3	10	ns	min
SCLK Pulse Separation	t_4	100	ns	min
SCLK to PCLK Delay	t_5	65	ns	min
SCLK to PCLK Delay and Release	$(t_5 + t_6)$	5	ms	max
PCLK Pulse Width	t_6	65	ns	min
Propagation Delay, PCLK to Switches On or Off	—	70	ns	max
Data Load Time	—	52	µs	SCLK = 5 MHz
SCLK Frequency	—	20	kHz	min
SCLK, PCLK Rise and Fall Times	—	1	µs	max

NOTES
[1]Timing measurement reference level is 1.5 V.
Specifications subject to change without notice.

TIMING DIAGRAM



OPERATION TRUTH TABLE

Control Lines PCLK	SCLK	SIN	SOUT	Operation/ Comment
1	0	X	X	No operation.
1	1	$Data_i$	$Data_{i-256}$	The data on the SIN line is loaded into the serial register; data clocked into the serial register 256 clocks ago appears at the SOUT output.
0	X	X	X	Data in the serial shift register transfers into the parallel latches which control the switch array.

APPLICATIONS INFORMATION

Loading Data

Data to control the switches is clocked serially into a 256-bit shift register and then transferred in parallel to 256 bits of memory. The rising edge of SCLK, the serial clock input, loads data into the shift register. The first bit loaded via SIN, the serial data input, controls the switch at the intersection of row Y15 and column X15. The next bits control the remaining columns (down to X0) of row Y15, and are followed by the bits for row Y14, and so on down to the data for the switch at the intersection of row Y0 and column X0. The shift register is dynamic, so there is a minimum clock rate, specified as 20 kHz.

After the shift register is filled with the new 256 bits of control data, PCLK is activated (pulsed low) to transfer the data to the parallel latches. Since the shift register is dynamic, there is a maximum time delay specified before the data is lost: PCLK must be activated and brought back high within 5 ms after filling the shift register. The switch control latches are static and will hold their data as long as power is applied.

To extend the number of switches in the array, you may cascade multiple AD75019s. The SOUT output is the end of the shift register, and may be directly connected to the SIN input of the next AD75019.

Power Supply Sequencing and Bypassing

All junction-isolated parts operating on multiple power supplies require proper attention to supply sequencing. Because BiMOS II is a junction-isolated process, parasitic diodes exist between V_{DD} and V_{CC}, and between V_{SS} and DGND. As a result, V_{DD} must always be greater than (V_{CC} − 0.5 V), and V_{SS} must always be less than (DGND + 0.5 V).

If you can't ensure that system power supplies will sequence to meet these conditions, external Schottky (e.g., 1N5818) or silicon (e.g., 1N4001) diodes may be used. To protect the positive side, the anode would connect to V_{CC} (Pin 42) and the cathode to V_{DD} (Pin 41). For the negative side, connect the anode to V_{SS} (Pin 4) and the cathode to DGND (Pin 43).

Each of the three power supply pins [V_{DD} (Pin 41), V_{CC} (Pin 42) and V_{SS} (Pin 4)] should be bypassed to DGND (Pin 43) through a 0.1 µF ceramic capacitor located close to the package pins.

Transistor Count

AD75019 contains 5,472 transistors. This number may be used for calculating projected reliability.

ABSOLUTE MAXIMUM RATINGS*

	Min	Max	Units	Conditions
V_{DD} to DGND	−0.5	+25.2	V	
V_{SS} to DGND	−25.2	+0.5	V	
V_{CC} to DGND	−0.5	+5.5	V	
V_{DD} to V_{SS}	−0.5	+25.2	V	
V_{CC} to V_{SS}	−0.5	+25.2	V	
Digital Inputs to DGND	−0.3	V_{CC} +0.5	V	
Power Dissipation		1.0	W	$T_A \leq 75°C$
Operating Temperature Range	0	+70	°C	
Storage Temperature	−65	+150	°C	
Lead Temperature		+300	°C	Soldering, 10 sec

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



ORDERING GUIDE

Model	Temperature Range	Package Option*
AD75019JP	0°C to +70°C	P-44A

*P = Plastic Leaded Chip Carrier (PLCC) Package.

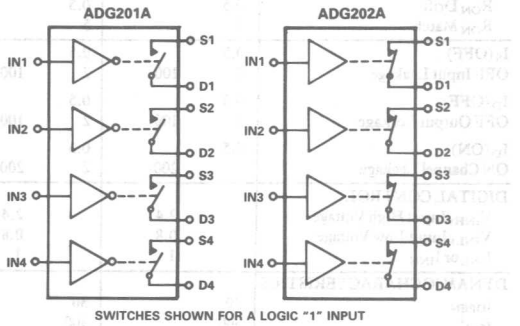
LC²MOS Quad SPST Switches

ADG201A/ADG202A

FEATURES

- 44V Supply Maximum Rating
- ±15V Analog Signal Range
- Low R_{ON} (60Ω)
- Low Leakage (0.5nA)
- Break Before Make Switching
- Extended Plastic Temperature Range (−40°C to +85°C)
- Low Power Dissipation (33mW)
- Available in 16-Lead DIP/ SOIC and 20-Lead PLCC/LCCC Packages
- Superior Second Source:
  - ADG201A Replaces DG201A, HI-201
  - ADG202A Replaces DG202

FUNCTIONAL BLOCK DIAGRAMS



5

GENERAL DESCRIPTION

The ADG201A and ADG202A are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS process which gives an increased signal handling capability of ±15V. These switches also feature high switching speeds and low R_{ON}.

The ADG201A and ADG202A consist of four SPST switches. They differ only in that the digital control logic is inverted. All devices exhibit break before make switching action. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended Signal Range:
   These switches are fabricated on an enhanced LC²MOS process, resulting in high breakdown and an increased analog signal range of ±15V.
2. Single Supply Operation:
   For applications where the analog signal is unipolar (0V to 15V), the switches can be operated from a single +15V supply.
3. Low Leakage:
   Leakage currents in the range of 500pA make these switches suitable for high precision circuits. The added feature of Break before Make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

Parameter	25°C	−40°C to +85°C	25°C	−40°C to +85°C	25°C	−55°C to +125°C	Units	Test Conditions
ANALOG SWITCH								
Analog Signal Range	±15	±15	±15	±15	±15	±15	Volts	
R_{ON}	60		60		60		Ω typ	$-10V \leq V_S \leq +10V$
	90	145	90	145	90	145	Ω max	$I_{DS} = 1.0mA$
								Test Circuit 1
R_{ON} vs. V_D (V_S)	20		20		20		% typ	
R_{ON} Drift	0.5		0.5		0.5		%/°C typ	
R_{ON} Match	5		5		5		% typ	$V_S = 0V$, $I_{DS} = 1mA$
I_S (OFF)	0.5		0.5		0.5		nA typ	$V_D = \pm 14V$; $V_S \mp 14V$; Test Circuit 2
OFF Input Leakage	2	100	2	100	1	100	nA max	
I_D (OFF)	0.5		0.5		0.5		nA typ	$V_D = \pm 14V$; $V_S = \mp 14V$; Test Circuit 2
OFF Output Leakage	2	100	2	100	1	100	nA max	
I_D (ON)	0.5		0.5		0.5		nA typ	$V_D = \pm 14V$; Test Circuit 3
ON Channel Leakage	2	200	2	200	1	200	nA max	
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	
DYNAMIC CHARACTERISTICS								
t_{OPEN}	30		30		30		ns typ	
t_{ON}[1]	300		300		300		ns max	Test Circuit 4
t_{OFF}[1]	250		250		250		ns max	Test Circuit 4
OFF Isolation	80		80		80		dB typ	$V_S = 10V$(p-p); f = 100kHz
								$R_L = 75\Omega$; Test Circuit 6
Channel-to-Channel Crosstalk	80		80		80		dB typ	Test Circuit 7
C_S (OFF)	5		5		5		pF typ	
C_D (OFF)	5		5		5		pF typ	
C_D, C_S (ON)	16		16		16		pF typ	
C_{IN} Digital Input Capacitance	5		5		5		pF typ	
Q_{INJ} Charge Injection	20		20		20		pC typ	$R_S = 0\Omega$; $C_L = 1000pF$; $V_S = 0V$
								Test Circuit 5
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	Digital Inputs = V_{INL} or V_{INH}
I_{DD}		2		2		2	mA max	
I_{SS}	0.1		0.1		0.1		mA typ	
I_{SS}		0.2		0.2		0.2	mA max	
Power Dissipation		33		33		33	mW max	

NOTES
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} to V_{SS} 44V
V_{DD} to GND 25V
V_{SS} to GND . . . . . −25V
Analog Inputs[1]
Voltage at S, D . . . . . V_{SS} −0.3V to V_{DD} +0.3V
Continuous Current, S or D 30mA
Pulsed Current S or D
1ms Duration, 10% Duty Cycle 70mA
Digital Inputs[1]
Voltage at IN . . . . . V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First

Power Dissipation (Any Package)
Up to +75°C 470mW
Derates above +75°C by . . . . . 6mW/°C
Operating Temperature
Commercial (K Version) . . . . . −40°C to +85°C
Industrial (B Version) . . . . . −40°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +300°C

NOTE
[1]Overvoltage at IN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG201AKN	−40°C to +85°C	N-16
ADG201AKR	−40°C to +85°C	R-16A
ADG201AKP	−40°C to +85°C	P-20A
ADG201ABQ	−40°C to +85°C	Q-16
ADG201ATQ	−55°C to +125°C	Q-16
ADG201ATE	−55°C to +125°C	E-20A
ADG202AKN	−40°C to +85°C	N-16
ADG202AKR	−40°C to +85°C	R-16A
ADG202AKP	−40°C to +85°C	P-20A
ADG202ABQ	−40°C to +85°C	Q-16
ADG202ATQ	−55°C to +125°C	Q-16
ADG202ATE	−55°C to +125°C	E-20A

NOTES

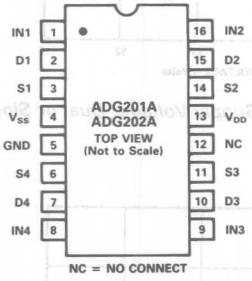
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers. See Analog Devices Military Products Databook (1990) for military data sheet.

[2]N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; E = Leadless Ceramic Chip Carrier (LCCC). For outline information see Package Information section.

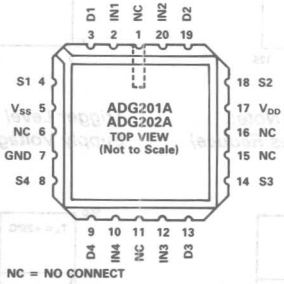
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PIN CONFIGURATIONS

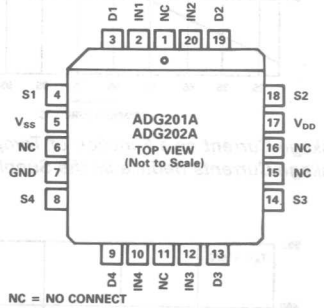
DIP, SOIC



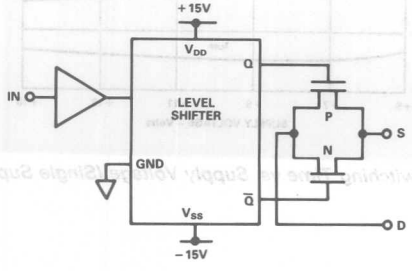
LCCC



PLCC



ADG201A/ADG202A FUNCTIONAL DIAGRAM



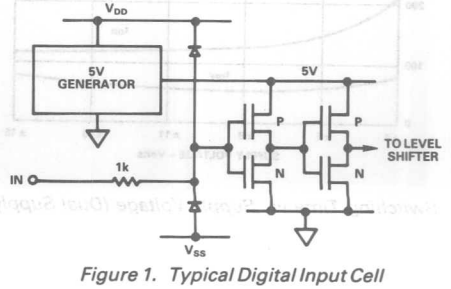
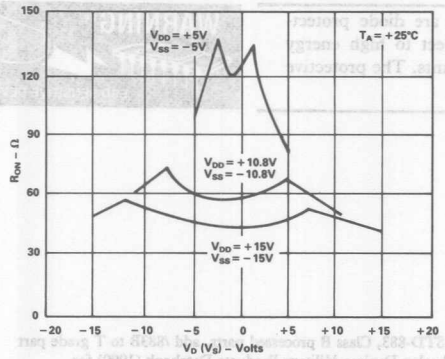


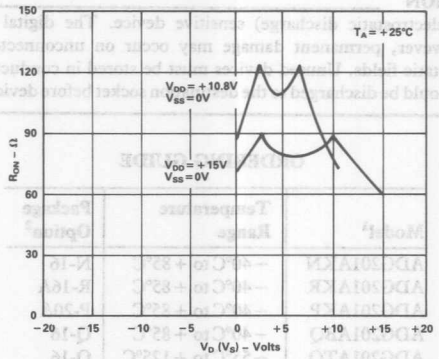
Figure 1. Typical Digital Input Cell

ADG201A/ADG202A—Typical Performance Characteristics

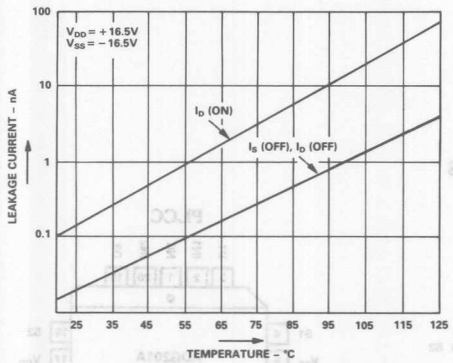
The switches are guaranteed functional with reduced single or dual supplies down to 4.5V.



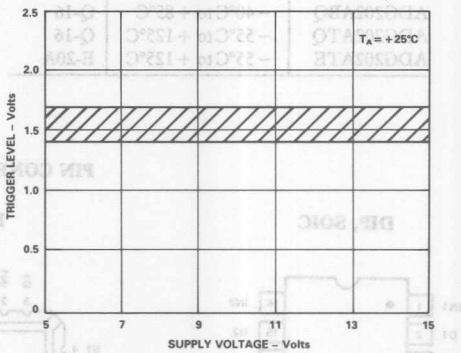
R_{ON} as a Function of V_D (V_S): Dual Supply Voltage



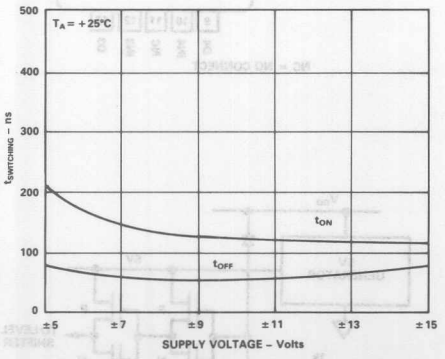
R_{ON} as a Function of V_D (V_S): Single Supply Voltage



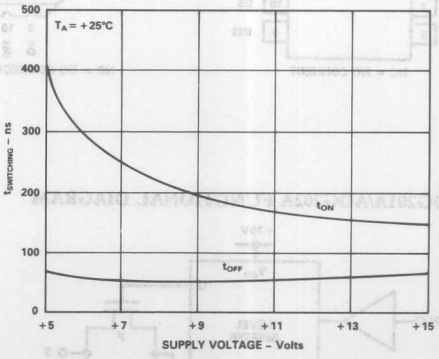
Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)



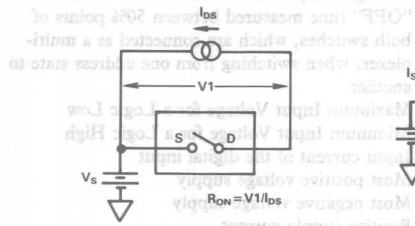
Trigger Level vs. Power Supply Voltage: Dual or Single Supply Voltage



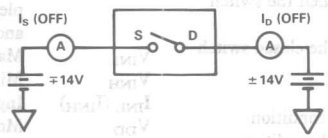
Switching Time vs. Supply Voltage (Dual Supply)



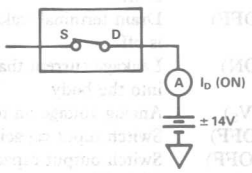
Switching Time vs. Supply Voltage (Single Supply)



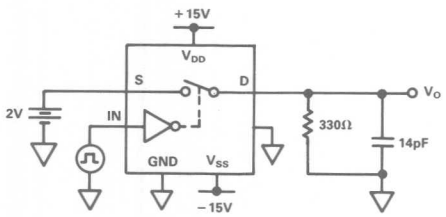
Test Circuit 1

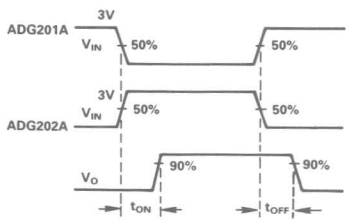


Test Circuit 2

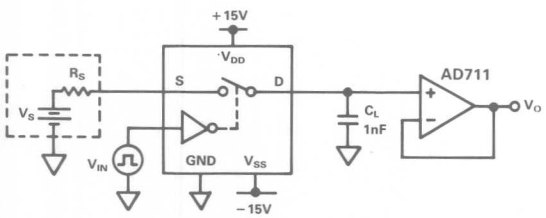


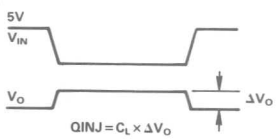
Test Circuit 3



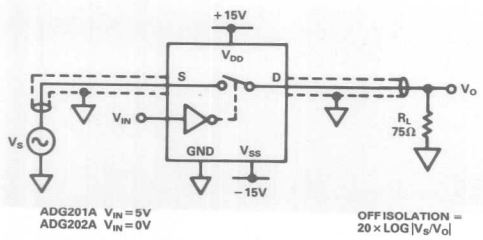


Test Circuit 4

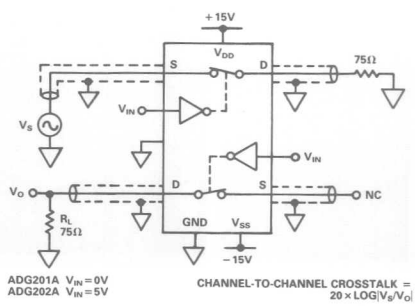




Test Circuit 5. Charge Injection



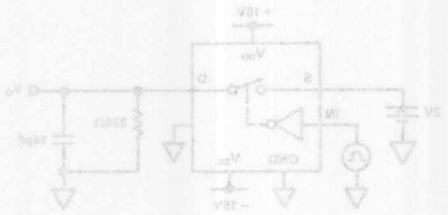
Test Circuit 6. Off Isolation

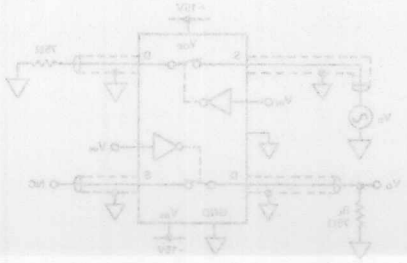


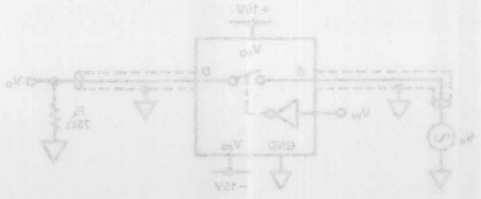
Test Circuit 7. Channel-to-Channel Crosstalk

TERMINOLOGY

R_{ON}	Ohmic resistance between terminals OUT and S
R_{ON} Match	Difference between the R_{ON} of any two channels
I_S (OFF)	Source terminal leakage current when the switch is off
I_D (OFF)	Drain terminal leakage current when the switch is off
I_D (ON)	Leakage current that flows from the closed switch into the body
V_D (V_S)	Analog voltage on terminal D, S
C_S (OFF)	Switch input capacitance "OFF" condition
C_D (OFF)	Switch output capacitance "OFF" condition
C_{IN}	Digital input capacitance
C_D, C_S (ON)	Input or output capacitance when the switch is on
t_{ON}	Delay time between the 50% and 90% points of the digital input and switch "ON" condition
t_{OFF}	Delay time between the 50% and 90% points of the digital input and switch "OFF" condition
t_{OPEN}	"OFF" time measured between 50% points of both switches, which are connected as a multiplexer, when switching from one address state to another
V_{INL}	Maximum Input Voltage for a Logic Low
V_{INH}	Minimum Input Voltage for a Logic High
I_{INL} (I_{INH})	Input current of the digital input
V_{DD}	Most positive voltage supply
V_{SS}	Most negative voltage supply
I_{DD}	Positive supply current
I_{SS}	Negative supply current







ANALOG DEVICES

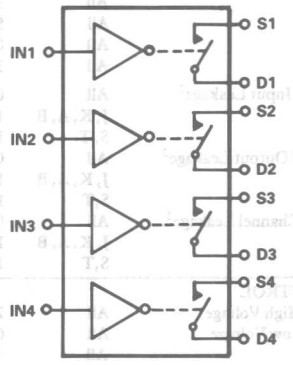
LC²MOS High Speed, Quad SPST Switch

ADG201HS

FEATURES

- 50ns max Switching Time Over Full Temperature Range
- Low R_{ON} (30Ω typ)
- Single Supply Specifications for +10.8V to +16.5V Operation
- Extended Plastic Temperature Range (−40°C to +85°C)
- Break-Before-Make Switching
- Low Leakage (100pA typ)
- 44V Supply max Rating
- Available in 16-Lead DIP/SOIC and 20-Lead LCCC/PLCC Packages
- ADG201HS (K, B, T) Replaces HI-201HS
- ADG201HS (J, A, S) Replaces DG271

FUNCTIONAL BLOCK DIAGRAM



5

GENERAL DESCRIPTION

The ADG201HS is a monolithic CMOS device comprising four independently selectable SPST switches. It is designed on an enhanced LC²MOS process which gives very fast switching speeds and low R_{ON}.

The switches also feature break-before-make switching action for use in multiplexer applications and low charge injection for minimum transients on the output when switching the digital inputs.

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG201HSJN	−40°C to +85°C	N-16
ADG201HSKN	−40°C to +85°C	N-16
ADG201HSKR	−40°C to +85°C	R-16A
ADG201HSAQ	−40°C to +85°C	Q-16
ADG201HSBQ	−40°C to +85°C	Q-16
ADG201HSJP	−40°C to +85°C	P-20A
ADG201HSKP	−40°C to +85°C	P-20A
ADG201HSSQ	−55°C to +125°C	Q-16
ADG201HSTQ[3]	−55°C to +125°C	Q-16
ADG201HSTE[3]	−55°C to +125°C	E-20A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers. See the Analog Devices Military Products Databook (1990) for military data sheet.
[2]E = Leadless Ceramic Chip Carrier; N = Narrow Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = 0.15″ Small Outline IC (SOIC). For outline information see Package Information section.
[3]Standard Military Drawing (SMD) approved by DESC. SMD numbers are
5962-86716012X (ADG201HSTE/883B)
5962-8671601EX (ADG201HSTQ/883B)

PRODUCT HIGHLIGHTS

1. 50ns max t_{ON} and t_{OFF}
   The ADG201HS top grades (K, B, T) have guaranteed 50ns max turn-on and turn-off times over the full operating temperature range. The lower grades (J, A, S) have guaranteed 75ns switching times over the full operating temperature range.
2. Single Supply Specifications
   The ADG201HS is fully specified for applications which require a single positive power supply in the +10.8V to +16.5V range.
3. Low Leakage
   Leakage currents in the range of 100pA make these switches suitable for high precision circuits. The added feature of break-before-make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

Truth Table

IN	Switch Condition
0	ON
1	OFF

ADG201HS—SPECIFICATIONS

Dual Supply (V_{DD} = +13.5V to +16.5V, V_{SS} = −13.5V to −16.5V, GND = 0V, V_{IN} = 3V (Logic High Level) or 0.8V (Logic Low Level) unless otherwise noted.)

Parameter	Version	+25°C	T_{min}–T_{max}[1]	Units	Comments
ANALOG SWITCH					
Analog Signal Range	All	V_{SS}	V_{SS}	Vmin	
	All	V_{DD}	V_{DD}	V max	
R_{ON}	All	30	–	Ω typ	$-10V \leq V_S \leq +10V$, I_{DS} = 1mA; Test Circuit 1
	All	50	75	Ω max	
R_{ON} Drift	All	0.5	–	%/°C typ	$-10V \leq V_S \leq +10V$, I_{DS} = 1mA
R_{ON} Match	All	3	–	% typ	$-10V \leq V_S \leq +10V$, I_{DS} = 1mA
I_S (OFF), Off Input Leakage[2]	All	0.1		nA typ	$V_D = \pm 14V$; $V_S = \mp 14V$; Test Circuit 2
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
I_D (OFF), Off Output Leakage[2]	All	0.1		nA typ	$V_D = \pm 14V$; $V_S = \mp 14V$; Test Circuit 2
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
I_D (ON), On Channel Leakage[2]	All	0.1		nA typ	$V_D = \pm 14V$; Test Circuit 3
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
DIGITAL CONTROL					
V_{INH}, Input High Voltage	All	2.4	2.4	V min	
V_{INL}, Input Low Voltage	All	0.8	0.8	V max	
I_{INL} or I_{INH}	All	1	1	μA max	
C_{IN}	All	8	8	pF max	
DYNAMIC CHARACTERISTICS					
t_{ON}	K, B, T	50	50	ns max	Test Circuit 4
	J, A, S	75	75	ns max	
t_{OFF1}	K, B, T	50	50	ns max	Test Circuit 4
	J, A, S	75	75	ns max	
t_{OFF2}	All	150	–	ns typ	Test Circuit 4
t_{OPEN}	All	5	5	ns typ	t_{ON}–t_{OFF1}; Test Circuit 4
Output Settling Time to 0.1%	All	180	–	ns typ	V_{IN} = 3V to 0V; Test Circuit 4
OFF Isolation	All	72	–	dB typ	V_S = 3V rms, f = 100kHz, R_L = 1kΩ; C_L = 10pF; Test Circuit 5
Channel-to-Channel Crosstalk	All	86	–	dB typ	V_S = 3V rms, f = 100kHz, R_L = 1kΩ; C_L = 10pF; Test Circuit 6
Q_{INJ}, Charge Injection	All	10	–	pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 7
C_S (OFF)	All	10	–	pF typ	
C_D (OFF)	All	10	–	pF typ	
C_D, C_S (ON)	All	30	–	pF typ	
C_{DS} (OFF)	All	0.5	–	pF typ	
POWER SUPPLY					
I_{DD}	All	10	10	mA max	
I_{SS}	All	6	6	mA max	
Power Dissipation	All	240	240	mW max	V_{DD} = +15V, V_{SS} = −15V

NOTES

[1]Temperature ranges are as follows: ADG201HSJ, K; −40°C to +85°C
ADG201HSA, B; −40°C to +85°C
ADG201HSS, T; −55°C to +125°C

[2]Leakage specifications apply with a V_D (V_S) of ±14V or with a V_D (V_S) of 0.5V within the supply voltages (V_{DD}, V_{SS}), whichever is the minimum.

Specifications subject to change without notice.

Single Supply (V_{DD} = +10.8V to +16.5V, V_{SS} = GND = 0V, V_{IN} = 3V [Logic High Level] or 0.8V [Logic Low Level] unless otherwise noted)

Parameter	Version	+25°C	T_{min}–T_{max}	Units	Comments
ANALOG SWITCH					
Analog Signal Range	All	V_{SS}	V_{SS}	Vmin	
	All	V_{DD}	V_{DD}	V max	
R_{ON}	All	65	–	Ω typ	$0V \leq V_S \leq +10V$, I_{DS} = 1mA; Test Circuit 1
	All	90	120	Ω max	
R_{ON} Drift	All	0.5	–	%/°C typ	$0V \leq V_S \leq +10V$, I_{DS} = 1mA
R_{ON} Match	All	3	–	% typ	$0V \leq V_S \leq +10V$, I_{DS} = 1mA
I_S (OFF), Off Input Leakage[1]	All	0.1		nA typ	V_D = +10V/+0.5V; V_S = +0.5V/+10V; Test Circuit 2
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
I_D (OFF), Off Output Leakage[1]	All	0.1		nA typ	V_D = +10V/+0.5V; V_S = +0.5V/+10V; Test Circuit 2
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
I_D (ON), On Channel Leakage[1]	All	0.1		nA typ	V_D = +10V/+0.5V; Test Circuit 3
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
DIGITAL CONTROL					
V_{INH}, Input High Voltage	All	2.4	2.4	V min	
V_{INL}, Input Low Voltage	All	0.8	0.8	V max	
I_{INL} or I_{INH}	All	1	1	μA max	
C_{IN}	All	8	8	pF max	
DYNAMIC CHARACTERISTICS					
t_{ON}	K, B, T	50	70	ns max	Test Circuit 4
	J, A, S	75	90	ns max	
t_{OFF1}	K, B, T	50	70	ns max	Test Circuit 4
	J, A, S	75	90	ns max	
t_{OFF2}	All	150	–	ns typ	Test Circuit 4
t_{OPEN}	All	5	5	ns typ	t_{ON}–t_{OFF1}; Test Circuit 4
Output Settling Time to 0.1%	All	180	–	ns typ	V_{IN} = 3V to 0V; Test Circuit 4
OFF Isolation	All	72	–	dB typ	V_S = 3V rms, f = 100kHz, R_L = 1kΩ; C_L = 10pF; Test Circuit 5
Channel-to-Channel Crosstalk	All	86	–	dB typ	V_S = 3V rms, f = 100kHz, R_L = 1kΩ; C_L = 10pF; Test Circuit 6
Q_{INJ}, Charge Injection	All	10	–	pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 7
C_S (OFF)	All	10	–	pF typ	
C_D (OFF)	All	10	–	pF typ	
C_D, C_S (ON)	All	30	–	pF typ	
C_{DS} (OFF)	All	0.5	–	pF typ	
POWER SUPPLY					
I_{DD}	All	10	10	mA max	
Power Dissipation	All	150	150	mW max	V_{DD} = +15V

NOTE
[1]The leakage specifications degrade marginally (typically 1nA at 25°C) with V_D (V_S) = V_{SS}.
Specifications subject to change without notice.

5

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C unless otherwise noted)

V_{DD} to V_{SS}	44V
V_{DD} to GND	−0.3V, 25V
V_{SS} to GND[1]	+0.3V, −25V
Analog Inputs[2]	
Voltage at S, D	V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First
Continuous Current, S or D	20mA
Pulsed Current S or D	
1ms Duration, 10% Duty Cycle	70mA
Digital Inputs[2]	
Voltage at IN	V_{SS} −4V to V_{DD} +4V or 20mA, Whichever Occurs First
Power Dissipation (Any Package)	
Up to +75°C	470mW
Derates above +75°C by	6mW/°C
Operating Temperature	
Commerical (J, K Version)	−40°C to +85°C
Industrial (A, B Version)	−40°C to +85°C
Extended (S, T Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

NOTES
[1]If V_{SS} is open circuited with V_{DD} and GND applied, the V_{SS} pin will be pulled positive, exceeding the Absolute Maximum Ratings. If this possibility exists, a Schottky diode from V_{SS} to GND (cathode end to GND) ensures that the Absolute Maximum Ratings will be observed.
[2]Overvoltage at IN, S or D, will be clamped by diodes. Current should be limited to the maximum rating above.

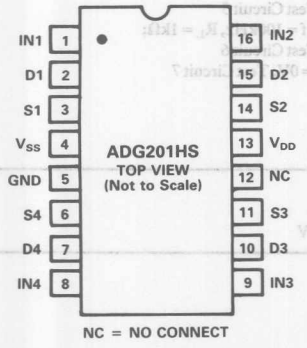
*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

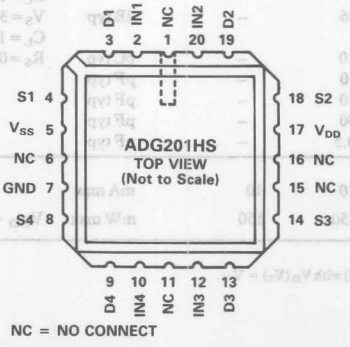


PIN CONFIGURATIONS

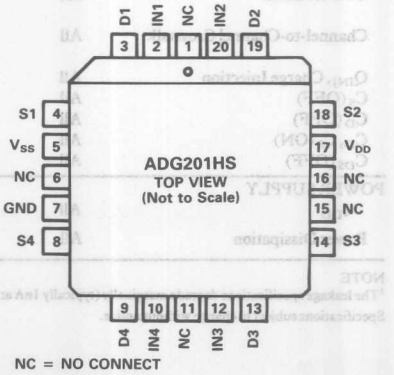
DIP, SOIC



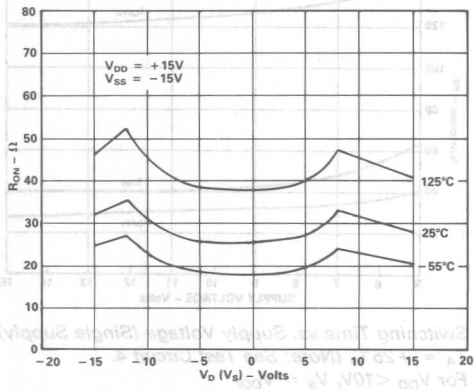
LCCC



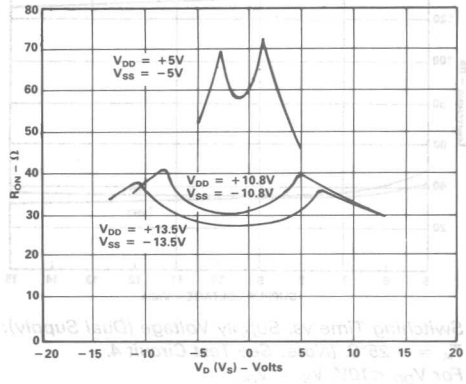
PLCC



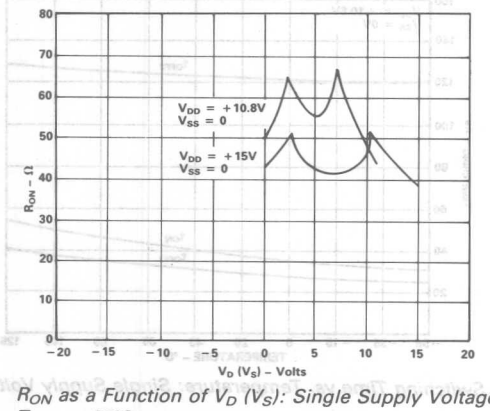
The switches are guaranteed functional with reduced single or dual supplies down to 4.5V.



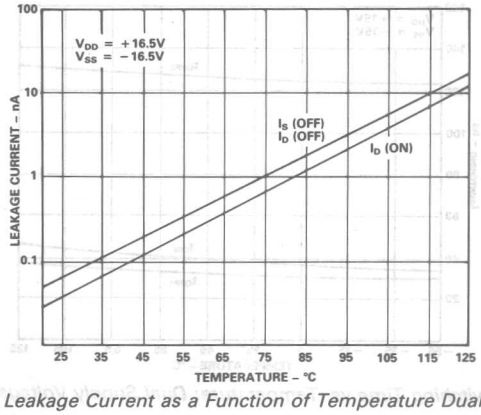
R_{ON} as a Function of V_D (V_S): Dual Supply Voltage



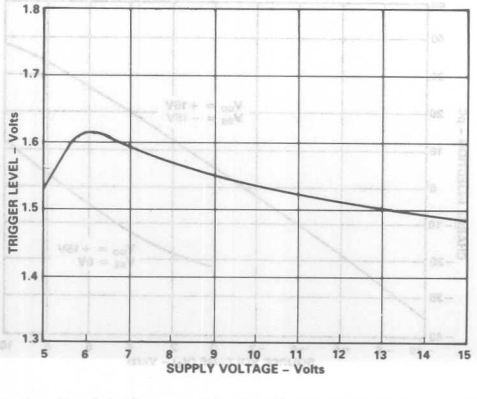
R_{ON} as a Function of V_D (V_S): Dual Supply Voltage, T_A = +25°C



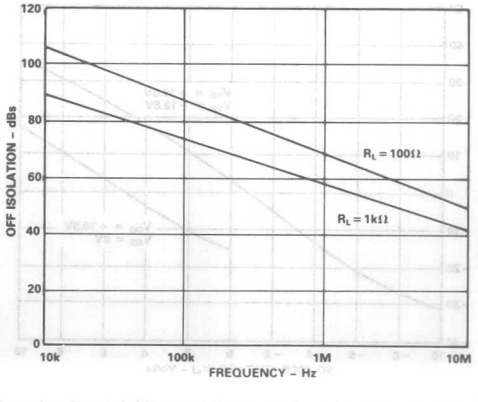
R_{ON} as a Function of V_D (V_S): Single Supply Voltage, T_A = +25°C



Leakage Current as a Function of Temperature Dual Supply Voltage. (Note: Leakage Currents Reduce as the Supply Voltages Reduce)

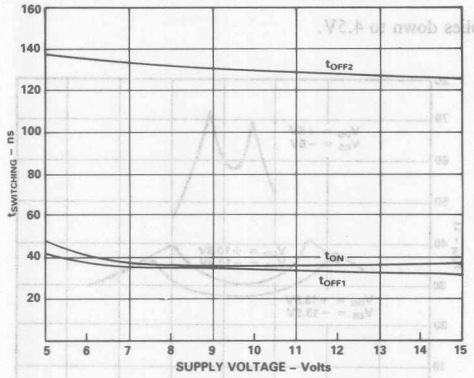


Trigger Levels vs. Power Supply Voltage, Dual or Single Supply, T_A = +25°C

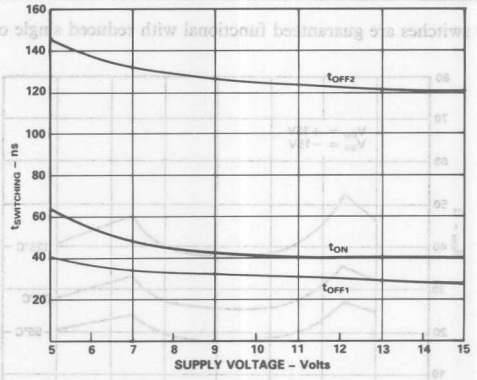


Off Isolation vs. Signal Frequency; Dual or Single 15V Supplies, T_A = +25°C

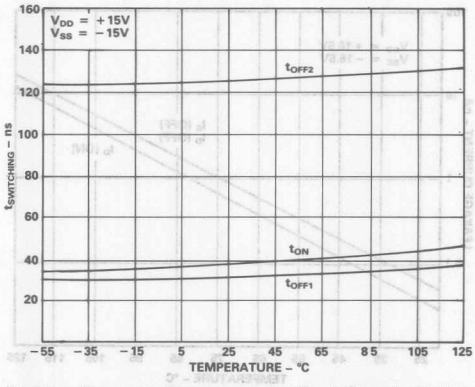
ADG201HS—Typical Performance Characteristics (Continued)



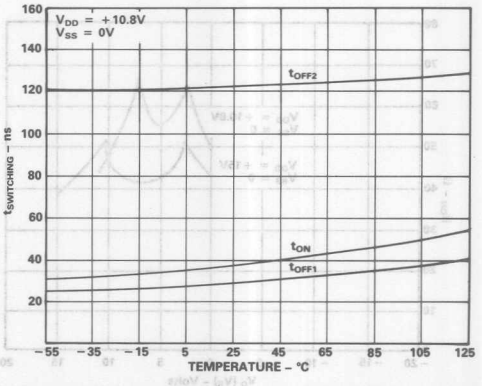
Switching Time vs. Supply Voltage (Dual Supply): T_A = +25°C. (Note: See Test Circuit 4. For V_{DD} <10V, V_S = V_{DD})



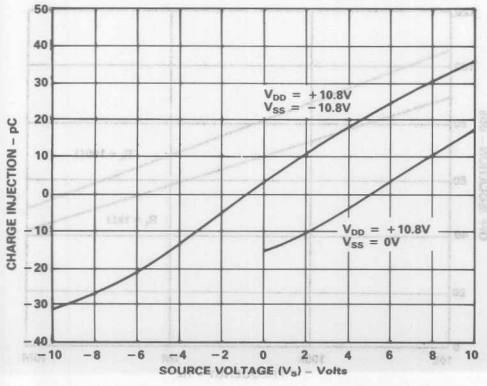
Switching Time vs. Supply Voltage (Single Supply): T_A = +25°C. (Note: See Test Circuit 4. For V_{DD} <10V, V_S = V_{DD})



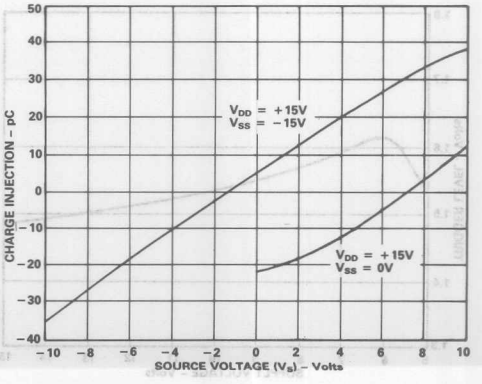
Switching Time vs. Temperature: Dual Supply Voltage



Switching Time vs. Temperature: Single Supply Voltage



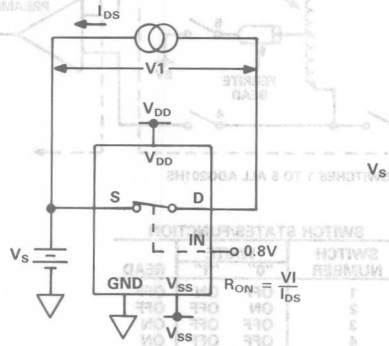
Charge Injection vs. Source Voltage (V_S) for Dual and Single 10.8V Supplies: T_A = +25°C



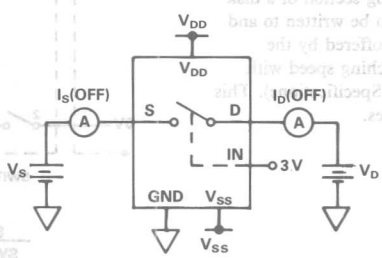
Charge Injection vs. Source Voltage (V_S) for Dual and Single 15V Supplies: T_A = +25°C

Note: All digital input signal rise and fall times measured from 10% to 90% of 3V. $t_R = t_F = 5ns$. Decoupling capacitors (0.01μF min) from V_{DD} and V_{SS} to GND are recommended to achieve specified performance.

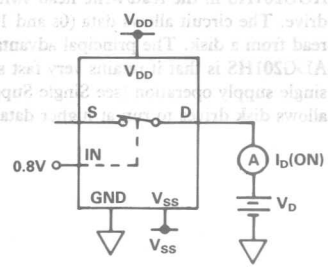
TEST CIRCUIT 1
R_{ON}



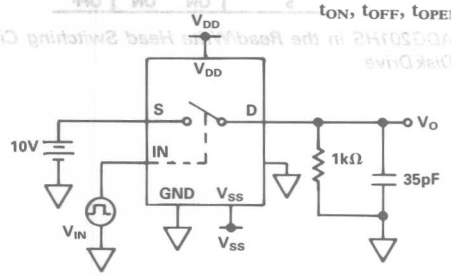
TEST CIRCUIT 2
I_S(OFF), I_D(OFF)

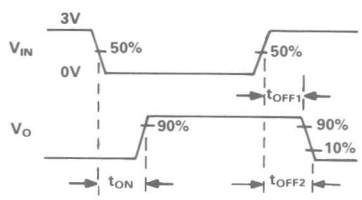


TEST CIRCUIT 3
I_D(ON)

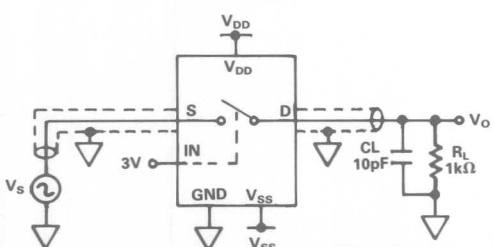


TEST CIRCUIT 4
t_{ON}, t_{OFF}, t_{OPEN}, SETTLING TIME



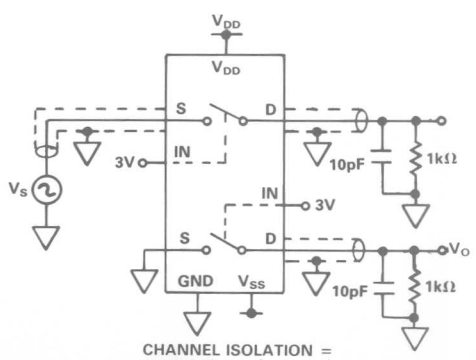


TEST CIRCUIT 5
OFF ISOLATION



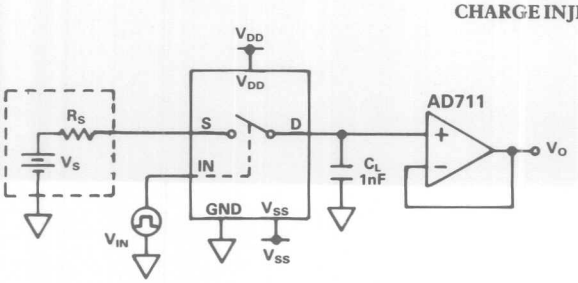
OFF ISOLATION =
$20 \times LOG|V_S/V_O|$

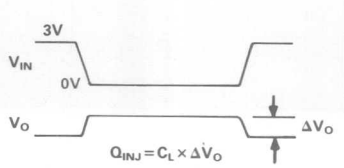
TEST CIRCUIT 6
CHANNEL-TO-CHANNEL CROSSTALK



CHANNEL ISOLATION =
$20 \times LOG|V_S/V_O|$

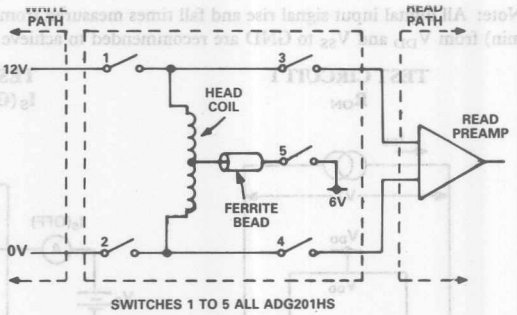
TEST CIRCUIT 7
CHARGE INJECTION





SINGLE SUPPLY DISK DRIVE APPLICATION

The excellent performance of the ADG201HS with single supply operation makes it suitable in applications such as disk drives where only positive power supply voltages are normally available. The accompanying circuit shows a typical application for the ADG201HS in the read/write head switching section of a disk drive. The circuit allows data (0s and 1s) to be written to and read from a disk. The principal advantage offered by the ADG201HS is that it retains very fast switching speed with single supply operation (see Single Supply Specifications). This allows disk drives to run at higher data rates.



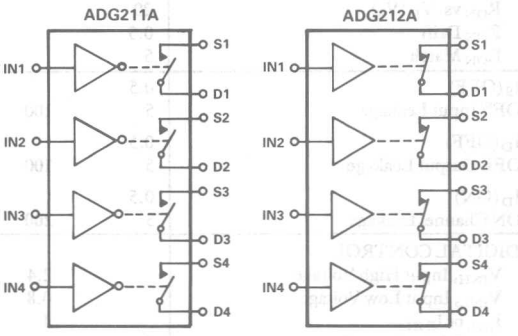
SWITCH STATES/FUNCTION

SWITCH NUMBER	WRITE "0"	WRITE "1"	READ
1	OFF	ON	OFF
2	ON	OFF	OFF
3	OFF	OFF	ON
4	OFF	OFF	ON
5	ON	ON	OFF

ADG201HS in the Read/Write Head Switching Circuit of a Disk Drive

ADG211A/ADG212A

FEATURES
44V Supply Maximum Rating
±15V Analog Signal Range
Low R_{ON} (115Ω max)
Low Leakage (0.5nA typ)
Break Before Make Switching
Single Supply Operation Possible
Extended Plastic Temperature Range (−40°C to +85°C)
TTL/CMOS Compatible
Available in 16-Lead DIP/SOIC and 20-Lead PLCC Packages
Superior Second Source:
ADG211A Replaces DG211
ADG212A Replaces DG212



SWITCHES SHOWN FOR A LOGIC "1" INPUT

5

GENERAL DESCRIPTION

The ADG211A and ADG212A are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC^2MOS process which gives an increased signal handling capability of ±15V. These switches also feature high switching speeds and low R_{ON}.

The ADG211A and ADG212A consist of four SPST switches. They differ only in that the digital control logic is inverted. In multiplexer applications, all switches exhibit break-before-make switching action when driven simultaneously. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended Signal Range:
   These switches are fabricated on an enhanced LC^2MOS process, resulting in high breakdown and an increased analog signal range of ±15V.
2. Single Supply Operation:
   For applications where the analog signal is unipolar (0V to 15V), the switches can be operated from a single +15V supply.
3. Low Leakage:
   Leakage currents in the range of 500pA make these switches suitable for high precision circuits. The added feature of Break before Make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

ADG211A IN	ADG212A IN	SWITCH CONDITION
0	1	ON
1	0	OFF

Table I. Truth Table

ADG211A/ADG212A—SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V, V_L = 5V, unless otherwise noted.)

	ADG211AKN ADG212AKN			
Parameter	**25°C**	**−40°C to +85°C**	**Units**	**Test Conditions**
ANALOG SWITCH				
Analog Signal Range	± 15	± 15	Volts	
R_{ON}	115	175	Ωmax	$-10V \leq V_S \leq +10V$, I_{DS} = 1mA, Test Circuit 1
R_{ON} vs. V_D (V_S)	20		% typ	
R_{ON} Drift	0.5		%/°C typ	
R_{ON} Match	5		% typ	V_S = 0V, I_{DS} = 1mA
I_S (OFF)	0.5		nA typ	$V_D = \pm 14V$; $V_S \mp 14V$; Test Circuit 2
OFF Input Leakage	5	100	nA max	
I_D (OFF)	0.5		nA typ	$V_D = \pm 14V$; $V_S = \mp 14V$; Test Circuit 2
OFF Output Leakage	5	100	nA max	
I_D (ON)	0.5		nA typ	$V_D = \pm 14V$; Test Circuit 3
ON Channel Leakage	5	200	nA max	
DIGITAL CONTROL				
V_{INH}, Input High Voltage		2.4	V min	TTL Compatibility is Independent of V_L
V_{INL}, Input Low Voltage		0.8	V max	
I_{INL} or I_{INH}		1	μA max	
C_{IN}, Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS				
t_{OPEN}[1]	30		ns typ	Test Circuit 4
t_{ON}[1]	600		ns max	Test Circuit 5
t_{OFF}[1]	450		ns max	Test Circuit 5
OFF Isolation	80		dB typ	V_S = 10V(p-p); f = 100kHz R_L = 75Ω; Test Circuit 6
Channel-to-Channel Crosstalk	80		dB typ	Test Circuit 7
C_S (OFF)	5		pF typ	
C_D (OFF)	5		pF typ	
C_S, C_D (ON)	16		pF typ	
Q_{INJ}, Charge Injection	20		pC typ	R_S = 0Ω; C_L = 1000pF; V_S = 0V Test Circuit 8
POWER SUPPLY				
I_{DD}	0.6		mA typ	Digital Inputs = V_{INL} or V_{INH}
I_{DD}	1		mA max	
I_{SS}	0.1		mA typ	
I_{SS}	0.2		mA max	
I_L	0.9		mA max	

NOTE
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise stated)

V_{DD} to V_{SS}	44V
V_{DD} to GND	25V
V_{SS} to GND	−25V
V_L to GND	−0.3V, 25V
Analog Inputs[1]	
Voltage at S, D	V_{SS} −0.3V to V_{DD} +0.3V
Continuous Current, S or D	30mA
Pulsed Current S or D	
1ms Duration, 10% Duty Cycle	70mA
Digital Inputs[1]	
Voltage at IN	V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First
Power Dissipation (Any Package)	
Up to +75°C	470mW
Derates above +75°C by	6mW/°C
Operating Temperature	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

NOTE
[1]Overvoltage at IN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

CAUTION

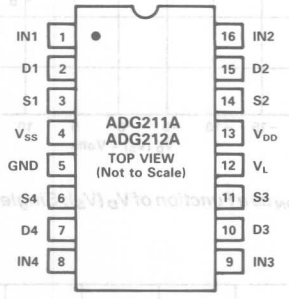
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



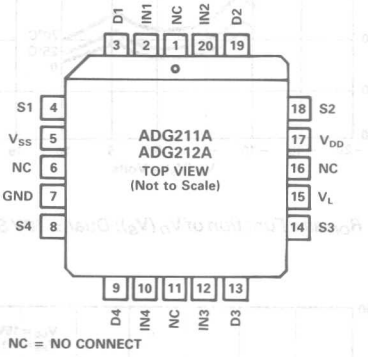
5

PIN CONFIGURATIONS

DIP, SOIC



PLCC



NC = NO CONNECT

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG211AKN	−40°C to +85°C	N-16
ADG211AKR	−40°C to +85°C	R-16A
ADG211AKP	−40°C to +85°C	P-20A
ADG212AKN	−40°C to +85°C	N-16
ADG212AKR	−40°C to +85°C	R-16A
ADG212AKP	−40°C to +85°C	P-20A

*N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); P = Plastic Leaded Chip Carrier (PLCC). For outline information see Package Information section.

ADG211A/ADG212A—Typical Performance Characteristics

The switches can comfortably operate anywhere in the 10V to 15V single or dual supply range, with only a slight degradation in performance. The following graphs show the relevant performance curves. The test circuits and test conditions are given in a following section, "Test Circuits."

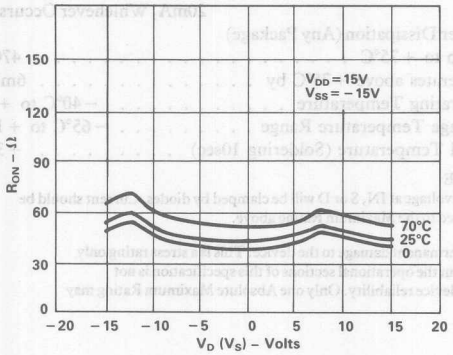


Figure 1. R_{ON} as a Function of V_D (V_S): Dual ± 15 Supplies

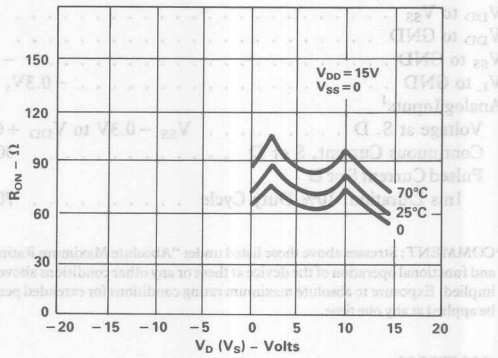


Figure 2. R_{ON} as a Function of V_D (V_S): Single + 15V Supply

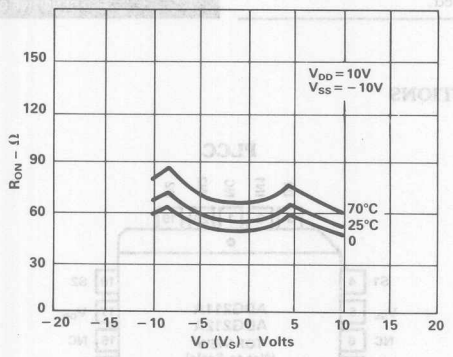


Figure 3. R_{ON} as a Function of V_D (V_S): Dual ± 10V Supplies

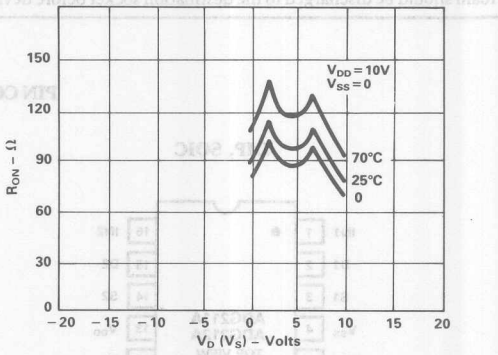


Figure 4. R_{ON} as a Function of V_D (V_S): Single + 10V Supply

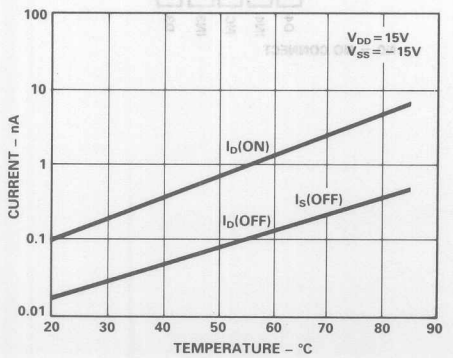


Figure 5. Leakage Current as a Function of Temperature (Note: Leakage Current Reduces as the Supply Voltages Reduce)

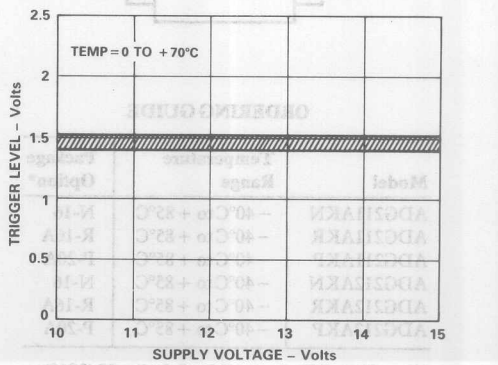


Figure 6. Trigger Levels vs. Power Supply Voltage, Dual or Single Supply Voltage

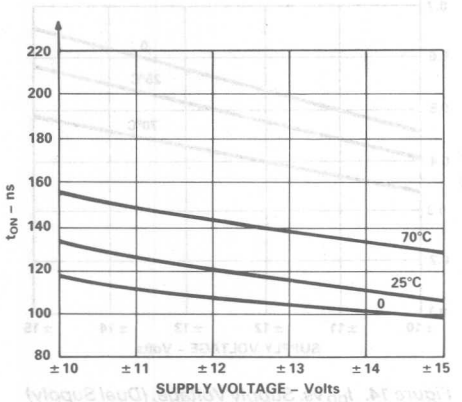


Figure 7. t_{ON} vs. Supply Voltage, (Dual Supply)

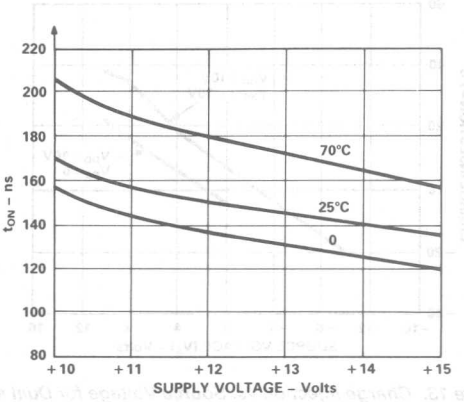


Figure 8. t_{ON} vs. Supply Voltage, (Single Supply)

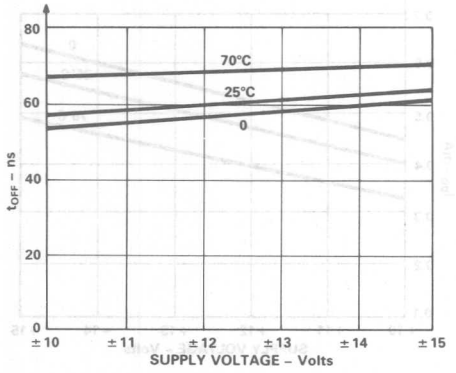


Figure 9. t_{OFF} vs. Supply Voltage, (Dual Supply)

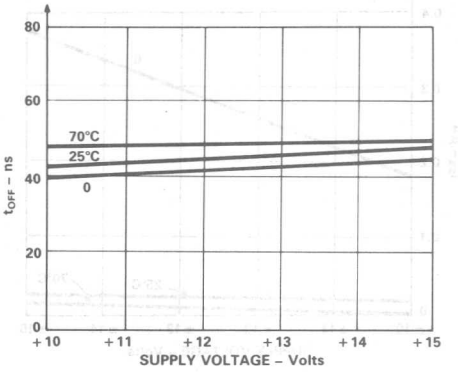


Figure 10. t_{OFF} vs. Supply Voltage, (Single Supply)

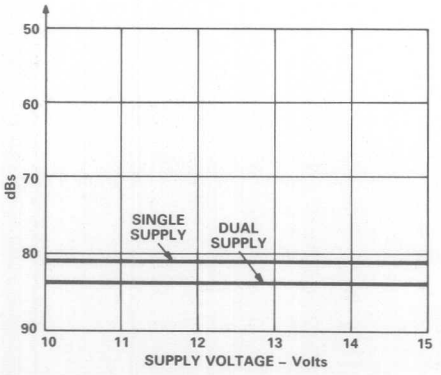


Figure 11. Off Isolation and Channel-to-Channel Crosstalk vs. Supply Voltage

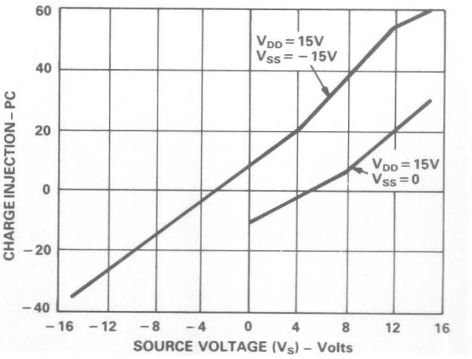


Figure 12. Charge Injection vs. Source Voltage (V_S) for Dual and Single 15V Supplies

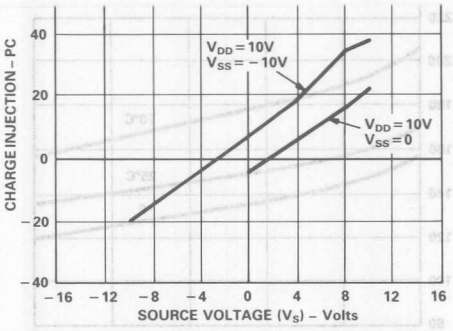


Figure 13. Charge Injection vs. Source Voltage for Dual and Single 10V Supplies

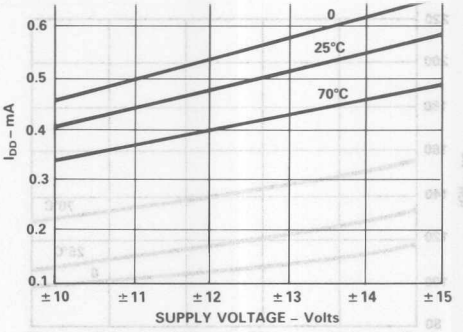


Figure 14. I_{DD} vs. Supply Voltage, (Dual Supply)

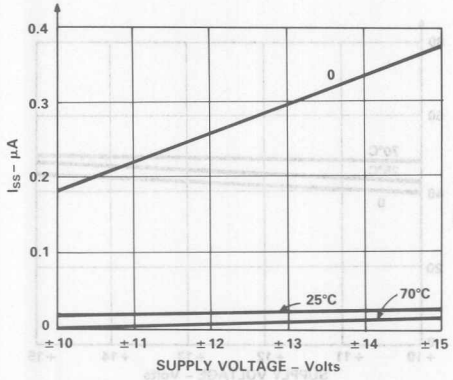


Figure 15. I_{SS} vs. Supply Voltage, (Dual Supply)

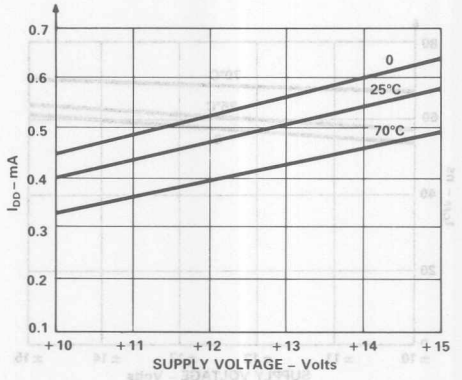
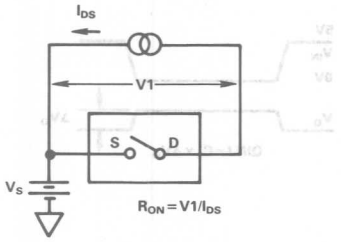
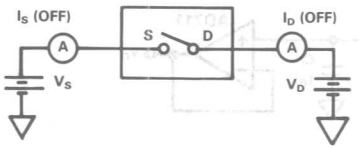


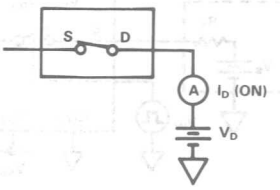
Figure 16. I_{DD} vs. Supply Voltage, (Single Supply)



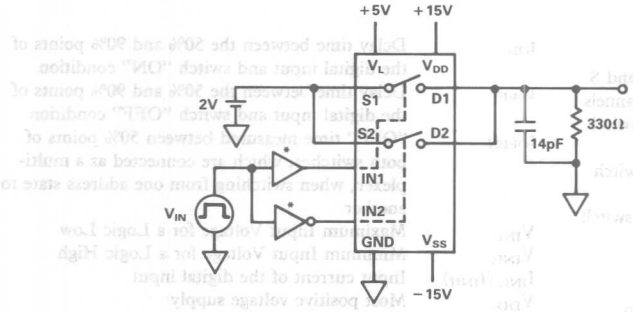
Test Circuit 1

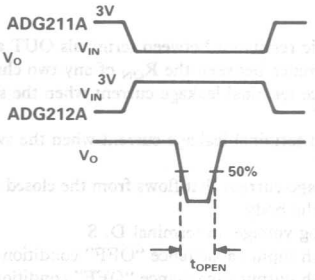


Test Circuit 2

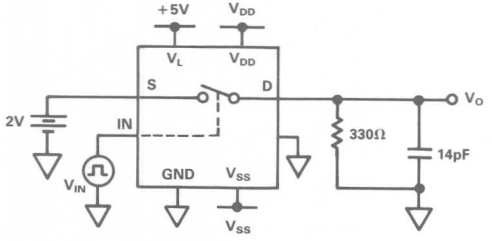


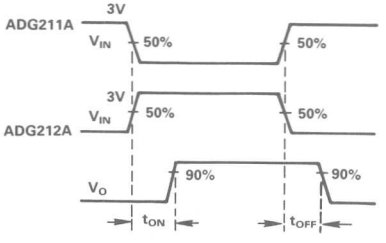
Test Circuit 3



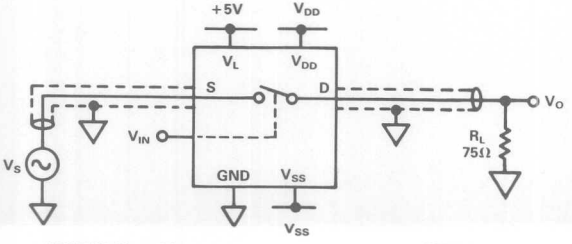


Test Circuit 4

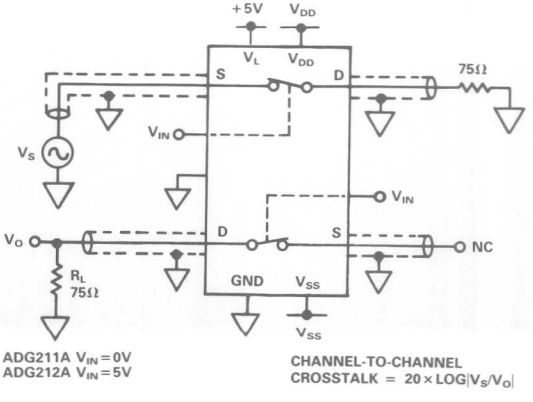




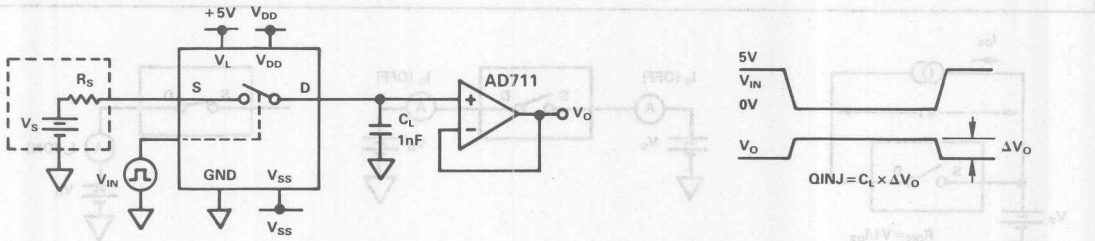
Test Circuit 5



Test Circuit 6. Off Isolation



Test Circuit 7. Channel-to-Channel Crosstalk



Test Circuit 8. Charge Injection

TERMINOLOGY

R_{ON}	Ohmic resistance between terminals OUT and S
R_{ON} Match	Difference between the R_{ON} of any two channels
I_S (OFF)	Source terminal leakage current when the switch is off
I_D (OFF)	Drain terminal leakage current when the switch is off
I_D (ON)	Leakage current that flows from the closed switch into the body
V_D (V_S)	Analog voltage on terminal D, S
C_S (OFF)	Switch input capacitance "OFF" condition
C_D (OFF)	Switch output capacitance "OFF" condition
C_{IN}	Digital input capacitance
C_D, C_S (ON)	Input or output capacitance when the switch is on
t_{ON}	Delay time between the 50% and 90% points of the digital input and switch "ON" condition
t_{OFF}	Delay time between the 50% and 90% points of the digital input and switch "OFF" condition
t_{OPEN}	"OFF" time measured between 50% points of both switches, which are connected as a multiplexer, when switching from one address state to another
V_{INL}	Maximum Input Voltage for a Logic Low
V_{INH}	Minimum Input Voltage for a Logic High
I_{INL} (I_{INH})	Input current of the digital input
V_{DD}	Most positive voltage supply
V_{SS}	Most negative voltage supply
V_L	Logic supply voltage
I_{DD}	Positive supply current
I_{SS}	Negative supply current

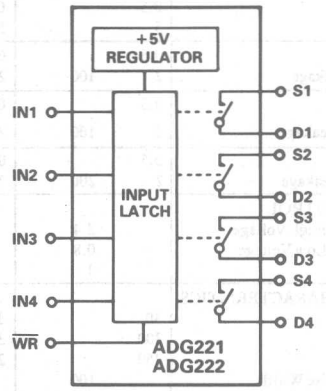
LC²MOS Quad SPST Switches

ADG221/ADG222

FEATURES

- 44V Supply Maximum Rating
- ±15V Analog Signal Range
- Low R_{ON} (60Ω)
- Low Leakage (0.5nA)
- Break Before Make Switching
- Extended Plastic Temperature Range (−40°C to +85°C)
- Low Power Dissipation (25.5mW)
- µP, TTL, CMOS Compatible
- Available in 16-Lead DIP/SOIC and 20-Lead PLCC/LCCC Packages
- Surface Mount Packages
- Superior DG221 Replacement

FUNCTIONAL BLOCK DIAGRAM



5

GENERAL DESCRIPTION

The ADG221 and ADG222 are monolithic CMOS devices comprising four independently selectable switches. On-chip latches facilitate microprocessor interfacing. They are designed on an enhanced LC²MOS process which gives an increased signal handling capability of ±15V. These switches also feature high switching speeds and low R_{ON}.

The ADG221 and ADG222 consist of four SPST switches. They differ only in that the digital control logic is inverted. All devices exhibit break before make switching action. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Easily Interfaced:
   Digital inputs are latched with a $\overline{WR}$ signal for microprocessor interfacing. A 5V regulated supply is internally generated permitting wider tolerances on the supplies without affecting the TTL digital input switching levels.
2. Single Supply Operation:
   For applications where the analog signal is unipolar (0V to 15V), the switches can be operated from a single +15V supply.
3. Low Leakage:
   Leakage currents in the range of 500pA make these switches suitable for high precision circuits. The added feature of Break before Make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

ADG221/ADG222—SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V, unless otherwise specified)

Parameter	K Version 25°C	K Version −40°C to +85°C	B Version 25°C	B Version −40°C to +85°C	T Version 25°C	T Version −55°C to +125°C	Units	Test Conditions
ANALOG SWITCH								
Analog Signal Range	± 15	± 15	± 15	± 15	± 15	± 15	Volts	
R_{ON}	60		60		60		Ω typ	$-10V \le V_S \le +10V$
	90	145	90	145	90	145	Ω max	I_{DS} = 1.0mA
								Test Circuit 1
R_{ON} vs. V_D (V_S)	20		20		20		% typ	
R_{ON} Drift	0.5		0.5		0.5		%/°C typ	
R_{ON} Match	5		5		5		% typ	V_S = 0V, I_{DS} = 1mA
I_S (OFF)	0.5		0.5		0.5		nA typ	V_D = ± 14V; V_S ∓ 14V; Test Circuit 2
OFF Input Leakage	2	100	2	100	1	100	nA max	
I_D (OFF)	0.5		0.5		0.5		nA typ	V_D = ± 14V; V_S = ∓ 14V; Test Circuit 2
OFF Output Leakage	2	100	2	100	1	100	nA max	
I_D (ON)	0.5		0.5		0.5		nA typ	V_D = ± 14V; Test Circuit 3
ON Channel Leakage	2	200	2	200	1	200	nA max	
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	
DYNAMIC CHARACTERISTICS								
t_{OPEN}	30		30		30		ns typ	
t_{ON}[1]	300		300		300		ns max	Test Circuit 4
t_{OFF}[1]	250		250		250		ns max	Test Circuit 4
t_W[1] Write Pulse Width		100		100	100	120	ns min	See Figure 2
t_S[1] Digital Input Setup Time		100		100	100	120	ns min	See Figure 2
t_H[1] Digital Input Hold Time		20		20	20	20	ns min	See Figure 2
OFF Isolation	80		80		80		dB typ	V_S = 10V (p-p); f = 100kHz
								R_L = 75Ω; Test Circuit 6
Channel-to-Channel Crosstalk	80		80		80		dB typ	Test Circuit 7
C_S (OFF)	5		5		5		pF typ	
C_D (OFF)	5		5		5		pF typ	
C_D, C_S (ON)	16		16		16		pF typ	
C_{IN} Digital Input Capacitance	5		5		5		pF typ	
Q_{INJ} Charge Injection	20		20		20		pC typ	R_S = 0Ω; C_L = 1000pF; V_S = 0V
								Test Circuit 5
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	Digital Inputs = V_{INL} or V_{INH}
I_{DD}		1.5		1.5		1.5	mA max	
I_{SS}	0.1		0.1		0.1		mA typ	
I_{SS}		0.2		0.2		0.2	mA max	
Power Dissipation		25.5		25.5		25.5	mW max	

NOTE
[1]Sample tested at 25°C to ensure compliance.
t_{ON}, t_{OFF} are the same for both IN and $\overline{WR}$ digital input changes.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} to V_{SS} 44V
V_{DD} to GND 25V
V_{SS} to GND . . . . . −25V
Analog Inputs[1]
  Voltage at S, D . . . . . V_{SS} −0.3V to V_{DD} +0.3V
  Continuous Current, S or D 30mA
  Pulsed Current S or D
    1ms Duration, 10% Duty Cycle 70mA
Digital Inputs[1]
  Voltage at IN, $\overline{WR}$ . . . . . V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First

Power Dissipation (Any Package)
  Up to +75°C 470mW
  Derates above +75°C by . . . . . 6mW/°C
Operating Temperature
  Commercial (K Version) . . . . . −40°C to +85°C
  Industrial (B Version) . . . . . −40°C to +85°C
  Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +300°C

NOTE
[1]Overvoltage at IN, $\overline{WR}$, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG221KN	−40°C to +85°C	N-16
ADG221KR	−40°C to +85°C	R-16A
ADG221KP	−40°C to +85°C	P-20A
ADG221BQ	−40°C to +85°C	Q-16
ADG221TQ	−55°C to +125°C	Q-16
ADG221TE	−55°C to +125°C	E-20A
ADG222KN	−40°C to +85°C	N-16
ADG222KR	−40°C to +85°C	R-16A
ADG222KP	−40°C to +85°C	P-20A
ADG222BQ	−40°C to +85°C	Q-16
ADG222TQ	−55°C to +125°C	Q-16
ADG222TE	−55°C to +125°C	E-20A

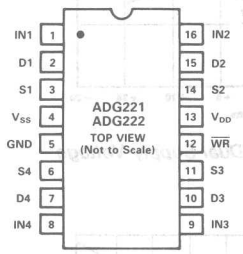
NOTES

[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers. See Analog Devices Military Products Databook (1990) for military data sheet.

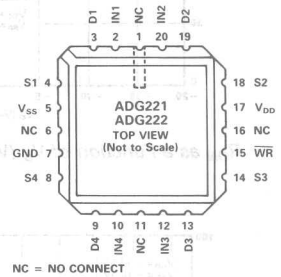
[2]N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; E = Leadless Ceramic Chip Carrier (LCCC). For outline information see Package Information section.

PIN CONFIGURATIONS

DIP, SOIC

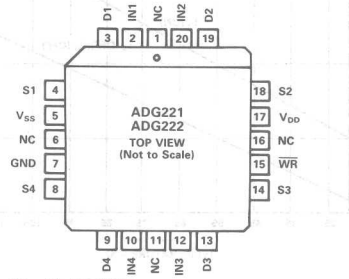


LCCC



NC = NO CONNECT

PLCC



NC = NO CONNECT

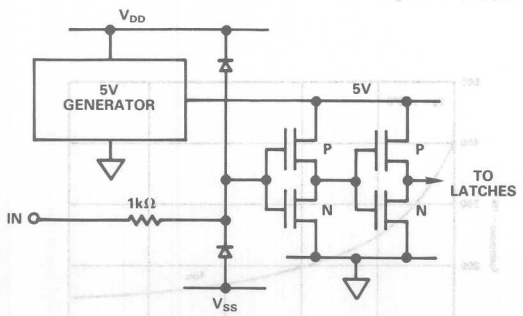


Figure 1. Typical Digital Input Cell

TIMING AND CONTROL SEQUENCE

Figure 2 shows the timing sequence for latching the switch digital inputs (IN1 – IN4). The latches are level sensitive and, therefore, while $\overline{WR}$ is held low the latches are transparent and the switches respond to the digital inputs. The digital inputs are latched on the rising edge of $\overline{WR}$.

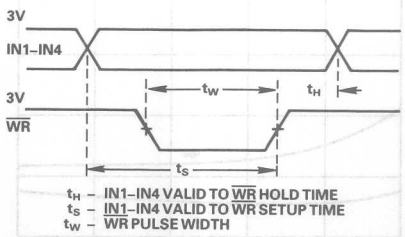
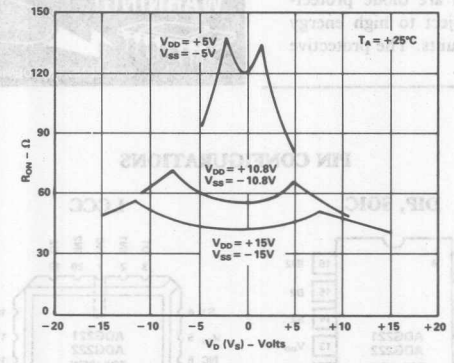


Figure 2. Timing and Control Sequence

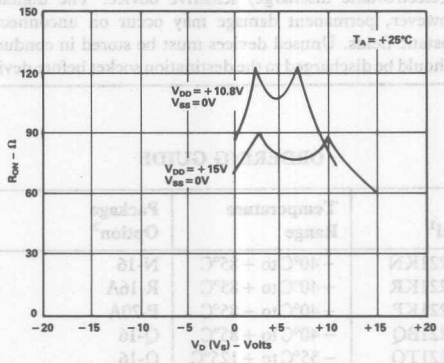
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ADG221/ADG222—Typical Performance Characteristics

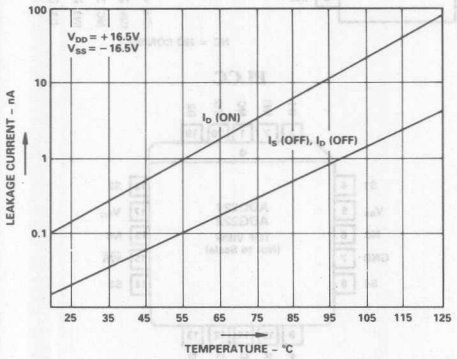
The switches are guaranteed functional with reduced single or dual supplies down to 4.5V.



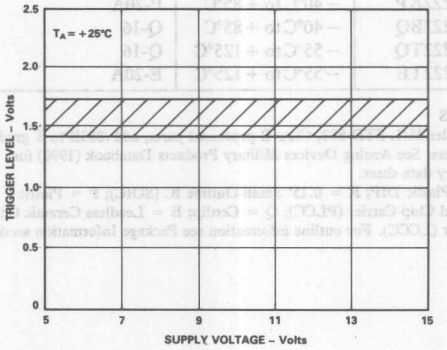
R_{ON} as a Function of V_D (V_S): Dual Supply Voltage



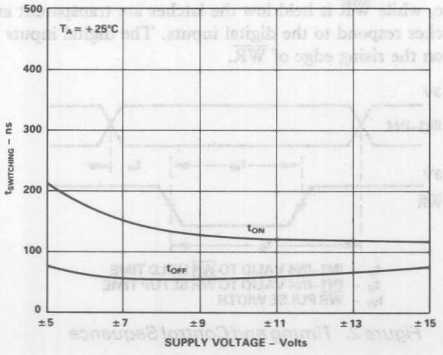
R_{ON} as a Function of V_D (V_S): Single Supply Voltage



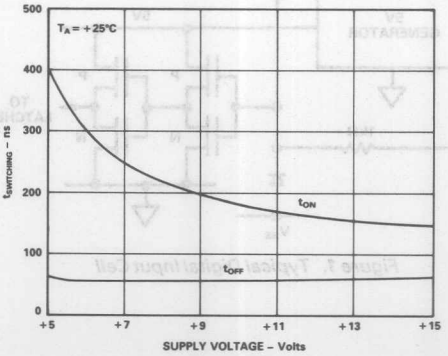
Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)



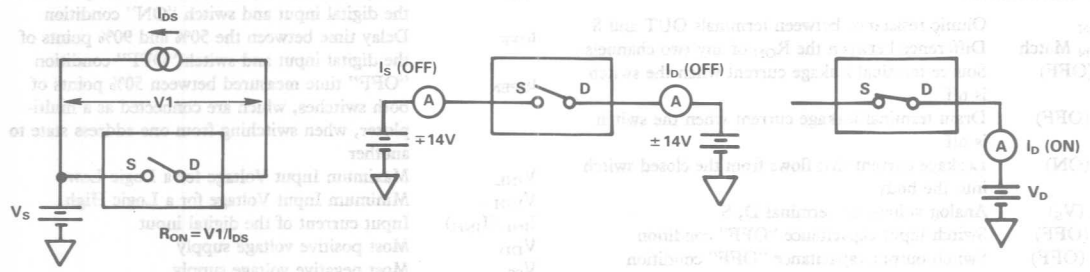
Trigger Level vs. Power Supply Voltage: Dual or Single Supply Voltage



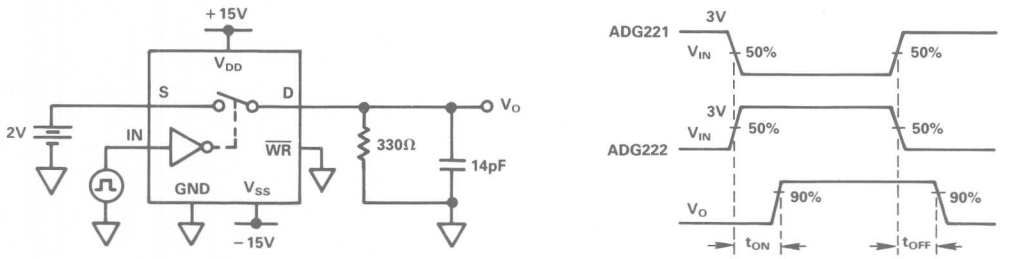
Switching Times vs. Supply Voltage (Dual Supply)



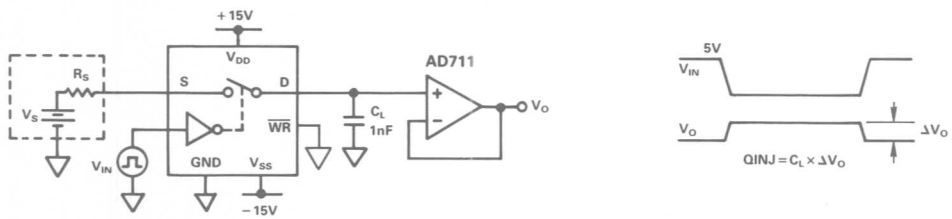
Switching Times vs. Supply Voltage (Single Supply)



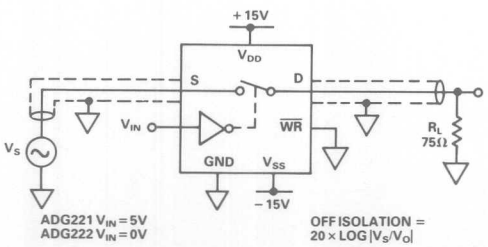
Test Circuit 1 *Test Circuit 2* *Test Circuit 3*



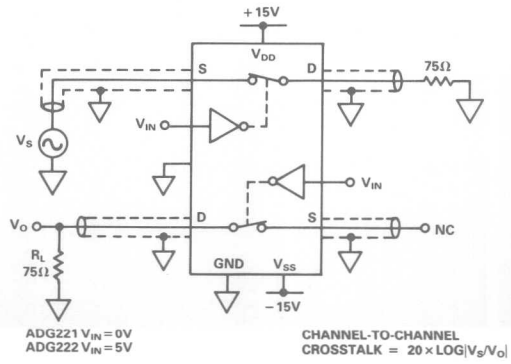
Test Circuit 4



Test Circuit 5. Charge Injection



Test Circuit 6. Off Isolation



Test Circuit 7. Channel-to-Channel Crosstalk

R_{ON}	Ohmic resistance between terminals OUT and S
R_{ON} Match	Difference between the R_{ON} of any two channels
I_S (OFF)	Source terminal leakage current when the switch is off
I_D (OFF)	Drain terminal leakage current when the switch is off
I_D (ON)	Leakage current that flows from the closed switch into the body
V_D (V_S)	Analog voltage on terminal D, S
C_S (OFF)	Switch input capacitance "OFF" condition
C_D (OFF)	Switch output capacitance "OFF" condition
C_{IN}	Digital input capacitance
C_D, C_S (ON)	Input or output capacitance when the switch is on
t_{OFF}	Delay time between the 50% and 90% points of the digital input and switch "OFF" condition
t_{OPEN}	"OFF" time measured between 50% points of both switches, which are connected as a multiplexer, when switching from one address state to another
V_{INL}	Maximum Input Voltage for a Logic Low
V_{INH}	Minimum Input Voltage for a Logic High
I_{INL} (I_{INH})	Input current of the digital input
V_{DD}	Most positive voltage supply
V_{SS}	Most negative voltage supply
I_{DD}	Positive supply current
I_{SS}	Negative supply current

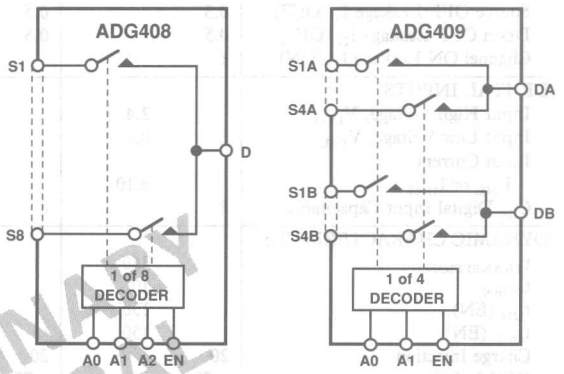
LC²MOS 4/8 Channel High Performance Analog Multiplexers

ADG408/ADG409

FEATURES
- 44 V Supply Maximum Ratings
- V_{SS} to V_{DD} Analog Signal Range
- Low On Resistance (<100 Ω)
- Low Power Dissipation (<2.2 mW)
- Fast Switching
- Latch Up Proof
- Plug-In Replacement for DG408/DG409

APPLICATIONS
- Audio and Video Routing
- Automatic Test Equipment
- Data Acquisition Systems
- Battery Powered Systems
- Sample Hold Systems
- Communication Systems

FUNCTIONAL BLOCK DIAGRAMS



PRELIMINARY TECHNICAL DATA

5

GENERAL DESCRIPTION

The ADG408 and ADG409 are monolithic CMOS analog multiplexers comprising 8 single channels and 4 differential channels, respectively. The ADG408 switches one of 8 inputs to a common output as determined by the 3 bit binary address lines A0, A1, A2. The ADG409 switches one of 4 differential inputs to a common differential output as determined by the 2 bit binary address lines A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched OFF.

The ADG408/ADG409 are designed on an enhanced LC²MOS, trench isolated process which provides low power dissipation yet gives high switching speed and low on resistance. Each channel conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition signal levels up to the supplies are blocked. All channels exhibit break-before-make switching action preventing momentary shorting when switching channels. Trench isolation gives all the benefits of dielectric isolation and ensures no latch up even under extreme overvoltage conditions. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

The ADG408/ADG409 are improved replacements for the DG408/DG409 analog multiplexers.

ADG408 Truth Table

A2	A1	A0	EN	On Switch
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

ADG409 Truth Table

A1	A0	EN	On Switch Pair
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG408/ADG409 are fabricated on an enhanced LC²MOS process giving an increased signal range which extends to the supply rails.
2. Low Power Dissipation
3. Low R_{ON}
4. Single/Dual Supply Operation
5. Trench isolation guards against latch up.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

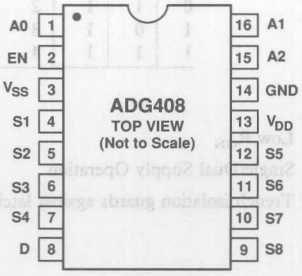
ADG408/ADG409—SPECIFICATIONS[1] (V_{DD} = +15 V, V_{SS} = −15 V, GND = 0 V, unless otherwise noted)

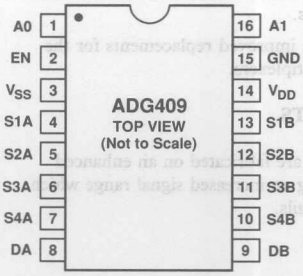
Parameter	B Version +25°C	B Version −40°C to +85°C	T Version +25°C	T Version −55°C to +125°C	Units	Test Conditions/Comments
Analog Signal Range	±15	±15	±15	±15	V	
R_{ON}		100		100	Ω max	V_D = ±10 V, I_S = −1 mA
ΔR_{ON}		15		15	Ω max	V_D = +10 V, −10 V
LEAKAGE CURRENTS						
Source OFF Leakage I_S (OFF)	0.5		0.5		nA max	V_D = ±10 V, V_S = ∓10 V
Drain OFF Leakage I_D (OFF)	0.5		0.5		nA max	V_D = ±10 V, V_S = ∓10 V
Channel ON Leakage I_D (ON)	1			1	nA max	V_S = V_D = ±10 V
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±10		±10	μA max	
C_{IN} Digital Input Capacitance	8		8		pF typ	
DYNAMIC CHARACTERISTICS[2]						R_L = 300 Ω, C_L = 35 pF, V_S = ±10 V
$t_{TRANSITION}$		250		250	ns max	
t_{OPEN}		10		10	ns min	
t_{ON} (EN)		150		150	ns max	
t_{OFF} (EN)		150		150	ns max	
Charge Injection	20		20		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF
OFF Isolation	−75		−75		dB typ	R_L = 1 kΩ, f = 100 kHz
C_S (OFF)	11		11		pF typ	
C_D (OFF)						
ADG408	40		40		pF typ	
ADG409	20		20		pF typ	
C_D (ON)						
ADG408	54		54		pF typ	
ADG409	34		34		pF typ	
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = −16.5 V Digital Inputs = 0 V or 5 V
I_{DD}	75	75	75	75	μA max	
I_{SS}	75	75	75	75	μA max	

NOTES
[1]Temperature ranges are as follows: B Versions: −40°C to +85°C; T Versions: −55°C to +125°C.
[2]Sample tested @+25°C to ensure compliance.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

PIN CONFIGURATIONS (DIP/SOIC)





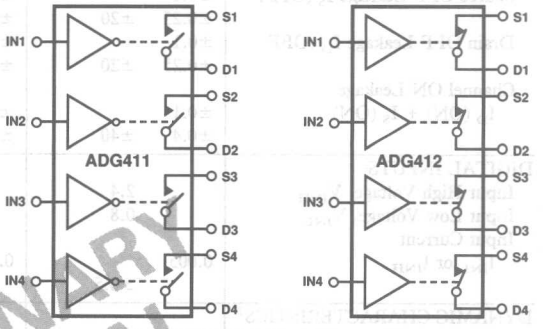
This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

LC²MOS
Precision Quad SPST Switches
ADG411/ADG412

FEATURES
- 44 V Supply Maximum Ratings
- ±15 V Analog Signal Range
- Low On Resistance (<35 Ω)
- Ultralow Power Dissipation (35 μW)
- Fast Switching Times
  - t_{ON} <175 ns
  - t_{OFF} <145 ns
- Latch-Up Proof
- Plug in Replacement for DG411/DG412

APPLICATIONS
- Audio and Video Switching
- Automatic Test Equipment
- Precision Data Acquisition
- Battery Powered Systems
- Sample Hold Systems
- Communication Systems

FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC "1" INPUT

5

PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The ADG411 and ADG412 are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS, trench isolated process which provides low power dissipation yet gives high switching speed and low on resistance. Trench isolation gives all the benefits of dielectric isolation and ensures no latch-up even under extreme over-voltage conditions. The on resistance profile is very flat over the full analog input range ensuring good linearity and low distortion when switching audio signals. High switching speed also makes the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

Both the ADG411 and the ADG412 contain four independent SPST switches. They differ only in that the digital control logic is inverted. Each switch conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition signal levels up to the supplies are blocked. All switches exhibit break before make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

Table I. Truth Table

ADG411 IN	ADG412 IN	Switch Condition
0	1	ON
1	0	OFF

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG411/ADG412 are fabricated on an enhanced LC²MOS, trench isolated process giving an increased signal range which extends to the supply rails.
2. Ultralow Power Dissipation
3. Low R_{ON}
4. Trench isolation guards against latch up.
5. Single Supply Operation
   For applications where the analog signal is unipolar, the ADG411/ADG412 can be operated from a single rail power supply.

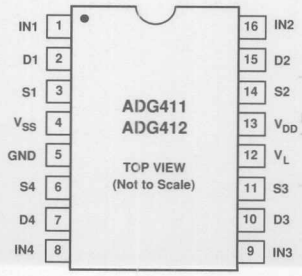
This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ADG411/ADG412—SPECIFICATIONS (V_{DD} = +15 V, V_{SS} = −15 V, V_L = +5 V, GND = 0 V, unless otherwise noted)

Parameter	B Version 25°C	B Version −40°C to +85°C	T Version 25°C	T Version −55°C to +125°C	Units	Test Conditions/ Comments
ANALOG SIGNAL RANGE		V_{DD} to V_{SS}		V_{DD} to V_{SS}	V	
R_{ON}	25		25		Ω typ	V_D = ±8.5 V, I_S = −10 mA
	35	45	35	45	Ω max	
LEAKAGE CURRENTS						V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source OFF Leakage I_S (OFF)	±0.1		±0.1		nA typ	V_D = ±15.5, V_S = ∓15.5 V
	±0.25	±20	±0.25	±20	nA max	
Drain OFF Leakage I_D (OFF)	±0.1		±0.1		nA typ	V_D = ±15.5, V_S = ∓15.5 V
	±0.25	±20	±0.25	±20	nA max	
Channel ON Leakage I_D (ON) + I_S (ON)	±0.1		±0.1		nA typ	V_D = V_S = ±15.5 V
	±0.4	±40	±0.4	±40	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current I_{INL} or I_{INH}	0.005		0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5		±0.5	μA max	
DYNAMIC CHARACTERISTICS[2]						
t_{ON}	110		110		ns typ	R_L = 300 Ω, C_L = 35 pF
		175		175	ns max	V_S = ±10 V
t_{OFF}	100		100		ns typ	R_L = 300 Ω, C_L = 35 pF
			145	145	ns max	V_S = ±10 V
Charge Injection	5		5		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF
OFF Isolation	68		68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
CS (OFF)	9		9		pF typ	f = 1 MHz
CD (OFF)	9		9		pF typ	f = 1 MHz
CD + CS (ON)	35		35		pF typ	f = 1 MHz
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = −16.5 V Digital Inputs = 0 V or 5 V
I_{DD}	0.0001		0.0001		μA typ	
	1	5	1	5	μA max	
I_{SS}	0.0001		0.0001		μA typ	
	1	5	1	5	μA max	
I_L	0.0001		0.0001			
	1	5	1	5	μA max	

NOTES
[1]Temperature ranges are as follows: B Versions: −40°C to +85°C; T Versions: −55°C to +125°C.
[2]Sample tested @ +25°C to ensure compliance.
Specifications subject to change without notice.

PIN CONFIGURATION



PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

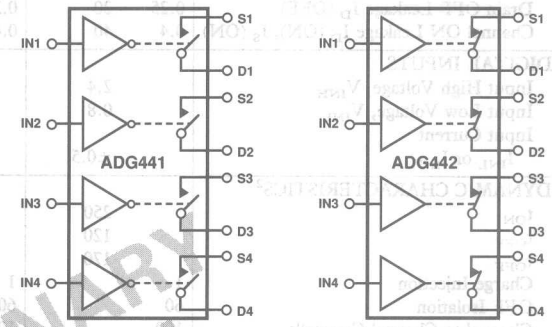
LC²MOS Quad SPST Switches

ADG441/ADG442

FEATURES
- 44 V Supply Maximum Ratings
- ±15 V Analog Signal Range
- Low On Resistance (<85 Ω)
- Low Power Dissipation (<1.6 mW)
- Fast Switching Times
  - t_{ON} < 250 ns
  - t_{OFF} < 120 ns
- Latch Up Proof
- Plug-In Upgrade for DG201A/ADG201A, DG202/ADG202A
- Plug-In Replacement for DG441/DG442

APPLICATIONS
- Audio and Video Switching
- Automatic Test Equipment
- Data Acquisition Systems
- Battery Powered Systems
- Sample Hold Systems
- Communication Systems

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

5

PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The ADG441 and ADG442 are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS, trench isolated process which provides low power dissipation yet gives high switching speed and low on resistance. The on resistance profile is very flat over the full analog input range ensuring good linearity and low distortion when switching audio signals. Trench isolation gives all the benefits of dielectric isolation and ensures no latch up even under extreme overvoltage conditions. High switching speed also makes the parts suitable for video signal switching. CMOS construction ensures low power dissipation making the parts suitable for portable and battery powered instruments. The ADG441/ADG442 are also pin compatible with ADG201A/DG201A, ADG202A/DG202 devices thereby offering easy system upgrading.

Both the ADG441 and the ADG442 contain four independent SPST switches. They differ only in that the digital control logic is inverted. Each switch conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

Truth Table

ADG441 In	ADG442 In	Switch Condition
0	1	ON
1	0	OFF

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG441/ADG442 are fabricated on an enhanced LC²MOS process giving an increased signal range which extends to the supply rails.
2. Low Power Dissipation
3. Low R_{ON}
4. Trench isolation guards against latch up.

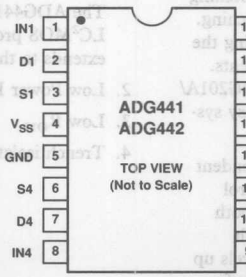
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Parameter	+25°C	−40°C to +85°C	+25°C	−55°C to +125°C	Units	Test Conditions/Comments
Analog Signal Range	±15	±15	±15	±15	V	
R_{ON}	85	100	85	100	Ω max	V_D = ±8.5 V, I_S = −10 mA
LEAKAGE CURRENTS						V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source OFF Leakage I_S (OFF)	0.25	20	0.25	20	nA max	V_D = ±15.5 V, V_S = ∓15.5 V
Drain OFF Leakage I_D (OFF)	0.25	20	0.25	20	nA max	V_D = ±15.5 V, V_S = ∓15.5 V
Channel ON Leakage I_D (ON), I_S (ON)	0.4	40	0.4	40	nA max	V_D = V_S = ±15.5 V
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current I_{INL} or I_{INH}		±0.5		±0.5	μA max	
DYNAMIC CHARACTERISTICS[2]						R_L = 1 kΩ, C_L = 35 pF, V_S = ±10 V
t_{ON}		250		250	ns max	
t_{OFF}		120		120	ns max	ADG441
t_{OFF}		170		170	ns max	ADG442
Charge Injection	1		1		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF
OFF Isolation	60		60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
Channel-to-Channel Crosstalk	100		100		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
C_S (OFF)	4		4		pF typ	
C_D (OFF)	4		4		pF typ	
C_D, C_S (ON)	16		16		pF typ	
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = −16.5 V Digital Inputs = 0 V or 5 V
I_{DD}	100	100	100	100	μA max	
I_{SS}	1	5	1	5	μA max	

NOTES
[1]Temperature ranges are as follows: B Versions: −40°C to +85°C; T Versions: −55°C to +125°C.
[2]Sample tested @ +25°C to ensure compliance.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

PIN CONFIGURATION



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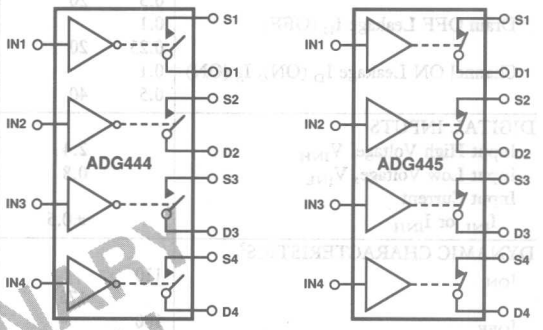
LC²MOS Quad SPST Switches

ADG444/ADG445

FEATURES
- 44 V Supply Maximum Ratings
- ±15 V Analog Signal Range
- Low On Resistance (<80 Ω)
- Ultralow Power Dissipation (35 μW)
- Fast Switching Times
  - t_{ON} < 250 ns
  - t_{OFF} < 120 ns
- Latch Up Proof
- Plug-In Upgrade for DG211/ADG211A, DG212/ADG212A
- Plug-In Replacement for DG411/DG412

APPLICATIONS
- Audio and Video Switching
- Automatic Test Equipment
- Precision Data Acquisition
- Battery Powered Systems
- Sample Hold Systems
- Communication Systems

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

5

PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The ADG444 and ADG445 are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS, trench isolated process which provides low power dissipation yet gives high switching speed and low on resistance. The on resistance profile is very flat over the full analog input range ensuring good linearity and low distortion when switching audio signals. Trench isolation gives all the benefits of dielectric isolation and ensures no latch up even under extreme overvoltage conditions. High switching speed also makes the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

Both the ADG444 and the ADG445 contain four independent SPST switches. They differ only in that the digital control logic is inverted. Each switch conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

Truth Table

ADG444 In	ADG445 In	Switch Condition
0	1	ON
1	0	OFF

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG444/ADG445 are fabricated on an enhanced LC²MOS trench isolated process giving an increased signal range which extends to the supply rails.
2. Ultralow Power Dissipation
3. Low R_{ON}
4. Trench isolation guards against latch up.
5. Single Supply Operation
   For applications where the analog signal is unipolar the ADG444/445 can be operated from a single rail power supply.

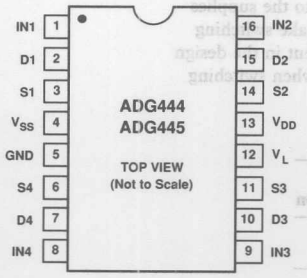
This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ADG444/ADG445—SPECIFICATIONS[1] (V_{DD} = +15 V, V_{SS} = −15 V, GND = 0 V, unless otherwise noted)

Parameter	B Version −40°C to +25°C	B Version −40°C to +85°C	T Version −55°C to +25°C	T Version −55°C to +125°C	Units	Test Conditions/ Comments
Analog Signal Range	±15	±15	±15	±15	V	
R_{ON}	80	100	80	100	Ω max	V_D = ±8.5 V, I_S = −10 mA
LEAKAGE CURRENTS						V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source OFF Leakage I_S (OFF)	0.01		0.01		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V
	0.5	20	0.5	20	nA max	
Drain OFF Leakage I_D (OFF)	0.1		0.1		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V
	0.25	20	0.25	20	nA max	
Channel ON Leakage I_D (ON), I_S (ON)	0.1		0.1		nA typ	V_D = V_S = ±15.5 V
	0.5	40	0.5	40	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±0.5		±0.5	μA max	
DYNAMIC CHARACTERISTICS[2]						
t_{ON}	110		110		ns typ	R_L = 300 Ω, C_L = 35 pF
		175		175	ns max	V_S = ±10 V
t_{OFF}	100		100		ns typ	RL = 300 Ω, C_L = 35 pF
		145		145	ns max	V_S = ±10 V
Charge Injection	1		1		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF
OFF Isolation	68		68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
Channel-to Channel Crosstalk	100		100		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
C_S (OFF)	4		4		pF typ	
C_D (OFF)	4		4		pF typ	
C_D, C_S (ON)	16		16		pF typ	
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = −16.5 V Digital Inputs = 0 V or 5 V
I_{DD}	0.0001		0.0001		μA typ	
	1	5	1	5	μA max	
I_{SS}	0.0001		0.0001		μA typ	
	1	5	1	5	μA max	
I_L	0.0001		0.0001			
	1	5	1	5	μA max	

NOTES
[1]Temperature ranges are as follows: B Versions: −40°C to +85°C; S Versions: −55°C to +125°C.
[2]Sample tested @ +25°C to ensure compliance.
Specifications subject to change without notice.

PIN CONFIGURATION (DIP/SOIC)



PRELIMINARY TECHNICAL DATA

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ANALOG DEVICES

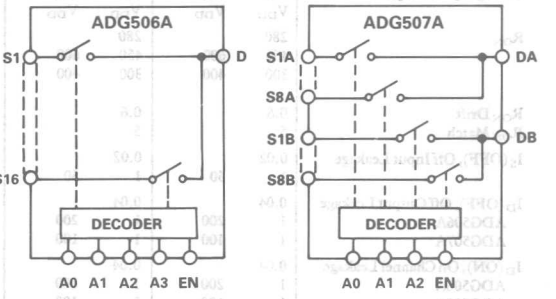
CMOS 8/16 Channel Analog Multiplexers

ADG506A/ADG507A

FEATURES

- 44V Supply Maximum Rating
- V_{SS} to V_{DD} Analog Signal Range
- Single/Dual Supply Specifications
- Wide Supply Ranges (10.8V to 16.5V)
- Extended Plastic Temperature Range (−40°C to +85°C)
- Low Power Dissipation (28mW max)
- Low Leakage (20pA typ)
- Available in 28-Lead DIP, SOIC, PLCC and LCCC Packages
- Superior Alternative to:
  - DG506A, HI-506
  - DG507A, HI-507

FUNCTIONAL BLOCK DIAGRAMS



5

GENERAL DESCRIPTION

The ADG506A and ADG507A are CMOS monolithic analog multiplexers with 16 channels and dual 8 channels respectively. The ADG506A switches one of 16 inputs to a common output depending on the state of four binary addresses and an enable input. The ADG507A switches one of 8 differential inputs to a common differential output depending on the state of three binary addresses and an enable input. Both devices have TTL and 5V CMOS logic compatible digital inputs.

The ADG506A and ADG507A are designed on an enhanced LC^2MOS process which gives an increased signal capability of V_{SS} to V_{DD} and enables operation over a wide range of supply voltages. The devices can comfortably operate anywhere in the 10.8V to 16.5V single or dual supply range. These multiplexers also feature high switching speeds and low R_{ON}.

PRODUCT HIGHLIGHTS

1. Single/Dual Supply Specifications with a Wide Tolerance:
   The devices are specified in the 10.8V to 16.5V range for both single and dual supplies.
2. Extended Signal Range:
   The enhanced LC^2MOS processing results in a high breakdown and an increased analog signal range of V_{SS} to V_{DD}.
3. Break-Before-Make Switching:
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
4. Low Leakage:
   Leakage currents in the range of 20pA make these multiplexers suitable for high precision circuits.

ORDERING INFORMATION

Model[1]	Temperature Range	Package Option[2]
ADG506AKN	−40°C to +85°C	N-28
ADG506AKR	−40°C to +85°C	R-28
ADG506AKP	−40°C to +85°C	P-28A
ADG506ABQ	−40°C to +85°C	Q-28
ADG506ATQ	−55°C to +125°C	Q-28
ADG506ATE	−55°C to +125°C	E-28A
ADG507AKN	−40°C to +85°C	N-28
ADG507AKR	−40°C to +85°C	R-28
ADG507AKP	−40°C to +85°C	P-28A
ADG507ABQ	−40°C to +85°C	Q-28
ADG507ATQ	−55°C to +125°C	Q-28
ADG507ATE	−55°C to +125°C	E-28A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. See Analog Devices Military Products Databook (1990) for military data sheet.
[2]N = Plastic DIP; R = 0.3" Small Outline IC (SOIC); P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; E = Leadless Ceramic Chip Carrier (LCCC). For outline information see Package Information section.

Dual Supply (V_{DD} = +10.8V to +16.5V, V_{SS} = -10.8V to -16.5V unless otherwise specified)

Parameter	ADG506A ADG507A K Version +25°C	K Version −40°C to +85°C	ADG506A ADG507A B Version +25°C	B Version −40°C to +85°C	ADG506A ADG507A T Version +25°C	T Version −55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V min V max	
R_{ON}	280		280		280		Ω typ	−10V≤V_S≤+10V, I_{DS} = 1mA; Test Circuit 1
	450	600	450	600	450	600	Ω max	
	300	400	300	400			Ω max	V_{DD} = 15V(±10%), V_{SS} = −15V(±10%)
					300	400	Ω max	V_{DD} = 15V(±5%), V_{SS} = −15V(±5%)
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	−10V≤V_S≤+10V, I_{DS} = 1mA
R_{ON} Match	5		5		5		% typ	−10V≤V_S≤+10V, I_{DS} = 1mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 2
	1	50	1	50	1	50	nA max	
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 3
ADG506A	1	200	1	200	1	200	nA max	
ADG507A	1	100	1	100	1	100	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 4
ADG506A	1	200	1	200	1	200	nA max	
ADG507A	1	100	1	100	1	100	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG507A only)		25		25		25	nA max	V1 = ±10V, V2 = ∓10V; Test Circuit 5.
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = =0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
$t_{TRANSITION}$[1]	200		200		200		ns typ	V1 = ±10V, V2 = ∓10V; Test Circuit 6
	300	400	300	400	300	400	ns max	
t_{OPEN}[1]	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON} (EN)[1]	200		200		200		ns typ	Test Circuit 8
	300	400	300	400	300	400	ns max	
t_{OFF} (EN)[1]	200		200		200		ns typ	Test Circuit 8
	300	400	300	400	300	400	ns max	
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF,
	50		50		50		dB min	V_S = 7V rms, f = 100kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8V
C_D (OFF)								
ADG506A	44		44		44		pF typ	V_{EN} = 0.8V
ADG507A	22		22		22		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 9
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
I_{SS}	20		20		20		μA typ	V_{IN} = V_{INL} or V_{INH}
		0.2		0.2		0.2	mA max	
Power Dissipation	10		10		10		mW typ	
		28		28		28	mW max	

NOTE
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

Single Supply (V_{DD} = +10.8V to +16.5V, V_{SS} = GND = 0V unless otherwise specified)

Parameter	ADG506A ADG507A K Version +25°C	K Version −40°C to +85°C	ADG506A ADG507A B Version +25°C	B Version −40°C to +85°C	ADG506A ADG507A T Version +25°C	T Version −55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}	500		500		500		Ω typ	0V≤V_S≤+10V, I_{DS} = 0.5mA; Test Circuit 1
	700	1000	700	1000	700	1000	Ω max	
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	0V≤V_S≤+10V, I_{DS} = 0.5mA
R_{ON} Match	5		5		5		% typ	0V≤V_S≤+10V, I_{DS} = 0.5mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = +10V/0V, V2 = 0V/+10V;
	1	50	1	50	1	50	nA max	Test Circuit 2
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = +10V/0V, V2 = 0V/+10V;
ADG506A	1	200	1	200	1	200	nA max	Test Circuit 3
ADG507A	1	100	1	100	1	100	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = +10V/0V, V2 = 0V/+10V;
ADG506A	1	200	1	200	1	200	nA max	Test Circuit 4
ADG507A	1	100	1	100	1	100	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG507A only)		25		25		25	nA max	V1 = +10V/0V, V2 = 0V/+10V; Test Circuit 5.
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
$t_{TRANSITION}$[1]	300		300		300		ns typ	V1 = +10V/0V, V2 = 0V/+10V; Test Circuit 6
	450	600	450	600	450	600	ns max	
t_{OPEN}[1]	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON} (EN)[1]	250		250		250		ns typ	Test Circuit 8
	450	600	450	600	450	600	ns max	
t_{OFF} (EN)[1]	250		250		250		ns typ	Test Circuit 8
	450	600	450	600	450	600	ns max	
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF,
	50		50		50		dB min	V_S = 3.5V rms, f = 100kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8V
C_D (OFF)								
ADG506A	44		44		44		pF typ	V_{EN} = 0.8V
ADG507A	22		22		22		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 9
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
Power Dissipation	10		10		10		mW typ	
		25		25		25	mW max	

NOTE
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

TRUTH TABLES

A3	A2	A1	A0	EN	ON SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

ADG506A

A2	A1	A0	EN	ON SWITCH PAIR
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

ADG507A

X = Don't Care

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

V_{DD} to V_{SS}	44V
V_{DD} to GND	25V
V_{SS} to GND	−25V
Analog Inputs[1]	
Voltage at S, D	V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First
Continuous Current, S or D	20mA
Pulsed Current S or D	
1ms Duration, 10% Duty Cycle	40mA
Digital Inputs[1]	
Voltage at A, EN	V_{SS} −4V to V_{DD} +4V or 20mA, Whichever Occurs First
Power Dissipation (Any Package)	
Up to +75°C	470mW
Derates above +75°C by	6mW/°C
Operating Temperature	
Commercial (K Version)	−40°C to +85°C
Industrial (B Version)	−40°C to +85°C
Extended (T Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

NOTE

[1]Overvoltage at A, EN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

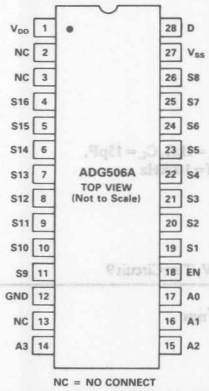
CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

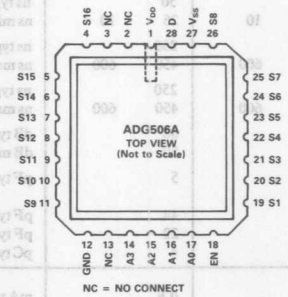


PIN CONFIGURATIONS

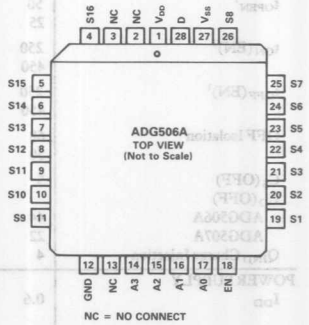
DIP, SOIC

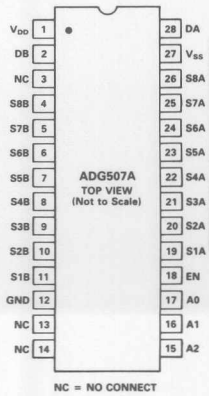


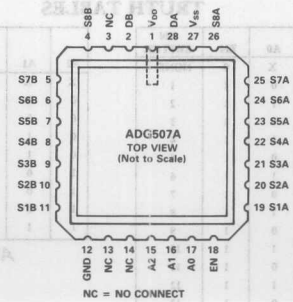
LCCC

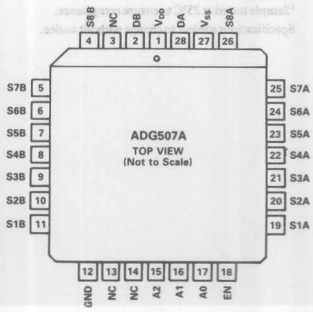


PLCC

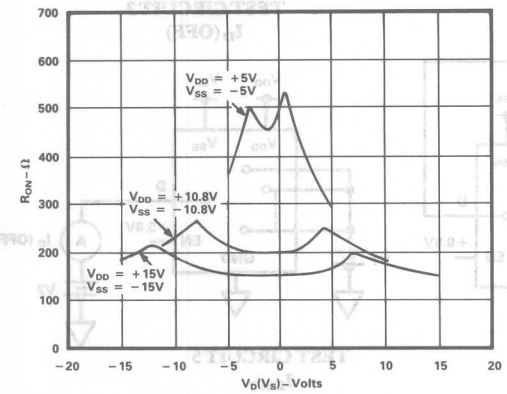




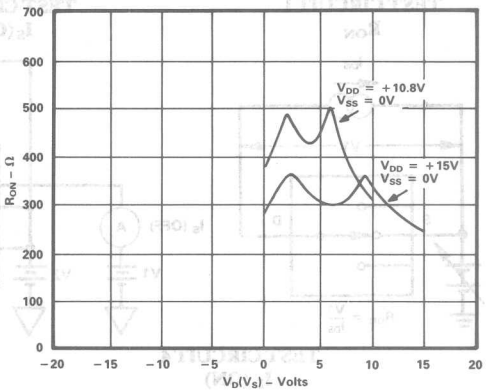




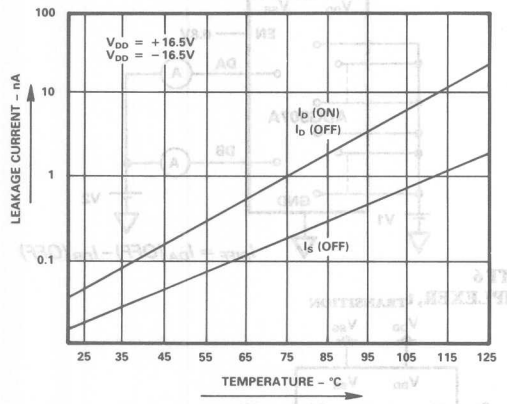
The multiplexers are guaranteed functional with reduced single or dual supplies down to 4.5V.



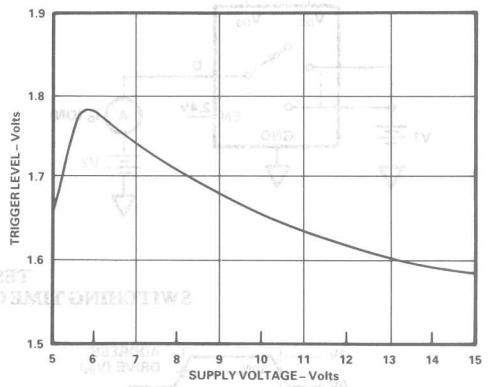
R_{ON} as a Function of $V_D(V_S)$: Dual Supply Voltage, T_A = +25°C



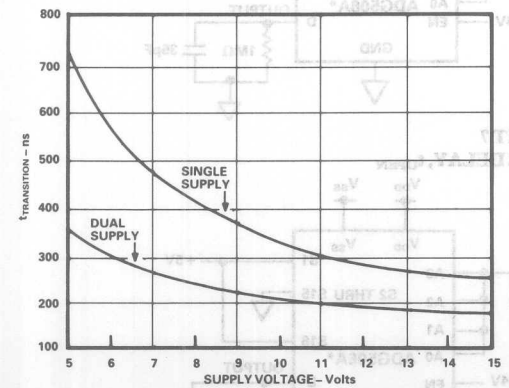
R_{ON} as a Function of $V_D(V_S)$: Single Supply Voltage, T_A = +25°C



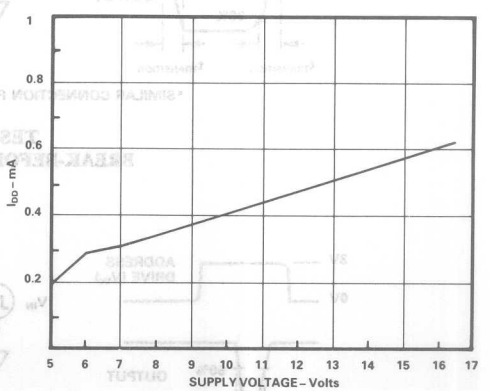
Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)



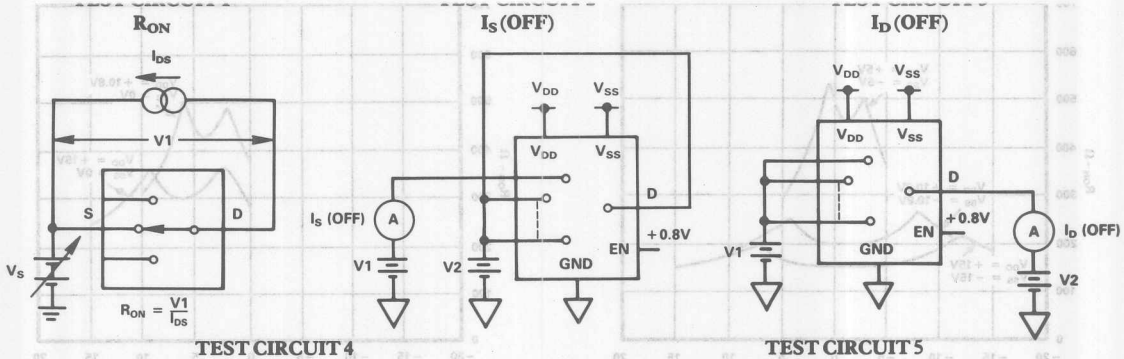
Trigger Levels vs. Power Supply Voltage, Dual or Single Supply, T_A = +25°C



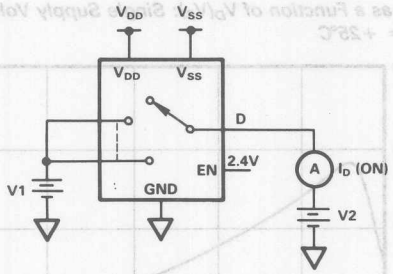
$t_{TRANSITION}$ vs. Supply Voltage: Dual and Single Supplies, T_A = +25°C (Note: For V_{DD} and $|V_{SS}| < 10V$; V1 = V_{DD}/V_{SS}, V2 = V_{SS}/V_{DD}. See Test Circuit 6)



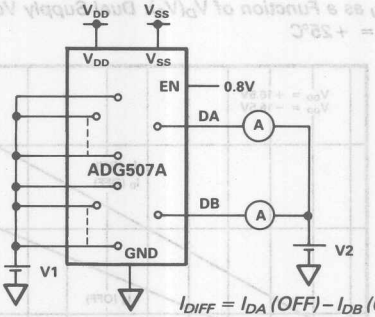
I_{DD} vs. Supply Voltage: Dual or Single Supply, T_A = +25°C



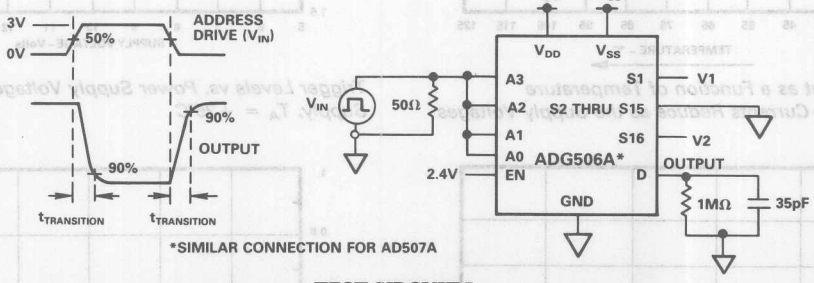
TEST CIRCUIT 4
I_D (ON)



TEST CIRCUIT 5
I_{DIFF}

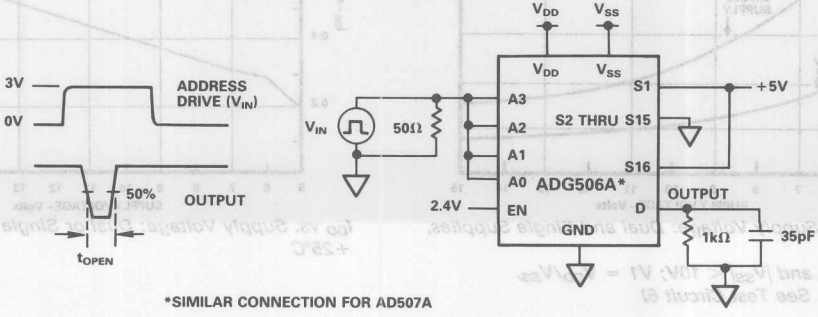


TEST CIRCUIT 6
SWITCHING TIME OF MULTIPLEXER, $t_{TRANSITION}$



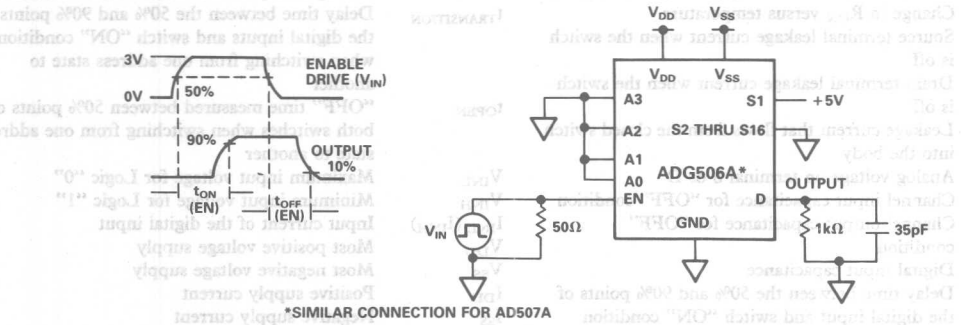
*SIMILAR CONNECTION FOR AD507A

TEST CIRCUIT 7
BREAK-BEFORE-MAKE DELAY, t_{OPEN}

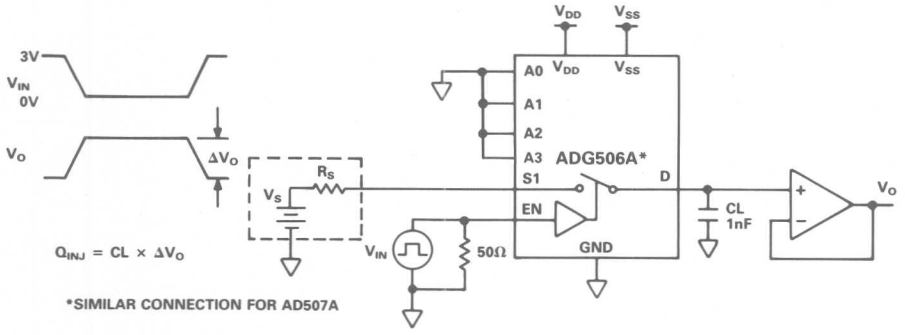


*SIMILAR CONNECTION FOR AD507A

TEST CIRCUIT 8
ENABLE DELAY, t_{ON} (EN), t_{OFF} (EN)



TEST CIRCUIT 9
CHARGE INJECTION

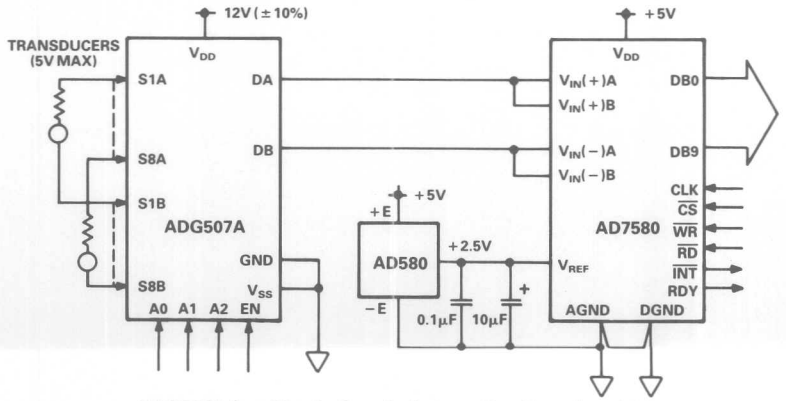


5

SINGLE SUPPLY AUTOMATIVE APPLICATION

The excellent performance of the multiplexers under single supply conditions makes the ADG506A/ADG507A suitable in applications, such as automotive and disc drives, where only positive power supply voltages are normally available. The following application circuit shows the ADG507A connected as an 8-channel differential multiplexer in an automotive, data acquisition application circuit.

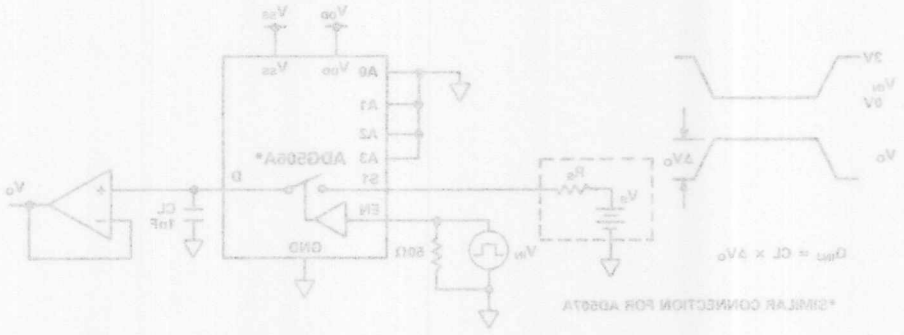
The AD7580 is a 10-bit successive approximation ADC which has an on-chip sample-hold amplifier and provides a conversion result in 20μs. The ADC has a differential analog inputs and is configured in the application circuit for a span of 2.5V over a common-mode range 0 to +5V. Wider common-mode ranges can be accomodated. See the AD7579/AD7580 data sheet for more details. The complete system operates from +12V (±10%) and +5V supplies. The analog input signals to the ADG507A contain information such as temperature, pressure, speed etc.

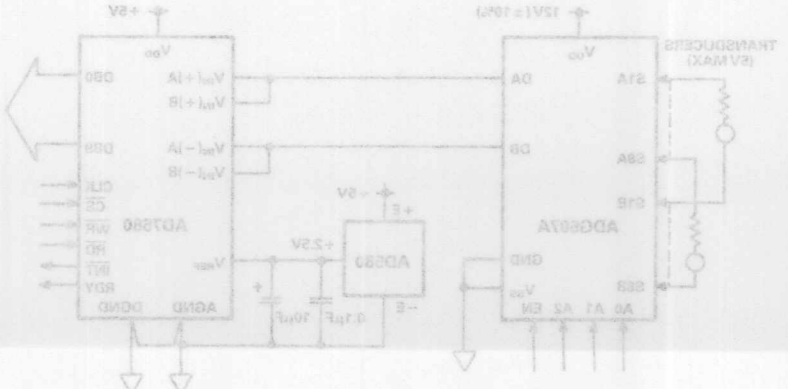


ADG507A in a Single Supply Automotive Data Acquisition Application.

TERMINOLOGY

R_{ON}	Ohmic resistance between terminals D and S
R_{ON} Match	Difference between the R_{ON} of any two channels
R_{ON} Drift	Change in R_{ON} versus temperature
I_S (OFF)	Source terminal leakage current when the switch is off
I_D (OFF)	Drain terminal leakage current when the switch is off
I_D (ON)	Leakage current that flows from the closed switch into the body
V_S (V_D)	Analog voltage on terminal S or D
C_S (OFF)	Channel input capacitance for "OFF" condition
C_D (OFF)	Channel output capacitance for "OFF" condition
C_{IN}	Digital input capacitance
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch "ON" condition
t_{OFF} (EN)	Delay time between the 50% and 10% points of the digital input and switch "OFF" condition
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and switch "ON" condition when switching from one address state to another
t_{OPEN}	"OFF" time measured between 50% points of both switches when switching from one address state to another
V_{INL}	Maximum input voltage for Logic "0"
V_{INH}	Minimum input voltage for Logic "1"
I_{INL} (I_{INH})	Input current of the digital input
V_{DD}	Most positive voltage supply
V_{SS}	Most negative voltage supply
I_{DD}	Positive supply current
I_{SS}	Negative supply current



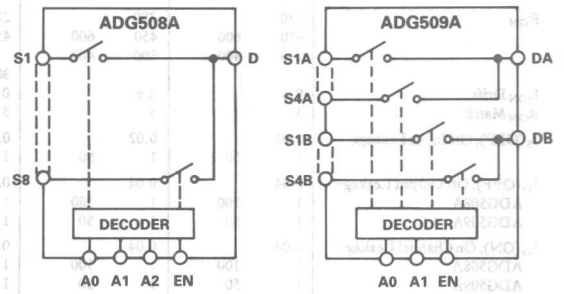


CMOS
4/8 Channel Analog Multiplexers

ADG508A/ADG509A

FEATURES
- 44V Supply Maximum Rating
- V_{SS} to V_{DD} Analog Signal Range
- Single/Dual Supply Specifications
- Wide Supply Ranges (10.8V to 16.5V)
- Extended Plastic Temperature Range (−40°C to +85°C)
- Low Power Dissipation (28mW max)
- Low Leakage (20pA typ)
- Available in 16-Lead DIP/SOIC and 20-Lead PLCC/LCCC Packages
- Superior Alternative to:
  - DG508A, HI-508
  - DG509A, HI-509

FUNCTIONAL BLOCK DIAGRAMS



5

GENERAL DESCRIPTION

The ADG508A and ADG509A are CMOS monolithic analog multiplexers with 8 channels and dual 4 channels respectively. The ADG508A switches one of 8 inputs to a common output depending on the state of three binary addresses and an enable input. The ADG509A switches one of 4 differential inputs to a common differential output depending on the state of two binary addresses and an enable input. Both devices have TTL and 5V CMOS logic compatible digital inputs.

The ADG508A and ADG509A are designed on an enhanced LC^{2}MOS process which gives an increased signal capability of V_{SS} to V_{DD} and enables operation over a wide range of supply voltages. The devices can comfortably operate anywhere in the 10.8V to 16.5V single or dual supply range. These multiplexers also feature high switching speeds and low R_{ON}.

PRODUCT HIGHLIGHTS

1. Single/Dual Supply Specifications with a Wide Tolerance:
   The devices are specified in the 10.8V to 16.5V range for both single and dual supplies.
2. Extended Signal Range:
   The enhanced LC^{2}MOS processing results in a high breakdown and an increased analog signal range of V_{SS} to V_{DD}.
3. Break-Before-Make Switching:
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
4. Low Leakage:
   Leakage currents in the range of 20pA make these multiplexers suitable for high precision circuits.

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG508AKN	−40°C to +85°C	N-16
ADG508AKR	−40°C to +85°C	R-16A
ADG508AKP	−40°C to +85°C	P-20A
ADG508ABQ	−40°C to +85°C	Q-16
ADG508ATQ[3]	−55°C to +125°C	Q-16
ADG508ATE[3]	−55°C to +125°C	E-20A
ADG509AKN	−40°C to +85°C	N-16
ADG509AKR	−40°C to +85°C	R-16A
ADG509AKP	−40°C to +85°C	P-20A
ADG509ABQ	−40°C to +85°C	Q-16
ADG509ATQ	−55°C to +125°C	Q-16
ADG509ATE	−55°C to +125°C	E-20A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. See Analog Devices Military Products Databook (1990) for military data sheet.
[2]E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; R = 0.15" Small Outline IC (SOIC). For outline information see Package Information section.

ADG508A/ADG509A—SPECIFICATIONS

Dual Supply (V_{DD} = +10.8V to +16.5V, V_{SS} = −10.8V to −16.5V unless otherwise noted.)

Parameter	ADG508A ADG509A K Version		ADG508A ADG509A B Version		ADG508A ADG509A T Version		Units	Comments
	+25°C	−40°C to +85°C	25°C	−40°C to +85°C	+25°C	−55°C to +125°C		
ANALOG SWITCH								
Analog Signal Range	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V min V max	
R_{ON}	280		280		280		Ω typ	−10V≤V_S≤+10V, I_{DS} = 1mA; Test Circuit 1
	450	600	450	600	450	600	Ω max	
	300	400	300	400			Ω max	V_{DD} = 15V(±10%), V_{SS} = −15V(±10%)
					300	400	Ω max	V_{DD} = 15V(±5%), V_{SS} = −15V(±5%)
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	V_S = 0, I_{DS = 1mA
R_{ON} Match	5		5		5		% typ	−10V≤V_S≤+10V, I_{DS} = 1mA
I_S(OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 2
	1	50	1	50	1	50	nA max	
I_D(OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 3
ADG508A	1	100	1	100	1	100	nA max	
ADG509A	1	50	1	50	1	50	nA max	
I_D(ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 4
ADG508A	1	100	1	100	1	100	nA max	
ADG509A	1	50	1	50	1	50	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG509A only)		25		25		25	nA max	V1 = ±10V, V2 = ∓10V; Test Circuit 5.
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
$t_{TRANSITION}$[1]	200		200		200		ns typ	V1 = ±10V, V2 = ∓10V; Test Circuit 6
	300	400	300	400	300	400	ns max	
t_{OPEN}[1]	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON}(EN)[1]	200		200		200		ns typ	Test Circuit 8
	300	400	300	400	300	400	ns max	
t_{OFF}(EN)[1]	200		200		200		ns typ	Test Circuit 8
	300	400	300	400	300	400	ns max	
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF,
	50		50		50		dB min	V_S = 7V rms, f = 100kHz
C_S(OFF)	5		5		5		pF typ	V_{EN} = 0.8V
C_D(OFF)								
ADG508A	22		22		22		pF typ	V_{EN} = 0.8V
ADG509A	11		11		11		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 9
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
I_{SS}	20		20		20		μA typ	V_{IN} = V_{INL} or V_{INH}
		0.2		0.2		0.2	mA max	
Power Dissipation	10		10		10		mW typ	
		28		28		28	mW max	

NOTE
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

Single Supply (V_{DD} = +10.8V to +16.5V, V_{SS} = GND = 0V unless otherwise noted.)

Parameter	ADG508A ADG509A K Version +25°C	ADG508A ADG509A K Version −40°C to +85°C	ADG508A ADG509A B Version +25°C	ADG508A ADG509A B Version −40°C to +85°C	ADG508A ADG509A T Version +25°C	ADG508A ADG509A T Version −55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	GND	GND	GND	GND	GND	GND	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}	500		500		500		Ω typ	GND≤V_S≤ + 10V, I_{DS} = 0.5mA; Test Circuit 1
	700	1000	700	1000	700	1000	Ω max	
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	V_S = 0, I_{DS} = 0.5mA
R_{ON} Match	5		5		5		% typ	GND≤V_S≤ + 10V, I_{DS} = 0.5mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = + 10V/GND, V2 = GND/ + 10V;
	1	50	1	50	1	50	nA max	Test Circuit 2
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = + 10V/GND, V2 = GND/ + 10V;
ADG508A	1	100	1	100	1	100	nA max	Test Circuit 3
ADG509A	1	50	1	50	1	50	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = + 10V/GND, V2 = GND/ + 10V;
ADG508A	1	100	1	100	1	100	nA max	Test Circuit 4
ADG509A	1	50	1	50	1	50	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG509A only)		25		25		25	nA max	V1 = + 10V/GND, V2 = GND/ + 10V; Test Circuit 5.
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
$t_{TRANSITION}$[1]	300		300		300		ns typ	V1 = + 10V/GND, V2 = GND/ + 10V; Test Circuit 6
	450	600	450	600	450	600	ns max	
t_{OPEN}[1]	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON} (EN)[1]	250		250		250		ns typ	Test Circuit 8
	450	600	450	600	450	600	ns max	
t_{OFF} (EN)[1]	250		250		250		ns typ	Test Circuit 8
	450	600	450	600	450	600	ns max	
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF,
	50		50		50		dB min	V_S = 3.5V rms, f = 100kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8V
C_D (OFF)								
ADG508A	22		22		22		pF typ	V_{EN} = 0.8V
ADG509A	11		11		11		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 9
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
Power Dissipation	10		10		10		mW typ	
		25		25		25	mW max	

NOTE
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

TRUTH TABLES

A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care *ADG508A*

A1	A0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

X = Don't Care *ADG509A*

V_{DD} to V_{SS} 44V
V_{DD} to GND 25V
V_{SS} to GND . . . . . −25V
Analog Inputs[1]
Voltage at S, D . . . . . V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First
Continuous Current, S or D 20mA
Pulsed Current S or D
1ms Duration, 10% Duty Cycle 40mA

Power Dissipation (Any Package)
Up to +75°C 470mW
Derates above +75°C by . . . . . 6mW/°C
Operating Temperature
Commercial (K Version) . . . . . −40°C to +85°C
Industrial (B Version) . . . . . −40°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C

NOTE
[1]Overvoltage at A, EN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

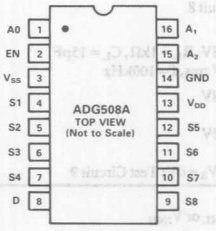
CAUTION

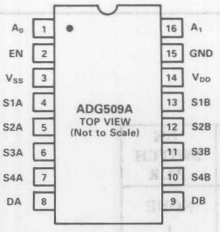
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



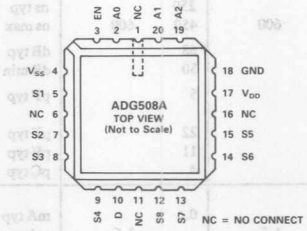
PIN CONFIGURATIONS

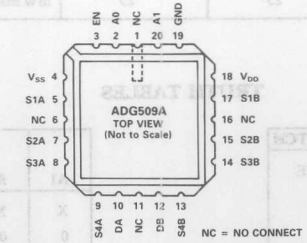
DIP, SOIC



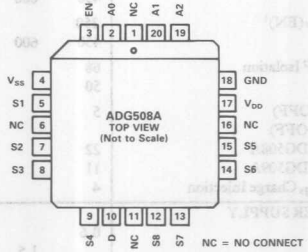


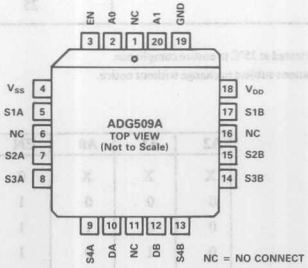
LCCC



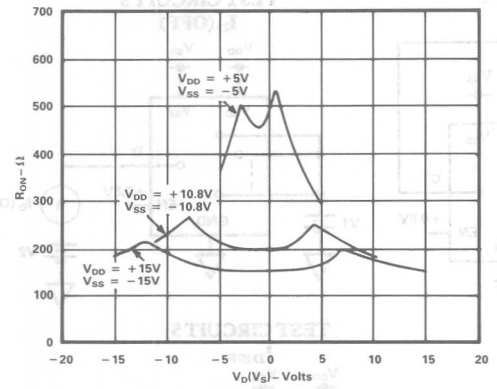


PLCC

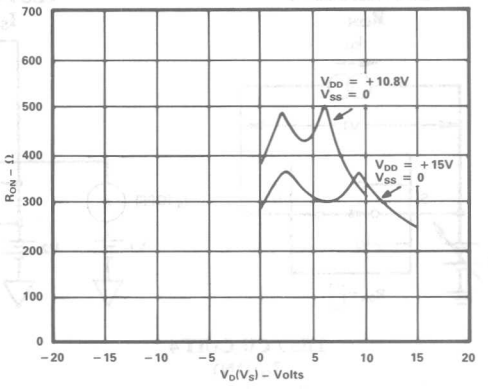




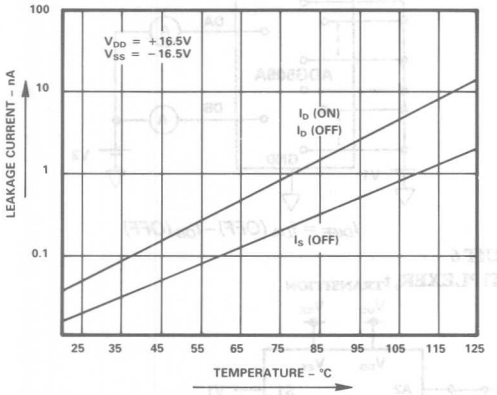
The multiplexers are guaranteed functional with reduced single or dual supplies down to 4.5V.



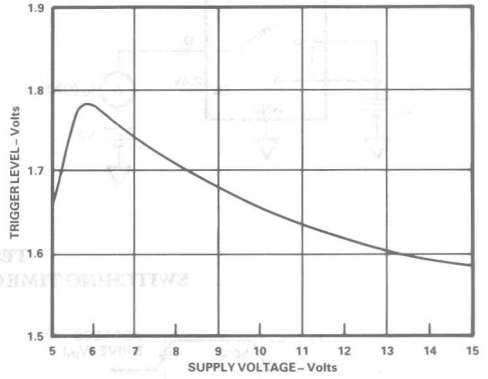
R_{ON} as a Function of $V_D(V_S)$: Dual Supply Voltage, T_A = +25°C



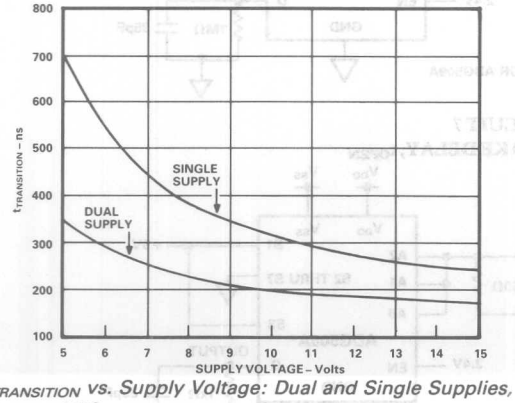
R_{ON} as a Function of $V_D(V_S)$: Single Supply Voltage, T_A = +25°C



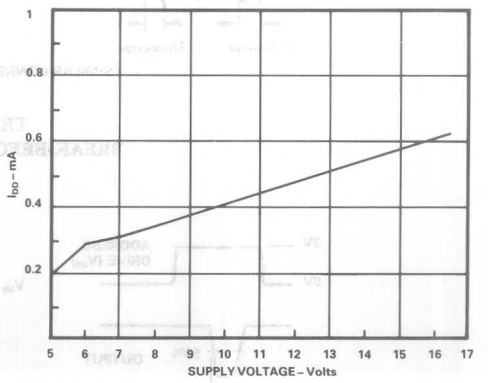
Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)



Trigger Levels vs. Power Supply Voltage, Dual or Single Supply, T_A = +25°C



$t_{TRANSITION}$ vs. Supply Voltage: Dual and Single Supplies, T_A = +25°C (Note: For V_{DD} and $|V_{SS}| < 10V$; V1 = V_{DD}/V_{SS}, V2 = V_{SS}/V_{DD}. See Test Circuit 6)

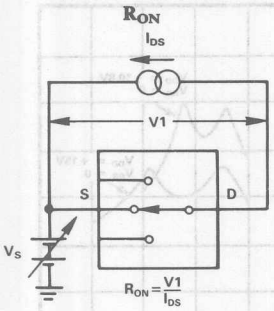


I_{DD} vs. Supply Voltage: Dual or Single Supply, T_A = +25°C

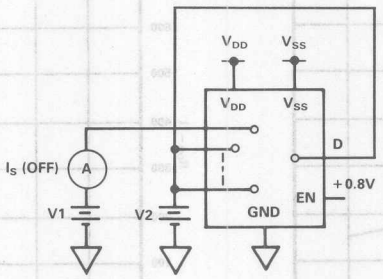
ADG508A/ADG509A—Test Circuits

Note: All Digital Input Signal Rise and Fall Times Measured from 10% to 90% of 3V. $t_R = t_F = 20ns$.

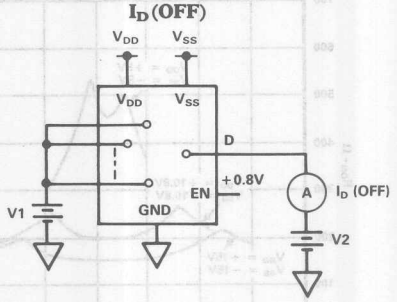
TEST CIRCUIT 1
R_{ON}



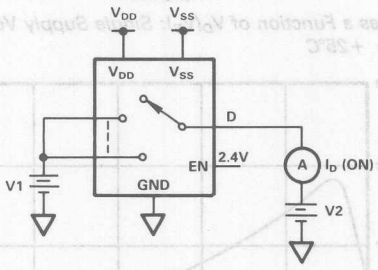
TEST CIRCUIT 2
I_S (OFF)



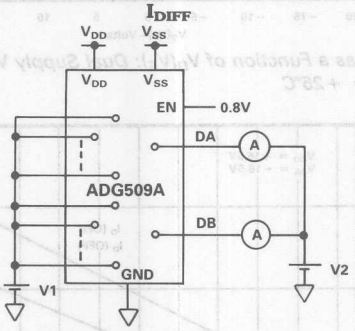
TEST CIRCUIT 3
I_D (OFF)



TEST CIRCUIT 4
I_D (ON)

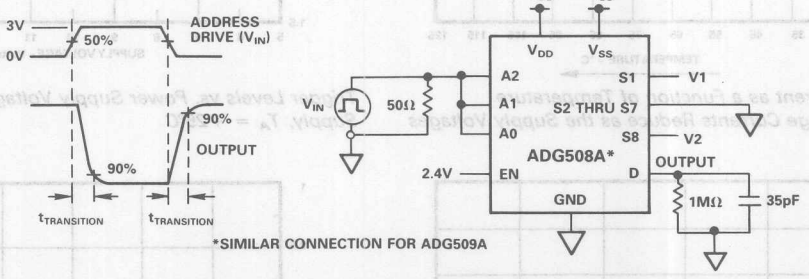


TEST CIRCUIT 5
I_{DIFF}



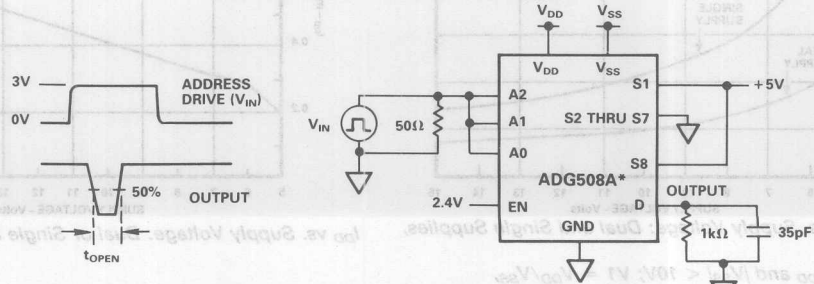
$I_{DIFF} = I_{DA}(OFF) - I_{DB}(OFF)$

TEST CIRCUIT 6
SWITCHING TIME OF MULTIPLEXER, $t_{TRANSITION}$



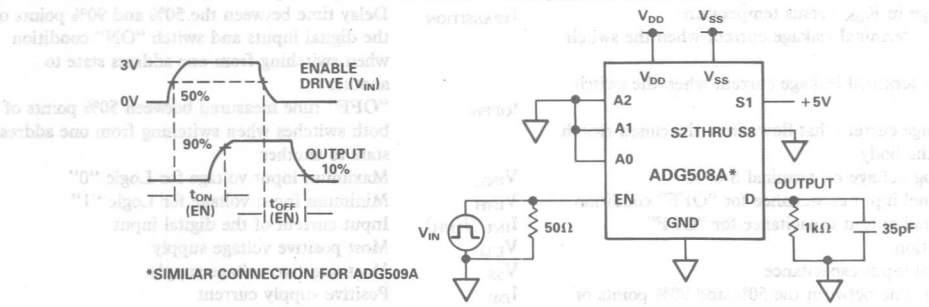
*SIMILAR CONNECTION FOR ADG509A

TEST CIRCUIT 7
BREAK-BEFORE-MAKE DELAY, t_{OPEN}

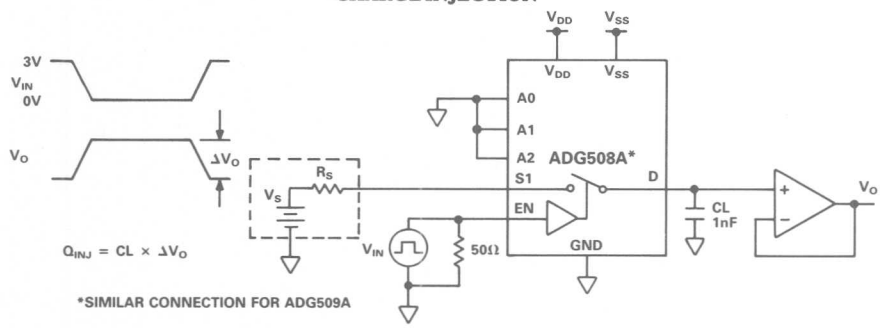


*SIMILAR CONNECTION FOR ADG509A

TEST CIRCUIT 8
ENABLE DELAY, t_{ON} (EN), t_{OFF} (EN)



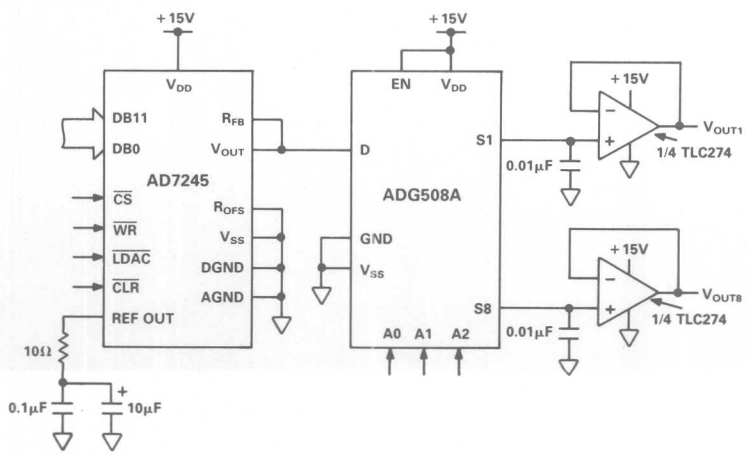
TEST CIRCUIT 9
CHARGE INJECTION



5

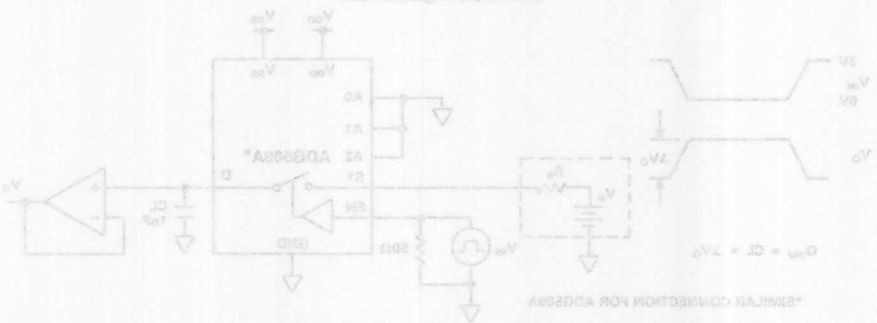
SINGLE SUPPLY OCTAL DAC APPLICATION

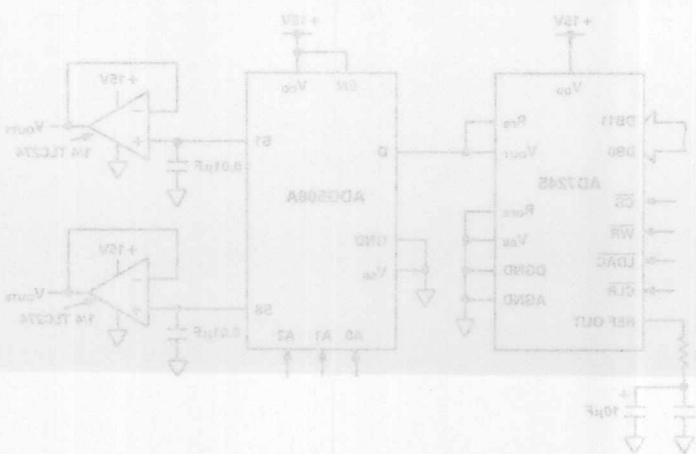
The following circuit shows the ADG508A connected as a demultiplexer to provide eight separate digitally programmable voltages (0 to +10V) from the AD7245. The AD7245 is a complete 12-bit, voltage output DAC with output amplifier and Zener voltage reference on a monolithic CMOS chip. The entire system operates from a single +15V power supply. The ADG508A is ideally suited for the application because it has both low charge injection and I_S (OFF) leakage current.



ADG508A in a Single-Supply Octal DAC Circuit

R_{ON}	Ohmic resistance between terminals D and S
R_{ON} Match	Difference between the R_{ON} of any two channels
R_{ON} Drift	Change in R_{ON} versus temperature
I_S (OFF)	Source terminal leakage current when the switch is off
I_D (OFF)	Drain terminal leakage current when the switch is off
I_D (ON)	Leakage current that flows from the closed switch into the body
V_S (V_D)	Analog voltage on terminal S or D
C_S (OFF)	Channel input capacitance for "OFF" condition
C_D (OFF)	Channel output capacitance for "OFF" condition
C_{IN}	Digital input capacitance
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch "ON" condition
t_{OFF} (EN)	Delay time between the 50% and 10% points of the digital input and switch "OFF" condition
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and switch "ON" condition when switching from one address state to another
t_{OPEN}	"OFF" time measured between 50% points of both switches when switching from one address state to another
V_{INL}	Maximum input voltage for Logic "0"
V_{INH}	Minimum input voltage for Logic "1"
I_{INL} (I_{INH})	Input current of the digital input
V_{DD}	Most positive voltage supply
V_{SS}	Most negative voltage supply
I_{DD}	Positive supply current
I_{SS}	Negative supply current





ANALOG DEVICES

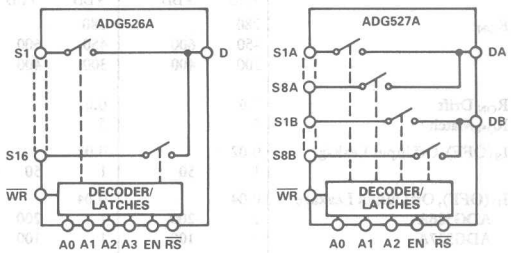
CMOS Latched 8/16 Channel Analog Multiplexers

ADG526A/ADG527A

FEATURES

- 44V Supply Maximum Rating
- V_{SS} to V_{DD} Analog Signal Range
- Single/Dual Supply Specifications
- Wide Supply Ranges (10.8V to 16.5V)
- Microprocessor Compatible (100ns $\overline{WR}$ Pulse)
- Extended Plastic Temperature Range (−40°C to +85°C)
- Low Leakage (20pA typ)
- Low Power Dissipation (28mW max)
- Available in DIP, SOIC, PLCC and LCCC Packages
- Superior Alternative to:
  - DG526
  - DG527

FUNCTIONAL BLOCK DIAGRAMS



5

GENERAL DESCRIPTION

The ADG526A and ADG527A are CMOS monolithic analog multiplexers with 16 channels and dual 8 channels respectively. On-chip latches facilitate microprocessor interfacing. The ADG526A switches one of 16 inputs to a common output depending on the state of four binary addresses and an enable input. The ADG527A switches one of 8 differential inputs to a common differential output depending on the state of three binary addresses and an enable input. Both devices have TTL and 5V CMOS logic compatible digital inputs.

The ADG526A and ADG527A are designed on an enhanced LC^2MOS process which gives an increased signal capability of V_{SS} to V_{DD} and enables operation over a wide range of supply voltages. The devices can comfortably operate anywhere in the 10.8V to 16.5V single or dual supply range. These multiplexers also feature high switching speeds and low R_{ON}.

PRODUCT HIGHLIGHTS

1. Single/Dual Supply Specifications with a Wide Tolerance:
   The devices are specified in the 10.8V to 16.5V range for both single and dual supplies.
2. Easily Interfaced:
   The ADG526A and ADG527A can be easily interfaced with microprocessors. The $\overline{WR}$ signal latches the state of the Address control lines and the Enable line. The $\overline{RS}$ signal clears both the address and enable data in the latches resulting in no output (all switches off). $\overline{RS}$ can be tied to the microprocessor reset pin.
3. Extended Signal Range:
   The enhanced LC^2MOS processing results in a high breakdown and an increased analog signal range of V_{SS} to V_{DD}.
4. Break-Before-Make Switching:
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
5. Low Leakage:
   Leakage currents in the range of 20pA make these multiplexers suitable for high precision circuits.

ADG526A/ADG527A—SPECIFICATIONS

Dual Supply (V_{DD} = +10.8V to +16.5V, V_{SS} = −10.8V to −16.5V unless otherwise noted.)

Parameter	ADG526A ADG527A K Version +25°C	ADG526A ADG527A K Version −40°C to +85°C	ADG526A ADG527A B Version +25°C	ADG526A ADG527A B Version −40°C to +85°C	ADG526A ADG527A T Version +25°C	ADG526A ADG527A T Version −55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V min V max	
R_{ON}	280		280		280		Ω typ	−10V≤V_S≤+10V, I_{DS} = 1mA; Test Circuit
	450	600	450	600	450	600	Ω max	
	300	400	300	400			Ω max	V_{DD} = 15V(±10%), V_{SS} = −15V(±10%)
					300	400	Ω max	V_{DD} = 15V(±5%), V_{SS} = −15V(±5%)
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	−10V≤V_S≤+10V, I_{DS} = 1mA
R_{ON} Match	5		5		5		% typ	−10V≤V_S≤+10V, I_{DS} = 1mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 2
	1	50	1	50	1	50	nA max	
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 3
ADG526A	1	200	1	200	1	200	nA max	
ADG527A	1	100	1	100	1	100	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 4
ADG526A	1	200	1	200	1	200	nA max	
ADG527A	1	100	1	100	1	100	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG527A only)		25		25		25	nA max	V1 = ±10V, V2 = ∓10V; Test Circuit 5
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS[1]								
$t_{TRANSITION}$	200		200		200		ns typ	V1 = ±10V, V2 = ∓10V; Test Circuit 6
	300	400	300	400	300	400	ns max	
t_{OPEN}	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON} (EN, $\overline{WR}$)	200		200		200		ns typ	Test Circuits 8 and 9
	300	400	300	400	300	400	ns max	
t_{OFF} (EN, $\overline{RS}$)	200		200		200		ns typ	Test Circuits 8 and 10
	300	400	300	400	300	400	ns max	
t_W Write Pulse Width	100	120	100	120	100	130	ns min	See Figure 1
t_S Address, Enable Setup Time		100		100		100	ns min	See Figure 1
t_H Address, Enable Hold Time		10		10		10	ns min	See Figure 1
t_{RS} Reset Pulse Width		100		100		100	ns min	See Figure 2
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF,
	50		50		50		dB min	V_S = 7V rms, f = 100kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8V
C_D (OFF)								
ADG526A	44		44		44		pF typ	V_{EN} = 0.8V
ADG527A	22		22		22		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 11
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
I_{SS}	20		20		20		μA typ	V_{IN} = V_{INL} or V_{INH}
		0.2		0.2		0.2	mA max	
Power Dissipation	10		10		10		mW typ	
		28		28		28	mW max	

NOTE
[1]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

Single Supply (V_{DD} = +10.8V to +16.5V, V_{SS} = GND = 0V unless otherwise noted.)

Parameter	ADG526A ADG527A K Version +25°C	ADG526A ADG527A K Version −40°C to +85°C	ADG526A ADG527A B Version +25°C	ADG526A ADG527A B Version −40°C to +85°C	ADG526A ADG527A T Version +25°C	ADG526A ADG527A T Version −55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}	500		500		500		Ω typ	0V ≤ V_S ≤ +10V, I_{DS} = 0.5mA; Test Circuit 1
	700	1000	700	1000	700	1000	Ω max	
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	0V ≤ V_S ≤ +10V, I_{DS} = 0.5mA
R_{ON} Match	5		5		5		% typ	0V ≤ V_S ≤ +10V, I_{DS} = 0.5mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = +10V/0V, V2 = 0V/+10V;
	1	50	1	50	1	50	nA max	Test Circuit 2
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = +10V/0V, V2 = 0V/+10V;
ADG526A	1	200	1	200	1	200	nA max	Test Circuit 3
ADG527A	1	100	1	100	1	100	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = +10V/0V, V2 = 0V/+10V;
ADG526A	1	200	1	200	1	200	nA max	Test Circuit 4
ADG527A	1	100	1	100	1	100	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG527A only)		25		25		25	nA max	V1 = +10V/0V, V2 = 0V/+10V; Test Circuit 5
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS[1]								
$t_{TRANSITION}$	300		300		300		ns typ	V1 = +10V/0V, V2 = 0V/+10V;
	450	600	450	600	450	600	ns max	Test Circuit 6
t_{OPEN}	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON} (EN, $\overline{WR}$)	250		250		250		ns typ	Test Circuits 8 and 9
	450	600	450	600	450	600	ns max	
t_{OFF} (EN, $\overline{RS}$)	250		250		250		ns typ	Test Circuits 8 and 10
	450	600	450	600	450	600	ns max	
t_W Write Pulse Width	100	120	100	120	100	130	ns min	See Figure 1
t_S Address, Enable Setup Time		100		100		100	ns min	See Figure 1
t_H Address, Enable Hold Time		10		10		10	ns min	See Figure 1
t_{RS} Reset Pulse Width		100		100		100	ns min	See Figure 2
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF,
	50		50		50		dB min	V_S = 3.5V rms, f = 100kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8V
C_D (OFF)								
ADG526A	44		44		44		pF typ	V_{EN} = 0.8V
ADG527A	22		22		22		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 11
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
Power Dissipation	11		11		11		mW typ	
		25		25		25	mW max	

NOTE
[1]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

5

TIMING DIAGRAMS

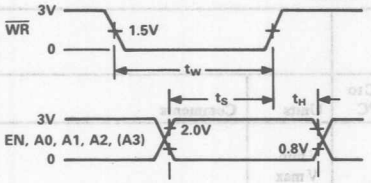


Figure 1.

Figure 1 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while $\overline{WR}$ is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of $\overline{WR}$.

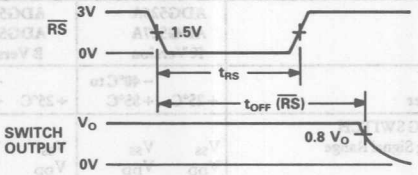


Figure 2.

Figure 2 shows the Reset Pulse Width, t_{RS}, and Reset Turn-off Time, t_{OFF} ($\overline{RS}$).

Note: All digital input signals rise and fall times measured from 10% to 90% of 3V. $t_R = t_F = 20ns$.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS}	44V
V_{DD} to GND	25V
V_{SS} to GND	−25V
Analog Inputs[1]	
Voltage at S, D	V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First
Continuous Current, S or D	20mA
Pulsed Current S or D	
1ms Duration, 10% Duty Cycle	40mA
Digital Inputs[1]	
Voltage at A, EN, $\overline{WR}$, $\overline{RS}$	V_{SS} −4V to V_{DD} +4V or 20mA, Whichever Occurs First
Power Dissipation (Any Package)	
Up to +75°C	470mW
Derates above +75°C by	6mW/°C
Operating Temperature	
Commerical (K Version)	−40°C to +85°C
Industrial (B Version)	−40°C to +85°C
Extended (T Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

NOTE

[1]Overvoltage at A, EN, $\overline{WR}$, $\overline{RS}$, S or D will be clamped by diodes. Current should be limited to the maximum rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG526AKN	−40°C to +85°C	N-28
ADG526AKR	−40°C to +85°C	R-28
ADG526AKP	−40°C to +85°C	P-28A
ADG526ABQ	−40°C to +85°C	Q-28
ADG526ATQ[3]	−55°C to +125°C	Q-28
ADG526ATE[3]	−55°C to +125°C	E-28A
ADG527AKN	−40°C to +85°C	N-28
ADG527AKR	−40°C to +85°C	R-28
ADG527AKP	−40°C to +85°C	P-28A
ADG527ABQ	−40°C to +85°C	Q-28
ADG527ATQ[3]	−55°C to +125°C	Q-28
ADG527ATE[3]	−55°C to +125°C	E-28A

NOTES

[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. See Analog Devices Military Products Databook (1990) for military data.

[2]E = Leadless Ceramic Chip Carrier; N = Narrow Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = 0.3" Small Outline IC (SOIC). For outline information see Package Information section.

[3]Standard Military Drawing (SMD) assigned by DESC. SMD numbers are

5962-89710013X (ADG526ATE/883B)
5962-8971001XX (ADG526ATQ/883B)
5962-89710023X (ADG527ATE/883B)
5962-8971002XX (ADG527ATQ/883B)

TRUTH TABLES

A3	A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
X	X	X	X	X	↓	1	Retains Previous Switch Condition
X	X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	X	0	0	1	NONE
0	0	0	0	1	0	1	1
0	0	0	1	1	0	1	2
0	0	1	0	1	0	1	3
0	0	1	1	1	0	1	4
0	1	0	0	1	0	1	5
0	1	0	1	1	0	1	6
0	1	1	0	1	0	1	7
0	1	1	1	1	0	1	8
1	0	0	0	1	0	1	9
1	0	0	1	1	0	1	10
1	0	1	0	1	0	1	11
1	0	1	1	1	0	1	12
1	1	0	0	1	0	1	13
1	1	0	1	1	0	1	14
1	1	1	0	1	0	1	15
1	1	1	1	1	0	1	16

X = Don't Care

ADG526A

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
X	X	X	X	↓	1	Retains Previous Switch Condition
X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

X = Don't Care

ADG527A

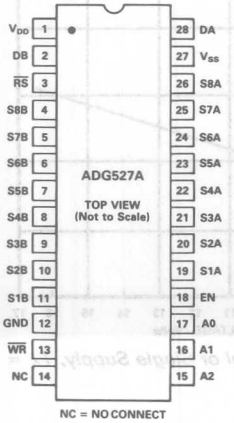
5

PIN CONFIGURATIONS

DIP, SOIC

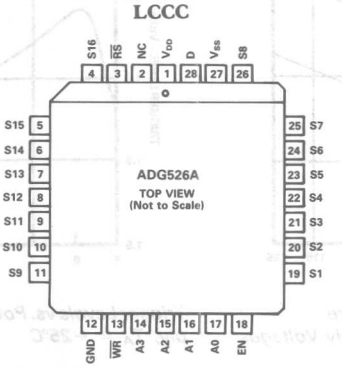


NC = NO CONNECT

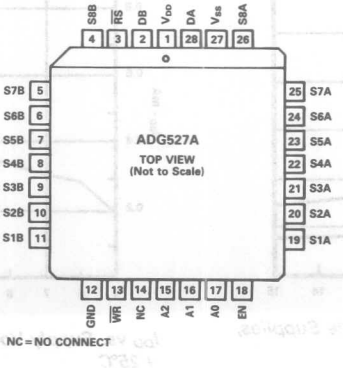


NC = NO CONNECT

LCCC

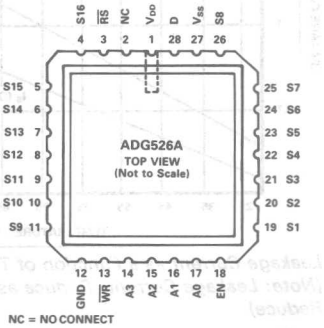


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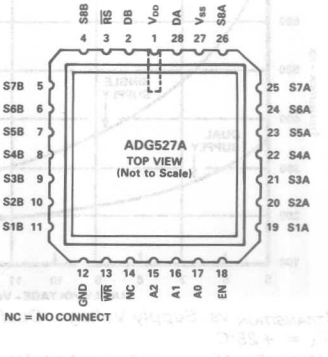


NC = NO CONNECT

PLCC



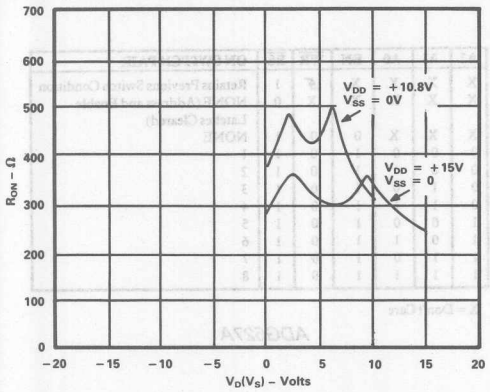
NC = NO CONNECT



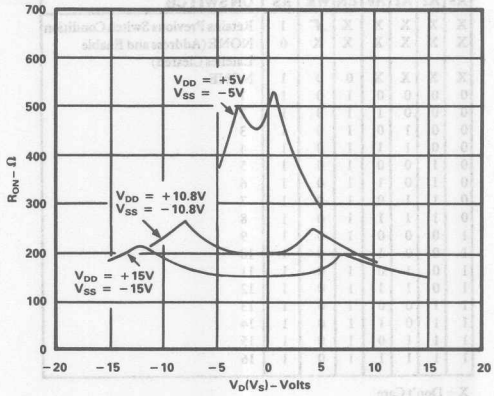
NC = NO CONNECT

Typical Performance Characteristics

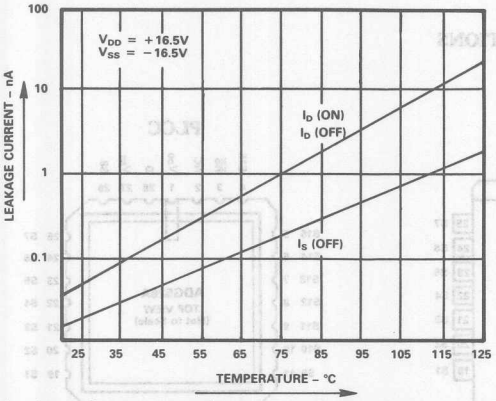
The multiplexers are guaranteed functional with reduced single or dual supplies down to 4.5V.



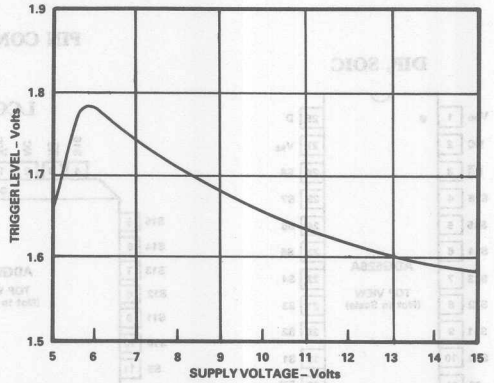
R_{ON} as a Function of $V_D(V_S)$: Dual Supply Voltage, T_A = +25°C



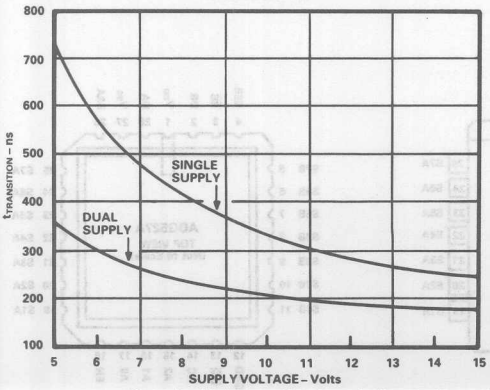
R_{ON} as a Function of $V_D(V_S)$: Single Supply Voltage, T_A = +25°C



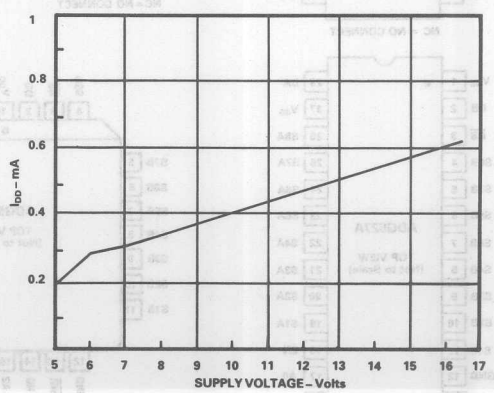
Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)



Trigger Levels vs. Power Supply Voltage, Dual or Single Supply, T_A = +25°C

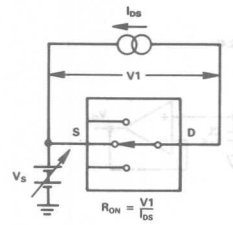


$t_{TRANSITION}$ vs. Supply Voltage: Dual and Single Supplies, T_A = +25°C (Note: For V_{DD} and $|V_{SS}| < 10V$; V1 = V_{DD}/V_{SS}, V2 = V_{SS}/V_{DD}. See Test Circuit 6)

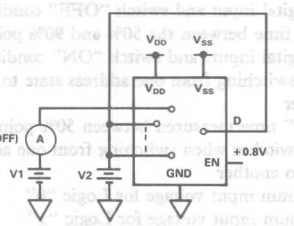


I_{DD} vs. Supply Voltage: Dual or Single Supply, T_A = +25°C

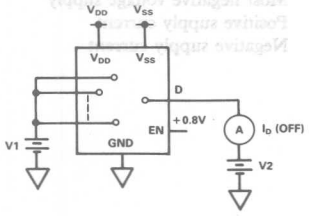
TEST CIRCUIT 1 R_{ON}



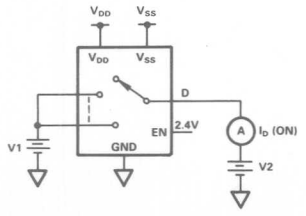
TEST CIRCUIT 2 I_S (OFF)



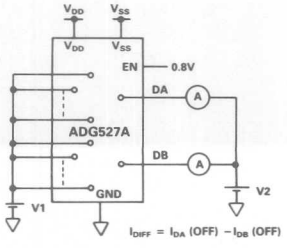
TEST CIRCUIT 3 I_D (OFF)



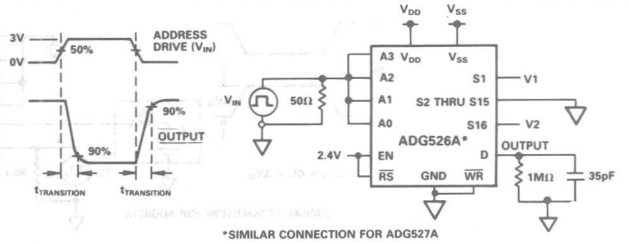
TEST CIRCUIT 4 I_D (ON)



TEST CIRCUIT 5 I_{DIFF}

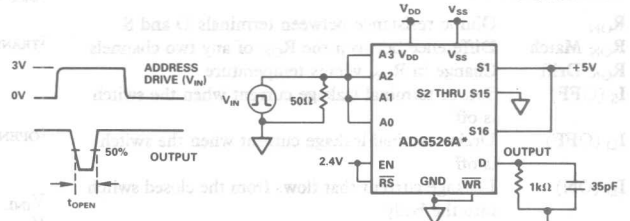


TEST CIRCUIT 6 SWITCHING TIME OF MULTIPLEXER, $t_{TRANSITION}$



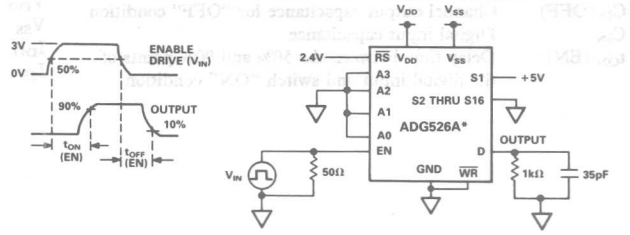
*SIMILAR CONNECTION FOR ADG527A

TEST CIRCUIT 7 BREAK-BEFORE-MAKE DELAY, t_{OPEN}



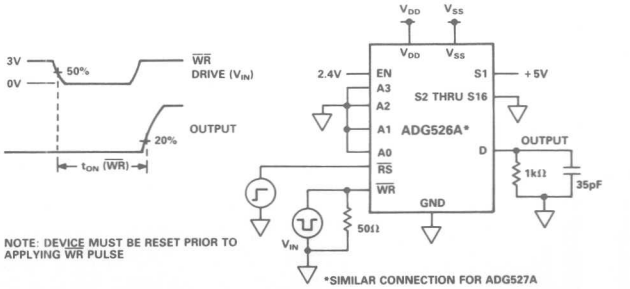
*SIMILAR CONNECTION FOR ADG527A

TEST CIRCUIT 8 ENABLE DELAY, t_{ON} (EN), t_{OFF} (EN)



*SIMILAR CONNECTION FOR ADG527A

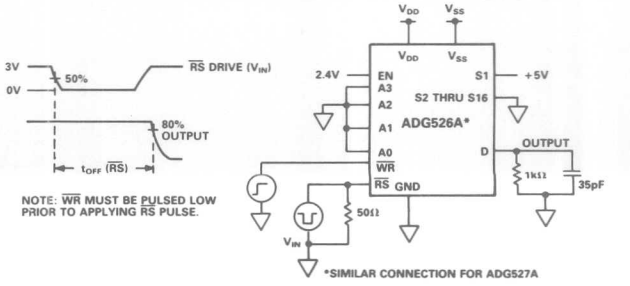
TEST CIRCUIT 9 WRITE TURN-ON TIME, t_{ON} ($\overline{WR}$)



NOTE: DEVICE MUST BE RESET PRIOR TO APPLYING WR PULSE

*SIMILAR CONNECTION FOR ADG527A

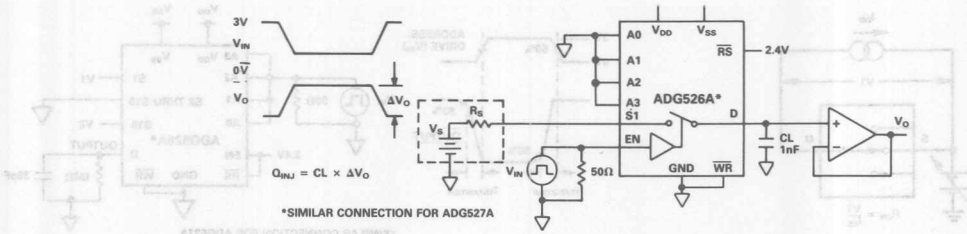
TEST CIRCUIT 10 RESET TURN-OFF TIME, t_{OFF} ($\overline{RS}$)



NOTE: WR MUST BE PULSED LOW PRIOR TO APPLYING RS PULSE.

*SIMILAR CONNECTION FOR ADG527A

5



TERMINOLOGY

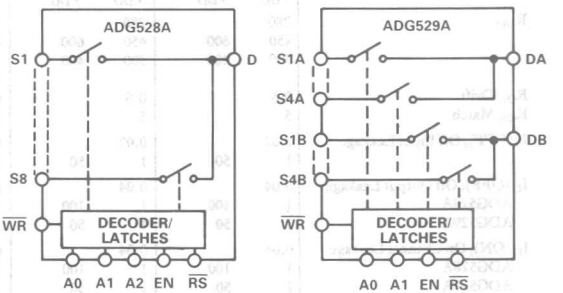
R_{ON}	Ohmic resistance between terminals D and S
R_{ON} Match	Difference between the R_{ON} of any two channels
R_{ON} Drift	Change in R_{ON} versus temperature
I_S (OFF)	Source terminal leakage current when the switch is off
I_D (OFF)	Drain terminal leakage current when the switch is off
I_D (ON)	Leakage current that flows from the closed switch into the body
V_S (V_D)	Analog voltage on terminal S or D
C_S (OFF)	Channel input capacitance for "OFF" condition
C_D (OFF)	Channel output capacitance for "OFF" condition
C_{IN}	Digital input capacitance
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch "ON" condition
t_{OFF} (EN)	Delay time between the 50% and 10% points of the digital input and switch "OFF" condition
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and switch "ON" condition when switching from one address state to another
t_{OPEN}	"OFF" time measured between 50% points of both switches when switching from one address state to another
V_{INL}	Maximum input voltage for Logic "0"
V_{INH}	Minimum input voltage for Logic "1"
I_{INL} (I_{INH})	Input current of the digital input
V_{DD}	Most positive voltage supply
V_{SS}	Most negative voltage supply
I_{DD}	Positive supply current
I_{SS}	Negative supply current

Latched 4/8 Channel Analog Multiplexers

ADG528A/ADG529A

FEATURES
44V Supply Maximum Rating
V_{SS} to V_{DD} Analog Signal Range
Single/Dual Supply Specifications
Wide Supply Ranges (10.8V to 16.5V)
Microprocessor Compatible (100ns $\overline{WR}$ Pulse)
Extended Plastic Temperature Range (−40°C to +85°C)
Low Leakage (20pA typ)
Low Power Dissipation (28mW max)
Available in 16-Lead DIP and 20-Lead LCCC/PLCC Packages
Superior Alternative to:
DG528
DG529

FUNCTIONAL BLOCK DIAGRAMS



5

GENERAL DESCRIPTION

The ADG528A and ADG529A are CMOS monolithic analog multiplexers with 8 channels and dual 4 channels respectively. On-chip latches facilitate microprocessor interfacing. The ADG528A switches one of 8 inputs to a common output depending on the state of three binary addresses and an enable input. The ADG529A switches one of 4 differential inputs to a common differential output depending on the state of two binary addresses and an enable input. Both devices have TTL and 5V CMOS logic compatible digital inputs.

The ADG528A and ADG529A are designed on an enhanced LC^{2}MOS process which gives an increased signal capability of V_{SS} to V_{DD} and enables operation over a wide range of supply voltages. The devices can comfortably operate anywhere in the 10.8V to 16.5V single or dual supply range. These multiplexers also feature high switching speeds and low R_{ON}.

PRODUCT HIGHLIGHTS

1. Single/Dual Supply Specifications with a Wide Tolerance:
   The devices are specified in the 10.8V to 16.5V range for both single and dual supplies.
2. Easily Interfaced:
   The ADG528A and ADG529A can be easily interfaced with microprocessors. The $\overline{WR}$ signal latches the state of the address control lines and the enable line. The $\overline{RS}$ signal clears both the address and enable data in the latches resulting in no output (all switches off). $\overline{RS}$ can be tied to the microprocessor reset pin.
3. Extended Signal Range:
   The enhanced LC^{2}MOS processing results in a high breakdown and an increased analog signal range of V_{SS} to V_{DD}.
4. Break-Before-Make Switching:
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
5. Low Leakage:
   Leakage currents in the range of 20pA make these multiplexers suitable for high precision circuits.

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG528AKN	−40°C to +85°C	N-28
ADG528AKP	−40°C to +85°C	P-20A
ADG528ABQ	−40°C to +85°C	Q-18
ADG528ATQ[3]	−55°C to +125°C	Q-18
ADG528ATE[3]	−55°C to +125°C	E-20A
ADG529AKN	−40°C to +85°C	N-18
ADG529AKP	−40°C to +85°C	P-20A
ADG529ABQ	−40°C to +85°C	Q-18
ADG529ATQ[3]	−55°C to +125°C	Q-18
ADG529ATE[3]	−55°C to +125°C	E-20A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. See Analog Devices Military Products Databook (1990) for military data sheet.
[2]E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information section.

ADG528A/ADG529A—SPECIFICATIONS

Dual Supply (V_{DD} = +10.8V to +16.5V, V_{SS} = −10.8V to −16.5V unless otherwise noted.)

Parameter	ADG528A ADG529A K Version		ADG528A ADG529A B Version		ADG528A ADG529A T Version		Units	Comments
	+25°C	−40°C to +85°C	+25°C	−40°C to +85°C	+25°C	−55°C to +125°C		
ANALOG SWITCH								
Analog Signal Range	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V min V max	
R_{ON}	280		280		280		Ω typ	−10V≤V_S≤+10V, I_{DS} = 1mA; Test Circuit 1
	450	600	450	600	450	600	Ω max	
	300	400	300	400			Ω max	V_{DD} = 15V(±10%), V_{SS} = −15V(±10%)
					300	400	Ω max	V_{DD} = 15V(±5%), V_{SS} = −15V(±5%)
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	−10V≤V_S≤+10V, I_{DS} = 1mA
R_{ON} Match	5		5		5		% typ	−10V≤V_S≤+10V, I_{DS} = 1mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 2
	1	50	1	50	1	50	nA max	
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 3
ADG528A	1	100	1	100	1	100	nA max	
ADG529A	1	50	1	50	1	50	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 4
ADG528A	1	100	1	100	1	100	nA max	
ADG529A	1	50	1	50	1	50	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG529A only)		25		25		25	nA max	V1 = ±10V, V2 = ∓10V; Test Circuit 5
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS[1]								
$t_{TRANSITION}$	200		200		200		ns typ	V1 = ±10V, V2 = ∓10V; Test Circuit 6
	300	400	300	400	300	400	ns max	
t_{OPEN}	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON} (EN, $\overline{WR}$)	200		200		200		ns typ	Test Circuits 8 and 9
	300	400	300	400	300	400	ns max	
t_{OFF} (EN, $\overline{RS}$)	200		200		200		ns typ	Test Circuits 8 and 10
	300	400	300	400	300	400	ns max	
t_W Write Pulse Width	100	120	100	120	100	130	ns min	See Figure 1
t_S Address, Enable Setup Time		100		100		100	ns min	See Figure 1
t_H Address, Enable Hold Time		10		10		10	ns min	See Figure 1
t_{RS} Reset Pulse Width		100		100		100	ns min	See Figure 2
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF,
	50		50		50		dB min	V_S = 7V rms, f = 100kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8V
C_D (OFF)								
ADG528A	22		22		22		pF typ	V_{EN} = 0.8V
ADG529A	11		11		11		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 11
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
I_{SS}	20		20		20		μA typ	V_{IN} = V_{INL} or V_{INH}
		0.2		0.2		0.2	mA max	
Power Dissipation	10		10		10		mW typ	
		28		28		28	mW max	

NOTE
[1]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

Single Supply (V_{DD} = +10.8V to +16.5V, V_{SS} = GND = 0V unless otherwise noted.)

Parameter	ADG528A ADG529A K Version +25°C	ADG528A ADG529A K Version −40°C to +85°C	ADG528A ADG529A B Version +25°C	ADG528A ADG529A B Version −40°C to +85°C	ADG528A ADG529A T Version +25°C	ADG528A ADG529A T Version −55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	GND	GND	GND	GND	GND	GND	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}	500		500		500		Ω typ	GND≤V_S≤+10V, I_{DS} = 0.5mA; Test Circuit 1
	700	1000	700	1000	700	1000	Ω max	
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	GND≤V_S≤+10V, I_{DS} = 0.5mA
R_{ON} Match	5		5		5		% typ	GND≤V_S≤+10V, I_{DS} = 0.5mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = +10V/GND, V2 = GND/+10V
	1	50	1	50	1	50	nA max	Test Circuit 2
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = +10V/GND, V2 = GND/+10V
ADG528A	1	100	1	100	1	100	nA max	Test Circuit 3
ADG529A	1	50	1	50	1	50	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = +10V/GND, V2 = GND/+10V
ADG528A	1	100	1	100	1	100	nA max	Test Circuit 4
ADG529A	1	50	1	50	1	50	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG529A only)		25		25		25	nA max	V1 = +10V/GND, V2 = GND/+10V Test Circuit 5.
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS[1]								
$t_{TRANSITION}$	300		300		300		ns typ	V1 = +10V/GND, V2 = GND/+10V; Test Circuit 6
	450	600	450	600	450	600	ns max	
t_{OPEN}	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON} (EN, $\overline{WR}$)	250		250		250		ns typ	Test Circuits 8 and 9
	450	600	450	600	450	600	ns max	
t_{OFF} (EN, $\overline{RS}$)	250		250		250		ns typ	Test Circuits 8 and 10
	450	600	450	600	450	600	ns max	
t_W Write Pulse Width	100	120	100	120	100	130	ns min	See Figure 1
t_S Address, Enable Setup Time		100		100		100	ns min	See Figure 1
t_H Address, Enable Hold Time		10		10		10	ns min	See Figure 1
t_{RS} Reset Pulse Width		100		100		100	ns min	See Figure 2
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF,
	50		50		50		dB min	V_S = 3.5V rms, f = 100kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8V
C_D (OFF)								
ADG528A	22		22		22		pF typ	V_{EN} = 0.8V
ADG529A	11		11		11		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 11
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
Power Dissipation	11		11		11		mW typ	
		25		25		25	mW max	

NOTE
[1]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

5

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS}	44V
V_{DD} to GND	25V
V_{SS} to GND	−25V
Analog Inputs[1]	
Voltage at S, D	V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First
Continuous Current, S or D	20mA
Pulsed Current S or D	
1ms Duration, 10% Duty Cycle	40mA
Digital Inputs[1]	
Voltage at A, EN, $\overline{WR}$, $\overline{RS}$	V_{SS} −4V to V_{DD} +4V or 20mA, Whichever Occurs First
Power Dissipation (Any Package)	
Up to +75°C	470mW
Derates above +75°C by	6mW/°C
Operating Temperature	
Commerical (K Version)	−40°C to +85°C
Industrial (B Version)	−40°C to +85°C
Extended (T Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

NOTE
[1]Overvoltage at A, EN, $\overline{WR}$, $\overline{RS}$, S or D will be clamped by diodes. Current should be limited to the maximum rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

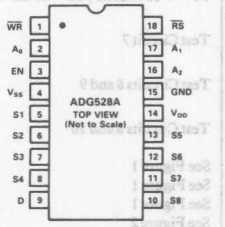
CAUTION

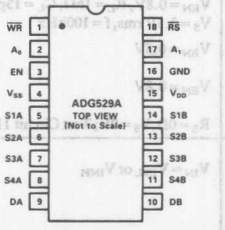
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



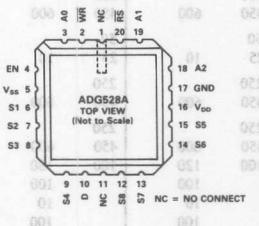
PIN CONFIGURATIONS

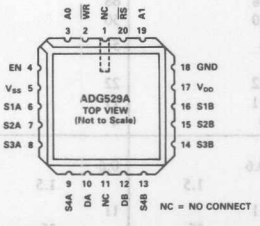
DIP



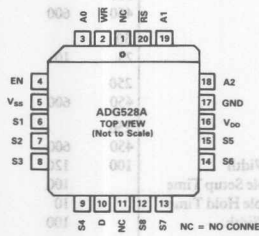


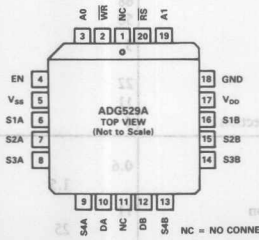
LCCC





PLCC





TRUTH TABLES

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
X	X	X	X	↓	1	Retains Previous Switch Condition
X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

X = Don't Care *ADG528A*

A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
X	X	X	↓	1	Retains Previous Switch Condition
X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

X = Don't Care *ADG529A*

TIMING DIAGRAMS

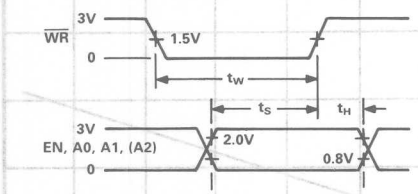


Figure 1

Figure 1 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while $\overline{WR}$ is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of $\overline{WR}$.

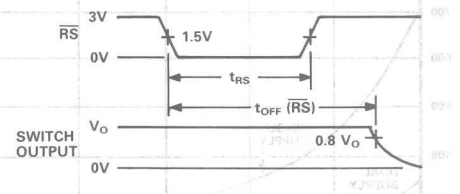


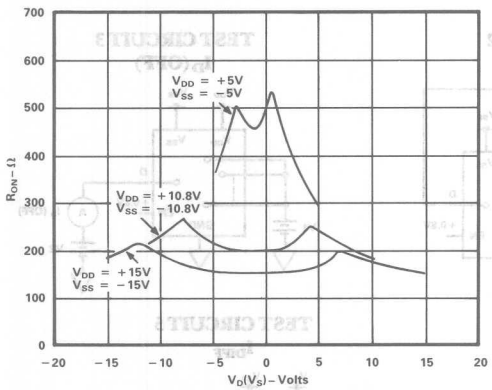
Figure 2

Figure 2 shows the Reset Pulse Width, t_{RS}, and Reset Turn-off Time, t_{OFF} ($\overline{RS}$).

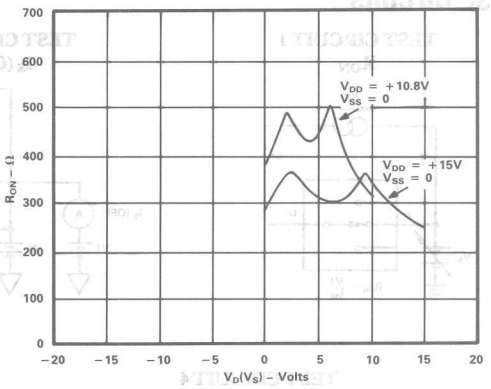
Note: All digital input signals rise and fall times measured from 10% to 90% of 3V. $t_R = t_F = 20ns$.

Typical Performance Characteristics

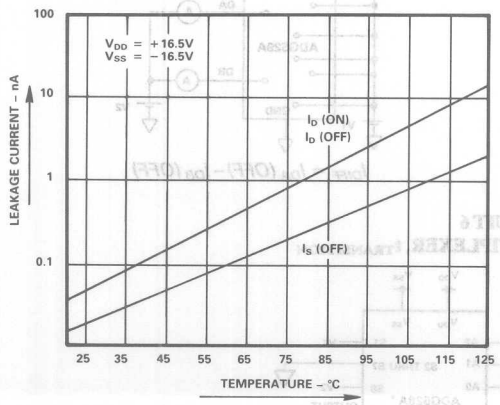
The multiplexers are guaranteed functional with reduced single or dual supplies down to 4.5V.



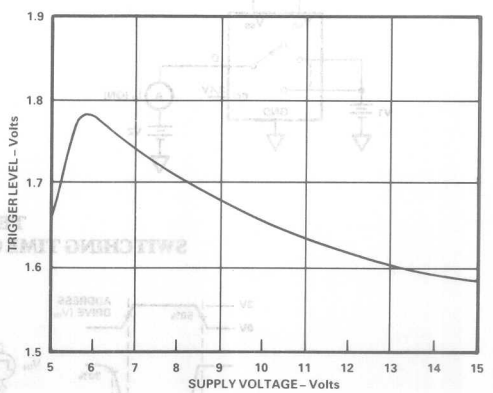
R_{ON} as a Function of $V_D(V_S)$: Dual Supply Voltage, T_A = +25°C



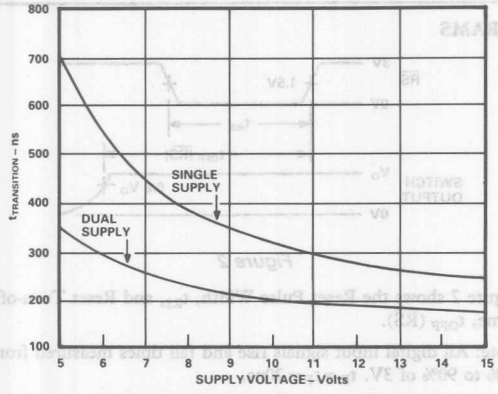
R_{ON} as a Function of $V_D(V_S)$: Single Supply Voltage, T_A = +25°C



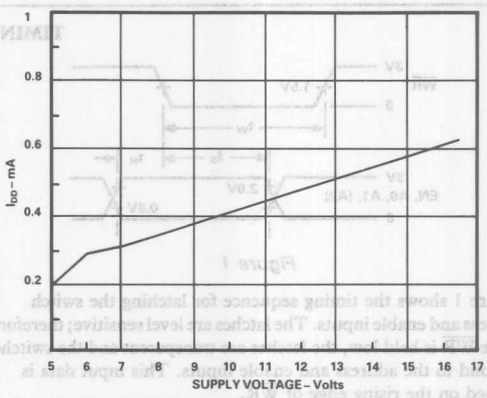
Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)



Trigger Levels vs. Power Supply Voltage, Dual or Single Supply, T_A = +25°C



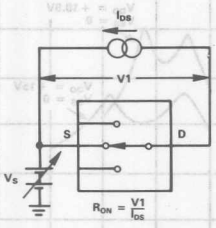
$t_{TRANSITION}$ vs. Supply Voltage: Dual and Single Supplies, T_A = +25°C
(Note: For V_{DD} and $|V_{SS}|$ < 10V; V1 = V_{DD}/V_{SS}, V2 = V_{SS}/V_{DD}. See Test Circuit 6)



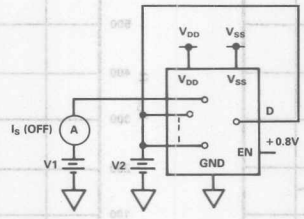
I_{DD} vs. Supply Voltage: Dual or Single Supply, T_A = +25°C

Test Circuits

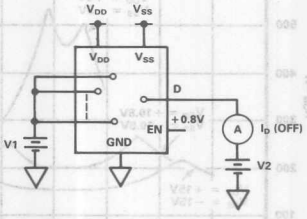
TEST CIRCUIT 1
R_{ON}



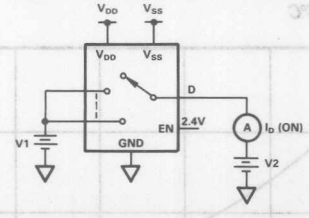
TEST CIRCUIT 2
I_S (OFF)



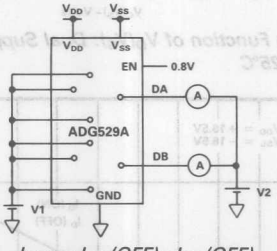
TEST CIRCUIT 3
I_D (OFF)



TEST CIRCUIT 4
I_D (ON)

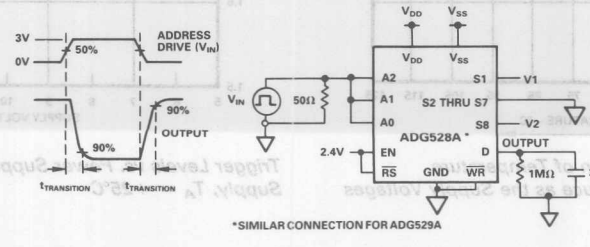


TEST CIRCUIT 5
I_{DIFF}



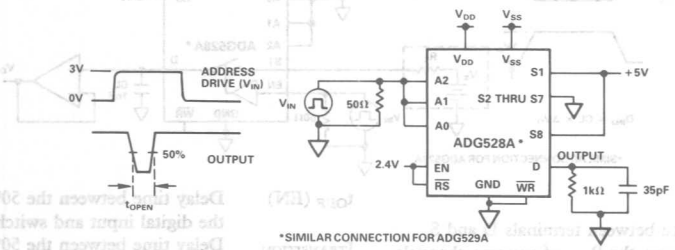
$I_{DIFF} = I_{DA}$ (OFF) – I_{DB} (OFF)

TEST CIRCUIT 6
SWITCHING TIME OF MULTIPLEXER, $t_{TRANSITION}$



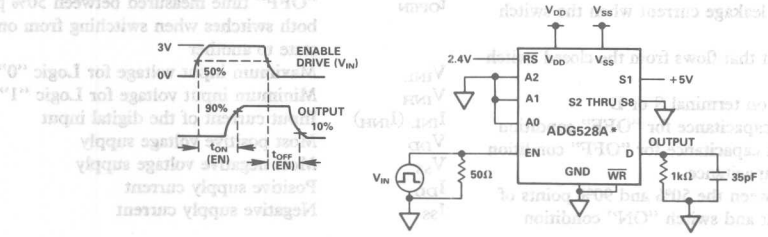
*SIMILAR CONNECTION FOR ADG529A

TEST CIRCUIT 7
BREAK-BEFORE-MAKE DELAY, t_{OPEN}



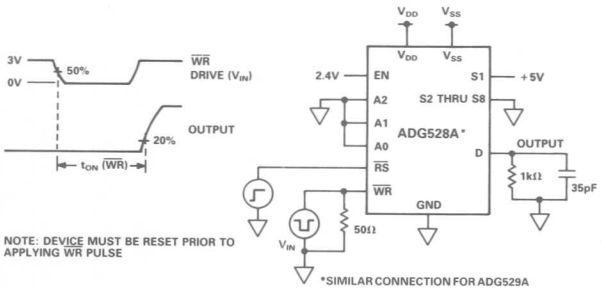
*SIMILAR CONNECTION FOR ADG529A

TEST CIRCUIT 8
ENABLE DELAY, t_{ON} (EN), t_{OFF} (EN)



*SIMILAR CONNECTION FOR ADG529A

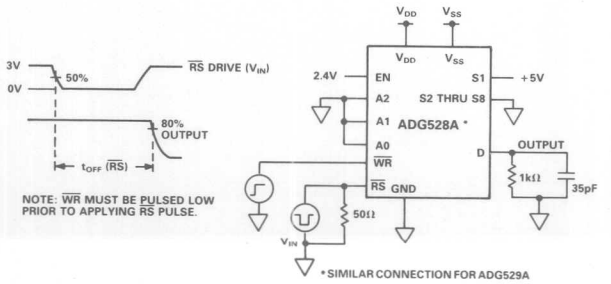
TEST CIRCUIT 9
WRITE TURN-ON TIME, t_{ON} ($\overline{WR}$)



NOTE: DEVICE MUST BE RESET PRIOR TO APPLYING WR PULSE

*SIMILAR CONNECTION FOR ADG529A

TEST CIRCUIT 10
RESET TURN-OFF TIME, t_{OFF} ($\overline{RS}$)

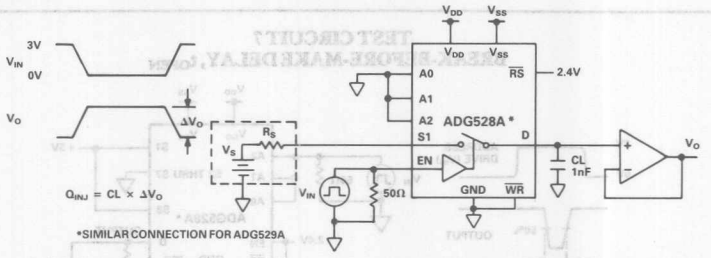


NOTE: WR MUST BE PULSED LOW PRIOR TO APPLYING RS PULSE.

*SIMILAR CONNECTION FOR ADG529A

5

TEST CIRCUIT 11
CHARGE INJECTION



TERMINOLOGY

R_{ON}	Ohmic resistance between terminals D and S
R_{ON} Match	Difference between the R_{ON} of any two channels
R_{ON} Drift	Change in R_{ON} versus temperature
I_S (OFF)	Source terminal leakage current when the switch is off
I_D (OFF)	Drain terminal leakage current when the switch is off
I_D (ON)	Leakage current that flows from the closed switch into the body
V_S (V_D)	Analog voltage on terminal S or D
C_S (OFF)	Channel input capacitance for "OFF" condition
C_D (OFF)	Channel output capacitance for "OFF" condition
C_{IN}	Digital input capacitance
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch "ON" condition
t_{OFF} (EN)	Delay time between the 50% and 10% points of the digital input and switch "OFF" condition
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and switch "ON" condition when switching from one address state to another
t_{OPEN}	"OFF" time measured between 50% points of both switches when switching from one address state to another
V_{INL}	Maximum input voltage for Logic "0"
V_{INH}	Minimum input voltage for Logic "1"
I_{INL} (I_{INH})	Input current of the digital input
V_{DD}	Most positive voltage supply
V_{SS}	Most negative voltage supply
I_{DD}	Positive supply current
I_{SS}	Negative supply current

8-Chan/Dual 4-Chan JFET Analog Multiplexers (Overvoltage & Power Supply Loss Protected)

MUX-08/MUX-24

FEATURES

- JFET Switches Rather Than CMOS
- Low "ON" Resistance ..... 220Ω Typ
- Highly Resistant to Static Discharge Damage
- No SCR Latch-Up Problems
- Digital Inputs Compatible With TTL and CMOS
- 125°C Temperature Tested Dice Available
- MUX-08 Pin Compatible With DG508, HI-508A, IH5108, IH6108, LF11508/12508/13508, AD7506
- MUX-24 Pin Compatible With DG509, HI-509A, IH5208, IH6208, LF11509/12509/13509, AD7507
- Available in Surface Mount Packages
- Available in Die Form

ORDERING INFORMATION †

25°C ON RESISTANCE	PACKAGE: CERDIP 16-PIN	PACKAGE: PLASTIC 16-PIN	PACKAGE: LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
220Ω	MUX08AQ*	–	–	MIL
	MUX08EQ	–	–	IND
	–	MUX08EP	–	COM
300Ω	MUXO8BQ*	–	MUX08BRC/883	MIL
	MUX08FQ	–	–	IND
	–	MUX08FP	–	XIND
	–	MUX08FS††	–	XIND
220Ω	MUX24AQ*	–	–	MIL
	MUX24EQ	–	–	IND
	–	MUX24EP	–	COM
300Ω	MUX24BQ*	–	–	MIL
	MUX24FQ	–	–	IND
	–	MUX24FP	–	XIND
	–	MUX24FS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The MUX-08 is a monolithic eight-channel analog multiplexer which connects a single output to one of the eight analog inputs depending upon the state of a 3-bit binary address.

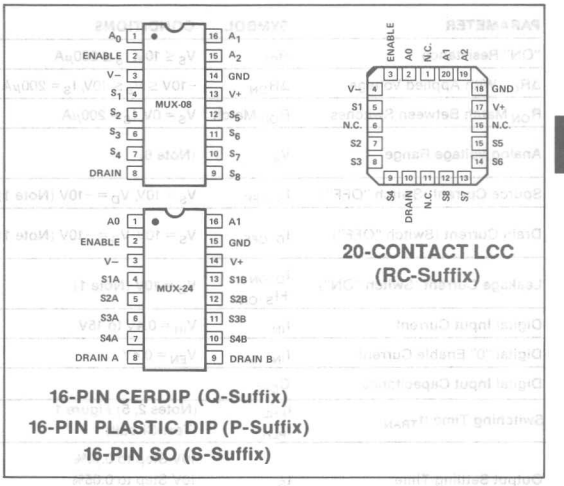
The MUX-24 is a monolithic four-channel differential analog multiplexer configured in a double pole, four-position (plus OFF) electronic switch array. A two-bit binary input address connects a pair of independent analog inputs from each four-channel input section to the corresponding pair of independent analog outputs.

All switches in the MUX-08/MUX-24 are turned OFF by applying logic "0" to the ENABLE pin, thereby providing a package select function.

Fabricated with Precision Monolithics' high performance Bipolar-JFET technology, these devices offer low, constant "ON" resistance, low leakage currents and fast settling time with low crosstalk to satisfy a wide variety of applications. These multiplexers do not suffer from latch-up or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors over the full operating temperature range.

For single sixteen-channel and dual eight-channel models, refer to the MUX-16/MUX-28 data sheet.

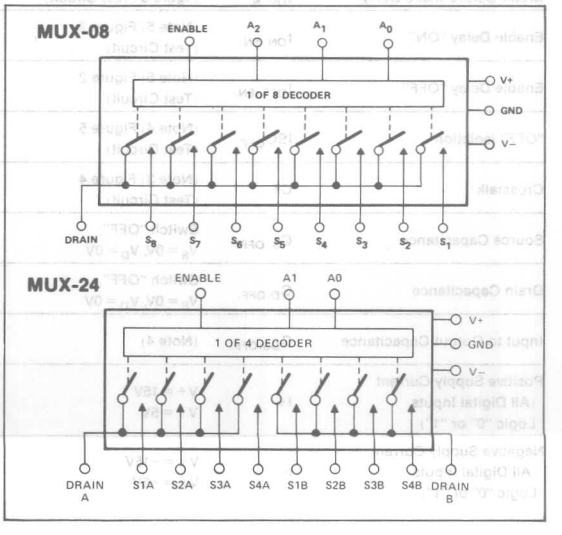
PIN CONNECTIONS



20-CONTACT LCC (RC-Suffix)

16-PIN CERDIP (Q-Suffix)
16-PIN PLASTIC DIP (P-Suffix)
16-PIN SO (S-Suffix)

FUNCTIONAL DIAGRAMS



ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature Range
- MUX-08/24-AQ, BQ, BRC ..... –55°C to +125°C
- MUX-02/24-EQ, FQ ..... –25°C to +85°C
- MUX-08/24-EP ..... 0°C to +70°C
- MUX-08/24-FP, FS ..... –40°C to +85°C

Junction Temperature (T_J) ..... –65°C to +150°C
Storage Temperature Range ..... –65°C to +150°C
- P-Suffix ..... –65°C to +125°C

Lead Temperature (Soldering, 60 sec) ..... 300°C
Maximum Junction Temperature ..... 150°C
V+ Supply to V– Supply 36V
Logic Input Voltage ..... (–4V or V–) to V+ Supply
Analog Input Voltage ..... V– Supply –20V to V+ Supply +20V
Maximum Current Through Any Pin 25mA

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin Plastic DIP (P)	82	39	°C/W
20-Contact LCC (RC)	98	38	°C/W
16-Pin SO (S)	111	35	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V+ = +15V, V– = –15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		MUX-08A/E MUX-24A/E MIN	TYP	MAX	MUX-08B/F MUX-24B/F MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_S \le 10V$, $I_S \le 200\mu A$		—	220	300	—	300	400	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_S \le 10V$, $I_S = 200\mu A$		—	1	5	—	3	7	%
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V$, $I_S = 200\mu A$		—	7	15	—	9	20	%
Analog Voltage Range	V_A	(Note 6)		+10 –10	+10.4 –15	— —	+10 –10	+10.4 –15	— —	V
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)		—	0.01	1.0	—	0.01	2.0	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)	MUX-08 MUX-24	— —	0.1 0.05	1.0 1.0	— —	0.1 0.05	2.0 2.0	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$ $+I_{S(ON)}$	$V_D = 10V$ (Note 1)	MUX-08 MUX-24	— —	0.1 0.05	1.0 1.0	— —	0.1 0.05	2.0 2.0	nA
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V		—	1	10	—	1	10	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$		—	4	10	—	4	10	μA
Digital Input Capacitance	C_{DIG}			—	3	—	—	3	—	pF
Switching Time (t_{TRAN})	t_{PHL} t_{PLH}	(Notes 2, 5) Figure 1 (Test Circuit)		— —	1.5 1.0	2.1 1.3	— —	1.5 1.0	2.1 1.3	μs
Output Settling Time	t_S	10V Step to 0.10% 10V Step to 0.05% 10V Step to 0.02%		— — —	2.2 2.7 3.4	— — —	— — —	2.2 2.7 3.4	— — —	μs
Break-Before-Make Delay	t_{OPEN}	Figure 3 (Test Circuit)		—	0.8	—	—	1.0	—	μs
Enable Delay "ON"	$t_{ON(EN)}$	(Note 5) Figure 2 (Test Circuit)		—	1	2	—	1	2	μs
Enable Delay "OFF"	$t_{OFF(EN)}$	(Note 5) Figure 2 (Test Circuit)	MUX-08 MUX-24	— —	0.1 0.2	0.4 0.5	— —	0.2 0.3	0.4 0.6	μs
"OFF" Isolation	ISO_{OFF}	(Note 4) Figure 5 (Test Circuit)	MUX-08 MUX-24	— —	60 66	— —	— —	60 66	— —	dB
Crosstalk	CT	(Note 3) Figure 4 (Test Circuit)	MUX-08 MUX-24	— —	70 76	— —	— —	70 76	— —	dB
Source Capacitance	$C_{S(OFF)}$	Switch "OFF", $V_S = 0V$, $V_D = 0V$	MUX-08 MUX-24	— —	2.5 2	— —	— —	2.5 2	— —	pF
Drain Capacitance	$C_{D(OFF)}$	Switch "OFF", $V_S = 0V$, $V_D = 0V$	MUX-08 MUX-24	— —	7 4	— —	— —	7 4	— —	pF
Input to Output Capacitance	$C_{DS(OFF)}$	(Note 4)	MUX-08 MUX-24	— —	0.3 0.15	— —	— —	0.3 0.15	— —	pF
Positive Supply Current (All Digital Inputs Logic "0" or "1")	I+	V+ = 15V V+ = 5V		— —	10 8	12 —	— —	6 5	12 —	mA
Negative Supply Current (All Digital Inputs Logic "0" or "1")	I–	V+ = –15V V+ = –5V		— —	3.0 2.5	3.8 —	— —	2.0 1.8	3.8 —	mA

ELECTRICAL CHARACTERISTICS at V+ = 15V, V− = −15V and −55°C ≤ T_A ≤ 125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		MUX-08A/ MUX-24A MIN	TYP	MAX	MUX-08B/ MUX-24B MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_S \leq 10V$, $I_S \leq 200\mu A$		—	—	400	—	—	500	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V$, $I_S = 200\mu A$		—	1.5	—	—	4.5	—	%
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V$, $I_S = 200\mu A$		—	10	—	—	15	—	%
Analog Voltage Range	V_A	(Note 6)		+10 −10	+10.4 −15	— —	+10 −10	+10.4 −15	— —	V
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Notes 1, 7)		—	—	25	—	—	50	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Notes 1, 7)	MUX-08 MUX-24	— —	— —	100 50	— —	— —	500 500	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$ $+I_{S(ON)}$	$V_D = 10V$ (Notes 1, 7)	MUX-08 MUX-24	— —	— —	100 50	— —	— —	500 500	nA
Digital "1" Input Voltage	V_{INH}	(Note 6)		2	—	—	2	—	—	V
Digital "0" Input Voltage	V_{INL}	(Note 6)		—	—	0.7	—	—	0.7	V
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V		—	—	20	—	—	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$		—	—	20	—	—	20	μA
Positive Supply Current	I+	All Digital Inputs Logic "0" or "1"		—	—	15	—	—	15	mA
Negative Supply Current	I−	All Digital Inputs Logic "0" or "1"		—	—	5	—	—	5	mA

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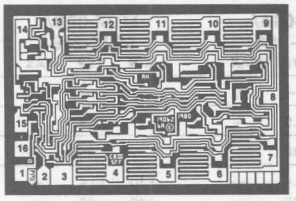
ELECTRICAL CHARACTERISTICS at V+ = 15V, V− = −15V and −25°C ≤ T_A +85°C for MUX-08EQ/FQ and MUX-24EQ/FQ; 0°C ≤ T_A ≤ +70°C for MUX-08EP and MUX-24EP; −40°C ≤ T_A ≤ +85°C for MUX-08FP/FS and MUX-24FP/FS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		MUX-08E/ MUX-24E MIN	TYP	MAX	MUX-08F/ MUX-24F MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_S \leq 10V$, $I_S \leq 200\mu A$		—	—	400	—	—	500	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V$, $I_S = 200\mu A$		—	1.5	—	—	4.5	—	%
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V$, $I_S = 200\mu A$		—	10	—	—	15	—	%
Analog Voltage Range	V_A	(Note 6)		+10 −10	+10.4 −15	— —	+10 −10	+10.4 −15	— —	V
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Notes 1, 7)		—	—	10	—	—	10	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Notes 1, 7)	MUX-08 MUX-24	— —	— —	100 50	— —	— —	100 50	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$ $+I_{S(ON)}$	$V_D = 10V$ (Notes 1, 7)	MUX-08 MUX-24	— —	— —	100 50	— —	— —	100 50	nA
Digital "1" Input Voltage	V_{INH}	(Note 6)		2	—	—	2	—	—	V
Digital "0" Input Voltage	V_{INL}	(Note 6)		—	—	0.8	—	—	0.8	V
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V		—	—	20	—	—	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$		—	—	20	—	—	20	μA
Positive Supply Current	I+	All Digital Inputs Logic "0" or "1"		—	—	15	—	—	15	mA
Negative Supply Current	I−	All Digital Inputs Logic "0" or "1"		—	—	5	—	—	5	mA

NOTES:

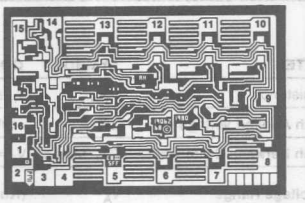
1. Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON".
2. $R_L = 10M\Omega$, $C_L = 10pF$.
3. Crosstalk is measured by driving channel 8 with channel 4 "ON". $R_L = 1M\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 500kHz.
4. "OFF" isolation is measured by driving channel 8 with ALL channels "OFF". $R_L = 1k\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, f = 500kHz. C_{DS} is computed from the OFF isolation measurement.
5. Sample tested.
6. Guaranteed by leakage current and R_{ON} tests.
7. Leakage tests are performed only on military temperature grades at 125°C.

DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



MUX-08

DIE SIZE 0.093 × 0.059 inch, 5487 sq. mils
(2.362 × 1.500 mm, 3543 sq. mm)



MUX-24

MUX-08		MUX-24	
1. A0	9. S8	1. A0	9. DRAIN B
2. ENABLE	10. S7	2. ENABLE	10. S4 B
3. V− (SUBSTRATE)	11. S6	3. V− (SUBSTRATE)	11. S3 B
4. S1	12. S5	4. S1 A	12. S2 B
5. S2	13. V+	5. S2 A	13. S1 B
6. S3	14. GND	6. S3 A	14. V+
7. S4	15. A2	7. S4 A	15. GND
8. DRAIN	16. A1	8. DRAIN A	16. A1

WAFER TEST LIMITS at V+ = 15V, V− = −15V, T_A = 25°C, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MUX-08/ MUX-24NT LIMIT	MUX-08/ MUX-24N LIMIT	MUX-08/ MUX-24G LIMIT	UNITS
"ON" Resistance	R_{ON}	V_S = 0V, I_S = 200μA	T_A = 125°C	300 400	300 —	400 —	Ω MAX
Digital "1" Input Voltage	V_{INH}	(Note 2)		2	2	2	V MIN
Digital "0" Input Voltage	V_{INL}	(Note 2)		0.8	0.8	0.8	V MAX
Digital "0" Input Current	I_{INL}	V_{IN} = 0.4V	T_A = 125°C	10 20	10 —	10 —	μA MAX
Digital "0" Enable Current	I_{INL-EN}	V_{IN} = 0.4V	T_A = 125°C	10 20	10 —	10 —	μA MAX
Positive Supply Current (All Digital Inputs Logic "0")	I+		T_A = 125°C	12 15	12 —	12 —	mA MAX
Negative Supply Current (All Digital Inputs Logic "0")	I−		T_A = 125°C	3.8 5	3.8 —	3.8 —	mA MAX
Analog Input Range	V_A	(Note 2)		±10	±10	±10	V MIN

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly mehtods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V+ = 15V, V− = −15V and T_A = 25°C for MUX-08/24N & G, T_A = 125°C for MUX-08/24NT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-08/ MUX-24NT TYPICAL	MUX-08/ MUX-24N TYPICAL	MUX-08/ MUX-24G TYPICAL	UNITS
Switching Time (t_{TRAN})	t_{PHL} t_{PLH}	(Note 1)	1.7 1.1	1.3 0.9	2.1 1.3	μs
Output Settling Time	t_S	10V Step to 0.1% (Note 1)	2.1	1.5	1.9	μs
Break-Before-Make Delay	t_{OPEN}	(Note 1)	0.8	0.8	1.0	μs
Crosstalk	CT	(Note 1)	70	70	70	dB
ΔR_{ON} With Applied Voltage	ΔR_{ON}	−10V ≤ V_S ≤ 10V, I_S = 200μA	2	2	6	%
Leakage Current (Switch "ON")	$I_{D(ON)}$	V_D = 10V (Note 1)	20	0.5	0.5	nA
Analog Input Range	V_A		+10.4/−15	+10.4/−15	+10.4/−15	V

NOTES:
1. The data shown is extrapolated from measurements made on the packaged devices.
2. Guaranteed by leakage current and R_{ON} tests.

MUX-08 LOGIC STATE

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

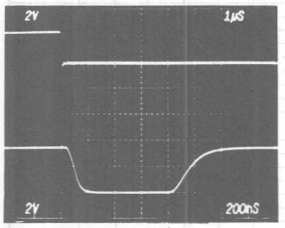
MUX-24 LOGIC STATE

A_1	A_0	EN	"ON" CHANNEL
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

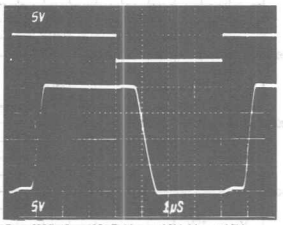
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MUX-08 BREAK-BEFORE-MAKE SWITCHING



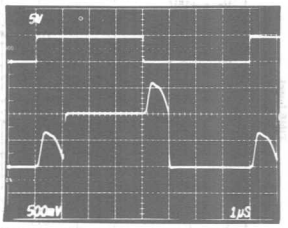
R_L = 1kΩ, C_L = 10pF, $V_{1,8}$ = 10V
VOLTAGE = 2V/DIV
TIME = 200ns/DIV

MUX-08 LARGE-SIGNAL SWITCHING



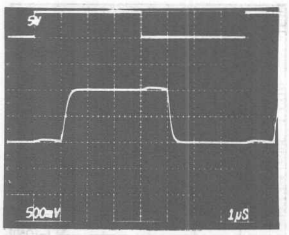
R_L = 1MΩ, C_L = 10pF, V_1 = –10V, V_8 = +10V
VOLTAGE = 5V/DIV
TIME = 1μs/DIV

MUX-08 SMALL-SIGNAL SWITCHING



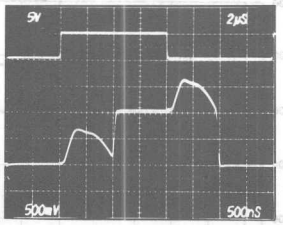
R_L = 1MΩ, C_L = 10pF, V_1 = –500mV, V_8 = +500mV
VOLTAGE = 500mV/DIV
TIME = 1μs/DIV

MUX-08 SMALL-SIGNAL SWITCHING WITH FILTERING



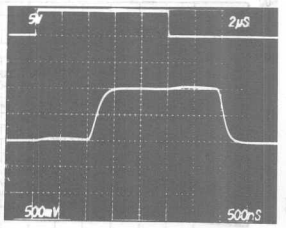
R_L = 1MΩ, C_L = 500pF, V_1 = 500mV, V_8 = +500mV
VOLTAGE = 500mV/DIV
TIME = 1μs/DIV

MUX-08 SMALL-SIGNAL SWITCHING WITH 2μs SAMPLE TIME



R_L = 1MΩ, C_L = 10pF, V_1 = –500mV, V_8 = +500mV
VOLTAGE = 500mV/DIV
TIME = 500ns/DIV

MUX-08 SMALL-SIGNAL SWITCHING WITH FILTERING AND 2.5μs SAMPLE TIME

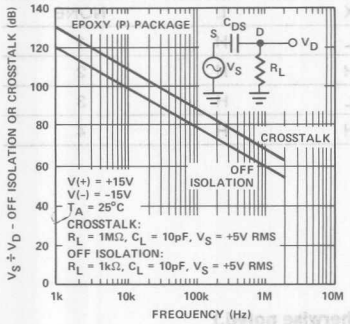


R_L = 1MΩ, C_L = 500pF, V_1 = –500mV, V_8 = +500mV
VOLTAGE = 500mV/DIV
TIME = 500ns/DIV

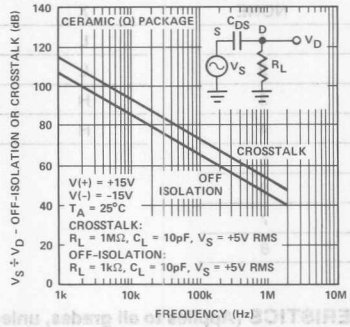
NOTE:
Top waveforms: Digital Input 5V/DIV
Bottom waveforms: Multiplexer Output

TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

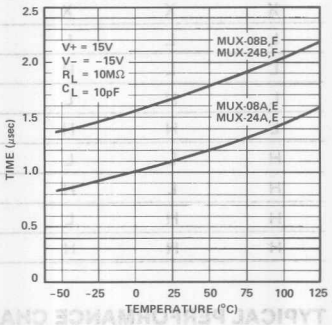
MUX-08 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 8



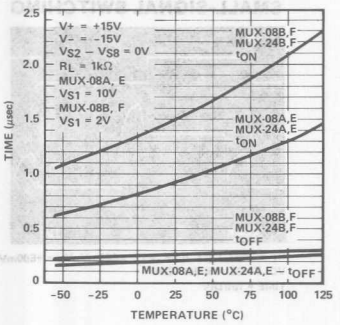
MUX-08 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 8



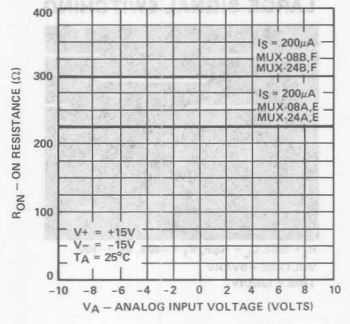
TRANSITION TIMES vs TEMPERATURE



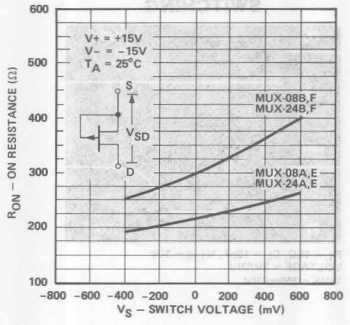
ENABLE DELAY TIMES vs TEMPERATURE



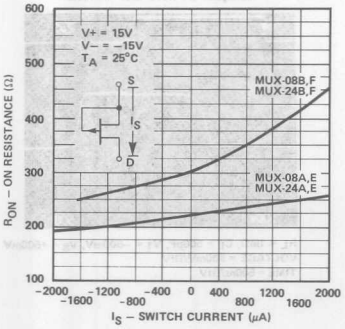
"ON" RESISTANCE (R_{ON}) vs ANALOG VOLTAGE (V_A)



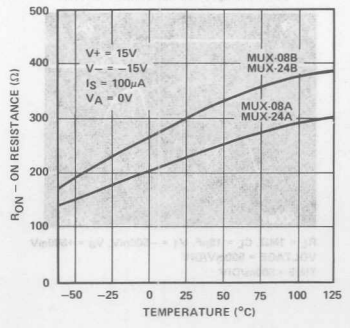
R_{ON} vs SWITCH VOLTAGE (V_{SD})



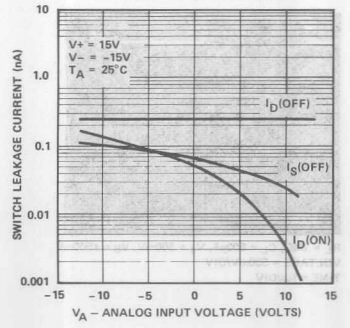
R_{ON} vs SWITCH CURRENT (I_S)



R_{ON} vs TEMPERATURE

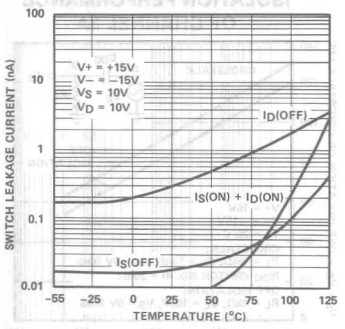


SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE

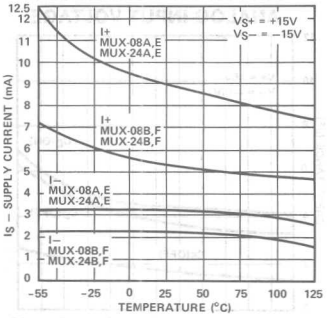


TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

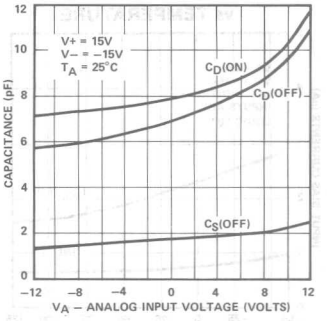
SWITCH LEAKAGE CURRENTS vs TEMPERATURE



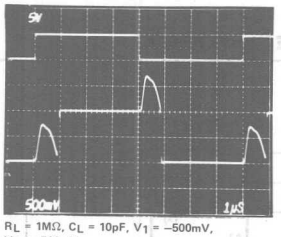
SUPPLY CURRENTS vs TEMPERATURE



MUX-08 SWITCH CAPACITANCES vs ANALOG INPUT VOLTAGE

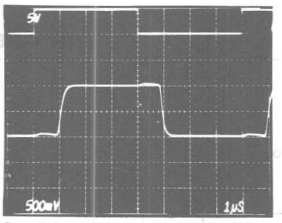


MUX-24 SMALL-SIGNAL SWITCHING



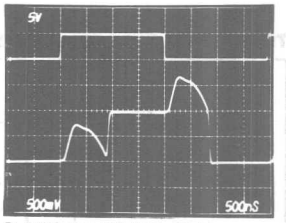
RL = 1MΩ, CL = 10pF, V1 = –500mV,
V4 = +500mV
VOLTAGE = 500mV/DIV, TIME = 1µs/DIV

MUX-24 SMALL-SIGNAL SWITCHING WITH FILTERING



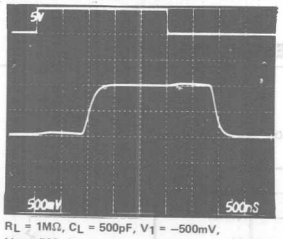
RL = 1MΩ, CL = 500pF, V1 = –500mV,
V4 = +500mV
VOLTAGE = 500mV/DIV, TIME = 1µs/DIV

MUX-24 SMALL-SIGNAL SWITCHING WITH 2µs SAMPLE TIME



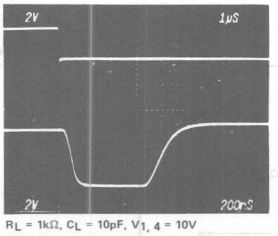
RL = 1MΩ, CL = 10pF, V1 = –500mV,
V4 = +500mV
VOLTAGE = 500mV/DIV, TIME = 500ns/DIV

MUX-24 SMALL-SIGNAL SWITCHING WITH FILTERING AND 2.5µs SAMPLE TIME



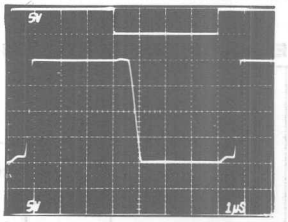
RL = 1MΩ, CL = 500pF, V1 = –500mV,
V4 = +500mV
VOLTAGE = 500mV/DIV, TIME = 500ns/DIV

MUX-24 BREAK-BEFORE-MAKE SWITCHING



RL = 1kΩ, CL = 10pF, V1, 4 = 10V
VOLTAGE = 2V/DIV, TIME = 200ns/DIV

MUX-24 LARGE-SIGNAL SWITCHING

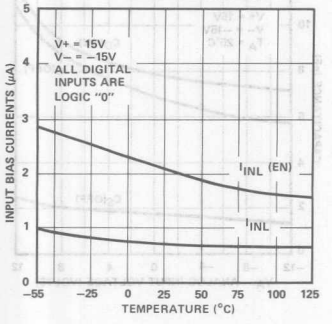


RL = 1MΩ, CL = 10pF, V1 = –10V, V4 = +10V
VOLTAGE = 5V/DIV, TIME = 1µs/DIV

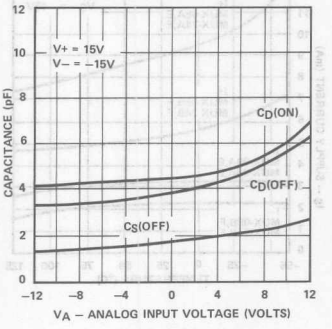
NOTE:
Top waveforms: Digital Input 5V/DIV
Bottom waveforms: Multiplexer Output

TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

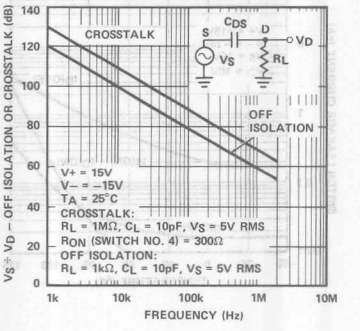
DIGITAL INPUT CURRENTS vs TEMPERATURE



MUX-24 SWITCH CAPACITANCES vs ANALOG INPUT VOLTAGE



MUX-24 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 3A



A.C. TEST CIRCUITS

TRANSITION TIME TEST CIRCUIT

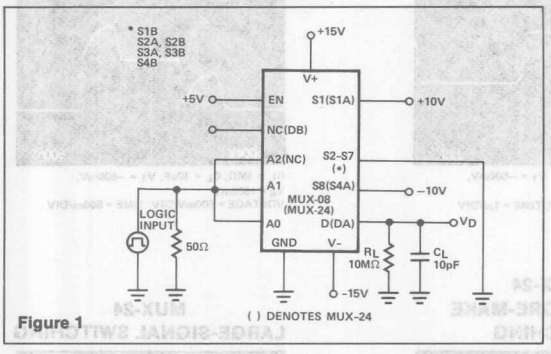


Figure 1

BREAK-BEFORE-MAKE TEST CIRCUIT

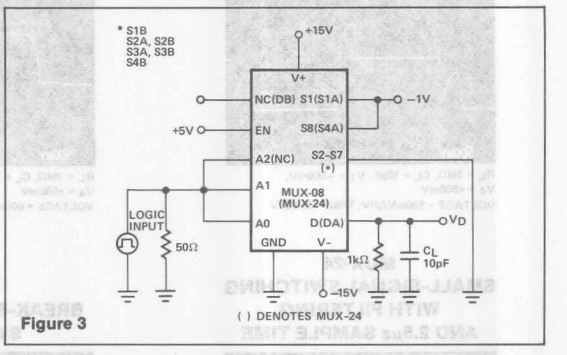


Figure 3

ENABLE DELAY TIME TEST CIRCUIT

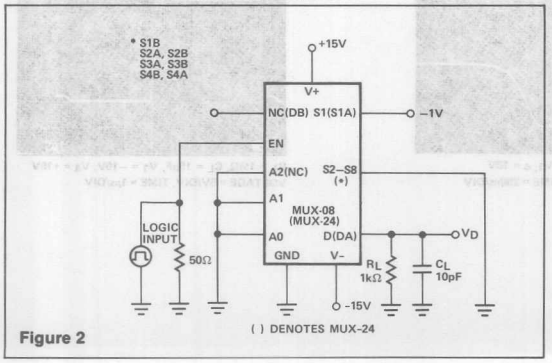


Figure 2

CROSSTALK MEASUREMENT CIRCUIT

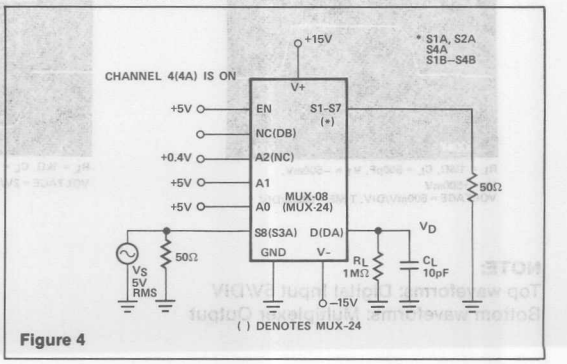


Figure 4

A.C. TEST CIRCUITS

OFF-ISOLATION MEASUREMENT CIRCUIT

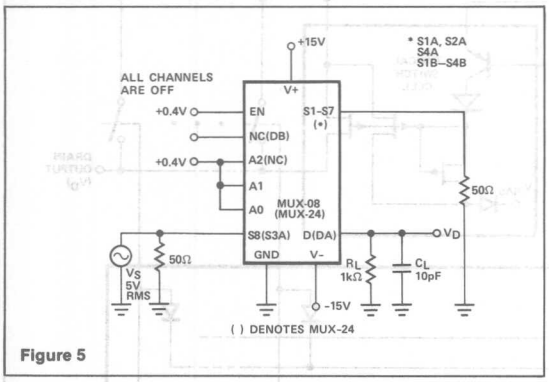
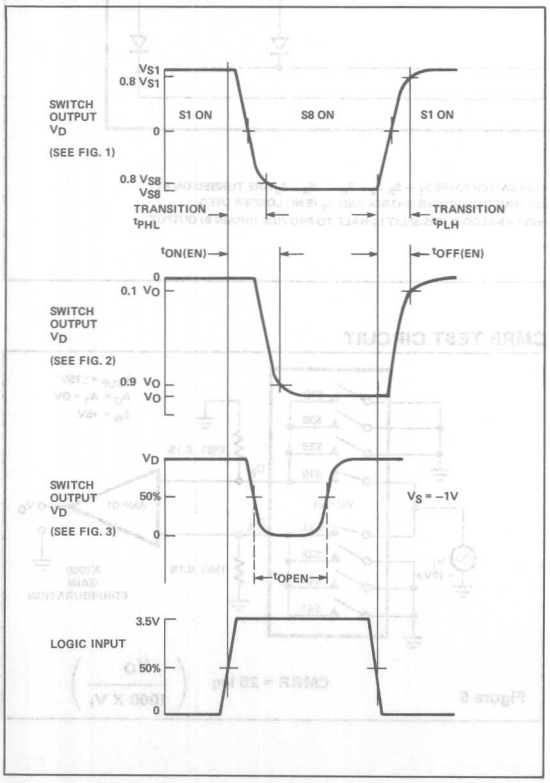


Figure 5

SWITCHING TIME WAVEFORMS



APPLICATIONS INFORMATION

These analog multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with Bipolar-JFET processing, **special handling as required with CMOS devices, is not necessary to prevent damage to this multiplexer.** Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above ≈ 1.4V.

The "ON" resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of −15V to +11V with $V_{SUPPLY} = \pm 15V$. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an "OFF" switch remains greater than its V_p, and prevents that channel from being falsely turned "ON". When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an "ON" switch exceeds −0.6V. While this condition will cause an error in the output, it will not damage the switch. In lab tests, the multiplexer output has been loaded with a 0.01μF capacitor in the circuit of Figure 1. With $V_1 = -10V$ and $V_8 = +10V$, the logic input was driven at a 1kHz rate. The positive-going slew rate was 0.3V/μs which is equivalent to a normal I_{DSS} of 3mA. The negative-going slew rate was 0.7V/μs which is equivalent to a "reverse" I_{DSS} of 7mA. Note that when switch 1 is first turned "ON" it has a drop of −20V across its terminals. In spite of that fact, the current is limited to approximately twice its normal I_{DSS}.

CROSSTALK AND OFF-ISOLATION

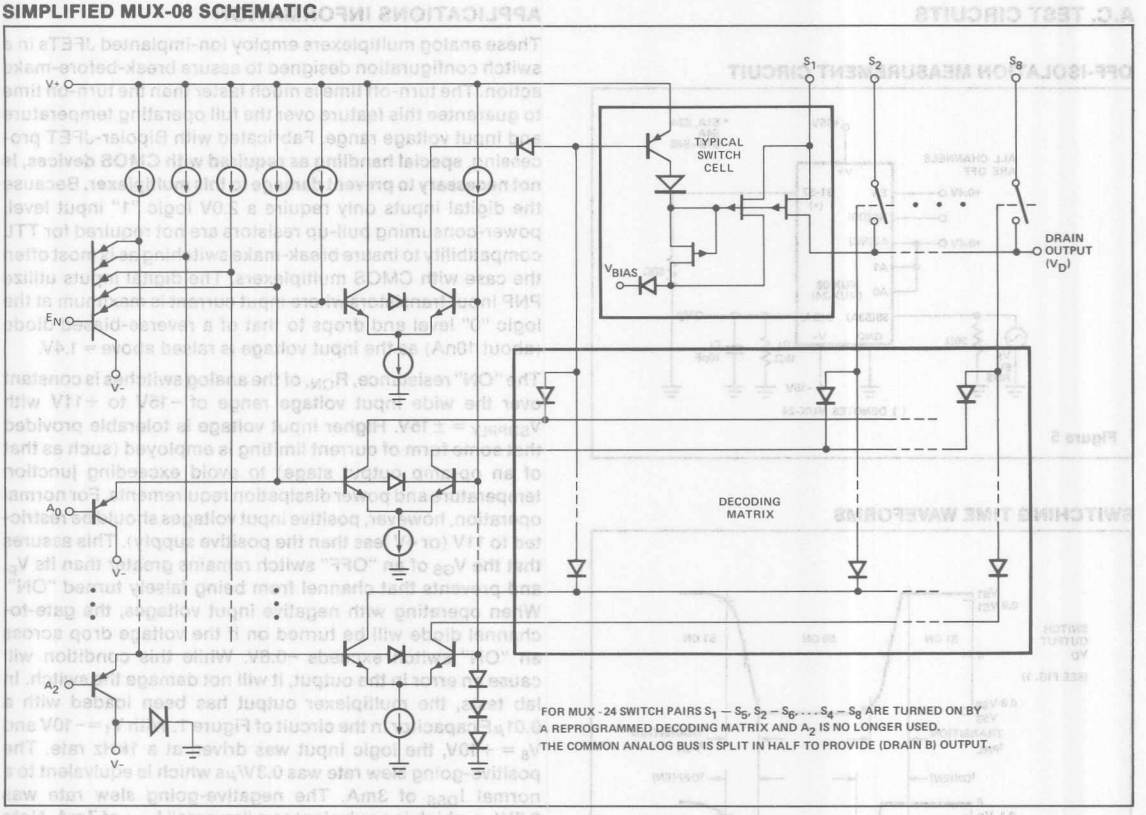
Crosstalk and off-isolation performance is influenced by the type of package selected. Epoxy (P) packaged devices typically exhibit a 12dB improvement in off-isolation (f = 500kHz) performance when compared to ceramic (Q) packaged devices. Epoxy packaged devices typically exhibit a 15dB improvement in crosstalk (f = 500kHz) performance when compared to ceramic (Q) packaged devices.

SINGLE SUPPLY OPERATION OF JFET MULTIPLEXERS

PMI's JFET multiplexers will operate from a single positive supply voltage with the negative supply pin at ground potential. The analog signal range will include ground.

For complete single supply operation information, refer to application note, AN-32.

SIMPLIFIED MUX-08 SCHEMATIC



The simplified MUX-08/MUX-24 schematic shows that logic trip points are determined by two forward diode drops. An internal clamping diode between V– and ground prevents excessive current flow between V+ and ground in the event that V– becomes open circuit. The decoding matrix is accomplished by a programmed diode array. The switch cell consists of P channel JFET's with appropriate blocking diodes which ruggedizes the circuit's overvoltage and supply loss characteristics.

DIFFERENTIAL MULTIPLEXERS

One characteristic unique to differential multiplexers (MUX-24) is the ability to reject common-mode signals from becoming differential error signals. Common-mode rejection is a parameter which defines the amount of rejection in terms of dB. The MUX-24 exhibits a 106dB at 60Hz and 101dB at 400Hz of CMRR using the test circuit of Figure 6.

CMRR TEST CIRCUIT

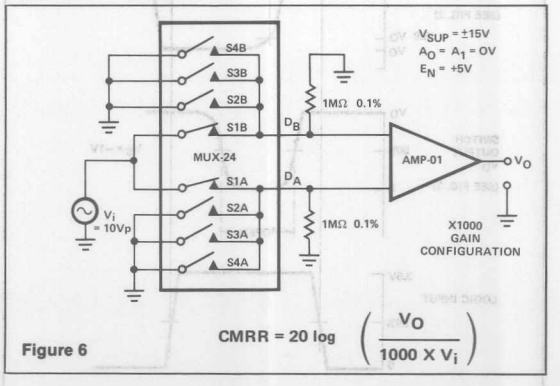
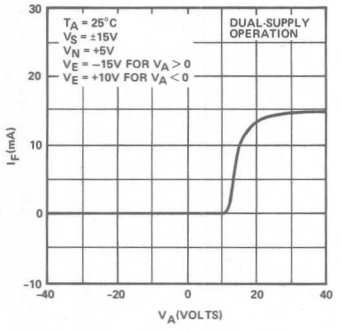


Figure 6

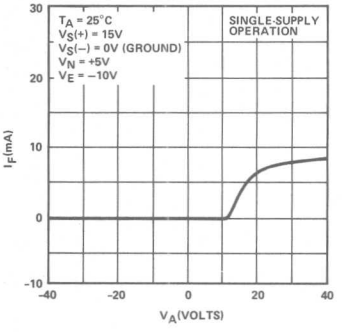
$$CMRR = 20 \log \left(\frac{V_O}{1000 \times V_i} \right)$$

TYPICAL PERFORMANCE CHARACTERISTICS

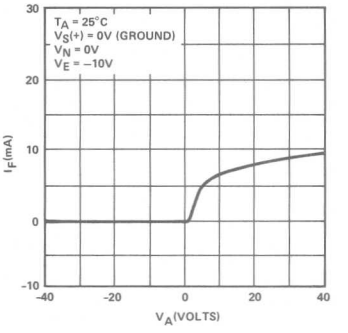
OVERVOLTAGE V-I CHARACTERISTIC



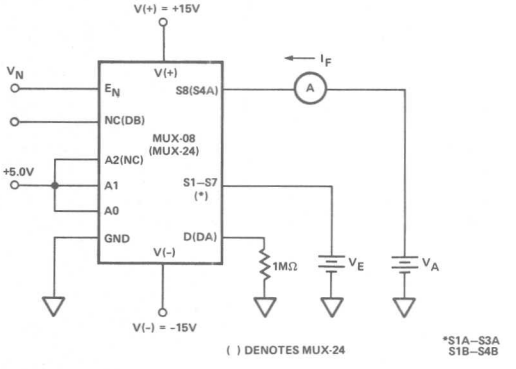
OVERVOLTAGE V-I CHARACTERISTIC



POWER-LOSS V-I CHARACTERISTIC



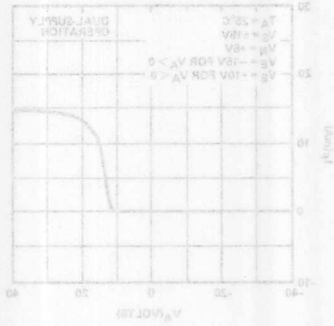
OVERVOLTAGE/POWER-LOSS MEASUREMENT TEST CIRCUIT



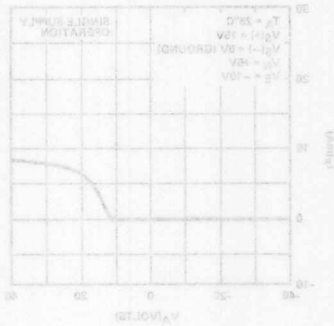
5

TYPICAL PERFORMANCE CHARACTERISTICS

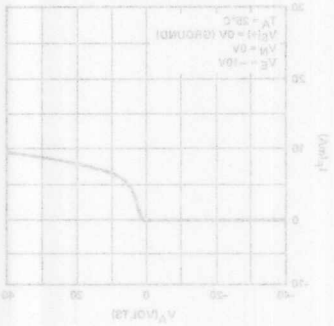
OVERVOLTAGE V-I CHARACTERISTIC



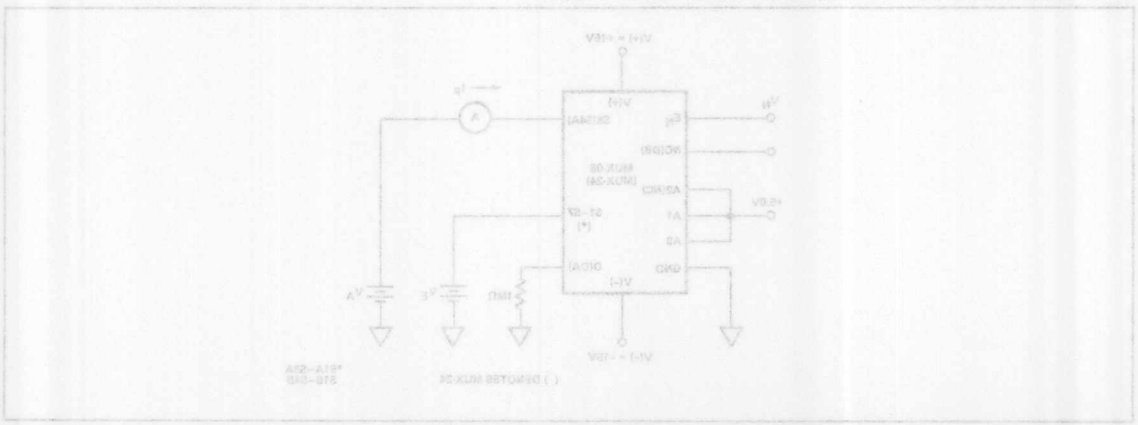
OVERVOLTAGE V-I CHARACTERISTIC



POWER-LOSS V-I CHARACTERISTIC



OVERVOLTAGE/POWER-LOSS MEASUREMENT TEST CIRCUIT



16-Channel/Dual 8-Channel JFET Analog Multiplexers (Overvoltage Protected)

MUX-16/MUX-28

FEATURES

- JFET Switches Rather Than CMOS
- Highly Resistant To Static Discharge Damage
- No SCR Latch-up Problems
- Low "ON" Resistance — 290Ω Typical
- Low Leakage Current
- Digital Inputs Compatible With TTL and CMOS
- Break-Before-Make Action
- 125° C Temperature-Tested Dice Available
- Overvoltage Protected
- Supply Loss Protection
- MUX-16 Pin Compatible With DG506, HI-506A, AD7506
- MUX-28 Pin Compatible With DG507, HI-507A, AD7507
- Available in Die Form

ORDERING INFORMATION †

25°C RESISTANCE	PACKAGE CERDIP 28-PIN	PACKAGE LCC 28-CONTACT	PACKAGE PLASTIC 28-PIN	OPERATING TEMPERATURE RANGE
290Ω	MUX16AT*	–	–	MIL
290Ω	MUX16ET	–	–	IND
400Ω	MUX16BT*	MUX16BTC/883	–	MIL
400Ω	MUX16FT	–	MUX16FP	XIND
400Ω	–	–	MUX16FPC	XIND
290Ω	MUX28AT*	–	–	MIL
290Ω	MUX28ET	–	–	IND
400Ω	MUX28BT*	MUX28BTC/883	–	MIL
400Ω	MUX28FT	–	MUX28FP	XIND
400Ω	–	–	MUX28FPC	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

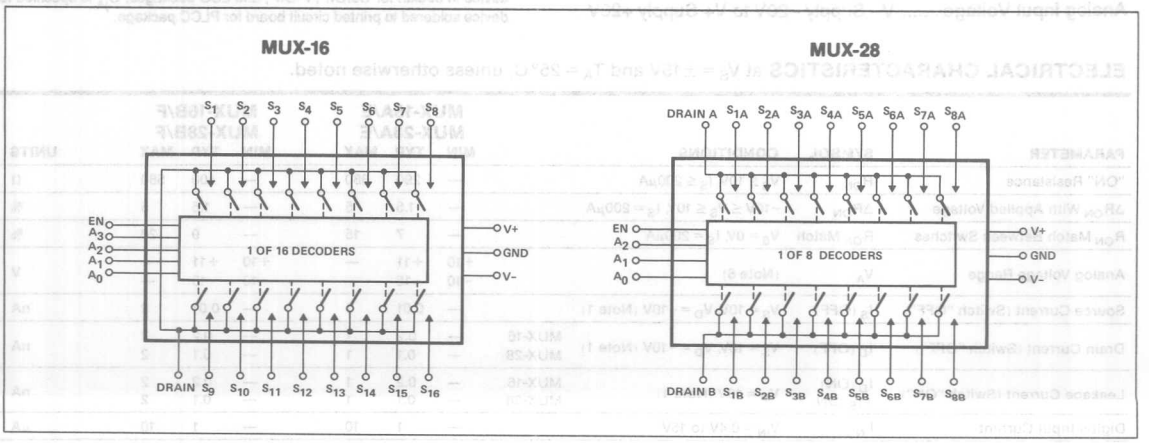
The MUX-16 is a monolithic 16-channel analog multiplexer which connects a single output to 1 of the 16 analog inputs depending upon the state of a 4-bit binary address. Disconnection of the output is provided by a logical "0" at the ENABLE input, thereby providing a package selection function.

The MUX-28 is a monolithic 8-channel differential analog multiplexer configured in a double pole, 8-position (plus OFF) electronic switch array. A 3-bit binary input address connects a pair of independent analog inputs from each 8-channel input section to the corresponding pair of independent analog outputs. Disconnection of both inputs is provided by a logical "0" at the ENABLE input, thereby offering a package select function.

Fabricated with Precision Monolithics' high performance Bipolar-JFET technology, these devices offer low, constant "ON" resistance. Performance advantages include low leakage currents and fast settling time with low crosstalk to satisfy a wide variety of applications. These multiplexers do not suffer from latch-up or static discharge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors. For single 8-channel and dual 4-channel models, refer to the MUX-08/MUX-24 data sheet.

5

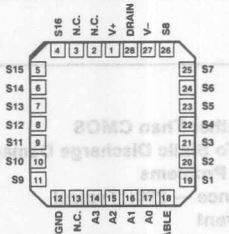
FUNCTIONAL DIAGRAMS



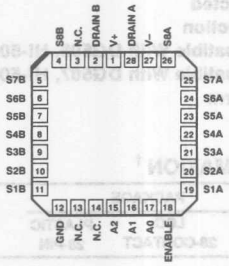
PIN CONNECTIONS & TRUTH TABLES



28-PIN PLASTIC DIP (P-Suffix)
28-PIN CERDIP (T-Suffix)



MUX-16BTC/883
LCC
(TC-Suffix)
PLCC
(PC-Suffix)



MUX-28BTC/883
LCC
(TC-Suffix)
PLCC
(PC-Suffix)

MUX-16

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

MUX-28

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature Range,
MUX-16/28-AT, BT, BTC ..... –55°C to +125°C
MUX-16/28-ET ..... –25°C to +85°C
MUX-16/28-FP, FPC, FT ..... –40°C to +85°C
Junction Temperature (T_j) ..... –65°C to +150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Maximum Junction Temperature ..... 150°C
V+ Supply to V– Supply 36V
Logic Input Voltage ..... (V– or –4V) to V+ Supply
Analog Input Voltage ..... V– Supply –20V to V+ Supply +20V

Maximum Current Through Any Pin 25mA

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
28-Pin Hermetic DIP (T)	55	15	°C/W
28-Pin Plastic DIP (P)	56	30	°C/W
28-Contact LCC (TC)	86	35	°C/W
28-Contact PLCC (PC)	70	33	°C/W

NOTES:
1. Ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for PLCC package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		MUX-16A/E MUX-28A/E MIN	TYP	MAX	MUX-16B/F MUX-28B/F MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_S \leq 10V$, $I_S \leq 200\mu A$		—	290	380	—	400	580	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V$, $I_S = 200\mu A$		—	1.5	5	—	1.5	5	%
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V$, $I_S = 200\mu A$		—	7	15	—	9	20	%
Analog Voltage Range	V_A	(Note 6)		+10 −10	+11 −15	— —	+10 −10	+11 −15	— —	V
Source Current (Switch "OFF")	I_S (OFF)	$V_S = 10V$, $V_D = -10V$ (Note 1)		—	0.01	1	—	0.01	2	nA
Drain Current (Switch "OFF")	I_D (OFF)	$V_S = 10V$, $V_D = -10V$ (Note 1)	MUX-16 MUX-28	— —	0.2 0.1	1 1	— —	0.2 0.1	2 2	nA
Leakage Current (Switch "ON")	I_D (ON) $+I_S$ (ON)	$V_D = 10V$ (Note 1)	MUX-16 MUX-28	— —	0.2 0.1	1 1	— —	0.2 0.1	2 2	nA
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V		—	1	10	—	1	10	μA

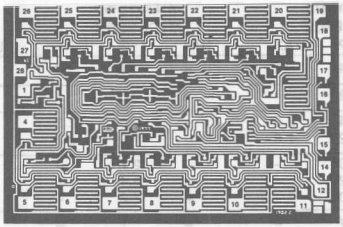
ELECTRICAL CHARACTERISTICS at V_S = ±15V and T_A = +25°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS		MUX-16A/E MUX-28A/E MIN	TYP	MAX	MUX-16B/F MUX-28B/F MIN	TYP	MAX	UNITS
Digital "0" Enable Current	I_{INL} (EN)	V_{EN} = 0.4V		–	4	10	–	4	10	µA
Digital Input Capacitance	C_{DIG}			–	3	–	–	3	–	pF
Switching Time (t_{TRAN})	t_{PHL}	(Notes 2,5) Figure 1		–	1.4	2.0	–	1.8	2.5	µs
	t_{PLH}	(Test Circuits)		–	1.2	1.8	–	1.6	2.2	
Output Settling Time	t_s	10V Step to 0.10%		–	2.6	–	–	2.7	–	µs
		10V Step to 0.05%		–	3.2	–	–	3.4	–	
		10V Step to 0.02%		–	4.0	–	–	7.2	–	
Break-Before-Make Delay	t_{OPEN}	Figure 3		–	0.7	–	–	1	–	µs
Enable Delay "ON"	$t_{ON (EN)}$	(Note 5) Figure 2 (Test Circuits)		–	1	2	–	1.2	2.5	µs
Enable Delay "OFF"	$t_{OFF (EN)}$	(Note 5) Figure 2 (Test Circuits)	MUX-16	–	0.25	0.5	–	0.25	0.5	µs
			MUX-28	–	0.25	0.5	–	0.25	0.6	
"OFF" Isolation	ISO_{OFF}	(Note 4) Figure 4 (Test Circuits)		–	66	–	–	66	–	dB
Crosstalk	CT	(Note 3) Figure 5 (Test Circuits)		–	75	–	–	75	–	dB
Source Capacitance	$C_{S (OFF)}$	Switch "OFF," V_S = 0V, V_D = 0V		–	2.5	–	–	2.5	–	pF
Drain Capacitance	$C_{D (OFF)}$	Switch "OFF," V_S = 0V, V_D = 0V	MUX-16	–	13	–	–	13	–	pF
			MUX-28	–	8	–	–	8	–	
Input to Output Capacitance	$C_{DS (OFF)}$	(Note 4)		–	0.15	–	–	0.15	–	pF
Positive Supply Current (All Digital Inputs Logic "0" or "1")	I+	V+ = 15V	MUX-16	–	15	19	–	9	19	mA
			MUX-28	–	15	19	–	8	19	
		V+ = 5V	MUX-16	–	12	–	–	8	–	
			MUX-28	–	12	–	–	7	–	
Negative Supply Current (All Digital Inputs Logic "0" or "1")	I–	V– = –15V	MUX-16	–	5	7	–	3.5	7	mA
			MUX-28	–	5	7	–	3	7	
		V– = –5V	MUX-16	–	4	–	–	3	–	
			MUX-28	–	4	–	–	2.5	–	

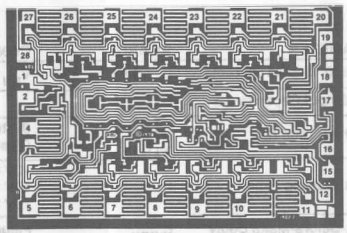
NOTES:
1. Conditions applied to leakage tests insure worst case leakages.
2. R_L = 10MΩ, C_L = 10pF.
3. Crosstalk is measured by driving channel 8 (8B*) with channel 7 (7B*) ON. R_L = 1MΩ, C_L = 10pF, V_S = 5V RMS, f = 500kHz.
4. "OFF" isolation is measured by driving channel 8 (8B) with ALL channels OFF. R_L = 1kΩ, C_L = 10pF, V_S = 5V RMS, f = 500kHz. C_{DS} is computed from the OFF isolation measurement.
5. Sample tested.
6. Guaranteed by leakage current and R_{ON} tests.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –55°C ≤ T_A ≤ +125°C for MUX-16AT/BT/BTC and MUX-28AT/BT/BTC; –25°C ≤ T_A ≤ +85°C for MUX-16ET and MUX-28ET; –40°C ≤ T_A ≤ +85°C for MUX-16 FT/FP/FPC and MUX-28FT/FP/FPC, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-16A/E MUX-28A/E MIN	TYP	MAX	MUX-16B/F MUX-28B/F MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	V_S ≤ 10, I_S ≤ 200µA	–	–	500	–	–	800	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	–10V ≤ V_S ≤ 10V, I_S = 200µA	–	2	–	–	5.5	–	%
R_{ON} Match Between Switches	R_{ON} Match	V_S = 0V, I_S = 200µA	–	10	–	–	15	–	%
Analog Voltage Range	V_A	(Note 6)	+10	+11	–	+10	+11	–	V
			–10	–15	–	–10	–15	–	
Source Current (Switch"OFF")	$I_{S (OFF)}$	V_S = 10V, V_D = –10V (Note 1)	–	–	25	–	–	50	nA
Drain Current (Switch "OFF")	$I_{D (OFF)}$	V_S = 10V, V_D = –10V (Note 1)	–	–	75	–	–	250	nA
Leakage Current (Switch "ON")	$I_{D (ON)}$ $+I_{S (ON)}$	V_D = 10V (Note 1)	–	–	75	–	–	250	nA
Digital "1" Input Voltage	V_{INH}	(Note 6)	2	–	–	2	–	–	V
Digital "0" Input Voltage	V_{INL}	(Note 6)	–	–	0.7	–	–	0.7	V
Digital Input Current	I_{IN}	V_{IN} = 0.4V to 15V	–	–	20	–	–	20	µA
Digital "0" Enable Current	I_{INL} (EN)	V_{EN} = 0.4V	–	–	20	–	–	20	µA
Positive Supply Current	I+	All Digital Inputs Logic "0" or "1"	–	–	24	–	–	24	mA
Negative Supply Current	I–	All Digital Inputs Logic "0" or "1"	–	–	8.2	–	–	8.2	mA



DIE SIZE 0.110 × 0.076 inch, 8360 sq. mils
(2.794 × 1.930 mm, 5392 sq. mm)



1. POSITIVE SUPPLY
4. SOURCE 16 (S16)
5. SOURCE 15 (S15)
6. SOURCE 14 (S14)
7. SOURCE 13 (S13)
8. SOURCE 12 (S12)
9. SOURCE 11 (S11)
10. SOURCE 10 (S10)
11. SOURCE 9 (S9)
12. GROUND
14. ADDRESS BIT 3 (A3)
15. ADDRESS BIT 2 (A2)
16. ADDRESS BIT 1 (A1)
17. ADDRESS BIT 0 (A0)
18. ENABLE
19. SOURCE 1 (S1)
20. SOURCE 2 (S2)
21. SOURCE 3 (S3)
22. SOURCE 4 (S4)
23. SOURCE 5 (S5)
24. SOURCE 6 (S6)
25. SOURCE 7 (S7)
26. SOURCE 8 (S8)
27. NEGATIVE SUPPLY (SUBSTRATE)
28. DRAIN

1. POSITIVE SUPPLY
2. DRAIN B
4. SOURCE 8 (S8B)
5. SOURCE 7 (S7B)
6. SOURCE 6 (S6B)
7. SOURCE 5 (S5B)
8. SOURCE 4 (S4B)
9. SOURCE 3 (S3B)
10. SOURCE 2 (S2B)
11. SOURCE 1 (S1B)
12. GROUND
15. ADDRESS BIT 2 (A2)
16. ADDRESS BIT 1 (A1)
17. ADDRESS BIT 0 (A0)
18. ENABLE
19. SOURCE 1 (S1A)
20. SOURCE 2 (S2A)
21. SOURCE 3 (S3A)
22. SOURCE 4 (S4A)
23. SOURCE 5 (S5A)
24. SOURCE 6 (S6A)
25. SOURCE 7 (S7A)
26. SOURCE 8 (S8A)
27. NEGATIVE SUPPLY (SUBSTRATE)
28. DRAIN A

WAFER TEST LIMITS at V+ = 15V, V− = −15V, T_A = 25° C for MUX-16/28 N and G, T_A = 125° C for MUX-16/28 NT and GT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-16/ MUX-28NT LIMIT	MUX-16/ MUX-28N LIMIT	MUX-16/ MUX-28GT LIMIT	MUX-16/ MUX-28G LIMIT	UNITS
"ON" Resistance	R_{ON}	V_S = 0V, I_S = 200μA	540	380	800	580	Ω MAX
Digital "1" Input Voltage	V_{INH}		2	2	2	2	V MIN
Digital "0" Input Voltage	V_{INL}		0.8	0.8	0.8	0.8	V MAX
Digital "0" Input Current	I_{INL}	V_{IN} = 0.4V	20	10	20	10	μA MAX
Digital "0" Enable Current	$I_{INL(EN)}$	V_{EN} = 0.4V	20	10	20	10	μA MAX
Positive Supply Current (All Digital Inputs Logic "0")	I+		24	19	24	19	mA MAX
Negative Supply Current (All Digital Inputs Logic "0")	I−		8.2	7	8.2	7	mA MAX
Analog Input Range	V_A	(Note 2)	±10	±10	±10	±10	V MIN

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

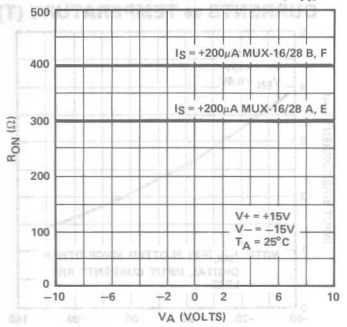
TYPICAL ELECTRICAL CHARACTERISTICS at V+ = 15V, V− = −15V and T_A = 25° C for MUX-16/28 N and G, T_A = 125° C for MUX-16/28 NT and GT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-16/ MUX-28NT TYPICAL	MUX-16/ MUX-28N TYPICAL	MUX-16/ MUX-28GT TYPICAL	MUX-16/ MUX-28G TYPICAL	UNITS
Switching Time (t_{TRAN})	t_{PHL} t_{PLH}	(Note 1) Figure 1	2 1.8	1 0.9	2.6 2.4	1.5 1.4	μs
Output Settling Time	t_S	10V Step to 0.1% (Note 1)	2.5	1.5	2.9	1.9	μs
Break-Before-Make Delay	t_{OPEN}	(Note 1) Figure 3 (Test Circuits)	0.8	0.8	1	1	μs
Crosstalk	CT	(Note 1) Figure 5 (Test Circuits)	70	70	70	70	dB
ΔR_{ON} With Applied Voltage	ΔR_{ON}	−10V ≤ V_S ≤ 10V, I_S = 200μA	1.5	1.5	1.5	1.5	%
Leakage Current (Switch "ON")	$I_{D(ON)}$	V_D = 10V (Note 1)	20	0.2	20	0.2	nA
Analog Input Range	V_A	(Note 2)	+11 −15	+11 −15	+11 −15	+11 −15	V

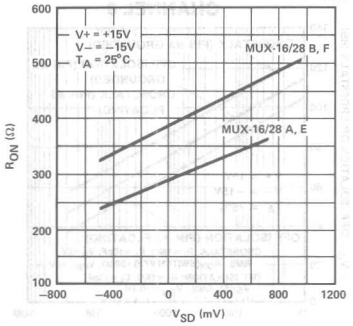
NOTES:
1. The data shown is extrapolated from measurements made on the packaged devices.
2. Guaranteed by R_{ON} and leakage current tests.

TYPICAL PERFORMANCE CHARACTERISTICS (apply to all grades, unless otherwise noted.)

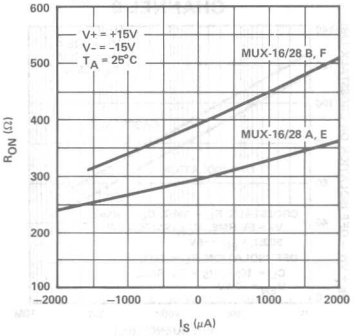
"ON" RESISTANCE (R_{ON}) vs ANALOG VOLTAGE (V_A)



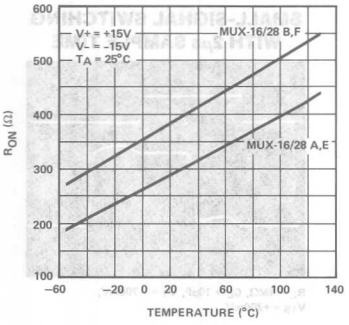
R_{ON} vs SWITCH VOLTAGE (V_{SD})



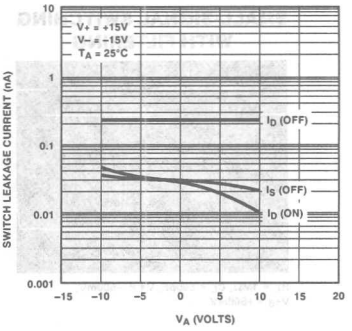
R_{ON} vs SWITCH CURRENT (I_S)



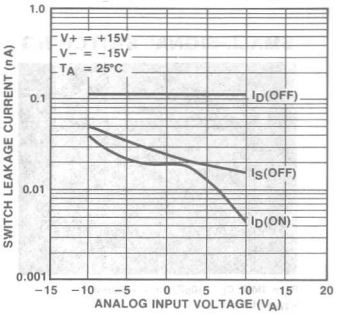
R_{ON} vs TEMPERATURE (T)



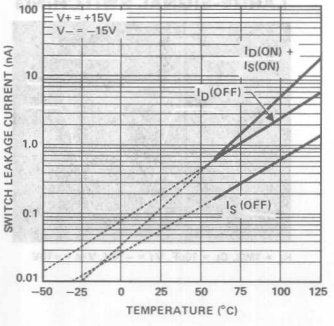
MUX-16 SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE (V_A)



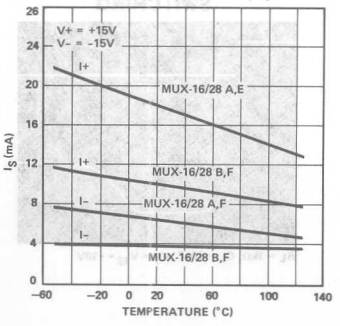
MUX-28 SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE (V_A)



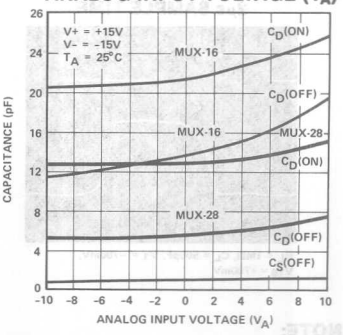
SWITCH LEAKAGE CURRENTS vs TEMPERATURE



SUPPLY CURRENTS vs TEMPERATURE (T)



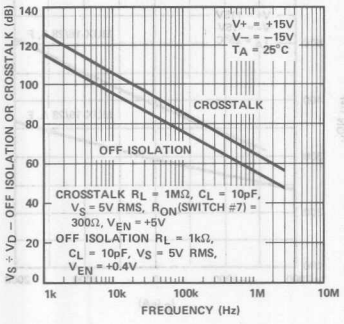
SWITCH CAPACITANCES vs ANALOG INPUT VOLTAGE (V_A)



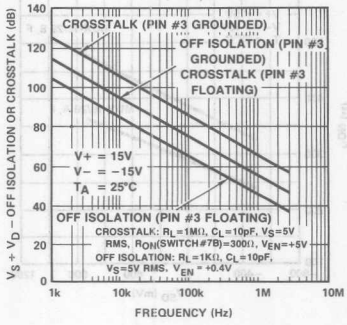
5

TYPICAL PERFORMANCE CHARACTERISTICS (apply to all grades, unless otherwise noted.)

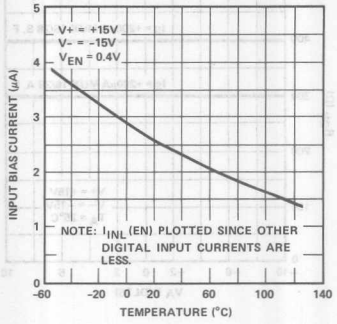
MUX-16 OFF PERFORMANCE OF CHANNEL 8



MUX-28 OFF PERFORMANCE OF CHANNEL 8

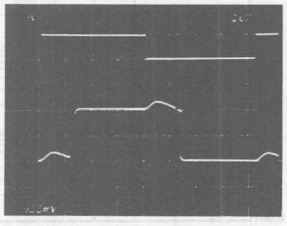


DIGITAL INPUT BIAS CURRENTS vs TEMPERATURE (T)



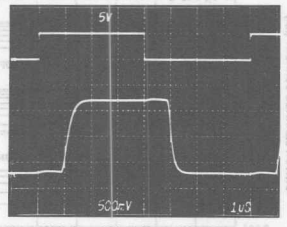
MUX-16 DYNAMIC CHARACTERISTIC CURVES

SMALL-SIGNAL SWITCHING



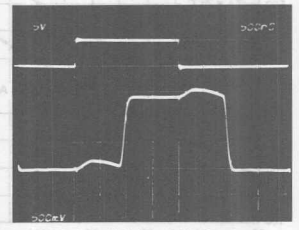
RL = 1MΩ, CL = 10pF, V1 = –500mV, V16 = +500mV

SMALL-SIGNAL SWITCHING WITH FILTERING



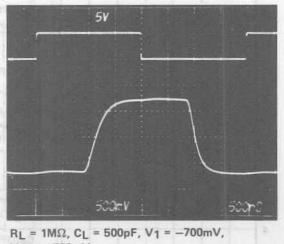
RL = 1MΩ, CL = 500pF, V1 = –500mV, V16 = +500mV

SMALL-SIGNAL SWITCHING WITH 2µs SAMPLE TIME



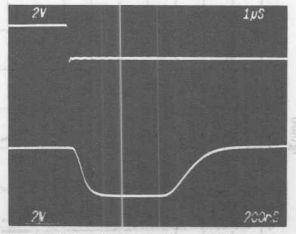
RL = 1MΩ, CL = 10pF, V1 = –700mV, V16 = +700mV

SMALL-SIGNAL SWITCHING WITH FILTERING AND 2µs SAMPLE TIME



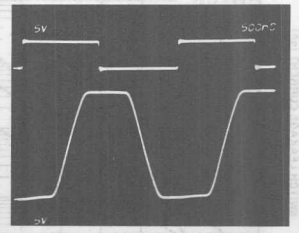
RL = 1MΩ, CL = 500pF, V1 = –700mV, V16 = +700mV

BREAK-BEFORE-MAKE SWITCHING



RL = 1kΩ, CL = 10pF, V1 = V16 = +10V

LARGE-SIGNAL SWITCHING

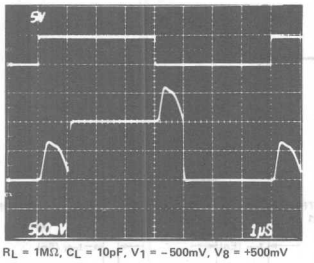


RL = 1MΩ, CL = 10pF, V1 = –10V, V16 = +10V

NOTE:
Top Waveforms: Digital Input 5V/Div
Bottom Waveforms: Multiplexer Output (V_D)

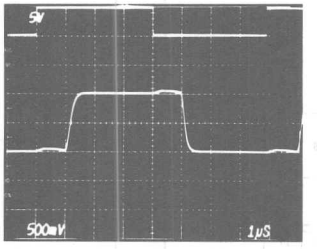
MUX-28 DYNAMIC CHARACTERISTIC CURVES

SMALL-SIGNAL SWITCHING



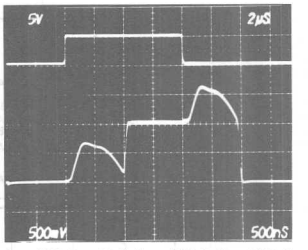
R_L = 1MΩ, C_L = 10pF, V_1 = −500mV, V_8 = +500mV

SMALL-SIGNAL SWITCHING WITH FILTERING



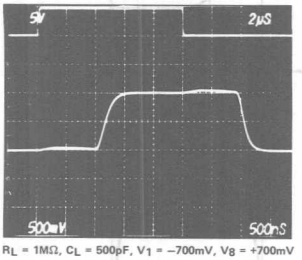
R_L = 1MΩ, C_L = 500pF, V_1 = −500mV, V_8 = +500mV

SMALL-SIGNAL SWITCHING WITH 2µs SAMPLE TIME



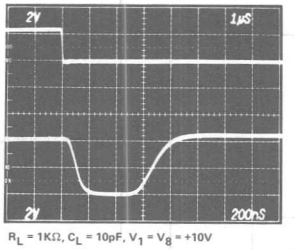
R_L = 1MΩ, C_L = 10pF, V_1 = −700mV, V_8 = +700mV

SMALL-SIGNAL SWITCHING WITH FILTERING AND 2.5µs SAMPLE TIME



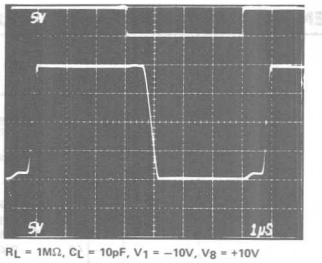
R_L = 1MΩ, C_L = 500pF, V_1 = −700mV, V_8 = +700mV

BREAK-BEFORE-MAKE SWITCHING



R_L = 1KΩ, C_L = 10pF, V_1 = V_8 = +10V

LARGE-SIGNAL SWITCHING

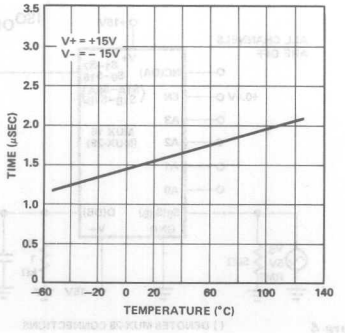


R_L = 1MΩ, C_L = 10pF, V_1 = −10V, V_8 = +10V

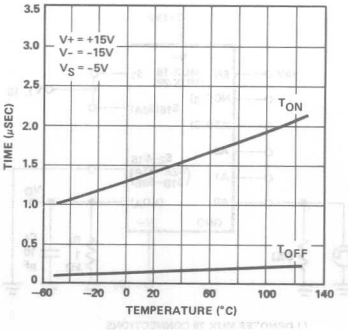
NOTE:
Top Waveforms: Digital Input 5V/Div
Bottom Waveforms: Multiplexer Output (V_D)

TYPICAL PERFORMANCE CHARACTERISTICS (apply to all grades, unless otherwise noted.)

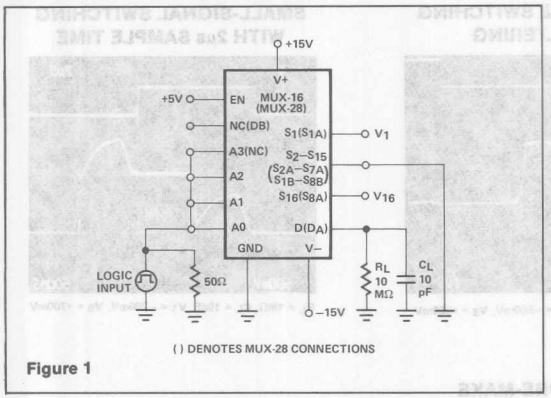
TRANSITION TIME vs TEMPERATURE



ENABLE DELAY TIME vs TEMPERATURE



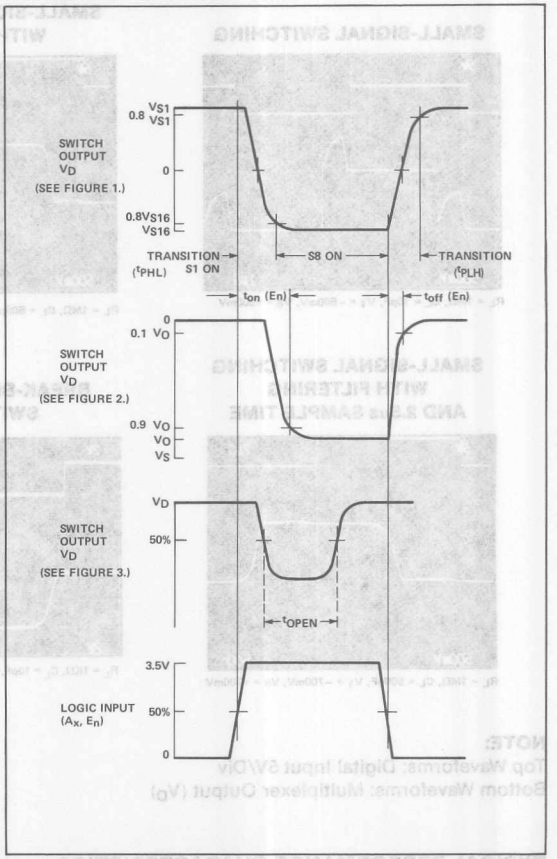
TRANSITION TIME TEST CIRCUIT



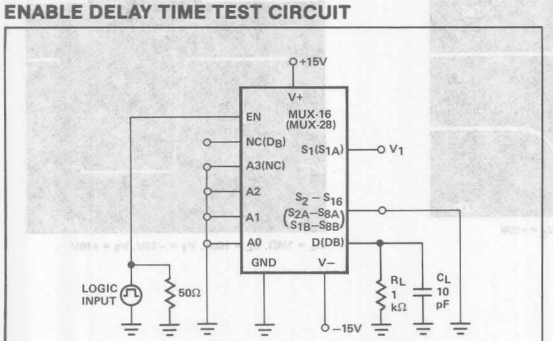
( ) DENOTES MUX-28 CONNECTIONS

Figure 1

SWITCHING TIME WAVEFORMS



ENABLE DELAY TIME TEST CIRCUIT



( ) DENOTES MUX-28 CONNECTIONS

Figure 2

BREAK-BEFORE-MAKE TEST CIRCUIT

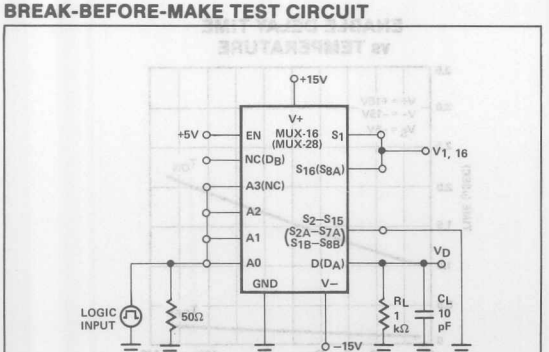


Figure 3 ( ) DENOTES MUX-28 CONNECTIONS

OFF ISOLATION TEST CIRCUIT

$$ISO_{OFF} = 20 \log \frac{|V_S|}{|V_D|}$$

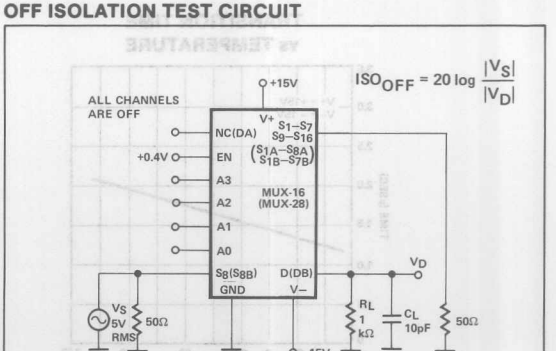


Figure 4 ( ) DENOTES MUX-28 CONNECTIONS

CROSSTALK MEASUREMENT CIRCUIT

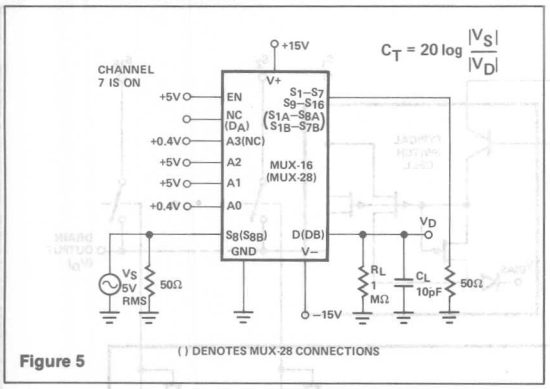
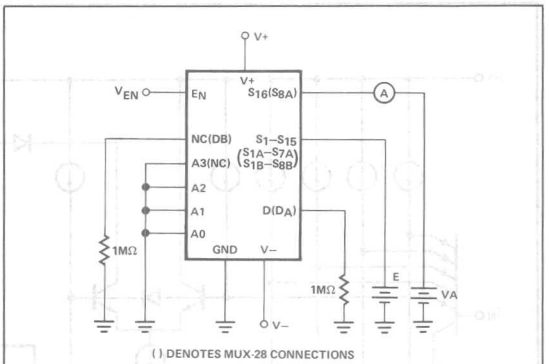


Figure 5

OVERVOLTAGE MEASUREMENT TEST CIRCUIT



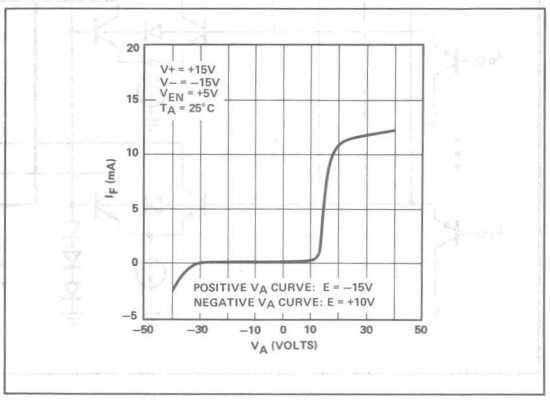
APPLICATIONS INFORMATION

These analog multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make (B.B.M.) action. The turn-off time is much faster than the turn-on time to guarantee B.B.M. over the full operating temperature and input voltage range. Fabricated with JFET processing rather than CMOS, special handling is not necessary to prevent damage to this multiplexer. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pullup resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above ≈ 1.4V.

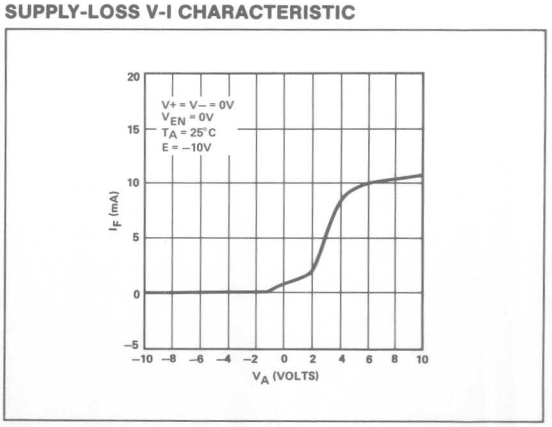
The "ON" resistance, R_{ON} of the analog switches is constant over the wide input voltage range of −15V to +11V with $V_{SUPPLY} = \pm 15V$. The overvoltage and supply-loss V-I characteristics shown indicate typical performance when the multiplexer is subjected to abnormal signals. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF FET switch remains greater than its V_P, preventing that channel from being falsely turned ON.

When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an ON switch exceeds −0.6V. While this condition will cause an error in the output, it will not damage the switch. In lab tests, the multiplexer output has been loaded with a 0.01μF capacitor in the circuit of Figure 1. With $V_1 = -10V$ and $V_{16} = +10V$, the logic input was driven at a 1kHz rate. The positive-going slew rate was 0.3V/μSec which is equivalent to a normal I_{DSS} of 3mA. The negative-going slew rate was 0.7V/μsec which is equivalent to a "reverse" I_{DSS} of 7mA. Note that when switch one (1) is first turned ON it has a drop of −20V across its terminals. In spite of that fact, the current is limited to approximately twice its normal I_{DSS}.

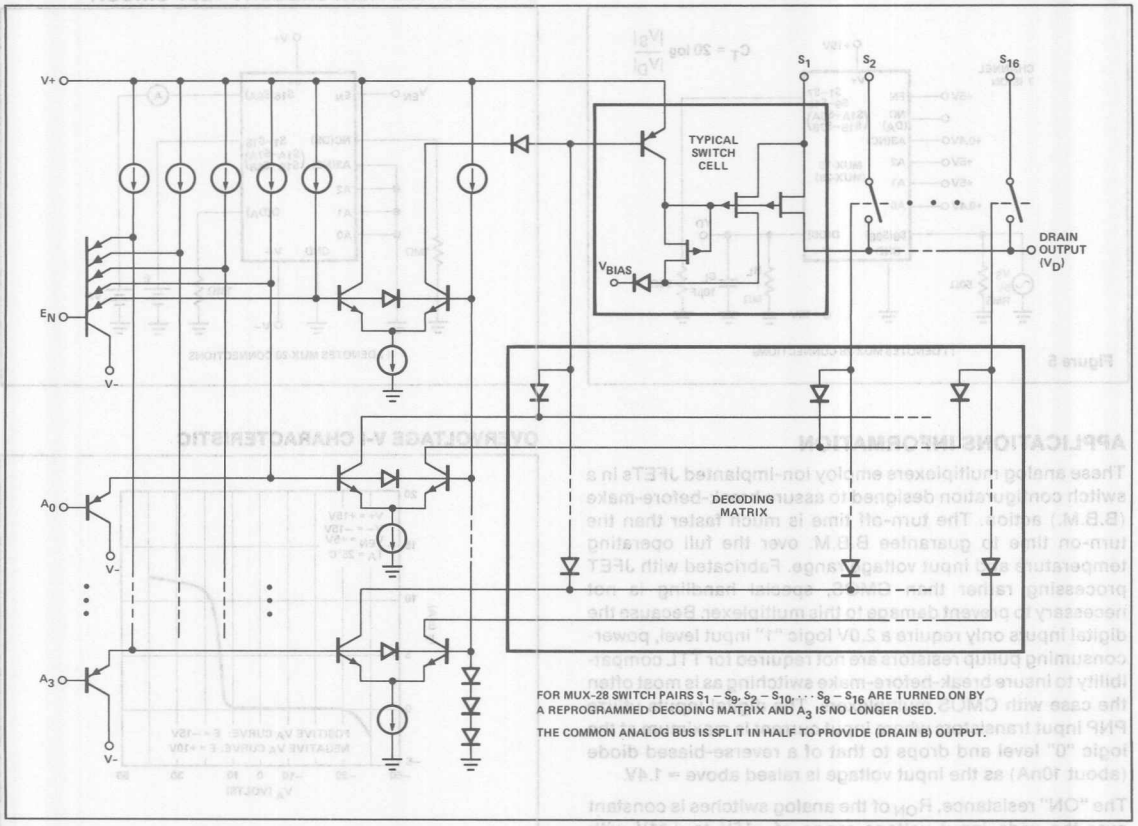
OVERVOLTAGE V-I CHARACTERISTIC



SUPPLY-LOSS V-I CHARACTERISTIC



SIMPLIFIED SCHEMATIC (MUX-16)



Dual Audio Analog Switches

SSM-2402/SSM-2412

FEATURES

- "Clickless" Bilateral Audio Switching
- Guaranteed "Break-Before-Make" Switching
- Low Distortion ..... 0.003% Typ
- Low Noise ..... 1nV/√Hz
- Superb OFF-Isolation ..... 120dB Typ
- Low ON-Resistance ..... 60Ω Typ
- Wide Signal Range:
  V_S = ±18V ..... 10V RMS
- Wide Power Supply Range ..... ±9V to ±20V
- Available in Dice Form

ORDERING INFORMATION

PACKAGE		OPERATING TEMPERATURE RANGE
PLASTIC 14-PIN	SOL 16-PIN	
SSM2402P	SSM2402S	XIND*
SSM2412P	SSM2412S	XIND*

*XIND = –40°C to +85°C

GENERAL DESCRIPTION

The SSM-2402/2412 are dual analog switches designed specifically for high-performance audio applications. Distortion and noise are negligible over the full audio operating range of 20Hz to 20kHz at signal levels of up to $10V_{RMS}$. The SSM-2402/2412 offer a monolithic integrated alternative to expensive and noisy relays or complex discrete JFET circuits. Unlike conventional general-purpose CMOS switches, the SSM-2402/2412 provide superb fidelity without audio "clicks" during switching.

Conventional TTL or CMOS logic can be used to control the switch state. No external pull-up resistors are needed. A "T" configuration provides superb OFF-isolation and true bilateral operation. The analog inputs and outputs are protected against overload and overvoltage.

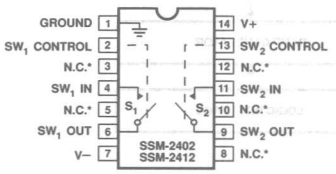
An important feature is the guaranteed "break-before-make" for **all** units, even IC-to-IC. In large systems with multiple switching channels, all separate switching units must open before any switch goes into the ON-state. With the SSM-2402/2412, you can be certain that multiple circuits will all break-before-make.

The SSM-2402/2412 represent a significant step forward in audio switching technology. Distortion and switching noise are significantly reduced in the new SSM-2402/2412 bipolar-JFET switches relative to CMOS switching technology. Based on a new circuit topology that optimizes audio performance, the SSM-2402/2412 make use of a proprietary bipolar-JFET process with thin-film resistor network capability. Nitride capacitors, which are very area efficient, are used for the proprietary ramp generator that controls the switch resistance transition. Very wide bandwidth amplifiers control the gate-to-source voltage over the full audio operating range for each switch. The ON-resistance remains constant with changes in signal amplitude and frequency, thus distortion is very low, less than 0.01% Max.

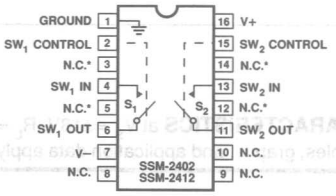
The SSM-2402 is the first analog switch truly optimized for high-performance audio applications. For broadcasting and other switching applications which require a faster switching time, we recommend the SSM-2412 – a dual analog switch with one-third of the switching time of the SSM-2402.

5

PIN CONNECTIONS



14-PIN PLASTIC DIP (P-Suffix)



16-PIN SOL (S-Suffix)

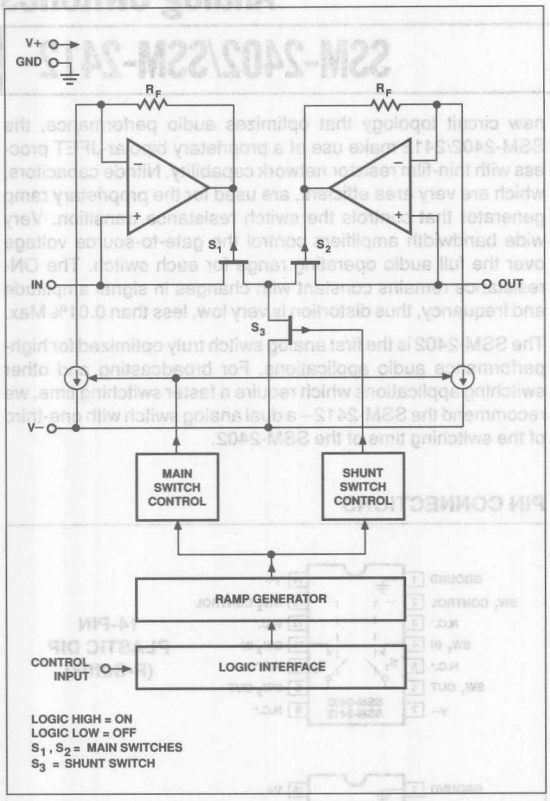
* GUARD PINS FOR INPUT/OUTPUT ISOLATION (GROUND FOR BEST PERFORMANCE)

CONTROL LOGIC

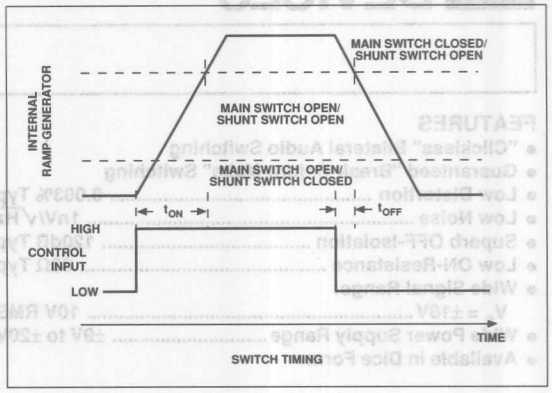
Logic In	Switch State
0	OFF
1	ON

Logic "0" ≤ 0.8V
Logic "1" ≥ 2.0V

FUNCTIONAL DIAGRAM



TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range ..... –40°C to +85°C
Operating Supply Voltage Range ..... ±20V
Analog Input Voltage Range
Continuous ..... V– +3.5V ≤ V_A ≤ V+ –3.5V
Maximum Current Through Switch 20mA
Logic Input Voltage Range ..... V+ Supply to –2V
V_A to V– Supply ..... +36V

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
14-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_S = ±18V, R_L = OPEN, and –40°C ≤ T_A ≤ +85°C, unless otherwise noted.

All specifications, tables, graphs, and application data apply to both the SSM-2402 and SSM-2412, unless otherwise noted.

			SSM-2402/2412			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Supply Current	$+I_{SY}$	V_{IL} = 0.8V, 2.0V (Note 1)	–	6.0	7.5	mA
Negative Supply Current	$-I_{SY}$	V_{IL} = 0.8V, 2.0V (Note 1)	–	4.8	6.0	mA
Ground Current	I_{GND}	V_{IL} = 0.8V, 2.0V (Note 1)	–	0.6	1.5	mA
Digital Input High	V_{INH}	T_A = Full Temperature Range (Note 2)	2.0	–	–	V
Digital Input Low	V_{INL}	T_A = Full Temperature Range	–	–	0.8	V
Logic Input Current	I_{LOGIC}	V_{IN} = 0 to 15V (Note 3)	–	1.0	5.0	µA
Analog Voltage Range (Note 3)	V_{ANALOG}		–14.2	–	+14.2	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 18V$, R_L = OPEN, and $-40°C \le T_A \le +85°C$, unless otherwise noted. *Continued*

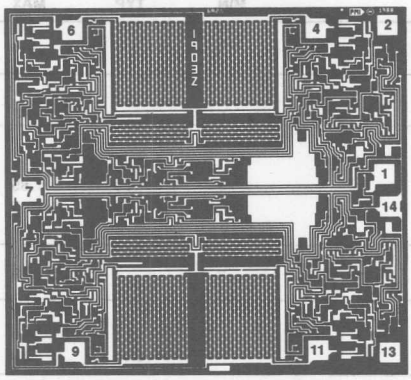
PARAMETER	SYMBOL	CONDITIONS		SSM-2402/2412 MIN	TYP	MAX	UNITS
Analog Current Range (Note 3)	I_{ANALOG}			–10	–	+10	mA
Overvoltage Input Current		$V_{IN} = \pm V_{SUPPLY}$		–	±40	–	mA
Switch ON Resistance	R_{ON}	$-14.2 \le V_A \le +14.2V$ $I_A = \pm 10mA$, $V_{IL} = 2.0V$ $T_A = +25°C$ T_A = Full Temperature Range Tempco ($\Delta R_{ON}/\Delta T$)		– – –	60 – 0.2	85 115 –	Ω Ω Ω/°C
R_{ON} Match	R_{ON}MATCH	$-14.2 \le V_A \le +14.2V$ $I_A = \pm 10mA$, $V_{IL} = 2.0V$		–	1	5	%
Switch ON Leakage Current (Notes 1, 3)	$I_{S(ON)}$	$V_{IL} = 2.0V$ $-14.2V \le V_A \le +14.2V$ $V_A = 0V$		– –	0.05 0.05	1.0 10.0	µA nA
Switch OFF Leakage Current (Notes 1, 3)	$I_{S(OFF)}$	$V_{IL} = 0.8V$ $-14.2V \le V_A \le +14.2V$ $V_A = 0V$		– –	0.05 0.05	1.0 10.0	µA nA
Turn-On Time (Note 5)	t_{ON}	$V_A = +10V$, $R_L = 2k\Omega$ $T_A = +25°C$, See Test Circuit	SSM-2402 SSM-2412	– –	10.0 3.5	– –	ms
Turn-Off Time (Note 6)	t_{OFF}	$V_A = +10V$, $R_L = 2k\Omega$ $T_A = +25°C$, See Test Circuit	SSM-2402 SSM-2412	– –	4.0 1.5	– –	ms
Break-Before-Make Time Delay (Note 7)	$t_{OFF} - t_{ON}$	$T_A = +25°C$	SSM-2402 SSM-2412	– –	6.0 2.0	– –	ms
Charge Injection	Q	$T_A = +25°C$	SSM-2402 SSM-2412	– –	50 150	– –	pC
ON-State Input Capacitance	$CS_{(ON)}$	$V_A = 1V_{RMS}$ f = 5kHz, $T_A = +25°C$		–	12	–	pF
OFF-State Input Capacitance	$CS_{(OFF)}$	$V_A = 1V_{RMS}$ f = 5kHz, $T_A = +25°C$		–	4	–	pF
OFF Isolation	$I_{SO(OFF)}$	$V_A = 10V_{RMS}$, 20Hz to 20kHz $T_A = +25°C$, See Test Circuit		–	120	–	dB
Channel-to-Channel Crosstalk	C_T	$V_A = 10V_{RMS}$, 20Hz to 20kHz $T_A = +25°C$		–	96	–	dB
Total Harmonic Distortion (Note 8)	THD	0 to $10V_{RMS}$, 20Hz to 20kHz $T_A = +25°C$, $R_L = 5k\Omega$		–	0.003	0.01	%
Spectral Noise Density	e_n	20Hz to 20kHz $T_A = +25°C$		–	1	–	$nV/\sqrt{Hz}$
Wideband Noise Density	$e_{n\,p\text{-}p}$	20Hz to 20kHz $T_A = +25°C$		–	0.2	–	$\mu V_{p\text{-}p}$

NOTES:
1. "V_{IL}" is the Logic Control Input.
2. Although not recommended, using unbalanced supplies with the positive rail in excess of 20V will result in an increased digital input high threshold. The threshold is set to 9.3% of the positive supply voltage.
3. Current tested at $V_{IN} = 0V$. This is the worst case condition.
4. Guaranteed by R_{ON} test condition.
5. Turn-ON Time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the final value.
6. Turn-OFF time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the initial value.
7. Switch is guaranteed by design to provide break-before-make operation.
8. THD guaranteed by design and dynamic R_{ON} testing.

5

DICE CHARACTERISTICS

SSM-2402/SSM-2412



DIE SIZE 0.105 x 0.097 inch, 10,185 sq. mils
(2.667 x 2.464 mm, 6.57 sq. mm)

1. GROUND
2. SWITCH$_1$ CONTROL
4. SWITCH$_1$ IN
6. SWITCH$_1$ OUT
7. V– SUPPLY
9. SWITCH$_2$ IN
11. SWITCH$_2$ OUT
13. SWITCH$_2$ CONTROL
14. V+ SUPPLY

For additional DICE information, refer to PMI's Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 18V$, R_L = OPEN, and $T_A = +25°C$.

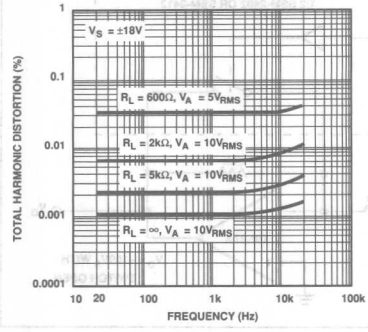
PARAMETER	SYMBOL	CONDITIONS (Note 1)	SSM-2402/2412NBC LIMIT	UNITS
Positive Supply Current	$+I_{SY}$	$V_{IL} = 0.8V$	7.5	mA MAX
Negative Supply Current	$-I_{SY}$	$V_{IL} = 0.8V$	6.0	mA MAX
Ground Current	I_{GND}	$V_{IL} = 0.8V$	1.5	mA MAX
Logic Input Current	I_{LOGIC}	$V_{IN} = 0V$ (Note 2)	5.0	µA MAX
Switch ON Resistance	R_{ON}	$-14.2 \le V_A \le +14.2V$, $I_A = \pm 10mA$, $V_{IL} = 2.0V$	85	Ω MAX
R_{ON} Match Between Switches	R_{ON}MATCH	$-14.2V \le V_A \le +14.2V$, $I_A = \pm 10mA$, $V_{IL} = 2.0V$	5	% MAX
Switch ON Leakage Current	$I_{S(ON)}$	$-14.2V \le V_A \le +14.2V$, $V_{IL} = 2.0V$	1.0	µA MAX
Switch OFF Leakage Current	$I_{S(OFF)}$	$-14.2V \le V_A \le +14.2V$, $V_{IL} = 0.8V$	1.0	µA MAX

NOTES:
1. V_{IL} = Logic Control Input
   V_A = Applied Analog Input Voltage
   I_A = Applied Analog Input Current
2. Worst Case Condition

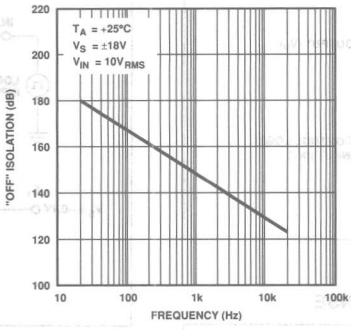
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

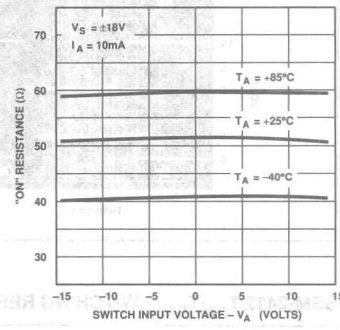
TOTAL HARMONIC DISTORTION vs FREQUENCY



"OFF" ISOLATION vs FREQUENCY

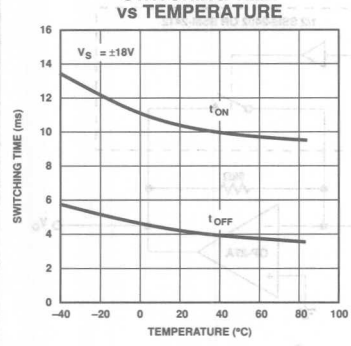


"ON" RESISTANCE vs ANALOG VOLTAGE

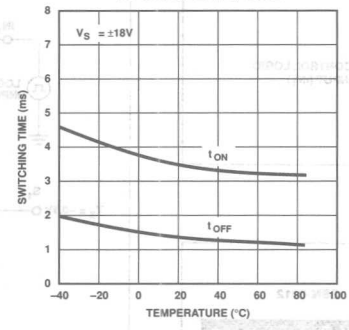


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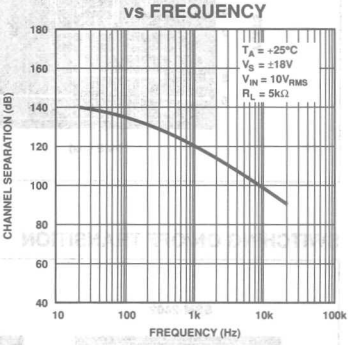
SSM-2402 SWITCHING TIME vs TEMPERATURE



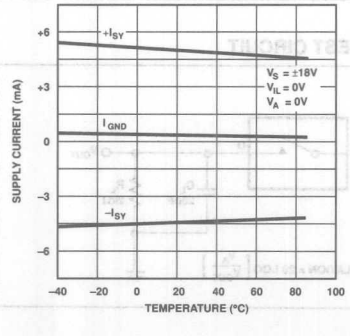
SSM-2412 SWITCHING TIME vs TEMPERATURE



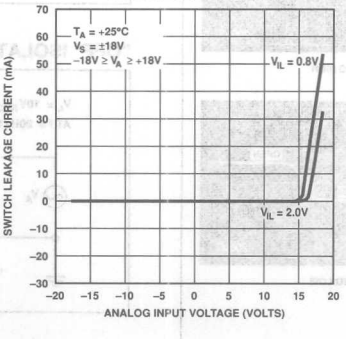
CHANNEL SEPARATION vs FREQUENCY



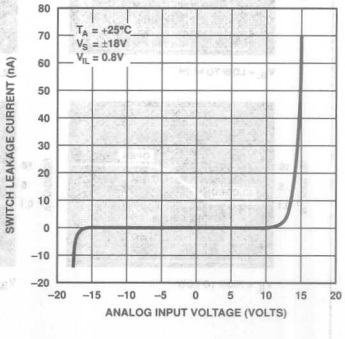
SUPPLY CURRENT vs TEMPERATURE



OVERVOLTAGE CHARACTERISTICS

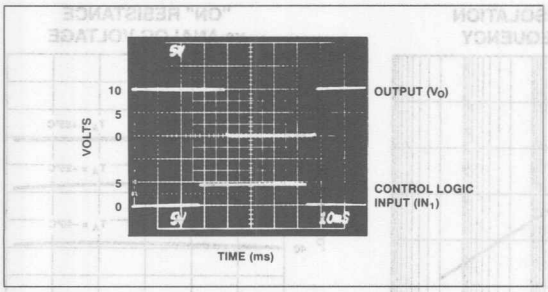


LEAKAGE CURRENT vs ANALOG VOLTAGE

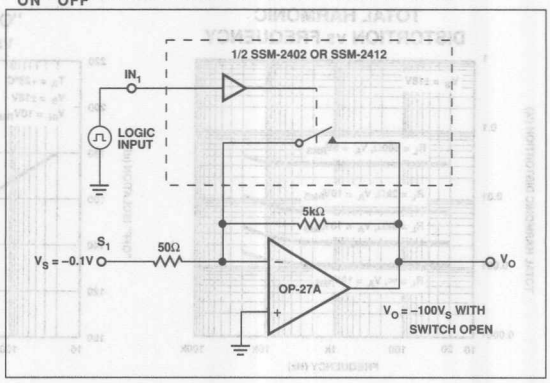


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

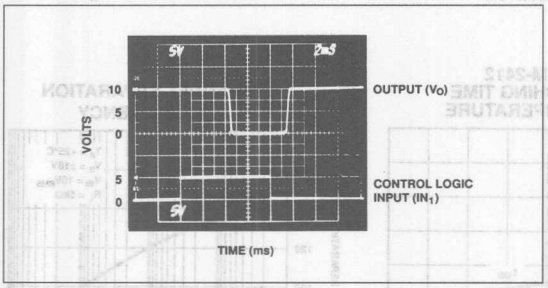
SSM-2402 T_{ON}/T_{OFF} SWITCHING RESPONSE



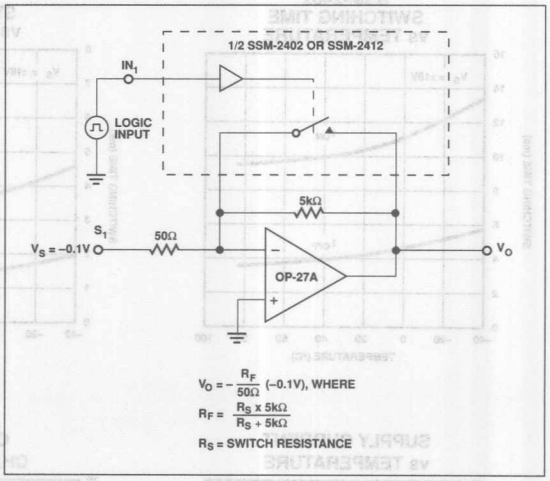
T_{ON}/T_{OFF} SWITCHING RESPONSE TEST CIRCUIT



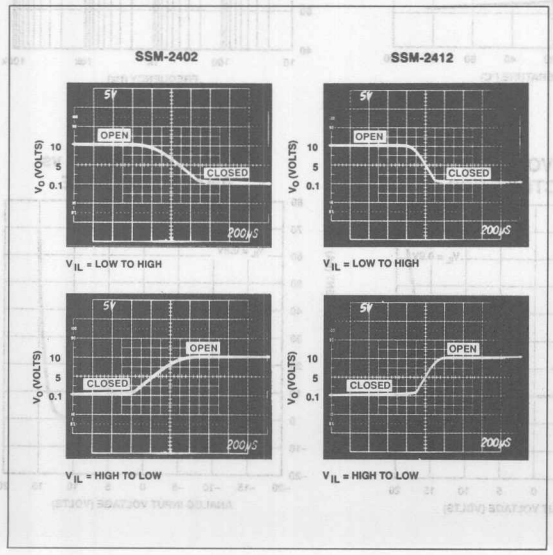
SSM-2412 T_{ON}/T_{OFF} SWITCHING RESPONSE



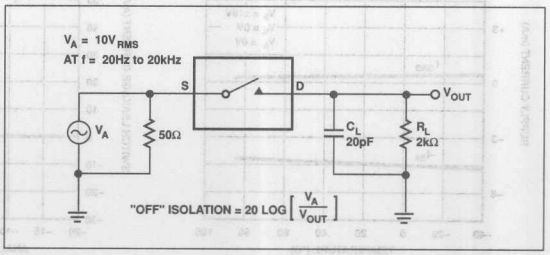
SWITCH ON/OFF TRANSITION TEST CIRCUIT



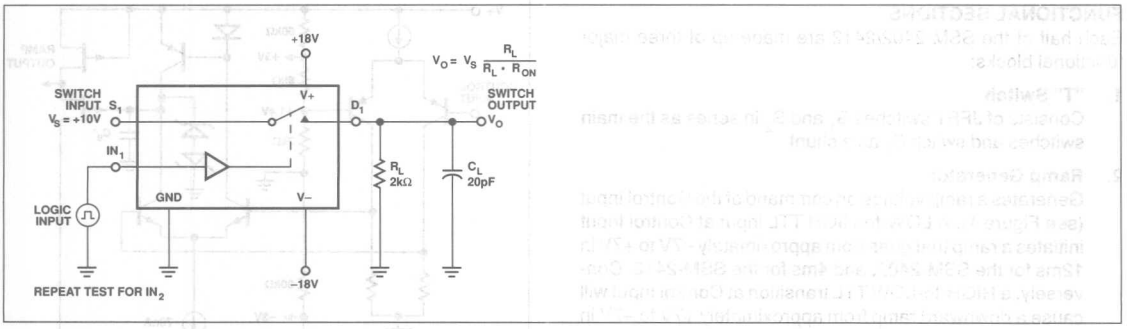
SWITCHING ON/OFF TRANSITION



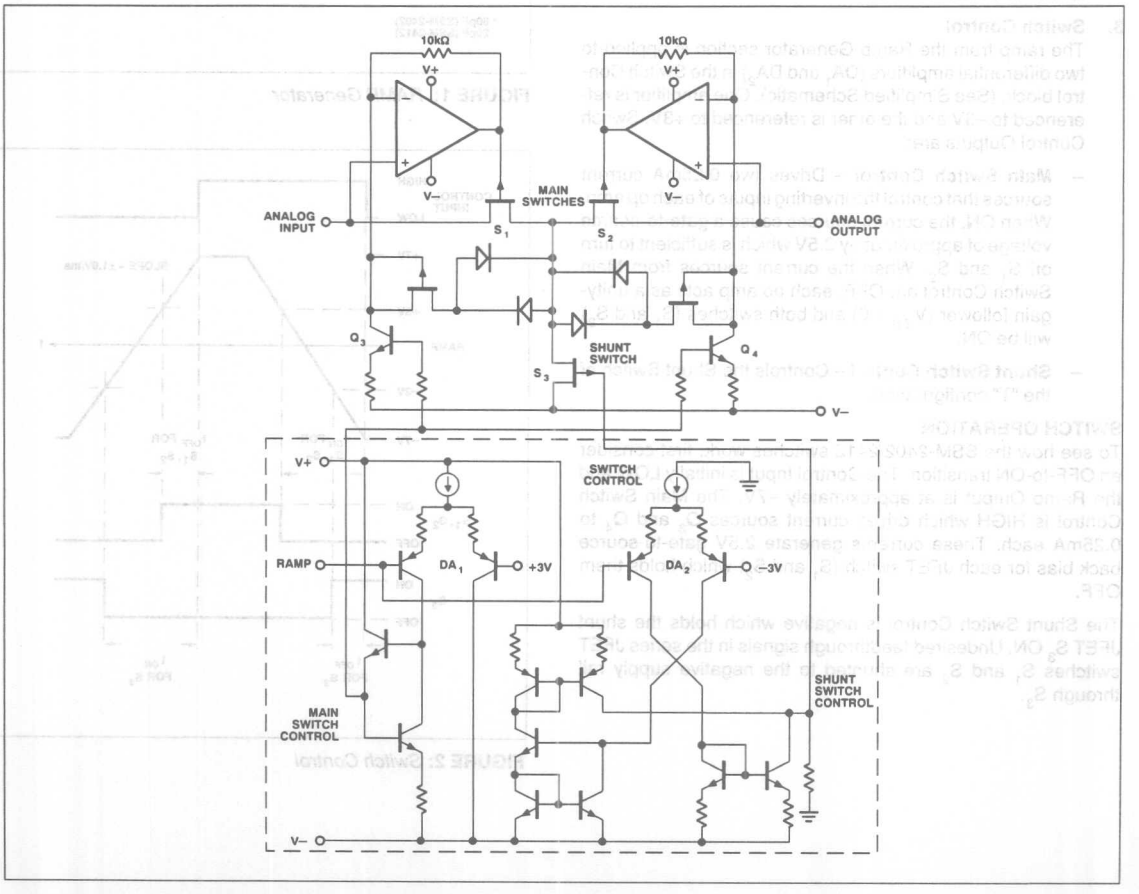
"OFF" ISOLATION TEST CIRCUIT



SWITCHING TIME TEST CIRCUIT



SIMPLIFIED SCHEMATIC



5

APPLICATIONS INFORMATION

FUNCTIONAL SECTIONS

Each half of the SSM-2402/2412 are made up of three major functional blocks:

1. **"T" Switch**
   Consists of JFET switches S_1 and S_2 in series as the main switches and switch S_3 as a shunt.

2. **Ramp Generator**
   Generates a ramp voltage on command of the Control Input (see Figure 1). A LOW-to-HIGH TTL input at Control Input initiates a ramp that goes from approximately –7V to +7V in 12ms for the SSM-2402, and 4ms for the SSM-2412. Conversely, a HIGH-to-LOW TTL transition at Control Input will cause a downward ramp from approximately +7V to –7V in 12ms for the SSM-2402, and 4ms for the SSM-2412. The Ramp Generator also supplies the +3V and –3V reference levels for Switch Control.

3. **Switch Control**
   The ramp from the Ramp Generator section is applied to two differential amplifiers (DA_1 and DA_2) in the Switch Control block. (See Simplified Schematic). One amplifier is referenced to –3V and the other is referenced to +3V. Switch Control Outputs are:

   – **Main Switch Control** – Drives two 0.25mA current sources that control the inverting inputs of each op amp. When ON, the current sources cause a gate-to-source voltage of approximately 2.5V which is sufficient to turn off S_1 and S_2. When the current sources from Main Switch Control are OFF, each op amp acts as a unity-gain follower ($V_{GS} = 0$) and both switches (S_1 and S_2) will be ON.

   – **Shunt Switch Control** – Controls the Shunt Switch of the "T" configuration.

SWITCH OPERATION

To see how the SSM-2402/2412 switches work, first consider an OFF-to-ON transition. The Control Input is initially LOW and the Ramp Output is at approximately –7V. The Main Switch Control is HIGH which drives current sources Q_3 and Q_4 to 0.25mA each. These currents generate 2.5V gate-to-source back bias for each JFET switch (S_1 and S_2) which holds them OFF.

The Shunt Switch Control is negative which holds the shunt JFET S_3 ON. Undesired feedthrough signals in the series JFET switches S_1 and S_2 are shunted to the negative supply rail through S_3.

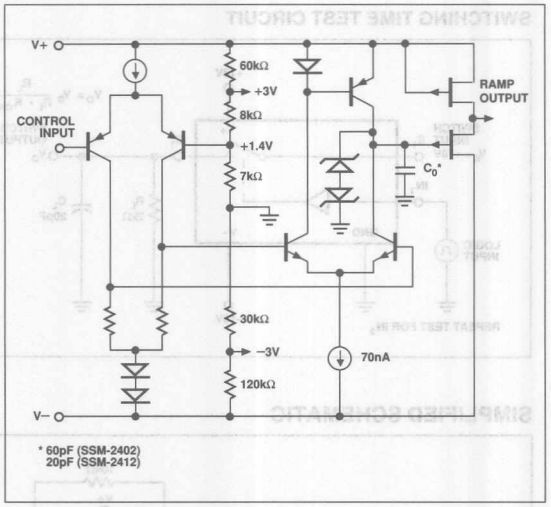


FIGURE 1: *RAMP Generator*

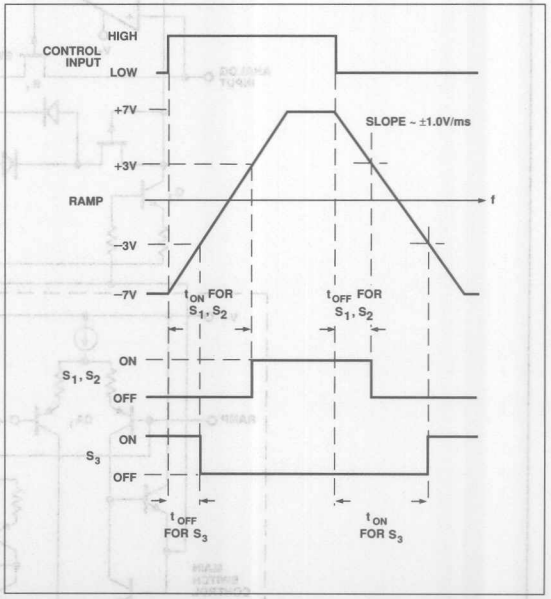


FIGURE 2: *Switch Control*

When the Control Input goes from LOW to HIGH, the Ramp Generator slews in the positive direction as shown in Figure 2. When the ramp goes more positive than –3V, the Shunt Switch Control is pulled positive by differential amplifier DA_2 which thereby puts shunt switch S_3 into the OFF state. Note that S_1 and S_2 are still OFF, so at this time all three switches in the "T" are OFF.

When the Ramp Output reaches +3V, and the drive for the Main Switch Control output is gated OFF by differential amplifier DA_1, current sources Q_3 and Q_4 go to the OFF state and the V_{GS} of each main switch goes to zero. The high-speed op amp followers provide essentially zero gate-to-source voltage over the full audio signal range; this in turn assures a constant low impedance in the ON state over the full audio signal range. Total time to turn on the SSM-2402 switch is approximately 10.0ms and 3.5ms for the SSM-2412.

In systems using a large number of separate switches, there are advantages to having faster switching into OFF state than into the ON state. Break-before-make can be maintained at the system level. To see how the SSM-2402/2412 guarantee break-before-make, consider the ON-to-OFF transition.

A Control Input LOW initiates the ON-to-OFF transition. The Ramp Generator integrates down from approximately +7V towards –7V. As the ramp goes through +3V, the comparator controlling the Main Switches (S_1 and S_2) goes HIGH and turns on current sources Q_3 and Q_4 which thereby puts S_1 and S_2 into the OFF state. At this time, all switches in the "T" are OFF. When the ramp integrates down to –3V, the Shunt Switch Control changes state and pulls shunt switch S_3 into the ON state. This completes the ON-to-OFF transistion; S_1 and S_2 are OFF, and S_3 is ON to shunt away any undesired feedthrough. Note though that the ON-to-OFF time for main switches S_1 and S_2 is only the time interval required for the ramp to go from +7V to +3V, about 4ms for the SSM-2402, and 1.5ms for the SSM-2412. The time to turn on is about 2.5 times as long as the time to turn off.

The SSM-2402/2412 are much more than a simple single solid-state switches. The "T" configuration provides superb OFF-isolation through shunting of feedthrough via shunt switch S_3. Break-before-make is inherent in the design. The ramp provides a controlled gating action that softens the ON/OFF transitions. Distortion is minimized by holding zero gate-to-source voltage for the two main FET switches, S_1 and S_2, using the two op amp followers. Figure 3 shows a distortion comparison between the SSM-2402 and a typical CMOS switch. In summary, the SSM-2402/2412 are designed specifically for high-performance audio system usage.

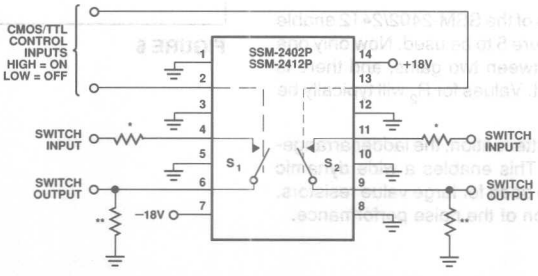
OVERVOLTAGE PROTECTION

The SSM-2402/2412 are designed to guarantee correct operation with inputs of up to ±14.2V with ±18V supplies. The switch input should never be forced to go beyond the supply rails. In the OFF condition, if the inputs exceeds +14.2V, there is a risk of turning the respective input pass FET "ON." When the input voltage rises to within 3.8V of the positive supply, the op amp follower saturates and will not be able to maintain the full 2.5V of back bias on the gate-to-source junction. Under this condition, current will flow from the input through the shunt FET to the negative supply. This current is substantial, but is limited by the FET I_{DSS}. Although this current will not damage the device, there is a danger of also turning on the output pass FET, especially if the output is close to the negative rail.

This risk of signal "breakthrough" for inputs above +14.2V can be eliminated by using a source resistor of 100-500Ω in series with the analog input to provide additional current limiting.

Near the negative supply, transistors Q_3 and Q_4 saturate and can no longer keep the switch OFF. Signal breakthrough cannot happen, but the danger here is latch-up via a path to V– through the shunt FET. Additional circuitry (not shown) has been incorporated to turn OFF the shunt FET under these conditions, and the potential for latch-up is thereby eliminated.

TYPICAL CONFIGURATION



* OPTIONAL INPUT RESISTORS
SEE SECTION ON OVERVOLTAGE PROTECTION

** OPTIONAL LOAD RESISTORS
LOWER VALUES WILL MINIMIZE "CLICKS" BUT WITH A $10V_{RMS}$ INPUT
IT IS RECOMMENDED THAT THEY BE GREATER THAN 2kΩ

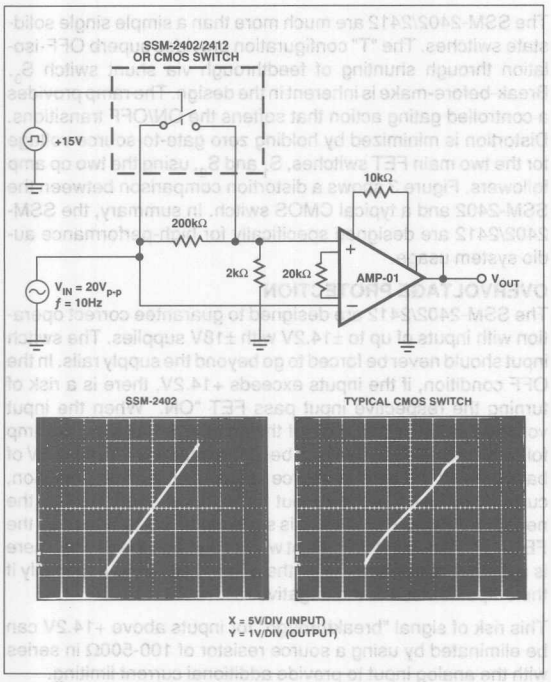


FIGURE 3: *Comparison of the SSM-2402 and Typical CMOS Switch for Distortion*

DIGITALLY-CONTROLLED ATTENUATOR

Figure 4 shows the usual approach to digitally-controlled attenuation. With S_1 closed, the signal passes unattenuated to the output. With S_1 open and S_2 closed, the signal is attenuated by R_1 and R_2. The advantage of this configuration is that the attenuator current does not have to flow through the switches. The disadvantage is that the output is undefined during the switching period, which can be several milliseconds.

The low distortion characteristics of the SSM-2402/2412 enable the alternate arrangement of Figure 5 to be used. Now only one switch is required to change between two gains, and there is always a signal path to the output. Values for R_2 will typically be in the low kilohm range.

For more gain steps and higher attenuation, the ladder arrangement of Figure 6 can be used. This enables a wide dynamic range to be achieved without the need for large value resistors, which would result in degradation of the noise performance.

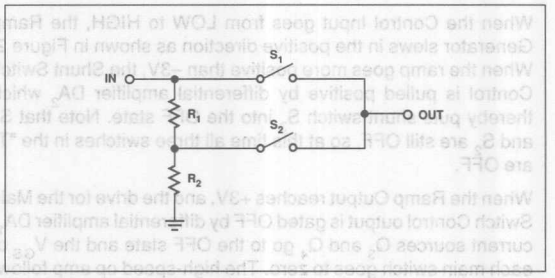


FIGURE 4

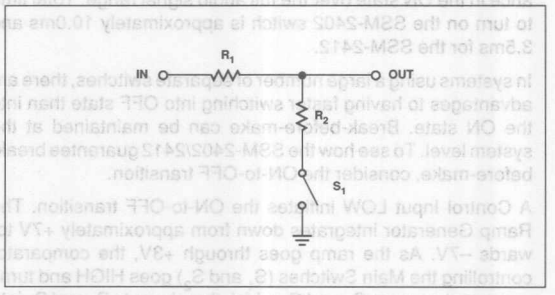


FIGURE 5

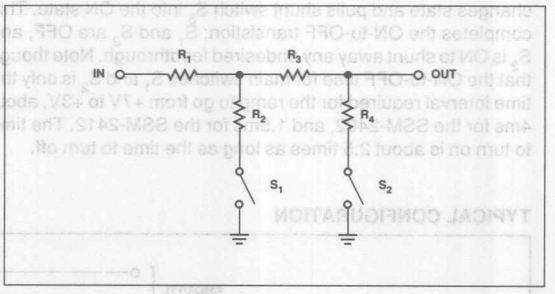


FIGURE 6

HIGH-PERFORMANCE STEREO ROUTING SWITCHER

The SSM-2402 Dual Audio Switch comprises the nucleus for this 16 channels-to-one high performance stereo audio routing switcher, which features negligible noise and low distortion over the frequency range of 20Hz to 20kHz. This performance is achieved even while driving 600Ω loads at signal levels up to +30dBu.

The SSM-2402 affords a much simplified electrical design and printed circuit board layout, along with reduced manufacturing cost, when compared with discrete JFET circuits of similar performance. The electrical performance of the design described is vastly superior to CMOS switch designs, which are more prone to failure resulting from electrical static discharge.

The switching control of the SSM-2402 may be activated by conventional mechanical switches or 5 volt TTL or CMOS logic circuits. The application shown utilizes a simple mechanical control switch for illustration purposes only. Many diverse X/Y control schemes, destination control, or computer controlled designs can be utilized.

The "T" configuration of the SSM-2402 switch provides excellent ON-OFF isolation. The SSM-2402 also features 7ms ramped turn on and 4ms ramped turn off for click-free switching. Additionally, the switch has a break-before-make switching sequence. Both features become significant in large audio switching systems where the audio path can pass through multiple switching elements. Such controlled switching is very important in large systems used in broadcast program switching or in production work.

The application circuit design also employs the SSM-2015 balanced input amplifier (Figure 7). The input impedance is high (≈100kΩ), balanced or unbalanced. The input circuit incorporates a single pole RFI filter with a cutoff frequency set at 145kHz. In addition, the input circuit attenuates the signal by 25dB and extends the common-mode input voltage range to ±98 volts peak, with common-mode rejection greater than 70dB from 20Hz to 20kHz. The SSM-2015 is set to produce a 15dB gain. The signal drive level into the SSM-2402 switch is then +10dBu with a +20dBu input level and +14dBu peak, well within

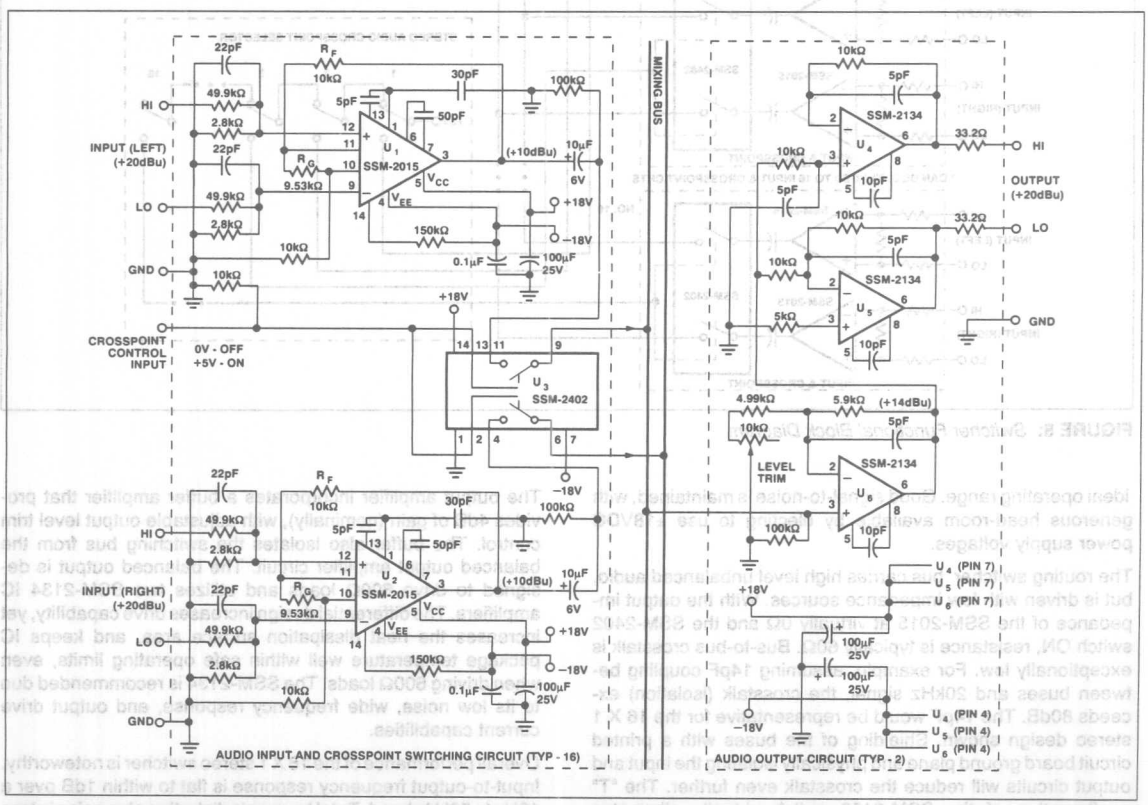


FIGURE 7: *Switcher Schematic*

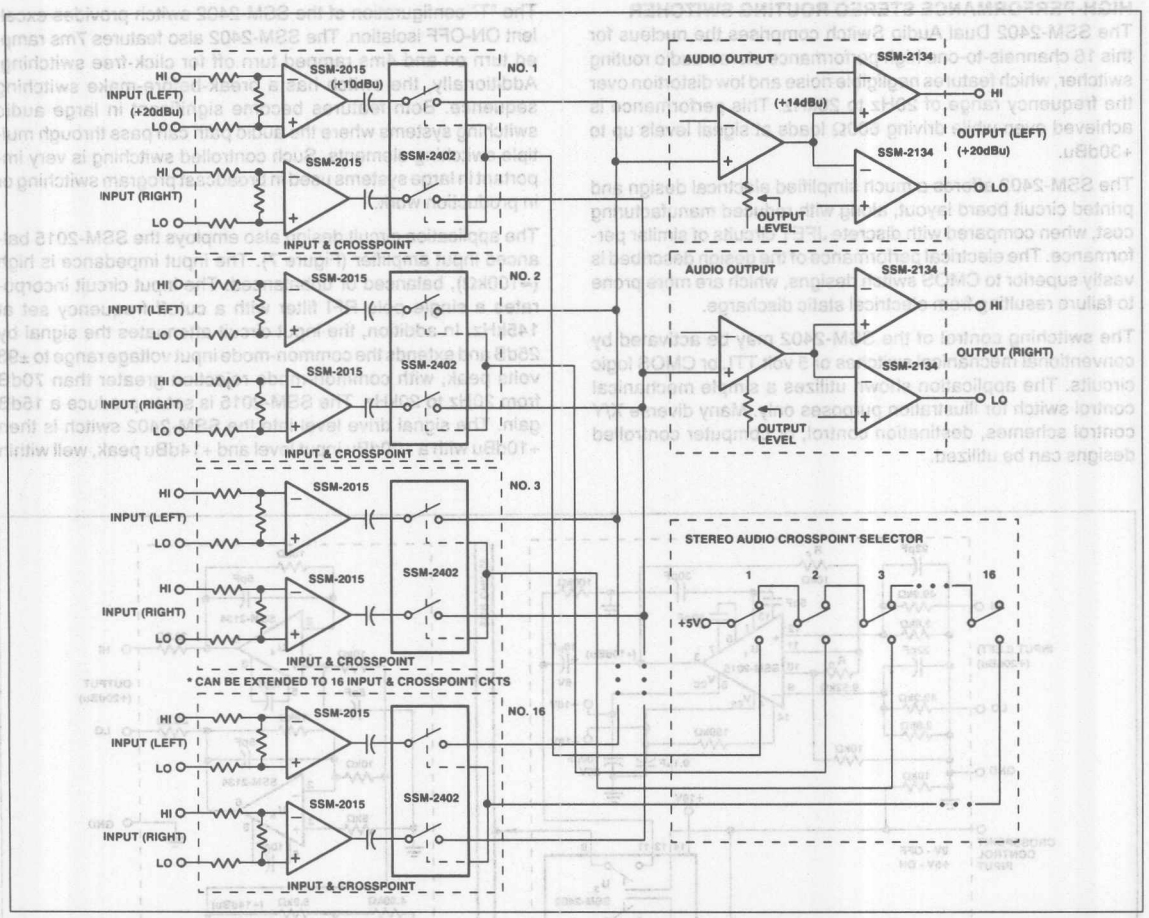


FIGURE 8: *Switcher Functional Block Diagram*

ideal operating range. Good signal-to-noise is maintained, with generous head-room available by electing to use ±18VDC power supply voltages.

The routing switcher bus carries high level unbalanced audio, but is driven with low impedance sources. With the output impedance of the SSM-2015 at virtually 0Ω and the SSM-2402 switch ON, resistance is typically 60Ω. Bus-to-bus crosstalk is exceptionally low. For example, assuming 14pF coupling between buses and 20kHz signal, the crosstalk (isolation) exceeds 80dB. The 14pF would be representative for the 16 X 1 stereo design shown. Shielding of the buses with a printed circuit board ground plane and physically isolating the input and output circuits will reduce the crosstalk even further. The "T" configuration of the SSM-2402 switch virtually eliminates crosstalk between the various input signal sources.

The output amplifier incorporates a buffer amplifier that provides 4dB of gain (nominally), with adjustable output level trim control. The buffer also isolates the switching bus from the balanced output amplifier circuit. The balanced output is designed to drive 600Ω loads and utilizes two SSM-2134 IC amplifiers. The differential design increases drive capability, yet increases the heat dissipation surface area, and keeps IC package temperature well within safe operating limits, even when driving 600Ω loads. The SSM-2134 is recommended due to its low noise, wide frequency response, and output drive current capabilities.

Overall performance of the 16 X 1 stereo switcher is noteworthy. Input-to-output frequency response is flat to within 1dB over a 10Hz to 50kHz band. Total harmonic distortion plus noise is less than 0.03%, from 20Hz to 20kHz. SMPTE intermodulation distortion is less than 0.02%. The use of ±18VDC power supplies produces a +30dBm clip level, even when driving 600Ω loads.

TABLE 1: Circuit Performance Specifications

Max Input Level	+30dBu
Input Impedance, Unbalanced	100kΩ
Input Impedance, Balanced	200kΩ
Common-Mode Rejection (20Hz to 20kHz)	>70dB
Common-Mode Voltage Limit	±98V Peak
Max Output Level	+30dBu/dBm
Output Impedance	67Ω
Gain Control Range	±2dB
Output Voltage Slew Rate	6V/μs
Frequency Response (±0.05dB)	20Hz to 20kHz
Frequency Response (±0.5dB)	10Hz to 50kHz
THD + Noise (20Hz to 20kHz, +8dBu)	0.005%
THD + Noise (20Hz to 20kHz, +24dBu)	0.03%
IMD (SMPTE 60Hz & 4kHz, 4:1, +24dBu)	0.02%
Crosstalk (20Hz to 20kHz)	>80dB
S/N Ratio @ 0dB Gain	135dB

ANALOG DEVICES

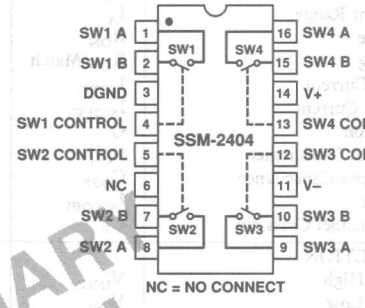
Quad Audio Switch

SSM-2404

FEATURES

- "Clickless" Bilateral Audio Switching
- Four SPST Switches in a 16-Pin Package
- Ultralow THD+N: 0.0009% @ 1 kHz (V_{IN} = 2 V rms, R_L = 100 kΩ)
- Low Charge Injection: 35 pC
- High OFF Isolation: 100 dB
- Low ON Resistance: 28 Ω
- Low Supply Current: 900 μA
- Single or Dual Supply Operation: +11 V to +24 V or ±5.5 V to ±12 V
- Guaranteed Break-Before-Make
- TTL and CMOS Compatible Logic Inputs
- Low Cost-Per-Switch

PIN CONNECTIONS



NC = NO CONNECT

PRELIMINARY TECHNICAL DATA

5

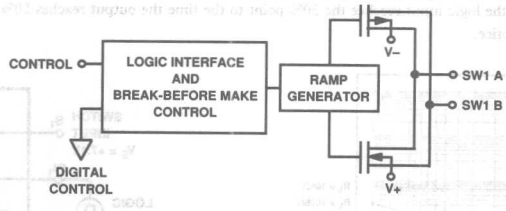
GENERAL DESCRIPTION

The SSM-2404 integrates four SPST analog switches in a single 16-pin package. Developed specifically for high performance audio applications, distortion and noise are negligible over the full operating range of 20 Hz to 20 kHz. With very low charge injection of 35 pC, "clickless" audio switching is possible, even under the most demanding conditions.

Switch control is realized by conventional TTL or CMOS logic. Guaranteed "break-before-make" operation assures that all switches in a large system will open before any switch reaches the ON state.

Single or dual supply operation is possible. Additional features include 100 dB OFF isolation, 28 Ω ON resistance, and a wide signal handling range. Although optimized for virtual ground switching, the SSM-2404 maintains good audio performance even under low load impedance conditions.

BLOCK DIAGRAM OF ONE SWITCH CHANNEL



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Total Harmonic Distortion Plus Noise	THD+N	@ 1 kHz, with 80 kHz Filter, R_L = 100 kΩ, V_{IN} = 2 V rms	0.0009	%
Spectral Noise Density	e_n	20 Hz to 20 kHz	0.8	nV/√Hz
Wideband Noise Density	e_n p–p	20 Hz to 20 kHz	0.6	μV p–p
ANALOG SIGNAL SECTION				
Analog Voltage Range	V_A	V_{INH} = 2 V, I_A = ±2 mA	±12	V
Analog Current Range	I_A	V_{INH} = 2 V, V_A = 0 V	±10	mA
ON Resistance	R_{ON}	I_A = ±10 mA, V_A = 7.1 V	28	Ω
R_{ON} Matching	R_{ON} Match	I_A = ±10 mA, V_A = 0 V	1	%
ON Leakage Current	$I_{S(ON)}$	V_A = 7.1 V	0.1	nA
OFF Leakage Current	$I_{S(OFF)}$	V_A = 7.1 V	0.1	nA
Charge Injection	Q		35	pC
ON-State Input Capacitance	C_{ON}	V_A = 5 V rms, f = 5 kHz	31	pF
OFF-State Input Capacitance	C_{OFF}	V_A = 5 V rms, f = 5 kHz	17	pF
OFF Isolation	$I_{SO(OFF)}$	V_A = 7.1 V, 20 Hz–20 kHz	100	dB
Channel-to-Channel Crosstalk	C_T	V_A = 7.1 V, 20 Hz–20 kHz	100	dB
CONTROL SECTION				
Digital Input High	V_{INH}	T_A = −40°C to +85°C	2.0	V
Digital Input Low	V_{INL}	T_A = −40°C to +85°C	0.8	V
Turn-On Time[1]	t_{ON}	See Test Circuit	8	ms
Turn-Off Time[2]	t_{OFF}	See Test Circuit	5	ms
Break-Before-Make Time Delay	t_{OFF}–t_{ON}		3	ms
Logic Input Current				
Logic HI		V_{INH} = 2 V	1.3	nA
Logic LO		V_{INL} = 0.8 V	1.0	nA
POWER SUPPLY				
Supply Voltage Range	V_S	Single Supply	+11 to +24	V
		Dual Supply	±5.5 to ±12	V
Positive Supply Current	I_{SY+}	All Channels On	0.9	mA
Negative Supply Current	I_{SY-}	All Channels On	−0.6	mA
Ground Current		All Channels On	−0.3	mA

PRELIMINARY TECHNICAL DATA

NOTES
[1]Turn-on time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the final value.
[2]Turn-off time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the initial value.
Specifications subject to change without notice.

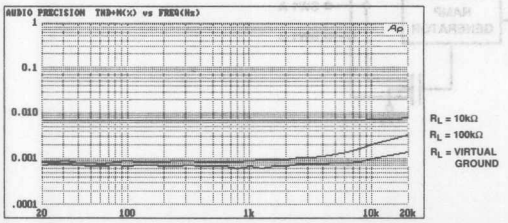
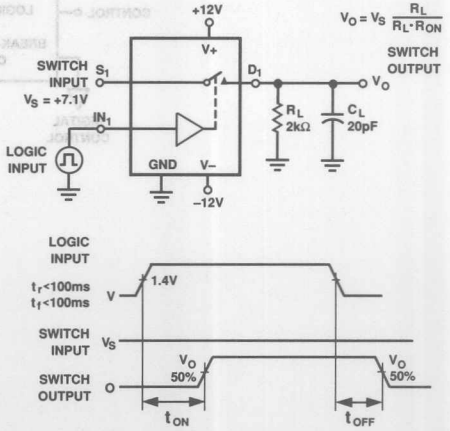


Figure 1. THD+N vs. Frequency (V_S = ±12 V, V_{IN} = 2 V rms, with 80 kHz Filter)



SSM-2404 Switch Timing Circuit

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Quad SPST JFET Analog Switch

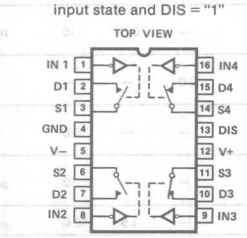
SW-06

FEATURES

- **Two Normally Open and Two Normally Closed SPST Switches with Disable**
- **Switches can be Easily Configured as a Dual SPDT or a DPDT**
- **Highly Resistant to Static Discharge Destruction**
- **Higher Resistance to Radiation Than Analog Switches Designed with MOS Devices**
- **Guaranteed R_{ON} Matching ..... 10% Max**
- **Guaranteed Switching Speeds ..... T_{ON} = 500ns Max**
  T_{OFF} = 400ns Max
- **Guaranteed Break-Before-Make Switching**
- **Low "ON" Resistance ..... 80Ω Max**
- **Low R_{ON} Variation from Analog Input Voltage 5%**
- **Low Total Harmonic Distortion 0.01%**
- **Low Leakage Currents at High Temperature:**
  T_A = 125° C ..... 100nA Max
  T_A = 85° C ..... 30nA Max
- **Digital Inputs TTL/CMOS Compatible and Independent of V+**
- **Improved Specifications and Pin Compatible to LF-11333/13333**
- **Dual or Single Power Supply Operation**
- **Available in Die Form**

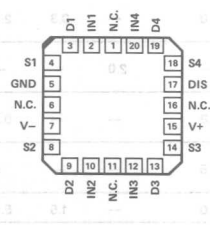
PIN CONNECTIONS

Switches are shown in the logic "0" input state and DIS = "1"



16-PIN DIP
(Q or P-Suffix)

16-PIN SOL
(S-Suffix)



SW-06BRC/883
LCC PACKAGE
(RC-Suffix)

ORDERING INFORMATION †

PLASTIC 16-PIN	CERDIP 16-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
–	SW06BQ*	SW06BRC/883	MIL
SW06GP	SW06FQ	–	XIND
SW06GS	–	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

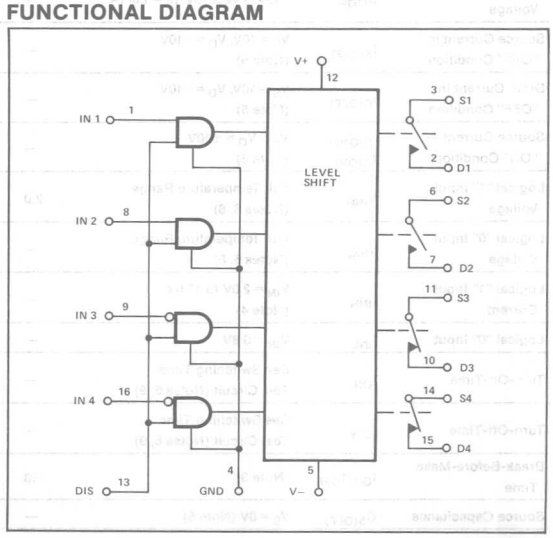
The SW-06 is a four channel single-pole, single-throw analog switch that employs both bipolar and ion-implanted FET devices. The SW-06 FET switches use bipolar digital logic inputs which are more resistant to static electricity than CMOS devices. Ruggedness and reliability are inherent in the SW-06 design and construction technology.

Increased reliability is complemented by excellent electrical specifications. Potential error sources are reduced by minimizing "ON" resistance and controlling leakage currents at high temperatures. The switching FET exhibits minimal R_{ON} variation over a 20V analog signal range and with power supply voltage changes. Operation from a single positive power supply voltage is possible. With V+ = 36V, V– = 0V, the analog signal range will extend from ground to +32V.

PNP logic inputs are TTL and CMOS compatible to allow the SW-06 to upgrade existing designs. The logic "0" and logic "1" input currents are at micro-ampere levels reducing loading on CMOS and TTL logic.

5

FUNCTIONAL DIAGRAM



TRUTH TABLE

DISABLE INPUT	LOGIC INPUT	SWITCH STATE CHANNELS 1 & 2	SWITCH STATE CHANNELS 3 & 4
0	X	OFF	OFF
1 or NC	0	OFF	ON
1 or NC	1	ON	OFF

ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature Range
- SW-06BQ, BRC ..... –55°C to +125°C
- SW-06FQ ..... –40°C to +85°C
- SW-06GP, GS ..... –40°C to +85°C

Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Maximum Junction Temperature ..... 150°C
V+ Supply To V– Supply 36V
V+ Supply to Ground 36V
Logic Input Voltage ..... (–4V or V–) to V+ Supply
Analog Input Voltage Range
- Continuous ..... V– Supply to V+ Supply +20V

Maximum Current Through
Any Pin Including Switch 30mA

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin Plastic DIP (P)	82	39	°C/W
20-Contact LCC (RC)	98	38	°C/W
16-Pin SOL (S)	98	30	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V+ = 15V, V– = –15V and T_A = 25°C, unless otherwise noted.

			SW-06B			SW-06F			SW-06G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	V_S = 0V, I_S = 1mA V_S = ±10V, I_S = 1mA	— —	60 65	80 80	— —	60 65	100 100	— —	100 100	150 150	Ω
R_{ON} Match Between Switches	R_{ON} Match	V_S = 0V, I_S = 100μA (Note 1)	—	5	10	—	5	20	—	—	20	%
Analog Voltage Range	V_A	I_S = 1mA (Note 8) I_S = 1mA	+10 –10	+11 –15	— —	+10 –10	+11 –15	— —	+10 –10	+11 –15	— —	V
Analog Current Range	I_A	V_S = ±10V	10	15	—	7	12	—	5	10	—	mA
ΔR_{ON} vs Applied Voltage	ΔR_{ON}	–10V ≤ V_S ≤ 10V, I_S = 1.0mA	—	5	15	—	10	20	—	10	20	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	V_S = 10V, V_D = –10V (Note 5)	—	0.3	2.0	—	0.3	2.0	—	0.3	10	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	V_S = 10V, V_D = –10V (Note 5)	—	0.3	2.0	—	0.3	2.0	—	0.3	10	nA
Source Current in "ON" Condition	$I_{S(ON)+}$ $I_{D(ON)}$	V_S = V_D = ±10V (Note 5)	—	0.3	2.0	—	0.3	2.0	—	0.3	10	nA
Logical "1" Input Voltage	V_{INH}	Full Temperature Range (Notes 6, 8)	2.0	—	—	2.0	—	—	2.0	—	—	V
Logical "0" Input Voltage	V_{INL}	Full Temperature Range (Notes 6, 8)	—	—	0.8	—	—	0.8	—	—	0.8	V
Logical "1" Input Current	I_{INH}	V_{IN} = 2.0V to 15.0V (Note 4)	—	—	5	—	—	5	—	—	10	μA
Logical "0" Input	I_{INL}	V_{IN} = 0.8V	—	1.5	5.0	—	1.5	5.0	—	1.5	10.0	μA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit (Notes 6, 9)	—	340	500	—	340	600	—	340	700	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit (Notes 6, 9)	—	200	400	—	200	400	—	200	500	ns
Break-Before-Make Time	t_{ON}–t_{OFF}	(Note 3)	50	140	—	50	140	—	50	140	—	ns
Source Capacitance	$C_{S(OFF)}$	V_S = 0V (Note 5)	—	7.0	—	—	7.0	—	—	7.0	—	pF
Drain Capacitance	$C_{D(OFF)}$	V_S = 0V (Note 5)	—	5.5	—	—	5.5	—	—	5.5	—	pF
Channel "ON" Capacitance	$C_{D(ON)+}$ $C_{S(ON)}$	V_S = V_D = 0V (Note 5)	—	15	—	—	15	—	—	15	—	pF
"OFF" Isolation	$I_{SO(OFF)}$	V_S = $5V_{RMS}$, R_L = 680Ω, C_L = 7pF, f = 500kHz (Note 5)	—	58	—	—	58	—	—	58	—	dB
Crosstalk	C_T	V_S = $5V_{RMS}$, R_L = 680Ω, C_L = 7pF, f = 500kHz (Note 5)	—	70	—	—	70	—	—	70	—	dB

ELECTRICAL CHARACTERISTICS at V+ = 15V, V– = –15V and T_A = 25°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	SW-06B MIN	SW-06B TYP	SW-06B MAX	SW-06F MIN	SW-06F TYP	SW-06F MAX	SW-06G MIN	SW-06G TYP	SW-06G MAX	UNITS
Positive Supply Current	I+	All Channels "OFF", DIS = "0" (Note 5)	–	5.0	6.0		5.0	9.0	–	6.0	9.0	mA
Negative Supply Current	I–	All Channels "OFF", DIS = "0" (Note 5)	–	3.0	5.0	–	4.0	7.0	–	4.0	7.0	mA
Ground Current	I_G	All Channels "ON" or "OFF" (Note 5)	–	3.0	4.0	–	3.0	4.0	–	3.0	5.0	mA

ELECTRICAL CHARACTERISTICS at V+ = 15V, V– = –15V, –55°C ≤ T_A ≤ +125°C for SW-06BQ, –40°C ≤ T_A ≤ +85°C for SW-06FQ and –40°C ≤ T_A ≤ +85°C for SW-06GP/GS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-06B MIN	SW-06B TYP	SW-06B MAX	SW-06F MIN	SW-06F TYP	SW-06F MAX	SW-06G MIN	SW-06G TYP	SW-06G MAX	UNITS
Temperature Range	T_A	Operating	–55	—	125	–25	—	85	0	—	70	°C
"ON" Resistance	R_{ON}	V_S = 0V, I_S = 1.0mA V_S = ±10V, I_S = 1.0mA	— —	75 80	110 110	— —	75 80	125 125	— —	75 80	175 175	Ω
R_{ON} Match Between Switches	R_{ON} Match	V_S = 0V, I_S = 100μA (Note 1)	—	6	20	—	6	25	—	10	—	%
Analog Voltage Range	V_A	I_S = 1.0mA (Note 8) I_S = 1.0mA	+10 –10	+11 –15	— —	+10 –10	+11 –15	— —	+10 –10	+11 –15	— —	V
Analog Current Range	I_A	V_S = ±10.0V	7	12	—	5	11	—	—	11	—	mA
ΔR_{ON} With Applied Voltage	ΔR_{ON}	–10V ≤ V_S ≤ +10V, I_S = 1.0mA	—	10	—	—	12	—	—	15	—	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	V_S = 10V, V_D = –10V, T_A = Max. Operating Temp. (Notes 5, 7)	—	—	60	—	—	30	—	—	60	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	V_S = 10V, V_D = –10V, T_A = Max. Operating Temp. (Notes 5, 7)	—	—	60	—	—	30	—	—	60	nA
Leakage Current in "ON" Condition	$I_{S(ON)}$+ $I_{D(ON)}$	V_S = V_D = ±10V, T_A = Max. Operating Temp. (Notes 5, 7)	—	—	100	—	—	30	—	—	60	nA
Logical "1" Input Current	I_{INH}	V_{IN} = 2.0V to 15.0V (Note 4)	—	—	10	—	—	10	—	—	15	μA
Logical "0" Input Current	I_{INL}	V_{IN} = 0.8V	—	4	10	—	4	10	—	5	15	μA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit (Notes 2, 6)	—	440	900	—	500	900	—	—	1000	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit (Notes 2, 6)	—	300	500	—	330	500	—	—	500	ns
Break-Before-Make Time	t_{ON}–t_{OFF}	(Note 3)	—	70	—	—	70	—	—	50	—	ns
Positive Supply Current	I+	All Channels "OFF" DIS = "0" (Note 5)	—	—	9.0	—	—	13.5	—	—	13.5	mA
Negative Supply Current	I–	All Channels "OFF" DIS = "0" (Note 5)	—	—	7.5	—	—	10.5	—	—	10.5	mA
Ground Current	I_G	All Channels "ON" or "OFF" (Note 5)	—	—	6.0	—	—	7.5	—	—	7.5	mA

NOTES:

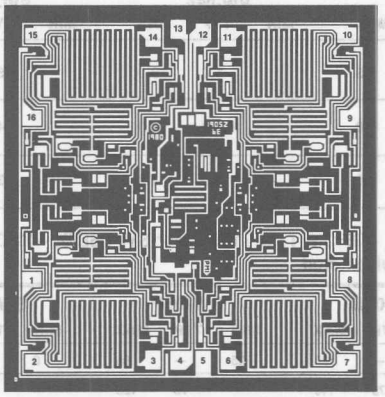
1. V_S = 0V, I_S = 100μA. Specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$

2. Guaranteed by design.
3. Switch is guaranteed by design to provide break-before-make operation.
4. Current tested at V_{IN} = 2.0V. This is worst case condition.
5. Switch being tested ON or OFF as indicated, V_{INH} = 2.0V or V_{INL} = 0.8V, per logic truth table.
6. Also applies to disable pin.
7. Parameter tested only at T_A = +125°C for military grade device.
8. Guaranteed by R_{ON} and leakage tests. For normal operation maximum analog signal voltages should be restricted to less than (V+) –4V.
9. Sample tested.

SW-06

DICE CHARACTERISTICS



DIE SIZE 0.101 × 0.097 inch, 9797 sq. mils
(2.565 × 2.464 mm, 6.320 sq. mm)

1. IN (1)
2. D (1)
3. S (1)
4. GND
5. V− (SUBSTRATE)
6. S (2)
7. D (2)
8. IN (2)
9. IN (3)
10. D (3)
11. S (3)
12. V+
13. DISABLE
14. S (4)
15. D (4)
16. IN (4)

WAFER TEST LIMITS at V+ = 15V, V− = −15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-06N LIMIT	SW-06G LIMIT	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	80	100	Ω MAX
R_{ON} Match Between Switches	R_{ON} Match	$V_A = 0V$, $I_S \le 100\mu A$	15	20	% MAX
ΔR_{ON} vs V_A	ΔR_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	10	20	% MAX
Positive Supply Current	I+	(Note 1)	6.0	9.0	mA MAX
Negative Supply Current	I−	(Note 1)	5.0	7.0	mA MAX
Ground Current	I_G	(Note 1)	4.0	4.0	mA MAX
Analog Voltage Range	V_A	$I_S = 1mA$	±10.0	±10.0	V MIN
Logic "1" Input Voltage	V_{INH}	(Note 3)	2.0	2.0	V MIN
Logic "0" Input Voltage	V_{INL}	(Note 3)	0.8	0.8	V MAX
Logic "0" Input Current	I_{INL}	$0V \le V_{IN} \le 0.8V$	5.0	5.0	μA MAX
Logic "1" Input Current	I_{INH}	$2.0V \le V_{IN} \le 15V$ (Note 2)	5	5	μA MAX
Analog Current Range	I_A	$V_S = \pm 10V$	10	7	mA MIN

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

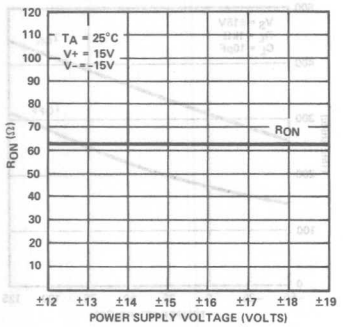
TYPICAL ELECTRICAL CHARACTERISTICS at V+ = 15V, V− = −15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-06N TYPICAL	SW-06G TYPICAL	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	60	60	Ω
Turn-On-Time	t_{ON}		340	340	ns
Turn-Off-Time	t_{OFF}		200	200	ns
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$	0.3	0.3	nA
"OFF" Isolation	$I_{SO(OFF)}$	$f = 500kHz$, $R_L = 680\Omega$	58	58	dB
Crosstalk	C_T	$f = 500kHz$, $R_L = 680\Omega$	70	70	dB

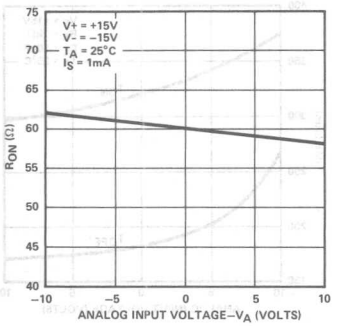
NOTES:
1. Power supply and ground current specified for switch "ON" or "OFF".
2. Current tested at V_{IN} = 2.0V. This is worst case condition.
3. Guaranteed by R_{ON} and leakage tests.

TYPICAL PERFORMANCE CHARACTERISTICS

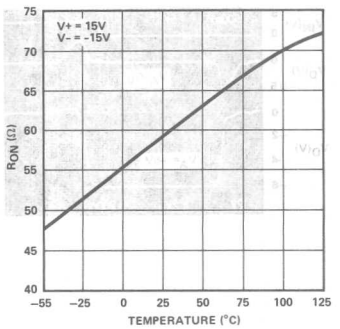
"ON" RESISTANCE vs POWER SUPPLY VOLTAGE



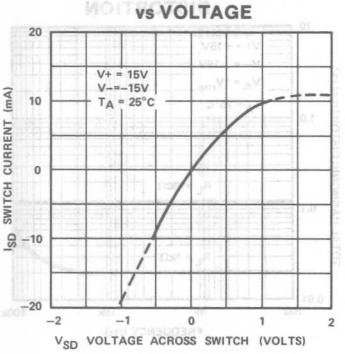
"ON" RESISTANCE vs ANALOG VOLTAGE



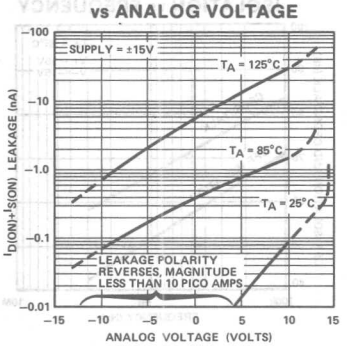
RON vs TEMPERATURE



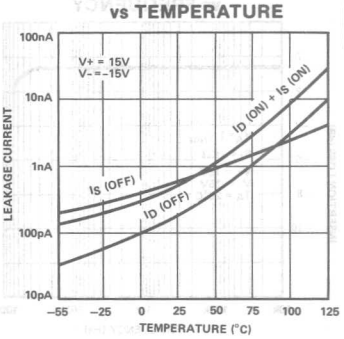
SWITCH CURRENT vs VOLTAGE



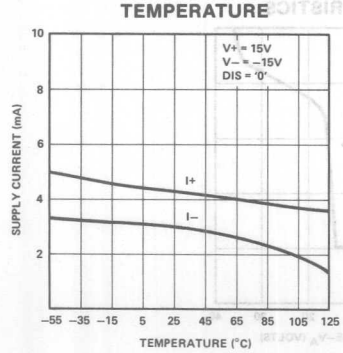
LEAKAGE CURRENT vs ANALOG VOLTAGE



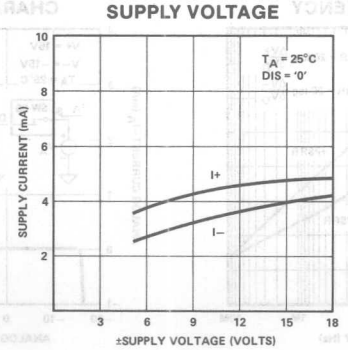
LEAKAGE CURRENT vs TEMPERATURE



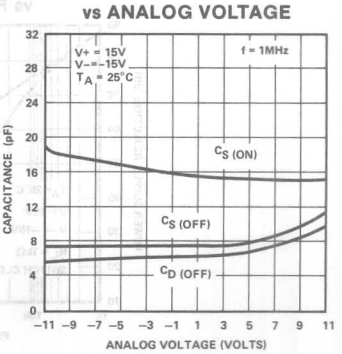
SUPPLY CURRENT vs TEMPERATURE



SUPPLY CURRENT vs SUPPLY VOLTAGE

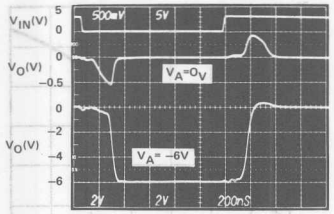


SWITCH CAPACITANCE vs ANALOG VOLTAGE

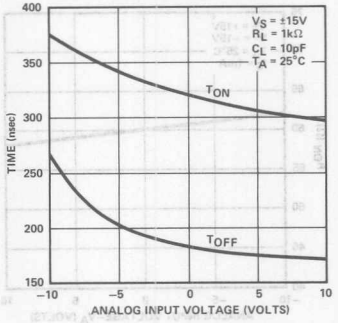


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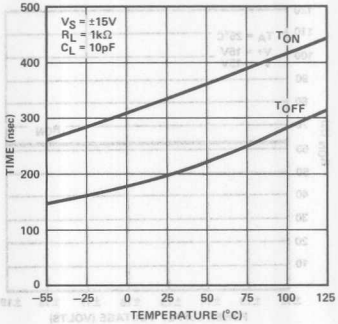
T_{ON}/T_{OFF} SWITCHING RESPONSE



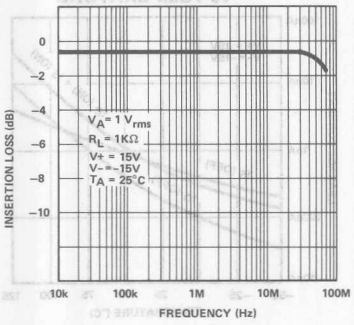
SWITCHING TIME vs ANALOG VOLTAGE



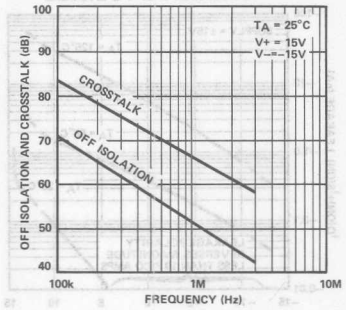
SWITCHING TIME vs TEMPERATURE



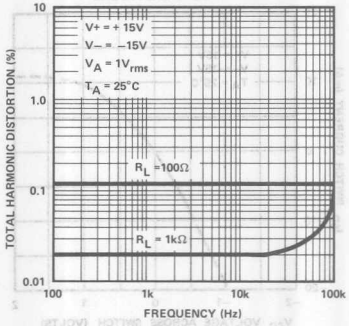
INSERTION LOSS vs FREQUENCY



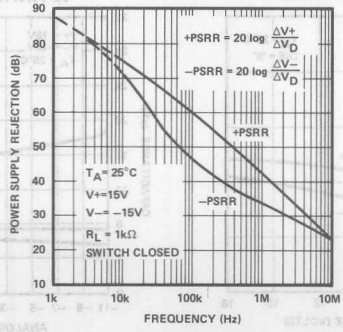
CROSSTALK AND "OFF" ISOLATION vs FREQUENCY



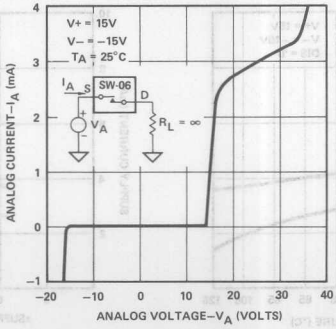
TOTAL HARMONIC DISTORTION



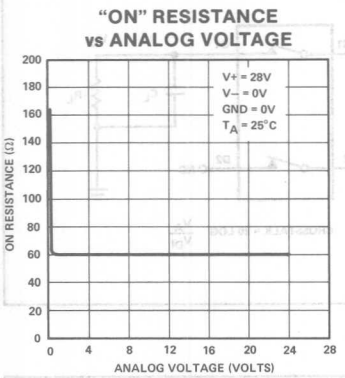
POWER SUPPLY REJECTION vs FREQUENCY

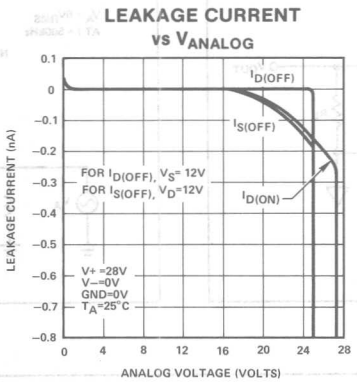


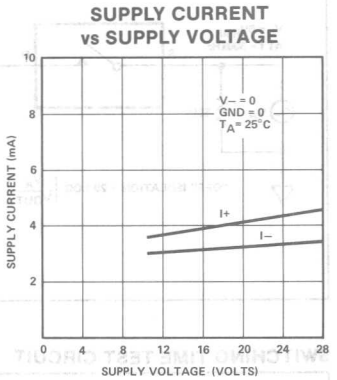
OVERVOLTAGE CHARACTERISTICS

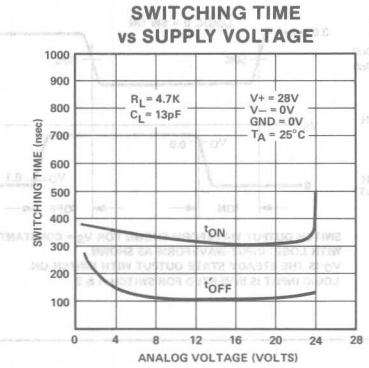


TYPICAL PERFORMANCE CHARACTERISTICS (OPERATING SINGLE SUPPLY)



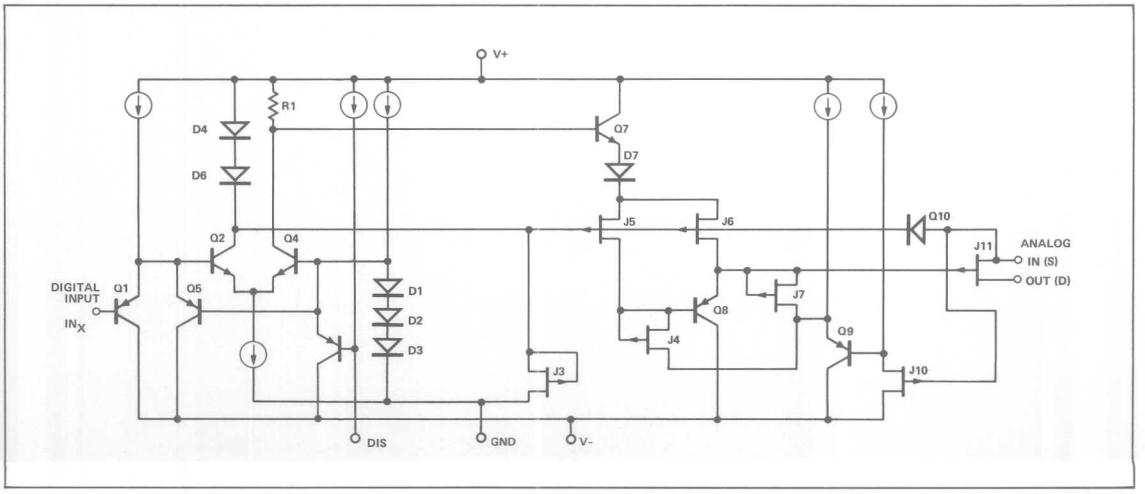






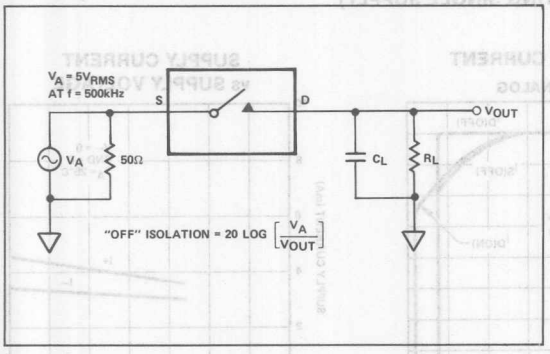
NOTE: These single-supply-operation characteristic curves are valid when the negative power supply V– is tied to the logic ground reference pin "GND". TTL input compatibility is still maintained when "GND" is the same potential as the TTL ground. t'_{OFF} is measured from 50% of logic input waveform to 0.9 V_O. The analog voltage range extends from 0 to V+ –4V, the switch will no longer respond to logic control when V_A is within 4 volts of V+.

SIMPLIFIED SCHEMATIC DIAGRAM (TYPICAL SWITCH)

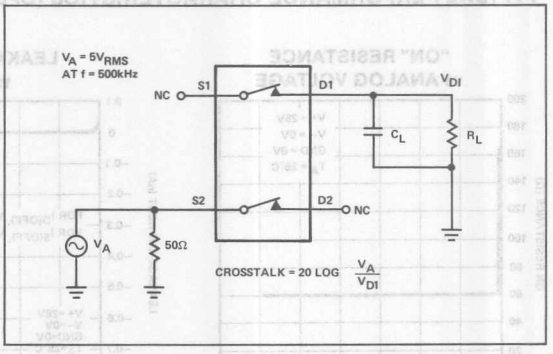


SW-06

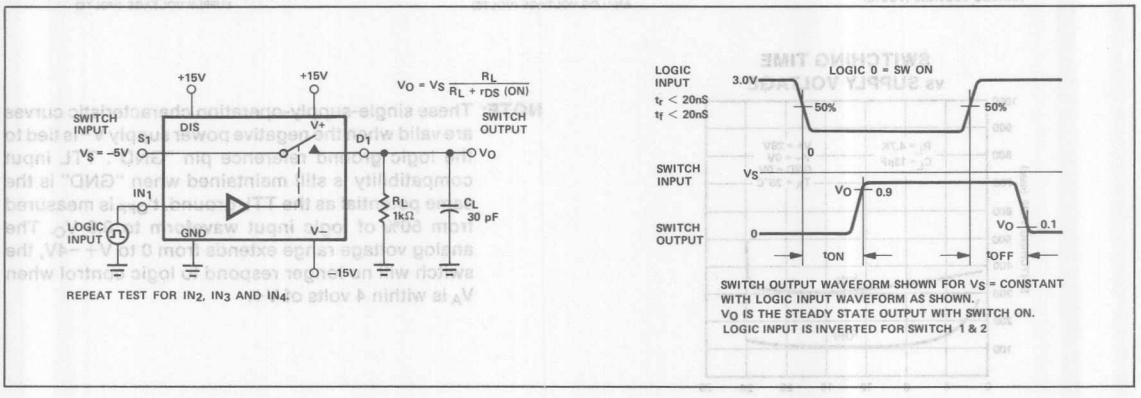
OFF ISOLATION TEST CIRCUIT

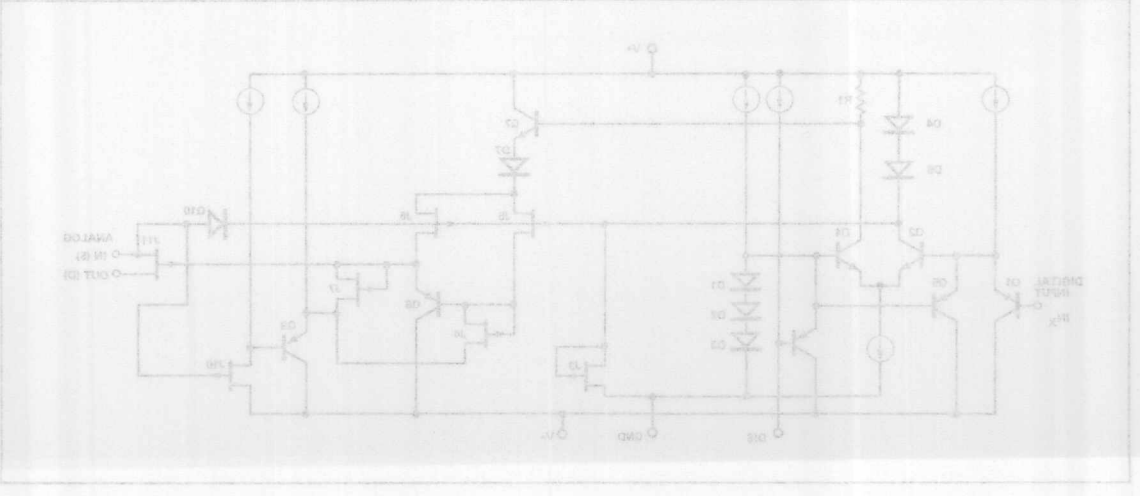


CROSSTALK TEST CIRCUIT



SWITCHING TIME TEST CIRCUIT





ANALOG CURRENT

The analog switches in the ON state are JFETs biased in their triode region and act as switches for analog current up to the I_A specification (see plot of I_{DS} vs V_{DS}). Some applications require pulsed currents exceeding the I_A spec. For example, an integrator reset switch discharging a shunt capacitor will produce a peak current of $I_{A(PEAK)} = V_{CAP}/R_{DS(ON)}$. In this application, it is best to connect the source to the most positive end of the capacitor, thereby achieving the lowest switch resistance and fastest reset times. The switch can easily handle any amount of capacitor discharge current subject only to the maximum heat dissipation of the package and the maximum operating junction temperature from which repetition rates can be established.

SWITCHING

Switching time t_{ON} and t_{OFF} characteristics are plotted versus V_{ANALOG} and temperature. In all cases, t_{OFF} is designed faster than t_{ON} to insure a break-before-make interval for SPDT and DPDT applications. The disable input (DIS) has the same switching times (t_{ON} and t_{OFF}) as the logic inputs (IN_X).

Switching transients occurring at the source and drain contacts results from AC coupling of the switching FETs gate-to-source and gate-to-drain coupling capacitance. The switch turn ON will cause a negative going spike to occur and the turn OFF will cause a positive spike to occur. These spikes can be reduced by additional capacitance loading, lower values of R_L, or switching an additional switch (with its extra contact floating) to the opposite state connected to the spike sensitive node.

DISABLE NODE

This TTL compatible node is similar to the logic inputs IN_X but has an internal 2μA current source pull-up. If disable is left unconnected, it will assume the logic "1" state, then the state of the switches is controlled only by the logic inputs IN_X.

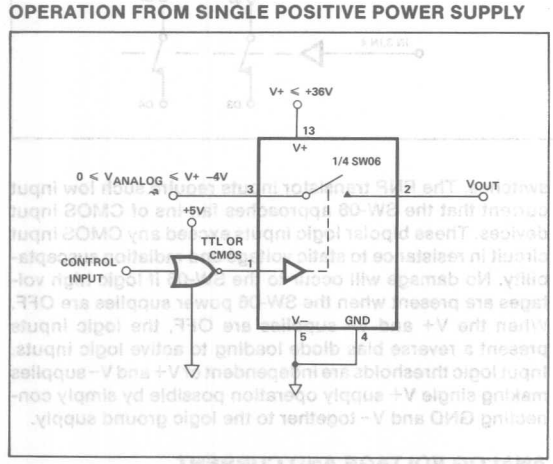
POWER SUPPLIES

This product operates with power supply voltages ranging from ±12 to ±18 volts; however, the specifications only guarantee device parameters with ±15 volt ±5% power supplies. The power supply sensitive parameters have plots to indicate effects of supply voltages other than ±15 volts.

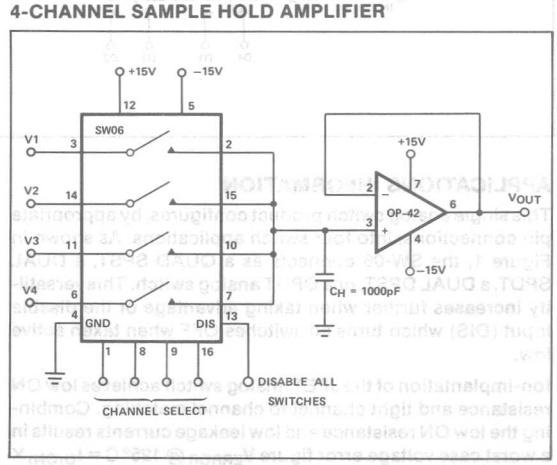
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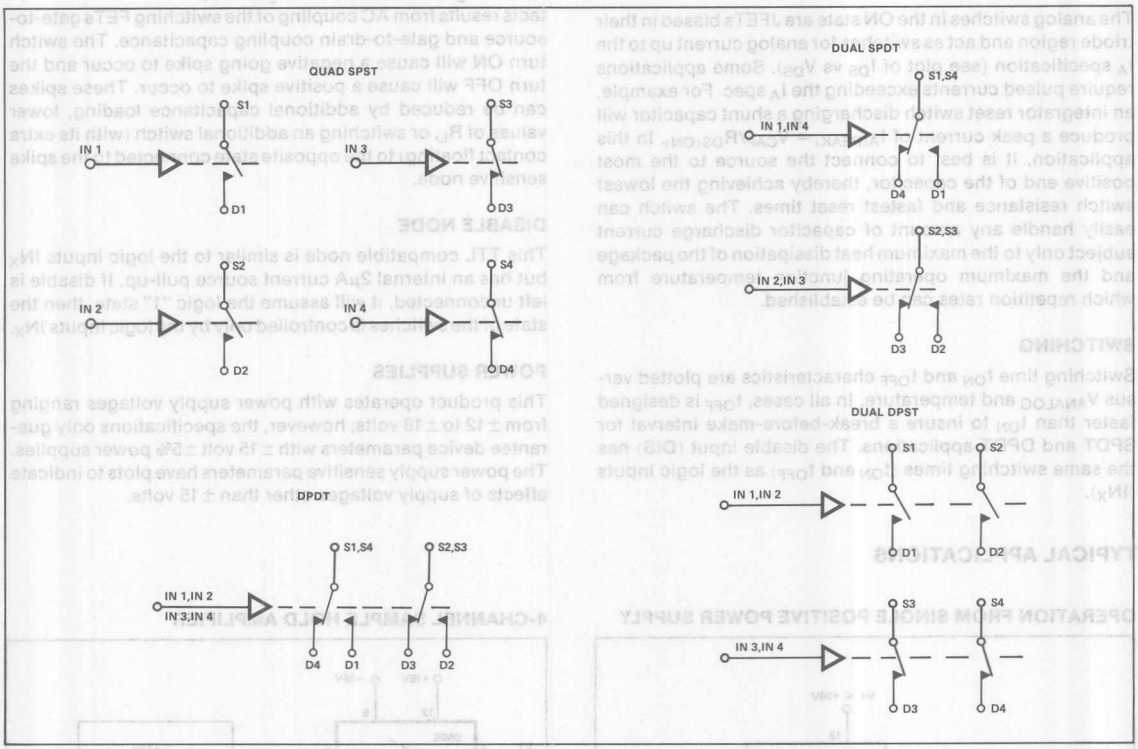
TYPICAL APPLICATIONS

OPERATION FROM SINGLE POSITIVE POWER SUPPLY



4-CHANNEL SAMPLE HOLD AMPLIFIER





APPLICATIONS INFORMATION

This single analog switch product configures, by appropriate pin connections, into four switch applications. As shown in Figure 1, the SW-06 connects as a QUAD SPST, a DUAL SPDT, a DUAL DPST, or a DPDT analog switch. This versatility increases further when taking advantage of the disable input (DIS) which turns all switches OFF when taken active low.

Ion-implantation of the JFET analog switch achieves low ON resistance and tight channel to channel matching. Combining the low ON resistance and low leakage currents results in a worst case voltage error figure V_{ERROR} @ 125° C = $I_{D(ON)} \times R_{SD(ON)} = 100nA \times 100\Omega = 11$ microvolts. This amount of error is negligible considering dissimilar-metal thermally-induced offsets will be in the 5 to 15 microvolt range.

LOGIC INPUTS

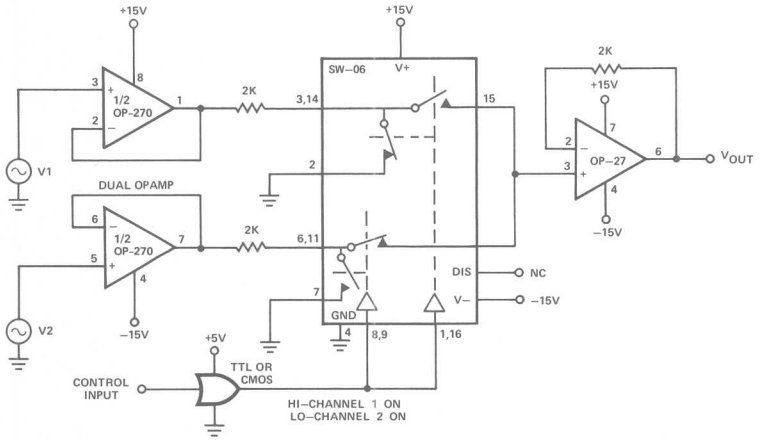
The logic inputs (IN_X) and disable input (DIS) are referenced to a TTL logic threshold value of two forward diode drops (1.4V at 25° C) above the GND terminal. These inputs use PNP transistors which draw maximum current at a logic "0" level and drops to a leakage current of a reverse biased diode as the logic input voltage raises above 1.4 volts. Any logic input voltage greater than 2.0 volts becomes logic "1", less than 0.8 volts becomes logic "0" resulting in full TTL noise immunity not available from similar CMOS input analog switches. The PNP transistor inputs require such low input current that the SW-06 approaches fan-ins of CMOS input devices. These bipolar logic inputs exceed any CMOS input circuit in resistance to static voltage and radiation susceptability. No damage will occur to the SW-06 if logic high voltages are present when the SW-06 power supplies are OFF. When the V+ and V− supplies are OFF, the logic inputs present a reverse bias diode loading to active logic inputs. Input logic thresholds are independent of V+ and V− supplies making single V+ supply operation possible by simply connecting GND and V− together to the logic ground supply.

ANALOG VOLTAGE AND CURRENT

ANALOG VOLTAGE

These switches have constant ON resistance for analog voltages from the negative power supply (V−) to within 4 volts of the positive power supply. This characteristic shown in the plots results in good total harmonic distortion, especially when compared to CMOS analog switches that have a 20 to 30 percent variation in ON resistance versus analog voltage. Positive analog input voltages should be restricted to 4 volts less than V+ assuring the switch remains open circuit in the OFF state. No increase in switch ON resistance occurs when operating at supply voltages less than ±15 volts (see plot). Small signals have a 3dB down frequency of 70MHz (see insertion loss versus frequency plot).

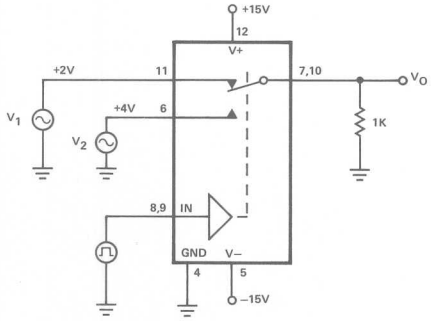
HIGH OFF ISOLATION SELECTOR SWITCH (Shunt-Series Switch)

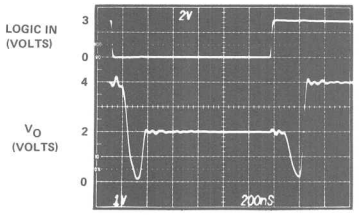


THIS SWITCH ARRANGEMENT IMPROVES OFF ISOLATION BY 30dB

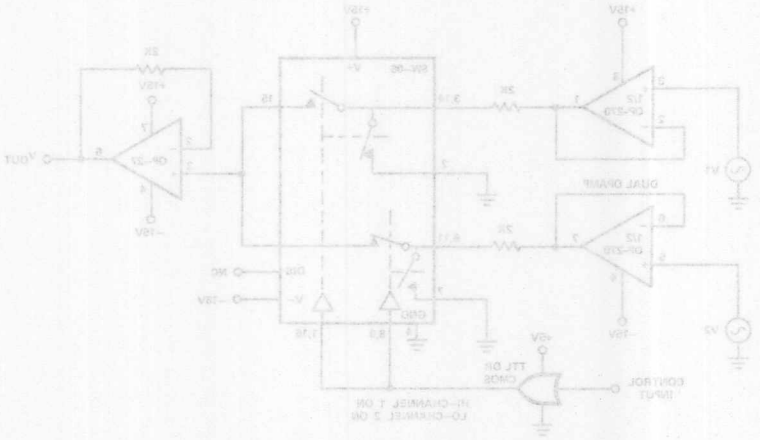
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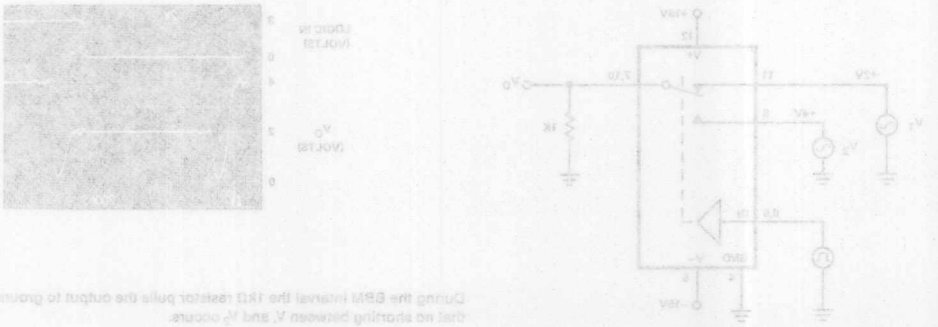
SINGLE POLE DOUBLE THROW SELECTOR SWITCH WITH BREAK-BEFORE-MAKE INTERVAL





During the BBM interval the 1kΩ resistor pulls the output to ground assuring that no shorting between V, and V_2 occurs.





Quad SPST JFET Analog Switches

SW-201/SW-202

FEATURES

SW-201

- **Normally "ON" for Logic 0 Input**
- **Improved Performance and Pin Compatible With DG-201, LF11201/13201, HI201, and IH201**

SW-202

- **Normally "OFF" For Logic 0 Input**
- **Improved Performance and Pin Compatible With LF11202/12202/13202 and IH202**

Both SW-201 and SW-202

- **Highly Resistant to Static Discharge Destruction**
- **Guaranteed Break-Before-Make Switching ($t_{OFF} < t_{ON}$)**
- **Low "ON" Resistance ..... 80Ω Max**
- **Guaranteed R_{ON} Matching ..... 15% Max**
- **Low R_{ON} Variation from Analog Input Voltage 5%**
- **High Analog Current Operation ..... 10mA Min**
- **Low Leakage Currents at High Temperatures:**
  T_A = 125°C ..... 60nA Max
  T_A = 85°C ..... 30nA Max
- **Guaranteed Switching Speeds:**
  t_{ON} = 500ns Max t_{OFF} = 400ns Max
- **Digital Inputs are TTL and CMOS Compatible**
- **Dual or Single Supply Operation**
- **Available in Die Form**

ORDERING INFORMATION †

DIP PACKAGE	SWITCH CONFIGURATION NC	SWITCH CONFIGURATION NO	OPERATING TEMPERATURE RANGE
16-PIN EPOXY	SW201GP	SW202GP	XIND
16-PIN SOL	SW201GS	SW202GS	XIND

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

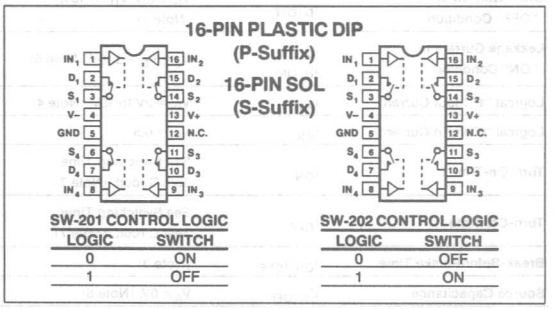
The SW-201 and SW-202 each consist of four independent, single-pole, single-throw (SPST) analog switches, which may be independently digitally controlled. Each SW-201 switch is normally closed (NC), whereas each SW-202 is normally open (NO) when the corresponding digital control input is a zero. The SW-201 and SW-202 are otherwise identical.

The judicious combination of bipolar and FET devices in a single monolithic IC results in a product with performance characteristics and ruggedness that are superior to those of a similar circuit fabricated using CMOS technology.

Increased reliability is complemented by excellent electrical specifications. Potential error sources are reduced by minimizing "ON" resistance and controlling leakage currents at high temperatures. The switching FET exhibits minimal R_{ON} variation over a 20V analog signal range and with power supply voltage changes. Operation from a single positive power supply voltage is possible. With V+ = 36V, V− = 0V, the analog signal range will extend from ground to +32V.

The PNP logic inputs are TTL and CMOS compatible. Logic input currents are at micro-ampere levels which improves circuit fan in.

PIN CONNECTIONS



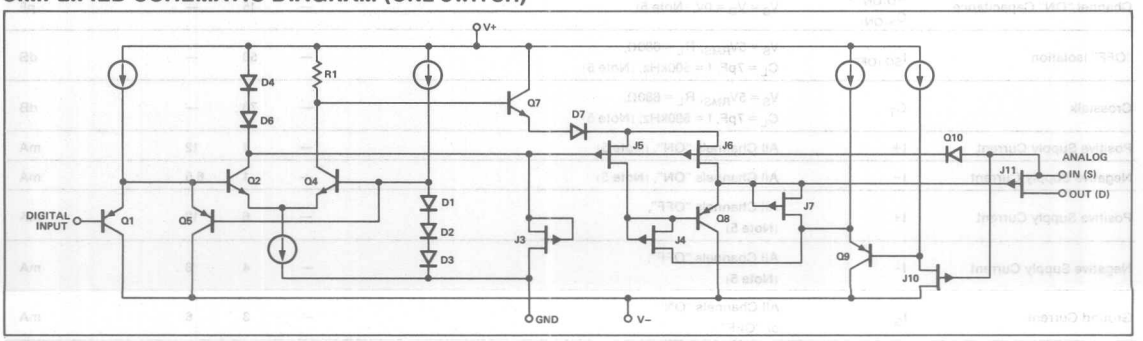
SW-201 CONTROL LOGIC

LOGIC	SWITCH
0	ON
1	OFF

SW-202 CONTROL LOGIC

LOGIC	SWITCH
0	OFF
1	ON

SIMPLIFIED SCHEMATIC DIAGRAM (ONE SWITCH)



Manufactured under the following patent: 4,228,367

ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature Range
SW-201GP, GS, SW202GP, GS ..... –40°C to +85°C
Junction Temperature (T_j) ..... –65°C to +150°C
Storage Temperature Range ..... –65°C to +150°C
P-Suffix ..... –65°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Maximum Junction Temperature ..... +150°C
V+ Supply to V– Supply 36V
V+ Supply to Ground 36V
Logic Input Voltage ..... (–4V or V–) to V+ Supply
Analog Input Voltage Range
Continuous ..... V– Supply to V+ Supply + 20V
1% Duty Cycle and Driving All 4 Inputs with
500µsec Pulse ..... V– Supply –15V to V+ Supply + 20V
Maximum Current Through Any Pin 30mA

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
16-Pin Plastic DIP (P)	82	39	°C/W
16-Pin SOL (S)	98	30	°C/W

NOTES:
1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for P-DIP package; Θ_{jA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V± = ±15V and T_A = 25° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-201G / SW-202G MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	V_A = 0V, I_S = 1mA V_A = ±10V, I_S = 1mA	— —	100 100	150 150	Ω
R_{ON} Match Between Switches	R_{ON} Match	V_A = 0V, I_D = 100µA; (Note 1)	—	—	20	%
Analog Voltage Range	V_A	I_S = 1.0mA I_S = 1.0mA (Note 6)	+10 –10	+11 –15	— —	V
Analog Current Range	I_A	V_S = ±10V	5	10	—	mA
ΔR_{ON} vs Applied Voltage	ΔR_{ON}	$V_S \leq$ 10V, I_S = 1mA	—	10	20	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	V_S = 10V, V_D = –10V, (Note 5)	—	—	10	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	V_S = 10V, V_D = –10V, (Note 5)	—	—	10	nA
Leakage Current in "ON" Condition	$I_{S(ON)}$ + $I_{D(ON)}$	$V_S = V_D$ = ±10V, (Note 5)	—	—	10	nA
Logical "1" Input Current	I_{INH}	V_{IN} = 2V to 15V, (Note 4)	—	—	10	µA
Logical "0" Input Current	I_{INL}	V_{IN} = 0.8	—	1.5	10.0	µA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit, (Note 7)	—	340	700	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit, (Note 7)	—	200	500	ns
Break-Before-Make Time	t_{ON}-t_{OFF}	(Note 3)	50	140	—	ns
Source Capacitance	$C_{S(OFF)}$	V_A = 0V, (Note 5)	—	7	—	pF
Drain Capacitance	$C_{D(OFF)}$	V_A = 0V, (Note 5)	—	5.5	—	pF
Channel "ON" Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$	$V_S = V_D$ = 0V, (Note 5)	—	15	—	pF
"OFF" Isolation	$I_{SO(OFF)}$	V_S = 5V_{RMS}, R_L = 680Ω, C_L = 7pF, f = 500kHz, (Note 5)	—	58	—	dB
Crosstalk	C_T	V_S = 5V_{RMS}, R_L = 680Ω, C_L = 7pF, f = 500kHz, (Note 5)	—	70	—	dB
Positive Supply Current	I+	All Channels "ON", (Note 5)	—	4	12	mA
Negative Supply Current	I–	All Channels "ON", (Note 5)	—	1	6.5	mA
Positive Supply Current	I+	All Channels "OFF", (Note 5)	—	6	12	mA
Negative Supply Current	I–	All Channels "OFF", (Note 5)	—	4	8	mA
Ground Current	I_G	All Channels "ON" or "OFF"	—	3	6	mA

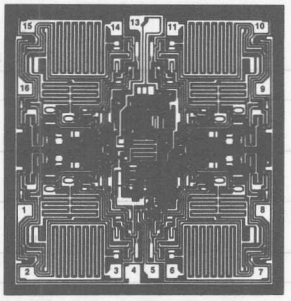
ELECTRICAL CHARACTERISTICS at $V\pm = \pm 15V$; $-40°C \le T_A \le +85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-201G SW-202G MIN	TYP	MAX	UNITS
Temperature Range	T_A	Operating	0	—	70	°C
"ON" Resistance	R_{ON}	$V_A = 0V$, $I_D = 1mA$ $V_A = \pm 10V$, $I_D = 1mA$	— —	— —	175 175	Ω
R_{ON} Match Between Switches	R_{ON} Match	$V_A = 0V$, $I_D = 100\mu A$; (Note 1)	—	10	—	%
Analog Voltage Range	V_A	$I_S = 1.0mA$ (Note 6) $I_S = 1.0mA$	+10 −10	+11 −15	— —	V
Analog Current Range	I_A	$V_S = \pm 10.0V$	—	11	—	mA
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$V_S \le +10V$ $I_S = 1mA$	—	15	—	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$, (Note 5) T_A = Max. Operating Temp.	—	—	60	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$, (Note 5) T_A = Max. Operating Temp.	—	—	60	nA
Leakage Current in "ON" Condition	$I_{S(ON)} + I_{D(ON)}$	$V_S = V_D = \pm 10V$, (Note 5) T_A = Max. Operating Temp.	—	—	60	nA
Logical "1" Input Voltage	V_{INH}	(Note 6)	2	—	—	V
Logic "0" Input Voltage	V_{INL}	(Note 6)	—	—	0.8	V
Logical "1" Input Current	I_{INH}	$V_{IN} = 2V$ to 15V, (Note 4)	—	—	15	μA
Logical "0" Input Current	I_{INL}	$V_{IN} = 0.8$	—	5	15	μA
Turn-On-Time	t_{ON}	See Switching Test Circuit, (Note 2)	—	—	1000	ns
Turn-Off-Time	t_{OFF}	See Switching Test Circuit, (Note 2)	—	—	500	ns
Break-Before-Make Time	$t_{ON}-t_{OFF}$	(Note 3)	—	50	—	ns
Positive Supply Current	I+	All Channels "ON", (Note 5)	—	—	15.8	mA
Negative Supply Current	I−	All Channels "ON", (Note 5)	—	—	14.5	mA
Positive Supply Current	I+	All Channels "OFF", (Note 5)	—	—	18	mA
Negative Supply Current	I−	All Channels "OFF", (Note 5)	—	—	14.5	mA
Ground Current	I_G	All Channels "ON" or "OFF"	—	—	10.0	mA

NOTES:

1. $V_A = 0V$, $I_D = 100\mu A$. Specified as a percentage of $R_{AVERAGE}$ where:
$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$
2. Guaranteed by design.
3. Switch is guaranteed by design to provide break-before-make operation.
4. Current tested at $V_{IN} = 2V$. This is worst case condition.
5. Switch being tested ON or OFF as indicated, $V_{INH} = 2V$ or $V_{INL} = 0.8V$, per logic truth table.
6. Guaranteed by R_{ON} and leakage tests. For normal operation analog signal voltages should be restricted to less than (V+) −4V.
7. Sample tested.

DICE CHARACTERISTICS



DIE SIZE 0.101 × 0.097 inch, 9797 sq. mils
(2.565 × 2.464 mm, 6.320 sq. mm)

1. IN1
2. D1
3. S1
4. V– (SUBSTRATE)
5. GND
6. S2
7. D2
8. IN2
9. IN3
10. D3
11. S3
13. V+
14. S4
15. D4
16. IN4

WAFER TEST LIMITS at V+ = 15V, V– = –15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-201N SW-202N LIMIT	SW-201G SW-202G LIMIT	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	80	100	Ω MAX
R_{ON} Mismatch	R_{ON} Match	$V_A = 0V$, $I_S \le 100\mu A$	15	20	% MAX
ΔR_{ON} vs V_A	ΔR_{ON}	$V_S \le 10V$, $I_S = 1mA$	15	20	% MAX
Positive Supply	I+	(Note 1)	9	10.5	mA MAX
Negative Supply Current	I–	(Note 1)	6	7	mA MAX
Ground Current	I_G		4	4	mA MAX
Analog Voltage Range	V_A	$I_S = 1mA$ (Note 3)	±10	±10	V MIN
Logic "1" Input Voltage	V_{INH}	(Note 3)	2	2	V MIN
Logic "0" Input Voltage	V_{INL}	(Note 3)	0.8	0.8	V MAX
Logic "0" Input Current	I_{INL}	$0V \le V_{IN} \le 0.8V$	5	5	μA MAX
Logic "1" Input Current	I_{INH}	$2V \le V_{IN} \le 15V$, (Note 2)	5	5	μA MAX
Analog Current Range	I_A	$V_S = \pm 10V$	10	7	mA MIN

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

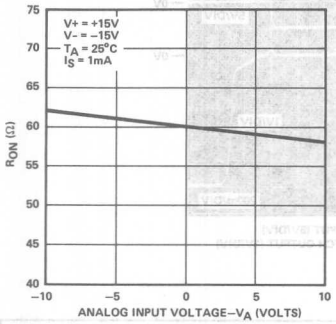
TYPICAL ELECTRICAL CHARACTERISTICS V+ = 15V, V– = –15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-201N SW-202N TYPICAL	SW-201G SW-202G TYPICAL	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	60	60	Ω
Turn-On-Time	t_{ON}		340	340	ns
Turn-Off-Time	t_{OFF}		200	200	ns
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$	0.3	0.3	nA
"OFF" Isolation	$I_{SO(OFF)}$	$f = 500kHz$, $R_L = 680\Omega$	58	58	dB
Crosstalk	C_T	$f = 500kHz$, $R_L = 680\Omega$	70	70	dB

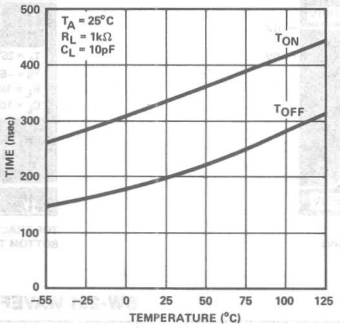
NOTES:
1. Power supply and ground current specified for switch "ON" or "OFF".
2. Current tested at V_{IN} = 2V. This is worst case condition.
3. Guaranteed by R_{ON} and leakage tests.

TYPICAL PERFORMANCE CHARACTERISTICS

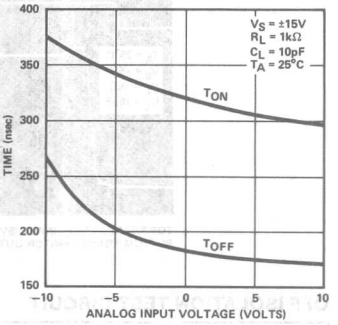
"ON" RESISTANCE vs ANALOG VOLTAGE (V_A)



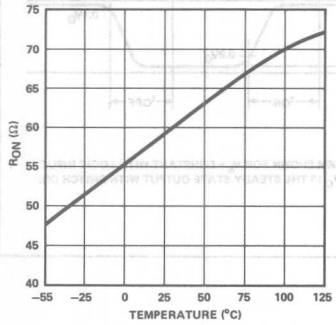
SWITCHING TIME vs TEMPERATURE



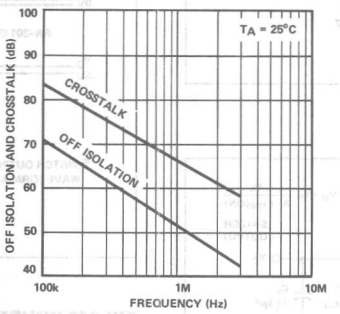
SWITCHING TIME vs ANALOG VOLTAGE



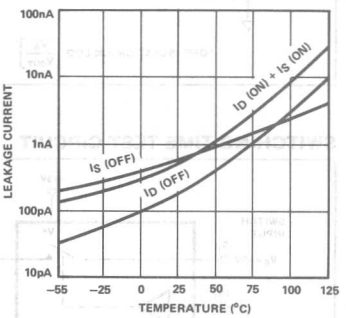
R_{ON} vs TEMPERATURE



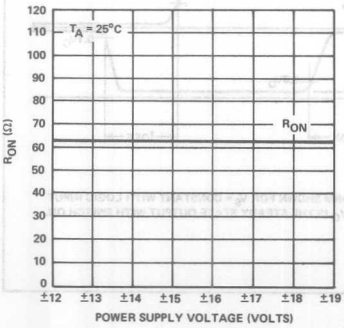
CROSSTALK AND "OFF" ISOLATION vs FREQUENCY



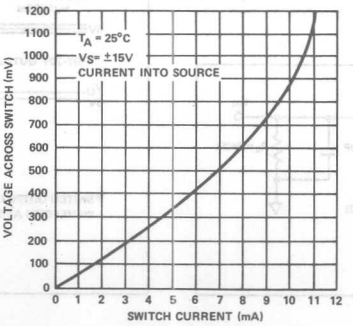
LEAKAGE CURRENT vs TEMPERATURE



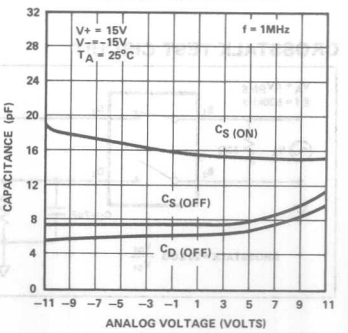
"ON" RESISTANCE vs POWER SUPPLY VOLTAGE



SWITCH CURRENT vs VOLTAGE



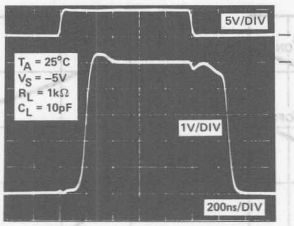
SWITCH CAPACITANCE vs ANALOG VOLTAGE



5

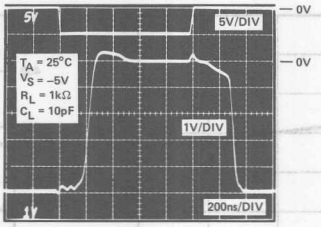
TYPICAL PERFORMANCE CHARACTERISTICS

SW-201
t_{ON}/t_{OFF} SWITCHING RESPONSE



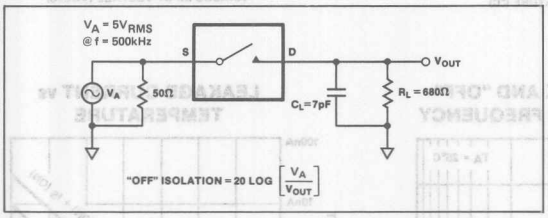
TOP TRACE: LOGIC INPUT (5V/DIV)
BOTTOM TRACE: SWITCH OUTPUT (1V/DIV)

SW-202
t_{ON}/t_{OFF} SWITCHING RESPONSE

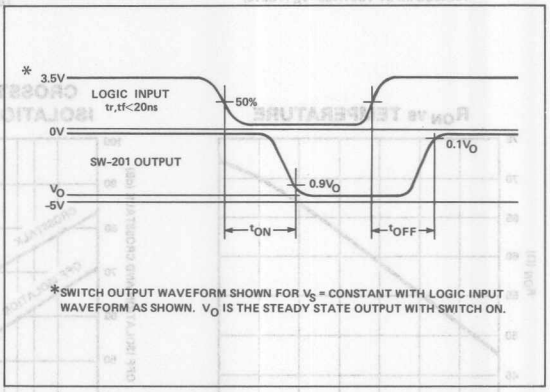


TOP TRACE: LOGIC INPUT (5V/DIV)
BOTTOM TRACE: SWITCH OUTPUT (1V/DIV)

OFF ISOLATION TEST CIRCUIT

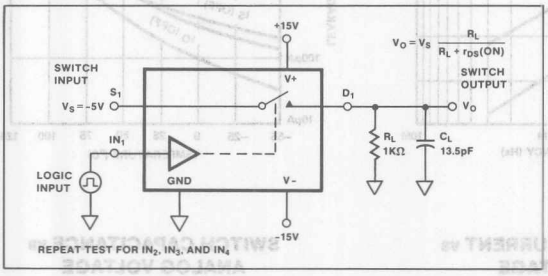


SW-201 WAVEFORMS

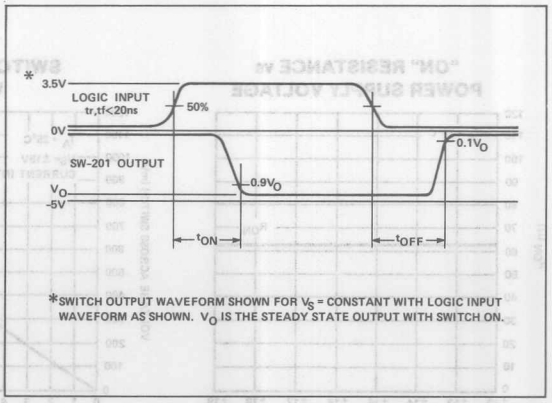


*SWITCH OUTPUT WAVEFORM SHOWN FOR V_S = CONSTANT WITH LOGIC INPUT WAVEFORM AS SHOWN. V_O IS THE STEADY STATE OUTPUT WITH SWITCH ON.

SWITCHING TIME TEST CIRCUIT

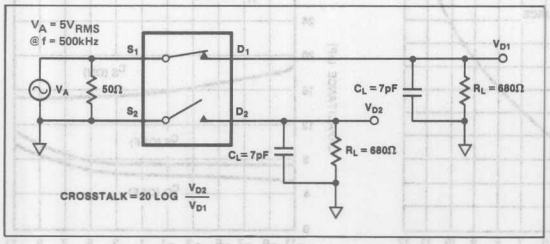


SW-202 WAVEFORMS



*SWITCH OUTPUT WAVEFORM SHOWN FOR V_S = CONSTANT WITH LOGIC INPUT WAVEFORM AS SHOWN. V_O IS THE STEADY STATE OUTPUT WITH SWITCH ON.

CROSSTALK TEST CIRCUIT

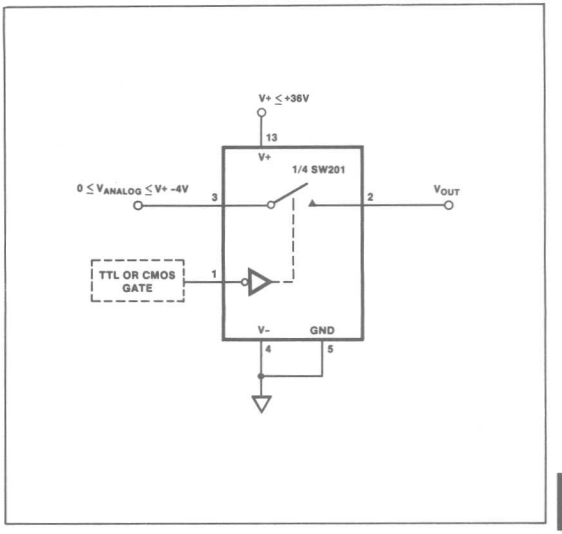


APPLICATIONS INFORMATION

This analog switch employs ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with Bipolar-JFET processing rather than CMOS, special handling is not necessary to prevent damage to these switches. Because the digital inputs only require a 2V logic "1" input level, power-consuming pullup resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS switches. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode as the input voltage is raised above ≈ 1.4V.

The "ON" resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of −15V to +11V with $V_{SUPPLY} = \pm 15V$. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_P, and prevents that channel from being falsely turned ON. Individual switches are "ON" without power applied.

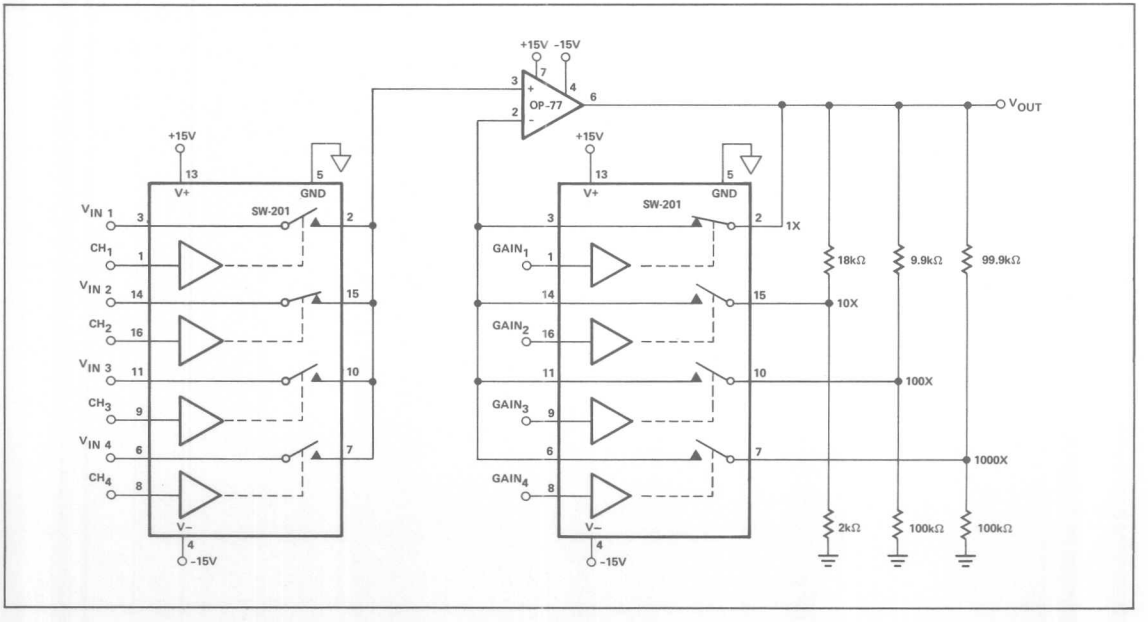
OPERATION FROM SINGLE POSITIVE POWER SUPPLY

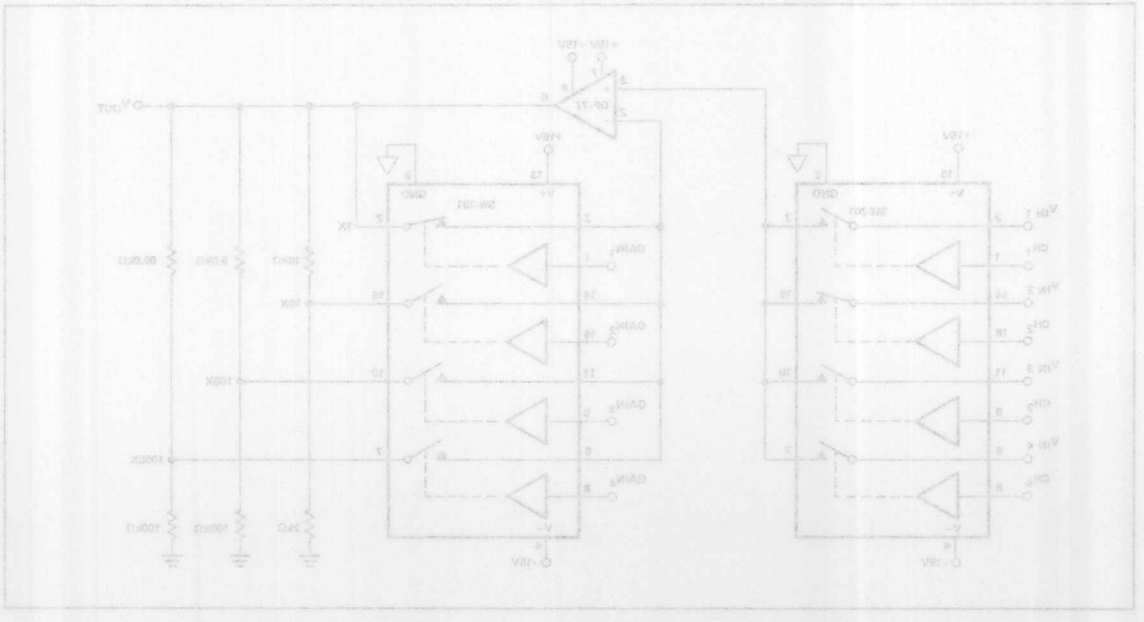


5

TYPICAL APPLICATIONS

PROGRAMMABLE GAIN NONINVERTING AMPLIFIER WITH SELECTABLE INPUTS



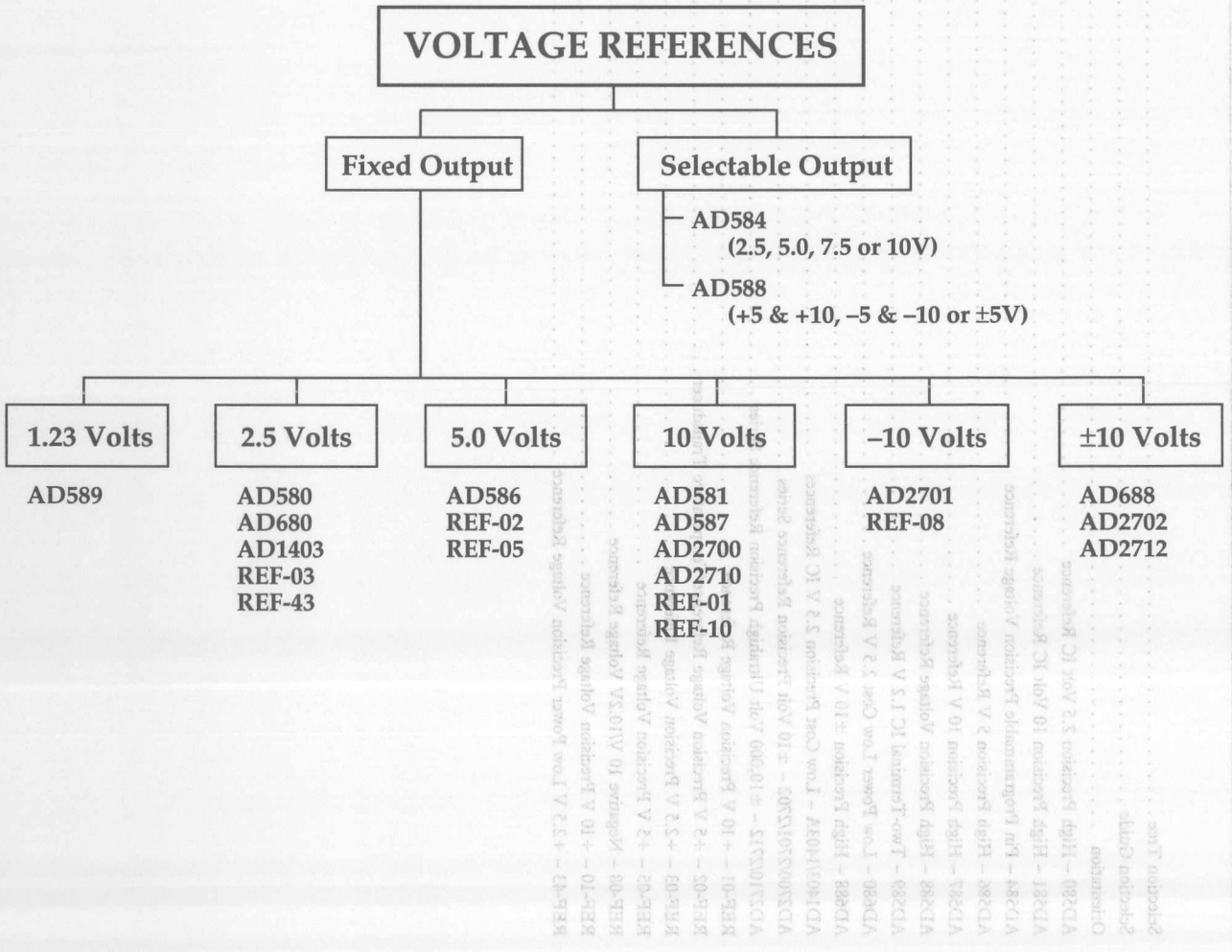


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6

Selection Tree
Voltage References



Selection Guide
Voltage References

Model	Output Voltage V	Initial Accuracy % FS max	Temp Stability pm/°C max	Package Options[1]	Temp Range[2]	Page	Comments
AD589	**+1.235**	**1.2–2.8**	**10–100**	**7**	**C, M**	**C II 6–51**	**Two Terminal, 1.2 V Reference**
***AD680**	**+2.5**	**0.2–0.4**	**20–30**	**2, 6, 16**	**C, I**	**C II 6–55**	**Low Cost, Low Power 2.5 V Reference**
AD580	**+2.5**	**0.4–3**	**10–85**	**7**	**C, M**	**C II 6–5**	**Precision, Three Terminal, 2.5 V Reference**
AD1403/AD1403A	+2.5	0.4–1	25–40	2	I	C II 6–71	Second Source, 2.5 V Reference
REF-43	**+2.5**	**0.6–1**	**10–25**	**2, 3, 6, 7**	**I, M**	**C II 6–127**	**Precision Bandgap Reference**
REF-03	**+2.5**	**0.6**	**50**	**2, 6**	**I**	**C II 6–99**	**Low Cost Bandgap Reference**
AD586	**+5**	**0.05–0.4**	**5–25**	**3, 6**	**C, M**	**C II 6–23**	**Precision, Buried Zener 5 V Reference**
REF-02	**+5**	**0.3–0.5**	**8.5–25**	**2, 3, 4, 6, 7**	**C, I, M**	**C II 6–91**	**Precision Bandgap Reference**
REF-05	**+5**	**0.3–0.6**	**8.5–25**	**7**	**M**	**C II 6–107**	**Guaranteed Long Term Stability**
AD2710	+10	0.01	1–5	2	C	C II 6–79	Ultrahigh Precision 10 V Reference
AD2700	+10	0.025–0.05	3–10	1	C, M	C II 6–75	Very High Precision 10 V Reference
AD587	**+10**	**0.05–0.1**	**5–20**	**3, 6**	**C, M**	**C II 6–31**	**Precision 10 V Buried Zener Reference**
AD581	**+10**	**0.05–0.3**	**5–30**	**7**	**C, M**	**C II 6–9**	**Three Terminal 10 V Bandgap Reference**
REF-01	**+10**	**0.3–0.5**	**8.5–25**	**2, 3, 4, 6, 7**	**C, I, M**	**C II 6–83**	**Precision Bandgap Reference**
REF-10	**+10**	**0.05–0.4**	**5–25**	**2, 3, 6, 7**	**I, M**	**C II 6–121**	**Precision Bandgap Reference**
AD2712	**±10**	**0.01**	**1–5**	**2**	**C**	**C II 6–79**	**Ultrahigh Precision ±10 V Reference**
AD688	**±10**	**0.02–0.05**	**1.5–6**	**3**	**I, M**	**C II 6–63**	**High Precision Monolithic ±10 V Reference**
AD2702	**±10**	**0.025–0.05**	**3–10**	**1**	**C, M**	**C II 6–75**	**Very High Precision ±10 V Reference**
AD2701	**−10**	**0.025–0.05**	**3–10**	**1**	**C, M**	**C II 6–75**	**Very High Precision −10 V Reference**
REF-08	**−10, −10.24**	**0.3–0.4**	**50–100**	**2, 3, 6**	**I, M**	**C II 6–113**	**General Purpose Buried Zener Reference, Pin Selectable Output**
AD588	**Selectable**	**0.01**	**1.5–6**	**2, 3, 4**	**C, I, M**	**C II 6–39**	**Ultrahigh Precision, Monolithic Programmable Reference**
AD584	**Selectable**	**0.05–0.3**	**5–30**	**4, 7**	**C, M**	**C II 6–15**	**Precision, Programmable Bandgap Reference**

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-In-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92.

[2]Temperature Ranges: C = Commercial, 0 to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.

Boldface Type: Product recommended for new design.

*New product since the publication of the most recent Databooks.

A voltage reference is used to provide an accurately known voltage which can be utilized in a circuit or system. For example, measurement systems rely on precision references in order to establish a basis for absolute measurement accuracy. Any reference inaccuracy will undermine the accuracy of the overall system. Thus, ideal references are characterized by accurately set (and traceable to recognized fundamental standards) constant output voltage, independent of temperature, load changes, input voltage variation and time.

TYPES OF REFERENCES

Some of the available IC reference circuits use the bandgap principle: the V_{BE} of any silicon transistor has a negative tempco of about 2 mV/°C, which can be extrapolated to approximately 1.2 volts at absolute zero (the *bandgap* voltage of silicon). Since identical transistors operating at constant current densities will have predictably different temperature coefficients of base emitter voltage, it is possible to arrange circuit elements so as to null out the temperature coefficients associated with the two phenomena and produce a constant voltage (usually 1.2 volts). This temperature-invariant voltage can be amplified and buffered to produce a standard voltage value, such as 2.5 V or 10.0 V. The following devices employ the bandgap architecture: AD580, AD581, AD584, AD589, AD680, REF01, REF02, REF03, REF05, REF10, and REF43.

Another popular form of reference circuit uses a selected low-drift Zener diode, followed by a buffer-amplifier as a precision-gain stage to provide a standard output voltage.

A buried-Zener design provides lower noise and drift than bandgap references. Laser trimming of thin-film resistors results in excellent accuracy and low drift versus temperature. This technique provides initial accuracy to ±1 mV and temperature drifts as low as 1.5 ppm in the AD588 (+10 V, +5 V, ±5 V tracking, −5 V and −10 V outputs) and the AD688 (±10 V tracking outputs). Similar reference designs with single voltage outputs (AD586 and AD587, +5 V and +10 V respectively) have accuracies and temperature coefficients that are nearly as good as the AD588 and AD688.

Several of the references allow the user to optionally connect a capacitor to a noise reduction pin on the IC which further reduces the noise output of the reference. In the AD586, the wideband noise (to 1 MHz) of 200 μV peak-to-peak (p–p) is reduced to 160 μV p–p by adding a 1 μF capacitor to the noise reduction point.

Many data converter ICs require a negative reference voltage, which in the past required an additional op amp to invert the output of a positive reference. The AD588 provides a ±5 V tracking output and the AD688 provides a ±10 V tracking output, while the REF-08 provides a −10 V or −10.24 V output.

Output current capability of the voltage reference must also be considered when selecting a reference. The amount of current that the reference must source, or sink, for the rest of the system affects which references are acceptable or which may need additional buffering.

Kelvin connections provide output sense and force connections, so that the actual voltage at the load is sensed and any IR drops in the leads are compensated. The AD588 and AD688 provide sense and force connections in their designs.

DEFINITION OF SPECIFICATIONS

Line Regulation
The change in output voltage due to a specified change in input voltage. It includes the effects of self-heating. Line Regulation is expressed in either percent per volt, parts-per-million per volt, or microvolts per volt change in input voltage.

Load Regulation
The change in output voltage for a specified change in load current. It includes the effects of self-heating. Load Regulation is expressed in either microvolts per milliampere, parts-per-million per milliampere, or ohms of dc output resistance.

Long-Term Stability
The change in output voltage versus time, specified in ppm/1000 hours.

Output Voltage Tolerance
The deviation from the nominal output voltage at 25°C with specified input voltage as measured by a device traceable to a recognized fundamental voltage standard.

Output Voltage Change with Temperature
The change in output voltage from the value at 25°C ambient; it is independent of variations in the other operating conditions. It may be expressed as either an error band or temperature coefficient. The error band (e.g., ±5 mV, −55°C to +125°C) is defined graphically in terms of a box (voltage vertically, temperature horizontally) whose diagonals extend from 25°C to T_{MAX} and 25°C to T_{MIN}, with a slope equal to the stated temperature coefficient. Thus, the total absolute error for a particular reference over its specified temperature range is equal to the output voltage tolerance at 25°C plus the error band.

Output Temperature Coefficient
The ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.

Output Turn-On Settling Time
The time, from a cold start, for the reference output to settle within a specified error band. This definition relates only to the electrical turn-on time of the chip, and does not include thermal settling time which depends on the package, heat-sinking and load-current change.

Output Voltage Noise
The narrowband (0.1 Hz to 10 Hz) and wideband (to 1 MHz) random noise on the reference output. It may be measured in μV p–p or in nV/$\sqrt{\text{Hz}}$.

Quiescent Supply Current
The current required from the supply to operate the device with no load.

High Precision 2.5V IC Reference

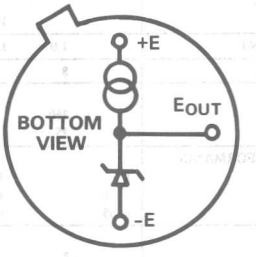
AD580*

FEATURES

- Laser Trimmed to High Accuracy: 2.500V ±0.4%
- 3-Terminal Device: Voltage In/Voltage Out
- Excellent Temperature Stability: 10ppm/°C (AD580M, U)
- Excellent Long Term Stability: 250μV (25μV/Month)
- Low Quiescent Current: 1.5mA max
- Small, Hermetic IC Package: TO-52 Can
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM

TO-52



PRODUCT DESCRIPTION

The AD580 is a three-terminal, low cost, temperature compensated, bandgap voltage reference which provides a fixed 2.5V output for inputs between 4.5V and 30V. A unique combination of advanced circuit design and laser-wafer-trimmed thin-film resistors provide the AD580 with an initial tolerance of ±0.4%, a temperature stability of better than 10ppm/°C and long-term stability of better than 250μV. In addition, the low quiescent current drain of 1.5mA max offers a clear advantage over classical zener techniques.

The AD580 is recommended as a stable reference for all 8-, 10- and 12-bit D-to-A converters that require an external reference. In addition, the wide input range of the AD580 allows operation with 5 volt logic supplies making the AD580 ideal for digital panel meter applications or whenever only a single logic power supply is available.

The AD580J, K, L and M are specified for operation over the 0 to +70°C temperature range; the AD580S, T and U are specified for operation over the extended temperature range of −55°C to +125°C.

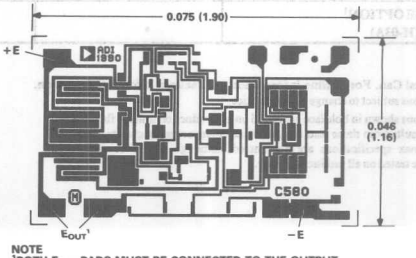
*Protected by Patent Nos. 3,887,863; RE30, 586.

PRODUCT HIGHLIGHTS

1. Laser-trimming of the thin-film resistors minimizes the AD580 output error. For example, the AD580L output tolerance is ±10mV.
2. The three-terminal voltage in/voltage out operation of the AD580 provides regulated output voltage without any external components.
3. The AD580 provides a stable 2.5V output voltage for input voltages between 4.5V and 30V. The capability to provide a stable output voltage using a 5-volt input makes the AD580 an ideal choice for systems that contain a single logic power supply.
4. Thin film resistor technology and tightly controlled bipolar processing provide the AD580 with temperature stabilities to 10ppm/°C and long term stability better than 250μV.
5. The low quiescent current drain of the AD580 makes it ideal for CMOS and other low power applications.
6. The AD580 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD580/883B data sheet for detailed specifications.

AD580 CHIP DIMENSIONS AND PAD LAYOUT

Dimensions shown in inches and (mm).



NOTE
1BOTH E_{OUT} PADS MUST BE CONNECTED TO THE OUTPUT.

The AD580 is also available in chip form. Consult the factory for specifications and applications information.

AD580—SPECIFICATIONS (@ E_{IN} = +15V and +25°C)

Model	AD580J			AD580K			AD580L			AD580M			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE TOLERANCE (Error from Nominal 2.500 Volt Output)			±75			±25			±10			±10	mV
OUTPUT VOLTAGE CHANGE													
T_{min} to T_{max}			15			7			4.3			1.75	mV
			85			40			25			10	ppm/°C
LINE REGULATION													
$7V \le V_{IN} \le 30V$		1.5	6		1.5	4			2			2	mV
$4.5V \le V_{IN} \le 7V$		0.3	3		0.3	2			1			1	mV
LOAD REGULATION													
ΔI = 10mA			10			10			10			10	mV
QUIESCENT CURRENT		1.0	1.5		1.0	1.5		1.0	1.5		1.0	1.5	mA
NOISE (0.1Hz to 10Hz)		8			8			8			8		μV (p-p)
STABILITY													
Long Term		250			250			250			250		μV
Per Month		25			25			25			25		μV
TEMPERATURE PERFORMANCE													
Specified	0		+70	0		+70	0		+70	0		+70	°C
Operating	−55		+125	−55		+125	−55		+125	−55		+125	°C
Storage	−65		+175	−65		+175	−65		+175	−65		+175	°C
PACKAGE OPTION[1]													
TO-52 (H-03A)		*			*			*			*		

Model	AD580S			AD580T			AD580U			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE TOLERANCE (Error from Nominal 2.500 Volt Output)			±25			±10			±10	mV
OUTPUT VOLTAGE CHANGE										
T_{min} to T_{max}			25			11			4.5	mV
			55			25			10	ppm/°C
LINE REGULATION										
$7V \le V_{IN} \le 30V$		1.5	6			2			2	mV
$4.5V \le V_{IN} \le 7V$		0.3	3			1			1	mV
LOAD REGULATION										
ΔI = 10mA			10			10			10	mV
QUIESCENT CURRENT		1.0	1.5		1.0	1.5		1.0	1.5	mA
NOISE (0.1Hz to 10Hz)		8			8			8		μV (p-p)
STABILITY										
Long Term		250			250			250		μV
Per Month		25			25			25		μV
TEMPERATURE PERFORMANCE										
Specified	−55		+125	−55		+125	−55		+125	°C
Operating	−55		+150	−55		+150	−55		+150	°C
Storage	−65		+175	−65		+175	−65		+175	°C
ABSOLUTE MAXIMUM RATINGS										
Input Voltage	40V									
Power Dissipation @ +25°C										
Ambient Temperature	350mW									
Derate above +25°C	2.8mW/°C									
Lead Temperature (Soldering, 10 sec)	300°C									
Thermal Resistance										
Junction-to-Case	100°C/W									
Junction-to-Ambient	360°C/W									
PACKAGE OPTION[1]										
TO-52 (H-03A)		*			*			*		

NOTE
* H = Metal Can. For outline information see Package Information section.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

THEORY OF OPERATION

The AD580 family (AD580, AD581, AD584, AD589) uses the "bandgap" concept to produce a stable, low-temperature-coefficient voltage reference suitable for high accuracy data-acquisition components and systems. The device makes use of the underlying physical nature of a silicon transistor base-emitter voltage in the forward-biased operating region. All such transistors have approximately a $-2mV/^{\circ}C$ temperature coefficient, unsuitable for use directly as a low TC reference; however, extrapolation of the temperature characteristic of any one of these devices to absolute zero (with emitter current proportional to absolute temperature) reveals that it will go to a V_{BE} of 1.205 volts at 0K, as shown in Figure 1. Thus, if a voltage could be developed with an opposing temperature coefficient to sum with V_{BE} to total 1.205 volts, a zero-TC reference would result and operation from a single, low-voltage supply would be possible. The AD580 circuit provides such a compensating voltage, V_1 in Figure 2, by driving two transistors at different current densities and amplifying the resulting V_{BE} difference (ΔV_{BE} – which now has a positive TC); the sum (V_Z) is then buffered and amplified up to 2.5 volts to provide a usable reference-voltage output. Figure 3 is the schematic diagram of the AD580.

The AD580 operates as a three-terminal reference, which means that no additional components are required for biasing or current setting. The connection diagram, Figure 4 is quite simple.

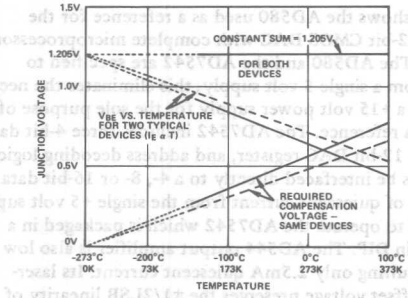


Figure 1. Extrapolated Variation of Base-Emitter Voltage with Temperature ($I_E \propto T$), and Required Compensation, Shown for Two Different Devices

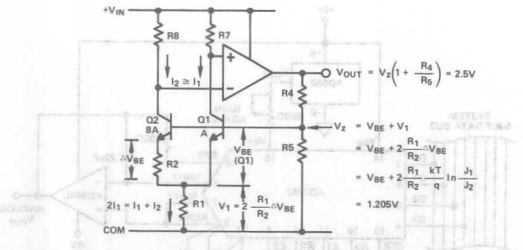


Figure 2. Basic Bandgap-Reference Regulator Circuit

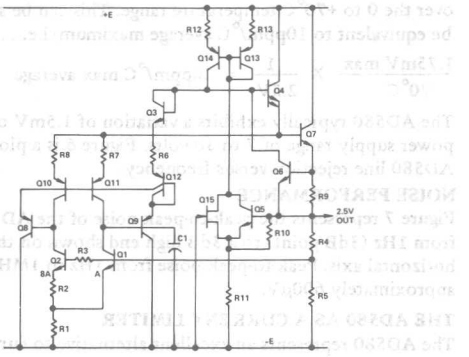


Figure 3. AD580 Schematic Diagram

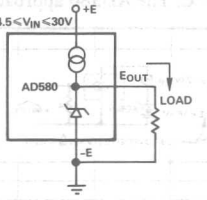


Figure 4. AD580 Connection Diagram

VOLTAGE VARIATION VS. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references are characterized using a maximum deviation per degree Centigrade; i.e., $10ppm/^{\circ}C$. However, because of the inconsistent nonlinearities in zener references (butterfly or "S" type characteristics), most manufacturers use a maximum limit error band approach to characterize their references. This technique measures the output voltage at 3 to 5 different temperatures and guarantees that the output voltage deviation will fall within the guaranteed error band at these discrete temperatures. This approach, of course, makes no mention or guarantee of performance at any other temperature within the operating temperature range of the device.

The consistent Voltage vs. Temperature performance of a typical AD580 is shown in Figure 5. Note that the characteristic is quasi-parabolic, not the possible "S" type characteristics of classical zener references. This parabolic characteristic permits a maximum output deviation specification over the device's full operating temperature range, rather than just at 3 to 5 discrete temperatures.

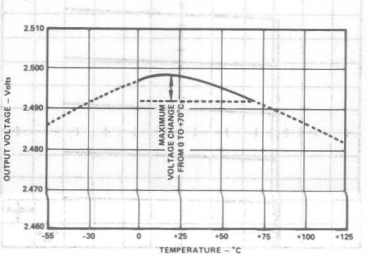


Figure 5. Typical AD580K Output Voltage vs. Temperature

6

The AD580M guarantees a maximum deviation of 1.75mV over the 0 to +70°C temperature range. This can be shown to be equivalent to 10ppm/°C average maximum; i.e. . .

$$\frac{1.75\text{mV max}}{70^\circ\text{C}} \times \frac{1}{2.5\text{V}} = 10\text{ppm}/^\circ\text{C max average}$$

The AD580 typically exhibits a variation of 1.5mV over the power supply range of 7 to 30 volts. Figure 6 is a plot of AD580 line rejection versus frequency.

NOISE PERFORMANCE

Figure 7 represents the peak-to-peak noise of the AD580 from 1Hz (3dB point) to a 3dB high end shown on the horizontal axis. Peak-to-peak noise from 1Hz to 1MHz is approximately 600μV.

THE AD580 AS A CURRENT LIMITER

The AD580 represents an excellent alternative to current limiter diodes which require factory-selection to achieve a desired current. This approach often results in temperature coefficients of 1%/°C. The AD580 approach is not limited to a specially selected factory set current limit; it can be programmed from 1 to 10mA with the insertion of a single external resistor. The approximate temperature coefficient of current limit for the AD580 used in this mode is 0.13%/°C for I_{LIM} = 1mA and 0.01%/°C for I_{LIM} = 13mA (see Figure 9). Figure 8 displays the high output impedance of the AD580 used as a current limiter for I_{LIM} = 1, 2, 3, 4, 5mA.

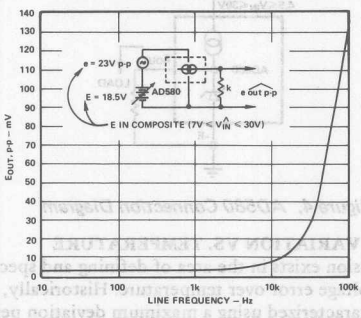


Figure 6. AD580 Line Rejection Plot

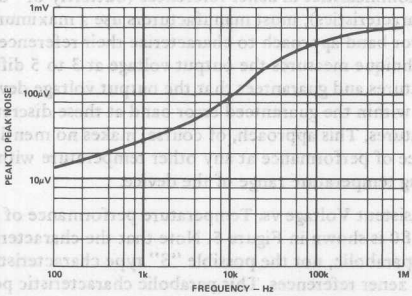


Figure 7. Peak-to-Peak Output Noise vs. Frequency

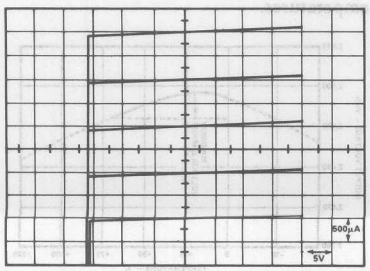


Figure 8. Input Current vs. Input Voltage (Integral Loads)

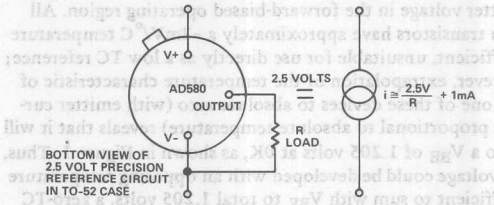


Figure 9. A Two-Component Precision Current Limiter

THE AD580 AS A LOW POWER, LOW VOLTAGE PRECISION REFERENCE FOR DATA CONVERTERS

The AD580 has a number of features that make it ideally suited for use with A/D and D/A data converters used in complex microprocessor-based systems. The calibrated 2.500 volt output minimizes user trim requirements and allows operation from a single low voltage supply. Low power consumption (1mA quiescent current) is commensurate with that of CMOS-type devices, while the low cost and small package complements the decreasing cost and size of the latest converters.

Figure 10 shows the AD580 used as a reference for the AD7542 12-bit CMOS DAC with complete microprocessor interface. The AD580 and the AD7542 are specified to operate from a single 5 volt supply; this eliminates the need to provide a +15 volt power supply for the sole purpose of operating a reference. The AD7542 includes three 4-bit data registers, a 12-bit DAC register, and address decoding logic; it may thus be interfaced directly to a 4-, 8- or 16-bit data bus. Only 8mA of quiescent current from the single +5 volt supply is required to operate the AD7542 which is packaged in a small 16-pin DIP. The AD544 output amplifier is also low power, requiring only 2.5mA quiescent current. Its laser-trimmed offset voltage preserves the ±1/2LSB linearity of the AD7542KN without user trims and it typically settles to ±1/2 LSB in less than 3μs. It will provide the 0 to –2.5 volt output swing from ±5 volt supplies.

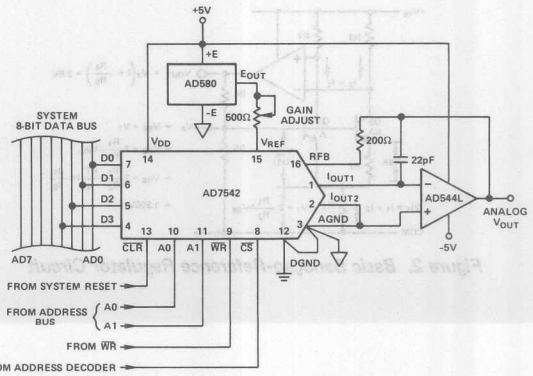


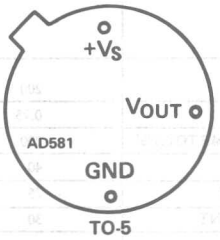
Figure 10. Low Power, Low Voltage Reference for the AD7542 Microprocessor-Compatible 12-Bit DAC

AD581*

FEATURES

Laser-Trimmed to High Accuracy:
10.000 Volts ±5mV (L and U)
Trimmed Temperature Coefficient:
5ppm/°C max, 0 to +70°C (L)
10ppm/°C max, −55°C to +125°C (U)
Excellent Long-Term Stability:
25ppm/1000 hrs. (Noncumulative)
Negative 10 Volt Reference Capability
Low Quiescent Current: 1.0mA max
10mA Current Output Capability
3-Terminal TO-5 Package
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



TO-5

BOTTOM VIEW

PRODUCT DESCRIPTION

The AD581 is a three-terminal, temperature compensated, monolithic band-gap voltage reference which provides a precise 10.00 volt output from an unregulated input level from 12 to 30 volts. Laser Wafer Trimming (LWT) is used to trim both the initial error at +25°C as well as the temperature coefficient, which results in high precision performance previously available only in expensive hybrids or oven-regulated modules. The 5mV initial error tolerance and 5ppm/°C guaranteed temperature coefficient of the AD581L represent the best performance combination available in a monolithic voltage reference.

The band-gap circuit design used in the AD581 offers several advantages over classical Zener breakdown diode techniques. Most important, no external components are required to achieve full accuracy and stability of significance to low power systems. In addition, total supply current to the device, including the output buffer amplifier (which can supply up to 10mA) is typically 750μA. The long-term stability of the band-gap design is equivalent or superior to selected Zener reference diodes.

The AD581 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD581J, K, and L are specified for operation from 0 to +70°C; the AD581S, T, and U are specified for the −55°C to +125°C range. All grades are packaged in a hermetically-sealed three-terminal TO-5 metal can.

PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD581L has a maximum deviation from 10.000 volts of ±7.25mV from 0 to +70°C, while the AD581U guarantees ±15mV maximum total error without external trims from −55°C to +125°C.
2. Since the laser trimming is done on the wafer prior to separation into individual chips, the AD581 will be extremely valuable to hybrid designers for its ease of use, lack of required external trims, and inherent high performance.
3. The AD581 can also be operated in a two-terminal "Zener" mode to provide a precision negative 10 volt reference with just one external resistor to the unregulated supply. The performance in this mode is nearly equal to that of the standard three-terminal configuration.
4. Advanced circuit design using the band-gap concept allows the AD581 to give full performance with an unregulated input voltage down to 13 volts. With an external resistor, the device will operate with a supply as low as 11.4 volts.
5. The AD581 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD581/883B data sheet for detailed specifications.

AD581—SPECIFICATIONS (@ V_{IN} = +15V and 25°C)

Model	AD581J Min	AD581J Typ	AD581J Max	AD581K Min	AD581K Typ	AD581K Max	AD581L Min	AD581L Typ	AD581L Max	Units
OUTPUT VOLTAGE TOLERANCE (Error from nominal 10,000V output)			**±30**			**±10**			**±5**	mV
OUTPUT VOLTAGE CHANGE										
Maximum Deviation from +25°C Value, T_{min} to T_{max}			**±13.5**			**±6.75**			**±2.25**	mV
(Temperature Coefficient)			30			15			5	ppm/°C
LINE REGULATION										
$15V \leq V_{IN} \leq 30V$			**3.0**			**3.0**			**3.0**	mV
			(0.002)			(0.002)			(0.002)	%/V
$13V \leq V_{IN} \leq 15V$			**1.0**			**1.0**			**1.0**	mV
			(0.005)			(0.005)			(0.005)	%/V
LOAD REGULATION										
$0 \leq I_{OUT} \leq 5mA$		200	**500**		200	**500**		200	**500**	µV/mA
QUIESCENT CURRENT		0.75	**1.0**		0.75	**1.0**		0.75	**1.0**	mA
TURN-ON SETTLING TIME TO 0.1%[1]		200			200			200		µs
NOISE (0.1 to 10Hz)		40			40			40		µV/p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 hrs.
SHORT-CIRCUIT CURRENT		30			30			30		mA
OUTPUT CURRENT										
Source @ +25°C	10			10			10			mA
Source T_{min} to T_{max}	5			5			5			mA
Sink T_{min} to T_{max}	5			5			5			µA
Sink −55°C to +85°C	–			–			–			mA
TEMPERATURE RANGE										
Specified	0		+70	0		+70	0		+70	°C
Operating	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[2]										
TO-5 (H-03B)		AD581JH			AD581KH			AD581LH		

Model	AD581S Min	AD581S Typ	AD581S Max	AD581T Min	AD581T Typ	AD581T Max	AD581U Min	AD581U Typ	AD581U Max	Units
OUTPUT VOLTAGE TOLERANCE (Error from nominal 10,000V output)			**±30**			**±10**			**±5**	mV
OUTPUT VOLTAGE CHANGE										
Maximum Deviation from +25°C Value, T_{min} to T_{max}			**±30**			**±15**			**±10**	mV
(Temperature Coefficient)			30			15			10	ppm/°C
LINE REGULATION										
$15V \leq V_{IN} \leq 30V$			**3.0**			**3.0**			**3.0**	mV
			(0.002)			(0.002)			(0.002)	%/V
$13V \leq V_{IN} \leq 15V$			**1.0**			**1.0**			**1.0**	mV
			(0.005)			(0.005)			(0.005)	%/V
LOAD REGULATION										
$0 \leq I_{OUT} \leq 5mA$		200	**500**		200	**500**		200	**500**	µV/mA
QUIESCENT CURRENT		0.75	**1.0**		0.75	**1.0**		0.75	**1.0**	mA
TURN-ON SETTLING TIME TO 0.1%[1]		200			200			200		µs
NOISE (0.1 to 10Hz)		40			40			40		µV/p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 hrs.
SHORT-CIRCUIT CURRENT		30			30			30		mA
OUTPUT CURRENT										
Source @ +25°C	10			10			10			mA
Source T_{min} to T_{max}	5			5			5			mA
Sink T_{min} to T_{max}	200			200			200			µA
Sink −55°C to +85°C	5			5			5			mA
TEMPERATURE RANGE										
Specified	−55		+125	−55		+125	−55		+125	°C
Operating	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[2]										
TO-5 (H-03B)		AD581SH			AD581TH			AD581UH		

NOTES
[1]See Figure 7.
[2]H = Hermetic Metal Can. For outline information see Package Information section.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Input Voltage V_{IN} to Ground 40V
Power Dissipation @ +25°C 600mW
Operating Junction Temperature Range . . −55°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C
Thermal Resistance
Junction-to-Ambient . . . . . 150°C/W

APPLYING THE AD581

The AD581 is easy to use in virtually all precision reference applications. The three terminals are simply primary supply, ground, and output, with the case grounded. No external components are required even for high precision applications; the degree of desired absolute accuracy is achieved simply by selecting the required device grade. The AD581 requires less than 1mA quiescent current from an operating supply range of 12 to 30 volts.

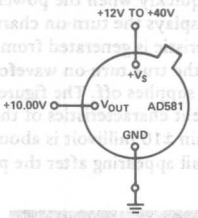
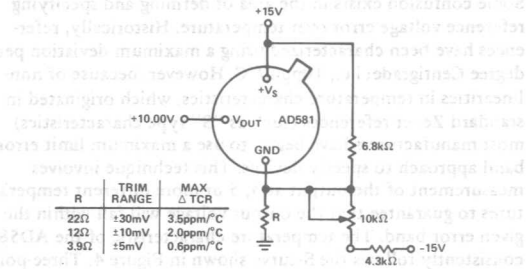


Figure 1. AD581 Pin Configuration (Top View)

An external fine trim may be desired to set the output level to exactly 10.000 volts within less than a millivolt (calibrated to a main system reference). System calibration may also require a reference slightly different from 10.00 volts. In either case, the optional trim circuit shown in Figure 2 can offset the output by up to ±30 millivolts (with the 22Ω resistor), if needed, with minimal effect on other device characteristics.



R	TRIM RANGE	MAX Δ TCR
22Ω	±30mV	3.5ppm/°C
12Ω	±10mV	2.0ppm/°C
3.9Ω	±5mV	0.6ppm/°C

Figure 2. Optional Fine Trim Configuration

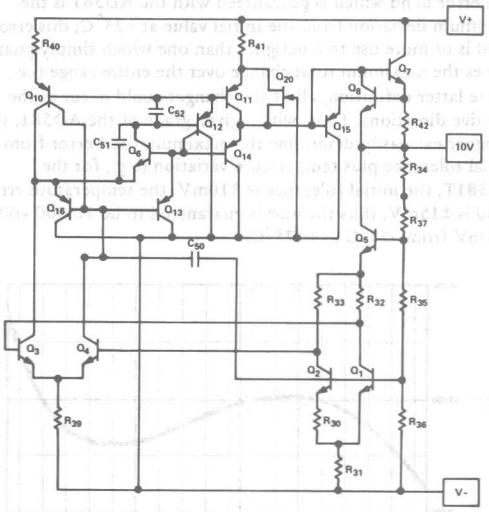


Figure 3. Simplified Schematic

reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of nonlinearities in temperature characteristics, which originated in standard Zener references (such as "S" type characteristics) most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves measurement of the output at 3, 5 or more different temperatures to guarantee that the output voltage will fall within the given error band. The temperature characteristic of the AD581 consistently follows the S-curve shown in Figure 4. Three-point measurement of each device guarantees the error band over the specified temperature range.

The error band which is guaranteed with the AD581 is the maximum deviation from the initial value at +25°C; this error band is of more use to a designer than one which simply guarantees the maximum total change over the entire range (i.e., in the latter definition, all of the changes could occur in the positive direction). Thus, with a given grade of the AD581, the designer can easily determine the maximum total error from initial tolerance plus temperature variation (e.g., for the AD581T, the initial tolerance is ±10mV, the temperature error band is ±15mV, thus the unit is guaranteed to be 10.000 volts ±25mV from -55°C to +125°C).

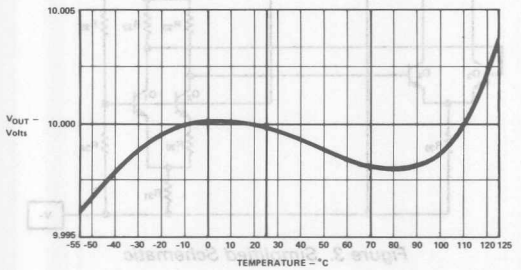


Figure 4. Typical Temperature Characteristic

OUTPUT CURRENT CHARACTERISTICS

The AD581 has the capability to either source or sink current and provide good load regulation in either direction, although it has better characteristics in the source mode (positive current into the load). The circuit is protected for shorts to either positive supply or ground. The output voltage vs. output current is displayed as negative current in the figure; sink current is positive. Note that the short circuit current (i.e., zero volts output) is about 28mA; when shorted to +15 volts, the sink current goes to about 20mA.

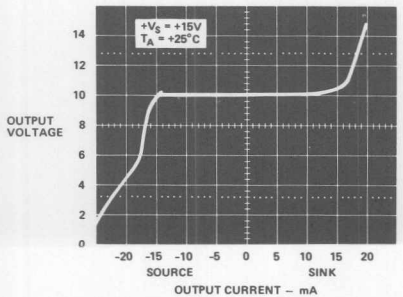


Figure 5. AD581 Output Voltage vs. Sink and Source Current

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 6 displays the turn-on characteristic of the AD581. This characteristic is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±10 millivolt is about 180μs, and there is no long thermal tail appearing after the point.

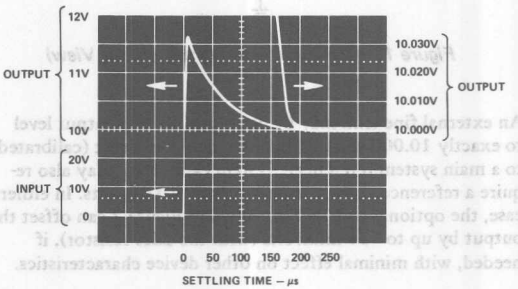


Figure 6. Output Settling Characteristic

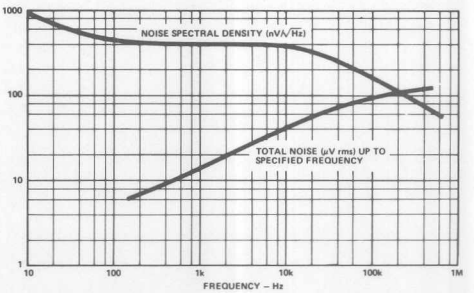


Figure 7. Spectral Noise Density and Total rms Noise vs. Frequency

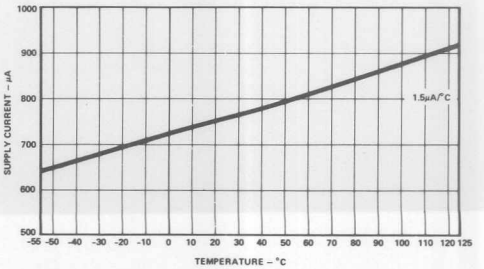


Figure 8. Quiescent Current vs. Temperature

darlington pnp devices to provide much greater output current capability. The circuit shown in Figure 9 delivers a precision 10 volt output with up to 4 amperes supplied to the load. The 0.1μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results from removing the capacitor.

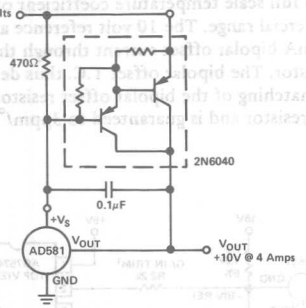


Figure 9. High Current Precision Supply

CONNECTION FOR REDUCED PRIMARY SUPPLY

While line regulation is specified down to 13 volts, the typical AD581 will work as specified down to 12 volts or below. The current sink capability allows even lower supply voltage capability such as operation from 12V ±5% as shown in Figure 10. The 560Ω resistor reduces the current supplied by the AD581 to a manageable level at full 5mA load. Note that the other bandgap references, without current sink capability, may be damaged by use in this circuit configuration.

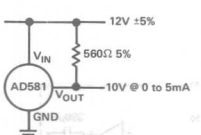


Figure 10. 12-Volt Supply Connection

THE AD581 AS A CURRENT LIMITER

The AD581 represents an alternative to current limiter diodes which require factory selection to achieve a desired current. This approach often results in temperature coefficients of 1%/°C. The AD581 approach is not limited to a defined set current limit; it can be programmed from 0.75 to 5mA with the insertion of a single external resistor. Of course, the minimum voltage required to drive the connection is 13 volts. The AD580, which is a 2.5 volt reference, can be used in this type of circuit with compliance voltage down to 4.5 volts.

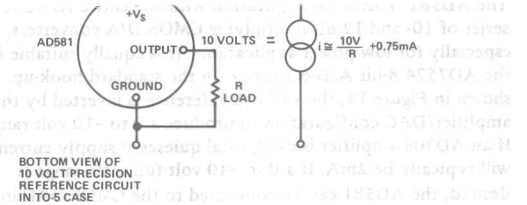


Figure 11. A Two-Component Precision Current Limiter

NEGATIVE 10-VOLT REFERENCE

The AD581 can also be used in a two-terminal "Zener" mode to provide a precision −10.00 volt reference. As shown in Figure 13, the V_{IN} and V_{OUT} terminals are connected together to the high supply (in this case, ground). The ground pin is connected through a resistor to the negative supply. The output is now taken from the ground pin instead of V_{OUT}. With 1mA flowing through the AD581 in this mode, a typical unit will show a 2mV increase in output level over that produced in the three-terminal mode. Note also that the effective output impedance in this connection increases from 0.2Ω typical to 2 ohms. It is essential to arrange the output load and the supply resistor, R_S, so that the net current through the AD581 is always between 1 and 5mA. For operation to +125°C, the net current should be between 2 and 5mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard three-terminal mode.

The AD581 can also be used in a two-terminal mode to develop a positive reference. V_{IN} and V_{OUT} are tied together and to the positive supply through an appropriate supply resistor. The performance characteristics will be similar to those of the negative two-terminal connection. The only advantage of this connection over the standard three-terminal connection is that a lower primary supply can be used, as low as 10.5 volts. This type of operation will require considerable attention to load and primary supply regulation to be sure the AD581 always remains within its regulating range of 1 to 5mA (2 to 5mA for operation beyond +85°C).

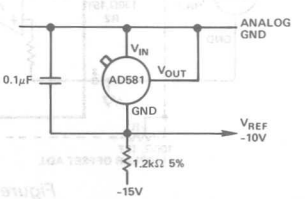


Figure 12. Two-Terminal −10 Volt Reference

6

10 VOLT REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD581 is ideal for application with the entire AD7533 series of 10- and 12-bit multiplying CMOS D/A converters, especially for low power applications. It is equally suitable for the AD7574 8-bit A/D converter. In the standard hook-up, as shown in Figure 14, the +10 volt reference is inverted by the amplifier/DAC configuration to produce a 0 to −10 volt range. If an AD308 amplifier is used, total quiescent supply current will typically be 2mA. If a 0 to +10 volt full scale range is desired, the AD581 can be connected to the CMOS DAC in its −10 volt "Zener" mode, as shown in Figure 12 (the $-10V_{REF}$ output is connected directly to the $V_{REF\ IN}$ of the CMOS DAC). The AD581 will normally be used in the −10 volt mode with the AD7574 to give a 0 to +10 volt ADC range. This is shown in Figure 14. Bipolar output applications and other operating details can be found in the data sheets for the CMOS products.

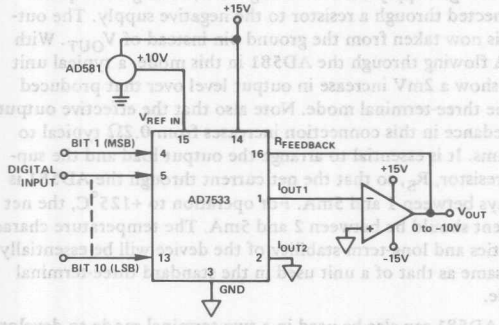


Figure 13. Low Power 10-Bit CMOS DAC Application

PRECISION 12-BIT D/A CONVERTER REFERENCE

The AD562, like most D/A converters, is designed to operate with a +10 volt reference element. In the AD562, this 10 volt reference voltage is converted into a reference current of approximately 0.5mA via the internal 19.95kΩ resistor (in series with the external 100Ω trimmer). The gain temperature coefficient of the AD562 is primarily governed by the temperature tracking of the 19.95kΩ resistor and the 5k/10k span resistors; this gain T.C. is guaranteed to 3ppm/°C. Thus, using the AD581L (at 5ppm/°C) as the 10 volt reference guarantees a maximum full scale temperature coefficient of 8ppm/°C over the commercial range. The 10 volt reference also supplies the normal 1mA bipolar offset current through the 9.95k bipolar offset resistor. The bipolar offset T.C. thus depends only on the T.C. matching of the bipolar offset resistor to the input reference resistor and is guaranteed to 3ppm/°C.

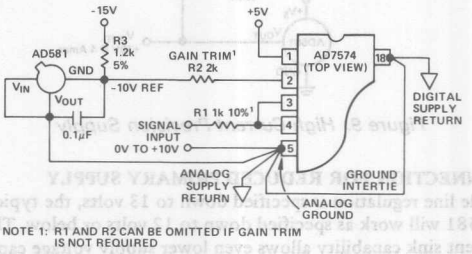


Figure 14. AD581 as Negative 10-Volt Reference for CMOS ADC

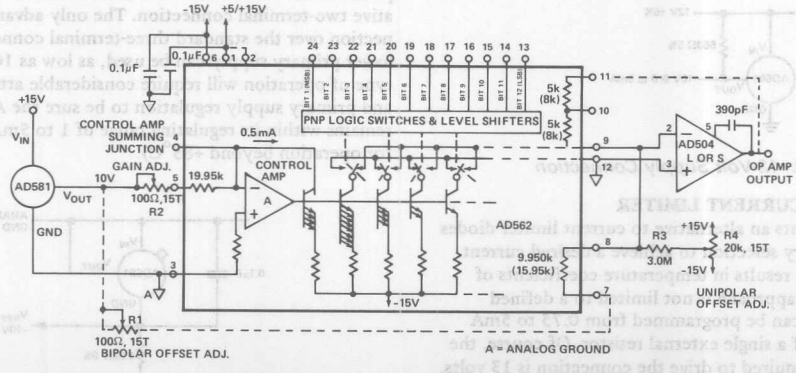


Figure 15. Precision 12-Bit D/A Converter

Pin Programmable Precision Voltage Reference

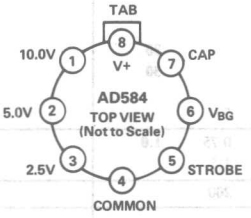
AD584*

FEATURES

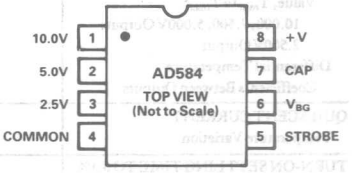
- Four Programmable Output Voltages:
  - 10.000V, 7.500V, 5.000V, 2.500V
- Laser-Trimmed to High Accuracies
- No External Components Required
- Trimmed Temperature Coefficient:
  - 5ppm/°C max, 0 to +70°C (AD584L)
  - 15ppm/°C max, −55°C to +125°C (AD584T)
- Zero Output Strobe Terminal Provided
- Two Terminal Negative Reference Capability (5V & Above)
- Output Sources or Sinks Current
- Low Quiescent Current: 1.0mA max
- 10mA Current Output Capability
- MIL-STD-883 Compliant Versions Available

PIN CONFIGURATIONS

8-Pin TO-99



8-Pin DIP



PRODUCT DESCRIPTION

The AD584 is an eight-terminal precision voltage reference offering pin-programmable selection of four popular output voltages: 10.000V, 7.500V, 5.000V and 2.500V. Other output voltages, above, below or between the four standard outputs, are available by the addition of external resistors. Input voltage may vary between 4.5 and 30 volts.

Laser Wafer Trimming (LWT) is used to adjust the pin-programmable output levels and temperature coefficients, resulting in the most flexible high precision voltage reference available in monolithic form.

In addition to the programmable output voltages, the AD584 offers a unique strobe terminal which permits the device to be turned on or off. When the AD584 is used as a power supply reference, the supply can be switched off with a single, low-power signal. In the "off" state the current drain by the AD584 is reduced to about 100μA. In the "on" state the total supply current is typically 750μA including the output buffer amplifier.

The AD584 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters of up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD584J, K and L are specified for operation from 0 to +70°C; the AD584S and T are specified for the -55°C to +125°C range. All grades are packaged in a hermetically sealed eight-terminal TO-99 metal can; the AD584J and K are also available in an 8-pin plastic DIP.

*Protected by U.S. Patent No. 3,887,863; RE 30, 586

PRODUCT HIGHLIGHTS

1. The flexibility of the AD584 eliminates the need to design-in and inventory several different voltage references. Furthermore one AD584 can serve as several references simultaneously when buffered properly.
2. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD584LH has a maximum deviation from 10.000 volts of ±7.25mV from 0 to +70°C.
3. The AD584 can be operated in a two-terminal "Zener" mode at 5 volts output and above. By connecting the input and the output, the AD584 can be used in this "Zener" configuration as a negative reference.
4. The output of the AD584 is configured to sink or source currents. This means that small reverse currents can be tolerated in circuits using the AD584 without damage to the reference and without disturbing the output voltage (10V, 7.5V and 5V outputs).
5. The AD584 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD584/883B data sheet for detailed specifications.

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AD584—SPECIFICATIONS (@ V_{IN} = 15V and 25°C)

Model	AD584J Min	AD584J Typ	AD584J Max	AD584K Min	AD584K Typ	AD584K Max	AD584L Min	AD584L Typ	AD584L Max	Units
OUTPUT VOLTAGE TOLERANCE										
Maximum Error[1] for Nominal Outputs of:										
10.000V			±30			±10			±5	mV
7.500V			±20			±8			±4	mV
5.000V			±15			±6			±3	mV
2.500V			±7.5			±3.5			±2.5	mV
OUTPUT VOLTAGE CHANGE										
Maximum Deviation from +25°C Value, T_{min} to T_{max}[2]										
10.000, 7.500, 5.000V Outputs			30			15			5	ppm/°C
2.500V Output			30			15			10	ppm/°C
Differential Temperature Coefficients Between Outputs		5			3			3		ppm/°C
QUIESCENT CURRENT		0.75	1.0		0.75	1.0		0.75	1.0	mA
Temperature Variation		1.5			1.5			1.5		µA/°C
TURN-ON SETTLING TIME TO 0.1%		200			200			200		µs
NOISE (0.1 to 10Hz)		50			50			50		µV p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 Hrs.
SHORT-CIRCUIT CURRENT		30			30			30		mA
LINE REGULATION (No Load)										
15V≤V_{IN}≤30V			0.002			0.002			0.002	%/V
(V_{OUT} + 2.5V)≤V_{IN}≤15V			0.005			0.005			0.005	%/V
LOAD REGULATION										
0≤I_{OUT}≤5mA, All Outputs		20	50		20	50		20	50	ppm/mA
OUTPUT CURRENT										
V_{IN}≥V_{OUT} + 2.5V										
Source @ +25°C	10			10			10			mA
Source T_{min} to T_{max}	5			5			5			mA
Sink T_{min} to T_{max}	5			5			5			mA
TEMPERATURE RANGE										
Operating	0		+70	0		+70	0		+70	°C
Storage	−65		+175	−65		+175	−65		+175	°C
PACKAGE OPTION[3]										
TO-99 (H-08A)		AD584JH			AD584KH			AD584LH		
Plastic (N-8)		AD584JN			AD584KN					

NOTES
[1]At Pin 1.
[2]Calculated as average over the operating temperature range.
[3]H = Hermetic Metal Can; N = Plastic DIP. For package outline information see Package Information section.

Specifications subject to change without notice.

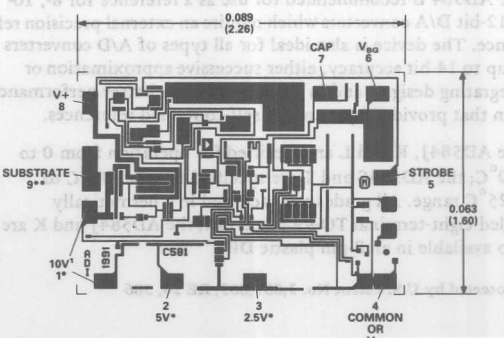
Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAX RATINGS

Input Voltage V_{IN} to Ground 40V
Power Dissipation @ +25°C 600mW
Operating Junction Temperature Range . . −55°C to +125°C
Lead Temperature (Soldering 10sec) . . . . . +300°C
Thermal Resistance
Junction-to-Ambient (H-08A) . . . . . 150°C/W

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



NOTES
[1]BOTH 10V PADS MUST BE CONNECTED TO THE OUTPUT.
*INTERCONNECTIONS REQUIRED; SEE PIN DESIGNATIONS FOR INFORMATION.
**NOT BROUGHT OUT IN PACKAGE DEVICE.
PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99, 8-PIN METAL PACKAGE.

Model	AD584S Min	AD584S Typ	AD584S Max	AD584T Min	AD584T Typ	AD584T Max	Units
OUTPUT VOLTAGE TOLERANCE							
Maximum Error[1] for Nominal Outputs of:							
10.000V			**±30**			**±10**	mV
7.500V			**±20**			**±8**	mV
5.000V			**±15**			**±6**	mV
2.500V			**±7.5**			**±3.5**	mV
OUTPUT VOLTAGE CHANGE							
Maximum Deviation from +25°C Value, T_{min} to T_{max}[2]							
10.000, 7.500, 5.000V Outputs			**30**			**15**	ppm/°C
2.500V Output			**30**			**20**	ppm/°C
Differential Temperature Coefficients Between Outputs		5			3		ppm/°C
QUIESCENT CURRENT		0.75	**1.0**		0.75	**1.0**	mA
Temperature Variation		1.5			1.5		µA/°C
TURN-ON SETTLING TIME TO 0.1%		200			200		µs
NOISE (0.1 to 10Hz)		50			50		µV p-p
LONG-TERM STABILITY		25			25		ppm/1000 Hrs.
SHORT-CIRCUIT CURRENT		30			30		mA
LINE REGULATION (No Load)							
$15V \leq V_{IN} \leq 30V$			**0.002**			**0.002**	%/V
$(V_{OUT} + 2.5V) \leq V_{IN} \leq 15V$			**0.005**			**0.005**	%/V
LOAD REGULATION $0 \leq I_{OUT} \leq 5mA$, All Outputs		20	**50**		20	**50**	ppm/mA
OUTPUT CURRENT $V_{IN} \geq V_{OUT} + 2.5V$							
Source @ +25°C	10			10			mA
Source T_{min} to T_{max}	5			5			mA
Sink T_{min} to T_{max}	5			5			mA
TEMPERATURE RANGE							
Operating	−55		+125	−55		+125	°C
Storage	−65		+175	−65		+175	°C
PACKAGE OPTIONS[3]							
TO-99 (H-08A)		AD584SH			AD584TH		

NOTES
[1]At Pin 1.
[2]Calculated as average over the operating temperature range.
[3]H = Hermetic Metal Can. For outline information see Package Information section.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Applying the AD584

APPLYING THE AD584

With power applied to pins 8 and 4 and all other pins open the AD584 will produce a buffered nominal 10.0V output between pins 1 and 4 (see Figure 1). The stabilized output voltage may be reduced to 7.5V, 5.0V or 2.5V by connecting the programming pins as follows:

OUTPUT VOLTAGE	PIN PROGRAMMING
7.5V	Join the 2.5V and 5.0V pins (2) and (3).
5.0V	Connect the 5.0V pin (2) to the output pin (1).
2.5V	Connect the 2.5V pin (3) to the output pin (1).

The options shown above are available without the use of any additional components. Multiple outputs using only one AD584, are also possible by simply buffering each voltage programming pin with a unity-gain noninverting op amp.

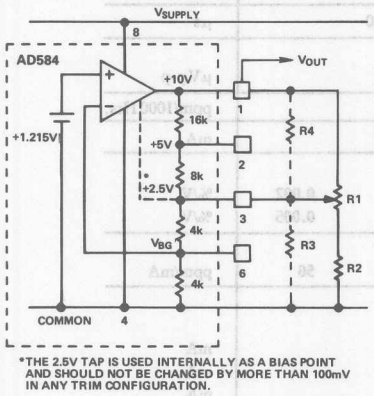


Figure 1. Variable Output Options

The AD584 can also be programmed over a wide range of output voltages, including voltages greater than 10V, by the addition of one or more external resistors. Figure 1 illustrates the general adjustment procedure, with approximate values given for the internal resistors of the AD584. The AD584 may be modeled as an op amp with a noninverting feedback connection, driven by a high stability 1.215 volt bandgap reference (see Figure 3 for schematic).

When the feedback ratio is adjusted with external resistors, the output amplifier can be made to multiply the reference voltage by almost any convenient amount, making popular outputs of 10.24V, 5.12V, 2.56V or 6.3V easy to obtain. The most general adjustment (which gives the greatest range and poorest resolution) uses R1 and R2 alone (see Figure 1). As R1 is adjusted to its upper limit the 2.5V pin 3 will be connected to the output, which will reduce to 2.5V. As R1 is adjusted to its lower limit, the output voltage will rise to a value limited by R2. For example, if R2 is about 6kΩ, the upper limit of the output range will be about 20V even for large values of R1. R2 should not be omitted; its value should be chosen to limit the output to a value which can be tolerated by the load circuits. If R2 is zero, adjusting R1 to its lower limit will result in a loss of control over the output voltage. If precision voltages are required to be set at levels other than the standard outputs, the 20% absolute tolerance in the internal resistor ladder must be accounted for.

Alternatively, the output voltage can be raised by loading the 2.5V tap with R3 alone. The output voltage can be lowered by connecting R4 alone. Either of these resistors can be a fixed resistor selected by test or an adjustable resistor. In all cases the resistors should have a low temperature coefficient to match the AD584 internal resistors, which have a negative T.C. less than 60ppm/°C. If both R3 and R4 are used, these resistors should have matched temperature coefficients.

When only small adjustments or trims are required, the circuit of Figure 2 offers better resolution over a limited trim range. The circuit can be programmed to 5.0V, 7.5V or 10V and adjusted by means of R1 over a range of about ±200mV. To trim the 2.5V output option, R2 (Figure 2) can be reconnected to the bandgap reference (pin 6). In this configuration, the adjustment should be limited to ±100mV in order to avoid affecting the performance of the AD584.

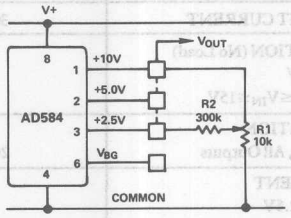


Figure 2. Output Trimming

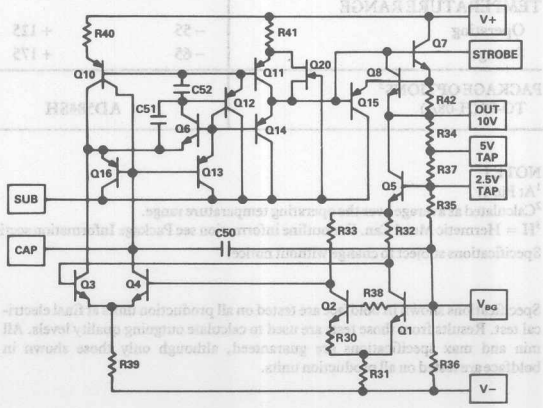


Figure 3. Schematic Diagram

PERFORMANCE OVER TEMPERATURE

Each AD584 is tested at three temperatures over the -55°C to +125°C range to ensure that each device falls within the Maximum Error Band (see Figure 4) specified for a particular grade (i.e., S and T grades); three-point measurement also guarantees performance within the error band from 0 to +70°C (i.e., J, K, or L grades). The error band guaranteed for the AD584 is the maximum deviation from the initial value at +25°C. Thus, given the grade of the AD584, the designer can easily determine the maximum total error from initial tolerance plus temperature variation. For example, for the AD584T, the initial tolerance is ±10mV and the error band is ±15mV. Hence, the unit is guaranteed to be 10.000 volts ±25mV from -55°C to +125°C.

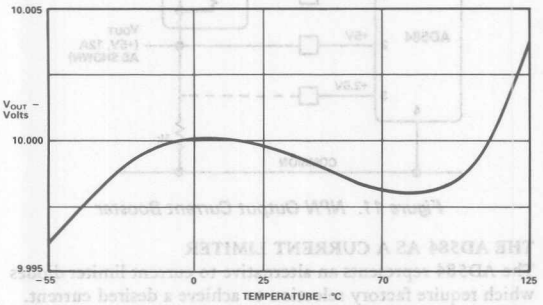


Figure 4. Typical Temperature Characteristic

OUTPUT CURRENT CHARACTERISTICS

The AD584 has the capability to either source or sink current and provide good load regulation in either direction, although it has better characteristics in the source mode (positive current into the load). The circuit is protected for shorts to either positive supply or ground. The output voltage vs. output current characteristics of the device is shown in Figure 5. Source current is displayed as negative current in the figure; sink current is positive. Note that the short circuit current (i.e., zero volts output) is about 28mA; when shorted to +15 volts, the sink current goes to about 20mA.

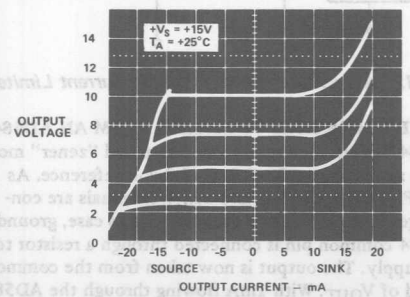


Figure 5. AD584 Output Voltage vs. Sink and Source Current

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 6 displays the turn-on characteristic of the AD584. Figure 6a is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±10 millivolts is about 180μs, and there is no long thermal tail appearing after the point.

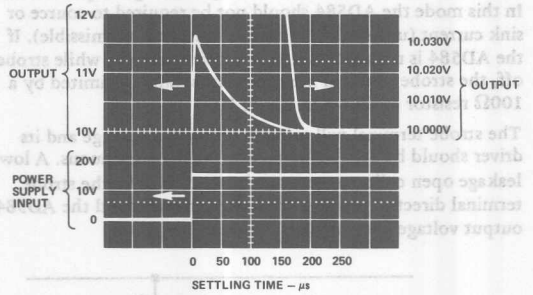


Figure 6. Output Settling Characteristic

NOISE FILTERING

The bandwidth of the output amplifier in the AD584 can be reduced to filter the output noise. A capacitor ranging between 0.01μF and 0.1μF connected between the Cap and V_{BG} terminals will further reduce the wideband and feedthrough noise in the output of the AD584, as shown in Figure 8. However, this will tend to increase the turn-on settling time of the device so ample warm-up time should be allowed.

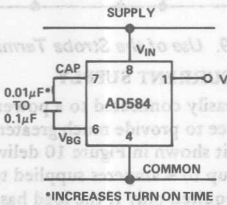


Figure 7. Additional Noise Filtering with an External Capacitor

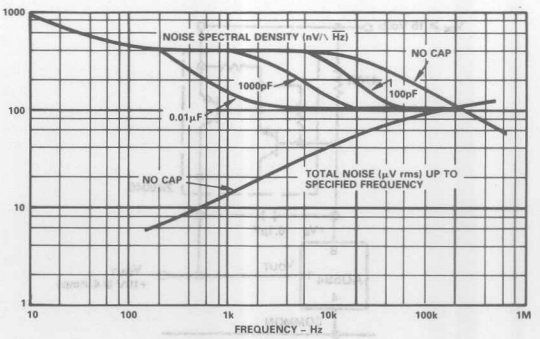


Figure 8. Spectral Noise Density and Total rms Noise vs. Frequency

AD584—Applications

USING THE STROBE TERMINAL

The AD584 has a strobe input which can be used to zero the output. This unique feature permits a variety of new applications in signal and power conditioning circuits.

Figure 9 illustrates the strobe connection. A simple NPN switch can be used to translate a TTL logic signal into a strobe of the output. The AD584 operates normally when there is no current drawn from pin 5. Bringing this terminal low, to less than 200mV, will allow the output voltage to go to zero. In this mode the AD584 should not be required to source or sink current (unless a 0.7V residual output is permissible). If the AD584 is required to sink a transient current while strobed off, the strobe terminal input current should be limited by a 100Ω resistor as shown in Figure 9.

The strobe terminal will tolerate up to 5μA leakage and its driver should be capable of sinking 500μA continuous. A low leakage open collector gate can be used to drive the strobe terminal directly, provided the gate can withstand the AD584 output voltage plus one volt.

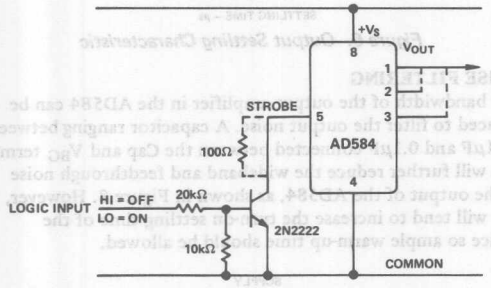


Figure 9. Use of the Strobe Terminal

PRECISION HIGH CURRENT SUPPLY

The AD584 can be easily connected to a power PNP or power Darlington PNP device to provide much greater output current capability. The circuit shown in Figure 10 delivers a precision 10 volt output with up to 4 amperes supplied to the load. The 0.1μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results from removing the capacitor.

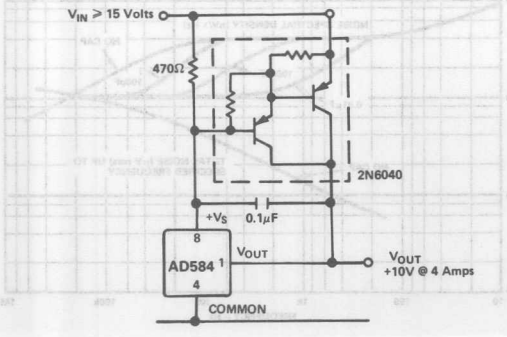


Figure 10. High Current Precision Supply

The AD584 can also use an NPN or Darlington NPN transistor to boost its output current. Simply connect the 10V output terminal of the AD584 to the base of the NPN booster and take the output from the booster emitter as shown in Figure 11. The 5.0V or 2.5V pin must connect to the actual output in this configuration. Variable or adjustable outputs (as shown in Figures 1 and 2) may be combined with +5.0V connection to obtain outputs above +5.0V.

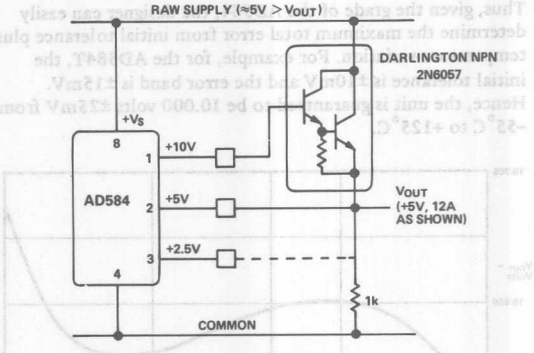


Figure 11. NPN Output Current Booster

THE AD584 AS A CURRENT LIMITER

The AD584 represents an alternative to current limiter diodes which require factory selection to achieve a desired current. Use of current limiting diodes often results in temperature coefficients of 1%/°C. Use of the AD584 in this mode is not limited to a set current limit; it can be programmed from 0.75 to 5mA with the insertion of a single external resistor (see Figure 12). Of course, the minimum voltage required to drive the connection is 5 volts.

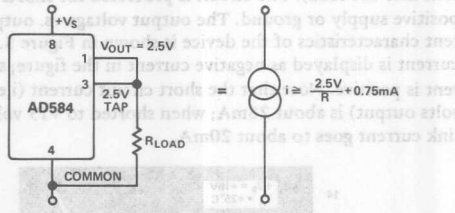


Figure 12. A Two-Component Precision Current Limiter

NEGATIVE REFERENCE VOLTAGES FROM AN AD584

The AD584 can also be used in a two-terminal "zener" mode to provide a precision –10, –7.5 or –5.0 volt reference. As shown in Figure 13, the V_{IN} and V_{OUT} terminals are connected together to the positive supply (in this case, ground). The AD584 common pin is connected through a resistor to the negative supply. The output is now taken from the common pin instead of V_{OUT}. With 1mA flowing through the AD584 in this mode, a typical unit will show a 2mV increase in output level over that produced in the three-terminal mode. Note also that the effective output impedance in this connection increases from 0.2Ω typical to 2Ω. It is essential to arrange the output load and the supply resistor, R_S, so that the net current through the AD584 is always between 1 and 5mA (between 2 and 5mA for operation beyond +85°C). The temperature characteristics and long-term stability of the

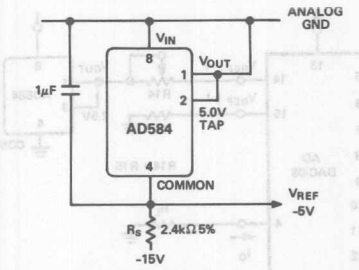


Figure 13. Two-Terminal -5 Volt Reference

device will be essentially the same as that of a unit used in the standard three-terminal mode.

The AD584 can also be used in a two-terminal mode to develop a positive reference. V_{IN} and V_{OUT} are tied together and to the positive supply through an appropriate supply resistor. The performance characteristics will be similar to those of the negative two-terminal connection. The only advantage of this connection over the standard three-terminal connection is that a lower primary supply can be used, as low as 0.5 volts above the desired output voltage. This type of operation will require considerable attention to load and primary supply regulation to be sure the AD584 always remains within its regulating range of 1 to 5mA (2 to 5mA for operation beyond 85°C).

10 VOLT REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD584 is ideal for application with the entire AD7520 series of 10- and 12-bit multiplying CMOS D/A converters, especially for low power applications. It is equally suitable for the AD7574 8-bit A/D converter. In the standard hook-up as shown in Figure 14, the standard output voltages are inverted by the amplifier/DAC configuration to produce converted voltage ranges. For example, a +10V reference produces a 0 to -10V range. If an AD308 amplifier is used, total quiescent supply current will typically be 2mA. The AD584 will normally be used in the -10 volt mode with the AD7574 to give a 0 to +10 volt ADC range. This is shown in Figure 16. Bipolar output applications and other operating details can be found in the data sheets for the CMOS products.

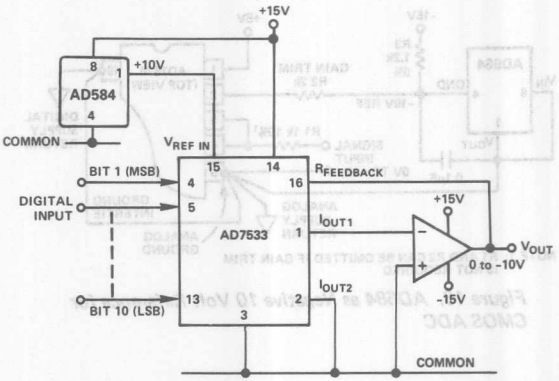


Figure 14. Low Power 10-Bit CMOS DAC Application

PRECISION D/A CONVERTER REFERENCE

The AD562, like many D/A converters, is designed to operate with a +10 volt reference element (Figure 15). In the AD562, this 10 volt reference voltage is converted into a reference current of approximately 0.5mA via the internal 19.95kΩ resistor (in series with the external 100Ω trimmer). The gain temperature coefficient of the AD562 is primarily governed by the temperature tracking of the 19.95kΩ resistor and the 5k/10k

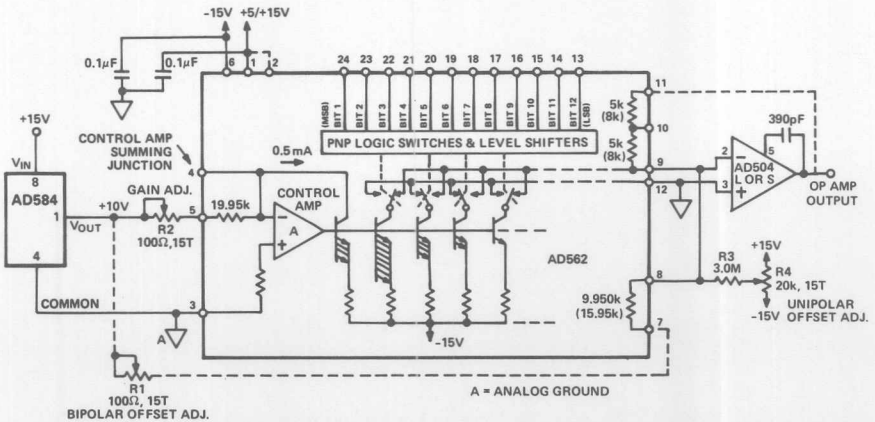
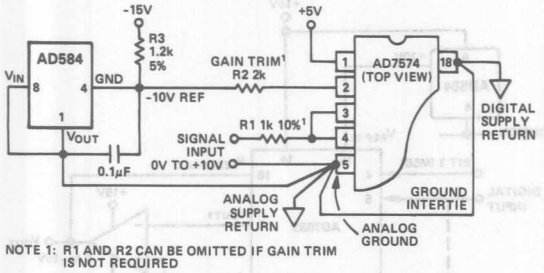


Figure 15. Precision 12-Bit D/A Converter

using the AD584L (at 5ppm/˚C) as the 10 volt reference guarantees a maximum full scale temperature coefficient of 8ppm/°C over the commercial range. The 10 volt reference also supplies the normal 1mA bipolar offset current through the 9.95k bipolar offset resistor. The bipolar offset T.C. thus depends only on the T.C. matching of the bipolar offset resistor to the input reference resistor and is guaranteed to 3ppm/°C. Figure 17 demonstrates the flexibility of the AD584 applied to another popular D/A configuration.



NOTE 1: R1 AND R2 CAN BE OMITTED IF GAIN TRIM IS NOT REQUIRED

Figure 16. AD584 as Negative 10 Volt Reference for CMOS ADC

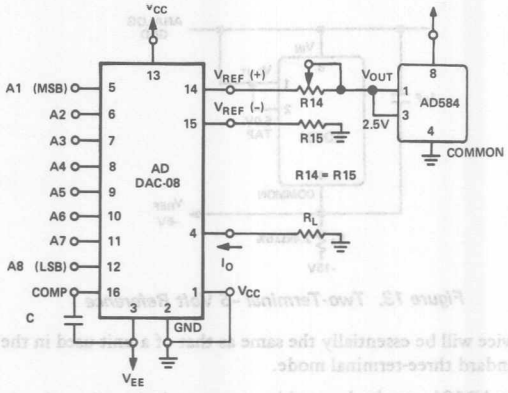


Figure 17. Current Output 8-Bit D/A

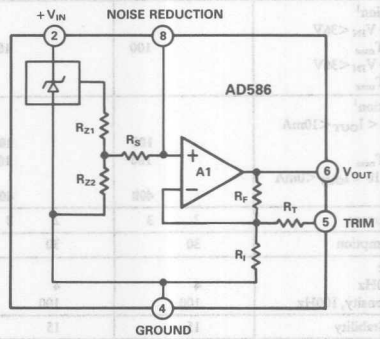
High-Precision 5V Reference

AD586

FEATURES

Laser Trimmed to High Accuracy:
5.000V ±2.0mV (M Grade)
Trimmed Temperature Coefficient:
2ppm/°C max, 0 to +70°C (M Grade)
10ppm/°C max, −55°C to +125°C (T Grade)
Noise Reduction Capability
Low Quiescent Current: 3mA max
Output Trim Capability
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



NOTE: PINS 1, 3 & 7 ARE INTERNAL TEST POINTS.
MAKE NO CONNECTIONS TO THESE POINTS.

PRODUCT DESCRIPTION

The AD586 represents a major advance in the state-of-the-art in monolithic voltage references. Using a proprietary ion-implanted buried Zener diode and laser wafer trimming of high stability thin-film resistors, the AD586 provides outstanding performance at low cost.

The AD586 offers much higher performance than most other 5V references. Because the AD586 uses an industry standard pinout, many systems can be upgraded instantly with the AD586. The buried Zener approach to reference design provides lower noise and drift than bandgap voltage references. The AD586 offers a noise reduction pin which can be used to further reduce the noise level generated by the buried Zener.

The AD586 is recommended for use as a reference for 8-, 10-, 12-, 14- or 16-bit D/A converters which require an external precision reference. The device is also ideal for successive approximation or integrating A/D converters with up to 14 bits of accuracy and, in general, can offer better performance than the standard on-chip references.

The AD586J, K, L and M are specified for operation from 0 to +70°C, and the AD586S and T are specified for −55°C to +125°C operation. All grades, except for the AD586M, are packaged in an 8-pin cerdip package. The AD586J, K, L and M are available in an 8-pin plastic package. The AD586J and the AD586K are also available in an 8-pin plastic surface mount small outline (SO) package.

PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficients results in very low errors over temperature without the use of external components. The AD586M has a maximum deviation from 5.000V of ±2.45mV between 0 and +70°C, and the AD586T guarantees ±7.5mV maximum total error between −55°C and +125°C.
2. For applications requiring higher precision, an optional fine-trim connection is provided.
3. Any system using an industry standard pinout reference can be upgraded instantly with the AD586.
4. Output noise of the AD586 is very low, typically 4μV p-p. A noise reduction pin is provided for additional noise filtering using an external capacitor.
5. The AD586 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD586/883B data sheet for detailed specifications.

AD586—SPECIFICATIONS ($T_A = +25°C$, $V_{IN} = +15V$ unless otherwise specified)

Model	AD586J Min	AD586J Typ	AD586J Max	AD586K Min	AD586K Typ	AD586K Max	AD586L Min	AD586L Typ	AD586L Max	AD586M Min	AD586M Typ	AD586M Max	AD586S Min	AD586S Typ	AD586S Max	AD586T Min	AD586T Typ	AD586T Max	Units
Output Voltage	4.980		5.020	4.995		5.005	4.9975		5.0025	4.998		5.002	4.990		5.010	4.9975		5.0025	V
Output Voltage Drift[1]																			
0 to +70°C			25			15			5			2							ppm/°C
−55°C to +125°C															20			10	
Gain Adjustment	+6			+6			+6			+6			+6			+6			%
	−2			−2			−2			−2			−2			−2			
Line Regulation[1]																			
$10.8V < +V_{IN} < 36V$																			
T_{min} to T_{max}			100			100			100			100							±μV/V
$11.4V < +V_{IN} < 36V$																			
T_{min} to T_{max}															150			150	
Load Regulation[1]																			
Sourcing $0 < I_{OUT} < 10mA$																			
25°C			100			100			100			100			150			150	μV/mA
T_{min} to T_{max}			100			100			100			100			150			150	
Sinking $-10 < I_{OUT} < 0mA$																			
25°C			400			400			400			400			400			400	
Quiescent Current		2	3		2	3		2	3		2	3		2	3		2	3	mA
Power Consumption		30			30			30			30			30			30		mW
Output Noise																			
0.1Hz to 10Hz		4			4			4			4			4			4		μV p-p
Spectral Density, 100Hz		100			100			100			100			100			100		nV/√Hz
Long-Term Stability		15			15			15			15			15			15		ppm/1000Hr
Short-Circuit Current-to-Ground		45	60		45	60		45	60		45	60		45	60		45	60	mA
Temperature Range																			
Specified Performance	0		+70	0		+70	0		+70	0		+70	−55		+125	−55		+125	°C
Operating Performance[2]	−40		+85	−40		+85	−40		+85	−40		+85	−55		+125	−55		+125	

NOTES

[1]Maximum output voltage drift is guaranteed for all packages and grades. Cerdip packaged parts are also 100% production tested.

[2]The operating temperature ranged is defined as the temperatures extremes at which the device will still function. Parts may deviate from their specified performance outside their specified temperature range.

Specifications subject to change without notice.

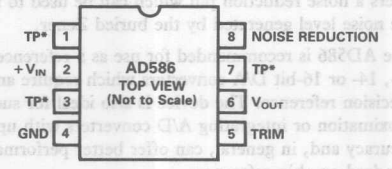
Specifications in boldface are tested on all production units at final electrical test. Result from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS*

V_{IN} to Ground 36V
Power Dissipation (25°C) 500mW
Storage Temperature . . . . . −65°C to +150°C
Lead Temp (Soldering, 10sec) . . . . . 300°C
Package Thermal Resistance
θ_{JC} . . . . . 22°C/W
θ_{JA} . . . . . 110°C/W
Output Protection: Output safe for indefinite short to ground or V_{IN}.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM
(Top View)



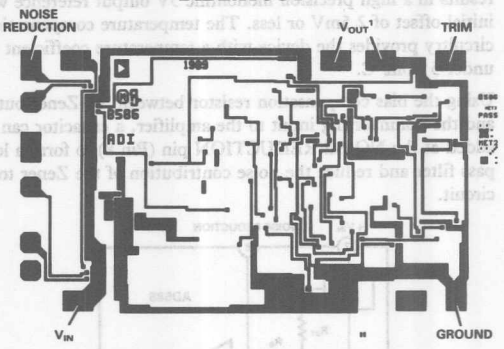
*TP DENOTES FACTORY TEST POINT. NO CONNECTIONS SHOULD BE MADE TO THESE PINS.

DIE SPECIFICATIONS

The following specifications are tested at the die level for AD586JCHIPS. These die are probed at 25°C only. (T_A = +25°C, V_{IN} = +15V unless otherwise specified)

Parameter	AD586JCHIPS Min	Typ	Max	Units
Output Voltage	4.980		5.020	V
Gain Adjustment	+6			%
	−2			%
Line Regression				
10.8V < +V_{IN} <36V			100	±μV/V
Load Regulation				
Sourcing 0<I_{OUT} <10mA			100	μV/mA
Sinking −10<I_{OUT} <0mA			400	μV/mA
Quiescent Current			3	mA
Short-Circuit Current-to-Ground			60	mA

DIE LAYOUT



Die Size: 0.96 × 0.061 inches

NOTES

[1]Both V_{OUT} pads should be connected to the output.

Die Thickness: The standard thickness of Analog Devices Bipolar dice is 24 mils ± 2 mils.

Die Dimensions: The dimensions given have a tolerance of ± 2 mils.

Backing: The standard backside surface is silicon (not plated). Analog Devices does not recommend gold-backed dice for most applications.

Edges: A diamond saw is used to separate wafers into dice thus providing perpendicular edges half-way through the die. In contrast to scribed dice, this technique provides a more uniform die shape and size. The perpendicular edges facilitate handling (such as tweezer pick-up) while the uniform shape and size simplifies substrate design and die attach.

Top Surface: The standard top surface of the die is covered by a layer of glassivation. All areas are covered except bonding pads and scribe lines.

Surface Metalization: The metalization to Analog Devices bipolar dice is aluminum. Minimum thickness is 10,000Å.

Bonding Pads: All bonding pads have a minimum size of 4 mils by 4 mils. The passivation windows have 3.5 mils by 3.5 mils minimum.

ORDERING GUIDE

Model[1]	Initial Error mV	Temp. Coefficient ppm/°C	Temp. Range °C	Package Option[2]
AD586JN	20	25	0 to +70	N-8
AD586JQ	20	25	0 to +70	Q-8
AD586JR	20	25	0 to +70	R-8
AD586KN	5	15	0 to +70	N-8
AD586KQ	5	15	0 to +70	Q-8
AD586KR	5	15	0 to +70	R-8
AD586LN	2.5	5	0 to +70	N-8
AD586MN	2	2	0 to +70	N-8
AD586LQ	2.5	5	0 to +70	Q-8
AD586SQ	10	20	−55 to +125	Q-8
AD586TQ	2.5	10	−55 to +125	Q-8
AD586JCHIPS	20	25	0 to +70	–

NOTES

[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD586/883B data sheet.

[2]N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

6

an amplifier to buffer the output and several high stability thin-film resistors as shown in the block diagram in Figure 1. This design results in a high precision monolithic 5V output reference with initial offset of 2.5mV or less. The temperature compensation circuitry provides the device with a temperature coefficient of under 5 ppm/°C.

Using the bias compensation resistor between the Zener output and the noninverting input to the amplifier, a capacitor can be added at the NOISE REDUCTION pin (Pin 8) to form a low pass filter and reduce the noise contribution of the Zener to the circuit.

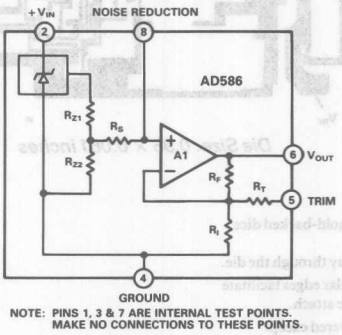


Figure 1. AD586 Functional Block Diagram

APPLYING THE AD586

The AD586 is simple to use in virtually all precision reference applications. When power is applied to Pin 2 and Pin 4 is grounded, Pin 6 provides a 5V output. No external components are required; the degree of desired absolute accuracy is achieved simply by selecting the required device grade. The AD586 requires less than 3mA quiescent current from an operating supply of +12V or +15V.

An external fine trim may be desired to set the output level to exactly 5.000V (calibrated to a main system reference). System calibration may also require a reference voltage that is slightly different from 5.000V, for example, 5.12V for binary applications. In either case, the optional trim circuit shown in Figure 2 can offset the output by as much as 300mV, if desired, with minimal effect on other device characteristics.

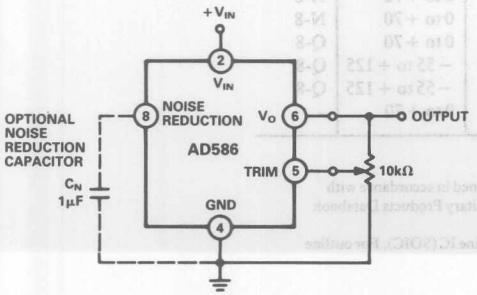


Figure 2. Optional Fine Trim Configuration

p-p over the 0.1Hz to 10Hz band. Noise in a 1MHz bandwidth is approximately 200μV p-p. The dominant source of this noise is the buried Zener which contributes approximately 100nV/$\sqrt{\text{Hz}}$. In comparison, the op amp's contribution is negligible. Figure 3 shows the 0.1Hz to 10Hz noise of a typical AD586. The noise measurement is made with a bandpass filter made of a 1-pole high-pass filter with a corner frequency at 0.1Hz and a 2-pole low-pass filter with a corner frequency at 12.6Hz to create a filter with a 9.922Hz bandwidth.

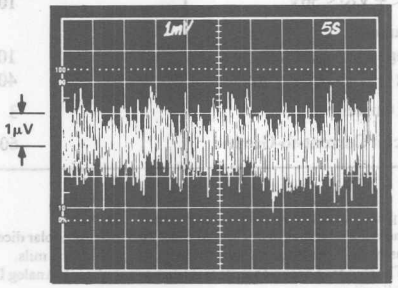


Figure 3. 0.1Hz to 10Hz Noise

If further noise reduction is desired, an external capacitor may be added between the NOISE REDUCTION pin and ground as shown in Figure 2. This capacitor, combined with the 4kΩ R_S and the Zener resistances form a low-pass filter on the output of the Zener cell. A 1μF capacitor will have a 3dB point at 12Hz, and it will reduce the high-frequency (to 1MHz) noise to about 160μV p-p. Figure 4 shows the 1MHz noise of a typical AD586 both with and without a 1μF capacitor.

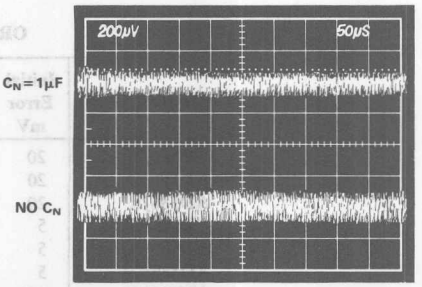
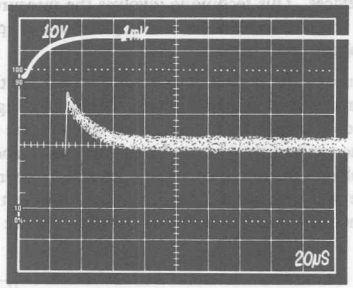


Figure 4. Effect of 1μF Noise Reduction Capacitor on Broadband Noise

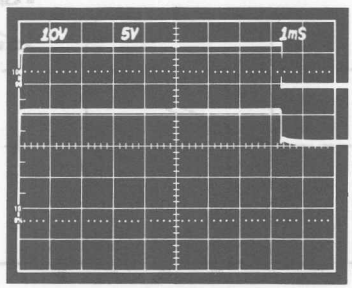
TURN-ON TIME

Upon application of power (cold start), the time required for the output voltage to reach its final value within a specified error band is defined as the turn-on settling time. Two components normally associated with this are: the time for the active circuits to settle, and the time for the thermal gradients on the chip to stabilize. Figure 5 shows the turn-on characteristics of the AD586. It shows the settling to be about 60μsec to 0.01%. Note the absence of any thermal tails when the horizontal scale is expanded to 1ms/cm in Figure 5b.

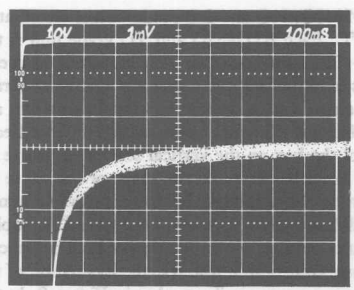
capacitor is used. When present, this capacitor acts as an additional load to the internal Zener diode's current source, resulting in a somewhat longer turn-on time. In the case of a 1μF capacitor, the initial turn-on time is approximately 400ms to 0.01% (see Figure 5c).



a. Electrical Turn-On



b. Extended Time Scale



c. Turn-On with 1μF C_N

Figure 5. Turn-On Characteristics

The output buffer amplifier is designed to provide the AD586 with static and dynamic load regulation superior to less complete references.

Many A/D and D/A converters present transient current loads to the reference, and poor reference response can degrade the converter's performance.

Figure 6 displays the characteristics of the AD586 output amplifier driving a 0 to 10mA load.

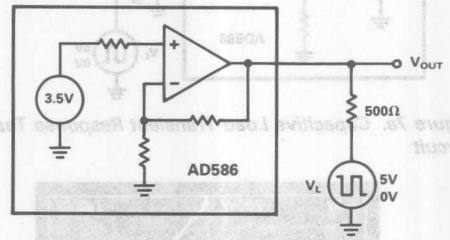


Figure 6a. Transient Load Test Circuit

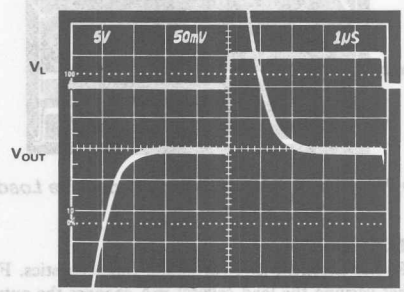


Figure 6b. Large-Scale Transient Response

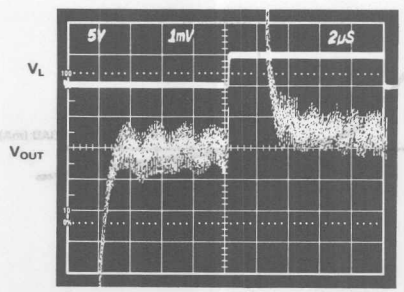


Figure 6c. Fine-Scale Settling for Transient Load

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In some applications, a varying load may be both resistive and capacitive in nature, or the load may be connected to the AD586 by a long capacitive cable.

Figure 7 displays the output amplifier characteristics driving a 1000pF, 0 to 10mA load.

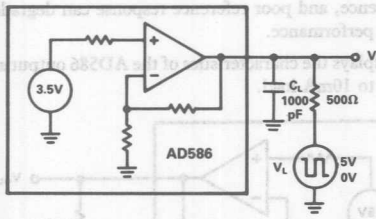


Figure 7a. Capacitive Load Transient Response Test Circuit

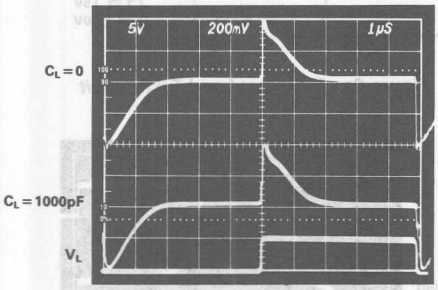


Figure 7b. Output Response with Capacitive Load

LOAD REGULATION

The AD586 has excellent load regulation characteristics. Figure 8 shows that varying the load several mA changes the output by a few μV. The AD586 has somewhat better load regulation performance sourcing current than sinking current.

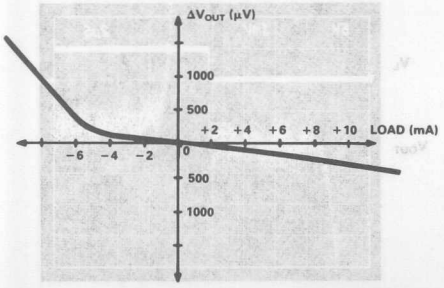


Figure 8. Typical Load Regulation Characteristics

TEMPERATURE PERFORMANCE

The AD586 is designed for precision reference applications where temperature performance is critical. Extensive temperature testing ensures that the device's high level of performance is maintained over the operating temperature range.

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centrigrade; i.e., ppm/°C. However, because of nonlinearities in temperature characteristics which originated in standard Zener references (such as "S" type characteristics), most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves the measurement of the output at three or more different temperatures to specify an output voltage error band.

Figure 9 shows the typical output voltage drift for the AD586L and illustrates the test methodology. The box in Figure 9 is bounded on the sides by the operating temperature extremes, and on the top and the bottom by the maximum and minimum output voltages measured over the operating temperature range. The slope of the diagonal drawn from the lower left to the upper right corner of the box determines the performance grade of the device.

$$\text{SLOPE} = \text{T.C.} = \frac{V_{max} - V_{min}}{(T_{max} - T_{min}) \times 5 \times 10^{-6}}$$

$$= \frac{5.0027 - 5.0012}{(70°C - 0) \times 5 \times 10^{-6}}$$

$$= 4.3\text{ppm/°C}$$

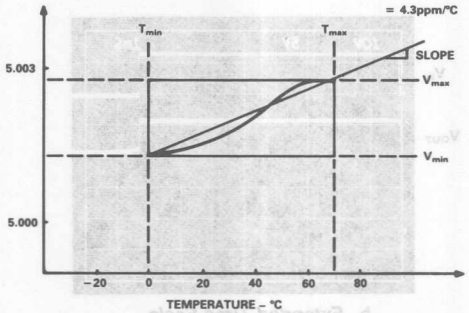


Figure 9. Typical AD586L Temperature Drift

Each AD586JQ, KQ and LQ grade unit is tested at 0, +25°C and +70°C. Each AD586SQ and TQ grade unit is tested at −55°C, +25°C and +125°C. This approach ensures that the variations of output voltage that occur as the temperature changes within the specified range will be contained within a box whose diagonal has a slope equal to the maximum specified drift. The position of the box on the vertical scale will change from device to device as initial error and the shape of the curve vary. The maximum height of the box for the appropriate temperature range and device grade is shown in Figure 10. Duplication of these results requires a combination of high accuracy and stable temperature control in a test system. Evaluation of the AD586 will produce a curve similar to that in Figure 9, but output readings may vary depending on the test methods and equipment utilized.

DEVICE GRADE	MAXIMUM OUTPUT CHANGE (mV)	
	0 TO +70°C	−55°C TO +125°C
AD586J	8.75	
AD586K	5.25	
AD586L	1.75	
AD586M	0.70	
AD586S		18.00
AD586T		9.00

Figure 10. Maximum Output Change in mV

NEGATIVE REFERENCE VOLTAGE FROM AN AD586

The AD586 can be used to provide a precision −5.000V output as shown in Figure 11. The V_{IN} pin is tied to at least a +6V supply, the output pin is grounded, and the AD586 ground pin is connected through a resistor, R_S, to a −15V supply. The −5V output is now taken from the ground pin (Pin 4) instead of V_{OUT}. It is essential to arrange the output load and the supply resistor R_S so that the net current through the AD586 is between 2.5mA and 10.0mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard +5V output configuration.

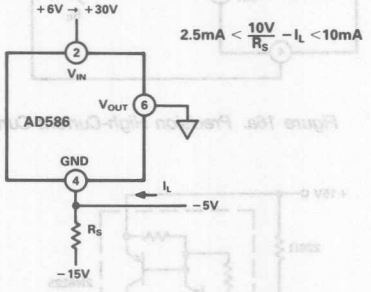


Figure 11. AD586 as a Negative 5V Reference

USING THE AD586 WITH CONVERTERS

The AD586 is an ideal reference for a wide variety of 8-, 12-, 14- and 16-bit A/D and D/A converters. Several representative examples follow.

5V REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD586 is ideal for applications with 10- and 12-bit multiplying CMOS D/A converters. In the standard hookup, as shown in Figure 12, the AD586 is paired with the AD7545 12-bit multiplying DAC and the AD711 high-speed BiFET Op Amp. The amplifier DAC configuration produces a unipolar 0 to −5V output range. Bipolar output applications and other operating details can be found on the individual product data sheets.

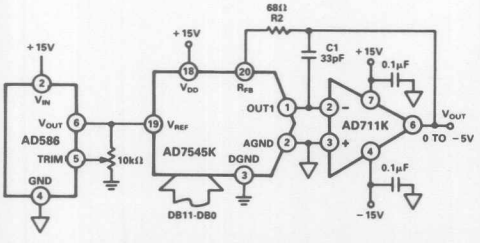


Figure 12. Low-Power 12-Bit CMOS DAC Application

The AD586 can also be used as a precision reference for multiple DACs. Figure 13 shows the AD586, the AD7628 dual DAC and the AD712 dual op amp hooked up for single supply operation to produce 0 to −5V outputs. Because both DACs are on the same die and share a common reference and output op amps, the DAC outputs will exhibit similar gain TCs.

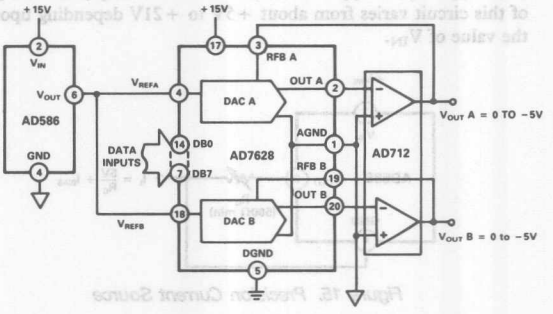


Figure 13. AD586 as a 5V Reference for a CMOS Dual DAC

STACKED PRECISION REFERENCES FOR MULTIPLE VOLTAGES

Often, a design requires several reference voltages. Three AD586s can be stacked, as shown in Figure 14, to produce +5.000V, +10.000V, and +15.000V outputs. This scheme can be extended to any number of AD586s as long as the maximum load current is not exceeded. This design provides the additional advantage of improved line regulation on the +5.0V output. Changes in V_{IN} of +18V to +50V produces an output change that is below the noise level of the references.

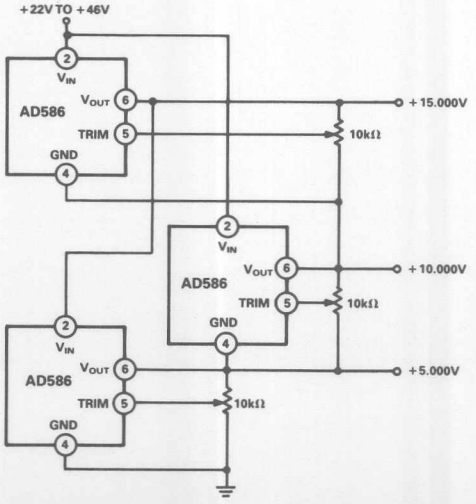


Figure 14. Multiple AD586s Stacked for Precision 5V, 10V and 15V Outputs

PRECISION CURRENT SOURCE

The design of the AD586 allows it to be easily configured as a current source. By choosing the control resistor R_C in Figure 15, you can vary the load current from the quiescent current (2mA typically) to approximately 10mA. The compliance voltage of this circuit varies from about +5V to +21V depending upon the value of V_{IN}.

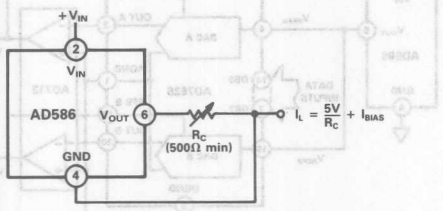


Figure 15. Precision Current Source

PRECISION HIGH CURRENT SUPPLY

For higher currents, the AD586 can easily be connected to a power PNP or power Darlington PNP device. The circuit in Figure 16 can deliver up to 4 amps to the load. The 0.1μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high-frequency supply rejection results can be obtained by removing the capacitor.

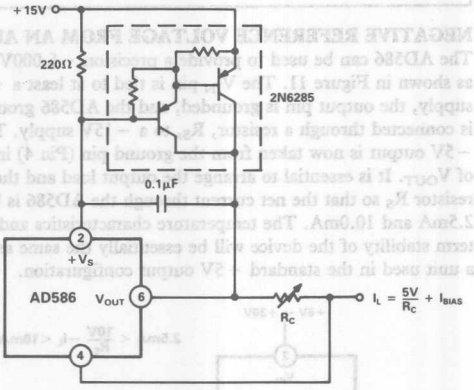


Figure 16a. Precision High-Current Current Source

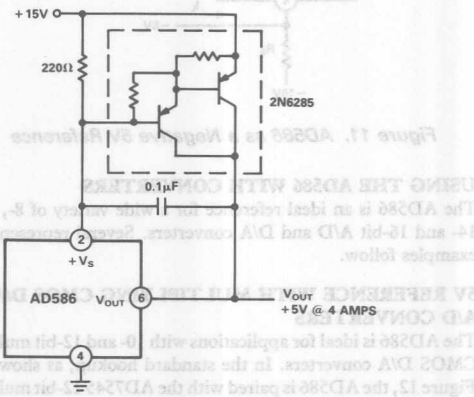


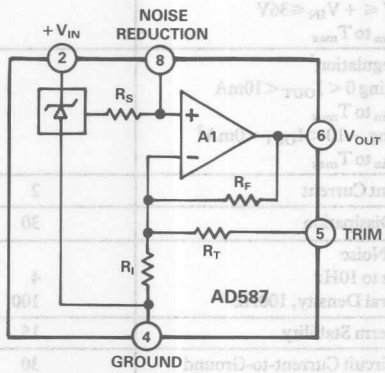
Figure 16b. Precision High-Current Voltage Source

AD587

FEATURES

- Laser Trimmed to High Accuracy:
  10.000V ±5mV (L and U Grades)
- Trimmed Temperature Coefficient:
  5ppm/°C max, (L and U Grades)
- Noise Reduction Capability
- Low Quiescent Current: 4mA max
- Output Trim Capability
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



NOTE: PINS 1, 3 & 7 ARE INTERNAL TEST POINTS.
NO CONNECTIONS TO THESE POINTS.

PRODUCT DESCRIPTION

The AD587 represents a major advance in the state-of-the-art in monolithic voltage references. Using a proprietary ion-implanted buried Zener diode and laser wafer trimming of high stability thin-film resistors, the AD587 provides outstanding performance at low cost.

The AD587 offers much higher performance than most other 10V references. Because the AD587 uses an industry standard pinout, many systems can be upgraded instantly with the AD587. The buried Zener approach to reference design provides lower noise and drift than band-gap voltage references. The AD587 offers a noise reduction pin which can be used to further reduce the noise level generated by the buried Zener.

The AD587 is recommended for use as a reference for 8-, 10-, 12-, 14- or 16-bit D/A converters which require an external precision reference. The device is also ideal for successive approximation or integrating A/D converters with up to 14 bits of accuracy and, in general, can offer better performance than the standard on-chip references.

The AD587J, K and L are specified for operation from 0 to +70°C, and the AD587S, T and U are specified for −55°C to +125°C operation. All grades are available in 8-pin cerdip. The J and K versions are also available in an 8-pin Small Outline IC (SOIC) package for surface mount applications, while the J, K and L grades also come in an 8-pin plastic package.

PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficients results in very low errors over temperature without the use of external components. The AD587L has a maximum deviation from 10.000V of ±8.5mV between 0 and +70°C, and the AD587U guarantees ±14mV maximum total error between −55°C and +125°C.
2. For applications requiring higher precision, an optional fine-trim connection is provided.
3. Any system using an industry standard pinout 10 volt reference can be upgraded instantly with the AD587.
4. Output noise of the AD587 is very low, typically 4μV p-p. A noise reduction pin is provided for additional noise filtering using an external capacitor.
5. The AD587 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD587/883B data sheet for detailed specifications.

Output Voltage	9.990		10.010	9.995		10.005	9.995		10.005	V
Output Voltage Drift[1]										
0 to +70°C			20			10			5	ppm/°C
−55°C to +125°C			20			10			5	
Gain Adjustment	+3			+3			+3			%
	−1			−1			−1			
Line Regulation[1]										
13.5V ≤ $+V_{IN}$ ≤36V										
T_{min} to T_{max}			100			100			100	± μV/V
Load Regulation[1]										
Sourcing 0 < I_{OUT} <10mA										
T_{min} to T_{max}			100			100			100	± μV/mA
Sinking −10 < I_{OUT} <0mA[2]										
T_{min} to T_{max}			100			100			100	
Quiescent Current		2	4		2	4		2	4	mA
Power Dissipation		30			30			30		mW
Output Noise										
0.1Hz to 10Hz		4			4			4		μV p-p
Spectral Density, 100Hz		100			100			100		$nV/\sqrt{Hz}$
Long-Term Stability		15			15			15		± ppm/1000Hr
Short-Circuit Current-to-Ground		30	50		30	50		30	50	mA
Short-Circuit Current-to-V_{IN}		30	50		30	50		30	50	mA
Temperature Range										
Specified Performance (J, K, L)	0		+70	0		+70	0		+70	°C
Operating Performance (J, K, L)[3]	−40		+85	−40		+85	−40		+85	
Specified Performance (S, T, U)	−55		+125	−55		+125	−55		+125	
Operating Performance (S, T, U)[3]	−55		+125	−55		+125	−55		+125	

NOTES
[1]Spec is guaranteed for all packages and grades. Cerdip packaged parts are 100% production tested.
[2]Load Regulation (Sinking) specification for SOIC (R) package is ± 200μV/mA.
[3]The operating temperature ranged is defined as the temperatures extremes at which the device will still function. Parts may deviate from their specified performance outside their specified temperature range.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Result from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ORDERING GUIDE

Model[1]	Initial Error mV	Temp. Coefficient ppm/°C	Temp. Range °C	Package Options[2]
AD587JQ	10	20	0 to +70	Q-8
AD587JR	10	20	0 to +70	R-8
AD587JN	10	20	0 to +70	N-8
AD587KQ	5	10	0 to +70	Q-8
AD587KR	5	10	0 to +70	R-8
AD587KN	5	10	0 to +70	N-8
AD587LQ	5	5	0 to +70	Q-8
AD587LN	5	5	0 to +70	N-8
AD587SQ	10	20	−55 to +125	Q-8
AD587TQ	10	10	−55 to +125	Q-8
AD587UQ	5	5	−55 to +125	Q-8
AD587JCHIPS	10	20	0 to +70	–

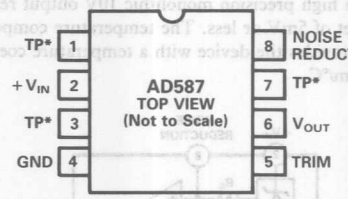
NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD587/883B data sheet.
[2]N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS*

V_{IN} to Ground 36V
Power Dissipation (25°C) 500mW
Storage Temperature . . . . . −65°C to +150°C
Lead Temp (Soldering, 10sec) . . . . . 300°C
Package Thermal Resistance
θ_{JC} . . . . . 22°C/W
θ_{JA} . . . . . 110°C/W
Output Protection: Output safe for indefinite short to ground and momentary short to V_{IN}.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM



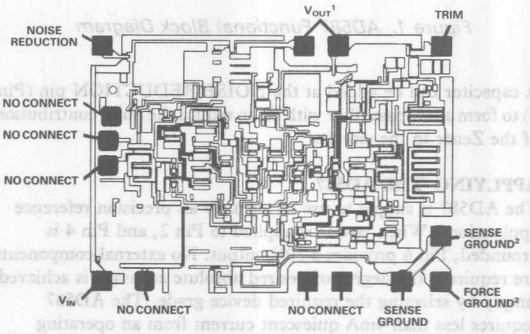
*TP DENOTES FACTORY TEST POINT. NO CONNECTIONS SHOULD BE MADE TO THESE PINS.

DIE SPECIFICATIONS

The following specifications are tested at the die level for AD587JCHIPS. These die are probed at 25°C only. ($T_A = +25°$, $V_{IN} = +15V$ unless otherwise specified)

Parameter	AD587JCHIPS Min	Typ	Max	Units
Output Voltage	9.990		10.010	V
Gain Adjustment	−1		3	%
Line Regulation 13.5V < + V_{IN} < 36V			100	± μV/V
Load Regulation Sourcing $0 < I_{OUT} < 10mA$ Sinking $-10 < I_{OUT} < 0mA$			100 100	μV/mA μV/mA
Quiescent Current		2	4	mA
Short-Circuit Current-to-Ground			50	mA
Short-Circuit Current-to-V_{OUT}			50	mA

DIE LAYOUT



Die Size: 0.081 × 0.060 inches

NOTES
[1]Both V_{OUT} pads should be connected to the output.
[2]Sense and force grounds must be tied together.

Die Thickness: The standard thickness of Analog Devices Bipolar dice is 24 mils ± 2 mils.

Die Dimensions: The dimensions given have a tolerance of ± 2 mils.

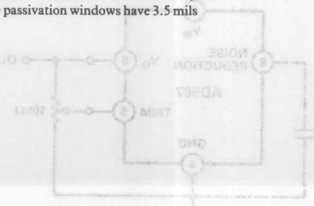
Backing: The standard backside surface is silicon (not plated). Analog Devices does not recommend gold-backed dice for most applications.

Edges: A diamond saw is used to separate wafers into dice thus providing perpendicular edges half-way through the die. In contrast to scribed dice, this technique provides a more uniform die shape and size. The perpendicular edges facilitate handling (such as tweezer pick-up) while the uniform shape and size simplifies substrate design and die attach.

Top Surface: The standard top surface of the die is covered by a layer of glassivation. All areas are covered except bonding pads and scribe lines.

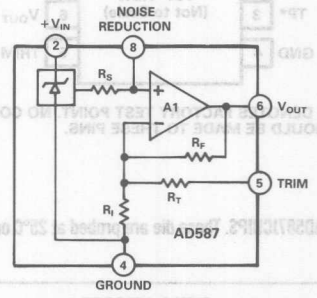
Surface Metalization: The metalization to Analog Devices bipolar dice is aluminum. Minimum thickness is 10,000Å.

Bonding Pads: All bonding pads have a minimum size of 4 mils by 4 mils. The passivation windows have 3.5 mils by 3.5 mils minimum.



THEORY OF OPERATION

The AD587 consists of a proprietary buried Zener diode reference, an amplifier to buffer the output and several high stability thin-film resistors as shown in the block diagram in Figure 1. This design results in a high precision monolithic 10V output reference with initial offset of 5mV or less. The temperature compensation circuitry provides the device with a temperature coefficient of under 5ppm/°C.



NOTE: PINS 1, 3 & 7 ARE INTERNAL TEST POINTS. NO CONNECTIONS TO THESE POINTS.

Figure 1. AD587 Functional Block Diagram

A capacitor can be added at the NOISE REDUCTION pin (Pin 8) to form a low pass filter with R_S to reduce the noise contribution of the Zener to the circuit.

APPLYING THE AD587

The AD587 is simple to use in virtually all precision reference applications. When power is applied to Pin 2, and Pin 4 is grounded, Pin 6 provides a 10V output. No external components are required; the degree of desired absolute accuracy is achieved simply by selecting the required device grade. The AD587 requires less than 4mA quiescent current from an operating supply of +15V.

Fine trimming may be desired to set the output level to exactly 10.000V (calibrated to a main system reference). System calibration may also require a reference voltage that is slightly different from 10.000V, for example, 10.24V for binary applications. In either case, the optional trim circuit shown in Figure 2 can offset the output by as much as 300mV, if desired, with minimal effect on other device characteristics.

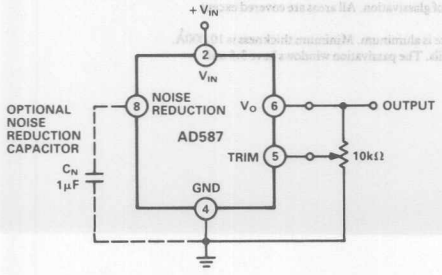


Figure 2. Optional Fine Trim Configuration

NOISE PERFORMANCE AND REDUCTION

The noise generated by the AD587 is typically less than 4μV p-p over the 0.1Hz to 10Hz band. Noise in a 1MHz bandwidth is approximately 200μV p-p. The dominant source of this noise is the buried Zener which contributes approximately 100nV/$\sqrt{\text{Hz}}$. In comparison, the op amp's contribution is negligible. Figure 3 shows the 0.1Hz to 10Hz noise of a typical AD587. The noise measurement is made with a bandpass filter made of a 1-pole high-pass filter with a corner frequency at 0.1Hz and a 2-pole low-pass filter with a corner frequency at 12.6Hz to create a filter with a 9.922Hz bandwidth.

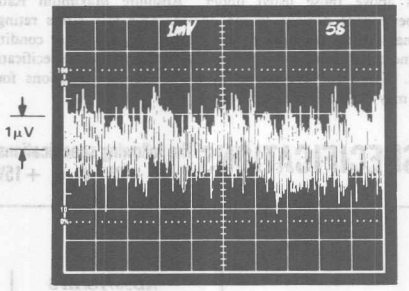


Figure 3. 0.1Hz to 10Hz Noise

If further noise reduction is desired, an external capacitor may be added between the NOISE REDUCTION pin and ground as shown in Figure 2. This capacitor, combined with the 4kΩ R_S and the Zener resistances, form a low-pass filter on the output of the Zener cell. A 1μF capacitor will have a 3dB point at 40Hz, and it will reduce the high-frequency (to 1MHz) noise to about 160μV p-p. Figure 4 shows the 1MHz noise of a typical AD587 both with and without a 1μF capacitor.

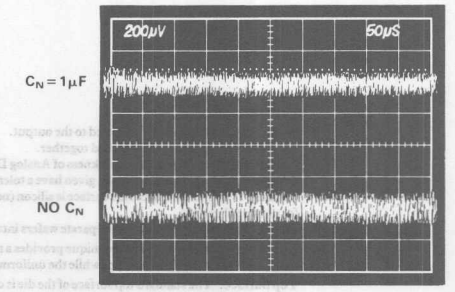
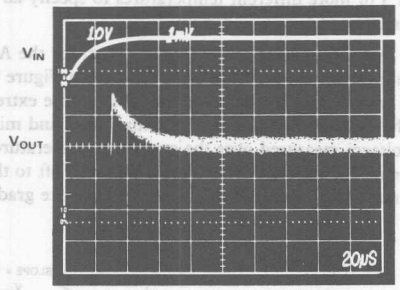


Figure 4. Effect of 1μF Noise Reduction Capacitor on Broadband Noise

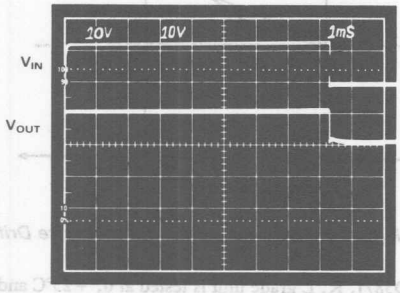
TURN-ON TIME

Upon application of power (cold start), the time required for the output voltage to reach its final value within a specified error band is defined as the turn-on settling time. Two components normally associated with this are: the time for the active circuits to settle, and the time for the thermal gradients on the chip to stabilize. Figure 5 shows the turn-on characteristics of the AD587. It shows the settling to be about 60μs to 0.01%. Note the absence of any thermal tails when the horizontal scale is expanded to 1ms/cm in Figure 5b.

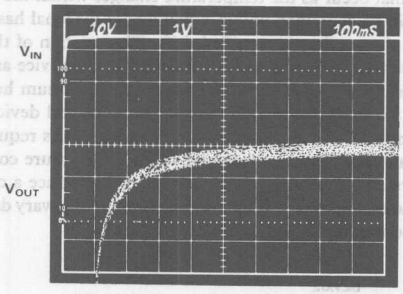
Output turn-on time is modified when an external noise reduction capacitor is used. When present, this capacitor acts as an additional load to the internal Zener diode's current source, resulting in a somewhat longer turn-on time. In the case of a 1μF capacitor, the initial turn-on time is approximately 400ms to 0.01% (see Figure 5c).



a. Electrical Turn-On



b. Extended Time Scale



c. Turn-On with 1μF C_N

Figure 5. Turn-On Characteristics

DYNAMIC PERFORMANCE

The output buffer amplifier is designed to provide the AD587 with static and dynamic load regulation superior to less complete references.

Many A/D and D/A converters present transient current loads to the reference, and poor reference response can degrade the converter's performance.

Figure 6 displays the characteristics of the AD587 output amplifier driving a 0 to 10mA load.

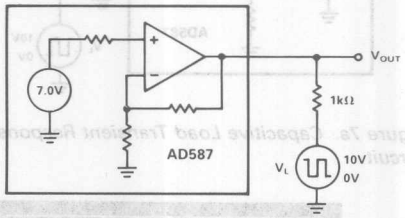


Figure 6a. Transient Load Test Circuit

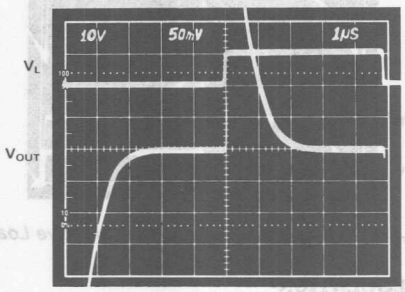


Figure 6b. Large-Scale Transient Response

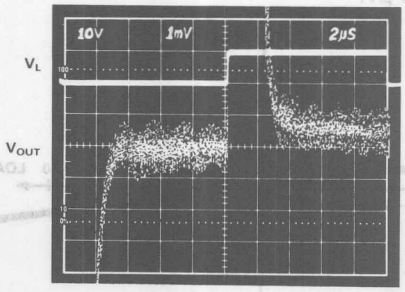


Figure 6c. Fine Scale Settling for Transient Load

6

capacitive in nature, or the load may be connected to the AD587 by a long capacitive cable.

Figure 7 displays the output amplifier characteristics driving a 1000pF, 0 to 10mA load.

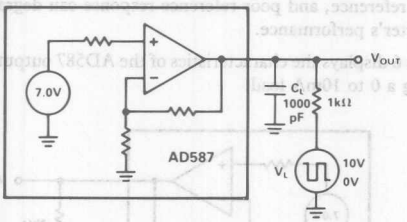


Figure 7a. Capacitive Load Transient Response Test Circuit

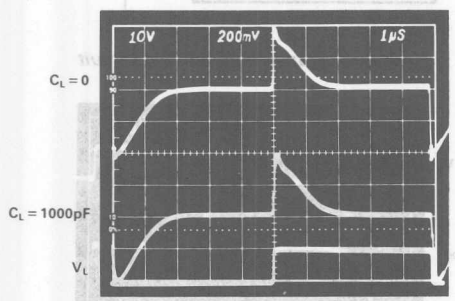


Figure 7b. Output Response with Capacitive Load

LOAD REGULATION

The AD587 has excellent load regulation characteristics. Figure 8 shows that varying the load several mA changes the output by only a few μV.

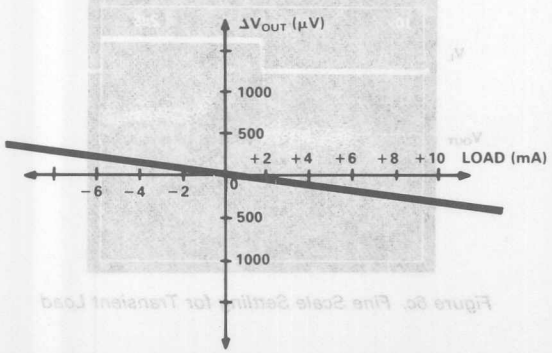


Figure 8. Typical Load Regulation Characteristics

TEMPERATURE PERFORMANCE

The AD587 is designed for precision reference applications where temperature performance is critical. Extensive temperature testing ensures that the device's high level of performance is maintained over the operating temperature range.

reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centrigrade; i.e., ppm/°C. However, because of nonlinearities in temperature characteristics which originated in standard Zener references (such as "S" type characteristics), most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves the measurement of the output at 3 or more different temperatures to specify an output voltage error band.

Figure 9 shows the typical output voltage drift for the AD587L and illustrates the test methodology. The box in Figure 9 is bounded on the sides by the operating temperature extremes, and on the top and the bottom by the maximum and minimum output voltages measured over the operating temperature range. The slope of the diagonal drawn from the lower left to the upper right corner of the box determines the performance grade of the device.

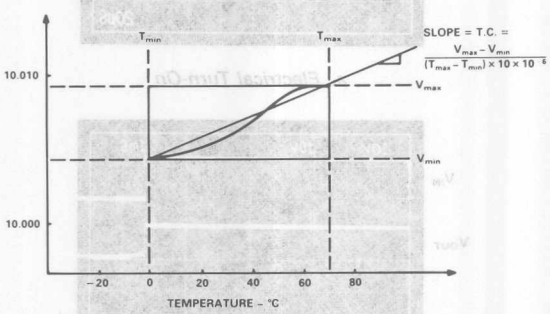


Figure 9. Typical AD587L Temperature Drift

Each AD587J, K, L grade unit is tested at 0, +25°C and +70°C. Each AD587S, T, and U grade unit is tested at −55°C, +25°C and +125°C. This approach ensures that the variations of output voltage that occur as the temperature changes within the specified range will be contained within a box whose diagonal has a slope equal to the maximum specified drift. The position of the box on the vertical scale will change from device to device as initial error and the shape of the curve vary. The maximum height of the box for the appropriate temperature range and device grade is shown in Figure 10. Duplication of these results requires a combination of high accuracy and stable temperature control in a test system. Evaluation of the AD587 will produce a curve similar to that in Figure 9, but output readings may vary depending on the test methods and equipment utilized.

DEVICE GRADE	MAXIMUM OUTPUT CHANGE – mV	
	0 TO +70°C	−55°C TO +125°C
AD587J	14.00	
AD587K	7.00	
AD587L	3.50	
AD587S		36.00
AD587T		18.00
AD587U		9.00

Figure 10. Maximum Output Change in mV

NEGATIVE REFERENCE VOLTAGE FROM AN AD587

The AD587 can be used to provide a precision −10.000V output as shown in Figure 11. The V_{IN} pin is tied to at least a +3.5V supply, the output pin is grounded, and the AD587 ground pin is connected through a resistor, R_S, to a −15V supply. The −10V output is now taken from the ground pin (Pin 4) instead of V_{OUT}. It is essential to arrange the output load and the supply resistor R_S so that the net current through the AD587 is between 2.5mA and 10.0mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard +10V output configuration.

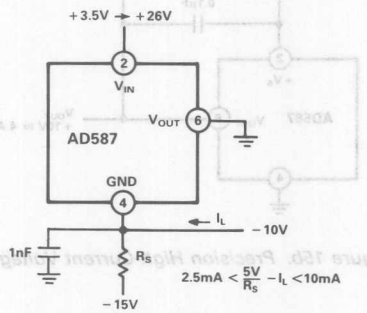


Figure 11. AD587 as a Negative 10V Reference

USING THE AD587 WITH CONVERTERS

The AD587 is an ideal reference for a wide variety of 8-, 12-, 14- and 16-bit A/D and D/A converters. Several representative examples follow.

10V REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD587 is ideal for applications with 10- and 12-bit multiplying CMOS D/A converters. In the standard hookup, as shown in Figure 12, the AD587 is paired with the AD7545 12-bit multiplying DAC and the AD711 high-speed BiFET Op Amp. The amplifier DAC configuration produces a unipolar 0 to −10V output range. Bipolar output applications and other operating details can be found on the individual product data sheets.

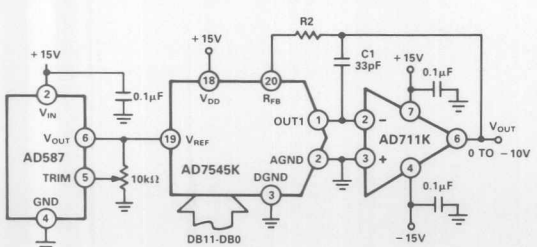


Figure 12. Low-Power 12-Bit CMOS DAC Application

The AD587 can also be used as a precision reference for multiple DACs. Figure 13 shows the AD587, the AD7628 dual DAC and the AD712 dual op amp hooked up for single supply operation to produce 0 to −10V outputs. Because both DACs are on the same die and share a common reference and output op amps; the DAC outputs will exhibit similar gain TCs.

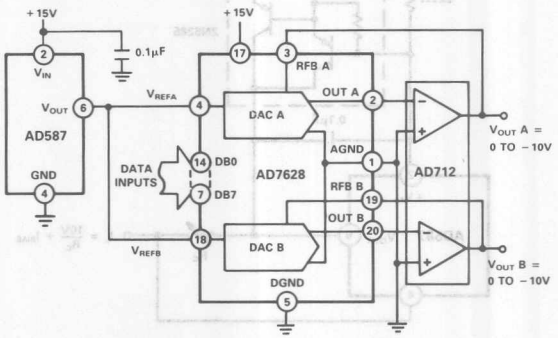


Figure 13. AD587 as a 10V Reference for a CMOS Dual DAC

PRECISION CURRENT SOURCE

The design of the AD587 allows it to be easily configured as a current source. By choosing the control resistor R_C in Figure 14, you can vary the load current from the quiescent current (2mA typically) to approximately 10mA.

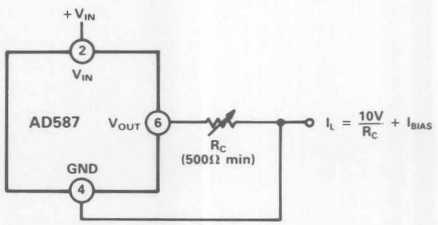


Figure 14. Precision Current Source

PRECISION HIGH CURRENT SUPPLY

For higher currents, the AD587 can easily be connected to a power PNP or power Darlington PNP device. The circuit in Figure 15 can deliver up to 4 amps to the load. The 0.1μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high-frequency supply rejection results can be obtained by removing the capacitor.

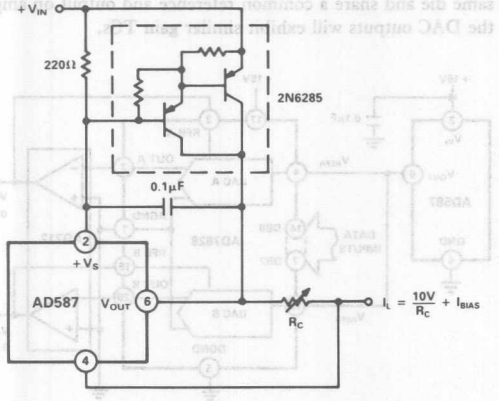


Figure 15a. Precision High-Current Current Source

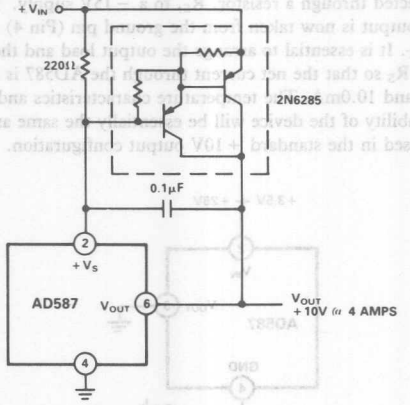


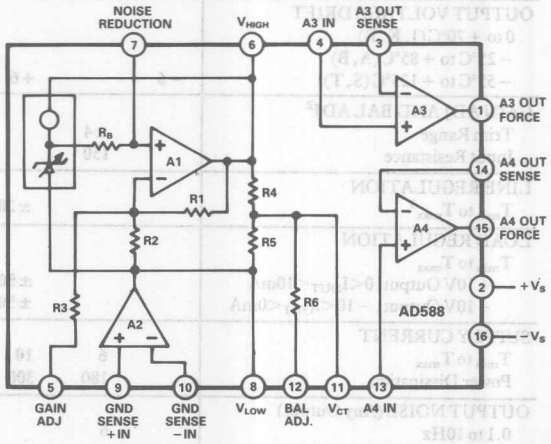
Figure 15b. Precision High-Current Voltage Source

High Precision Voltage Reference

AD588*

FEATURES
Low Drift – 1.5ppm/°C
Low Initial Error – 1mV
Pin-Programmable Output
+10V, +5V, ±5V Tracking, –5V, –10V
Flexible Output Force and Sense Terminals
High Impedance Ground Sense
Machine-Insertable DIP Packaging
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAMS



PRODUCT DESCRIPTION

The AD588 represents a major advance in the state-of-the-art in monolithic voltage references. Low initial error and low temperature drift give the AD588 absolute accuracy performance previously not available in monolithic form. The AD588 uses a proprietary ion-implanted buried Zener diode, and laser-wafer-drift-trimming of high stability thin-film resistors to provide outstanding performance at low cost.

The AD588 includes the basic reference cell and three additional amplifiers which provide pin-programmable output ranges. The amplifiers are laser-trimmed for low offset and low drift to maintain the accuracy of the reference. The amplifiers are configured to allow Kelvin connections to the load and/or boosters for driving long lines or high-current loads, delivering the full accuracy of the AD588 where it is required in the application circuit.

The low initial error allows the AD588 to be used as a system reference in precision measurement applications requiring 12-bit absolute accuracy. In such systems, the AD588 can provide a known voltage for system calibration in software and the low drift allows compensation for the drift of other components in a system. Manual system calibration and the cost of periodic recalibration can therefore be eliminated. Furthermore, the mechanical instability of a trimming potentiometer and the potential for improper calibration can be eliminated by using the AD588 in conjunction autocalibration software.

The AD588 is available in seven versions. The AD588 JQ and KQ grades are packaged in a 16-pin cerdip and are specified for 0 to +70°C operation. AD588AD and BD grades are packaged in a 16-pin side-brazed ceramic DIP and are specified for the –25°C to +85°C industrial temperature range. The ceramic AD588SD and TD grades are specified for the full military/aerospace temperature range. For military surface mount applications. the AD588SE and TE grades will also be available in 20-pin LCC packages.

*Covered by Patent Number 4,644,253

PRODUCT HIGHLIGHTS

1. The AD588 offers 12-bit absolute accuracy without any user adjustments. Optional fine-trim connections are provided for applications requiring higher precision. The fine-trimming does not alter the operating conditions of the Zener or the buffer amplifiers and thus does not increase the temperature drift.
2. Output noise of the AD588 is very low – typically 6μV p-p. A pin is provided for additional noise filtering using an external capacitor.
3. A precision ±5V tracking mode with Kelvin output connections is available with no external components. Tracking error is less than one millivolt and a fine-trim is available for applications requiring exact symmetry between the +5V and –5V outputs.
4. Pin strapping capability allows configuration of a wide variety of outputs: ±5V, +5V & +10V, –5V & –10V dual outputs or +5V, –5V, +10V, –10V single outputs.
5. Extensive temperature testing at –55°C, –25°C, 0, +25°C, +50°C, +70°C, +85°C and +125°C ensures that the specified temperature coefficient is truly representative of device performance.

6

AD588—SPECIFICATIONS (typical @ +25°C, +10V output, V_S = ±15V unless otherwise noted[1])

	AD588SD			AD588JQ/AD/TD			AD588KQ/BD			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
OUTPUT VOLTAGE ERROR										
+10V, −10V Outputs	−5		+5	−3		+3	−1		+1	mV
+5V, −5V Outputs	−5		+5	−3		+3	−1		+1	mV
±5V TRACKING MODE										
Symmetry Error	−1.5		+1.5	−1.5		+1.5	−0.75		+0.75	mV
OUTPUT VOLTAGE DRIFT										
0 to +70°C (J, K, B)				−3	±2	+3	−1.5		+1.5	ppm/°C
−25°C to +85°C (A, B)				−3		+3	−3		+3	ppm/°C
−55°C to +125°C (S, T)	−6		+6	−4		+4				ppm/°C
GAIN ADJ AND BAL ADJ[2]										
Trim Range		±4			±4			±4		mV
Input Resistance		150			150			150		kΩ
LINE REGULATION										
T_{min} to T_{max}[3]			±200			±200			±200	μV/V
LOAD REGULATION										
T_{min} to T_{max}										
+10V Output, 0<I_{OUT}<10mA			±50			±50			±50	μV/mA
−10V Output, −10<I_{OUT}<0mA			±50			±50			±50	μV/mA
SUPPLY CURRENT										
T_{min} to T_{max}		6	10		6	10		6	10	mA
Power Dissipation		180	300		180	300		180	300	mW
OUTPUT NOISE (Any Output)										
0.1 to 10Hz		6			6			6		μV p-p
Spectral Density, 100Hz		100			100			100		nV/√Hz
LONG-TERM STABILITY (@ +25°C)		15			15			15		ppm/1000hr
BUFFER AMPLIFIERS										
Offset Voltage		100			100			100		μV
Offset Voltage Drift		1			1			1		μV/°C
Bias Current		20			20			20		nA
Open Loop Gain		110			110			110		dB
Output Current A3, A4	−10		+10	−10		+10	−10		+10	mA
Common Mode Rejection (A3, A4)										
V_{CM} = 1V p-p		100			100			100		dB
Short-Circuit Current		50			50			50		mA
TEMPERATURE RANGE										
Specified Performance										
J, K Grades				0		+70	0		+70	°C
A, B Grades				−25		+85	−25		+85	°C
S, T Grades	−55		+125	−55		+125				°C

NOTES

[1]Output Configuration
+10V Figure 2a
−10V Figure 2c
+5V, −5V, ±5V Figure 2b

Specifications tested using +10V configuration unless otherwise indicated.

[2]Gain and balance adjustments guaranteed capable of trimming output voltage error and symmetry error to zero.

[3]Test Conditions:
+10V Output $-V_S = -15V, 13.5V \le +V_S \le 18V$
−10V Output $-18V \le -V_S \le -13.5V, +V_S = 15V$
±5V Output $+V_S = +18V, -V_S = -18V$
$+V_S = +10.8V, -V_S = -10.8V$

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ORDERING GUIDE

Part Number[1]	Initial Error	Temperature Coefficient	Temperature Range °C	Package Option[2]
AD588AD	3mV	3ppm/°C	−25 to +85	Ceramic (D-16)
AD588BD	1mV	1.5ppm/°C	−25 to +85[3]	Ceramic (D-16)
AD588SD	5mV	6ppm/°C	−55 to +125	Ceramic (D-16)
AD588TD	3mV	4ppm/°C	−55 to +125	Ceramic (D-16)
AD588JQ	3mV	3ppm/°C	0 to +70	Cerdip (Q-16)
AD588KQ	1mV	1.5ppm/°C	0 to +70	Cerdip (Q-16)

NOTES

[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD588/883B data sheet.

[2]For outline information see Package Information section.

[3]Temperature coefficient specified from 0 to +70°C.

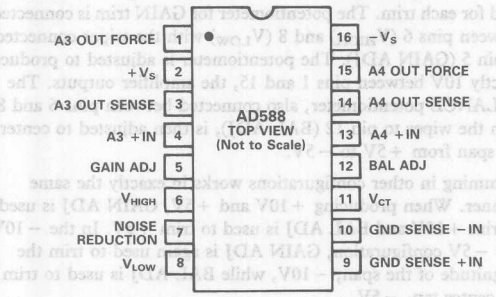
ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to $-V_S$ 36V
Power Dissipation (+25°C)
D Package 600mW
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . 300°C
Package Thermal Resistance
D (θ_{JA}/θ_{JC}) . . . . . 90/25°C/W
Output Protection: All outputs safe if shorted to ground

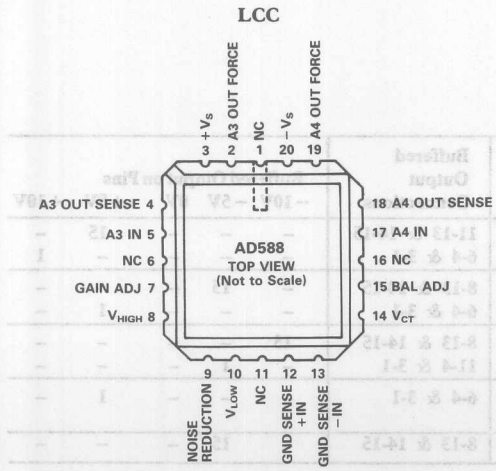
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS

DIP



LCC



NC = NO CONNECT

THEORY OF OPERATION

The AD588 consists of a buried Zener diode reference, amplifiers used to provide pin programmable output ranges, and associated thin-film resistors as shown in the block diagram of Figure 1. The temperature compensation circuitry provides the device with a temperature coefficient of 1.5ppm/°C or less.

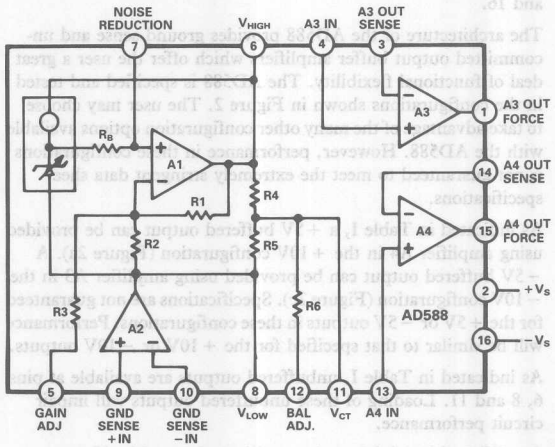


Figure 1. AD588 Functional Block Diagram

Amplifier A1 performs several functions. A1 primarily acts to amplify the Zener voltage from 6.5V to the required 10V output. In addition, A1 also provides for external adjustment of the 10V output through pin 5, the GAIN ADJUST. Using the bias compensation resistor between the Zener output and the non-inverting input to A1, a capacitor can be added at the NOISE REDUCTION pin (pin 7) to form a low pass filter and reduce the noise contribution of the Zener to the circuit. Two matched 10kΩ nominal thin film resistors (R4 & R5) divide the 10V output in half. Pin V_{CT} (pin 11) provides access to the center of the voltage span and pin 12 (BALANCE ADJUST) can be used for fine adjustment of this division.

Ground sensing for the circuit is provided by amplifier A2. The noninverting input (pin 9) senses the system ground which will be transferred to the point on the circuit where the inverting input (pin 10) is connected. This may be pin 6, 8 or 11. The output of A2 drives pin 8 to the appropriate voltage. Thus, if pin 10 is connected to pin 8, the V_{LOW} pin will be the same voltage as the system ground. Alternatively, if pin 10 is connected to the V_{CT} pin, it will be ground and pin 6 and pin 8 will be +5V and −5V respectively.

Amplifiers A3 and A4 are internally compensated and are used to buffer the voltages at pins 6, 8 and 11 as well as to provide a full Kelvin output. Thus, the AD588 has a full Kelvin capability by providing the means to sense a system ground and provide forced and sensed outputs referenced to that ground.

6

APPLYING THE AD588

The AD588 can be configured to provide +10V and −10V reference outputs as shown in Figures 2a and 2c respectively. It can also be used to provide +5V, −5V or a ±5V tracking reference as shown in Figure 2b. Table I details the appropriate pin connections for each output range. In each case, pin 9 is connected to system ground and power is applied to pins 2 and 16.

The architecture of the AD588 provides ground sense and uncommitted output buffer amplifiers which offer the user a great deal of functional flexibility. The AD588 is specified and tested in the configurations shown in Figure 2. The user may choose to take advantage of the many other configuration options available with the AD588. However, performance in these configurations is not guaranteed to meet the extremely stringent data sheet specifications.

As indicated in Table I, a +5V buffered output can be provided using amplifier A4 in the +10V configuration (Figure 2a). A −5V buffered output can be provided using amplifier A3 in the −10V configuration (Figure 2c). Specifications are not guaranteed for the +5V or −5V outputs in these configurations. Performance will be similar to that specified for the +10V or −10V outputs.

As indicated in Table I, unbuffered outputs are available at pins 6, 8 and 11. Loading of these unbuffered outputs will impair circuit performance.

Amplifiers A3 and A4 can be used interchangeably. However, the AD588 is tested (and the specifications are guaranteed) with the amplifiers connected as indicated in Figure 2 and Table I. When either A3 or A4 is unused, its output force and sense pins should be connected and the input tied to ground.

Two outputs of the same voltage may be obtained by connecting both A3 and A4 to the appropriate unbuffered output on pin 6, 8 or 11. Performance in these dual output configurations will typically meet data sheet specifications.

CALIBRATION

Generally, the AD588 will meet the requirements of a precision system without additional adjustment. Initial output voltage error of 1mV and output noise specs of 10μV p-p allow for accuracies of 12-16 bits. However, in applications where an even greater level of accuracy is required, additional calibration may be called for. Provision for trimming has been made through the use of the GAIN ADJUST and BALANCE ADJUST pins (pins 5 and 12 respectively).

The AD588 provides a precision 10V span with a center tap (V_{CT}) which is used with the buffer and ground sense amplifiers to achieve the voltage output configurations in Table I. GAIN ADJUST and BALANCE ADJUST can be used in any of these configurations to trim the magnitude of the span voltage and the position of the center tap within the span. The GAIN ADJUST should be performed first. Although the trims are not interactive within the device, the GAIN trim will move the BALANCE trim point as it changes the magnitude of the span.

Figure 2b. shows GAIN and BALANCE trims in a +5V and −5V tracking configuration. A 100kΩ 20-turn potentiometer is used for each trim. The potentiometer for GAIN trim is connected between pins 6 (V_{HIGH}) and 8 (V_{LOW}) with the wiper connected to pin 5 (GAIN ADJ). The potentiometer is adjusted to produce exactly 10V between pins 1 and 15, the amplifier outputs. The BALANCE potentiometer, also connected between pins 6 and 8 with the wiper to pin 12 (BAL ADJ), is then adjusted to center the span from +5V to −5V.

Trimming in other configurations works in exactly the same manner. When producing +10V and +5V, GAIN ADJ is used to trim +10V and BAL ADJ is used to trim +5V. In the −10V and −5V configuration, GAIN ADJ is again used to trim the magnitude of the span, −10V, while BAL ADJ is used to trim the center tap, −5V.

Range	Connect Pin 10 to Pin:	Unbuffered[1] Output on Pins −10V	−5V	0V	+5V	+10V	Buffered Output Connections	Buffered Output on Pins −10V	−5V	0V	+5V	+10V
+10V	8	–	–	8	11	6	11-13 & 14-15	–	–	–	15	–
							6-4 & 3-1	–	–	–	–	1
−5V or +5V	11	–	8	11	6	–	8-13 & 14-15	–	15	–	–	–
							6-4 & 3-1	–	–	–	1	–
−10V	6	8	11	6	–	–	8-13 & 14-15	15	–	–	–	–
							11-4 & 3-1	–	1	–	–	–
+5V	11	–	–	–	6	–	6-4 & 3-1	–	–	–	1	–
−5V		–	8	–	–	–	8-13 & 14-15	–	15	–	–	–

[1]"Unbuffered" outputs should not be loaded.

Table I. AD588 Connections

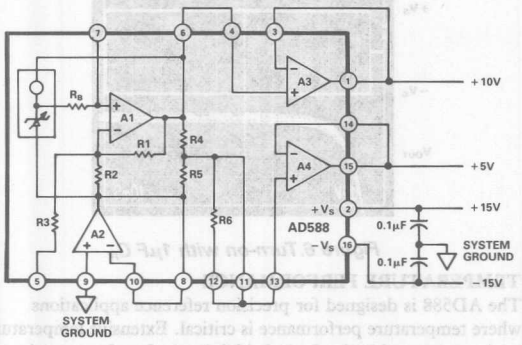


Figure 2a. +10V Output

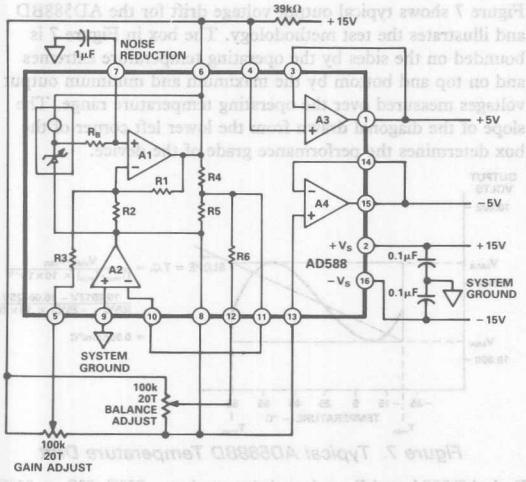


Figure 2b. +5V and –5V Outputs

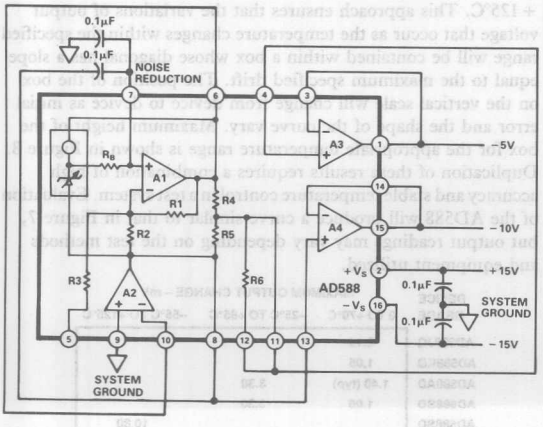


Figure 2c. –10V Output

In single output configurations, GAIN ADJ is used to trim outputs utilizing the full span (+10V or –10V) while BAL ADJ is used to trim outputs using half the span (+5V or –5V).

Input impedance on both the GAIN ADJUST and BALANCE ADJUST pins is approximately 150kΩ. The GAIN ADJUST trim network effectively attenuates the 10V across the trim potentiometer by a factor of about 1500 to provide a trim range of –3.5mV to +7.5mV with a resolution of approximately 550μV/turn (20 turn potentiometer). The BALANCE ADJUST trim network attenuates the trim voltage by a factor of about 1400, providing a trim range of ±4.5mV with resolution of 450μV/turn.

Trimming the AD588 introduces no additional errors over temperature so precision potentiometers are not required.

For single output voltage ranges, or in cases when BALANCE ADJUST is not required, pin 12 should be connected to pin 11. If GAIN ADJUST is not required, pin 5 should be left floating.

NOISE PERFORMANCE AND REDUCTION

The noise generated by the AD588 is typically less than 6μV p-p over the 0.1Hz to 10Hz band. Noise in a 1MHz bandwidth is approximately 600μV p-p. The dominant source of this noise is the buried Zener which contributes approximately 100nV/$\sqrt{\text{Hz}}$. In comparison, the op amp's contribution is negligible. Figure 3 shows the 0.1Hz to 10Hz noise of a typical AD588.

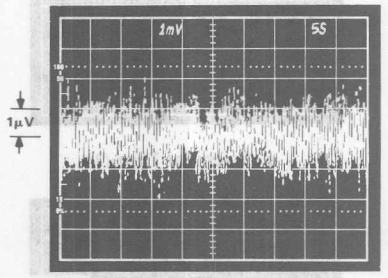


Figure 3. 0.1Hz to 10Hz Noise

If further noise reduction is desired, an optional capacitor may be added between the NOISE REDUCTION pin and ground as shown in Figure 2b. This will form a low pass filter with the 4kΩ R_B on the output of the Zener cell. A 1μF capacitor will have a 3dB point at 40Hz and will reduce the high frequency (to 1MHz) noise to about 200μV p-p. Figure 4 shows the 1MHz noise of a typical AD588 both with and without a 1μF capacitor.

Note that a second capacitor is needed in order to implement the NOISE REDUCTION feature when using the AD588 in the –10V mode (Figure 2c.). The NOISE REDUCTION capacitor is limited to 0.1μF maximum in this mode.

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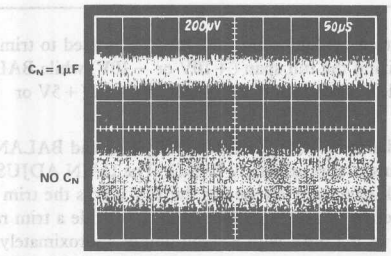
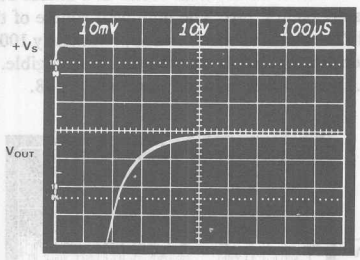


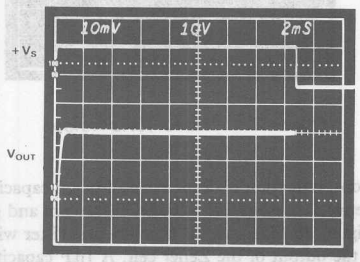
Figure 4. Effect of 1μF Noise Reduction Capacitor on Broadband Noise

TURN-ON TIME

Upon application of power (cold start), the time required for the output voltage to reach its final value within a specified error band is the turn-on settling time. Two components normally associated with this are: time for active circuits to settle and time for thermal gradients on the chip to stabilize. Figure 5 shows the turn-on characteristics of the AD588. It shows the settling to be about 600μs. Note the absence of any thermal tails when the horizontal scale is expanded to 2ms/cm in Figure 5b.



a. Electrical Turn-On



b. Extended Time Scale

Figure 5. Turn-On Characteristics

Output turn-on time is modified when an external noise reduction capacitor is used. When present, this capacitor presents an additional load to the internal Zener diode's current source, resulting in a somewhat longer turn-on time. In the case of a 1μF capacitor, the initial turn-on time is approximately 60ms (see Figure 6).

Note: If the NOISE REDUCTION feature is used in the ±5V configuration, a 39kΩ resistor between pins 6 and 2 is required for proper startup.

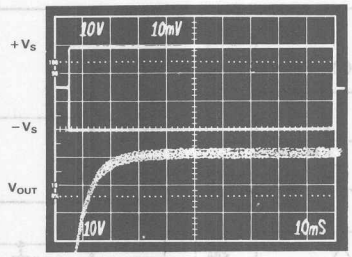


Figure 6. Turn-on with 1μF C_N

TEMPERATURE PERFORMANCE

The AD588 is designed for precision reference applications where temperature performance is critical. Extensive temperature testing ensures that the device's high level of performance is maintained over the operating temperature range.

Figure 7 shows typical output voltage drift for the AD588BD and illustrates the test methodology. The box in Figure 7 is bounded on the sides by the operating temperature extremes and on top and bottom by the maximum and minimum output voltages measured over the operating temperature range. The slope of the diagonal drawn from the lower left corner of the box determines the performance grade of the device.

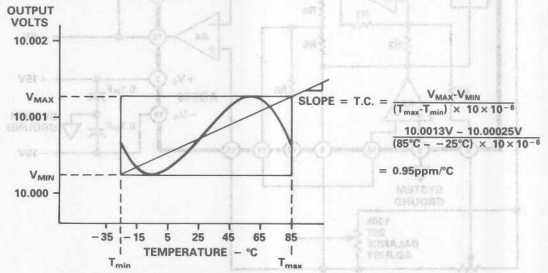


Figure 7. Typical AD588BD Temperature Drift

Each AD588A and B grade unit is tested at −25°C, 0°C, +25°C, +50°C, +70°C and +85°C. Each AD588S and T grade unit is tested at −55°C, −25°C, 0°C, +25°C, +50°C, +70°C and +125°C. This approach ensures that the variations of output voltage that occur as the temperature changes within the specified range will be contained within a box whose diagonal has a slope equal to the maximum specified drift. The position of the box on the vertical scale will change from device to device as initial error and the shape of the curve vary. Maximum height of the box for the appropriate temperature range is shown in Figure 8. Duplication of these results requires a combination of high accuracy and stable temperature control in a test system. Evaluation of the AD588 will produce a curve similar to that in Figure 7, but output readings may vary depending on the test methods and equipment utilized.

DEVICE GRADE	MAXIMUM OUTPUT CHANGE – mV		
	0 TO +70°C	−25°C TO +85°C	−55°C TO +125°C
AD588JQ	2.10		
AD588KQ	1.05		
AD588AD	1.40 (typ)	3.30	
AD588BD	1.05	3.30	
AD588SD			10.80
AD588TD			7.20

Figure 8. Maximum Output Change – mV

KELVIN CONNECTIONS

Force and sense connections, also referred to as Kelvin connections, offer a convenient method of eliminating the effects of voltage drops in circuit wires. As seen in Figure 9a, the load current and wire resistance produce an error ($V_{ERROR} = R \times I_L$) at the load. The Kelvin connection of Figure 9b overcomes the problem by including the wire resistance within the forcing loop of the amplifier and sensing the load voltage. The amplifier corrects for any errors in the load voltage. In the circuit shown, the output of the amplifier would actually be at 10 volts + V_{ERROR} and the voltage at the load would be the desired 10 volts.

The AD588 has three amplifiers which can be used to implement Kelvin connections. Amplifier A2 is dedicated to the ground force-sense function while uncommitted amplifiers A3 and A4 are free for other force-sense chores.

In some single-output applications, one amplifier may be unused.

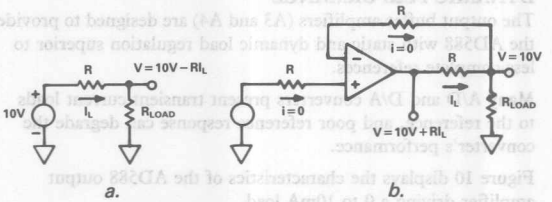
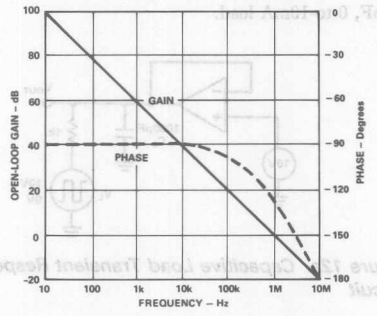


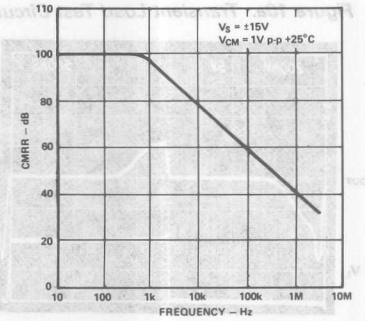
Figure 9. Advantage of Kelvin Connection

In such cases, the unused amplifier should be connected as a unity-gain follower (force + sense pin tied together) and the input should be connected to ground.

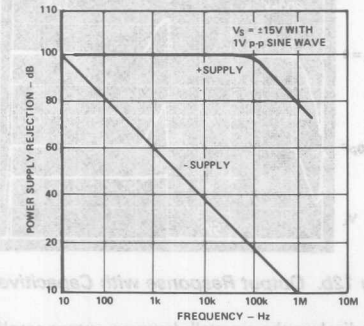
An unused amplifier section may be used for other circuit functions as well. The curves on this page show the typical performance of A3 and A4.



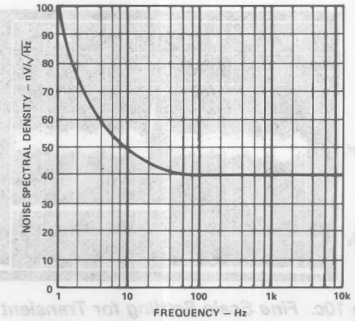
Open Loop Frequency Response (A3, A4)



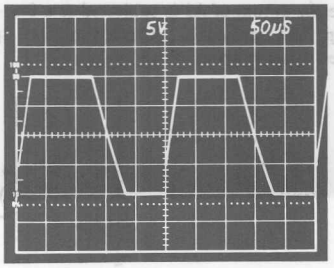
Common Mode Rejection vs. Frequency (A3, A4)



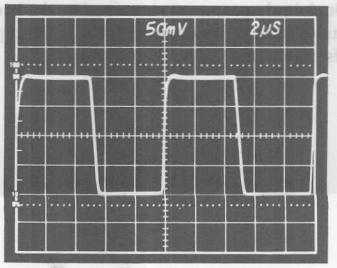
Power Supply Rejection vs. Frequency (A3, A4)



Input Noise Voltage Spectral Density



Unity Gain Follower Pulse Response (Large Signal)



Unity Gain Follower Pulse Response (Small Signal)

DYNAMIC PERFORMANCE

The output buffer amplifiers (A3 and A4) are designed to provide the AD588 with static and dynamic load regulation superior to less complete references.

Many A/D and D/A converters present transient current loads to the reference, and poor reference response can degrade the converter's performance.

Figure 10 displays the characteristics of the AD588 output amplifier driving a 0 to 10mA load.

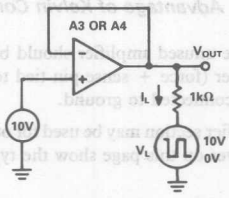


Figure 10a. Transient Load Test Circuit

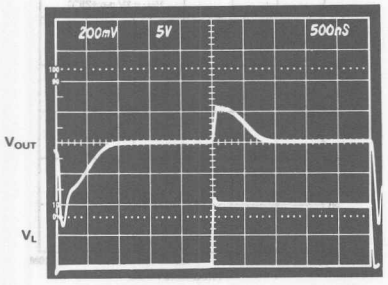


Figure 10b. Large-Scale Transient Response

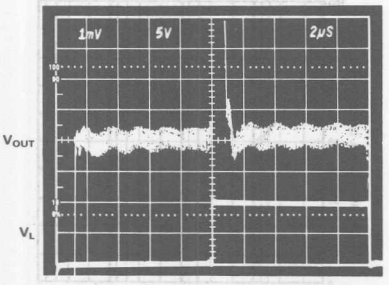


Figure 10c. Fine Scale Settling for Transient Load

Figure 11 displays the output amplifier characteristics driving a 5mA to 10mA load, a common situation found when the reference is shared among multiple converters or is used to provide a bipolar offset current.

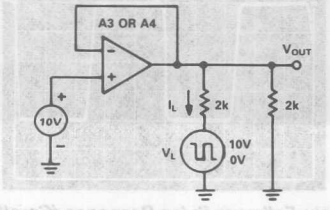


Figure 11a. Transient and Constant Load Test Circuit

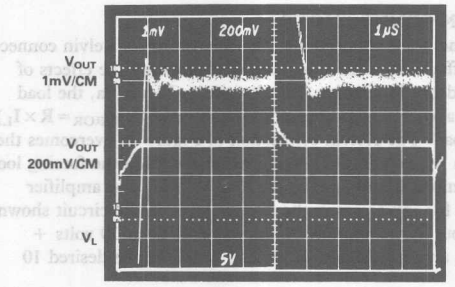


Figure 11b. Transient Response 5-10mA Load

In some applications, a varying load may be both resistive and capacitive in nature, or be connected to the AD588 by a long capacitive cable.

Figure 12 displays the output amplifier characteristics driving a 1,000pF, 0-to-10mA load.

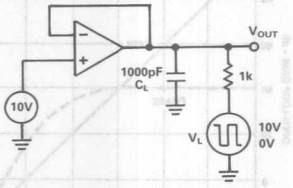


Figure 12a. Capacitive Load Transient Response Test Circuit

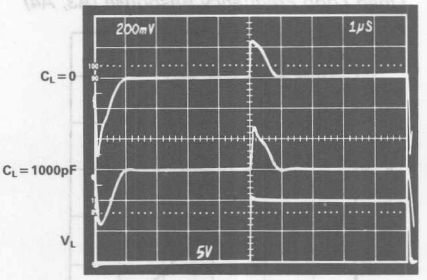


Figure 12b. Output Response with Capacitive Load

Figure 13 displays the crosstalk between output amplifiers. The top trace shows the output of A4, dc-coupled and offset by 10 volts, while the output of A3 is subjected to a 0-to-10mA load current step. The transient at A4 settles in about 1µs, and the load-induced offset is about 100µV.

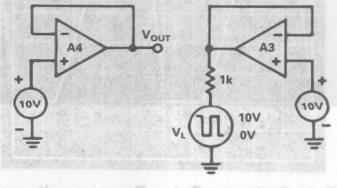


Figure 13a. Load Crosstalk Test Circuit

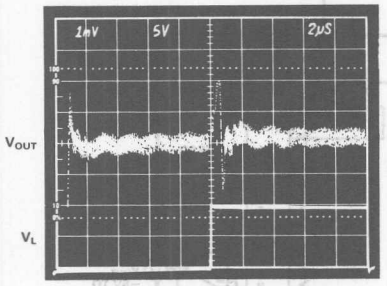


Figure 13b. Load Crosstalk

Attempts to drive a large capacitive load (in excess of 1,000pF) may result in ringing or oscillation, as shown in the step response photo (Figure 14a). This is due to the additional pole formed by the load capacitance and the output impedance of the amplifier, which consumes phase margin. The recommended method of driving capacitive loads of this magnitude is shown in Figure 14b. The 150Ω resistor isolates the capacitive load from the output stage, while the 10kΩ resistor provides a dc feedback path and preserves the output accuracy. The 1μF capacitor provides a high-frequency feedback loop. The performance of this circuit is shown in Figure 14c.

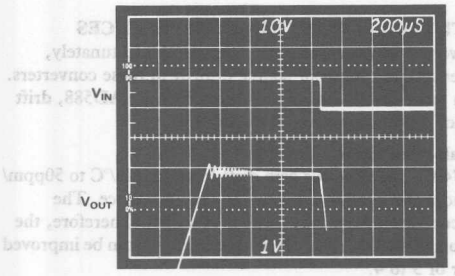


Figure 14a. Output Amplifier Step Response, $C_L = 1\mu F$

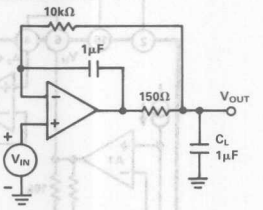


Figure 14b. Compensation for Capacitive Loads

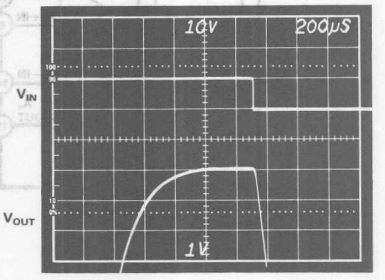


Figure 14c. Output Amplifier Step Response Using Figure 14b Compensation

6

USING THE AD588 WITH CONVERTERS

The AD588 is an ideal reference for a wide variety of A/D and D/A converters. Several representative examples follow.

14-Bit Digital-to-Analog Converter – AD7535

High resolution CMOS D/A converters require a reference voltage of high precision to maintain rated accuracy. The combination of the AD588 and AD7535 takes advantage of the initial accuracy, drift and full Kelvin output capability of the AD588 as well as the resolution, monotonicity and accuracy of the AD7535 to produce a subsystem with outstanding characteristics.

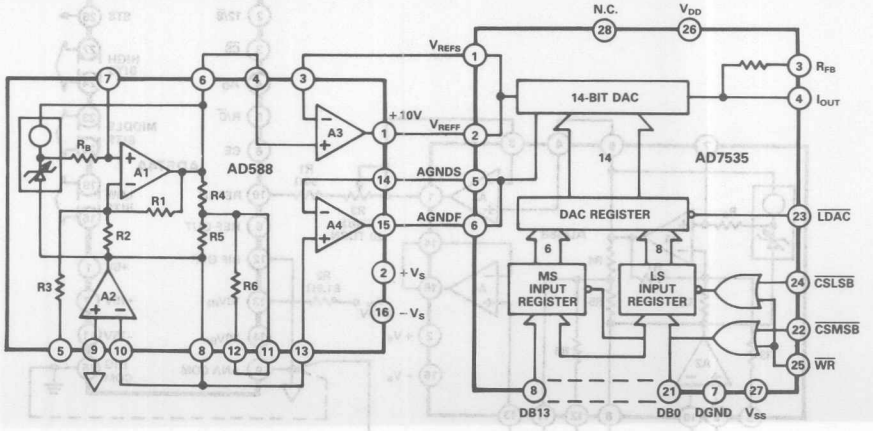


Figure 15. AD588/AD7535 Connections

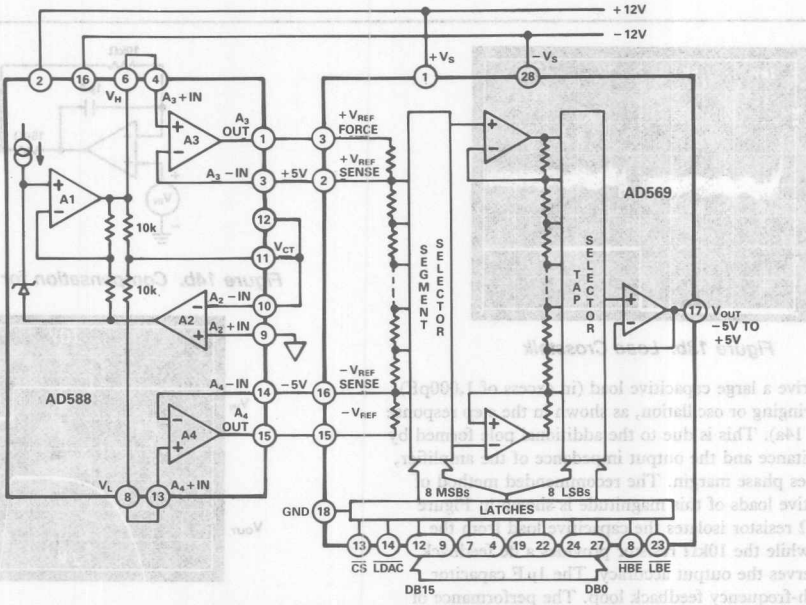


Figure 16. High-Accuracy ±5V Tracking Reference for AD569

16-Bit Digital-to-Analog Converter – AD569

Another application which fully utilizes the capabilities of the AD588 is supplying a reference for the AD569, as shown in Figure 16. Amplifier A2 senses system common and forces V_{CT} to assume this value, producing +5V and −5V at pins 6 and 8 respectively. Amplifiers A3 and A4 buffer these voltages out to the appropriate reference force-sense pins of the AD569. The full Kelvin scheme eliminates the effect of the circuit traces or wires and the wire bonds of the AD588 and AD569 themselves, which would otherwise degrade system performance.

SUBSTITUTING FOR INTERNAL REFERENCES

Many converters include built-in references. Unfortunately, such references are the major source of drift in these converters. By using a more stable external reference like the AD588, drift performance can be improved dramatically.

12-Bit Analog-to-Digital Converter – AD574A

The AD574A is specified for gain drift from 10ppm/°C to 50ppm/°C, (depending on grade) using the on-chip reference. The reference contributes typically 75% of this drift. Therefore, the total drift using an AD588 to supply the reference can be improved by a factor of 3 to 4.

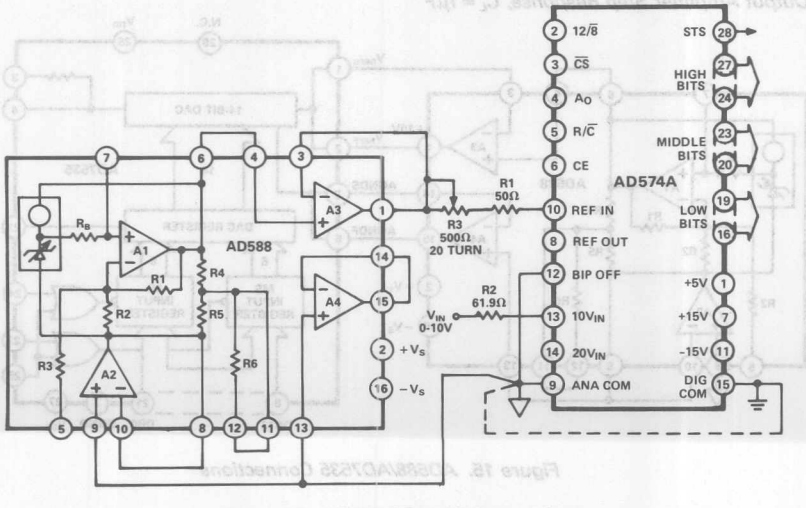


Figure 17. AD588/AD574A Connections

Using this combination may result in apparent increases in full-scale error due to the difference between the on-board reference by which the device is laser trimmed and the external reference with which the device is actually applied. The on-board reference is specified to be 10V ±100mV while the external reference is specified to be 10V ±1mV. This may result in up to 101mV of apparent full-scale error beyond the ±25mV specified AD574 gain error. Resistors R2 and R3 allow this error to be nulled. Their contribution to full-scale drift is negligible.

The high output drive capability allows the AD588 to drive up to 6 converters in a multi-converter system. All converters will have gain errors that track to better than ±5ppm/°C.

RTD EXCITATION

The Resistance Temperature Detector (RTD) is a circuit element whose resistance is characterized by a positive temperature coefficient. A measurement of resistance indicates the measured temperature. Unfortunately, the resistance of the wires leading to the RTD often adds error to this measurement. The 4-wire ohms measurement overcomes this problem. This method uses two wires to bring an excitation current to the RTD and two additional wires to tap off the resulting RTD voltage. If these additional two wires go to a high input impedance measurement circuit, the effect of their resistance is negligible. Therefore, they transmit the true RTD voltage.

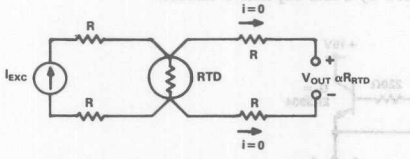


Figure 18. 4-Wire Ohms Measurement

A practical consideration when using the 4-wire ohms technique with an RTD is the self-heating effect that the excitation current has on the temperature of the RTD. The designer must choose the smallest practical excitation current that still gives the desired resolution. RTD manufactures usually specify the self-heating effect of each of their models or types of RTDs.

Figure 19 shows an AD588 providing the precision excitation current for a 100Ω RTD. The small excitation current of 1mA dissipates a mere 0.1mW of power in the RTD.

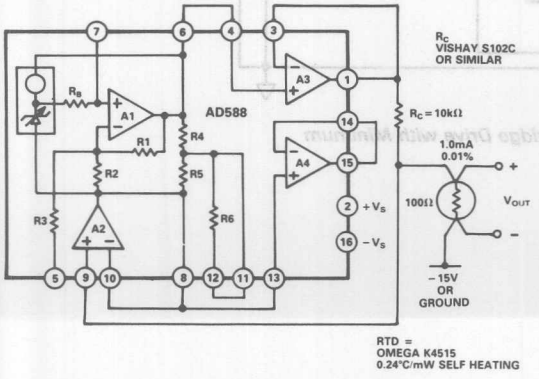


Figure 19. Precision Current Source for RTD

BOOSTED PRECISION CURRENT SOURCE

In the RTD current-source application the load current is limited to ±10mA by the output drive capability of amplifier A3. In the event that more drive current is needed, a series pass transistor can be inserted inside the feedback loop to provide higher current. Accuracy and drift performance are unaffected by the pass transistor.

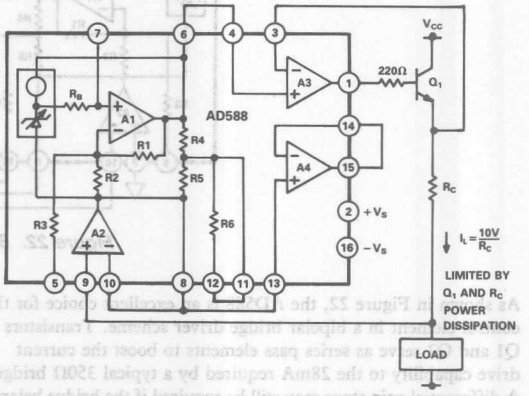
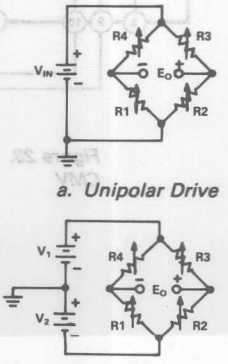


Figure 20. Boosted Precision Current Source

BRIDGE DRIVER CIRCUITS

The Wheatstone bridge is a common transducer. In its simplest form, a bridge consists of 4 two terminal elements connected to form a quadrilateral, a source of excitation connected along one of the diagonals and a detector comprising the other diagonal. Figure 21a shows a simple bridge driven from a unipolar excitation supply. E_O, a differential voltage, is proportional to the deviation of the element from the initial bridge values. Unfortunately, this bridge output voltage is riding on a common-mode voltage equal to approximately $V_{IN}/2$. Further processing of this signal may necessarily be limited to high common-mode rejection techniques such as instrumentation or isolation amplifiers.

Figure 21b shows the same bridge transducer, but this time it is driven from pair of bipolar supplies. This configuration ideally eliminates the common-mode voltage and relaxes the restrictions on any processing elements that follow.



a. Unipolar Drive

b. Bipolar Drive

Figure 21. Bridge Transducer Excitation

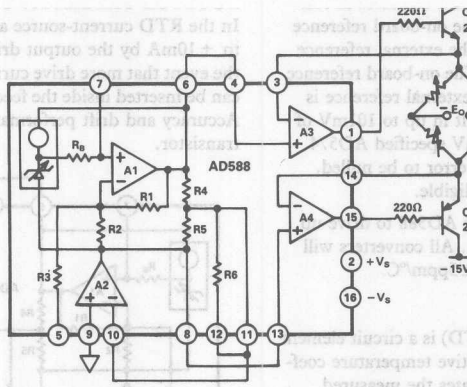


Figure 22. Bipolar Bridge Drive

As shown in Figure 22, the AD588 is an excellent choice for the control element in a bipolar bridge driver scheme. Transistors Q1 and Q2 serve as series pass elements to boost the current drive capability to the 28mA required by a typical 350Ω bridge. A differential gain stage may still be required if the bridge balance is not perfect. Such gain stages can be expensive.

Additional common-mode voltage reduction is realized by using the circuit illustrated in Figure 23. A1, the ground sense amplifier, servo's the supplies on the bridge to maintain a virtual ground at one center tap. The voltage which appears on the opposite center tap is now single-ended (referred to ground) and can be amplified by a less expensive circuit.

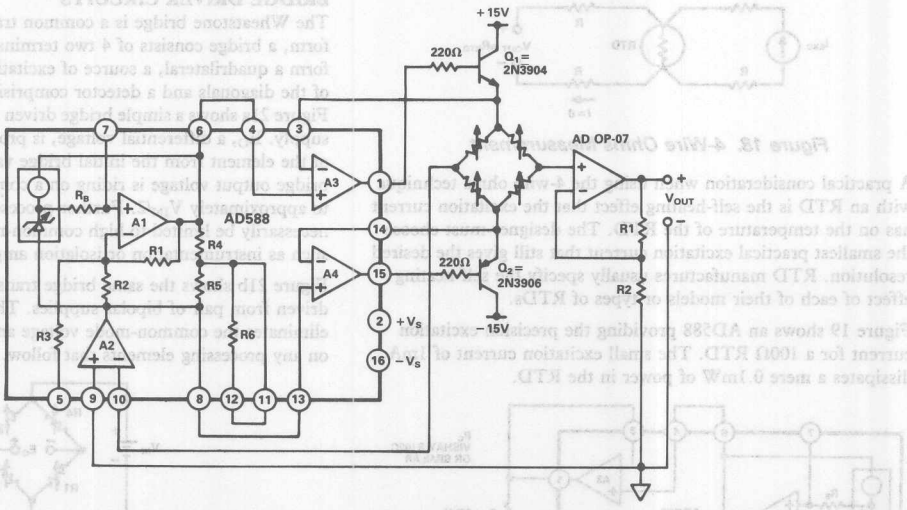


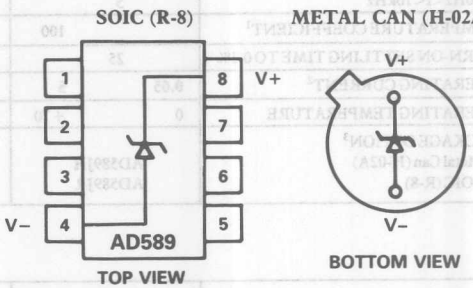
Figure 23. Floating Bipolar Bridge Drive with Minimum CMV

AD589

FEATURES

- Superior Replacement for Other 1.2V References
- Wide Operating Range: 50μA to 5mA
- Low Power: 60μW Total P_D at 50μA
- Low Temperature Coefficient:
  - 10ppm/°C max, 0 to +70°C (AD589M)
  - 25ppm/°C max, –55°C to +125°C (AD589U)
- Two-Terminal "Zener" Operation
- Low Output Impedance: 0.6Ω
- No Frequency Compensation Required
- Low Cost
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAMS



PRODUCT DESCRIPTION

The AD589 is a two-terminal, low cost, temperature compensated bandgap voltage reference which provides a fixed 1.23V output voltage for input currents between 50μA and 5.0mA.

The high stability of the AD589 is primarily dependent upon the matching and thermal tracking of the on-chip components. Analog Devices' precision bipolar processing and thin-film technology combine to provide excellent performance at low cost.

Additionally, the active circuit produces an output impedance ten times lower than typical low-TC zener diodes. This feature allows operation with no external components required to maintain full accuracy under changing load conditions.

The AD589 is available in seven versions. The AD589J, K, L and M grades are specified for 0 to +70°C operation, while the S, T and U grades are rated for the full –55°C to +125°C temperature range. All grades are available in a metal can (H-02A) package. The AD589J is also available in an 8-pin SOIC package.

PRODUCT HIGHLIGHTS

1. The AD589 is a two-terminal device which delivers a a constant reference voltage for a wide range of input current.
2. Output impedance of 0.6Ω and temperature coefficients as low as 10ppm/°C insure stable output voltage over a wide range of operating conditions.
3. The AD589 can be operated as a positive or negative reference. "Floating" operation is also possible.
4. The AD589 will operate with total current as low as 50μA (60μW total power dissipation), ideal for battery powered instrument applications.
5. The AD589 is an exact replacement for other 1.2V references, offering superior temperature performance and reduced sensitivity to capacitive loading.
6. The AD589 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD589/883B data sheet for detailed specifications.

AD589—SPECIFICATIONS (typical @ I_{IN} = 500μA and T_A = +25°C unless otherwise noted)

Model	AD589JH/JR			AD589KH			AD589LH			AD589MH			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE, T_A = +25°C	**1.200**	1.235	**1.250**	**1.200**	1.235	**1.250**	**1.200**	1.235	**1.250**	**1.200**	1.235	**1.250**	V
OUTPUT VOLTAGE CHANGE vs. CURRENT (50μA – 5mA)			5			5			5			5	mV
DYNAMIC OUTPUT IMPEDANCE		0.6	2		0.6	2		0.6	2		0.6	2	Ω
RMS NOISE VOLTAGE 10Hz<f<10kHz		5			5			5			5		μV
TEMPERATURE COEFFICIENT[1]			100			**50**			25			**10**	ppm/°C
TURN-ON SETTLING TIME TO 0.1%		25			25			25			25		μs
OPERATING CURRENT[2]	**0.05**		5	**0.05**		5	**0.05**		5	**0.05**		5	mA
OPERATING TEMPERATURE	0		+70	0		+70	0		+70	0		+70	°C
PACKAGE OPTION[3] Metal Can (H-02A) SOIC (R-8)	AD589JH AD589JR			AD589KH			AD589LH			AD589MH			

Model	AD589SH			AD589TH			AD589UH			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE, T_A = +25°C	**1.200**	1.235	**1.250**	**1.200**	1.235	**1.250**	**1.200**	1.235	**1.250**	V
OUTPUT VOLTAGE CHANGE vs. CURRENT (50μA – 5mA)			5			5			5	mV
DYNAMIC OUTPUT IMPEDANCE		0.6	2		0.6	2		0.6	2	Ω
RMS NOISE VOLTAGE 10Hz<f<10kHz		5			5			5		μV
TEMPERATURE COEFFICIENT[1]			100			**50**			25	ppm/°C
TURN-ON SETTLING TIME TO 0.1%		25			25			25		μs
OPERATING CURRENT[2]	**0.05**		5	**0.05**		5	**0.05**		5	mA
OPERATING TEMPERATURE	–55		+125	–55		+125	–55		+125	°C
PACKAGE OPTION[3] Metal Can (H-02A)	AD589SH			AD589TH			AD589UH			

NOTES
[1]See following page for explanation of temperature coefficient measurement method.
[2]Optimum performance is obtained at currents below 500μA. For current operation below 200μA, stray shunt capacitances should be limited to 20pF or increased to 1μF. If strays can not be avoided, operation at 500μA and a shunt capacitor of at least 1000pF are recommended.
[3]H = Hermetic Metal Can; R = SOIC. For outline information see Package Information section.

Specifications shown in boldface are tested on all production units at final electrical test.

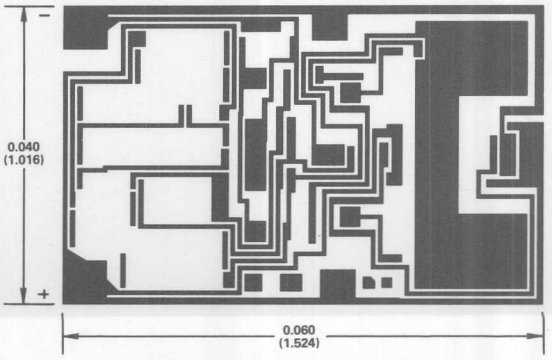
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Current 10mA
Reverse Current 10mA
Power Dissipation[1] 125mW
Storage Temperature Range . . . . . –65°C to +175°C
Operating Junction Temperature Range . –55°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C

NOTE
[1]Absolute maximum power dissipation is limited by maximum current through the device. Maximum rating at elevated temperatures must be computed assuming $T_J \leq 150°C$, and $\theta_{JA} = 400 = C/W$.

AD589 CHIP DIMENSIONS AND PAD LAYOUT



THE AD589 IS AVAILABLE IN CHIP FORM WITH FULLY TESTED AND GUARANTEED SPECIFICATIONS. CONSULT FACTORY FOR AVAILABLE GRADES AND PRICING.

VOLTAGE VARIATION vs. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of nonlinearities in temperature characteristics, which originated in standard zener references (such as "S" type characteristics) most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves measurement of the output at 3, 5 or more different temperatures to guarantee that the output voltage will fall within the given error band. The temperature characteristic of the AD589 consistently follows the curve shown in Figure 1. Three-point measurement guarantees the error band over the specified temperature range. The temperature coefficients specified on page 2 represent the slopes of the diagonals of the error band from +25°C to T_{min} and +25°C to T_{max}.

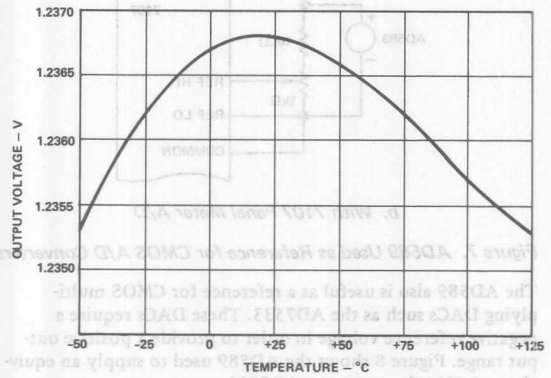


Figure 1. Typical AD589 Temperature Characteristics

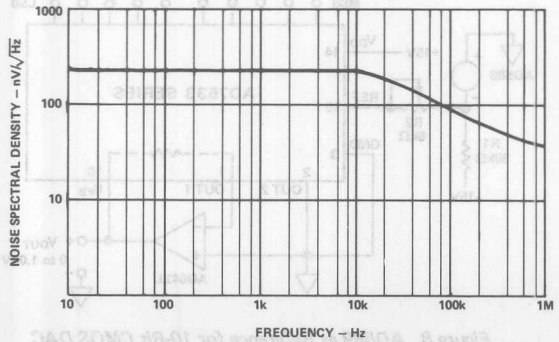


Figure 2. Noise Spectral Density

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 3 displays the turn-on characteristic of the AD589. This characteristic is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±1 millivolt is about 25μs, and there is no long thermal tail appearing after that point.

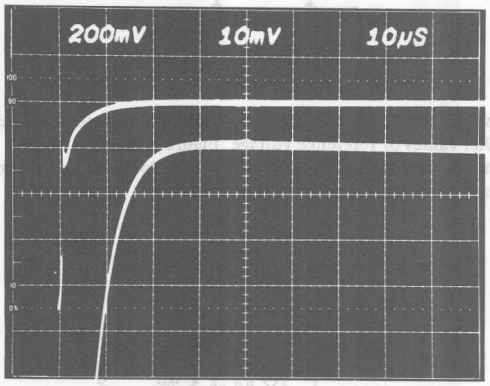


Figure 3. Output Settling Characteristics

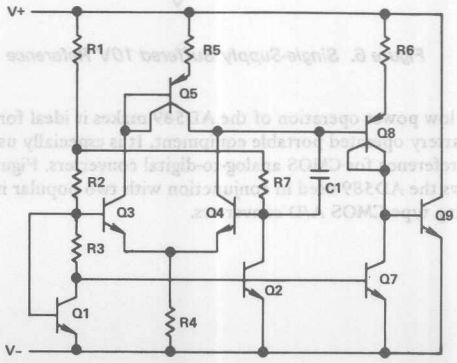


Figure 4. Schematic Diagram

6

The AD589 functions as a two-terminal shunt-type regulator. It provides a constant 1.23V output for a wide range of input current from 50μA to 5mA. Figure 5 shows the simplest configuration for an output voltage of 1.2V or less. Note that no frequency compensation is required. If additional filtering is desired for ultra low noise applications, minimum recommended capacitance is 1000pF.

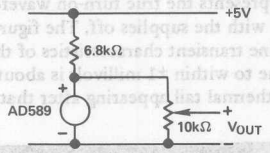


Figure 5. Basic Configuration for 1.2V or Less

The AD589 can also be used as a building block to generate other values of reference voltage. Figure 6 shows a circuit which produces a buffered 10V output. Total supply current for this circuit is approximately 2mA.

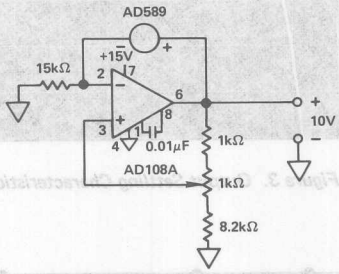
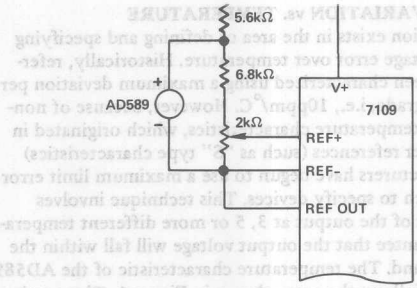
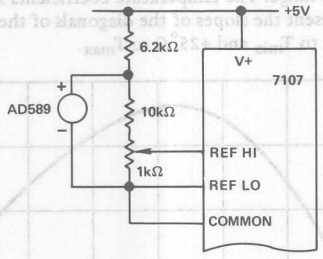


Figure 6. Single-Supply Buffered 10V Reference

The low power operation of the AD589 makes it ideal for use in battery operated portable equipment. It is especially useful as a reference for CMOS analog-to-digital converters. Figure 7 shows the AD589 used in conjunction with two popular integrating type CMOS A/D converters.



a. With 7109 12-Bit Binary A/D



b. With 7107 Panel Meter A/D

Figure 7. AD589 Used as Reference for CMOS A/D Converters

The AD589 also is useful as a reference for CMOS multiplying DACs such as the AD7533. These DACs require a negative reference voltage in order to provide a positive output range. Figure 8 shows the AD589 used to supply an equivalent −1.0V reference to an AD7533.

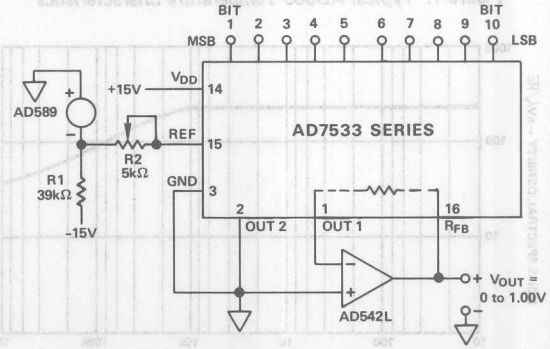


Figure 8. AD589 as Reference for 10-Bit CMOS DAC

Low Power, Low Cost 2.5 V Reference

AD680*

FEATURES

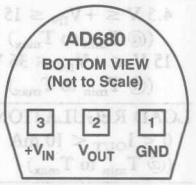
Low Quiescent Current: 250 μA max
Laser Trimmed to High Accuracy:
2.5 V ±5 mV max (AN Grade)
Trimmed Temperature Coefficient:
20 ppm/°C max (AN Grade)
Low Noise: 8 μV p–p from 0.1 to 10 Hz
250 nV/√Hz Wideband
Temperature Output Pin (N, R Packages)
Available in Three Package Styles:
8-Pin Plastic DIP, 8-Pin SOIC and 3-Pin TO-92

CONNECTION DIAGRAMS



NC = NO CONNECT

*TP DENOTES FACTORY TEST POINT. NO CONNECTIONS SHOULD BE MADE TO THESE PINS.



PRODUCT DESCRIPTION

The AD680 is a bandgap voltage reference which provides a fixed 2.5 V output from inputs between 4.5 V and 36 V. The architecture of the AD680 enables the reference to be operated at a very low quiescent current while still realizing excellent dc characteristics and noise performance. Trimming of the high stability thin-film resistors is performed for initial accuracy and temperature coefficient, resulting in low errors over temperature.

The precision dc characteristics of the AD680 make it ideal for use as a reference for D/A converters which require an external precision reference. The device is also ideal for A/D converters and, in general, can offer better performance than the standard on-chip references.

Based upon the low quiescent current of the AD680, which rivals that of many incomplete two-terminal references, the AD680 is recommended for low power applications such as hand-held battery equipment.

A temperature output pin is provided on the 8-pin package versions of the AD680. The temperature output pin provides an output voltage that varies linearly with temperature and allows the AD680 to be configured as a temperature transducer while providing a stable 2.5 V output.

The AD680 is available in four grades. The AD680AN is specified for operation from −40°C to +85°C, while the AD680JN is specified for 0°C to +70°C operation. Both the AD680AN and AD680JN are available in 8-pin plastic DIP packages. The AD680JR is specified for 0°C to +70°C operation and is available in an 8-pin Small Outline IC (SOIC) package. The AD680JT is specified for 0°C to +70°C operation and is available in a 3-pin TO-92 package.

***Protected by Patent Nos. 4,902,959; 4,250,445 and 4,857,862.**

PRODUCT HIGHLIGHTS

1. The AD680 bandgap reference operates on a very low quiescent current which rivals that of many two-terminal references. This makes the complete, higher accuracy AD680 ideal for use in power sensitive applications.
2. Laser trimming of both initial accuracy and temperature coefficients results in low errors over temperature without the use of external components. The AD680AN has a maximum variation of 6.25 mV between −40°C and +85°C.
3. The AD680 noise is low, typically 8 μV p–p from 0.1 to 10 Hz. Spectral density is also low, typically 250 nV/√Hz.
4. The temperature output pin on the 8-pin package versions enables the AD680 to be configured as a temperature transducer.
5. Plastic DIP packaging provides machine insertability, while SOIC packaging provides surface mount capability. TO-92 packaging offers a cost effective alternative to two-terminal references, offering a complete solution in the same package in which two-terminal references are usually found.

AD680—SPECIFICATIONS (T_A = +25°C, V_{IN} = +5 V unless otherwise specified)

Model	AD680AN Min	AD680AN Typ	AD680AN Max	AD680JN/JR Min	AD680JN/JR Typ	AD680JN/JR Max	AD680JT Min	AD680JT Typ	AD680JT Max	Units
OUTPUT VOLTAGE	2.495		2.505	2.490		2.510	2.490		2.510	V
OUTPUT VOLTAGE DRIFT[1]										
0°C to +70°C		10			10	25		10	30	ppm/°C
−40°C to +85°C			20		25			25		
LINE REGULATION										
4.5 V ≤ $+V_{IN}$ ≤ 15 V			40			*			*	µV/V
(@ T_{min} to T_{max})			40			*			*	
15 V ≤ $+V_{IN}$ ≤ 36 V			40			*			*	
(@ T_{min} to T_{max})			40			*			*	
LOAD REGULATION										
0 < I_{OUT} < 10 mA		80	100		*	*		*	*	µV/mA
(@ T_{min} to T_{max})		80	100		*	*		*	*	
QUIESCENT CURRENT		195	250		*	*		*	*	µA
(@ T_{min} to T_{max})		280				*			*	
POWER DISSIPATION		1	1.25		*	*		*	*	mW
OUTPUT NOISE										
0.1 to 10 Hz		8	10		*	*		*	*	µV p–p
Spectral Density, 100 Hz		250			*			*		nV/√Hz
CAPACITIVE LOAD			50			*			*	nF
LONG TERM STABILITY		25			*			*		ppm/1000 hr
SHORT CIRCUIT CURRENT TO GROUND		25	50		*	*		*	*	mA
TEMPERATURE PIN										
Voltage Output @ 25°C	540	596	660	*	*	*				mV
Temperature Sensitivity		2			*					mV/°C
Output Current	−5		+5	*		*				µA
Output Resistance		12			*					kΩ
TEMPERATURE RANGE										
Specified Performance	−40		+85	0		+70	0		+70	°C
Operating Performance[2]	−40		+85	−40		+85	−40		+85	

NOTES

[1]Maximum output voltage drift is guaranteed for all packages.

[2]The operating temperature range is defined as the temperature extremes at which the device will still function. Parts may deviate from their specified performance outside their specified temperature range.

*Same as AD680AN specification.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed.

ABSOLUTE MAXIMUM RATINGS*

V_{IN} to Ground . . . . . 36 V
Power Dissipation (25°C) . . . . . 500 mW
Storage Temperature . . . . . −65°C to +125°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
Package Thermal Resistance
θ_{JA} (All Packages) . . . . . 120°C/W
Output Protection: Output safe for indefinite short to ground and momentary short to V_{IN}.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8-Pin Plastic DIP and 8-Pin SOIC Packages



NC = NO CONNECT

*TP DENOTES FACTORY TEST POINT. NO CONNECTIONS SHOULD BE MADE TO THESE PINS.

TO-92 Package

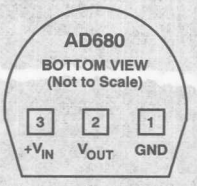


Figure 1. Connection Diagrams

THEORY OF OPERATION

Bandgap references are the high performance solution for low supply voltage operation. A typical precision bandgap will consist of a reference core and buffer amplifier. Based on a new, patented bandgap reference design (Figure 2), the AD680 merges the amplifier and the core bandgap function to produce a compact, complete precision reference. Central to the device is a high gain amplifier with an intentionally large Proportional To Absolute Temperature (PTAT) input offset. This offset is controlled by the area ratio of the amplifier input pair, Q1 and Q2, and is developed across resistor R1. Transistor Q12's base emitter voltage has a Complementary To Absolute Temperature (CTAT) characteristic. Resistor R2 and the parallel combination of R3 and R4 "multiply" the PTAT voltage across R1. Trimming resistors R3 and R4 to the proper ratio produces a temperature invariant 2.5 V at the output. The result is an accurate, stable output voltage accomplished with a minimum number of components.

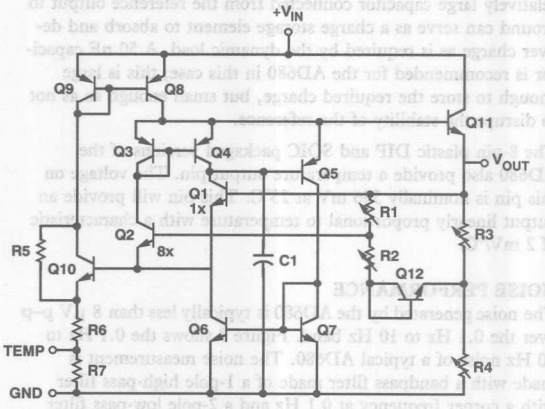


Figure 2. AD680 Schematic Diagram

An additional feature with this approach is the ability to minimize the noise while maintaining very low overall power dissipation for the entire circuit. Frequently it is difficult to independently control the dominant noise sources for bandgap references: bandgap transistor noise and resistor thermal noise. By properly choosing the operating currents of Q1 and Q2 and separately sizing R1, low wideband noise is realized while maintaining 1 mW typical power dissipation.

ORDERING GUIDE

Model	Initial Error mV	Temperature Coeff. ppm/°C	Temperature Range	Package Description	Package Option*
AD680JN	10	25	0°C to +70°C	Plastic	N-8
AD680JR	10	25	0°C to +70°C	SOIC	R-8
AD680JT	10	30	0°C to +70°C	TO-92	TO-92
AD680AN	5	20	−40°C to +85°C	Plastic	N-8

*N = Plastic DIP Package; R = SOIC Package; T = TO-92 Package. For outline information see Package Information section.

APPLYING THE AD680

The AD680 is simple to use in virtually all precision reference applications. When power is applied to $+V_{IN}$ and the GND pin is tied to ground, V_{OUT} provides a +2.5 V output. The AD680 typically requires less than 250 μA of current when operating from a supply of +4.5 V to +36 V.

To operate the AD680, the $+V_{IN}$ pin must be bypassed to the GND pin with a 0.1 μF capacitor tied as close to the AD680 as possible. Although the ground current for the AD680 is small (typically 195 μA), a direct connection should be made between the AD680 GND pin and the system ground plane.

Reference outputs are frequently required to handle fast transients caused by input switching networks, as are commonly found in ADCs and measurement instrumentation equipment. Many of the dynamic problems associated with this situation can be minimized with a few simple techniques. Using a series resistor between the reference output and the load will tend to "decouple" the reference output from the transient source. Or a relatively large capacitor connected from the reference output to ground can serve as a charge storage element to absorb and deliver charge as is required by the dynamic load. A 50 nF capacitor is recommended for the AD680 in this case; this is large enough to store the required charge, but small enough so as not to disrupt the stability of the reference.

The 8-pin plastic DIP and SOIC packaged versions of the AD680 also provide a temperature output pin. The voltage on this pin is nominally 596 mV at 25°C. This pin will provide an output linearly proportional to temperature with a characteristic of 2 mV/°C.

NOISE PERFORMANCE

The noise generated by the AD680 is typically less than 8 μV p–p over the 0.1 Hz to 10 Hz band. Figure 3 shows the 0.1 Hz to 10 Hz noise of a typical AD680. The noise measurement is made with a bandpass filter made of a 1-pole high-pass filter with a corner frequency at 0.1 Hz and a 2-pole low-pass filter with a corner frequency at 12.6 Hz to create a filter with a 9.922 Hz bandwidth.

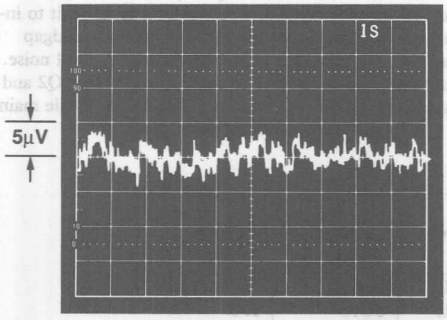


Figure 3. 0.1 Hz to 10 Hz Noise

Noise in a 300 kHz bandwidth is approximately 800 μV p–p. Figure 4 shows the broadband noise of a typical AD680.

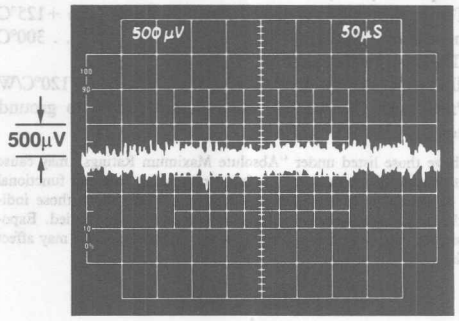


Figure 4. Broadband Noise at 300 kHz

TURN-ON TIME

Upon application of power (cold start), the time required for the output voltage to reach its final value within a specified error band is defined as the turn-on settling time. Two components normally associated with this are: the time for the active circuits to settle, and the time for the thermal gradients on the chip to stabilize. Figure 5 shows the turn-on settling time of the AD680 to be about 20 μs to 0.025% of its final value.

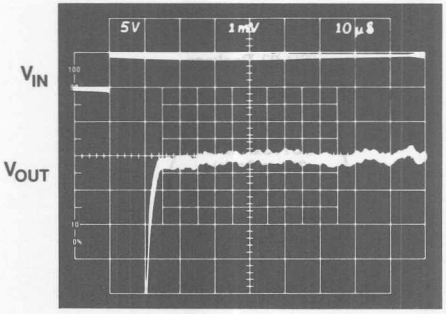


Figure 5. Turn-On Settling Time

The AD680 thermal settling characteristic benefits from its compact design. Once initial turn-on is achieved, the output linearly approaches its final value; the output is typically within 0.01% of its final value after 25 ms.

DYNAMIC PERFORMANCE

The output stage of the amplifier is designed to provide the AD680 with static and dynamic load regulation superior to less complete references.

Figure 6 displays the characteristics of the AD680 output amplifier driving a 0 to 10 mA load. Longer settling times will result if the reference is forced to sink any transient current.

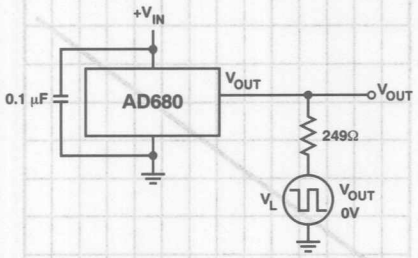


Figure 6a. Transient Load Test Circuit

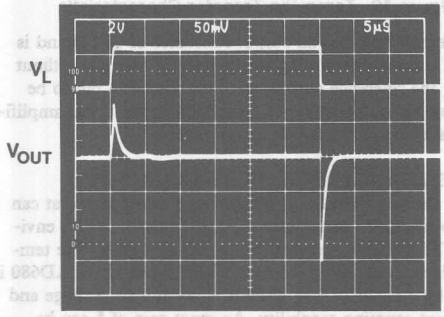


Figure 6b. Large-Scale Transient Response

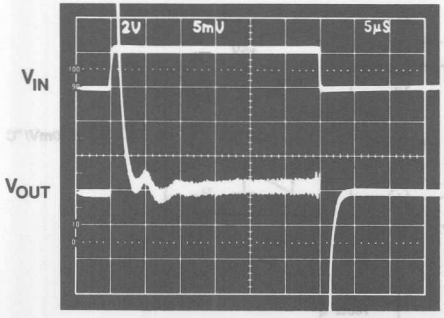


Figure 6c. Fine Scale Settling for Transient Load

In some applications, a varying load may be both resistive and capacitive in nature, or the load may be connected to the AD680 by a long capacitive cable.

Figure 7 displays the output amplifier characteristics driving a 1000 pF, 0 to 10 mA load.

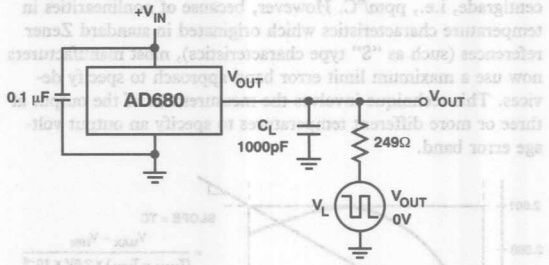


Figure 7a. Capacitive Load Transient Response Test Circuit

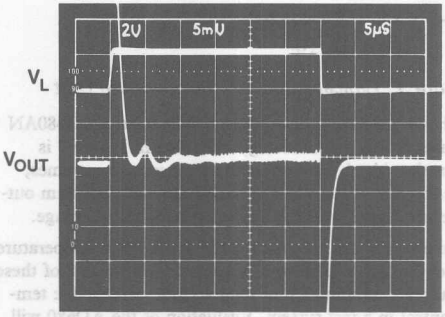


Figure 7b. Output Response with Capacitive Load

LOAD REGULATION

Figure 8 shows the load regulation characteristics of the AD680.

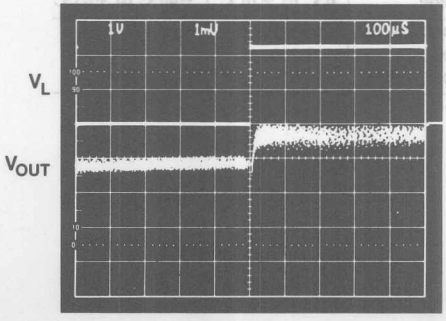


Figure 8. Typical Load Regulation Characteristics

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TEMPERATURE PERFORMANCE

The AD680 is designed for reference applications where temperature performance is important. Extensive temperature testing and characterization ensures that the device's performance is maintained over the specified temperature range.

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree centigrade, i.e., ppm/°C. However, because of nonlinearities in temperature characteristics which originated in standard Zener references (such as "S" type characteristics), most manufacturers now use a maximum limit error band approach to specify devices. This technique involves the measurement of the output at three or more different temperatures to specify an output voltage error band.

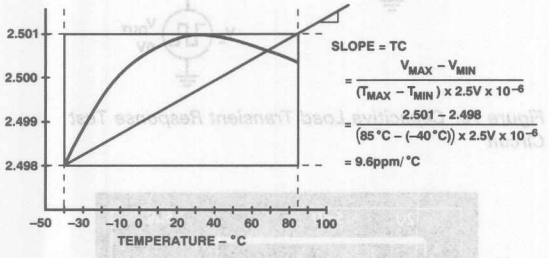


Figure 9. Typical AD680AN Temperature Drift

Figure 9 shows a typical output voltage drift for the AD680AN and illustrates the test methodology. The box in Figure 9 is bounded on the sides by the operating temperature extremes, and on the top and bottom by the maximum and minimum output voltages measured over the operating temperature range.

The maximum height of the box for the appropriate temperature range and device grade is shown in Table I. Duplication of these results requires a combination of high accuracy and stable temperature control in a test system. Evaluation of the AD680 will produce a curve similar to that in Figure 9, but output readings may vary depending upon the test equipment utilized.

Table I. Maximum Output Change in mV

Device Grade	Maximum Output Change (mV) 0°C to +70°C	−40°C to +85°C
AD680JN/JR	4.375	—
AD680JT	5.250	—
AD680AN	—	6.250

TEMPERATURE OUTPUT PIN

The 8-pin packaged versions of the AD680 provide a temperature output pin on Pin 3 of each device. The output of Pin 3 (TEMP) is a voltage that varies linearly with temperature. V_{TEMP} at 25°C is 596 mV, and the temperature coefficient is 2 mV/°C. Figure 10 shows the output of this pin over temperature.

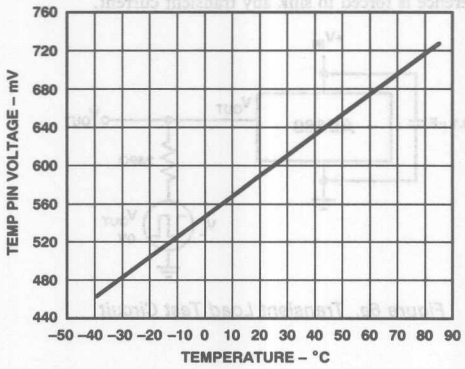


Figure 10. Temp Pin Transfer Characteristic

The temperature pin has an output resistance of 12 kΩ and is capable of sinking or sourcing currents of up to 5 μA without disturbing the reference output, enabling the temp pin to be buffered by any of a number of inexpensive operational amplifiers that have bias currents below this value.

DIFFERENTIAL TEMPERATURE TRANSDUCER

Figure 11 shows a differential temperature transducer that can be used to measure temperature changes in the AD680's environment. This circuit operates from a +5 V supply. The temperature dependent voltage from the TEMP pin of the AD680 is amplified by a factor of 5 to provide wider full-scale range and more current sourcing capability. An exact gain of 5 can be achieved by adjusting the trim potentiometer until the output varies by 10 mV/°C. To minimize resistance changes with temperature, resistors with low temperature coefficients, such as metal film resistors, should be used.

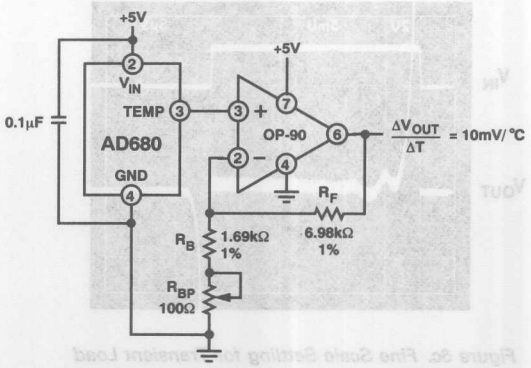


Figure 11. Differential Temperature Transducer

LOW POWER, LOW VOLTAGE REFERENCE FOR DATA CONVERTERS

The AD680 has a number of features that make it ideally suited for use with A/D and D/A converters. The low supply voltage required makes it possible to use the AD680 with today's converters that run on 5 V supplies without having to add a higher supply voltage for the reference. The low quiescent current (195 μA), combined with the completeness and accuracy of the AD680 make it ideal for low power applications such as handheld, battery operated meters.

One such ADC that the AD680 is well suited for is the AD7701. Figure 12a shows the AD680 used as the reference for this converter. The AD7701 is a 16-bit A/D converter with on-chip digital filtering intended for the measurement of wide dynamic range, low frequency signals such as those representing chemical, physical or biological processes. It contains a charge balancing (sigma-delta) ADC, calibration microcontroller with on-chip static RAM, a clock oscillator and a serial communications port.

This entire circuit runs on ±5 V supplies. The power dissipation of the AD7701 is typically 25 mW and, when combined with the power dissipation of the AD680 (1 mW), the entire circuit consumes just 26 mW of power.

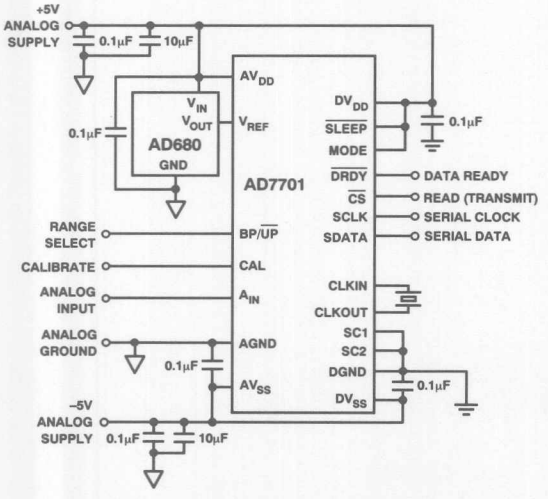


Figure 12a. Low Power, Low Voltage Supply Reference for the AD7701 16-Bit A/D Converter

Figure 12b shows the AD680 connected to the AD773 high speed 8-bit ADC. The low pass filter shown minimizes the AD680's wideband noise.

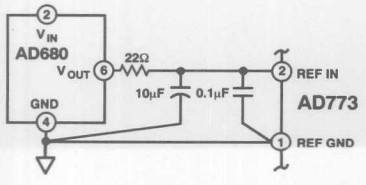


Figure 12b. AD680 to AD773 Connection

The AD773's high impedance reference input allows direct connection to the AD680. Unlike the resistor ladder requirements of a flash converter the AD773's single pin, high impedance input can be driven from one low cost, low power reference. The high impedance input allows multiple AD773's to be driven from one AD680 thus minimizing drift errors.

+4.5 V REFERENCE FROM A +5 V SUPPLY

The AD680 can be used to provide a low power, +4.5 V reference as shown in Figure 13. In addition to the AD680, the circuit uses a low power op amp and a transistor in a feedback configuration that provides a regulated +4.5 V output for a power supply voltage as low as +4.7 V. The high quality tantalum 10 μF capacitor (C1) in parallel with the ceramic 0.1 μF capacitor (C2) and the 3.9 Ω resistor (R5) ensure a low output impedance up to around 50 MHz.

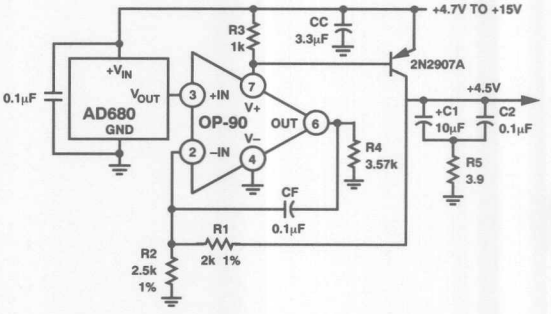


Figure 13. +4.5 V Reference Running from a Single +5 V Supply

VOLTAGE REGULATOR FOR PORTABLE EQUIPMENT

The AD680 is ideal for providing a stable, low cost and low power reference voltage in portable equipment power supplies. Figure 14 shows how the AD680 can be used in a voltage regulator that not only has low output noise (as compared to a switchmode design) and low power, but also a very fast recovery after current surges. Some precaution should be taken in the selection of the output capacitors. Too high an ESR (effective series resistance) could endanger the stability of the circuit. A solid tantalum capacitor, 16 V or higher, and an aluminum electrolytic capacitor, 10 V or higher, are recommended for C1 and C2, respectively. Also, the path from the ground side of C1 and C2 to the ground side of R1 should be kept as short as possible.

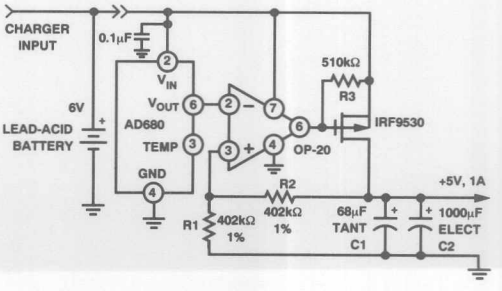
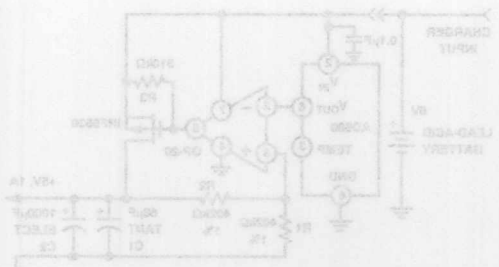


Figure 14. Voltage Regulator for Portable Equipment

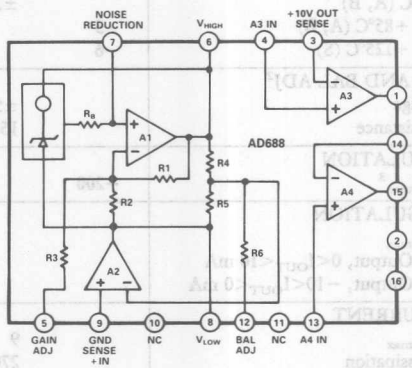


AD688*

FEATURES

±10 V Tracking Outputs
Kelvin Connections
Low Tracking Error – 1.5 mV
Low Initial Error – 2.0 mV
Low Drift – 1.5 ppm/°C
Low Noise – 6 μV p–p
Flexible Output Force and Sense Terminals
High Impedance Ground Sense
Machine Insertable DIP Packaging
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD688 is a high precision ±10 V tracking reference. Low tracking error, low initial error and low temperature drift give the AD688 reference absolute ±10 V accuracy performance previously unavailable in monolithic form. The AD688 uses a proprietary ion-implanted buried Zener diode, and laser-wafer-drift-trimming of high stability thin-film resistors to provide outstanding performance at low cost.

The AD688 includes the basic reference cell and three additional amplifiers. The amplifiers are laser-trimmed for low offset and low drift and maintain the accuracy of the reference. The amplifiers are configured to allow Kelvin connections to the load and/or boosters for driving long lines or high current loads, delivering the full accuracy of the AD688 where it is required in the application circuit.

The low initial error allows the AD688 to be used as a system reference in precision measurement applications requiring 12-bit absolute accuracy. In such systems, the AD688 can provide a known voltage for system calibration and the cost of periodic recalibration can therefore be eliminated. Furthermore, the mechanical instability of a trimming potentiometer and the potential for improper calibration can be eliminated by using the AD688 and calibration software.

The AD688 is available in three versions. The AD688AQ and BQ grades are packaged in 16-pin cerdip (0.3″) packages and are specified for operation from −40°C to +85°C. The AD688SQ grade is specified for operation from −55°C to +125°C.

***Protected by Patent Number 4,644,253.**

PRODUCT HIGHLIGHTS

1. The AD688 offers precision tracking ±10 V Kelvin output connections with no external components. Tracking error is less than 1.5 mV and a fine-trim is available for applications requiring exact symmetry between the +10 V and −10 V outputs.
2. The AD688 offers 12-bit absolute accuracy without any user adjustments. Optional fine-trim connections are provided for applications requiring higher precision. The fine-trimming does not alter the operating conditions of the Zener or the buffer amplifiers and thus does not increase the temperature drift.
3. Output noise of the AD688 is low – typically 6 μV p–p. A pin is provided for broadband noise filtering using an external capacitor.
4. The AD688 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD688/883B data sheet for detailed specifications.

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OUTPUT VOLTAGE ERROR						
+10V, −10V Outputs	−5		+5	−2	+2	mV
±10V TRACKING ERROR	−3		+3	−1.5	+1.5	mV
OUTPUT VOLTAGE DRIFT						
+10V, −10V Outputs						
0 to +70°C (A, B)		±2		−1.5	+1.5	ppm/°C
−40°C to +85°C (A, B)	−3		+3	−3	+3	ppm/°C
−55°C to +125°C (S)	−6		+6			ppm/°C
GAIN ADJ AND BAL ADJ[2]						
Trim Range		±5			±5	mV
Input Resistance		150			150	kΩ
LINE REGULATION						
T_{min} to T_{max}[3]	−200		+200	−200	+200	μV/V
LOAD REGULATION						
T_{min} to T_{max}						
+10 V Output, $0<I_{OUT}<10$ mA			±50		±50	μV/mA
−10 V Output, $-10<I_{OUT}<0$ mA			±50		±50	μV/mA
SUPPLY CURRENT						
T_{min} to T_{max}		9	12		9	12	mA
Power Dissipation		270	360		270	360	mW
OUTPUT NOISE (ANY OUTPUT)						
0.1 Hz to 10 Hz		6			6		μV p–p
Spectral Density, 100 Hz		140			140		$nV/\sqrt{Hz}$
LONG TERM STABILITY (@ +25°C)		15			15		ppm/1000 hours
BUFFER AMPLIFIERS						
Offset Voltage		100			100		μV
Offset Voltage Drift		1			1		μV/°C
Bias Current		20			20		nA
Open Loop Gain		110			110		dB
Output Current A3, A4	−10		+10	−10	+10		mA
Common Mode Rejection (A3, A4)						
V_{CM} = 1 V p–p		100			100		dB
Short-Circuit Current		50			50		mA
TEMPERATURE RANGE						
Specified Performance						
A, B Grades	−40		+85	−40	+85		°C
S Grade	−55		+125				°C

NOTES

[1]See Figure 2a for output configuration. Specifications tested using +10 V output unless otherwise indicated.

[2]Gain and balance adjustments guaranteed capable of trimming output voltage error and symmetry error to zero.

[3]Test Condition: $+V_S$ = +18 V, $-V_S$ = −18 V; $+V_S$ = +13.5 V, $-V_S$ = −13.5 V.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to $-V_S$ . . . . . 36 V

Power Dissipation (+25°C)

Q Package . . . . . 600 mW

Storage Temperature . . . . . −65°C to +150°C

Lead Temperature (Soldering, 10 Seconds) . . . . . +300°C

Package Thermal Resistance

Q (θ_{JA}/θ_{JC}) . . . . . 120/35°C/W

Output Protection: All outputs safe if shorted to ground

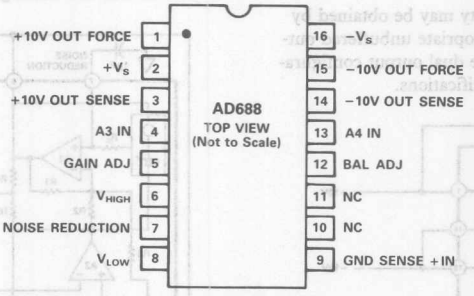
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ORDERING GUIDE

Part Number[1]	Initial Error	Temperature Coefficient	Temperature Range – °C	Package Option[2]
AD688AQ	5 mV	3 ppm/°C	−40 to +85	Q-16
AD688BQ	2 mV	3 ppm/°C	−40 to +85[3]	Q-16
AD688SQ	5 mV	6 ppm/°C	−55 to +125	Q-16
AD688/883B	*	*	−55 to +125	*

NOTE
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD688/883B data sheet.
[2]Q = Cerdip. For outline information see Package Information section.
[3]Temperature coefficient specified from 0 to +70°C.
*Refer to AD688/883B military data sheet.

PIN CONFIGURATION



NC = NO CONNECT

NC PINS ARE USED AS TEST POINTS BY THE FACTORY. TO ENSURE PROPER OPERATION, DO NOT CONNECT ANYTHING TO THESE PINS.

THEORY OF OPERATION

The AD688 consists of a buried Zener diode reference, amplifiers and associated thin-film resistors as shown in the block diagram of Figure 1. The temperature compensation circuitry provides the device with a temperature coefficient of 1.5 ppm/°C or less.

Amplifier A1 performs several functions. A1 primarily acts to amplify the Zener voltage to the required 20 volts. In addition, A1 also provides for external adjustment of the 20 V output through Pin 5, the GAIN ADJUST. Using the bias compensation resistor between the Zener output and the noninverting input to A1, a capacitor can be added at the NOISE REDUCTION pin (Pin 7) to form a low pass filter and reduce the noise contribution of the Zener to the circuit. Two matched 12 kΩ nominal thin-film resistors (R4 and R5) divide the 20 V output in half.

Ground sensing for the circuit is provided by Amplifier A2. The noninverting input (Pin 9) senses the system ground and forces the midpoint of resistors R4 and R5 to be a virtual ground. Pin 12 (BALANCE ADJUST) can be used for fine adjustment of this midpoint transfer.

Amplifiers A3 and A4 are internally compensated and are used to buffer the voltages at Pins 6 and 8 as well as to provide a full Kelvin output. Thus, the AD688 has a full Kelvin capability by providing the means to sense a system ground and provide forced and sensed outputs referenced to that ground.

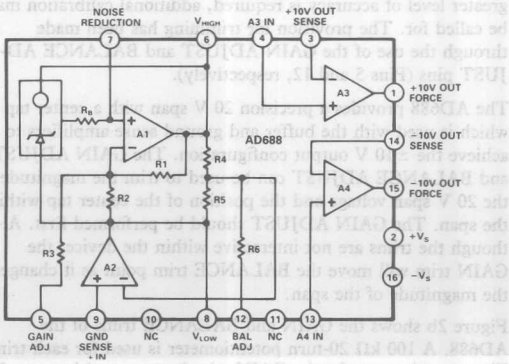


Figure 1. AD688 Functional Block Diagram

APPLYING THE AD688

The AD688 can be configured to provide ±10 V reference outputs as shown in Figure 2a. The architecture of the AD688 provides ground sense and uncommitted output buffer amplifiers which offer the user a great deal of functional flexibility. The AD688 is specified and tested in the configuration shown in Figure 2a. The user may choose to take advantage of other configuration options available with the AD688; however performance in these configurations is not guaranteed to meet the stringent data sheet specifications.

Unbuffered outputs are available at Pins 6 and 8. Loading of these unbuffered outputs will impair circuit performance.

Amplifiers A3 and A4 can be used interchangeably. However, the AD688 is tested (and the specifications are guaranteed) with the amplifiers connected as indicated in Figure 2a. When either A3 or A4 is unused, its output force and sense pins should be connected and the input tied to ground.

Two outputs of the same voltage polarity may be obtained by connecting both A3 and A4 to the appropriate unbuffered output on Pin 6 or 8. Performance in these dual output configurations will typically meet data sheet specifications.

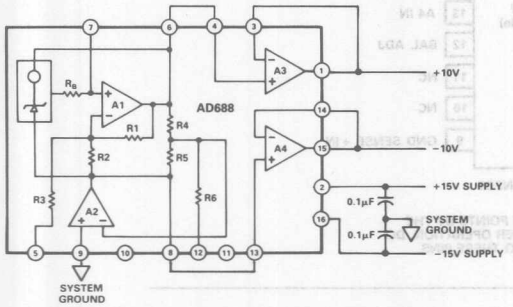


Figure 2a. +10 V and −10 V Outputs

CALIBRATION

Generally, the AD688 will meet the requirements of a precision system without additional adjustment. Initial output voltage error of 2 mV and output noise specs of 6 μV p–p allow for accuracies of 12–16 bits. However, in applications where an even greater level of accuracy is required, additional calibration may be called for. The provision for trimming has been made through the use of the GAIN ADJUST and BALANCE ADJUST pins (Pins 5 and 12, respectively).

The AD688 provides a precision 20 V span with a center tap which is used with the buffer and ground sense amplifiers to achieve the ±10 V output configuration. The GAIN ADJUST and BALANCE ADJUST can be used to trim the magnitude of the 20 V span voltage and the position of the center tap within the span. The GAIN ADJUST should be performed first. Although the trims are not interactive within the device, the GAIN trim will move the BALANCE trim point as it changes the magnitude of the span.

Figure 2b shows the GAIN and BALANCE trims of the AD688. A 100 kΩ 20-turn potentiometer is used for each trim. The potentiometer for the GAIN trim is connected between Pins 6 (V_{HIGH}) and 8 (V_{LOW}) with the wiper connected to Pin 5 (GAIN ADJ). The potentiometer is adjusted to produce exactly 20 V between Pins 1 and 15, the amplifier outputs. The BALANCE potentiometer, also connected between Pins 6 and 8 with the wiper to Pin 12 (BAL ADJ), is then adjusted to center the span from +10 V to −10 V.

Input impedance on both the GAIN ADJUST and the BALANCE ADJUST pins is approximately 150 kΩ. The GAIN ADJUST trim network effectively attenuates the 20 V across the trim potentiometer by a factor of about 1150 to provide a trim range of −5.8 mV to +12.0 mV with a resolution of approximately 900 μV/turn (20 turn potentiometer). The BALANCE ADJUST trim network attenuates the trim voltage by a factor of about 1250, providing a trim range of ±8 mV with a resolution of 800 μV/turn.

Trimming the AD688 introduces no additional errors over temperature, so precision potentiometers are not required.

In cases when BALANCE ADJUST is not necessary, Pin 12 should be left floating. If GAIN ADJUST is not required, Pin 5 should also be left floating.

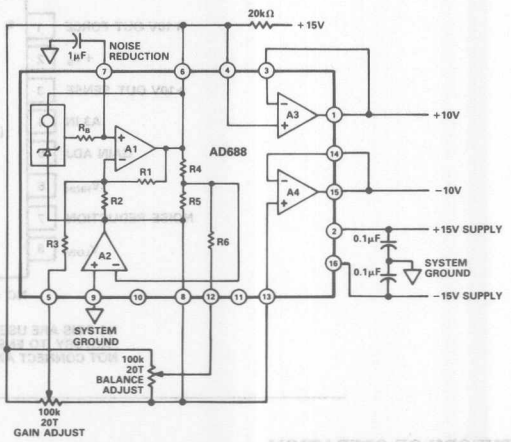


Figure 2b. Gain and Balance Adjust with Noise Reduction

NOISE PERFORMANCE AND REDUCTION

The noise generated by the AD688 is typically less than 6 μV p–p over the 0.1 Hz to 10 Hz band. Noise in a 1 MHz bandwidth is approximately 840 μV p–p. The dominant source of this noise is the buried Zener which contributes approximately 140 nV/$\sqrt{\text{Hz}}$. In comparison, the op amp's contribution is negligible. Figure 3 shows the 0.1 Hz to 10 Hz noise of a typical AD688.

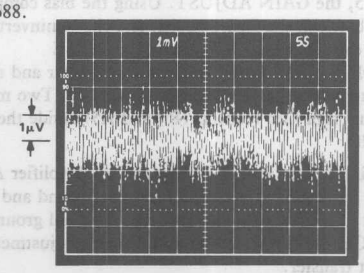


Figure 3. 0.1 Hz to 10 Hz Noise

If further noise reduction is desired, an optional capacitor may be added between the NOISE REDUCTION pin and ground as shown in Figure 2b. This will form a low pass filter with the

5 kΩ R_B on the output of the Zener cell. A 1 μF capacitor will have a 3 dB point at 32 Hz and will reduce the high frequency noise (to 1 MHz) to about 250 μV p-p. Figure 4 shows the 1 MHz noise of a typical AD688 both with and without a 1 μF capacitor.

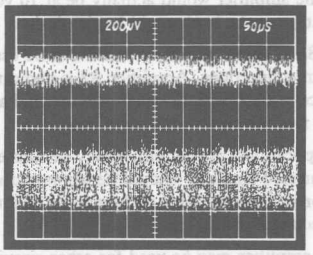
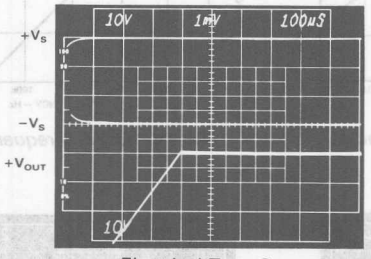


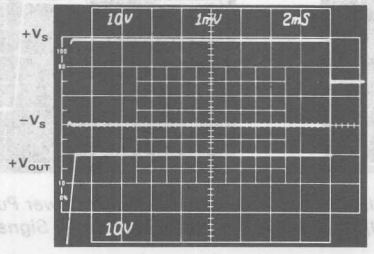
Figure 4. Effect of 1 μF Noise Reduction Capacitor on Broadband Noise

TURN-ON TIME

Upon application of power (cold start), the time required for the output voltage to reach its final value within a specified error is the turn-on settling time. Two components normally associated with this are: time for active circuits to settle and time for thermal gradients on the chip to stabilize. Figure 5 shows the turn-on characteristics of the AD688. It shows the settling time to be about 600 μs. Note the absence of any thermal tails when the horizontal scale is expanded to 2 ms/cm in Figure 5b.



a. Electrical Turn-On



b. Extended Time Scale

Figure 5. Turn-On Characteristics

Output turn-on time is modified when an external noise reduction capacitor is used. When present, this capacitor presents an additional load to the internal Zener diode's current source, resulting in a somewhat longer turn-on time. In the case of a 1 μF capacitor, the initial turn-on time is approximately 100 ms (see Figure 6).

When the NOISE REDUCTION feature is used, a 20 kΩ resistor between Pins 6 and 2 is required for proper startup.

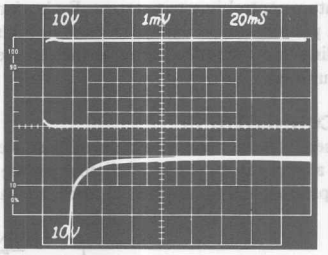


Figure 6. Turn-On With 1μF C_N

TEMPERATURE PERFORMANCE

The AD688 is designed for precision reference applications where temperature performance is critical. Extensive temperature testing ensures that the device's high level of performance is maintained over the operating temperature range.

Figure 7 shows the typical output voltage drift for the AD688SQ and illustrates the test methodology. The box in Figure 7 is bounded on the sides by the operating temperature extremes and on top and bottom by the maximum and minimum +10 V output error voltages measured over the operating temperature range. The slopes of the diagonals drawn for both the +10 V and −10 V outputs determine the performance grade of the device.

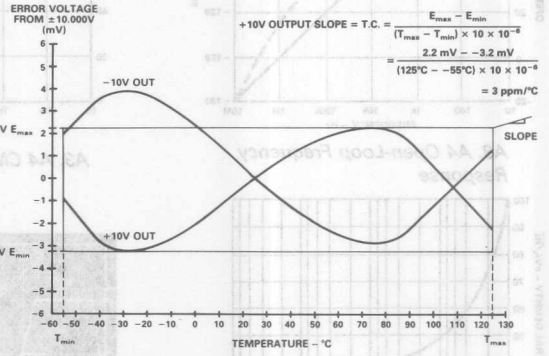


Figure 7. Typical AD688SQ Temperature Drift

Each AD688A and B grade unit is tested at −40°C, −25°C, 0°C, +25°C, +50°C, +70°C and +85°C. Each AD688S grade unit is tested at −55°C, −25°C, +25°C, +70°C and +125°C. This approach ensures that the variations of output voltage that occur as the temperature changes within the specified range will be contained within a box whose diagonal has a slope equal to the maximum specified drift. The position of the box on the vertical scale will change from device to device as initial error and the shape of the curve vary. Maximum height of the box for the appropriate temperature range is shown in Figure 8. Duplication

DEVICE GRADE	MAXIMUM OUTPUT CHANGE mV 0 TO +70°C	−40°C TO +85°C	−55°C TO +125°C
AD688AQ	1.40 (typ)	3.75	
AD688BQ	1.05	3.75	
AD688SQ			10.80

Figure 8. Maximum +10 V or −10 V Output Change

AD688 will produce curves similar to those in Figure 7, but output readings may vary depending on the test methods and equipment utilized.

KELVIN CONNECTIONS

Force and sense connections, also referred to as Kelvin connections, offer a convenient method of eliminating the effects of voltage drops in circuit wires. As seen in Figure 9a, the load

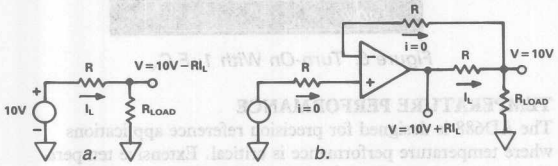


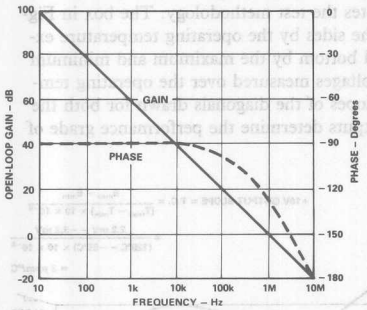
Figure 9. Advantage of Kelvin Connection

problem by including the wire resistance within the forcing loop of the amplifier and sensing the load voltage. The amplifier corrects for any errors in the load voltage. In the circuit shown, the output of the amplifier would actually be at 10 volts + V_{ERROR} and the voltage at the load would be the desired 10 volts.

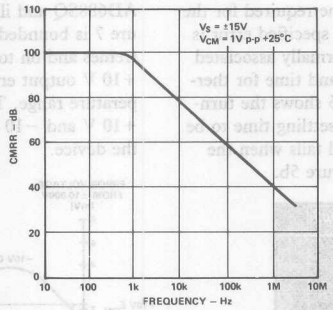
The AD688 has three amplifiers which can be used to implement Kelvin connections. Amplifier A2 is dedicated to the ground force-sense function while uncommitted amplifiers A3 and A4 are free for other force-sense chores.

In some applications, one amplifier may be unused. In such cases, the unused amplifier should be connected as a unity-gain follower (force and sense pins tied together) and the input should be connected to ground.

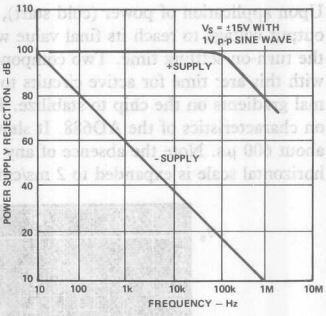
An unused amplifier may be used for other circuit functions as well. The curves on this page show the typical performance of A3 and A4.



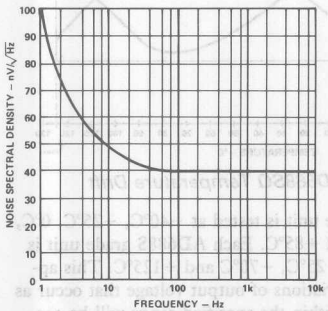
A3, A4 Open-Loop Frequency Response



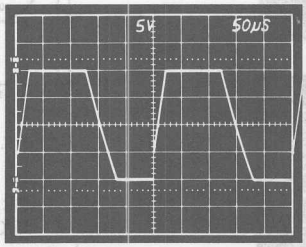
A3, A4 CMR vs. Frequency



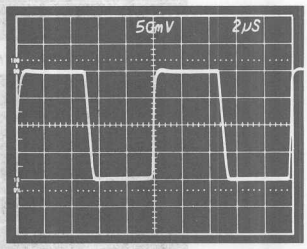
A3, A4 PSR vs. Frequency



Input Noise Voltage Spectral Density



Unity-Gain Follower Pulse Response (Large Signal)



Unity-Gain Follower Pulse Response (Small Signal)

DYNAMIC PERFORMANCE

The output buffer amplifiers (A3 and A4) are designed to provide the AD688 with static and dynamic load regulation superior to less complete references.

Many A/D and D/A converters present transient current loads to the reference, and poor reference response can degrade the converter's performance.

Figure 10 displays the characteristic of the AD688 output amplifier driving a 0–to–10 mA load.

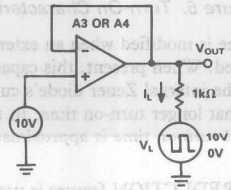


Figure 10a. Transient Load Test Circuit

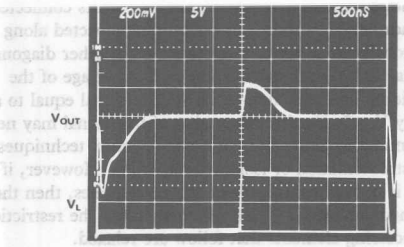


Figure 10b. Large-Scale Transient Response

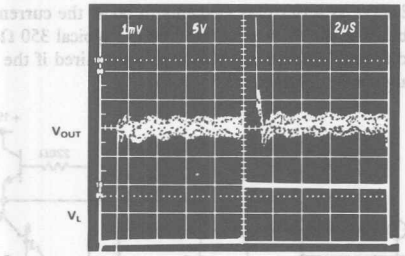


Figure 10c. Fine-Scale Settling for Transient Load

Figure 11 displays the output amplifier characteristic driving a 5 mA–to–10 mA load, a common situation found when the reference is shared among multiple converters or is used to provide bipolar offset current.

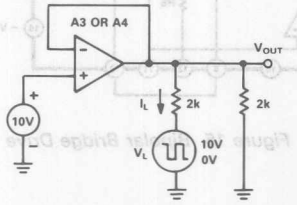


Figure 11a. Transient and Constant Load Test Circuit

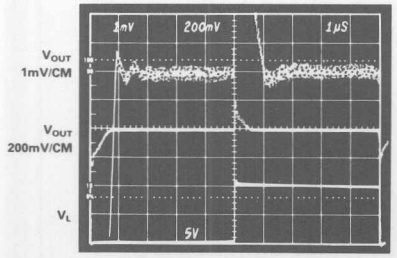


Figure 11b. Transient Response 5–10 mA Load

capacitive in nature, or be connected to the AD688 by a long capacitive cable. Figure 12 displays the output amplifier characteristics driving a 1,000 pF, 0–to–10 mA load.

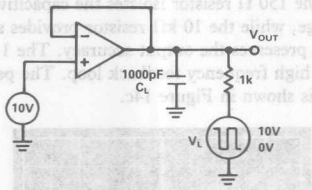


Figure 12a. Capacitive Load Transient Response Test Circuit

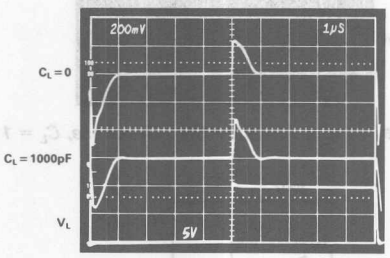


Figure 12b. Output Response with Capacitive Load

Figure 13 displays the crosstalk between output amplifiers. The top trace shows the output of A4, dc-coupled and offset by 10 volts, while the output of A3 is subjected to a 0–to–10 mA load current step. The transient at A4 settles in about 1 µs, and the load-induced offset is about 100 µV.

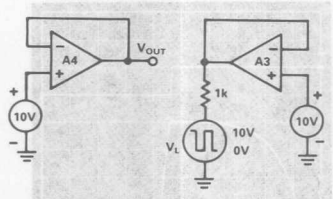


Figure 13a. Load Crosstalk Test Circuit

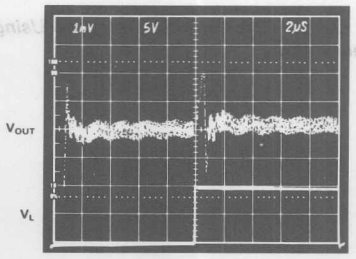


Figure 13b. Load Crosstalk

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Attempts to drive a large capacitive load (in excess of 1,000 pF) may result in ringing or oscillation, as shown in the step response photo (Figure 14a). This is due to the additional pole formed by the load capacitance and the output impedance of the amplifier, which consumes phase margin. The recommended method of driving capacitive loads of this magnitude is shown in Figure 14b. The 150 Ω resistor isolates the capacitive load from the output stage, while the 10 kΩ resistor provides a dc feedback path and preserves the output accuracy. The 1 μF capacitor provides a high frequency feedback loop. The performance of this circuit is shown in Figure 14c.

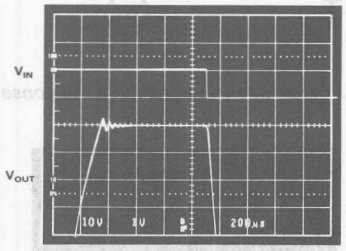


Figure 14a. Output Amplifier Step Response, C_L = 1 μF

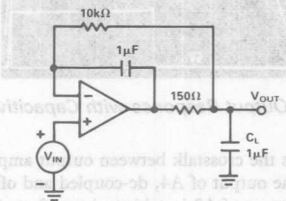


Figure 14b. Compensation for Capacitive Loads

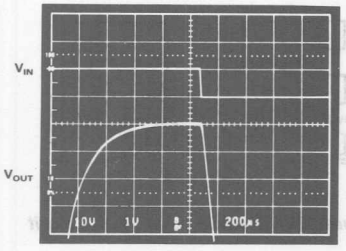


Figure 14c. Output Amplifier Step Response Using Figure 14b Compensation

BRIDGE DRIVER CIRCUIT

The Wheatstone bridge is a common transducer. In its simplest form, a bridge consists of 4 two-terminal elements connected to form a quadrilateral, a source of excitation connected along one of the diagonals and a detector comprising the other diagonal. In this unipolar drive configuration, the output voltage of the bridge is riding on a common-mode voltage signal equal to approximately $V_{IN}/2$. Further processing of this signal may necessarily be limited to high common-mode rejection techniques such as instrumentation or isolation amplifiers. However, if the bridge is driven from a pair of bipolar supplies, then the common-mode voltage is ideally eliminated and the restrictions on any processing elements that follow are relaxed.

As shown in Figure 15, the AD688 is an excellent choice for the control element in a bipolar bridge driver scheme. Transistors Q1 and Q2 serve as series pass elements to boost the current drive capability to the 57 mA required by the typical 350 Ω bridge. A differential gain stage may still be required if the bridge balance is not perfect.

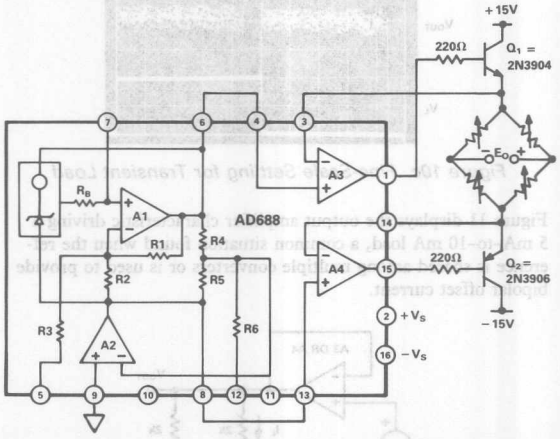


Figure 15. Bipolar Bridge Drive

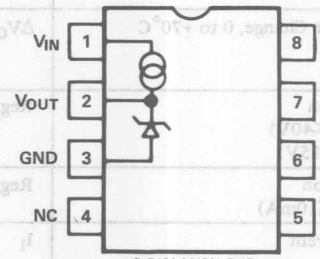
Low Cost, Precision 2.5V IC References

AD1403/AD1403A*

FEATURES

Improved, Lower Cost, Replacements for Standard 1403, 1403A
3-Terminal Device: Voltage In/Voltage Out
Laser Trimmed to High Accuracy: 2.500V ±10mV (AD1403A)
Excellent Temperature Stability: 25ppm/°C (AD1403A)
Low Quiescent Current: 1.5mA max
10mA Current Output Capability
Low Cost
Convenient Mini-DIP Package

FUNCTIONAL BLOCK DIAGRAM



8 PIN MINI-DIP

PRODUCT DESCRIPTION

The AD1403 and AD1403A are improved three-terminal, low cost, temperature compensated, bandgap voltage references that provide a fixed 2.5V output voltage for inputs between 4.5V and 40V. A unique combination of advanced circuit design and laser-wafer-trimmed thin-film resistors provides the AD1403/AD1403A with an initial tolerance of ±10mV and a temperature stability of better than 25ppm/°C. In addition, the low quiescent current drain of 1.5mA (max) offers a clear advantage over classical Zener techniques.

The AD1403 or AD1403A is recommended as a stable reference for all 8-, 10- and 12-bit D-to-A converters that require an external reference. In addition, the wide input range of the AD1403/AD1403A allows operation with 5 volt logic supplies, making these devices ideal for digital panel meter applications and when only a single logic supply is available.

The AD1403 and AD1403A are specified for operation over the 0 to +70°C temperature range. The AD580 series of 2.5 volt precision IC references is recommended for applications where operation over the −55°C to +125°C range is required.

PRODUCT HIGHLIGHTS

1. The AD1403A offers improved initial tolerance over the industry-standard 1403A: ±10mV versus ±25mV at a lower cost.
2. The three-terminal voltage in/voltage out operation of the AD1403/AD1403A provides a regulated output voltage without any external components.
3. The AD1403/AD1403A provides a stable 2.5V output voltage for input voltages between 4.5V and 40V making these devices ideal for systems that contain a single logic supply.
4. Thin film resistor technology and tightly controlled bipolar processing provide the AD1403A with temperature stabilities of 25ppm/°C.
5. The low 1.5mA maximum quiescent current drain of the AD1403 and AD1403A makes them ideal for CMOS and other low power applications.

6

*Covered by Patent Numbers: 3,887,863; RE30,586.

AD1403/AD1403A—SPECIFICATIONS (V_{IN} = 15V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 0mA)	V_O				
AD1403		2.475	2.500	2.525	V
AD1403A		2.490	2.500	2.510	
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				ppm/°C
AD1403		–	10	40	
AD1403A		–	10	25	
Output Voltage Change, 0 to +70°C	ΔV_O				mV
AD1403		–	–	7.0	
AD1403A		–	–	4.4	
Line Regulation	Reg_{in}				mV
(15V≤V_{IN}≤40V)		–	1.2	4.5	
(4.5≤V_{IN}≤15V)		–	0.6	3.0	
Load Regulation (0mA<I_O<10mA)	Reg_{load}	–	–	10	mV
Quiescent Current (I_O = 0mA)	I_I	–	1.2	1.5	mA

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Input Voltage	V_{IN}	40	V
Storage Temperature	T_{STG}	–25 to 100	°C
Junction Temperature	T_J	+175	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C

Specifications subject to change without notice.

ORDERING GUIDE

Model	Initial Tolerance	Package Option*
AD1403	±25mV	N-8
AD1403A	±10mV	N-8

*N = Plastic DIP. For outline information see Package Information section.

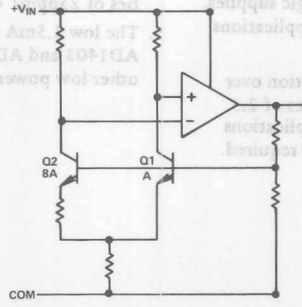


Figure 1. Simplified AD1403 Schematic

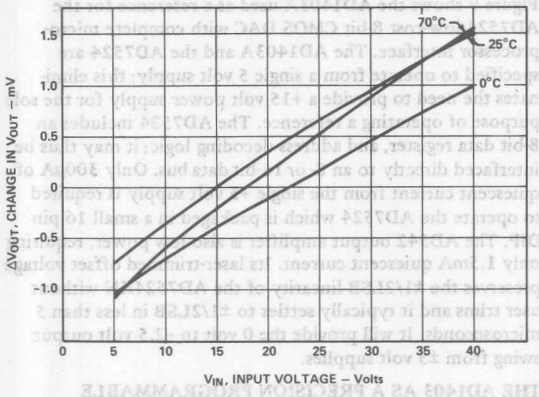


Figure 2. Typical Change in V_{OUT} vs. V_{IN} (Normalized to V_{OUT} @ V_{IN} = 15V @ T_C = 25°C)

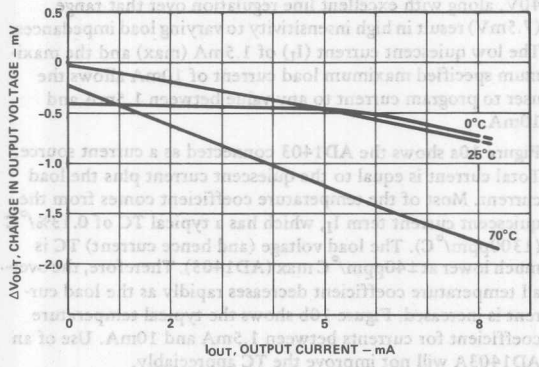


Figure 3. Change in Output Voltage vs. Load Current (Normalized to V_{OUT} @ V_{IN} = 15V, I_{OUT} = 0mA)

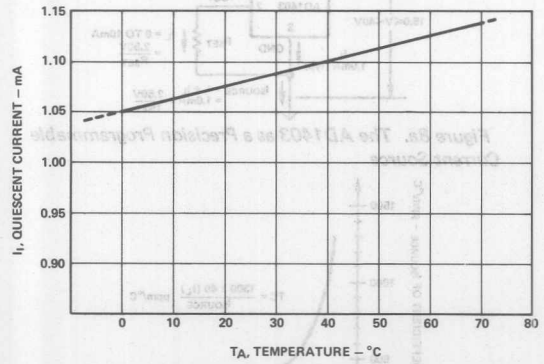


Figure 4. Quiescent Current vs. Temperature (V_{IN} = 15V, I_{OUT} = 0mA)

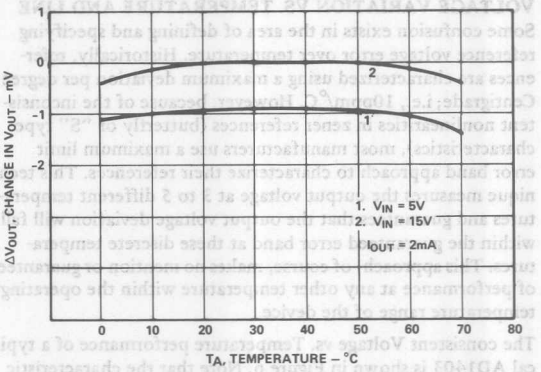


Figure 5. Change in V_{OUT} vs. Temperature (Normalized to V_{OUT} @ V_{IN} = 15V)

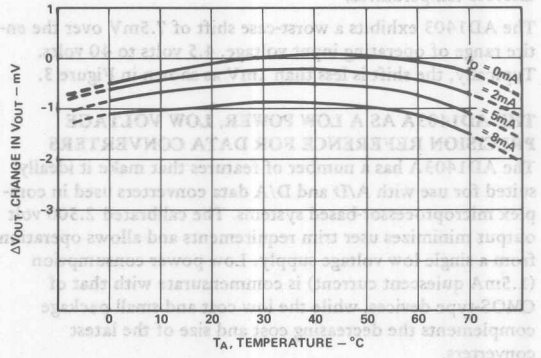
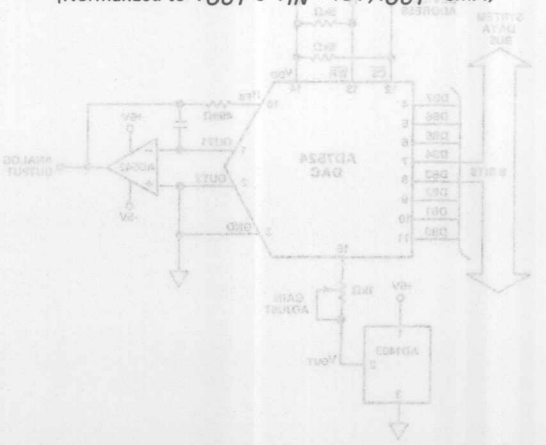


Figure 6. Change in V_{OUT} vs. Temperature (Normalized to V_{OUT} @ V_{IN} = 15V, I_{OUT} = 0mA)



6

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references are characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of the inconsistent nonlinearities in zener references (butterfly or "S" type characteristics), most manufacturers use a maximum limit error band approach to characterize their references. This technique measures the output voltage at 3 to 5 different temperatures and guarantees that the output voltage deviation will fall within the guaranteed error band at these discrete temperatures. This approach, of course, makes no mention or guarantee of performance at any other temperature within the operating temperature range of the device.

The consistent Voltage vs. Temperature performance of a typical AD1403 is shown in Figure 6. Note that the characteristic is quasi-parabolic, not the possible "S" type characteristics of classical zener references. This parabolic characteristic permits a maximum output deviation specification over the device's full operating temperature range, rather than just at 3 to 5 discrete temperatures.

The AD1403 exhibits a worst-case shift of 7.5mV over the entire range of operating input voltage, 4.5 volts to 40 volts. Typically, the shift is less than 1mV as shown in Figure 3.

THE AD1403A AS A LOW POWER, LOW VOLTAGE PRECISION REFERENCE FOR DATA CONVERTERS

The AD1403A has a number of features that make it ideally suited for use with A/D and D/A data converters used in complex microprocessor-based systems. The calibrated 2.500 volt output minimizes user trim requirements and allows operation from a single low voltage supply. Low power consumption (1.5mA quiescent current) is commensurate with that of CMOS-type devices, while the low cost and small package complements the decreasing cost and size of the latest converters.

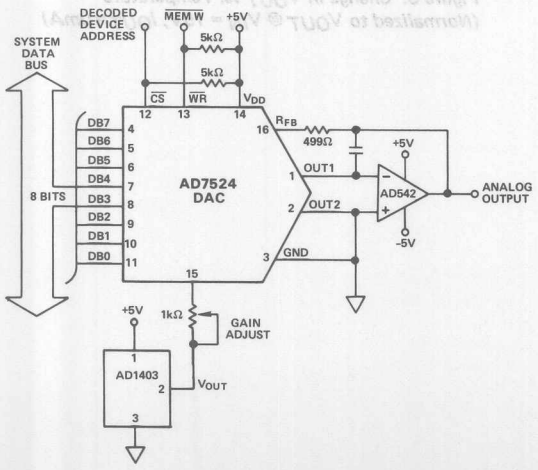


Figure 7. Low Power, Low Voltage Reference for the AD7524 Microprocessor-Compatible 8-Bit DAC

AD7524 low-cost 8-bit CMOS DAC with complete microprocessor interface. The AD1403A and the AD7524 are specified to operate from a single 5 volt supply; this eliminates the need to provide a +15 volt power supply for the sole purpose of operating a reference. The AD7524 includes an 8-bit data register, and address decoding logic; it may thus be interfaced directly to an 8- or 16-bit data bus. Only 300μA of quiescent current from the single +5 volt supply is required to operate the AD7524 which is packaged in a small 16 pin DIP. The AD542 output amplifier is also low power, requiring only 1.5mA quiescent current. Its laser-trimmed offset voltage preserves the ±1/2LSB linearity of the AD7524KN without user trims and it typically settles to ±1/2LSB in less than 5 microseconds. It will provide the 0 volt to −2.5 volt output swing from ±5 volt supplies.

THE AD1403 AS A PRECISION PROGRAMMABLE CURRENT SOURCE

The AD1403 is an excellent building block for precision current sources. Its wide range of operating voltages, 4.5V to 40V, along with excellent line regulation over that range (7.5mV) result in high insensitivity to varying load impedances. The low quiescent current (I_I) of 1.5mA (max) and the maximum specified maximum load current of 10mA allows the user to program current to any value between 1.5mA and 10mA.

Figure 10a shows the AD1403 connected as a current source. Total current is equal to the quiescent current plus the load current. Most of the temperature coefficient comes from the quiescent current term I_I, which has a typical TC of 0.13%/°C (1300ppm/°C). The load voltage (and hence current) TC is much lower at ±40ppm/°C max (AD1403). Therefore, the overall temperature coefficient decreases rapidly as the load current is increased. Figure 10b shows the typical temperature coefficient for currents between 1.5mA and 10mA. Use of an AD1403A will not improve the TC appreciably.

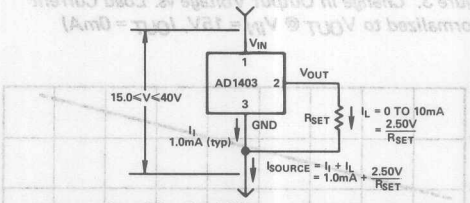


Figure 8a. The AD1403 as a Precision Programmable Current Source

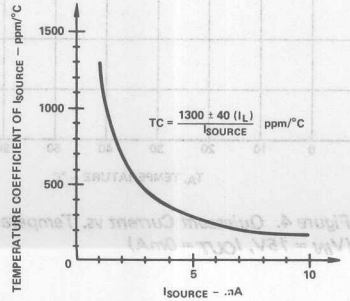


Figure 8b. Typical Temperature Coefficient of Current Source

ANALOG DEVICES

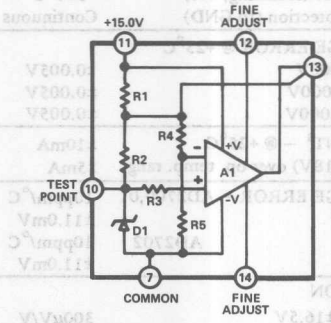
±10 Volt Precision Reference Series

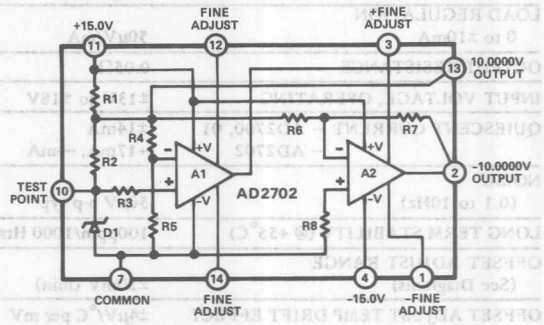
AD2700/AD2701/AD2702

FEATURES

- Very High Accuracy: 10.000 Volts ±2.5mV (L and U)
- Low Temperature Coefficient: 3ppm/°C
- Performance Guaranteed -55°C to +125°C
- 10mA Output Current Capability
- Low Noise
- Short Circuit Protected
- Available as /883B

FUNCTIONAL BLOCK DIAGRAMS





PRODUCT DESCRIPTION

The AD2700 family of precision 10 volt references offer the user excellent accuracy and stability at a moderate price by combining the recognized advantages of thin film technology and active laser trimming. The low temperature drift (3ppm/°C) achieved with these technologies can be matched only by the use of ovens, chip heaters for temperature regulation, or with hand selected components and manual trimming. In addition, temperature-regulated devices are guaranteed only up to +85°C operation, whereas the U- and S-grade devices in the AD2700 family are guaranteed to +125°C.

The AD2700 is a +10 volt reference which is designed to interface with high accuracy bipolar D/A converters of 10 and 12 bit resolution. The 10mA output drive capability also makes the AD2700 ideal for use as a general positive system reference.

The AD2701 is a negative 10 volt reference especially designed to interface with CMOS D/A and A/D converters, as shown in the applications. For systems requiring a dual tracking reference, the AD2702 offers both positive and negative precision 10 volt outputs in a single package. Both are often used with 52XX Series 12-bit A/D converters which require -10V external references for high accuracy over wide temperature ranges.

All three devices are offered in "J" and "L" grades for operation from -25°C to +85°C and "S" and "U" grades for the -55°C to +125°C temperature range. Screening to MIL-STD-883 is available for "S" and "U" grades of the AD2700 family.

PRODUCT HIGHLIGHTS

1. Active laser trimming of both initial accuracy and temperature performance results in very high accuracy over the temperature range without external components. The AD2700/01/02 LD grades have a maximum output voltage error at 25°C of ±2.5mV with no external adjustments.
2. The performance of the AD2700 series is achieved by a well-characterized design and precise control over the manufacturing process.
3. The AD2700 series is well suited for a broad range of applications requiring an accurate, stable reference source such as high resolution data converters (12 or 14 bits), test and measurement systems and calibration standards.

Model	Output
AD2700	+10.000V
AD2701	-10.000V
AD2702	±10.000V

6

AD2700/AD2701/AD2702—SPECIFICATIONS (max or min @ E_{IN} ±15V @ +25°C, R_L = 2kΩ unless otherwise noted.)

MODEL	JD	LD	SD	UD
ABSOLUTE MAX RATINGS				
Input Voltage (for applicable supply)	±20V	*	*	*
Power Dissipation @ +25°C – AD2700, 01	300mW	*	*	*
– AD2702	450mW	*	*	*
Operating Temperature Range	-25°C to +85°C	*	-55°C to +125°C	***
Storage Temperature Range	-65°C to +150°C	*	*	*
Lead Temperature (soldering, 10s)	+300°C	*	*	*
Short Circuit Protection (to GND)	Continuous	*	*	*
OUTPUT VOLTAGE ERROR @ +25°C				
AD2700 10.000V	±0.005V	±0.0025V	*	**
AD2701 -10.000V	±0.005V	±0.0025V	*	**
AD2702 ±10.000V	±0.005V	±0.0025V	*	**
OUTPUT CURRENT[1] – @ +25°C	±10mA	*	*	*
(V_{IN} = ±13 to ±18V) over op. temp. range	±5mA	+5mA, -2mA	**	**
OUTPUT VOLTAGE ERROR – AD2700,01	10ppm/°C	3ppm/°C	**	**
(T_{min} to T_{max})[2]	±11.0mV	±4.3mV	±8mV	±5.5mV
AD2702	10ppm/°C	5ppm/°C	**	3ppm/°C
	±11.0mV	±5.5mV	±10.0mV	±5.5mV
LINE REGULATION				
V_{IN} = ±13.5 to ±16.5V	300μV/V	*	*	*
LOAD REGULATION				
0 to ±10mA	50μV/mA	*	*	*
OUTPUT RESISTANCE	0.05Ω	*	*	*
INPUT VOLTAGE, OPERATING	±13V to ±18V	*	*	*
QUIESCENT CURRENT – AD2700, 01	±14mA	*	*	*
– AD2702	+17mA, -4mA	*	*	*
NOISE				
(0.1 to 10Hz)	50μV p-p typ	*	*	*
LONG TERM STABILITY (@ +55°C)	100ppm/1000 Hrs. (typ)	*	*	*
OFFSET ADJUST RANGE				
(See Diagrams)	±20mV (min)	*	*	*
OFFSET ADJUST TEMP DRIFT EFFECT	±4μV/°C per mV of Adjust (typ)	*	*	*
PACKAGE OPTION[3,4]	DH-14C	DH-14C	DH-14C	DH-14C

NOTES
*Same as "JD" grade performance.
**Same as "LD" grade performance.
***Same as "SD" grade performance.

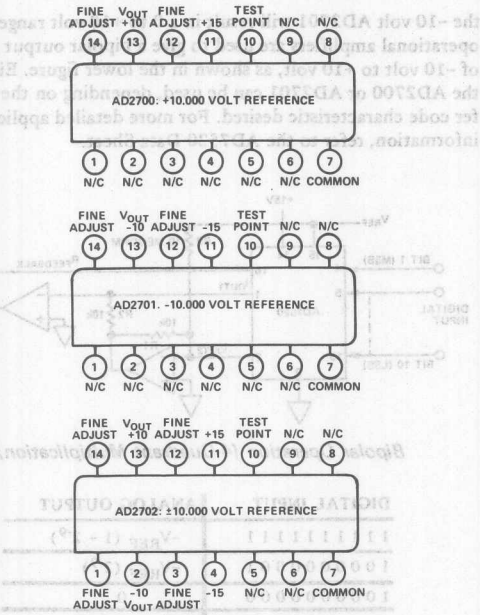
[1] Specified with resistive load to common. Device not intended for use in driving a dynamic load.

[2] Output voltage error as a function of temperature is determined using the box method. Each unit is tested at T_{min}, T_{max} and +25°C. At each temperature V_{OUT} must fall within the rectangular area bounded by the minimum and maximum temperature and whose maximum V_{OUT} value is equal to V_{OUT} nominal plus or minus the maximum +25°C error plus the maximum drift error from +25°C. The box limits are noted below the drift values used to calculate the box.

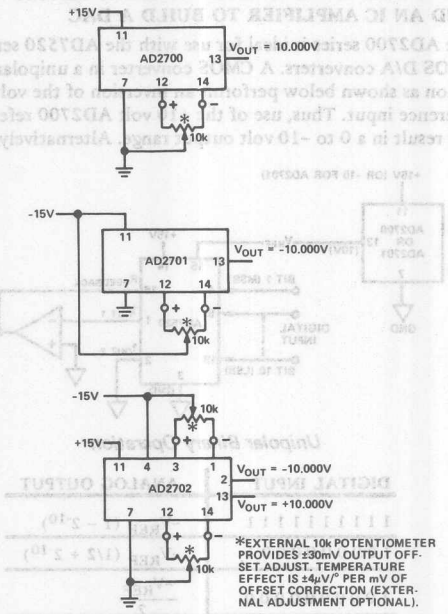
[3] Analog Devices reserves the right to ship side-brazed ceramic packages (outline DH-14D) in lieu of the standard ceramic packages for J and L grade parts.

[4] For outline information, see Package Information section.

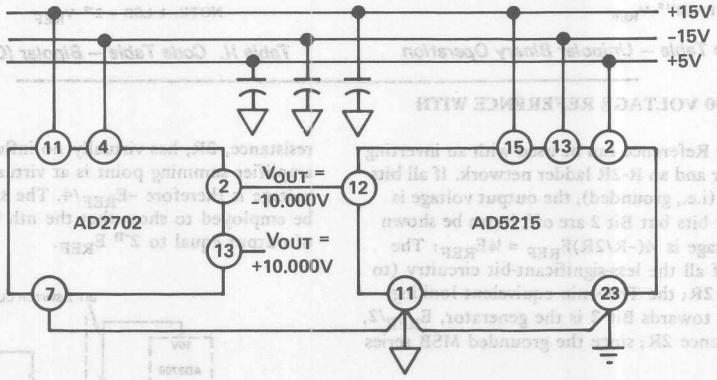
Specifications subject to change without notice.



Pin Designations



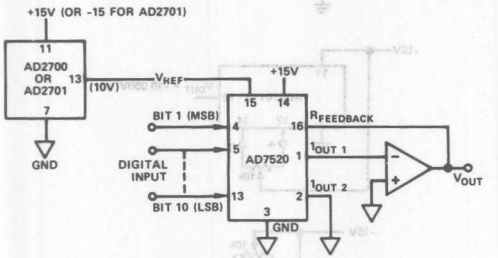
Fine Trim Connections



Using AD2702 Reference with the Fast, High Accuracy AD5215 – 12-Bit ADC

USING AD2700 REFERENCE WITH THE AD7520 AND AN IC AMPLIFIER TO BUILD A DAC

The AD2700 series is ideal for use with the AD7520 series of CMOS D/A converters. A CMOS converter in a unipolar application as shown below performs an inversion of the voltage reference input. Thus, use of the +10 volt AD2700 reference will result in a 0 to −10 volt output range. Alternatively, using the −10 volt AD2701 will result in a 0 to +10 volt range. Two operational amplifiers are used to give a bipolar output range of −10 volt to +10 volt, as shown in the lower figure. Either the AD2700 or AD2701 can be used, depending on the transfer code characteristic desired. For more detailed applications information, refer to the AD7520 Data Sheet.

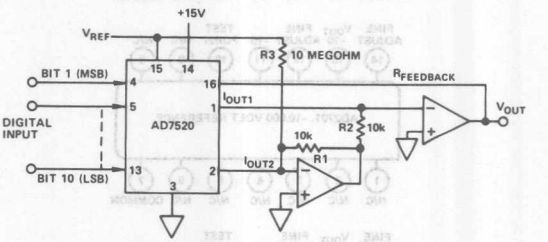


Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (1/2 + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$\frac{-V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1/2 - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

NOTE: 1 LSB = 2^{-10} V_{REF}

Table I. Code Table — Unipolar Binary Operation



Bipolar Operation (4-Quadrant Multiplication)

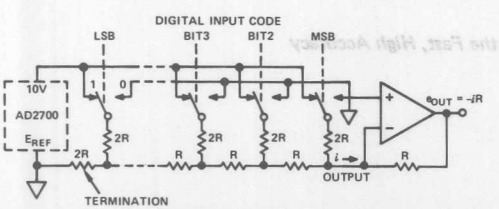
DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}\ (2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}\ (1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

NOTE: 1 LSB = 2^{-9} V_{REF}

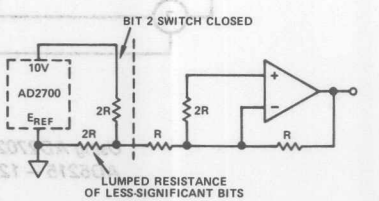
Table II. Code Table — Bipolar (Offset Binary) Operation

USING THE AD2700 VOLTAGE REFERENCE WITH D/A CONVERTER

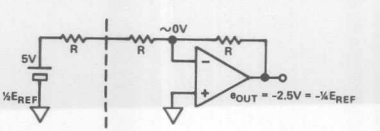
An AD2700 Voltage Reference can be used with an inverting operational amplifier and an R-2R ladder network. If all bits but the MSB are off (i.e., grounded), the output voltage is $(-R/2R)E_{REF}$. If all bits but Bit 2 are off, it can be shown that the output voltage is $\frac{1}{2}(-R/2R)E_{REF} = \frac{1}{4}E_{REF}$: The lumped resistance of all the less-significant-bit circuitry (to the left of Bit 2) is 2R; the Thevenin equivalent looking back from the MSB towards Bit 2 is the generator, $E_{REF}/2$, and the series resistance 2R; since the grounded MSB series resistance, 2R, has virtually no influence — because the amplifier summing point is at virtual ground — the output voltage is therefore $-E_{REF}/4$. The same line of thinking can be employed to show that the nth bit produces an increment of output equal to 2^{-n} E_{REF}.



a. Basic Circuit



b. Example: Contribution of Bit 2; All Other Bits "0"



c. Simplified Equivalent of Circuit (b.)

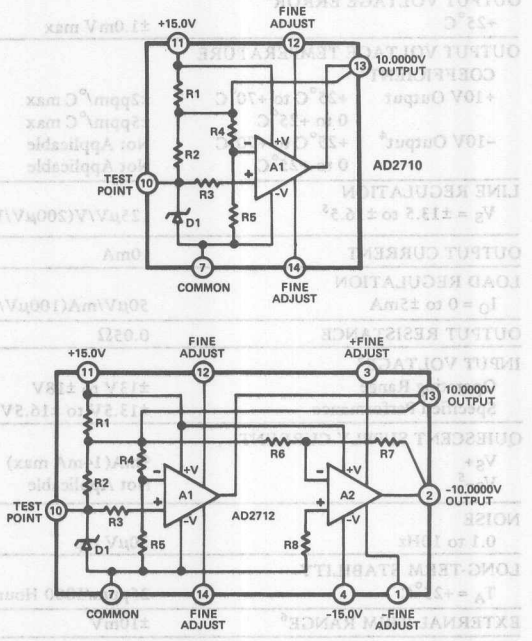
±10.000 Volt Ultrahigh Precision Reference Series

AD2710/AD2712

FEATURES

Laser Trimmed to High Accuracy: 10.000V ± 1.0mV
Low Temperature Coefficient: 1ppm/°C (L Grade)
Excellent Long Term Stability: 25ppm/1000hrs.
5mA Output Current Capability
Low Noise: 30μV p-p
Short Circuit Protected
No Heater Utilized
Small Size (Standard 14-Pin DIP Package)

FUNCTIONAL BLOCK DIAGRAMS



PRODUCT DESCRIPTION

The AD2710 and AD2712 are temperature-compensated, hybrid voltage references which provide precise 10.000V output from an unregulated input level from 13.5 to 16.5 volts. Active laser trimming is used to trim both the initial error at +25°C as well as the temperature coefficient, which results in ultra high precision performance previously available only in oven-regulated modules. The 1.0mV maximum initial error and 1ppm/°C guaranteed maximum temperature coefficient of the AD2710L and AD2712L represent the best performance combination available without using ovens or heated substrates for temperature regulation.

The AD2710 series of precision 10.000 volt references offer the user unequalled accuracy and stability with performance guaranteed over the 0 to +70°C temperature range. The devices combine the recognized advantages of thin film technology and active laser trimming with a unique integrated ceramic package design to provide an excellent reference for use in applications requiring high accuracy and stability.

The AD2710 is recommended for use as a reference for 10-, 12- and 14-bit D/A converters which require an external reference. The device is also suitable for many types of high resolution A/D converters, either successive approximation or integrating designs. The 5mA output drive capability of the device also makes the AD2710 ideal for use as a master system reference.

For systems requiring a dual tracking reference, the AD2712 offers both positive and negative outputs in a single package. All units are packaged in an integrated ceramic 14-pin side-brazed package offering superior reliability over other package designs.

PRODUCT HIGHLIGHTS

1. Active laser trimming of both initial accuracy and temperature coefficient results in very high accuracy over the temperature range without the use of external components. AD2710 has a maximum deviation from 10.000 volts of ±1.00mV at 25°C with no external adjustments.
2. The AD2710 and AD2712 are well suited for a broad range of applications requiring an accurate, stable reference source such as data converters, test and measurement systems and calibration standards.
3. The performance of the AD2710 series is achieved by a well-characterized design and close control over the manufacturing process. This eliminates the need for temperature-controlled ovens to provide stability.
4. The advanced multilayer integrated ceramic package results in superior electrical performance as well as inherent high reliability.

AD2710/AD2712—SPECIFICATIONS (typical @ V_S ±15V after a 5 minute warm-up at +25°C, no load condition unless otherwise specified)

Model		AD2710KN	AD2710LN	AD2712KN	AD2712LN
ABSOLUTE MAXIMUM RATINGS					
Input Voltage (for applicable supply)		±18V	*	*	*
Power Dissipation @ +25°C		300mW	*	450mW	**
Operating Temperature Range		0 to +70°C	*	*	*
Storage Temperature Range		−55°C to +100°C	*	*	*
Lead Temperature (soldering, 20s)		+260°C	*	*	*
Short Circuit Protection (to GND)		Continuous	*	*	*
OUTPUT VOLTAGE ERROR[1]					
+25°C		±1.0mV max	*	*	*
OUTPUT VOLTAGE TEMPERATURE COEFFICIENT[2]					
+10V Output	+25°C to +70°C	±2ppm/°C max	±1ppm/°C max	±2ppm/°C max	±1ppm/°C max
	0 to +25°C	±5ppm/°C max	*[3]	*	*[3]
−10V Output[4]	+25°C to +70°C	Not Applicable	Not Applicable	±3ppm/°C max	±2ppm/°C max
	0 to +25°C	Not Applicable	Not Applicable	±5ppm/°C max	**
LINE REGULATION					
V_S = ±13.5 to ±16.5[5]		125μV/V(200μV/V max)	*	*	*
OUTPUT CURRENT		10mA	*	*	*
LOAD REGULATION					
I_O = 0 to ±5mA		50μV/mA(100μV/mA max)	*	*	*
OUTPUT RESISTANCE		0.05Ω	*	*	*
INPUT VOLTAGE[5]					
Operating Range		±13V to ±18V	*	*	*
Specified Performance		±13.5V to ±16.5V	*	*	*
QUIESCENT SUPPLY CURRENT					
V_S+		9mA(14mA max)	*	12mA (16mA max)	**
V_S−[5]		Not Applicable	Not Applicable	2mA (4mA max)	**
NOISE					
0.1 to 10Hz		30μV p-p	*	*	*
LONG-TERM STABILITY					
T_A = +25°C		25ppm/1000 Hours	*	*	*
EXTERNAL TRIM RANGE[6]		±10mV	*	*	*
PACKAGE OPTION[7]		DH-14D	*	*	*

NOTES
*Same as AD2710KN. **Same as AD2712KN performance.
[1] Specifications apply to both outputs of the AD2712.
[2] Refer to next page for definition of temperature-related error specifications.
[3] The AD2710LN and AD2712LN outputs are guaranteed for a maximum ±2ppm/°C temperature coefficient over the +15°C to +25°C temperature range. Refer to Figure 1.
[4] The +10V and −10V outputs of the AD2712 typically track within ±1ppm/°C over the specified temperature range.
[5] Negative power supply not required for AD2710.
[6] Use of the output trim will change the temperature coefficient approximately 0.3ppm/°C for each millivolt of adjustment.
[7] For outline information see Package Information section.

Specifications subject to change without notice.

UNDERSTANDING THE SPECIFICATIONS

The AD2710 and AD2712 precision references are designed for applications requiring both the lowest possible initial error at room temperature and the lowest possible temperature drift. The specification for initial error is relatively straight-forward, and is the absolute error from exactly 10.000V. The specification for temperature drift, however, must be explained.

Various methods have been used to specify the temperature drift of voltage references, including the "butterfly", "box", and "modified-box" (or total error) methods. The AD2710 and AD2712 are specified with the "butterfly" method.

Using three or more temperatures provides the user with a tighter drift specification, eliminating possible mid-range excursions. The AD2710 and AD2712 have been designed and characterized as having a smooth drift curve with a virtually straight segment from +25°C to +70°C. The typical curve as shown is concave downward and gradually increases slope near 0°C.

As can be seen from Figure 1, the AD2710L and AD2712L +10V outputs will exhibit a maximum temperature coefficient of ±1ppm/°C (±2ppm/°C for "K" grade) from +25°C to +70°C. Over the short range between +15°C and +25°C, the AD2710L and AD2712L +10V outputs have a maximum drift of only ±2ppm/°C and a maximum drift of ±5ppm/°C from 0 to +15°C. The negative output of the AD2712L has a similar temperature coefficient characteristic with a maximum slope of ±2ppm/°C from +25°C to +70°C. This limit continues from +25°C to +15°C and then increases to a ±5ppm/°C maximum slope from +15°C and 0°C. Every unit is 100 percent tested and guaranteed to meet these specifications over the full 0 to +70°C temperature range.

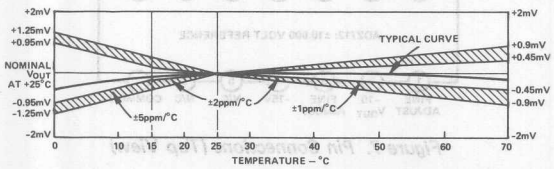


Figure 1. Maximum Change from +10V Output from +25°C Value vs. Temperature

All grades of the AD2710 and AD2712 are tested after a five minute warm-up period. This warm-up allows the entire circuit to attain thermal equilibrium. The warm-up drift is approximately 500 microvolts and is completely settled approximately three minutes after turn-on. Figure 2 shows the typical warm-up characteristics of the AD2710.

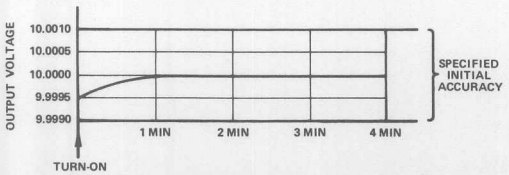


Figure 2. AD2710 Typical Warm-Up Drift

USING THE AD2710 AS A DAC REFERENCE

Digital-to-analog converters require a reference to establish the full scale output range. It is this reference which will ultimately determine the absolute accuracy of the converter. While many converters include internal reference sources, better overall performance can be obtained if a higher precision external reference is used.

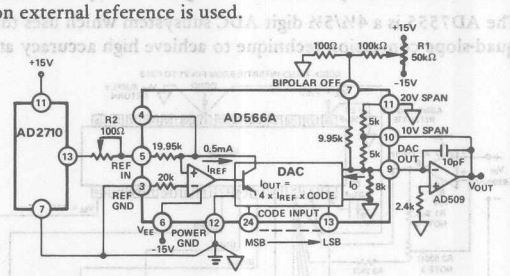


Figure 3. Low Drift 12-Bit D/A Converter

Figure 3 shows the AD2710 used with the AD566A high-speed 12-bit DAC. The AD566AKD is laser trimmed for ±1/4LSB maximum nonlinearity, and exhibits a gain temperature coefficient of 3ppm/°C. Use of the AD2710LN reference will result in a worst case total gain temperature coefficient of 4ppm/°C. After initial calibration of the DAC scale factor at room temperature, 12-bit absolute accuracy can be maintained over the +15°C to +70°C temperature range. The high output current capability of the AD2710 allows it to serve as a reference for up to 10 such converters in a system.

The resolution of the AD566A can be extended as shown in Figure 3 by summing the output of another DAC. In this example, an AD559 is used to provide 4 additional bits. Since the AD559 is driven from the same AD2710 reference as the AD566A which provides the higher-order bits, and uses a similar internal thin-film resistor ladder, it will exhibit first-order temperature tracking. While this circuit provides 16-bits of resolution, it is only as accurate as the AD566A used for the most significant bits. Use of an AD566AKD will typically achieve ±0.003% accuracy (±1/2LSB at 14 bits).

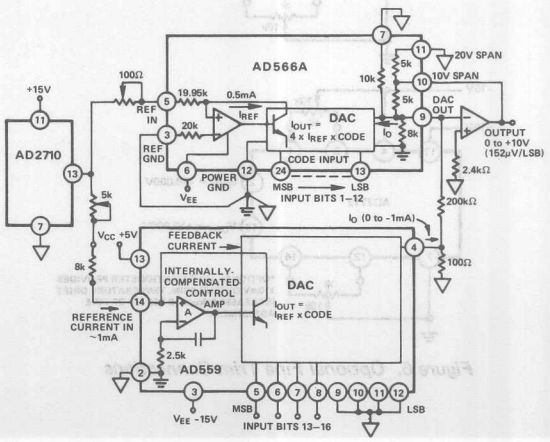
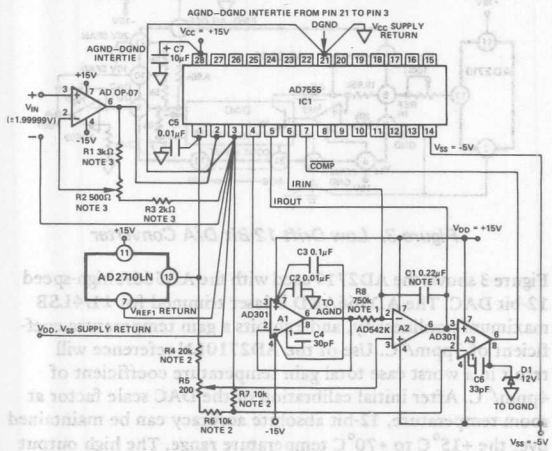


Figure 4. 16-Bit Binary DAC with AD2710 Reference

lent absolute accuracy and low temperature drift allow low-cost measurement systems to offer high levels of performance.

The AD7555 is a 4½/5½ digit ADC subsystem which uses the quad-slope conversion technique to achieve high accuracy at



NOTES:
1. R8 C1 VALUES SHOWN ARE FOR 5 1/2 DIGIT MODE. FOR 4 1/2 DIGIT MODE R_8 = 360k, C_1 = 0.22μF. SUITABLE CAPACITORS AVAILABLE FROM COMPONENT RESEARCH CO. INC., 1655 26th STREET, SANTA MONICA, CA, 90404. (STOCK NUMBER FOR 0.22μF CAPACITOR IS D11B224KXW).
2. R4, R6, R7 1% TOLERANCE.
3. R1, R3 SHOULD TRACK WITHIN 0.5ppm/°C. EITHER BULK METAL OR WIRE-WOUND RESISTORS (OR A THIN-FILM NETWORK) SHOULD BE USED. R2 SHOULD BE A LOW-TC TYPE POTENTIOMETER OR A SELECTED LOW DRIFT FIXED RESISTOR.

Figure 5. High Accuracy Low Drift A/D Converter

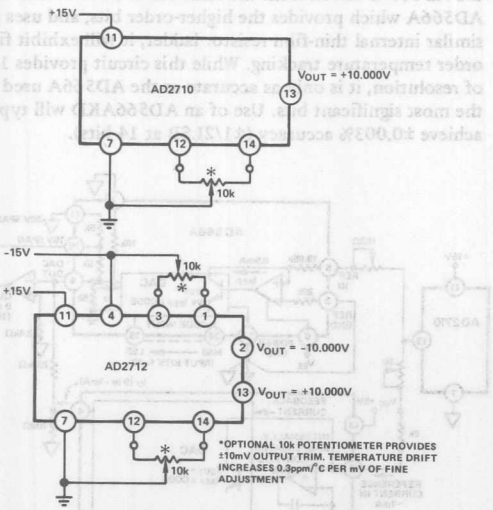


Figure 6. Optional Fine Trim Connections

1.2ppm/°C is possible using the AD2710L reference and medium-precision external amplifiers. This represents a full scale drift of less than ±10 counts in ±200,000 from +15°C to +45°C. Less than 1 count of drift will occur in the 4 1/2 digit mode.

The AD7555 was designed for use with a 4.096V reference, which produces a ±2 volt input range. When the AD2710 is used, the input range is increased to ±4.88281V (24.4μV/count). The new scaling can be handled either by using a precision gain stage before the AD7555 analog input as shown or by using a microprocessor to digitally correct the scale. The actual input signal value can be computed by multiplying the count produced by the AD7555 by V_{REF1} (10 volts in this case), and dividing the result by 409600. Details of the digital circuitry of the AD7555 can be found on the AD7555 data sheet.

It should be noted that when the AD7555 is used with the AD2710 10 volt reference, it is necessary to use a V_{CC} greater than 10 volts. Thus the digital inputs and outputs of the ADC will be compatible with CMOS logic levels.

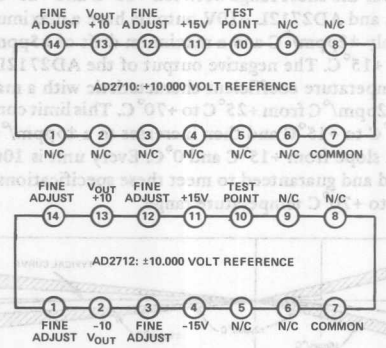


Figure 7. Pin Connections (Top View)

FEATURES

- **10 Volt Output** ..... **±0.3% Max**
- **Adjustment Range** ..... **±3% Min**
- **Excellent Temperature Stability** ..... **8.5ppm/°C Max**
- **Low Noise** ..... **30μV_{p-p} Max**
- **Low Supply Current** ..... **1.4mA Max**
- **Wide Input Voltage Range** ..... **12V to 40V**
- **High Load-Driving Capability** **20mA**
- **No External Components**
- **Short-Circuit Proof**
- **MIL-STD-883 Screening Available**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = 25°C	PACKAGE				OPERATING
ΔV_{OS} MAX (mV)	TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	TEMPERATURE RANGE
±30	REF01AJ*	REF01AZ*	—	—	MIL
±30	REF01EJ	REF01EZ	—	—	COM
±50	REF01J*	REF01Z*	—	REF01RC/883	MIL
±50	REF01HJ	REF01HZ	REF01HP	—	COM
±100	REF01CJ	REF01CZ	—	—	COM
±100	—	—	REF01CP	—	XIND
±100	—	—	REF01CS††	—	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

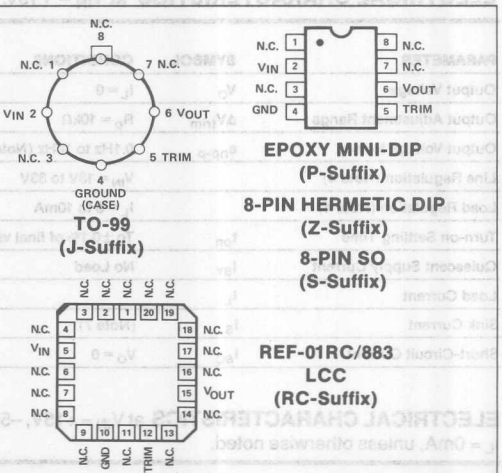
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

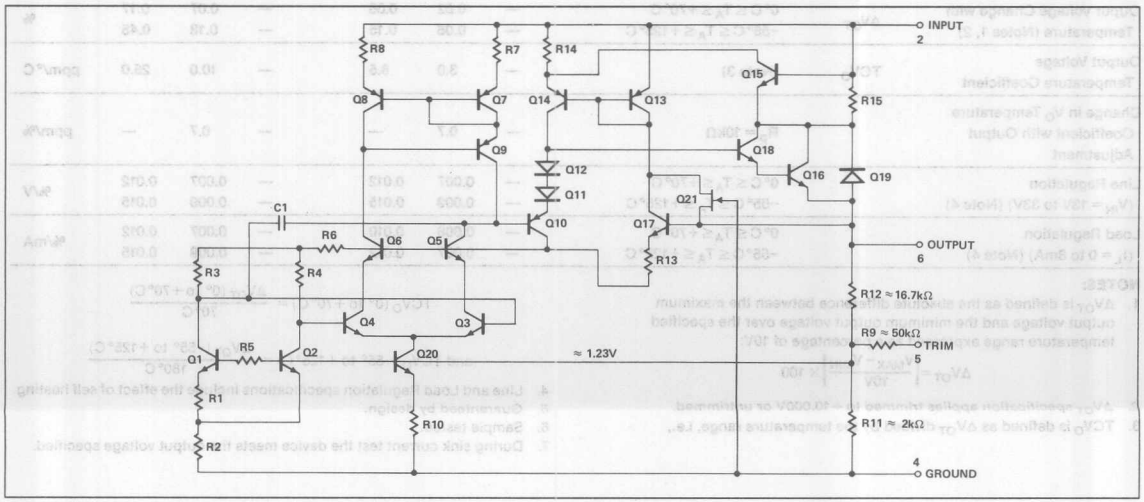
GENERAL DESCRIPTION

The REF-01 precision voltage reference provides a stable +10V output which can be adjusted over a ±3% range with minimal effect on temperature stability. Single-supply operation over an input voltage range of 12V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-01 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. Full military temperature range devices with screening to MIL-STD-883 are available. For guaranteed long-term drift see the REF-10 data sheet.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



6

REF-01

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage
- REF-01, A, E, H, RC, All DICE 40V
- REF-01C 30V

Output Short-Circuit Duration
- (to Ground or V_{IN}) ..... Indefinite

Storage Temperature Range
- J, RC, and Z Packages ..... –65° C to +150°C
- P Package ..... –65°C to +125°C

Operating Temperature Range
- REF-01A, REF-01, REF-01RC ..... –55°C to +125°C
- REF-01E, REF-01H, REF-01CJ, REF-01CZ ..... 0°C to +70°C
- REF-01CP, REF-01CS ..... –40°C to +85°C

Junction Temperature (T_j) ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
TO-99 (J)	170	24	°C/W
8-Pin Hermetic DIP (Z)	162	26	°C/W
8-Pin Plastic DIP (P)	110	50	°C/W
20-Contact LCC (RC)	120	40	°C/W
8-Pin SO (S)	160	44	°C/W
20-Contact PLCC (PC)	80	39	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO and PLCC packages.

ELECTRICAL CHARACTERISTICS at V_{IN} = +15V, T_A = 25° C, unless otherwise noted.

			REF-01A/E			REF-01/H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Output Voltage	V_O	I_L = 0	9.97	10.00	10.03	9.95	10.00	10.05	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3.0	±3.3	—	±3.0	±3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 6)	—	20	30	—	20	30	μV_{p-p}
Line Regulation (Note 4)		V_{IN} = 13V to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 4)		I_L = 0 to 10mA	—	0.005	0.008	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S	(Note 7)	−0.3	−0.5	—	−0.3	−0.5	—	mA
Short-Circuit Current	I_{SC}	V_O = 0	—	30	—	—	30	—	mA

ELECTRICAL CHARACTERISTICS at V_{IN} = +15V, –55°C ≤ T_A ≤ +125°C for REF-01 A/E, and 0°C ≤ T_A ≤ +70°C for REF-01 H and I_L = 0mA, unless otherwise noted.

			REF-01A/E			REF-01/H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Ouput Voltage Change with Temperature (Notes 1, 2)	ΔV_{OT}	0°C ≤ T_A ≤ +70°C	—	0.02	0.06	—	0.07	0.17	%
		−55°C ≤ T_A ≤ +125°C	—	0.06	0.15	—	0.18	0.45	
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	3.0	8.5	—	10.0	25.0	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (V_{IN} = 13V to 33V) (Note 4)		0°C ≤ T_A ≤ +70°C	—	0.007	0.012	—	0.007	0.012	%/V
		−55°C ≤ T_A ≤ +125°C	—	0.009	0.015	—	0.009	0.015	
Load Regulation (I_L = 0 to 8mA) (Note 4)		0°C ≤ T_A ≤ +70°C	—	0.006	0.010	—	0.007	0.012	%/mA
		−55°C ≤ T_A ≤ +125°C	—	0.007	0.012	—	0.009	0.015	

NOTES:
1. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{10V} \right| \times 100$$

2. ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.
3. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O\,(0° \text{ to } +70°C) = \frac{\Delta V_{OT}\,(0° \text{ to } +70°C)}{70°C}$$

$$\text{and } TCV_O\,(-55° \text{ to } +125°C) = \frac{\Delta V_{OT}\,(-55° \text{ to } +125°C)}{180°C}$$

4. Line and Load Regulation specifications include the effect of self heating.
5. Guaranteed by design.
6. Sample tested.
7. During sink current test the device meets the output voltage specified.

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-01C MIN	REF-01C TYP	REF-01C MAX	UNITS
Output Voltage	V_O	$I_L = 0mA$	9.90	10.00	10.10	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	±2.7	±3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 6)	—	25	35	μV_{p-p}
Line Regulation (Note 4)		$V_{IN} = 13V$ to 30V	—	0.009	0.015	%/V
Load Regulation (Note 4)		$I_L = 0$ to 8mA	—	0.006	0.015	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.6	mA
Load Current	I_L		8	21	—	mA
Sink Current	I_S	(Note 7)	−0.3	−0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	—	30	—	mA

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V°C \le T_A \le +70°C$ for REF-01CJ, CZ, $-40°C \le T_A \le +85°C$ for REF-01CP,CS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-01C MIN	REF-01C TYP	REF-01C MAX	UNITS
Ouput Voltage Change with Temperature	ΔV_{OT}	(Notes 1 and 2)	—	0.14	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	20	65	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		$R_p = 10k\Omega$	—	0.7	—	ppm/%
Line Regulation (Note 4)		$V_{IN} = 13V$ to 30V	—	0.011	0.018	%/V
Load Regulation (Note 4)		$I_L = 0$ to 5mA	—	0.008	0.018	%/mA

NOTES:

1. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

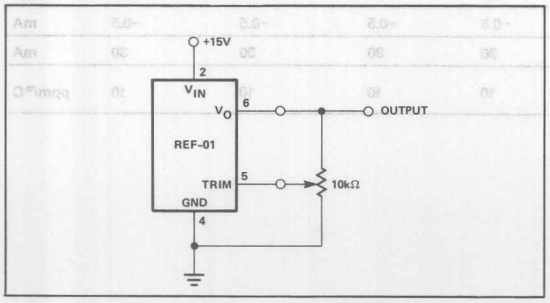
$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{10V} \right| \times 100$$

2. ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.
3. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

4. Line and Load Regulation specifications include the effect of self heating.
5. Guaranteed by design.
6. Sample tested.
7. During sink current test the device meets the output voltage specified.

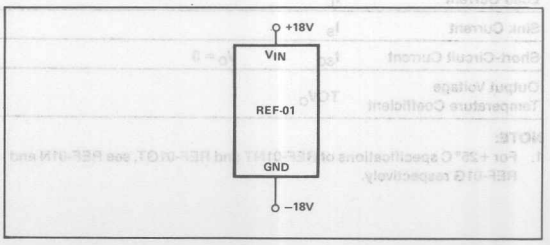
OUTPUT ADJUSTMENT

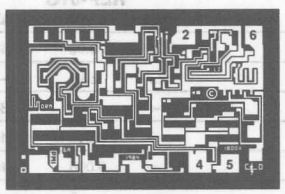


The REF-01 trim terminal can be used to adjust the output voltage over a 10V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V. Of course, the output can also be set to exactly 10.000V, or to 10.240V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately 0.7 ppm/° C for 100mV of output adjustment.

BURN-IN CIRCUIT





DIE SIZE 0.074 × 0.048 inch, 3552 sq. mils
(1.88 × 1.22 mm, 2.29 sq. mm)

2. INPUT VOLTAGE (V_{IN})
4. GROUND
5. TRIM
6. OUTPUT VOLTAGE (V_{OUT})

WAFER TEST LIMITS at $V_{IN} = +15V$, $T_A = 25°C$ for REF-01N and REF-01G devices; $T_A = 125°C$ for REF-01NT and REF-01GT devices, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	REF-01NT LIMIT	REF-01N LIMIT	REF-01GT LIMIT	REF-01G LIMIT	UNITS
Output Voltage	V_O	$I_L = 0$	10.05 9.95	10.03 9.97	10.10 9.90	10.05 9.95	V MAX V MIN
Output Adjustment Range	V_{trim}	$R_P = 10k\Omega$	—	±3.0	—	±3.0	% MIN
Line Regulation		$V_{IN} = 13V$ to 33V	0.015	0.01	0.015	0.01	%/V MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

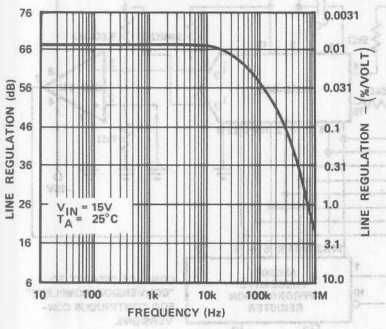
TYPICAL ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-01NT TYPICAL	REF-01N TYPICAL	REF-01GT TYPICAL	REF-01G TYPICAL	UNITS
Load Regulation		$I_L = 0$ to 10mA $I_L = 0$ to 8mA, NT, GT @ +125°C	0.007	0.005	0.009	0.006	%/mA
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz	20	20	20	20	μV_{p-p}
Turn-On Settling Time	t_{ON}	To ±0.1% of Final Value NT, GT @ +125°C	7.5	5.0	7.5	5.0	μs
Quiescent Current	I_{SY}	No Load, NT, GT @ +125°C	1.4	1.0	1.4	1.0	mA
Load Current	I_L		21	21	21	21	mA
Sink Current	I_S		−0.5	−0.5	−0.5	−0.5	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	30	30	30	30	mA
Output Voltage Temperature Coefficient	TCV_O		10	10	10	10	ppm/°C

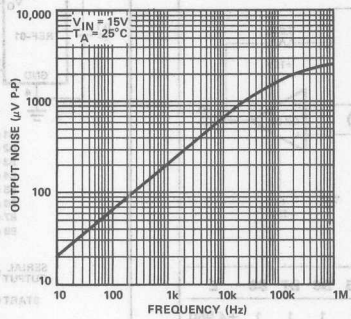
NOTE:
1. For +25°C specifications of REF-01NT and REF-01GT, see REF-01N and REF-01G respectively.

TYPICAL PERFORMANCE CHARACTERISTICS

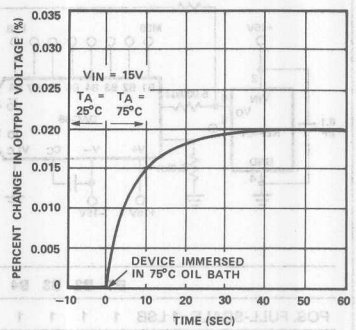
LINE REGULATION vs FREQUENCY



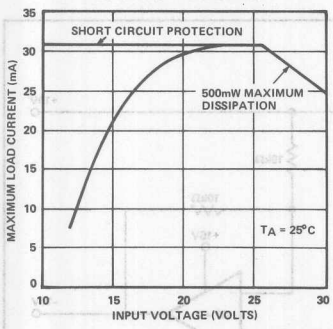
OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



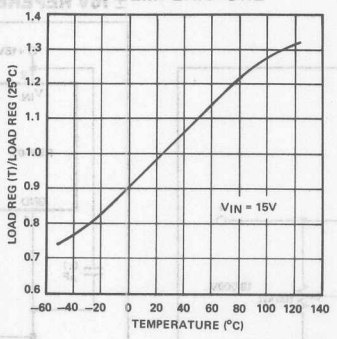
OUTPUT CHANGE DUE TO THERMAL SHOCK



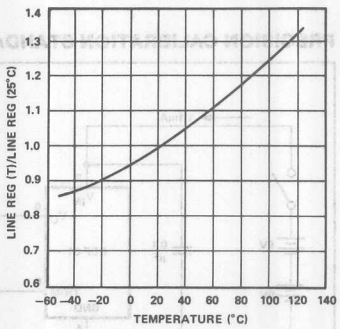
MAXIMUM LOAD CURRENT vs INPUT VOLTAGE



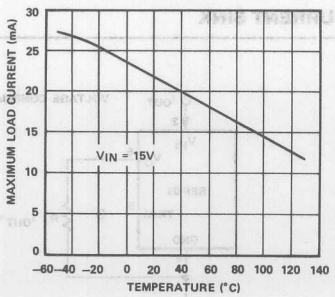
NORMALIZED LOAD REGULATION (ΔI_L = 10mA) vs TEMPERATURE



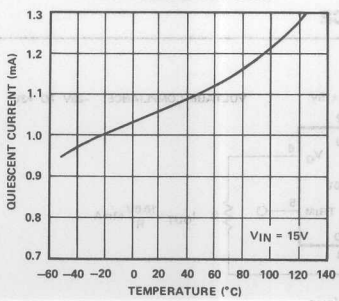
NORMALIZED LINE REGULATION vs TEMPERATURE



MAXIMUM LOAD CURRENT vs TEMPERATURE



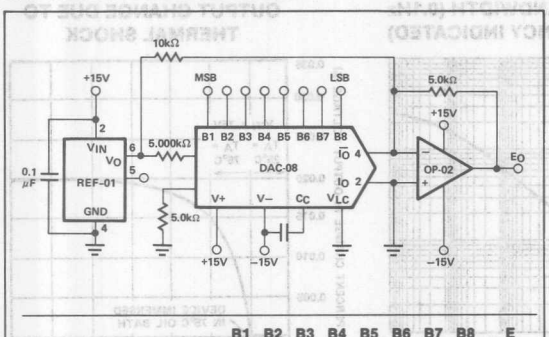
QUIESCENT CURRENT vs TEMPERATURE



6

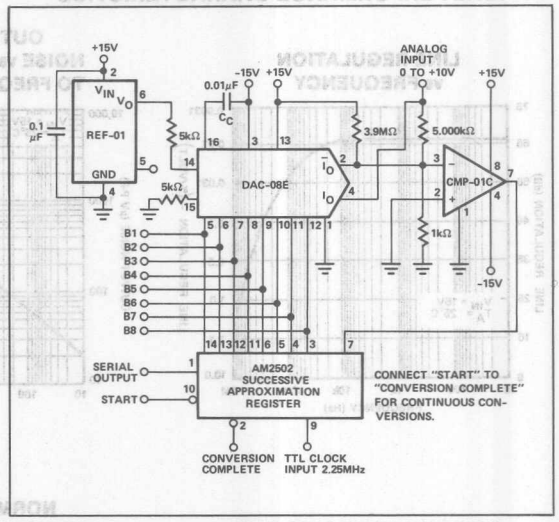
TYPICAL APPLICATIONS

D/A CONVERTER REFERENCE

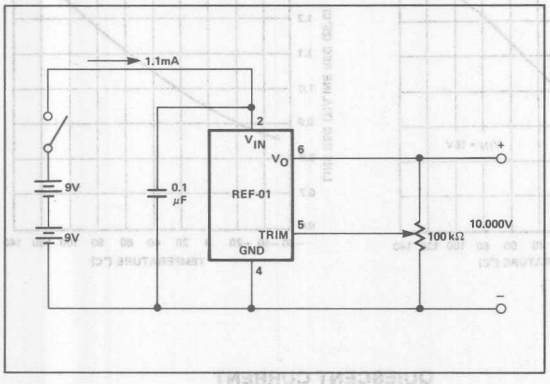


	B1	B2	B3	B4	B5	B6	B7	B8	E
POS. FULL-SCALE −1 LSB	1	1	1	1	1	1	1	1	+4.960
ZERO—SCALE	1	0	0	0	0	0	0	0	0.000
NEG. FULL-SCALE +1 LSB	0	0	0	0	0	0	0	1	−4.960
NEG. FULL-SCALE	0	0	0	0	0	0	0	0	−5.000

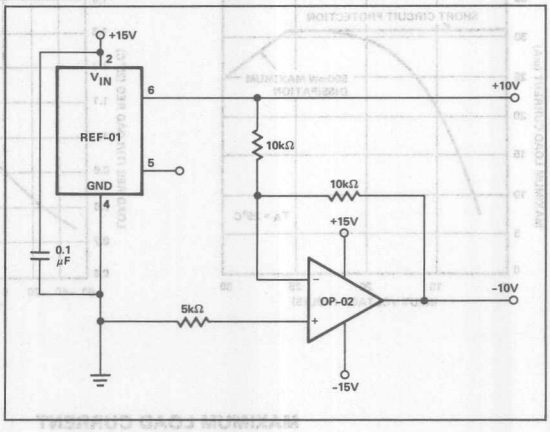
A/D CONVERTER REFERENCE



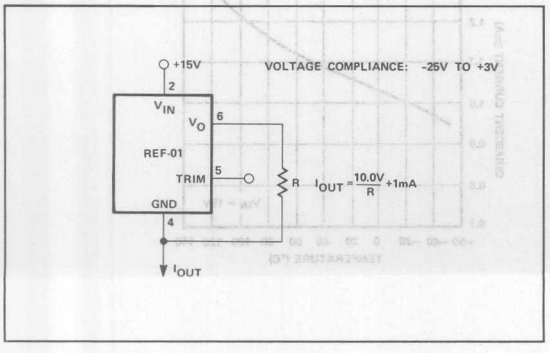
PRECISION CALIBRATION STANDARD



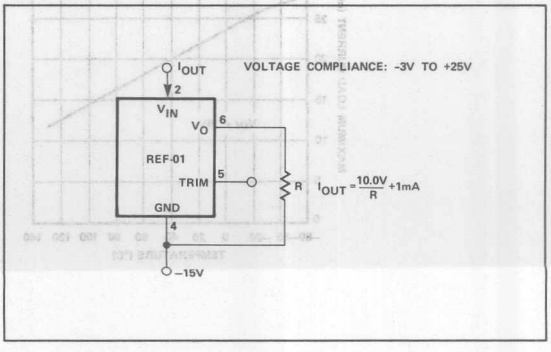
±10V REFERENCE



CURRENT SOURCE



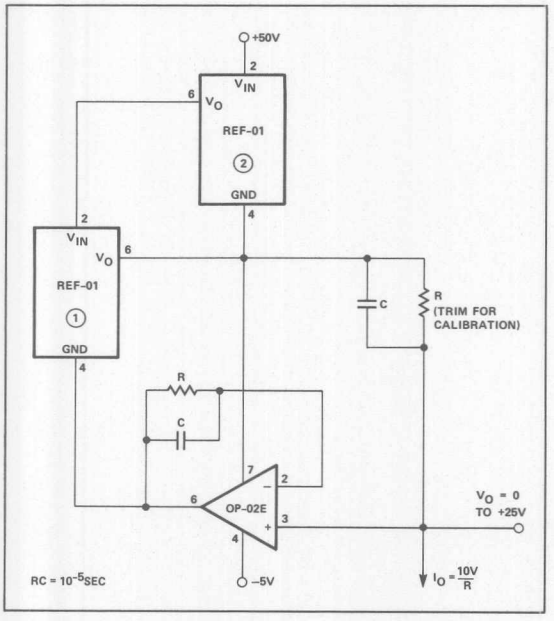
CURRENT SINK



PRECISION CURRENT SOURCE

A current source with 25V output compliance and excellent output impedance can be obtained using this circuit. REF-01 (2) keeps the line voltage and power dissipation constant in device (1); the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical 3μV/V PSRR of the OP-02E will create an 8ppm change (3μV/V × 25V/10V) in output current over a 25V range. For example, a 10mA current source can be built (R = 1kΩ) with 300MΩ output impedance.

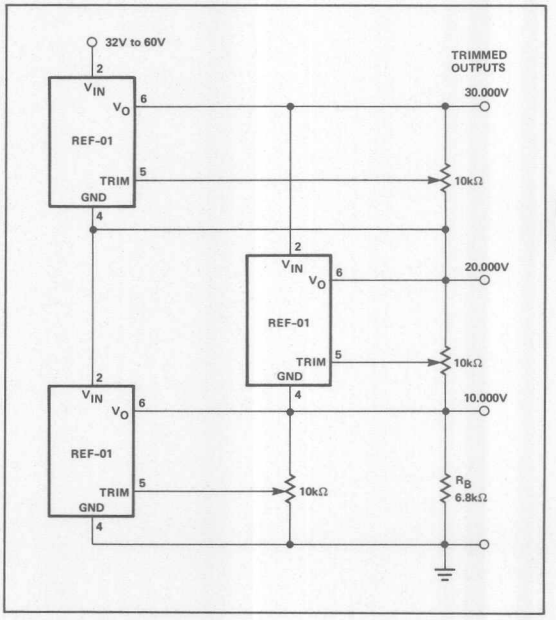
$$R_O = \frac{25V}{8 \times 10^{-6} \times 10mA}$$



REFERENCE STACK WITH EXCELLENT LINE REGULATION

Three REF-01's can be stacked to yield 10.000, 20.000, and 30.000V outputs. An additional advantage is near-perfect line regulation of the 10.0V and 20.0V output. A 32V to 60V input change produces an output change which is less than the noise voltage of the devices. A load bypass resistor (R_B) provides a path for the supply current (I_{SY}) of the 20.000V regulator.

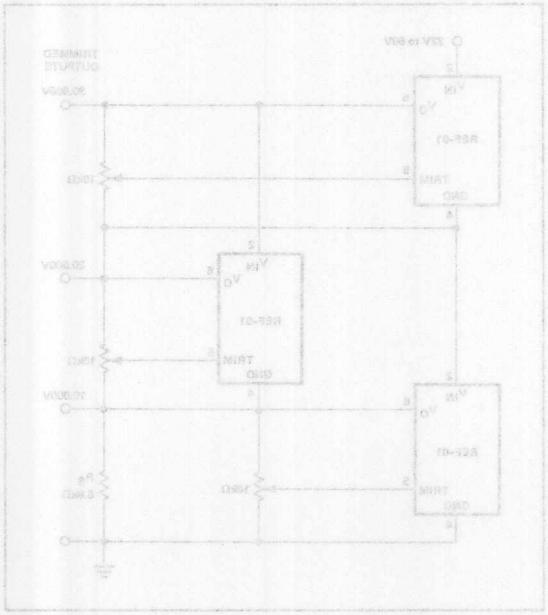
In general, any number of REF-01's can be stacked this way. For example, ten devices will yield outputs of 10, 20, 30 . . . 100V. The line voltage can range from 105V to 130V. However, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21mA).

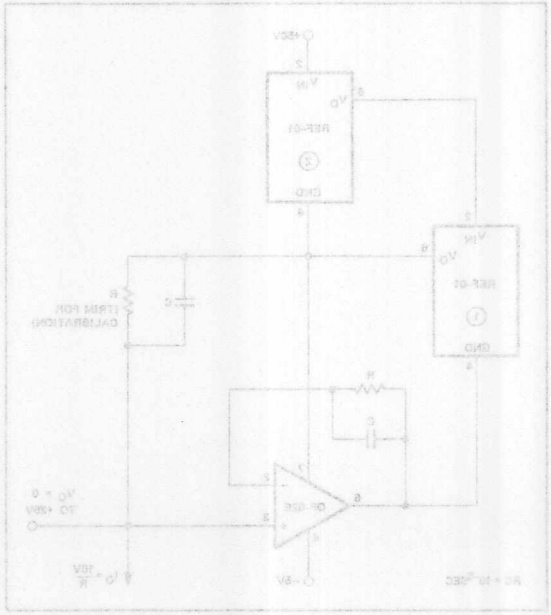


SUPPLY BYPASSING

For best results, it is recommended that the power supply pin is bypassed with a 0.1μF disc ceramic capacitor.

6





+5V Precision Voltage Reference/Temperature Transducer

REF-02

FEATURES

- 5 Volt Output ..... ±0.3% Max
- Temperature Voltage Output ..... 2.1mV/°C
- Adjustment Range ..... ±3% Min
- Excellent Temperature Stability ..... 8.5ppm/°C Max
- Low Noise ..... $15\mu V_{p-p}$ Max
- Low Supply Current ..... 1.4mA Max
- Wide Input Voltage Range ..... 7V to 40V
- High Load-Driving Capability 20mA
- No External Components
- Short-Circuit Proof
- MIL-STD-883 Screening Available
- Available in Die Form

GENERAL DESCRIPTION

The REF-02 precision voltage reference provides a stable +5V output which can be adjusted over a ±6% range with minimal effect on temperature stability. Single-supply operation over an input voltage range of 7V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-02 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. The versatility of the REF-02 is enhanced by its use as a monolithic temperature transducer. For +10V references, see the REF-01 and REF-10 data sheets.

ORDERING INFORMATION †

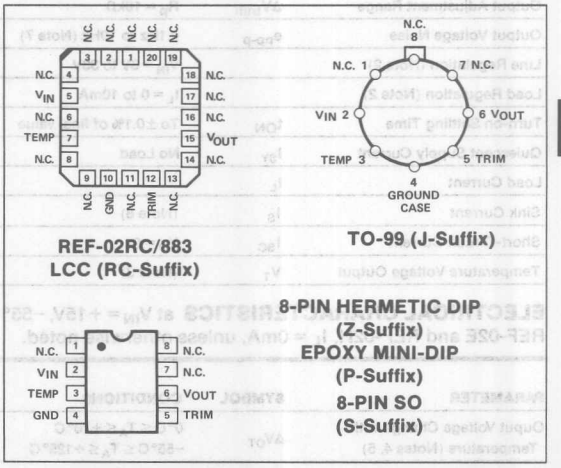
T_A = 25°C V_{OS} MAX (mV)	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
±15	REF02AJ*	REF02AZ*	–	–	MIL
±15	REF02EJ	REF02EZ	–	–	COM
±25	REF02J*	REF02Z*	–	REF02RC/883	MIL
±25	REF02HJ	REF02HZ	REF02HP	–	COM
±50	REF02CJ	REF02CZ	–	–	COM
±50	–	–	REF02CP	–	XIND
±50	–	–	REF02CS††	–	XIND
±100	REF02DJ	REF02DZ	REF02DP	–	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

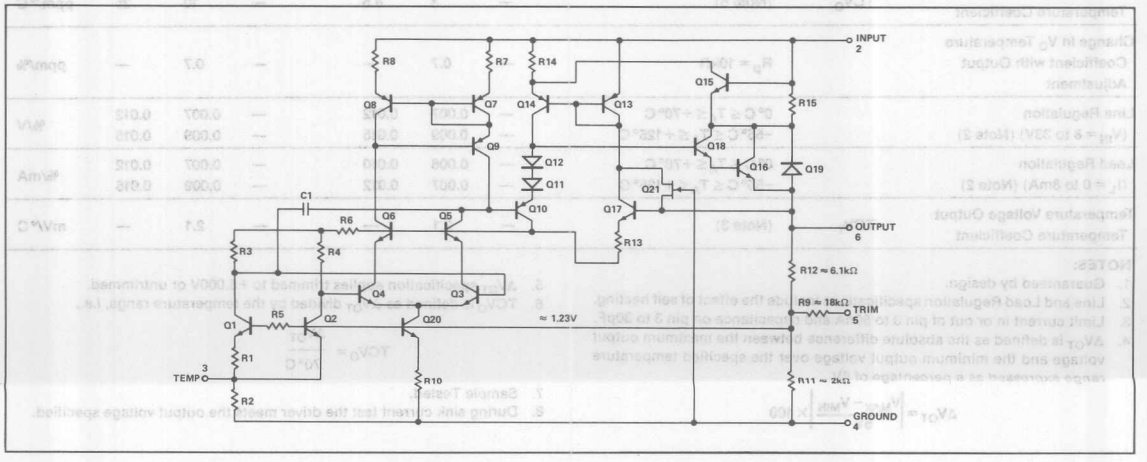
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



6

REF-02

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage
- REF-02A, E, H, RC, All DICE 40V
- REF-02C, D 30V

Output Short-Circuit Duration
- (to Ground or V_{IN}) ..... Indefinite

Storage Temperature Range
- J, RC, and Z Packages ..... –65°C to +150°C
- P Packages ..... –65°C to +125°C

Operating Temperature Range
- REF-02A, REF-02, REF-02RC ..... –55°C to +125°C
- REF-02E, REF-02H ..... 0°C to +70°C
- REF-02CJ,CZ, REF-02D ..... 0°C to +70°C
- REF-02CP, CS ..... –40°C to +85°C

Lead Temperature (Soldering, 60 sec) ..... 300°C

Junction Temperature (T_J) ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
TO-99 (J)	170	24	°C/W
8-Pin Hermetic DIP (Z)	162	26	°C/W
8-Pin Plastic DIP (P)	110	50	°C/W
20-Contact LCC (RC, TC)	120	40	°C/W
8-Pin SO (S)	160	44	°C/W
20-Contact PLCC (PC)	80	39	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO and PLCC packages.

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = +25°C$, unless otherwise noted.

			REF-02A/E			REF-02/H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Output Voltage	V_O	$I_L = 0$	4.985	5.000	5.015	4.975	5.000	5.025	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	±3	±6	—	±3	±6	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 7)	—	10	15	—	10	15	μV_{p-p}
Line Regulation (Note 2)		$V_{IN} = 8V$ to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 2)		$I_L = 0$ to 10mA	—	0.005	0.010	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S	(Note 8)	−0.3	−0.5	—	−0.3	−0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	—	30	—	—	30	—	mA
Temperature Voltage Output	V_T	(Note 3)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $-55°C \le T_A \le +125°C$ for REF-02A and REF-02, $0°C \le T_A \le +70°C$ for REF-02E and REF-02H, $I_L = 0mA$, unless otherwise noted.

			REF-02A/E			REF-02/H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Ouput Voltage Change with Temperature (Notes 4, 5)	ΔV_{OT}	$0°C \le T_A \le +70°C$ $-55°C \le T_A \le +125°C$	— —	0.02 0.06	0.06 0.15	— —	0.07 0.18	0.17 0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	—	3	8.5	—	10	25	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		$R_p = 10k\Omega$	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (V_{IN} = 8 to 33V) (Note 2)		$0°C \le T_A \le +70°C$ $-55°C \le T_A \le +125°C$	— —	0.007 0.009	0.012 0.015	— —	0.007 0.009	0.012 0.015	%/V
Load Regulation (I_L = 0 to 8mA) (Note 2)		$0°C \le T_A \le +70°C$ $-55°C \le T_A \le +125°C$	— —	0.006 0.007	0.010 0.012	— —	0.007 0.009	0.012 0.015	%/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 3)	—	2.1	—	—	2.1	—	mV/°C

NOTES:
1. Guaranteed by design.
2. Line and Load Regulation specifications include the effect of self heating.
3. Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
4. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V.

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5V} \right| \times 100$$

5. ΔV_{OT} specification applies trimmed to +5.000V or untrimmed.
6. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

7. Sample Tested.
8. During sink current test the driver meets the output voltage specified.

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02C MIN	REF-02C TYP	REF-02C MAX	REF-02D MIN	REF-02D TYP	REF-02D MAX	UNITS
Output Voltage	V_O	$I_L = 0mA$	4.950	5.000	5.050	4.900	5.000	5.100	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	±2.7	±6.0	—	±2.0	±6.0	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 7)	—	12	18	—	12	—	μV_{p-p}
Line Regulation (Note 2)		$V_{IN} = 8V$ to 30V	—	0.009	0.015	—	0.010	0.04	%/V
Load Regulation (Note 2)		$I_L = 0$ to 8mA	—	0.006	0.015	—	—	—	%/mA
		$I_L = 0$ to 4mA	—	—	—	—	0.015	0.04	
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.6	—	1.0	2.0	mA
Load Current	I_L		8	21	—	8	21	—	mA
Sink Current	I_S	(Note 8)	−0.3	−0.5	—	−0.3	−0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	—	30	—	—	30	—	mA
Temperature Voltage Output	V_T	(Note 3)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$; $I_L = 0mA$, $0°C \le T_A \le +70°C$ for REF-02CJ, CZ, DJ, DZ, DP; $-40°C \le T_A \le +85°C$ for REF-02CP, CS; unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02C MIN	REF-02C TYP	REF-02C MAX	REF-02D MIN	REF-02D TYP	REF-02D MAX	UNITS
Ouput Voltage Change with Temperature	ΔV_{OT}	(Notes 4 and 5)	—	0.14	0.45	—	0.49	1.7	%
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	—	20	65	—	70	250	ppm/°C
Change in V_O Temperature Coefficient With Output Adjustment		$R_p = 10k\Omega$	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (Note 2)		$V_{IN} = 8V$ to 30V	—	0.011	0.018	—	0.012	0.05	%/V
Load Regulation (Note 2)		$I_L = 0$ to 5mA	—	0.008	0.018	—	0.016	0.05	%/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 3)	—	2.1	—	—	2.1	—	mV/°C

NOTES:

1. Guaranteed by design.
2. Line and Load Regulation specifications include the effect of self heating.
3. Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
4. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V.

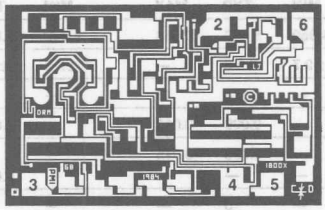
$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5V} \right| \times 100$$

5. ΔV_{OT} specification applies trimmed to +5.000V or untrimmed.
6. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

7. Sample Tested.
8. During sink current test the device meets the output voltage specified.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.074 × 0.048 inch, 3552 sq. mils
(1.88 × 1.22 mm, 2.29 sq. mm)

2. INPUT VOLTAGE (V_{IN})
3. TEMPERATURE TRANSDUCER OUTPUT VOLTAGE (TEMP)
4. GROUND
5. TRIM
6. OUTPUT VOLTAGE (V_{OUT})

WAFER TEST LIMITS at $V_{IN} = +15V$, $T_A = 25°C$ for REF-02N and REF-02G devices; $T_A = 125°C$ for REF-02NT and REF-02GT devices, unless otherwise noted. (Note 3)

PARAMETER	SYMBOL	CONDITIONS	REF-02NT LIMIT	REF-02N LIMIT	REF-02GT LIMIT	REF-02G LIMIT	UNITS
Output Voltage	V_O	$I_L = 0$	4.975 5.025	4.985 5.015	4.950 5.050	4.975 5.025	V MIN V MAX
Output Adjustment Range	V_{trim}	$R_P = 10k\Omega$	—	±3	—	±3	% MIN
Line Regulation		$V_{IN} = 8V$ to 33V	0.015	0.01	0.015	0.01	%/V MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02NT TYPICAL	REF-02N TYPICAL	REF-02GT TYPICAL	REF-02G TYPICAL	UNITS
Temp. Voltage Output	V_T	(Notes 1, 2)	630	630	630	630	mV
Temp. Voltage Output Temp. Coefficient	TCV_T	(Notes 1, 2)	2.1	2.1	2.1	2.1	mV/°C
Output Voltage Temp. Coefficient	TCV_O		10	10	10	10	ppm/°C
Load Regulation		$I_L = 0$ to 10mA $I_L = 0$ to 8mA, NT, GT @ +125°C	0.007	0.005	0.009	0.006	%/mA
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz	10	10	10	10	μV_{p-p}
Turn-On Settling Time	t_{ON}	To ±0.1% of final value, NT, GT @ +125°C	7.5	5.0	7.5	5.0	μs
Quiescent Supply Current	I_{SY}	No Load, NT, GT @ +125°C	1.4	1.0	1.4	1.0	mA
Load Current	I_L		21	21	21	21	mA
Sink Current	I_S		−0.5	−0.5	−0.5	−0.5	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	30	30	30	30	mA

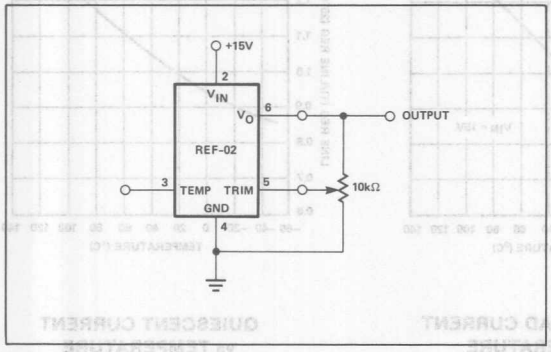
NOTES:
1. See AN-18 for detailed REF-02 thermometer applications information.
2. Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
3. For+25° C specifications of REF-02NT and REF-02GT, see REF-02N and REF-02G respectively.

OUTPUT ADJUSTMENT

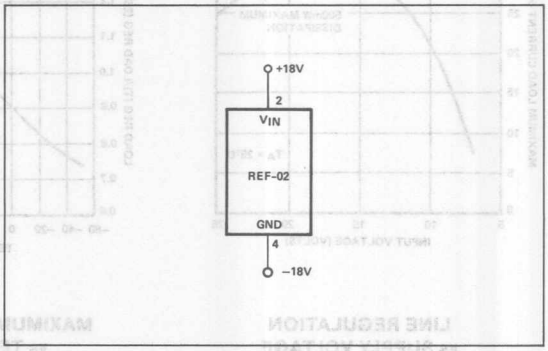
The REF-02 trim terminal can be used to adjust the output voltage over a 5V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V. Of course, the output can also be set to exactly 5.000V or to 5.12V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. Typically, the temperature coefficent change is 0.7ppm/° C for 100mV of output adjustment.

OUTPUT ADJUSTMENT CIRCUIT

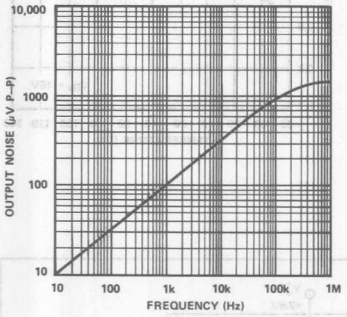


BURN-IN CIRCUIT

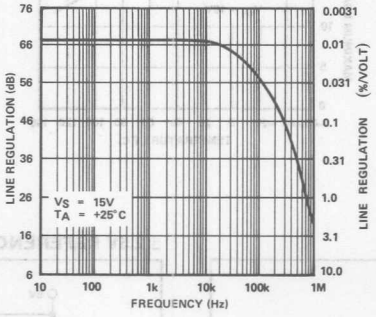


TYPICAL PERFORMANCE CHARACTERISTICS

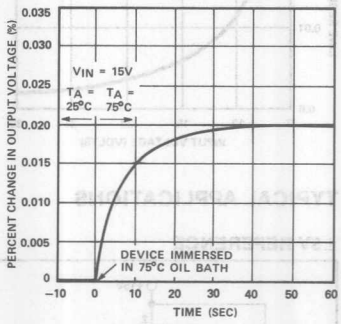
OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



LINE REGULATION vs FREQUENCY



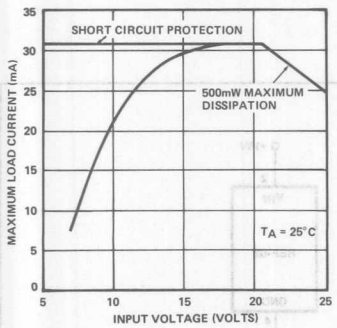
OUTPUT CHANGE DUE TO THERMAL SHOCK



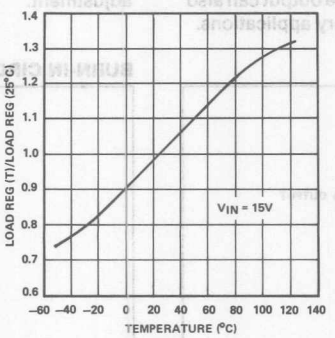
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TYPICAL PERFORMANCE CHARACTERISTICS

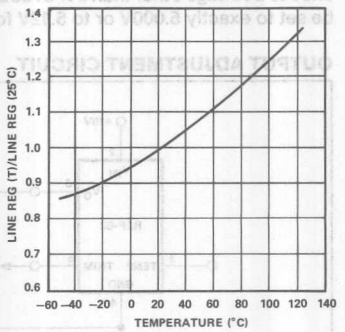
MAXIMUM LOAD CURRENT vs INPUT VOLTAGE



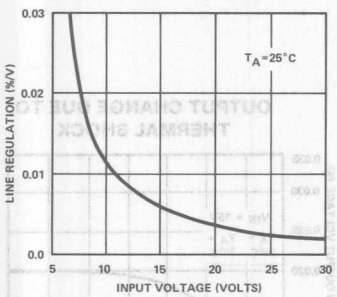
NORMALIZED LOAD REGULATION (ΔI_L = 10mA) vs TEMPERATURE



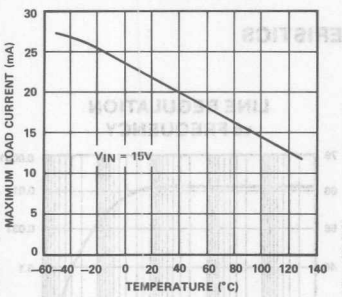
NORMALIZED LINE REGULATION vs TEMPERATURE



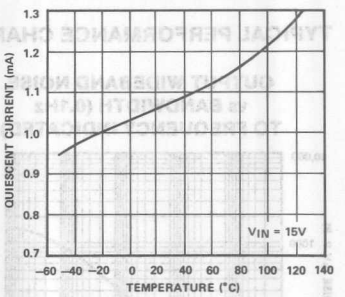
LINE REGULATION vs SUPPLY VOLTAGE



MAXIMUM LOAD CURRENT vs TEMPERATURE

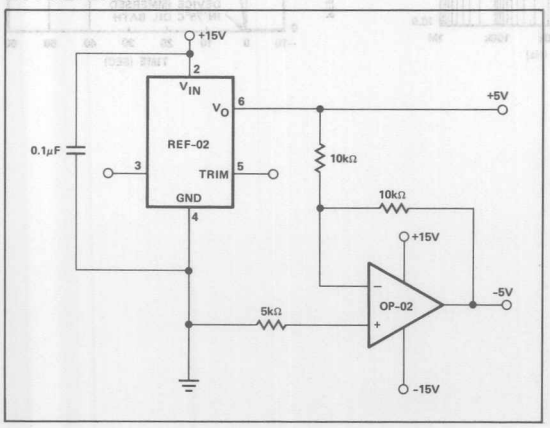


QUIESCENT CURRENT vs TEMPERATURE

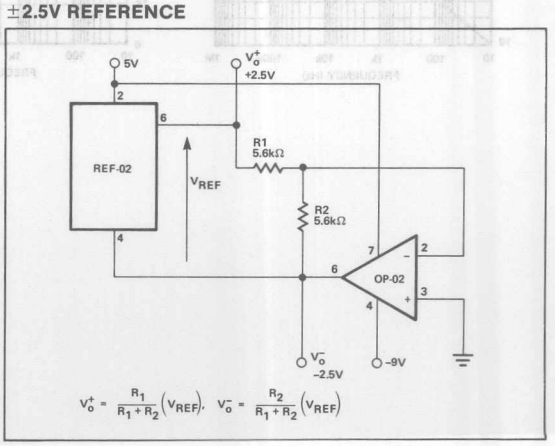


TYPICAL APPLICATIONS

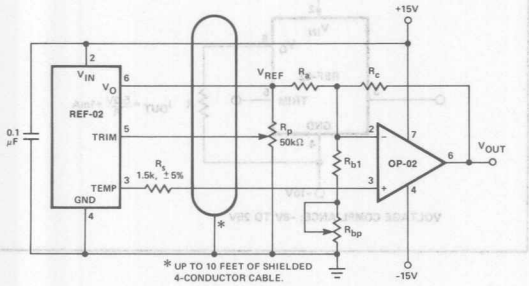
±5V REFERENCE



±2.5V REFERENCE



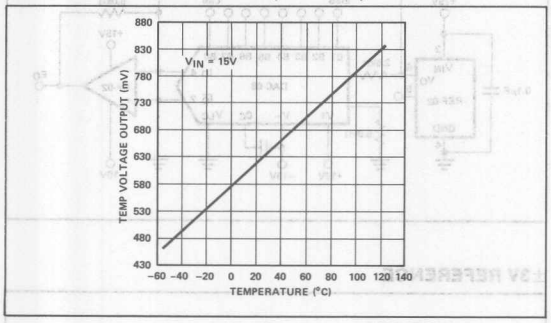
PRECISION TEMPERATURE TRANSDUCER WITH REMOTE SENSOR



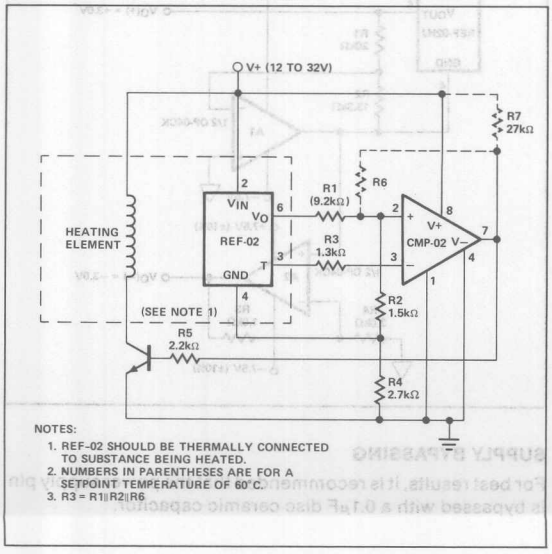
RESISTOR VALUES			
TCV_{OUT} SLOPE (S)	10mV/°C	100mV/°C	10mV/°F
TEMPERATURE RANGE	−55°C to +125°C	−55°C to +125°C	−67°F to +257°C
OUTPUT VOLTAGE RANGE	−0.55V to +1.25V	−5.5V to +12.5V*	−0.67V to +2.57V
ZERO-SCALE	0V @ 0°C	0V @ 0°C	0V @ 0°F
R_a (± 1% resistor)	9.09kΩ	15kΩ	7.5kΩ
R_{b1} (± 1% resistor)	1.5kΩ	1.82kΩ	1.21kΩ
R_{bp} (Potentiometer)	200Ω	500Ω	200Ω
R_c (±1% resistor)	5.11kΩ	84.5kΩ	8.25kΩ

*For 125°C operation, the op amp output must be able to swing to +12.5V, increase V_{IN} to +18V from +15V if this is a problem.

TYPICAL TEMPERATURE VOLTAGE OUTPUT vs TEMPERATURE (REF-02A)



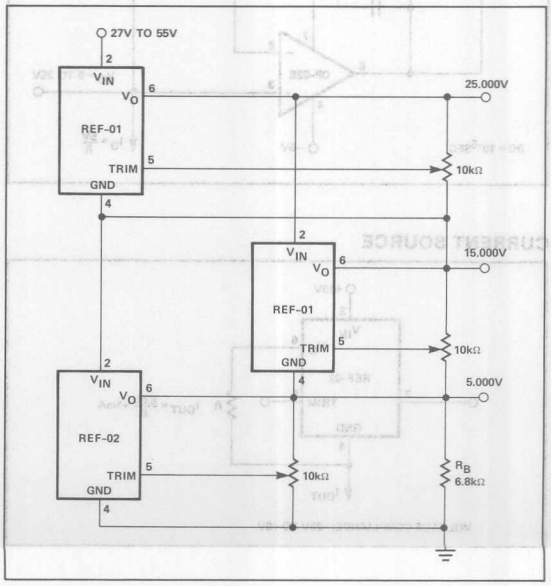
TEMPERATURE CONTROLLER



REFERENCE STACK WITH EXCELLENT LINE REGULATION

Two REF-01's and one REF-02 can be stacked to yield 5.000V, 15.000V and 25.000V outputs. An additional advantage of this circuit is near-perfect line regulation of the 5.0V and 15.0V outputs. A 27V to 55V input change produces an output change which is less than the noise voltage of the devices. A load bypass resistor (R_B) provides a path for the supply current (I_{SY}) of the 15.000V regulator.

In general, any number of REF-01's and REF-02's can be stacked this way. For example, ten devices will yield ten outputs in 5V or 10V steps. The line voltage can range from 100V to 130V. However, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21mA).

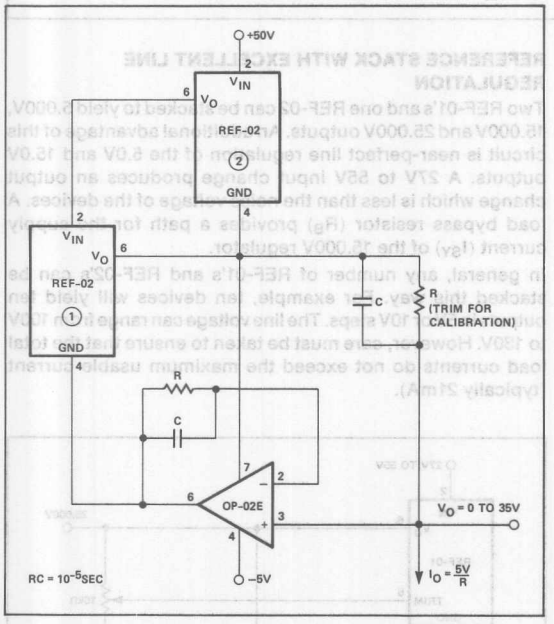


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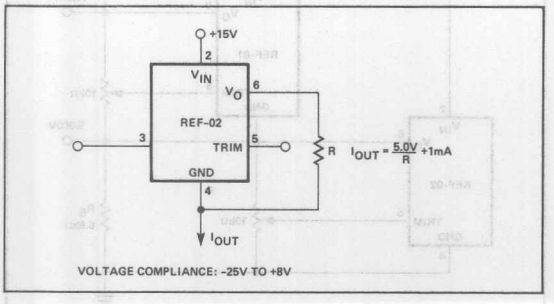
PRECISION CURRENT SOURCE

A current source with 35V output compliance and excellent output impedance can be obtained using this circuit. REF-02 ② keeps the line voltage and power dissipation constant in device ①; the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical 3μV/V PSRR of the OP-02E will create a 20ppm change (3μV/V × 35V/5V) in output current over a 35V range. For example, a 5mA current source can be built (R = 1kΩ) with 350MΩ output impedance.

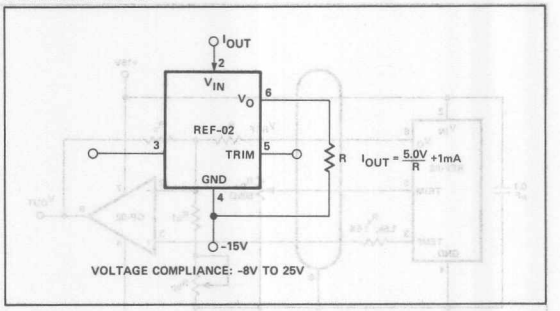
$$R_O = \frac{35V}{20 \times 10^{-6} \times 5mA}$$



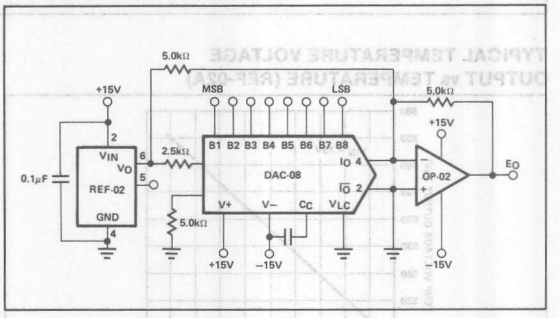
CURRENT SOURCE



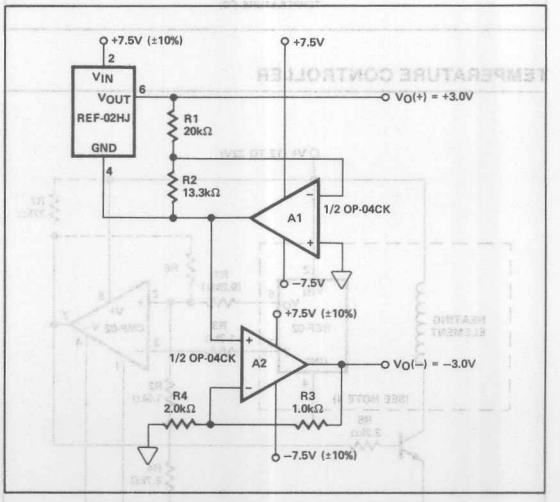
CURRENT SINK



D/A CONVERTER REFERENCE



±3V REFERENCE



SUPPLY BYPASSING

For best results, it is recommended that the power supply pin is bypassed with a 0.1μF disc ceramic capacitor.

+2.5V Precision Voltage Reference

REF-03

FEATURES

- +2.5 Volt Output ..... ±0.6% Max
- Wide Input Voltage Range ..... 4.5V to 33V
- Supply Current ..... 1.4mA Max
- Output Voltage Tempco ..... 50ppm/°C Max
- Line Regulation ..... 50ppm/V Max
- Load Regulation ..... 100ppm/mA Max
- Extended Industrial Temp Range ..... −40°C to +85°C
- Low Cost
- Available in Die Form

ORDERING INFORMATION†

PLASTIC PACKAGE	OPERATING TEMPERATURE RANGE
REF03GP	XIND
REF03GS††	XIND

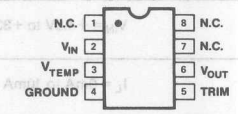
† Burn-in is available on commercial and industrial temperature range parts in plastic DIP.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The REF-03 precision voltage reference provides a stable +2.5V output, with minimal change for variations in supply voltage, ambient temperature or loading conditions. Single-supply operation over an input voltage range of +4.5V to +33V with a current drain of 1mA and good temperature stability is achieved using an improved bandgap design. Primarily targeted at price-sensitive applications, the REF-03 is available in plastic mini-dips and surface-mountable small outline plastic packages. For improved performance or −55°C/125°C operation, see the REF-43 data sheet.

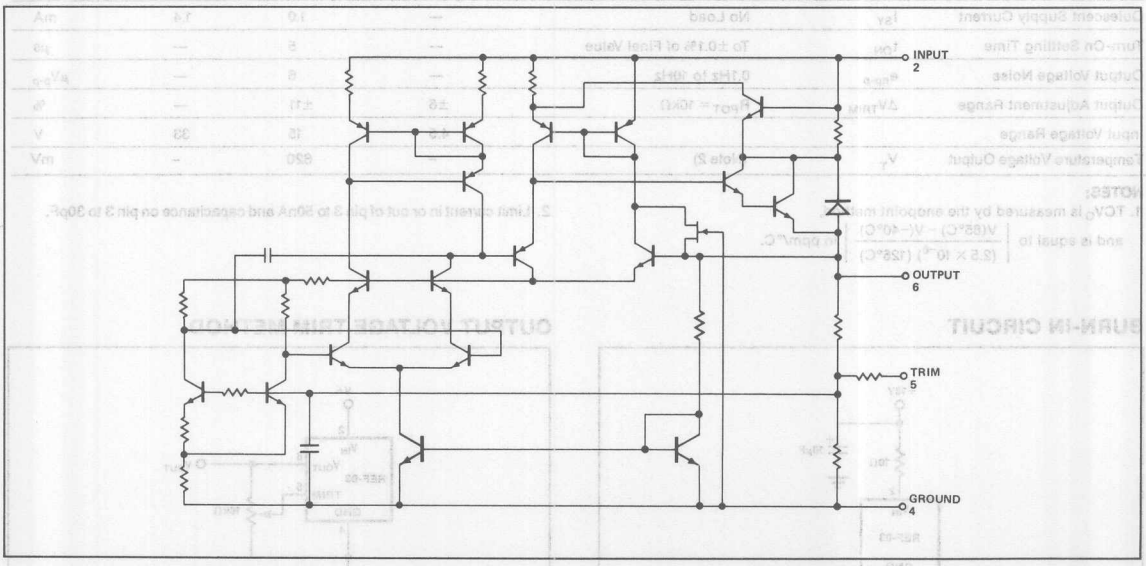
PIN CONNECTIONS



8-PIN PLASTIC DIP (P-Suffix)

8-PIN SO (S-Suffix)

SIMPLIFIED SCHEMATIC



6

Supply Voltage ..... +40V
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range
REF-03G (P,S) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +175°C
Junction Temperature Range ..... –65°C to +175°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

8-Pin Plastic DIP (P)	110	50	°C/W
8-Pin SO (S)	160	44	°C/W

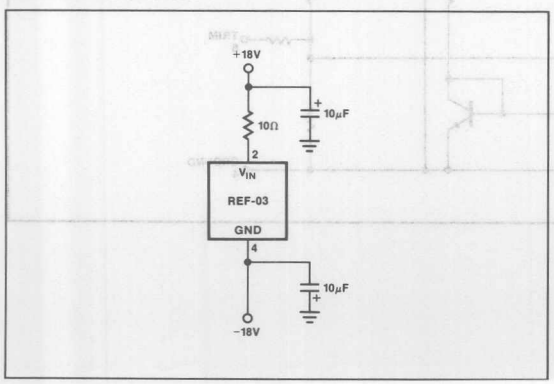
NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_{IN} = +15V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted.

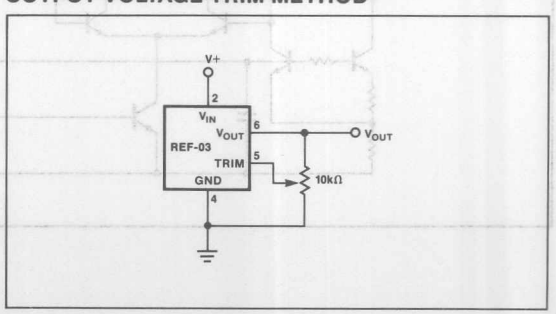
			REF-03G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V_O	No Load	2.485	2.500	2.515	V
Output Voltage Tolerance		No Load	—	0.2	0.6	%
Output Voltage Temperature Coefficient	TCV_O	(Note 1)	—	10	50	ppm/°C
Line Regulation		V_{IN} = +4.5V to +33V	—	20	50	ppm/V
			—	0.002	0.005	%/V
Load Regulation		I_L = 0mA to 10mA	—	60	100	ppm/mA
			—	0.006	0.010	%/mA
Load Current (Sourcing)	I_L		10	21	—	mA
Load Current (Sinking)	I_S		–0.3	–0.5	—	mA
Short-Circuit Output Current	I_{SC}	Output Shorted to Ground	—	24	—	mA
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	mA
Turn-On Settling Time	t_{ON}	To ±0.1% of Final Value	—	5	—	μs
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz	—	6	—	μV_{p-p}
Output Adjustment Range	ΔV_{TRIM}	R_{POT} = 10kΩ	±6	±11	—	%
Input Voltage Range			4.5	15	33	V
Temperature Voltage Output	V_T	(Note 2)	–	620	–	mV

NOTES:
1. TCV_O is measured by the endpoint method, and is equal to $\left| \frac{V(85°C) - V(-40°C)}{(2.5 \times 10^{-6})\ (125°C)} \right|$ in ppm/°C.
2. Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.

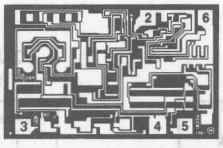
BURN-IN CIRCUIT



OUTPUT VOLTAGE TRIM METHOD



DICE CHARACTERISTICS



2. V_{IN}
3. V_{TEMP}
4. GROUND
5. TRIM
6. V_{OUT}

DIE SIZE 0.048 × 0.074 inch, 3552 sq. mils
(1.22 × 1.88 mm, 2.29 sq. mm)

WAFER TEST LIMITS at V_{IN} = +15V, T_A = 25°C.

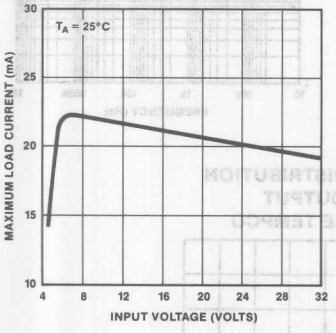
PARAMETER	SYMBOL	CONDITIONS	REF-03G LIMIT	UNITS
Output Voltage Tolerance	V_O	I_L = 0	2.500 ±0.015	V MAX
			0.6	% MAX
Line Regulation		V_{IN} = +4.5V to +33V	50	ppm/V MAX
			0.005	% MAX
Output Adjust Range	V_{TRIM}	R_P = 10kΩ	±6	% MIN
Quiescent Supply Current	I_{SY}	No Load	1.4	mA MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

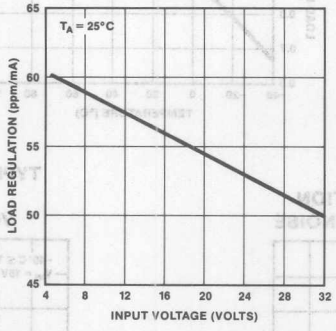
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TYPICAL PERFORMANCE CHARACTERISTICS

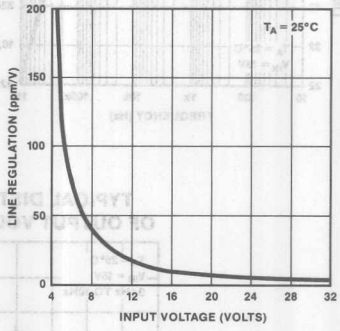
MAXIMUM LOAD CURRENT vs INPUT VOLTAGE



LOAD REGULATION (ΔI_L = 10mA) vs INPUT VOLTAGE

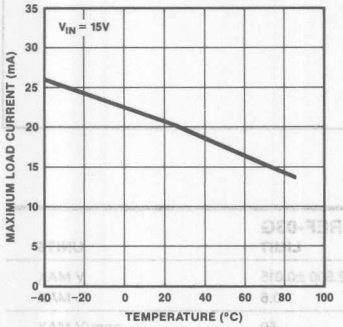


LINE REGULATION vs INPUT VOLTAGE

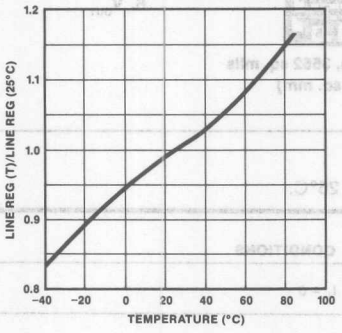


TYPICAL PERFORMANCE CHARACTERISTICS

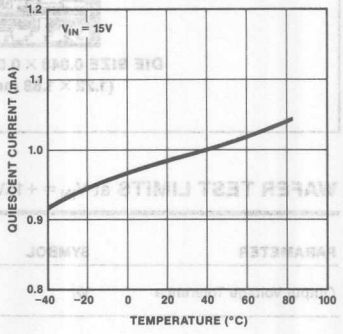
MAXIMUM LOAD CURRENT vs TEMPERATURE



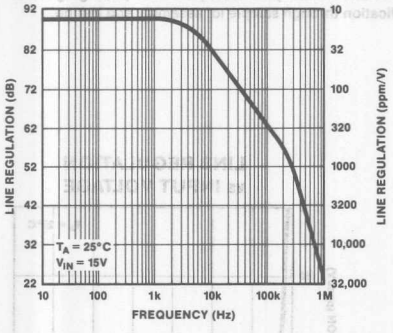
NORMALIZED LINE REGULATION (4.5V TO 33V) vs TEMPERATURE



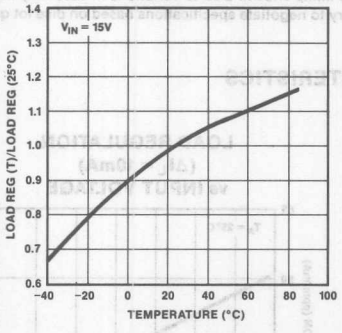
QUIESCENT CURRENT vs TEMPERATURE



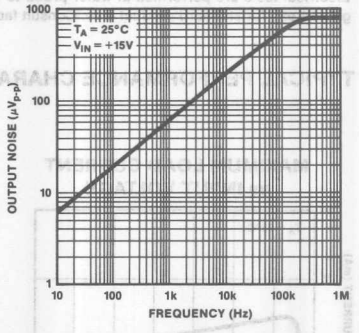
LINE REGULATION vs FREQUENCY



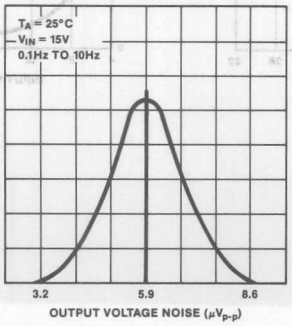
NORMALIZED LOAD REGULATION (ΔI_L = 10mA) vs TEMPERATURE



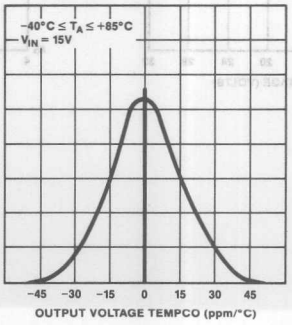
WIDEBAND OUTPUT NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



TYPICAL DISTRIBUTION OF OUTPUT VOLTAGE NOISE



TYPICAL DISTRIBUTION OF OUTPUT VOLTAGE TEMPCO



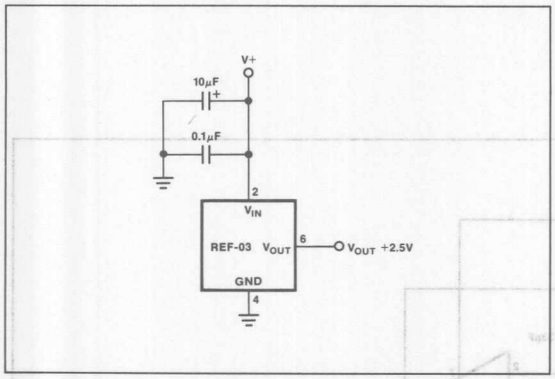
APPLICATIONS INFORMATION

The REF-03 provides a stable +2.5V output voltage with minimal dependence on load current, line voltage or temperature. This voltage is typically used to set an absolute reference point in data conversion circuits, or in analog circuits such as log amps, 4-20mA transmitters and power supplies. The REF-03 is of particular value in systems requiring a precision reference using a single +5V supply rail.

Because an onboard operational amplifier is used to amplify the basic bandgap cell voltage to 2.5V, supply decoupling is critical to the transient performance of a voltage reference. The supply line should be bypassed with a 10μF tantalum capacitor in parallel with a 0.01μF to 0.1μF ceramic capacitor for best results as shown in Figure 1. For less critical conditions, a single 0.1μF capacitor is adequate. The bypass capacitors should be located as close to the reference as possible. Inadequate bypassing can lead to instabilities.

Output bypass capacitors are not generally recommended. If necessary for high-frequency output impedance reduction, the capacitance value used should be at least 1μF.

FIGURE 1: Basic Connections



GENERATING AN ADJUSTABLE BIPOLAR VOLTAGE REFERENCE

Many times, there is a requirement for an adjustable bipolar reference. A simple method of generating such a reference is to connect the output of the REF-03 to an op amp in an adjustable gain configuration as shown in Figure 2. The trimable resistor is then used to generate the desired output voltage from −2.5V to +2.5V.

GENERATING A −2.5V REFERENCE

Often, there is a requirement for a negative reference voltage. The simplest method of generating a −2.5V reference with the REF-03 is to connect an op amp in a gain of −1 to the output, as shown in Figure 3. This provides both positive and negative 2.5V references. Figure 4 shows another method of obtaining a negative reference, in which the current-output element is a PNP transistor, with the REF-03 in a servo loop to ensure that the output remains 2.5V below ground.

FIGURE 2: Adjustable Bipolar Reference

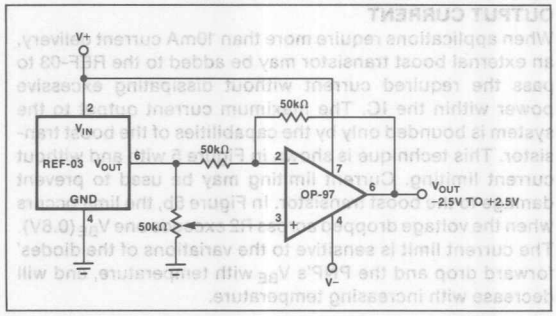


FIGURE 3: ±2.5V Reference

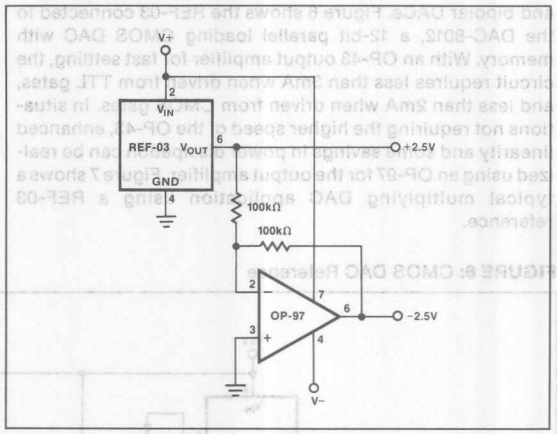
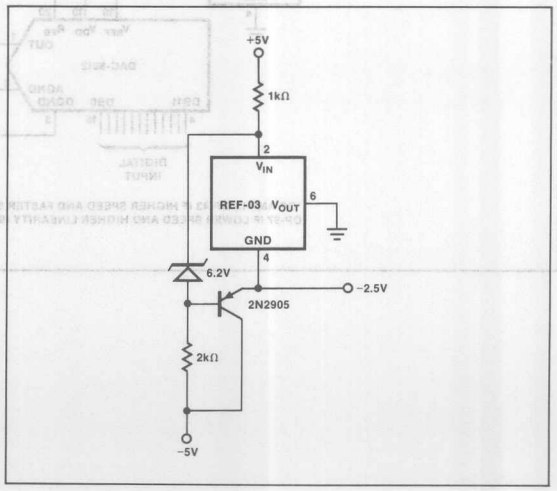


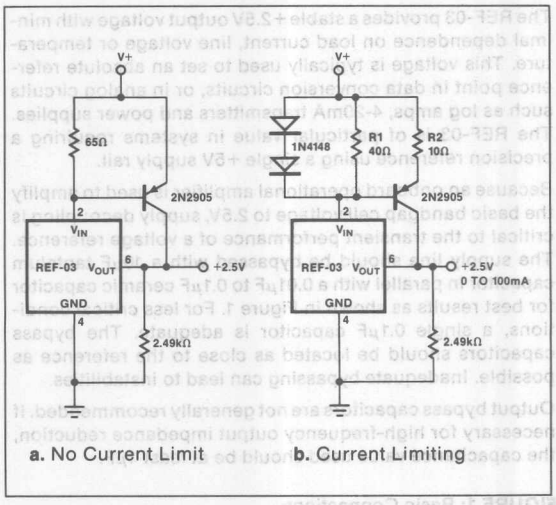
FIGURE 4: −2.5V Reference



BOOST TRANSISTOR PROVIDES HIGH OUTPUT CURRENT

When applications require more than 10mA current delivery, an external boost transistor may be added to the REF-03 to pass the required current without dissipating excessive power within the IC. The maximum current output to the system is bounded only by the capabilities of the boost transistor. This technique is shown in Figure 5 with and without current limiting. Current limiting may be used to prevent damage to the boost transistor. In Figure 5b, the limit occurs when the voltage dropped across R2 exceeds one V_{BE} (0.6V). The current limit is sensitive to the variations of the diodes' forward drop and the PNP's V_{BE} with temperature, and will decrease with increasing temperature.

FIGURE 5: Output Current Boost



CMOS DAC REFERENCE

The REF-03 makes an excellent reference for use with CMOS and bipolar DACs. Figure 6 shows the REF-03 connected to the DAC-8012, a 12-bit parallel loading CMOS DAC with memory. With an OP-43 output amplifier for fast settling, the circuit requires less than 3mA when driven from TTL gates, and less than 2mA when driven from CMOS gates. In situations not requiring the higher speed of the OP-43, enhanced linearity and some savings in power dissipation can be realized using an OP-97 for the output amplifier. Figure 7 shows a typical multiplying DAC application using a REF-03 reference.

FIGURE 6: CMOS DAC Reference

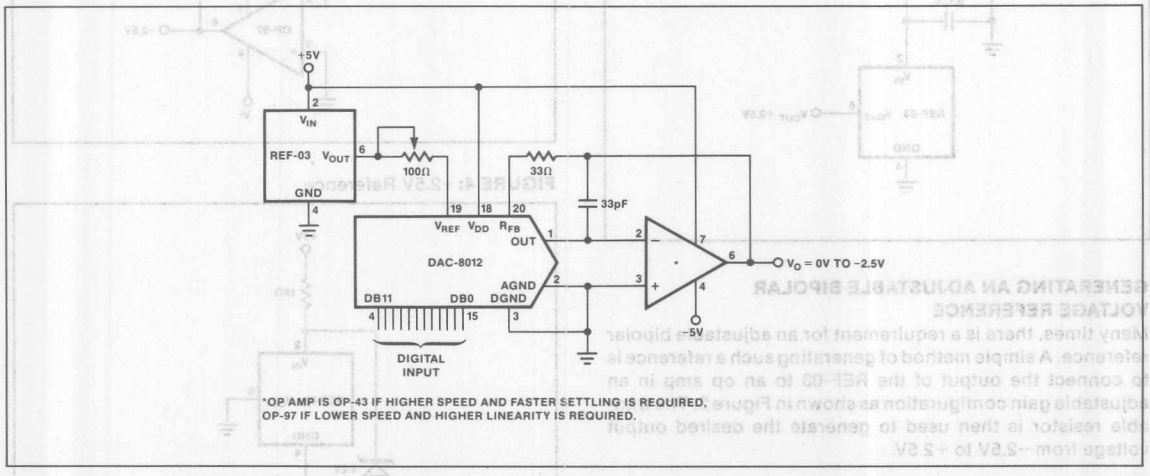
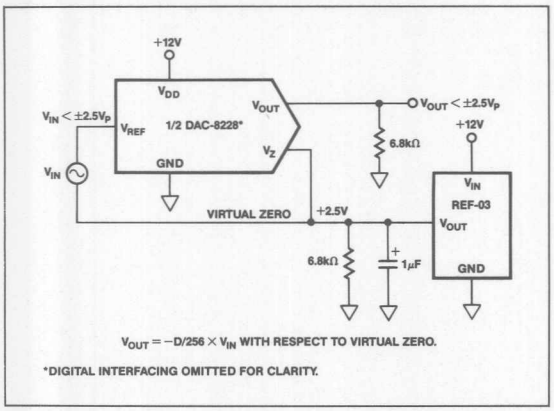


FIGURE 7: Multiplying CMOS DAC Reference

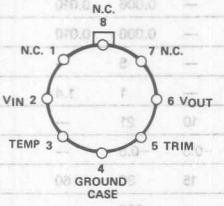


6

FEATURES

- 5 Volt Output
- Guaranteed Long-Term Stability ..... 100ppm/1000 Hrs Max
- Excellent Temperature Stability ..... 8.5ppm/°C Max
- Low Noise ..... $15\mu V_{p-p}$ Max
- Low Supply Current ..... 1.4mA Max
- Wide Input Voltage Range ..... 7V to 40V
- High Load-Driving Capability 20mA
- Short-Circuit Proof
- Processed Per MIL-STD-883

PIN CONNECTIONS & ORDERING INFORMATION

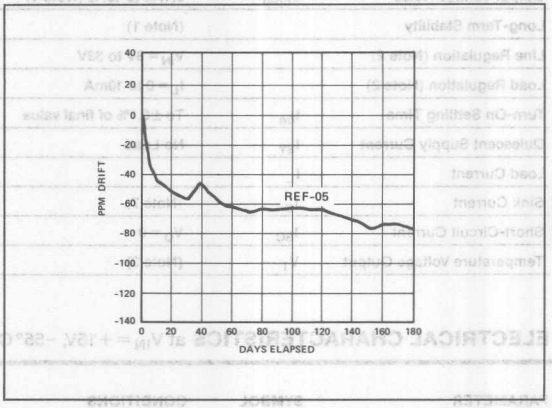


TO-99 (J-Suffix)
REF-05AJ/883
REF-05BJ/883

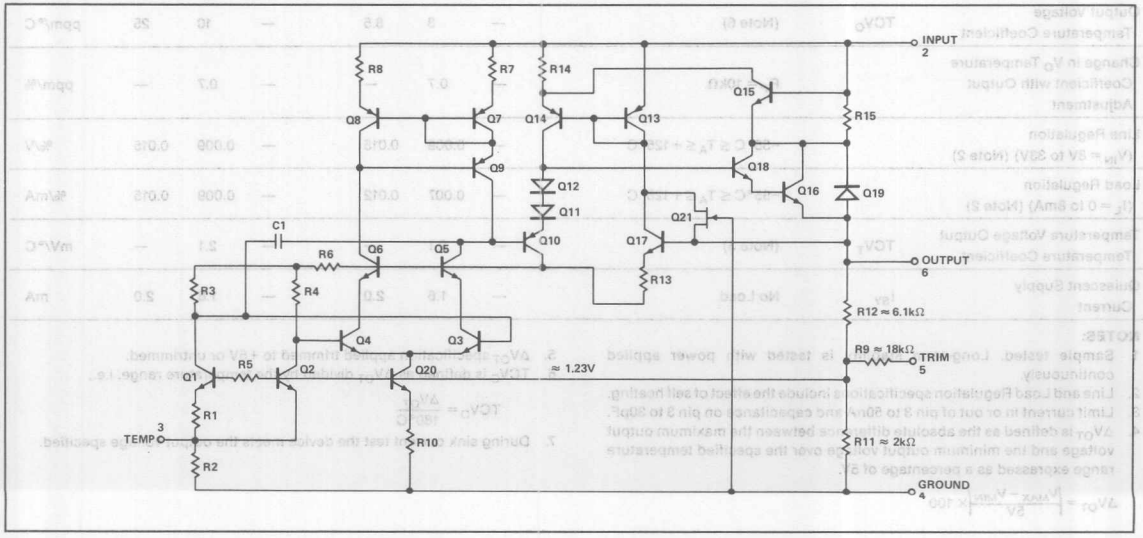
GENERAL DESCRIPTION

The REF-05 precision voltage reference provides a stable +5V output which can be adjusted over a ±6% range with minimal effect on temperature stability. Long-term drift is guaranteed at 100ppm/1000 hrs. maximum. Single-supply operation over an input voltage range of 7V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-05 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. The versatility of the REF-05 is enhanced by its use as a monolithic temperature transducer. For +10V Precision Voltage References see the REF-10 data sheet.

LONG-TERM DRIFT PLOT (Average of 20 Devices)



SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage
REF-05A, B 40V
Output Short-Circuit Duration
(to Ground or V_{IN}) ..... Indefinite
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Operating Temperature Range
REF-05A, REF-05B ..... –55°C to +125°C

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
TO-99 (J)	170	24	°C/W

NOTES:
1. Derate at 7.1mW/°C above 80°C ambient temperature for TO-99 (J) package.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO package.

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = 25°C$, unless otherwise noted.

			REF-05A			REF-05B			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Output Voltage	V_O	$I_L = 0$	4.985	5.0	5.015	4.975	5.0	5.025	V
Output Adjustment Range	ΔV_{trim}	$R_P = 10k\Omega$	±3	±6	—	±3	±6	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 1)	—	10	15	—	10	15	μV_{p-p}
Long-Term Stability		(Note 1)	—	65	100	—	65	100	ppm/1kHrs
Line Regulation (Note 2)		$V_{IN} = 8V$ to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 2)		$I_L = 0$ to 10mA	—	0.005	0.010	—	0.006	0.010	%/mA
Turn-On Settling Time	t_{on}	To ±0.1% of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1	1.4	—	1	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S	(Note 7)	–0.3	–0.5	—	–0.3	–0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	15	30	60	15	30	60	mA
Temperature Voltage Output	V_T	(Note 3)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $-55°C \le T_A \le +125°C$ and $I_L = 0mA$, unless otherwise noted.

			REF-05A			REF-05B			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Output Voltage Change with Temperature (Notes 4 & 5)	ΔV_{OT}	$-55°C \le T_A \le +125°C$	—	0.06	0.15	—	0.18	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	—	3	8.5	—	10	25	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		$R_P = 10k\Omega$	—	0.7	—	—	0.7	—	ppm/%
Line Regulation ($V_{IN} = 8V$ to 33V) (Note 2)		$-55°C \le T_A \le +125°C$	—	0.009	0.015	—	0.009	0.015	%/V
Load Regulation ($I_L = 0$ to 8mA) (Note 2)		$-55°C \le T_A \le +125°C$	—	0.007	0.012	—	0.009	0.015	%/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 3)	—	2.1	—	—	2.1	—	mV/°C
Quiescent Supply Current	I_{SY}	No Load	—	1.6	2.0	—	1.6	2.0	mA

NOTES:
1. Sample tested. Long-term stability is tested with power applied continuously.
2. Line and Load Regulation specifications include the effect of self heating.
3. Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
4. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V.

$$\Delta V_{OT} = \left|\frac{V_{MAX} - V_{MIN}}{5V}\right| \times 100$$

5. ΔV_{OT} specification applied trimmed to +5V or untrimmed.
6. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{180°C}$$

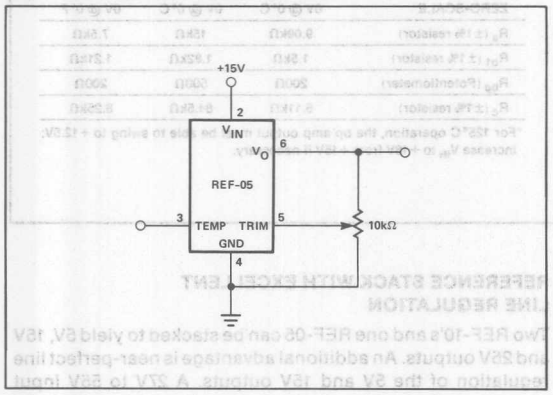
7. During sink current test the device meets the output voltage specified.

OUTPUT ADJUSTMENT

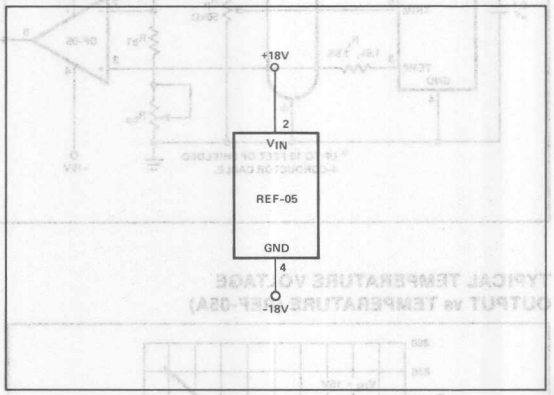
The REF-05 trim terminal can be used to adjust the output voltage over a 5V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V. Of course, the output can also be set to exactly 5V or to 5.12V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. Typically the temperature coefficient change is 0.7ppm/°C for 100mV of output adjustment.

OUTPUT ADJUSTMENT CIRCUIT



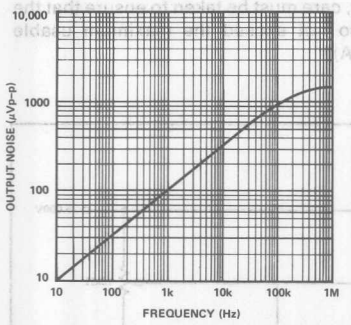
BURN-IN CIRCUIT



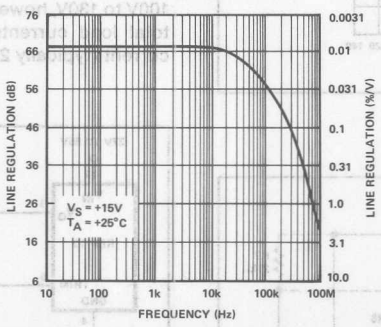
6

TYPICAL PERFORMANCE CHARACTERISTICS

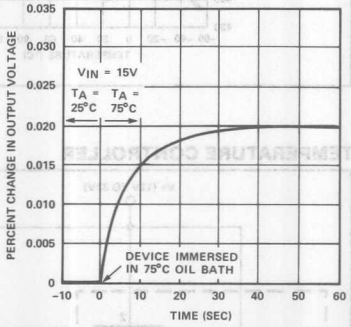
OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



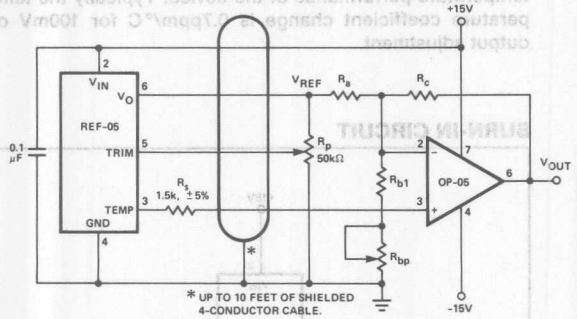
LINE REGULATION vs FREQUENCY



OUTPUT CHANGE DUE TO THERMAL SHOCK



PRECISION TEMPERATURE TRANSDUCER WITH REMOTE SENSOR

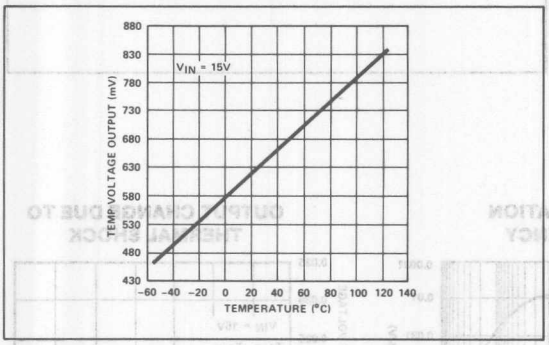


RESISTOR VALUES

TCV_{OUT} SLOPE (S)	10mV/°C	100mV/°C	10mV/°F
TEMPERATURE RANGE	−55°C to +125°C	−55°C to +125°C	−67°F to +257°F
OUTPUT VOLTAGE* RANGE	−0.55V to +1.25V	−5.5V to +12.5V	−0.67V to +2.57V
ZERO-SCALE	0V @ 0°C	0V @ 0°C	0V @ 0°F
R_a (±1% resistor)	9.09kΩ	15kΩ	7.5kΩ
R_{b1} (±1% resistor)	1.5kΩ	1.82kΩ	1.21kΩ
R_{bp} (Potentiometer)	200Ω	500Ω	200Ω
R_c (±1% resistor)	5.11kΩ	84.5kΩ	8.25kΩ

*For 125°C operation, the op amp output must be able to swing to +12.5V; increase V_{IN} to +18V from +15V if necessary.

TYPICAL TEMPERATURE VOLTAGE OUTPUT vs TEMPERATURE (REF-05A)

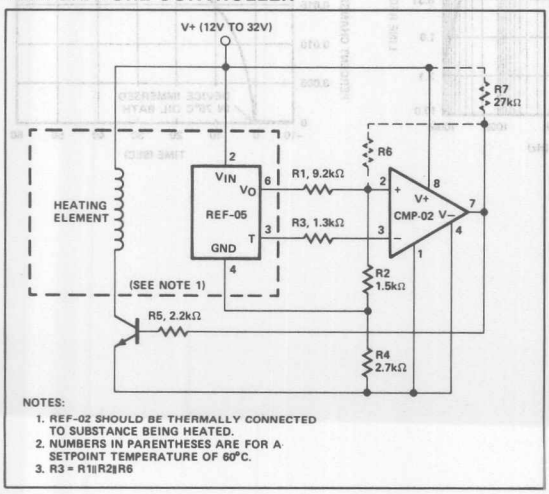


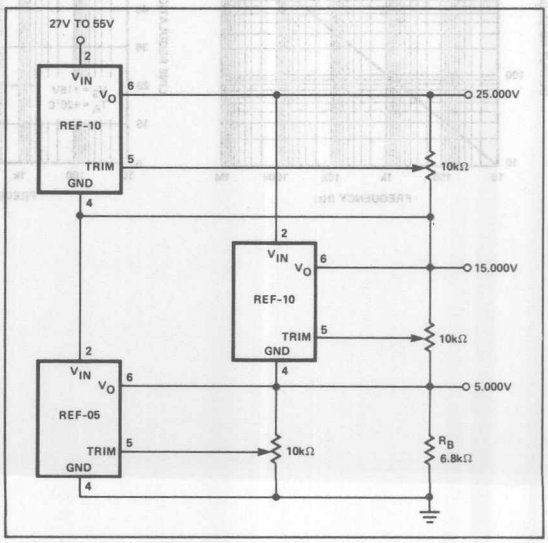
REFERENCE STACK WITH EXCELLENT LINE REGULATION

Two REF-10's and one REF-05 can be stacked to yield 5V, 15V and 25V outputs. An additional advantage is near-perfect line regulation of the 5V and 15V outputs. A 27V to 55V input change produces an output change which is less than the noise voltage of the devices. A load bypass resistor (R_g) provides a path for the supply current (I_{SY}) of the 15V regulator.

In general, any number of REF-10's and REF-05's can be stacked this way. For example, ten devices will yield ten outputs in 5V or 10V steps. The line voltage can range from 100V to 130V, however, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21mA).

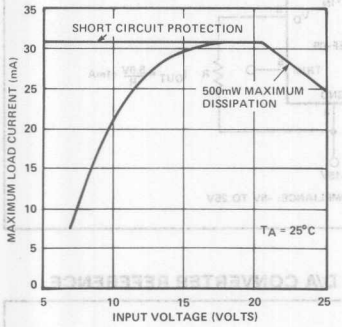
TEMPERATURE CONTROLLER



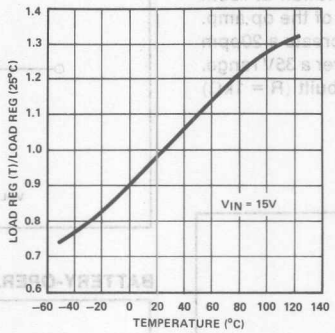


TYPICAL PERFORMANCE CHARACTERISTICS

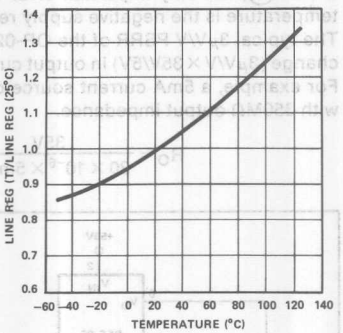
MAXIMUM LOAD CURRENT vs INPUT VOLTAGE



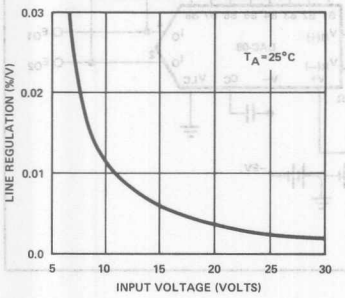
NORMALIZED LOAD REGULATION (ΔI_L = 10mA) vs TEMPERATURE



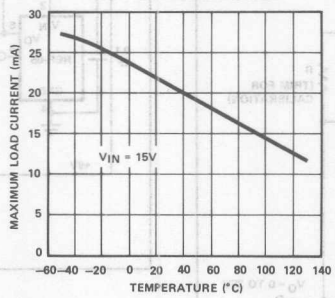
NORMALIZED LINE REGULATION vs TEMPERATURE



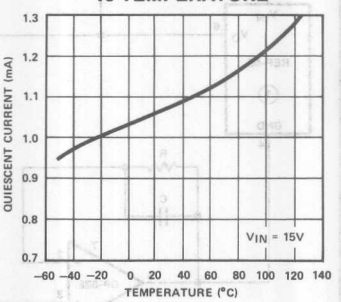
LINE REGULATION vs SUPPLY VOLTAGE



MAXIMUM LOAD CURRENT vs TEMPERATURE

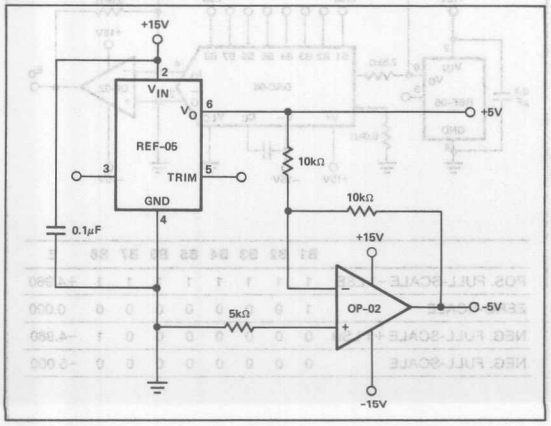


QUIESCENT CURRENT vs TEMPERATURE

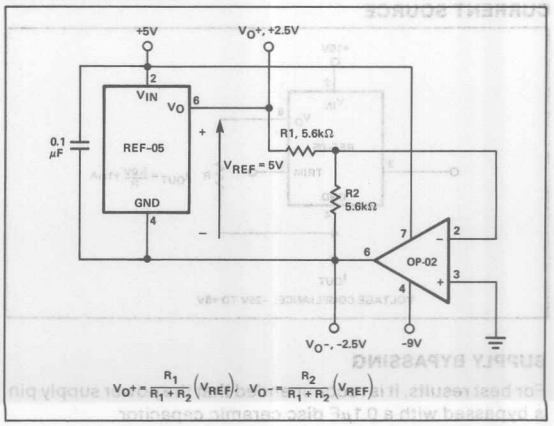


TYPICAL APPLICATIONS

±5V REFERENCE



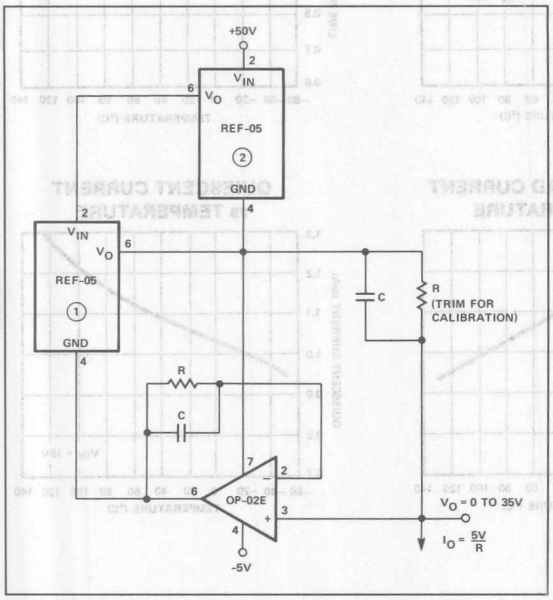
±2.5V REFERENCE



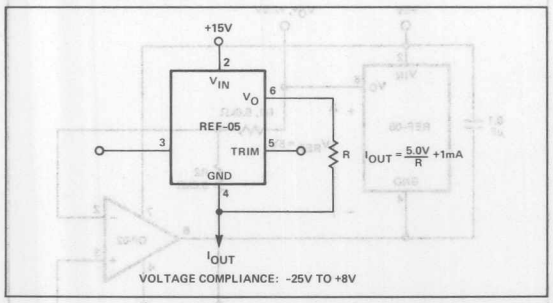
PRECISION CURRENT SOURCE

A current source with 35V output compliance and excellent output impedance can be obtained using this circuit. REF-05 (2) keeps the line voltage and power dissipation constant in device (1); the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical 3μV/V PSRR of the OP-02E will create a 20ppm change (3μV/V × 35V/5V) in output current over a 35V range. For example, a 5mA current source can be built (R = 1kΩ) with 350MΩ output impedance.

$$R_O = \frac{35V}{20 \times 10^{-6} \times 5mA}$$



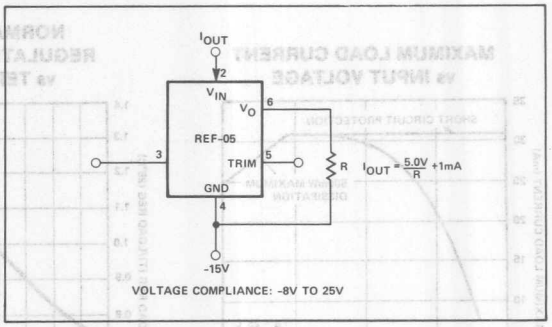
CURRENT SOURCE



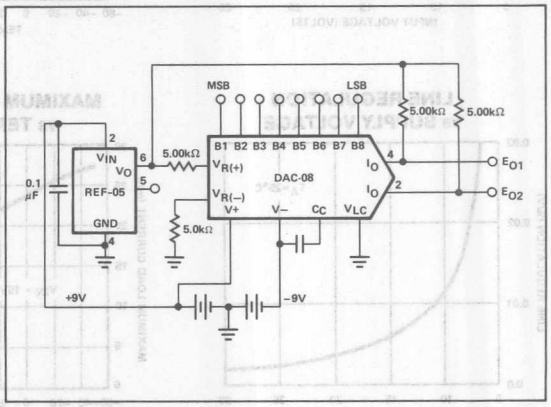
SUPPLY BYPASSING

For best results, it is recommended that the power supply pin is bypassed with a 0.1μF disc ceramic capacitor.

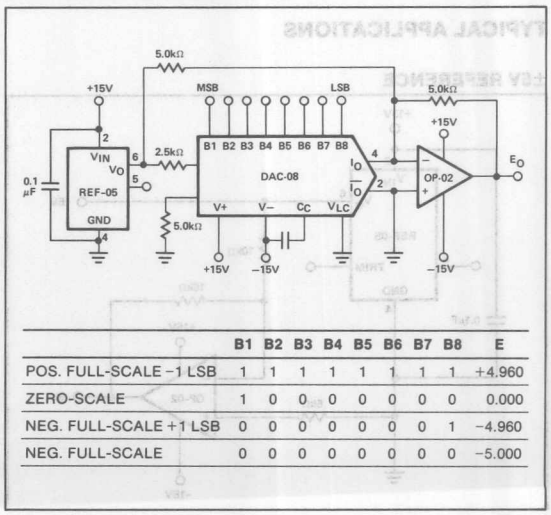
CURRENT SINK



BATTERY-OPERATED D/A CONVERTER REFERENCE



D/A CONVERTER REFERENCE



	B1	B2	B3	B4	B5	B6	B7	B8	E
POS. FULL-SCALE −1 LSB	1	1	1	1	1	1	1	1	+4.960
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000
NEG. FULL-SCALE +1 LSB	0	0	0	0	0	0	0	1	−4.960
NEG. FULL-SCALE	0	0	0	0	0	0	0	0	−5.000

Negative 10V/10.24V Voltage Reference

REF-08

FEATURES

- Low Cost Negative Reference
- Pin Selectable To –10.24V Output For Binary Applications
- 10mA Minimum Output Current
- Wide Input Voltage Range, –11.4V to –36V
- Low 1.4V Drop Out Voltage
- Wide ±270mV Adjustment Range
- Available in Die Form

APPLICATIONS

- 8 & 10-Bit CMOS A/D and D/A Converters
- Voltage-to-Frequency Converters
- Strain Gauge Bridge Reference
- Precision Negative Ten Volt Regulator

ORDERING INFORMATION †

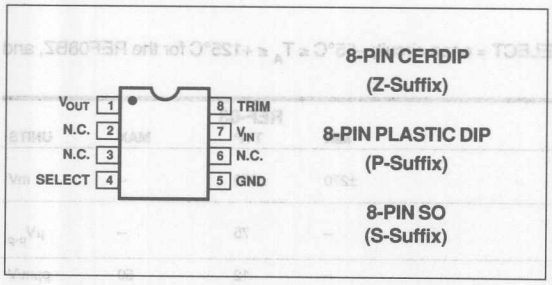
	PACKAGE			
TCV_O ppm/°C	CERDIP 8-PIN	PLASTIC 8-PIN	SO 8-PIN	OPERATING TEMPERATURE RANGE
50	REF08BZ*	–	–	MIL
80	REF08GZ	–	–	XIND
100	–	REF08HP	REF08HS††	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS



GENERAL DESCRIPTION

The REF-08 is a series regulation, buried Zener, negative voltage reference with pin selectable output voltage. Its low temperature coefficient, low noise, and selectable output make it an ideal reference for A/D converters such as the ADC-908 or the PM-7574. The REF-08 is also well suited for CMOS DAC applications where a positive output voltage is desired.

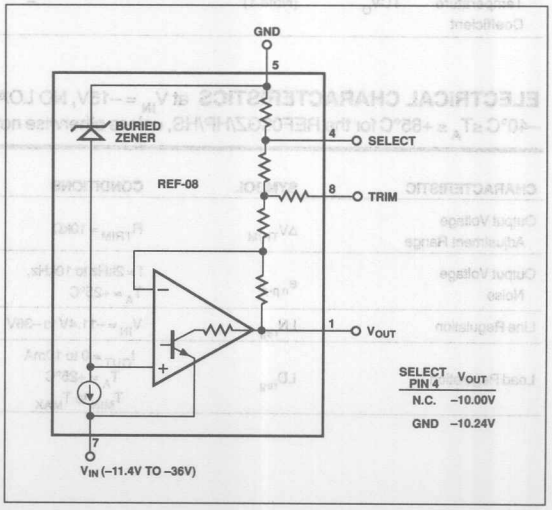
Applications with 8-bit accuracy will typically be able to use the REF-08 without trimming its output voltage. This is particularly true of CMOS DACs with low gain errors such as the DAC-8408 and PM-7528.

Leaving the SELECT pin open will result in a –10V output. Grounding SELECT will produce a –10.24V output (i.e. –10mV per 10-bit LSB) that is ideal for binary applications.

A ±270mV adjustment range is available with the REF-08 which exhibits a tight 0.04ppm/°C/mV of adjustment temperature coefficient. In many applications, the combined tempcos of an adjusted REF-08 will be superior to more expensive precision references with tighter initial tempcos but greater changes with adjustment.

The REF-08 has been designed to operate from a "worst case" –12V power supply (–11.4V). This low dropout voltage makes the best of the poor supply regulation in some digital systems. Its 10mA output current capability and unloaded supply current of only 2mA provide better power/performance than most traditional op amp inverter circuits.

FUNCTIONAL DIAGRAM



6

Input Voltage (V_{IN}) .....
Output Voltage (V_{OUT}) .....+0.3V to V_{IN}
TRIM Voltage (pin 8) .....+0.3V to V_{IN}
SELECT Voltage (pin 4).....+0.3V to V_{OUT}
Output Short-Circuit Duration
(to Ground or V_{IN}).....30 seconds
Operating Temperature Range
REF-08BZ .....–55°C to +125°C
REF-08GZ, HP, HS .....–40°C to 85°C
Storage Temperature Range
Z Package .....–65°C to +150°C
S, P Packages.....–65°C to +125°C

Lead Temperature (Soldering, 60 sec.) .....300°C

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	162	26	°C/W
8-Pin Plastic DIP (P)	110	50	°C/W
8-Pin SO (S)	160	44	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_{IN} = –15V, NO LOAD, SELECT = open circuit; –55°C ≤ T_A ≤ +125°C for the REF08BZ, and –40°C ≤ T_A ≤ +85°C for the REF08GZ/HP/HS, unless otherwise noted.

			REF-08B		REF-08G		REF-08H		
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
–10V Output Voltage	V_O	T_A = +25°C	–10.03	–9.97	–10.04	–9.96	–10.04	–9.96	V
		T_{MIN} to T_{MAX}	–10.05	–9.95	–10.06	–9.94	–10.08	–9.92	
–10V Output Voltage Tolerance	ΔV_O	T_A = +25°C	–	±30	–	±40	–	±40	mV
		T_{MIN} to T_{MAX}	–	±50	–	±60	–	±80	
–10.24 Output Voltage (Select=GND)	V_O	T_A = +25°C	–10.28	–10.20	–10.29	–10.19	–10.30	–10.18	V
		T_{MIN} to T_{MAX}	–10.30	–10.18	–10.32	–10.16	–10.36	–10.12	
–10.24V Output Voltage Tolerance (Select=GND)	ΔV_O	T_A = +25°C	–	±40	–	±50	–	±60	mV
		T_{MIN} to T_{MAX}	–	±60	–	±80	–	±120	
Output Voltage Temperature Coefficient	TCV_O	(Note 1)	–	50	–	80	–	100	ppm/°C

ELECTRICAL CHARACTERISTICS at V_{IN} = –15V, NO LOAD, SELECT = open circuit; –55°C ≤ T_A ≤ +125°C for the REF08BZ, and –40°C ≤ T_A ≤ +85°C for the REF08GZ/HP/HS, unless otherwise noted.

			REF-08			
CHARACTERISTIC	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Adjustment Range	ΔV_{TRIM}	R_{TRIM} = 10kΩ	±270	±350	–	mV
Output Voltage Noise	$e_{n\ p-p}$	f = 2kHz to 10kHz, T_A = +25°C	–	75	–	μV_{p-p}
Line Regulation	LN_{reg}	V_{IN} = –11.4V to –36V	–	12	50	ppm/V
Load Regulation	LD_{reg}	I_{OUT} = 0 to 10mA, T_A = +25°C	–	10	25	ppm/mA
		T_{MIN} to T_{MAX}	–	15	50	

ELECTRICAL CHARACTERISTICS at V_{IN} = –15V, NO LOAD, SELECT = open circuit; –55°C ≤ T_A ≤ +125°C for the REF08BZ, and –40°C ≤ T_A ≤ +85°C for the REF08GZ/HP/HS, unless otherwise noted. *Continued*

CHARACTERISTIC	SYMBOL	CONDITIONS	REF-08 MIN	REF-08 TYP	REF-08 MAX	UNITS
Load Current (Into Pin 1)	I_{OUT}	(Note 2)	10	20	–	mA
Load Current (Out of Pin 1)	I_{OUT}	–10.04V ≤ V_O ≤ –9.96V	–0.1	–0.2	–	mA
Short-Circuit Output Current	I_{SC}		–	45	–	mA
Quiescent Supply Current	I_{SY}		–	1.1	2.0	mA

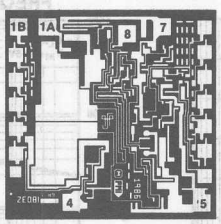
NOTES:

1. The REF-08BZ TCV_O is tested by measuring Output Voltage at –55°C and +125°C to guarantee the TCV_O limit. The REF-08GZ, HP, HS are tested by measuring Output Voltage at 25°C to guarantee the TCV_O limits. TCV_O is calculated by the end point method:

$$TCV_O = \left[\frac{V_O(T_{MAX}) - V_O(T_{MIN})}{(10V)(10^{-6})(125°C)}\right] \text{ in ppm/°C}$$

2. Guaranteed by Load Regulation Test.

DICE CHARACTERISTICS



DIE SIZE 0.066 x 0.065 inch, 4290 sq. mils (1.68 x 1.65mm, 2.77 sq. mm)

1A. V_{OUT}*
1B. V_{OUT}*
4. SELECT
5. GND
7. V_{IN}
8. TRIM

*** Pads 1A and 1B must be bonded together to V_{OUT}.**

6

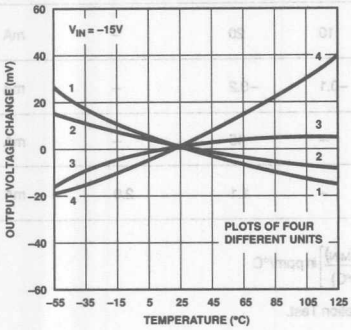
WAFER TEST LIMITS at V_{IN} = –15V, NO LOAD, SELECT = Open Circuit, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-08N LIMITS	UNITS
Output Voltage	V_O		–10.04 –9.96	V MIN V MAX
Output Voltage	V_O	SELECT = GND	–10.30 –10.18	V MIN V MAX
Line Regulation	LN_{reg}	V_{IN} = –11.4V to –16.5V	±50	ppm/V MAX
Load Regulation	LD_{reg}	Load Current = 0mA to 10mA	±25	ppm/mA MAX
Output Adjustment Voltage Range	V_{TRIM}	R_{TRIM} = 10kΩ	±270	mV MIN
Quiescent Supply Current	I_{SY}		2.0	mA MAX

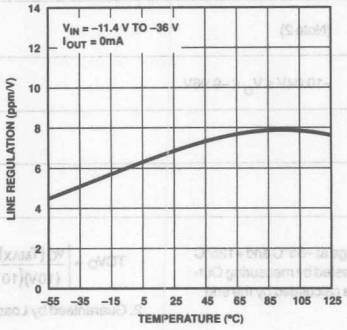
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS

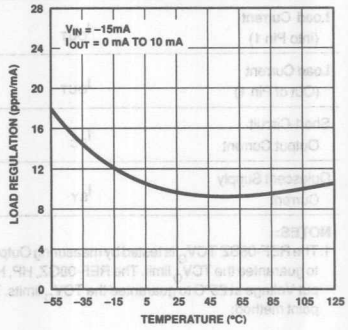
OUTPUT VOLTAGE CHANGE vs TEMPERATURE



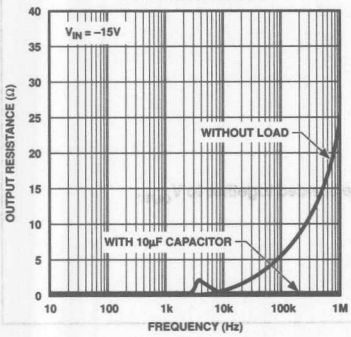
LINE REGULATION vs TEMPERATURE



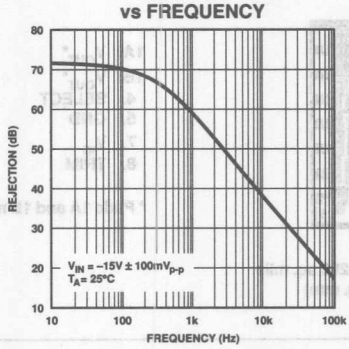
LOAD REGULATION vs TEMPERATURE



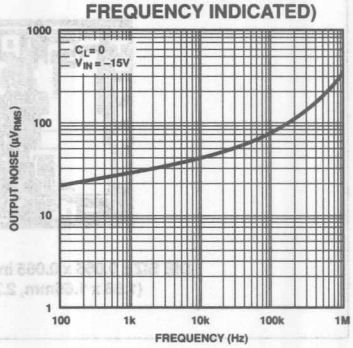
OUTPUT RESISTANCE vs FREQUENCY



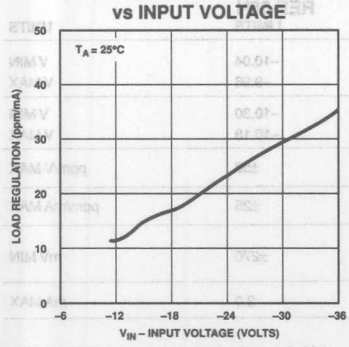
RIPPLE REJECTION vs FREQUENCY



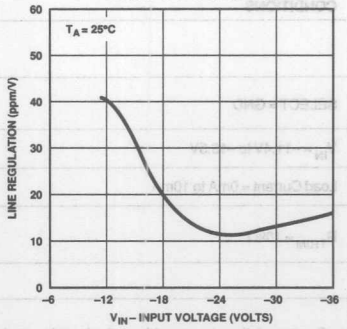
WIDEBAND NOISE vs FREQUENCY (10Hz TO FREQUENCY INDICATED)



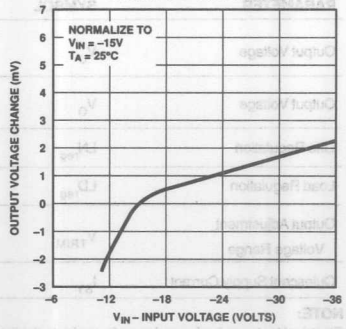
LOAD REGULATION vs INPUT VOLTAGE



LINE REGULATION vs INPUT VOLTAGE

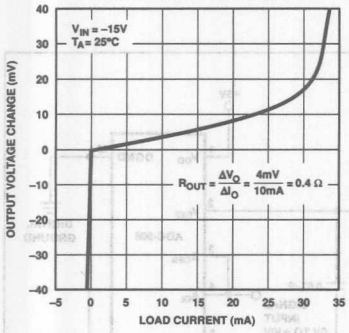


OUTPUT VOLTAGE CHANGE vs INPUT VOLTAGE

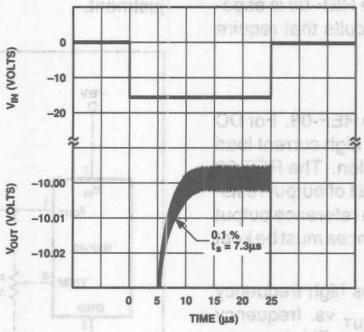


TYPICAL ELECTRICAL CHARACTERISTICS *Continued*

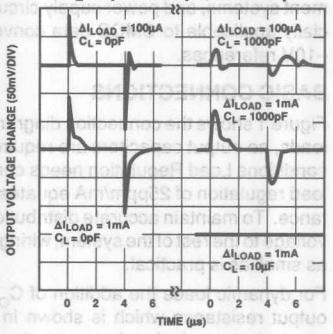
OUTPUT VOLTAGE CHANGE vs LOAD CURRENT



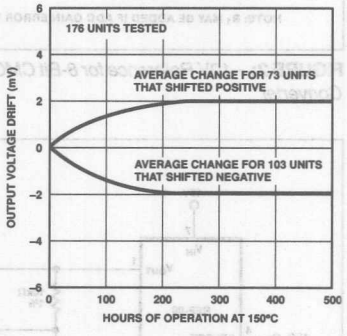
START-UP TIME



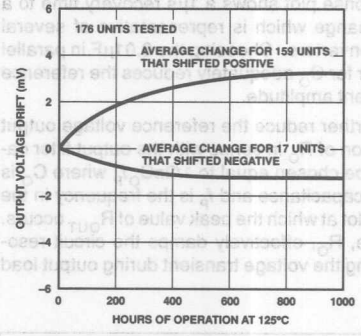
LOAD TRANSIENT RESPONSE C_L = 0pF, 1000pF, AND 10µF



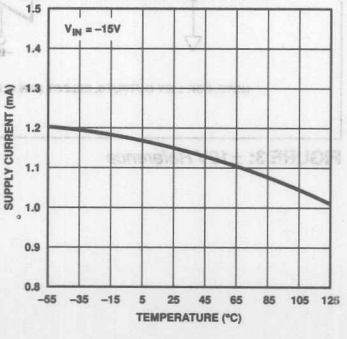
LONG TERM DRIFT ACCELERATED BY BURN-IN CERDIP PACKAGE



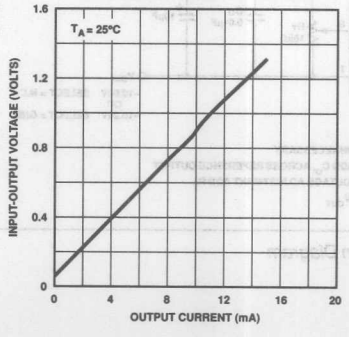
LONG TERM DRIFT ACCELERATED BY BURN-IN PLASTIC PACKAGES



SUPPLY CURRENT vs TEMPERATURE



MINIMUM INPUT-OUTPUT DIFFERENTIAL VOLTAGE



6

dependence on load current, input voltage or temperature variations. This single package device works well as an absolute reference point in data conversion circuits, or in analog circuits such as logarithmic amplifiers, strain gauge bridge measurement systems, and power supply circuits. The REF-08 is especially applicable to CMOS data converter circuits that require –10V references.

BASIC CONNECTIONS

Figure 1 shows the connection diagram for the REF-08. For DC loads, no output capacitors are required. For high current load conditions Load Regulation needs consideration. The REF-08 load regulation of 25ppm/mA equates to 0.25Ω of output resistance. To maintain accurate distribution of the reference output voltage to the rest of the system, wiring resistances must be kept as small as is practical.

For dynamic loads the addition of C_O reduces high frequency output resistance which is shown in the R_{OUT} vs. frequency graphs in the typical performance characteristics. This is generally important with A/D converters that have a continuously changing load.

In the typical performance characteristics graph section, the Load Transient response plot shows a 1µs recovery time to a 1mA load current change which is representative of several typical CMOS A/D converters. Choosing the 0.01µF in parallel with a 10µF capacitor for C_O adequately reduces the reference output voltage transient amplitude.

One refinement to further reduce the reference voltage output transient is introduction of R_O in series with the output filter capacitors. R_O should be chosen equal to $1/2\pi C_O f_P$ where C_O is the total output filter capacitance and f_P is the frequency in the R_{OUT} vs. frequency plot at which the peak value of R_{OUT} occurs. This extra resistance, R_O, effectively damps the circuit resonance further reducing the voltage transient during output load changes.

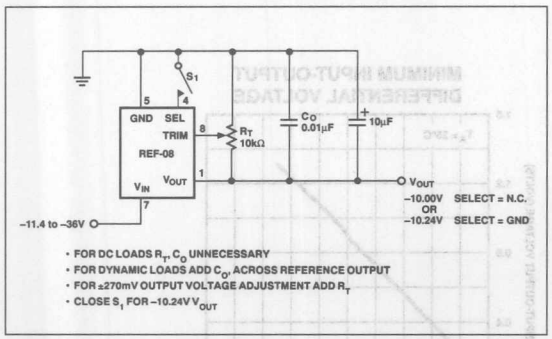


FIGURE 1: *Connection Diagram*

Output voltages within ±270mV of nominal can easily be obtained by addition of the 10k Trimpot*. This range adequately addresses the full-scale adjustment ranges required by CMOS A/D and D/A converters. The effect on the REF-08 output voltage temperature coefficient is a low 0.04ppm/°C per mV of adjustment.

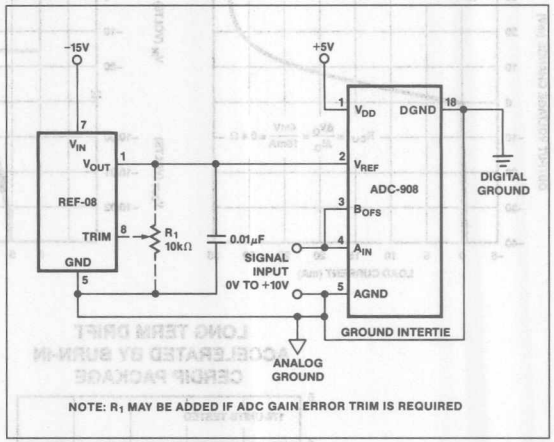


FIGURE 2: *–10V Reference for 8-Bit CMOS Analog-to-Digital Converter*

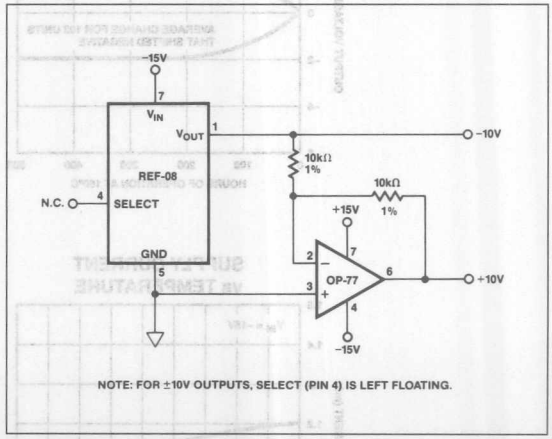


FIGURE 3: *±10V Reference*

*Trimpot is a registered trademark of Bourns, Inc.

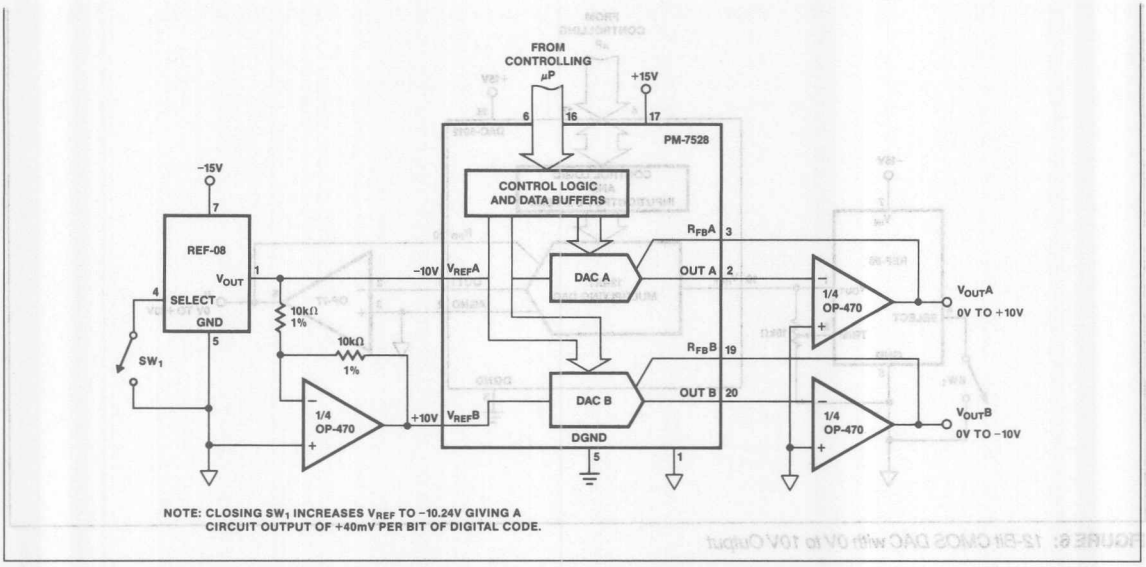


FIGURE 4: *8-Bit Resolution, Dual Output "No-Trim" DAC with 0V to +10V and 0V to −10V Outputs*

6

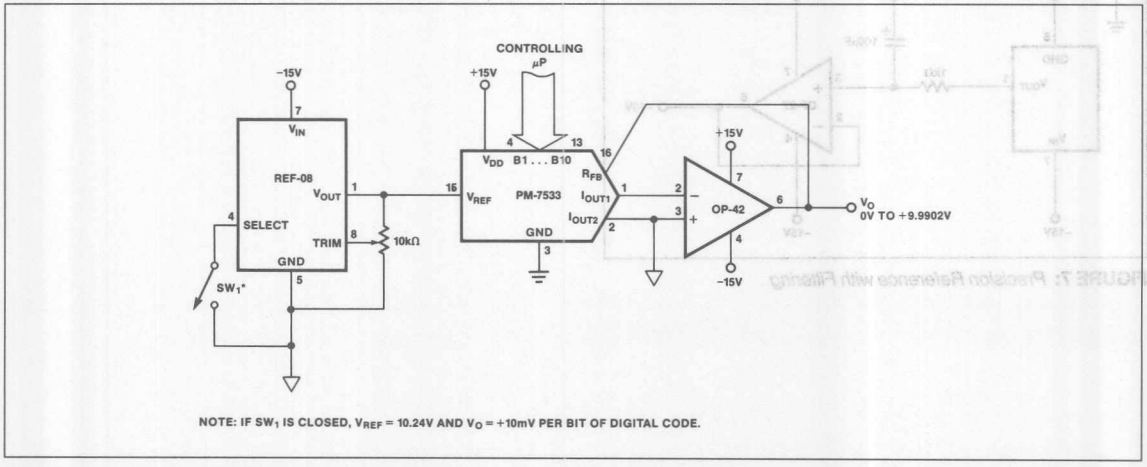


FIGURE 5: *10-Bit CMOS DAC with 0V to +10V Output*

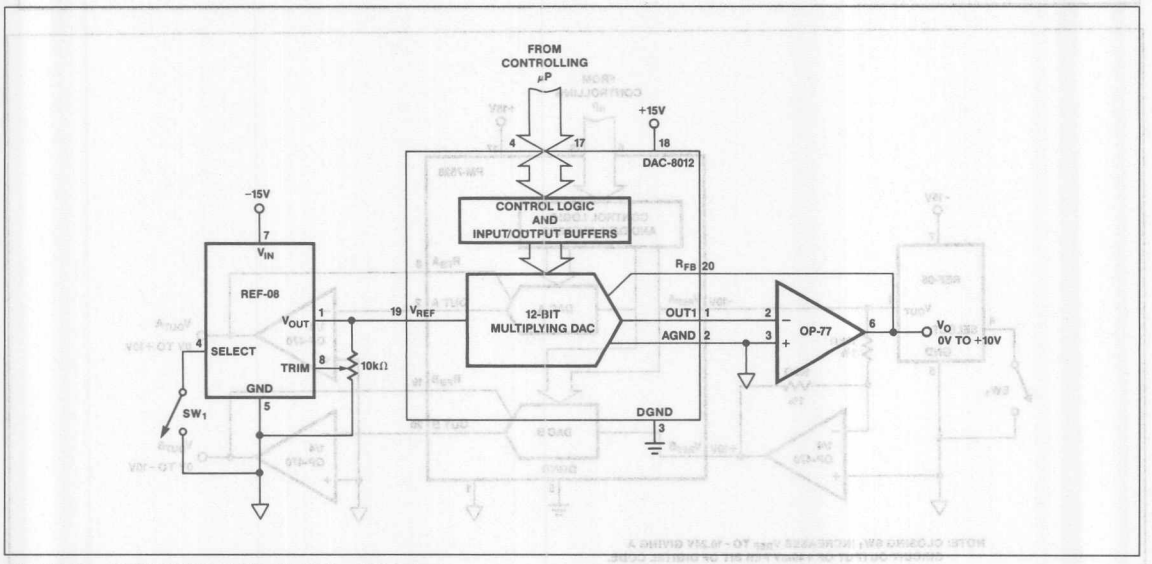


FIGURE 6: *12-Bit CMOS DAC with 0V to 10V Output*

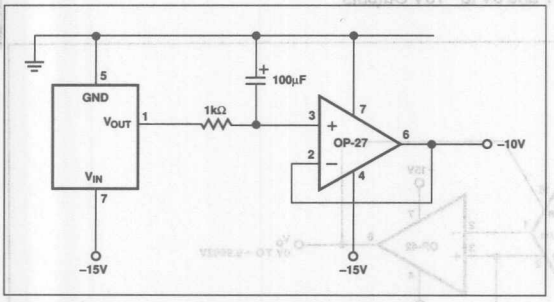


FIGURE 7: *Precision Reference with Filtering*

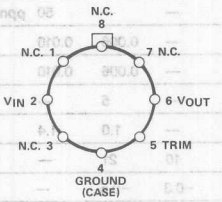
+10V Precision Voltage Reference (Guaranteed Long-Term Stability)

REF-10

FEATURES

- 10 Volt Output
- Guaranteed Long-Term Stability ..... 50ppm/1000 Hrs Max
- Excellent Temperature Stability ..... 8.5ppm/°C Max
- Low Noise ..... $30\mu V_{p-p}$ Max
- Low Supply Current ..... 1.4mA Max
- Wide Input Voltage Range ..... 12V to 40V
- High Load-Driving Capability 20mA
- Short-Circuit Proof
- Processed Per MIL-STD-883

PIN CONNECTIONS & ORDERING INFORMATION

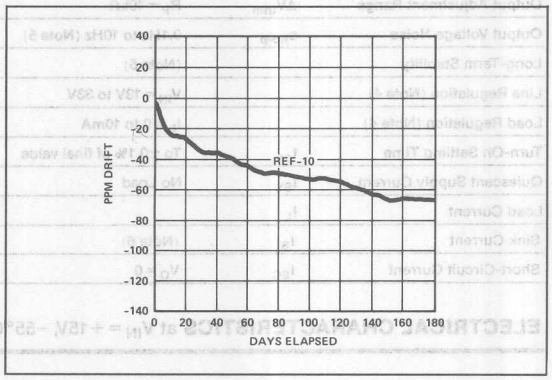


TO-99 (J-Suffix)
REF-10AJ/883
REF-10BJ/883

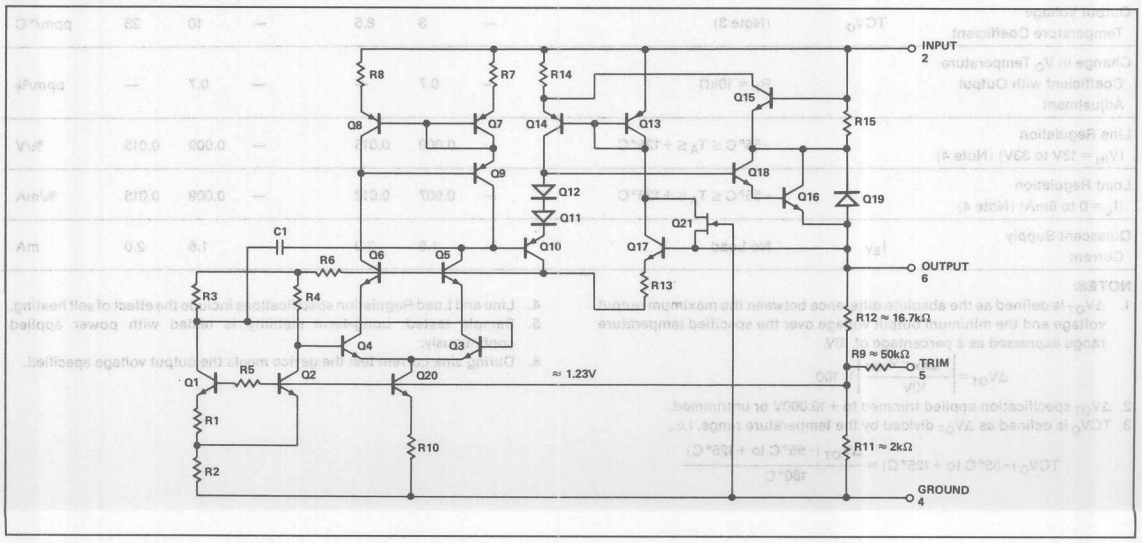
GENERAL DESCRIPTION

The REF-10 precision voltage reference provides a stable +10V output that can be adjusted over a ±3% range with minimal effect on temperature stability. Long-term drift is guaranteed at 50ppm/1000 hrs. maximum. Single-supply operation over an input voltage range of 12V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-10 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. For +5V precision voltage references, see the REF-05 data sheet.

LONG-TERM DRIFT PLOT (Average of 20 Devices)



SIMPLIFIED SCHEMATIC



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ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage
REF-10A, B 40V
Output Short-Circuit Duration
(to Ground or V_{IN}) ..... Indefinite
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Operating Temperature Range
REF-10A, REF-10B ..... –55°C to +125°C

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
TO-99 (J)	170	24	°C/W

NOTES:
1. Derate at 7.1mW/°C above 80°C ambient temperature for TO-99 package.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO package.

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = 25°C$, unless otherwise noted.

			REF-10A			REF-10B			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Output Voltage	V_O	$I_L = 0$	9.97	10	10.03	9.95	10	10.05	V
Output Adjustment Range	ΔV_{trim}	$R_P = 10k\Omega$	+3	±3.3	—	±3	±3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 5)	—	20	30	—	20	30	μV_{p-p}
Long-Term Stability		(Note 5)	—	—	50	—	—	50	ppm/1000 Hrs
Line Regulation (Note 4)		$V_{IN} = 13V$ to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 4)		$I_L = 0$ to 10mA	—	0.005	0.08	—	0.006	0.010	%/mA
Turn-On Settling Time	t_{on}	To ±0.1% of final value	—	5	—	—	5	—	μsec.
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S	(Note 6)	−0.3	−0.5	—	−0.3	−0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	15	30	60	15	30	60	mA

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $-55°C \le T_A \le +125°C$ and $I_L = 0$, unless otherwise noted.

			REF-10A			REF-10B			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Output Voltage Change with Temperature (Notes 1 & 2)	ΔV_{OT}	$-55°C \le T_A \le +125°C$	—	0.06	0.15	—	0.18	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	3	8.5	—	10	25	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		$R_P = 10k\Omega$	—	0.7	—	—	0.7	—	ppm/%
Line Regulation ($V_{IN} = 13V$ to 33V) (Note 4)		$-55°C \le T_A \le +125°C$	—	0.009	0.015	—	0.009	0.015	%/V
Load Regulation ($I_L = 0$ to 8mA) (Note 4)		$-55°C \le T_A \le +125°C$	—	0.007	0.012	—	0.009	0.015	%/mA
Quiescent Supply Current	I_{SY}	No Load	—	1.6	2.0	—	1.6	2.0	mA

NOTES:
1. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V.

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{10V} \right| \times 100$$

2. ΔV_{OT} specification applied trimmed to +10.000V or untrimmed.
3. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O\,(-55°C \text{ to } +125°C) = \frac{\Delta V_{OT}\,(-55°C \text{ to } +125°C)}{180°C}$$

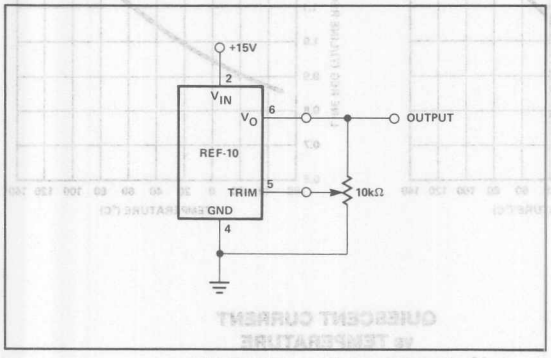
4. Line and Load Regulation specifications include the effect of self heating.
5. Sample tested. Long-term stability is tested with power applied continuously.
6. During sink current test the device meets the output voltage specified.

OUTPUT ADJUSTMENT

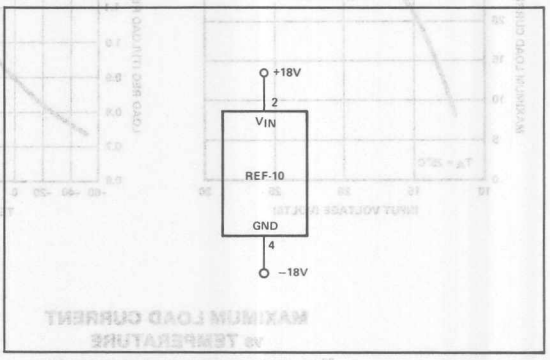
The REF-10 trim terminal can be used to adjust the output voltage over a 10V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V. Of course, the output can also be set to exactly 10.000V.

Adjustment of the output does not significantly affect the temperature performance of the device. Typically, the temperature coefficient change is 0.7ppm/°C per 100mV of output adjustment.

OUTPUT ADJUSTMENT CIRCUIT



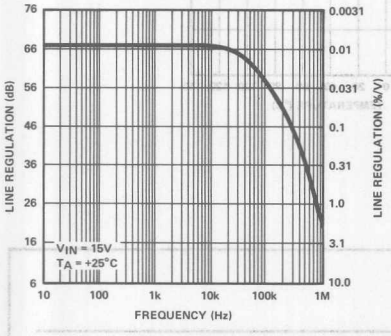
BURN-IN CIRCUIT



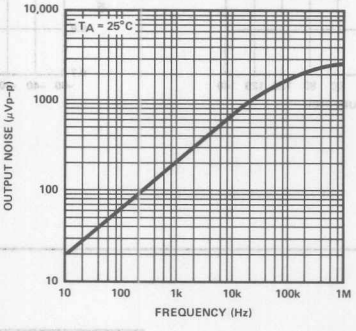
6

TYPICAL PERFORMANCE CHARACTERISTICS

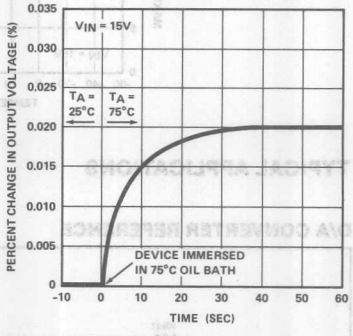
LINE REGULATION vs FREQUENCY



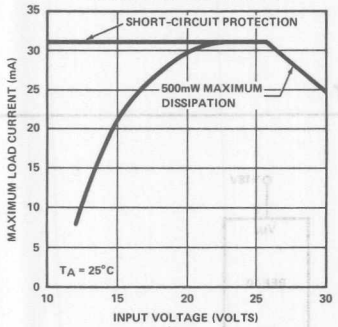
OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



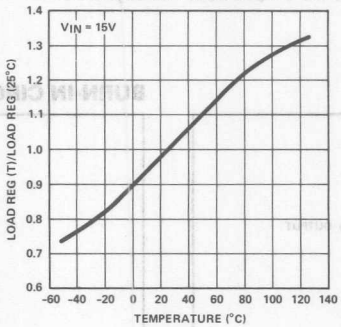
OUTPUT CHANGE DUE TO THERMAL SHOCK



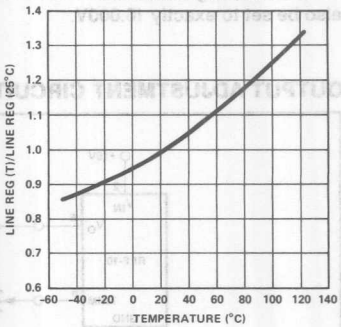
MAXIMUM LOAD CURRENT vs INPUT VOLTAGE



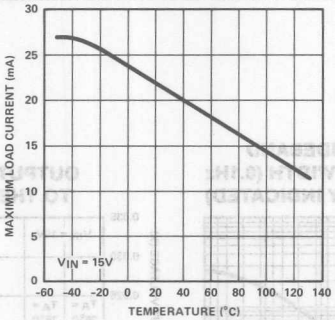
NORMALIZED LOAD REGULATION (ΔI_L = 10mA) vs TEMPERATURE



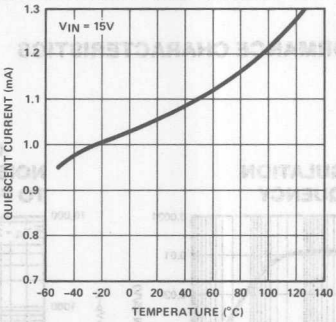
NORMALIZED LINE REGULATION vs TEMPERATURE



MAXIMUM LOAD CURRENT vs TEMPERATURE

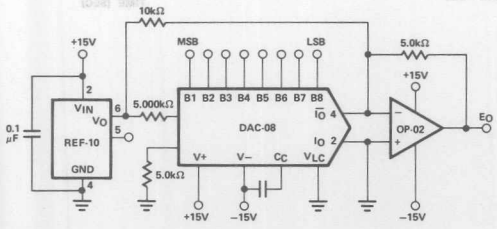


QUIESCENT CURRENT vs TEMPERATURE



TYPICAL APPLICATIONS

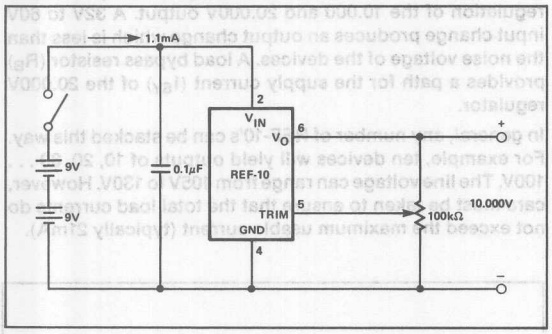
D/A CONVERTER REFERENCE



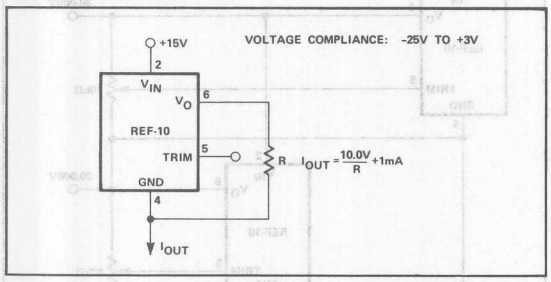
	B1	B2	B3	B4	B5	B6	B7	B8	E
POS FULL-SCALE −1LSB	1	1	1	1	1	1	1	1	+4.960
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000
NEG FULL-SCALE +1LSB	0	0	0	0	0	0	0	1	−4.960
NEG FULL-SCALE	0	0	0	0	0	0	0	0	−5.000

TYPICAL APPLICATIONS

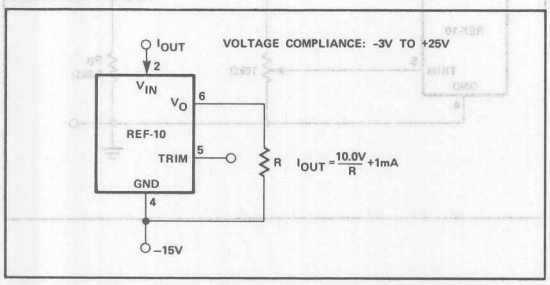
PRECISION CALIBRATION STANDARD



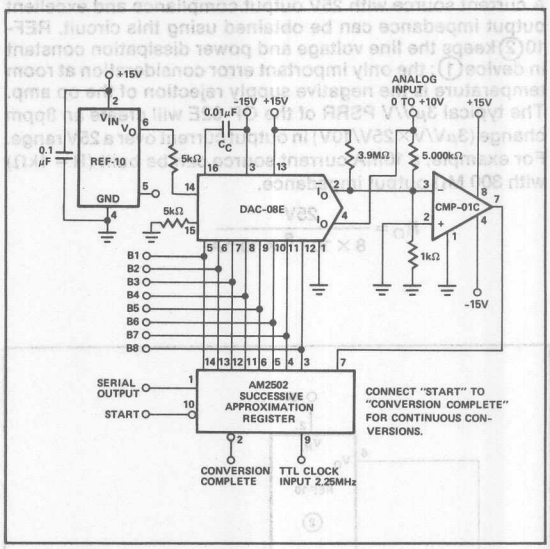
CURRENT SOURCE



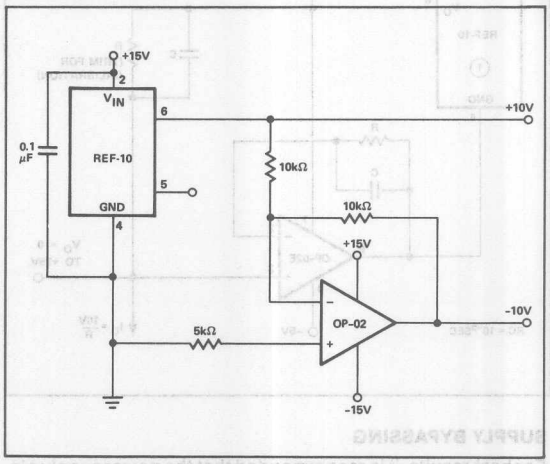
CURRENT SINK



A/D CONVERTER REFERENCE



±10V REFERENCE

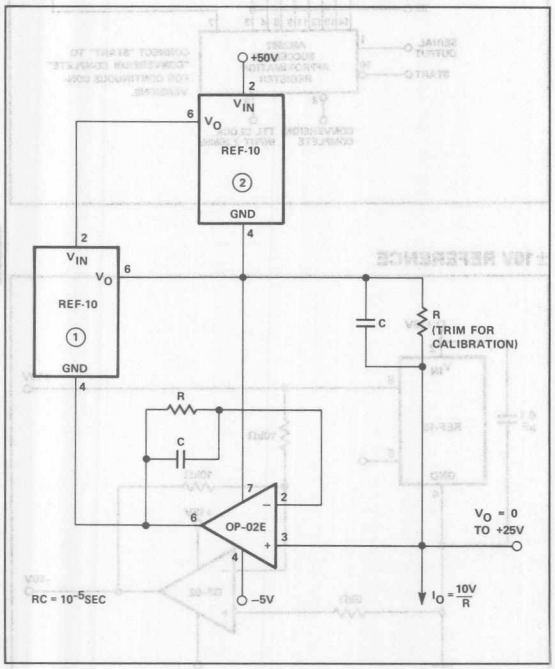


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PRECISION CURRENT SOURCE

A current source with 25V output compliance and excellent output impedance can be obtained using this circuit. REF-10(2) keeps the line voltage and power dissipation constant in device(1); the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical 3μV/V PSRR of the OP-02E will create an 8ppm change (3μV/V × 25V/10V) in output current over a 25V range. For example, a 10mA current source can be built (R = 1kΩ) with 300 MΩ output impedance.

$$R_O = \frac{25V}{8 \times 10^{-6} \times 10mA}$$



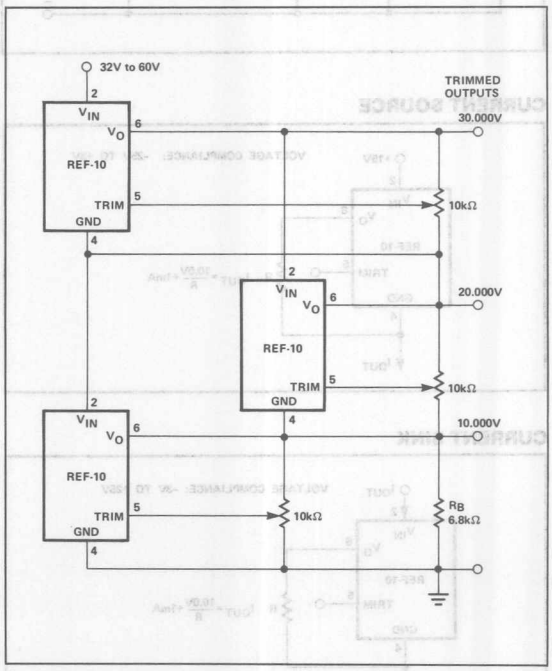
SUPPLY BYPASSING

For best results, it is recommended that the power supply pin is bypassed with a 0.1μF disc ceramic capacitor.

REFERENCE STACK WITH EXCELLENT LINE REGULATION

Three REF-10's can be stacked to yield 10.000, 20.000 and 30.000V outputs. An additional advantage is near-perfect line regulation of the 10.000 and 20.000V output. A 32V to 60V input change produces an output change which is less than the noise voltage of the devices. A load bypass resistor (R_B) provides a path for the supply current (I_{SY}) of the 20.000V regulator.

In general, any number of REF-10's can be stacked this way. For example, ten devices will yield outputs of 10, 20, 30 . . . 100V. The line voltage can range from 105V to 130V. However, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21mA).



REF-43

FEATURES

- +2.5 Volt Output ..... ±0.05% Max
- Low Temperature Coefficient ..... 10ppm/°C Max
- Excellent Regulation
  - Load Regulation ..... 20ppm/mA Max
  - Line Regulation ..... 2ppm/V Max
- Supply Current ..... 450μA Max
- Temperature Voltage Output ..... +1.9mV/°C
- Operating Voltage Range ..... +4.5V to +40V
- Extended Industrial Temp Range ..... −40°C to +85°C
- Available in Die Form

ORDERING INFORMATION †

	PACKAGE				OPERATING
TCV_O	TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	TEMPERATURE RANGE
10	REF43BJ*	REF43BZ*	–	REF43BRC/883*	MIL
10	REF43FJ	REF43FZ	–	–	XIND
25	REF43GJ	REF43GZ	REF43GP	–	XIND
25	–	–	REF43GS	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

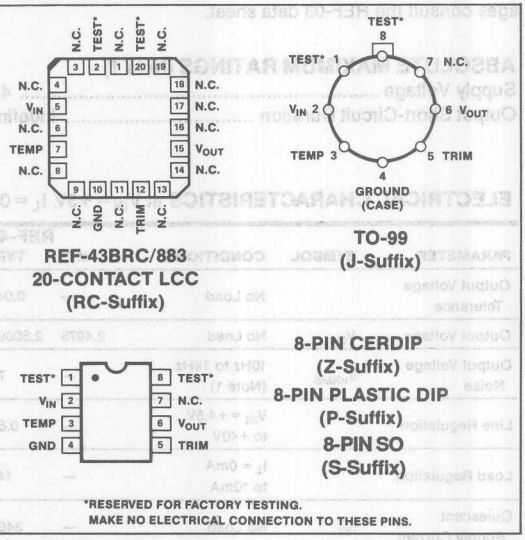
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

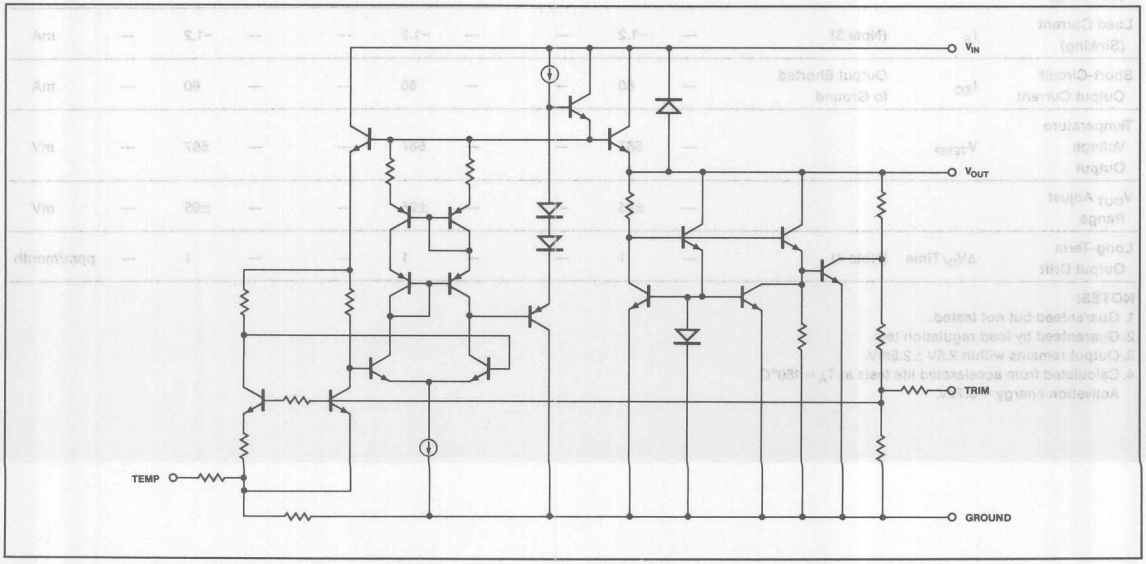
The REF-43 is a low-power precision reference providing a stable +2.5V output independent of variations in supply voltage, load conditions or ambient temperature. It is suitable as a reference level for 8, 10 and 12-bit data acquisition systems, or wherever a stable, known voltage is required.

Tight output tolerances and low thermal drift are assured by zener-zap trimming of both output voltage and its temperature coefficient. A unique curvature correction circuit reduces the thermal curvature which is characteristic of many previous bandgap references.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



to +40V. The output voltage changes by less than 178μV from one extreme of supply voltage to the other. With only 450μA maximum quiescent current, the REF-43 is ideally suited to applications where power dissipation must be minimized, as in precision battery-powered equipment. The low supply current minimizes drift due to self-heating after power-up.

A temperature output provides a means of determining system ambient temperature. Applications of the REF-43 include A/D and D/A conversion, 4-20mA transmitter/receiver operation, log amplifiers, and power-supply regulators.

For a low-cost 2.5V reference available in small-outline packages consult the REF-03 data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage 40V
Output Short-Circuit Duration ..... Indefinite
REF-43F (J, Z) ..... –40°C to +85°C
REF-43G (J, Z, P, S) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +175°C
Junction Temperature Range ..... –65°C to +175°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_{IN} = +5V, I_L = 0mA, T_A = 25°C unless otherwise noted.

			REF-43B			REF-43F			REF-43G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Output Voltage Tolerance		No Load	—	0.04	0.1	—	0.02	0.06	—	0.04	0.1	%
Output Voltage	V_O	No Load	2.4975	2.5000	2.5025	2.4985	2.5000	2.5015	2.4975	2.5000	2.5025	V
Output Voltage Noise	e_{nRMS}	10Hz to 1kHz (Note 1)	—	7	10	—	7	10	—	7	10	μV_{RMS}
Line Regulation		V_{IN} = +4.5V to +40V	—	0.8	2	—	0.8	2	—	0.8	2	ppm/V
Load Regulation		I_L = 0mA to 10mA	—	14	20	—	14	20	—	14	20	ppm/mA
Quiescent Supply Current	I_{SY}	No Load	—	340	450	—	340	450	—	340	450	μA
Load Current (Sourcing)	I_L	(Note 2)	10	20	—	10	20	—	10	20	—	mA
Load Current (Sinking)	I_S	(Note 3)	—	–1.2	—	—	–1.2	—	—	–1.2	—	mA
Short-Circuit Output Current	I_{SC}	Output Shorted to Ground	—	60	—	—	60	—	—	60	—	mA
Temperature Voltage Output	V_{TEMP}		—	567	—	—	567	—	—	567	—	mV
V_{OUT} Adjust Range			—	±95	—	—	±95	—	—	±95	—	mV
Long-Term Output Drift	ΔV_O/Time	(Note 4)	—	1	—	—	1	—	—	1	—	ppm/month

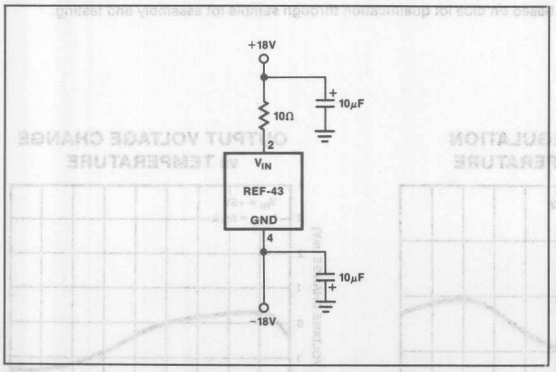
NOTES:
1. Guaranteed but not tested.
2. Guaranteed by load regulation test.
3. Output remains within 2.5V ±2.5mV.
4. Calculated from accelerated life tests at T_A = 150°C. Activation energy = 0.7eV.

ELECTRICAL CHARACTERISTICS at V_{IN} = +5V, I_L = 0mA, –55°C ≤ T_A ≤ +125°C for the REF-43B and –40°C ≤ T_A ≤ +85°C for the REF-43F/G, unless otherwise noted.

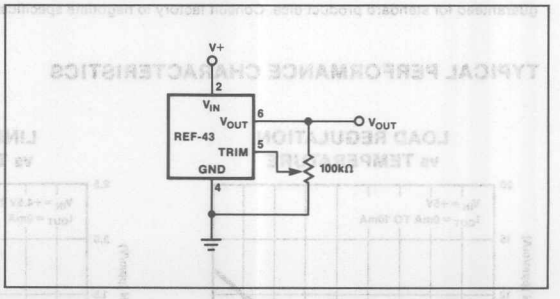
PARAMETER	SYMBOL	CONDITIONS	REF-43B MIN	REF-43B TYP	REF-43B MAX	REF-43F MIN	REF-43F TYP	REF-43F MAX	REF-43G MIN	REF-43G TYP	REF-43G MAX	UNITS
Output Voltage Tolerance		No Load	–	0.1	0.2	–	0.06	0.12	–	0.1	0.2	%
Output Voltage	V_O	No Load	2.495	2.500	2.505	2.497	2.500	2.503	2.495	2.500	2.505	V
Output Voltage Temperature Coefficient	TCV_O	–55°C ≤ T_A ≤ +125°C –40°C ≤ T_A ≤ +85°C (Note 1)	– –	6 –	10 –	– –	– 6	– 10	– –	– 10	– 25	ppm/°C
Line Regulation		V_{IN} = +4.5V to +40V	–	1	3	–	1	3	–	1	3	ppm/V
Load Regulation		I_L = 0mA to 10mA	–	25	40	–	20	35	–	25	40	ppm/mA
Quiescent Supply Current	I_{SY}	No Load	–	400	600	–	400	600	–	400	600	µA
Load Current (Sourcing)	I_L	(Note 2)	10	20	–	10	20	–	10	20	–	mA
Temperature Hysteresis of Output Voltage		ΔT = ±25°C	–	100	–	–	100	–	–	100	–	µV
Temperature Voltage Output Tempco	TCV_{TEMP}		–	1.9	–	–	1.9	–	–	1.9	–	mV/°C

NOTES:
1. Output voltage temperature coefficient is measured by the box method. The tempco is defined as the slope of the diagonal of a box drawn around the output voltage plotted against temperature. V_{OUT} is measured at T_{MIN}, 25°C and T_{MAX} for the applicable temperature range. The lowest of these three readings is subtracted from the highest reading and the resulting difference is divided by (T_{MAX} - T_{MIN}).
2. Guaranteed by Load Regulation test.

BURN-IN CIRCUIT

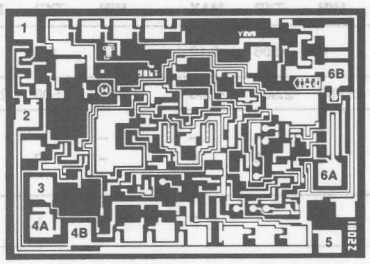


OUTPUT VOLTAGE TRIM METHOD



6

DICE CHARACTERISTICS



DIE SIZE 0.085 × 0.062 inch, 5270 sq. mils
(2.16 × 1.57 mm, 3.39 sq. mm)

2. V_{IN}
3. TEMPERATURE OUT
4A. GROUND*
4B. GROUND*
5. TRIM
6A. V_{OUT} FORCE†
6B. V_{OUT} SENSE†

*PADS 4A AND 4B MUST BOTH BE BONDED TO GROUND.
†V_{OUT} FORCE AND SENSE ARE TYPICALLY BONDED TOGETHER AT THE LOAD.

WAFER TEST LIMITS at $V_S = +5V$, $T_j = 25°C$, unless otherwise noted.

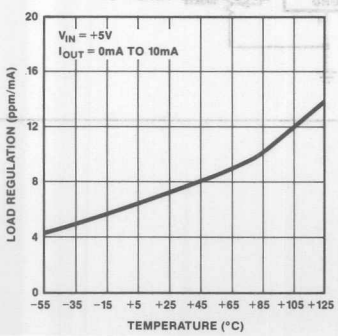
PARAMETER	SYMBOL	CONDITIONS	REF-43N LIMIT	UNITS
Output Voltage Tolerance		No Load	2.500 ± 0.005	V MAX
		(Note 1)	0.2	% MAX
Line Regulation		$V_{IN} = +4.5V$ to $+40V$	2	ppm MAX
Load Regulation		$I_L = 0mA$ to $10mA$	20	ppm MAX
Quiescent Supply Current	I_{SY}	No Load	450	µA MAX
Load Current (Sourcing)	I_L	(Note 2)	10	mA MIN

NOTES:
1. Final output trims are not performed on standard product dice. These trims are typically performed after packaging. Precision Monolithics Inc. assumes no responsibility for improper trimming by the customer. Contact factory for trim methods.
2. Guaranteed by load regulation test.

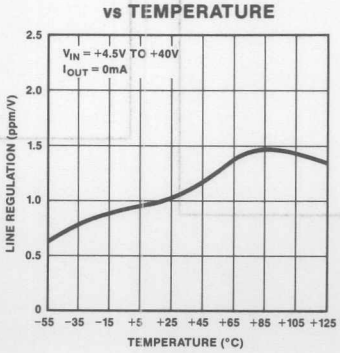
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

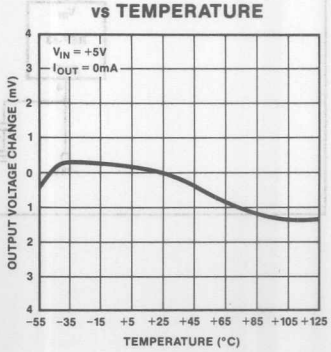
LOAD REGULATION vs TEMPERATURE



LINE REGULATION vs TEMPERATURE

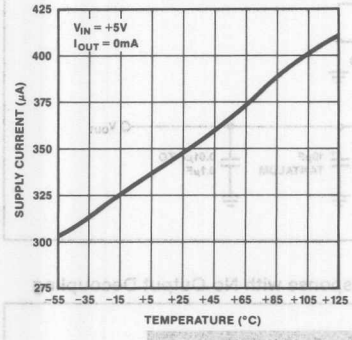


OUTPUT VOLTAGE CHANGE vs TEMPERATURE

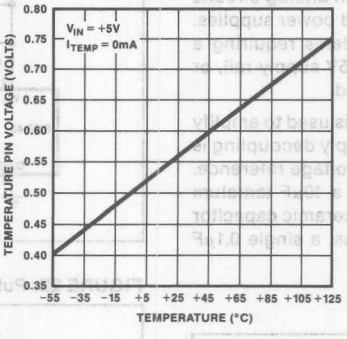


TYPICAL PERFORMANCE CHARACTERISTICS

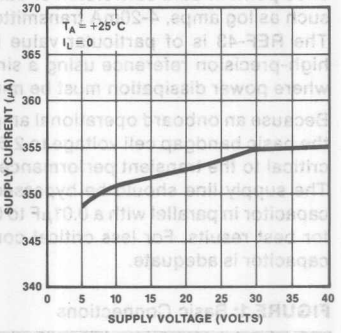
SUPPLY CURRENT vs TEMPERATURE



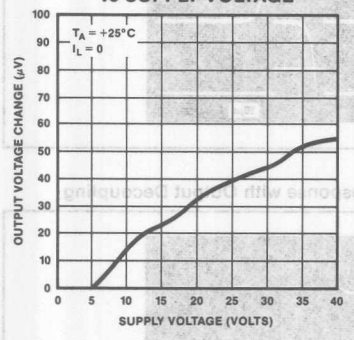
TEMPERATURE PIN VOLTAGE vs TEMPERATURE



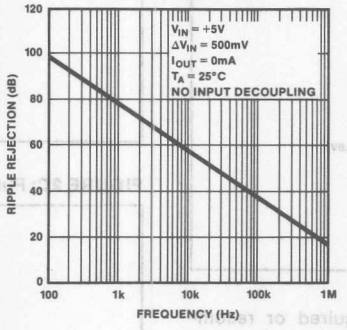
SUPPLY CURRENT vs SUPPLY VOLTAGE



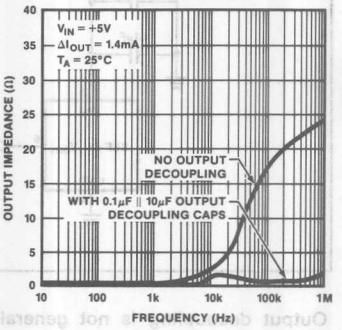
OUTPUT VOLTAGE CHANGE vs SUPPLY VOLTAGE



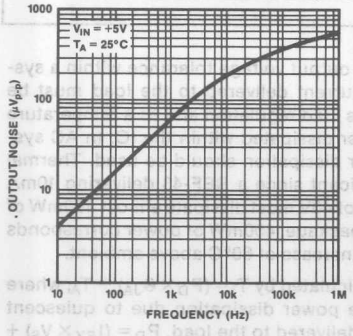
RIPPLE REJECTION vs FREQUENCY



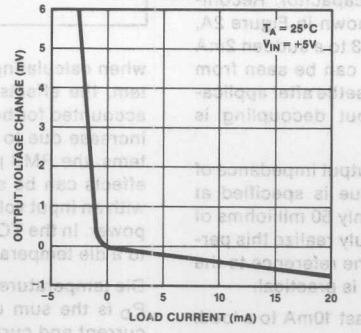
OUTPUT IMPEDANCE vs FREQUENCY



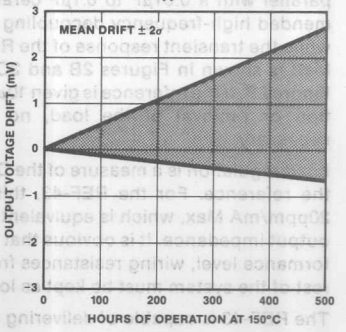
WIDEBAND OUTPUT NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



OUTPUT VOLTAGE CHANGE vs LOAD CURRENT



BURN-IN DRIFT AT T_A = 150°C

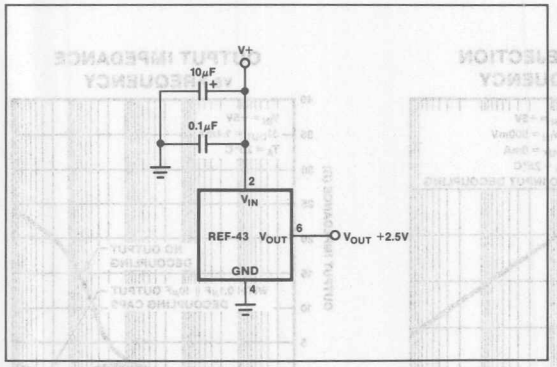


6

REF-43 provides a stable +2.5V output voltage with minimal dependence on load current, line voltage or temperature. This voltage is typically used to set an absolute reference point in data conversion circuits, or in analog circuits such as log amps, 4-20mA transmitters and power supplies. The REF-43 is of particular value in systems requiring a high-precision reference using a single +5V supply rail, or where power dissipation must be minimized.

Because an onboard operational amplifier is used to amplify the basic bandgap cell voltage to 2.5V, supply decoupling is critical to the transient performance of a voltage reference. The supply line should be bypassed with a 10μF tantalum capacitor in parallel with a 0.01μF to 0.1μF ceramic capacitor for best results. For less critical conditions, a single 0.1μF capacitor is adequate.

FIGURE 1: Basic Connections



Output decoupling is not generally required or recommended, except to achieve the lowest possible high-frequency output impedance when loads are being switched in and out quickly. As was the case with supply decoupling, best results will be achieved with a 10μF tantalum capacitor in parallel with a 0.01μF to 0.1μF ceramic capacitor. Recommended high-frequency decoupling is shown in Figure 2A, while the transient response of the REF-43 to a sudden 2mA load is shown in Figures 2B and 2C. As can be seen from Figure 2B, if the reference is given 10μs to settle after application or removal of the load, no output decoupling is necessary.

Load regulation is a measure of the DC output impedance of the reference. For the REF-43, this value is specified at 20ppm/mA Max, which is equivalent to only 50 milliohms of output impedance. It is obvious that to truly realize this performance level, wiring resistances from the reference to the rest of the system must be kept as low as is practical.

The REF-43 is capable of delivering at least 10mA to a load. To maintain its precision operation, loads should be kept within the 10mA specification. High-speed testing requires that load regulation is measured on a pulse basis, therefore

High-Frequency Pulse Response

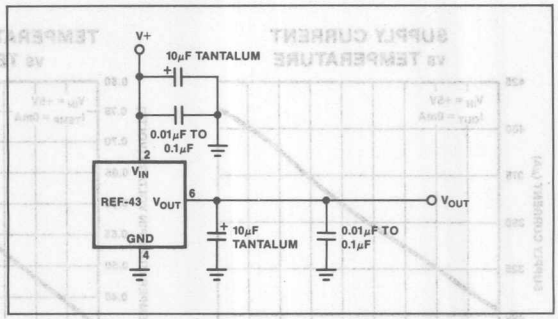


FIGURE 2B: Pulse Response with No Output Decoupling

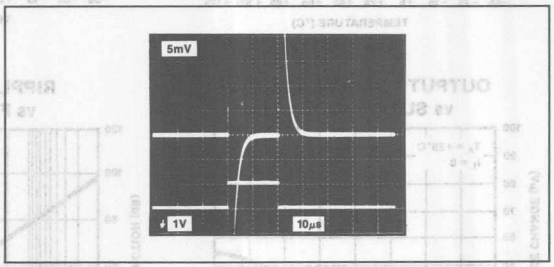
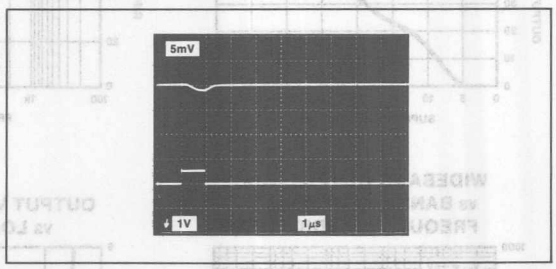


FIGURE 2C: Pulse Response with Output Decoupling



when calculating the output voltage tolerance within a system, the effects of current delivered to the load must be accounted for both as load regulation and as a temperature increase due to power dissipated within the IC. In AC systems, the RMS power dissipation should be used. Thermal effects can be significant since a REF-43 delivering 10mA with an input voltage of 40V must dissipate almost 400mW of power. In the TO-99 package, 400mW of power corresponds to a die temperature increase of 60°C above ambient.

Die temperature is calculated by $T_j = (P_D \times \Theta_{JA}) + T_A$, where P_D is the sum of the power dissipation due to quiescent current and current delivered to the load, $P_D = (I_{SY} \times V_S) + (I_{LOAD} \times (V_S - 2.5V))$. The Θ_{JA} for different packages in a PC board surrounded by free air are listed below.

PACKAGE TYPE	TYP Θ_{JA}(°C/W)
TO-99	150
CERDIP	80
PLASTIC	80
LCC	110

An additional source of error is due to temperature gradients across the package leads, resulting in thermocouple effects. Temperature gradients will be generated when the IC is required to dissipate large amounts of power. Even at low power levels, thermocouple effects may appear as low frequency noise due to air currents across the leads. A significant improvement in low-frequency noise will be found by encasing the reference and any metal junctions such as solder joints (which form thermocouples) along the reference path in a light insulating foam or other enclosure to reduce turbulence. Thermocouple effects can easily add over $10\mu V_{p-p}$ of low-frequency noise.

The temperature output of the REF-43 provides an output voltage which is proportional to the die temperature. When the REF-43 is operating at constant load current, this is a good indication of system temperature. The nominal output voltage at 25°C is 567mV, and the slope is typically 1.9mV/°C(±0.2mV/°C). The TEMP output is affected by the internal trimming done for output voltage tolerance, and will vary between units. If the temperature pin 3 is connected to external circuitry, it should be buffered by an op amp. Current into or out of pin 3 will change the temperature coefficient and curvature of the output voltage, while capacitance at the pin can create instabilities within the reference amplifier.

GENERATING A −2.5V REFERENCE

Often, there is a requirement for a negative reference voltage. The simplest method of generating a −2.5V reference with the REF-43 is to connect an op amp in a gain of −1 to the output, as shown in Figure 3. This provides both positive and negative 2.5V references. Figure 4 shows another method of obtaining a negative reference, in which the current-output

FIGURE 3: ±2.5V Reference

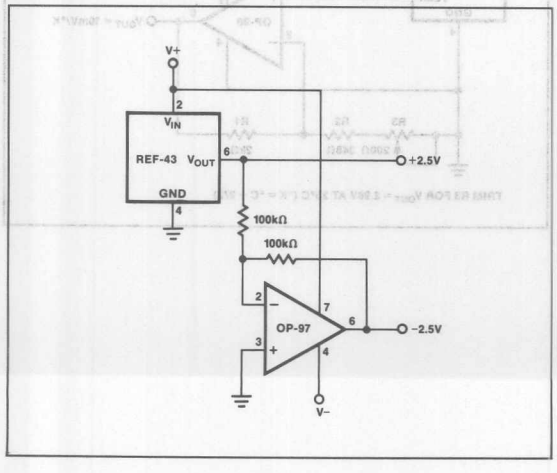
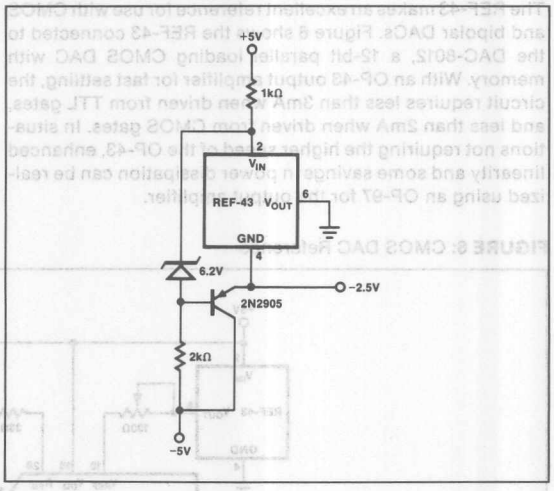


FIGURE 4: −2.5V Reference

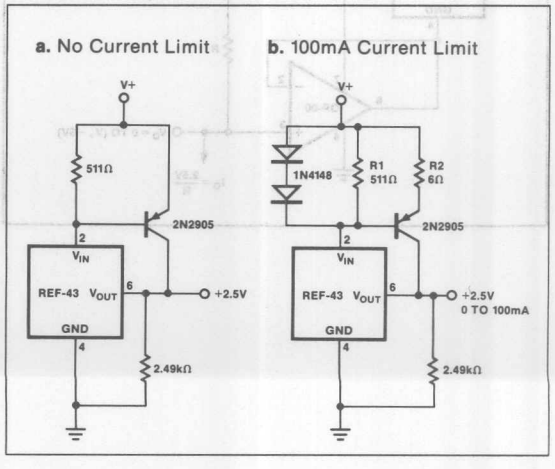


element is a PNP transistor, with the REF-43 in a servo loop to ensure that the output remains 2.5V below ground.

BOOST TRANSISTOR PROVIDES HIGH OUTPUT CURRENT

When applications require more than 10mA current delivery, an external boost transistor may be added to the REF-43 to pass the required current without dissipating excessive power within the IC. The maximum current output to the system is bounded only by the capabilities of the boost transistor. This technique is shown in Figure 5 with and without current limiting. Current limiting may be used to prevent damage to the boost transistor. In Figure 5b, the limit occurs when the voltage dropped across R2 exceeds one V_{BE}(0.6V). The current limit is sensitive to the variations of the diodes' forward drop and the PNP's V_{BE} with temperature, and will decrease with increasing temperature.

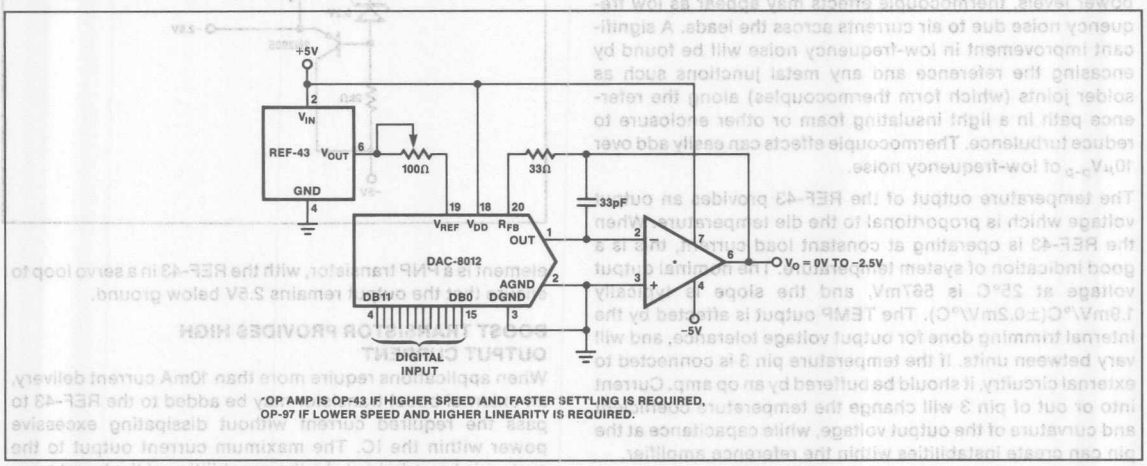
FIGURE 5: Output Current Boost



LOW-POWER CMOS DAC REFERENCE

The REF-43 makes an excellent reference for use with CMOS and bipolar DACs. Figure 6 shows the REF-43 connected to the DAC-8012, a 12-bit parallel loading CMOS DAC with memory. With an OP-43 output amplifier for fast settling, the circuit requires less than 3mA when driven from TTL gates, and less than 2mA when driven from CMOS gates. In situations not requiring the higher speed of the OP-43, enhanced linearity and some savings in power dissipation can be realized using an OP-97 for the output amplifier.

FIGURE 6: CMOS DAC Reference



PRECISION CURRENT SOURCE

Current sources are often required in analog processing and computational circuits. The circuit of Figure 7 shows a high-output-impedance current source capable of single-supply operation. Performance is optimal at current levels below 1mA, since output voltage changes directly affect the power dissipated within the REF-43.

FIGURE 7: Precision Current Source

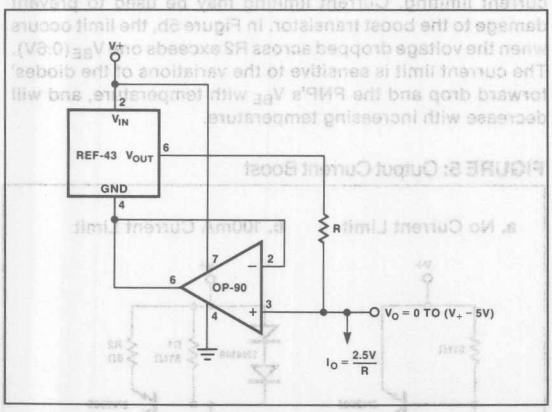
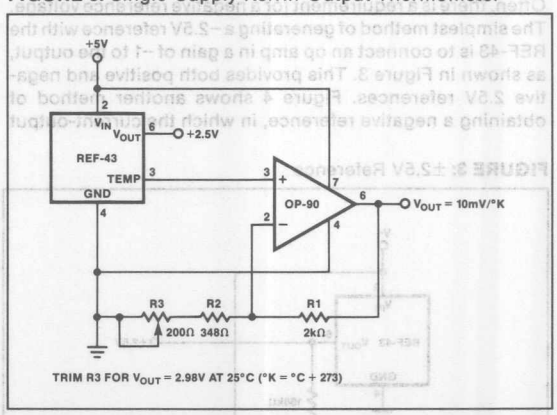
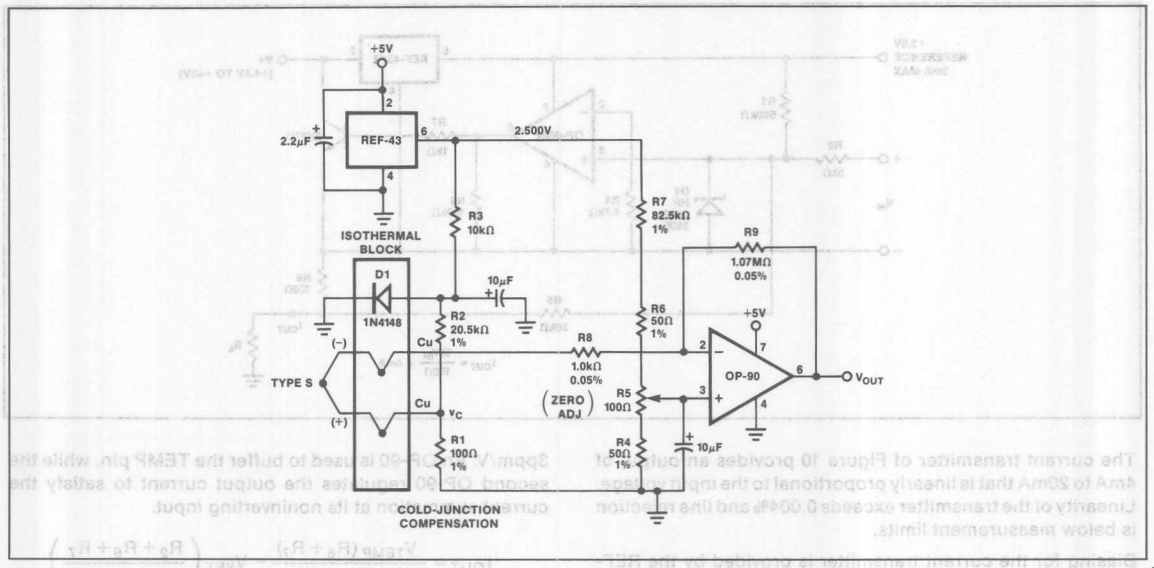


FIGURE 8: Single-Supply Kelvin-Output Thermometer





TEMPERATURE MEASUREMENT

Using the REF-43's TEMP output, a Kelvin-output thermometer that operates off a single +5V supply can be built as shown in Figure 8. Since the output of the REF-43's TEMP pin is theoretically zero at 0°K, trimming R3 adjusts both the slope and zero point. In actuality, the ±40mV zero point found by extrapolating the TEMP voltage vs. actual temperature to zero will create a small error. A 4-20mA temperature transmitter is described on page 10 which uses two trims to eliminate this inaccuracy.

For wider temperature ranges than semiconductors can withstand, thermocouples are commonly used. Depending upon the type used, a thermocouple can measure temperatures over 1000°C. Thermocouples require a reference junction, at a known temperature, usually 0°C. Since it is not generally convenient to have an ice bath, electronic methods of simulating this junction have been developed, called cold-junction compensation. In Figure 9, diode D1 is mounted isothermally to the termination of the thermocouple, and along with R1 and R2 provides the cold-junction compensation required for accurate measurement. Using an OP-90 as the amplifier, the circuit will operate off a single +5V supply and is capable of measuring temperatures from 0°C to +400°C. If negative temperatures must be measured, dual supplies must be used to allow the op amp to swing negative. In cases where the electronics are subject to temperature fluctuations, an OP-77 is recommended for its extremely low TCV_{OS}.

Calibration of the thermocouple amplifier is done after a 15 minute warm-up time using R5. A copper wire short is placed across the thermocouple terminating junctions, simulating a 0°C condition. R5 is then adjusted for a 0.00V output. The short is then removed and the amplifier is ready for use. Note that special care must be used in calibration when this circuit is operated single-supply, as the output of the OP-90 will swing to within 500μV of ground, but not below ground. Thus R5 must be trimmed to the point where the output just barely reaches its swing limit.

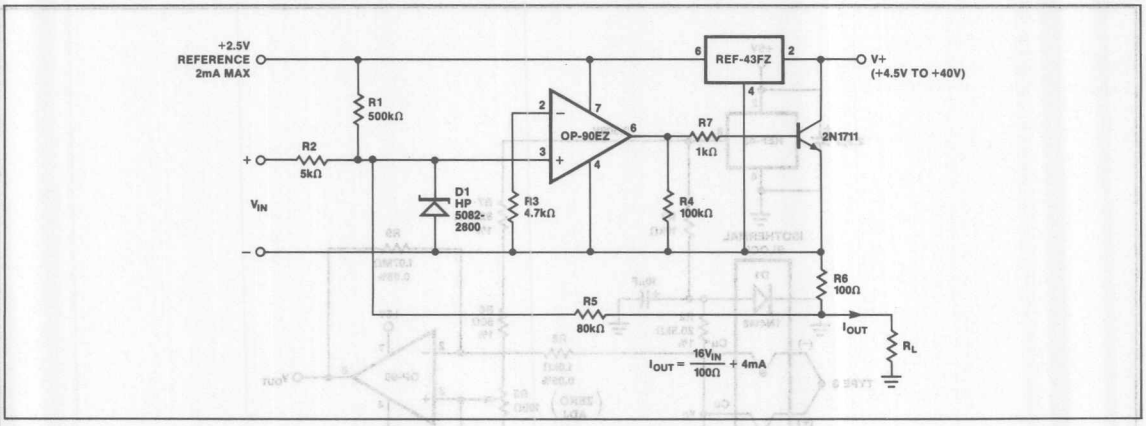
By changing the appropriate resistor values, the amplifier may be used with type S, J or K thermocouples. In all cases, the output has been scaled with R9 to provide an output of 10mV/°C.

TYPE	SEEBECK COEFFICIENT, α	R1	R2	R7	R9
K	39.2μV/°C	110Ω	5.76kΩ	102kΩ	269kΩ
J	50.2μV/°C	100Ω	4.02kΩ	80.6kΩ	200kΩ
S	10.3μV/°C	100Ω	20.5kΩ	392kΩ	1.07MΩ

TWO-WIRE 4-20mA TRANSMITTERS

4-20mA current loops are used in noisy environments for many types of remote data acquisition. With a two-wire loop, the sensing circuitry can be powered with the same lines used for signal transmission.

FIGURE 10: Two Wire 4-20mA Transmitter



The current transmitter of Figure 10 provides an output of 4mA to 20mA that is linearly proportional to the input voltage. Linearity of the transmitter exceeds 0.004% and line rejection is below measurement limits.

Biasing for the current transmitter is provided by the REF-43FZ. The OP-90EZ regulates the output current to satisfy the current summation at the noninverting node:

$$I_{OUT} = \frac{1}{R6}\left(\frac{V_{IN}\,R5}{R2} + \frac{2.5V\,R5}{R1}\right)$$

For the values shown in Figure 10,

$$I_{OUT} = \left(\frac{16}{100\Omega}\right)V_{IN} + 4mA$$

giving a full-scale output of 20mA with a 100mV input. Adjustment of R2 will provide an offset trim and adjustment of R1 will provide a gain trim. These trims do not interact since the noninverting input of the OP-90 is at virtual ground. The Schottky diode, D1, prevents input voltage spikes from pulling the noninverting input more than 300mV below the inverting input. Without the diode, such spikes could cause phase reversal of the OP-90 and possible latch-up of the transmitter. Compliance of this circuit is from 4.5V to 40V. The voltage reference output can provide up to 2mA for transducer excitation.

The OP-90 is also available in dual and quad versions. Using an OP-490, three of the amplifiers can be used to implement a full instrumentation amplifier for signal conditioning before delivery to the 4-20mA transmitter. All four OP-90s require less than 80μA supply current, and thus have virtually no impact on the current-budget of the 4-20mA loop.

A simple temperature to 4-20mA transmitter is shown in Figure 11. After calibration, the transmitter is accurate to within 1°C over the −50°C to +150°C temperature range. The transmitter operates from +6V to +40V with supply rejection better than 3ppm/V. An OP-90 is used to buffer the TEMP pin, while the second OP-90 regulates the output current to satisfy the current summation at its noninverting input.

$$I_{OUT} = \frac{V_{TEMP}\,(R_6 + R_7)}{R_2\,R_{10}} - V_{SET}\left(\frac{R_2 + R_6 + R_7}{R_2\,R_{10}}\right)$$

The change in output current with temperature is the derivative of the transfer function:

$$\frac{\Delta I_{OUT}}{\Delta T} = \frac{\frac{\Delta V_{TEMP}}{\Delta T}\,(R_6 + R_7)}{R_2\,R_{10}}$$

From the formulas, it can be seen that if the gain trim is adjusted before the final offset trim, the two trims are not interactive, which greatly simplifies the calibration procedure.

To calibrate the transmitter, begin by placing the REF-43 in an ice water (0°C) bath. If necessary, adjust the offset trim, R5, so that the output current is above 4mA.

Record the output current. Next, place the REF-02 in a boiling water (100°C) bath. Adjust the gain trim, R6, so that the change in the output current reflects the desired mA/°C ratio described as follows:

$$\text{Output Ratio} = \frac{\Delta I_{FS}}{\Delta T_{OPERATING}} = \frac{16mA}{\Delta T_{OPERATING}}$$

As an example, assume the transmitter is to operate over the −50°C to +150°C temperature range:

$$\text{Output Ratio} = \frac{16mA}{(150°C - 50°C)} = \frac{16mA}{(200°C)} = 0.08mA/°C$$

If I_{OUT} in the ice water bath equaled 6.3mA, then in the boiling water bath:

$$I_{OUT(100°C)} = I_{OUT(0°C)} + 100°C\ (0.08mA/°C)$$
$$= 6.3mA + 8mA = 14.3mA$$

With the REF-43 in the boiling water bath, the gain trim, R6, in this example should be adjusted so I_{OUT} equals 14.3mA.

Once the gain trim has been completed, the offset trim can be made. Remember, that adjusting the offset trim will not affect the gain.

The offset trim can be set at any known temperature by adjusting R5 until the output current equals:

$$I_{OUT} = \left(\frac{\Delta I_{FS}}{\Delta T_{OPERATING}}\right)(T_{AMBIENT} - T_{MIN}) + 4mA$$

Using the previous example and assuming the REF-43 is at 20°C:

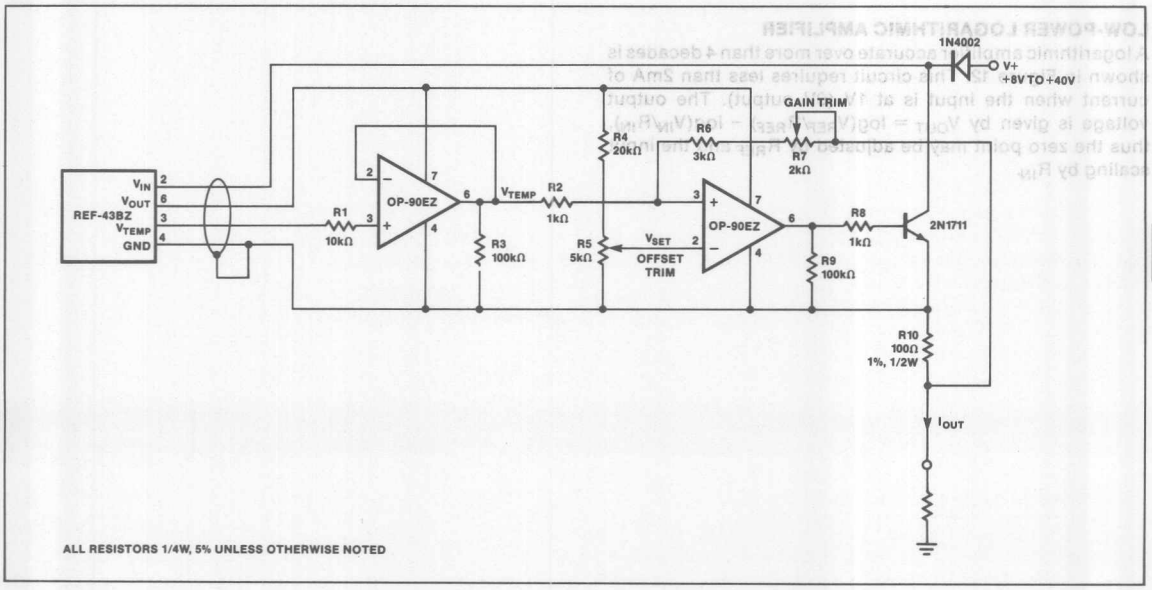
$$I_{OUT} = \left(\frac{16mA}{200°C}\right)\left[20°C - (-50°C)\right] + 4mA = 9.6mA$$

Table 1 shows the values of R6 and R7 required for various temperature ranges.

TABLE 1

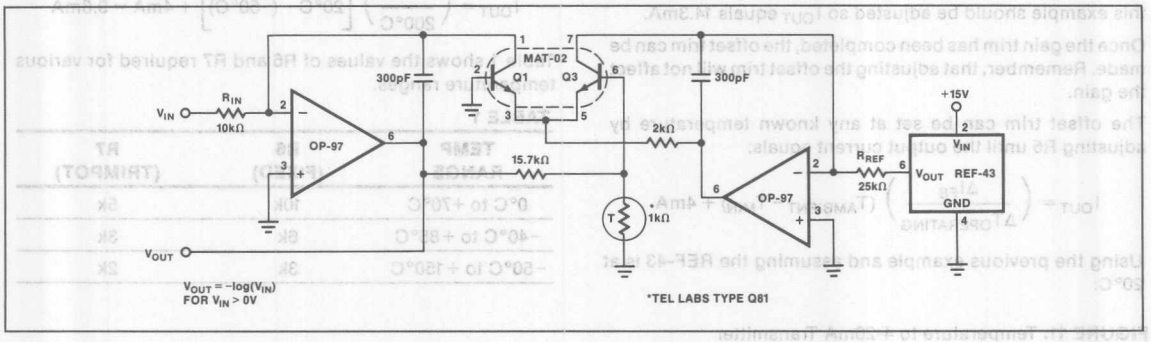
TEMP RANGE	R6 (FIXED)	R7 (TRIMPOT)
0°C to +70°C	10k	5k
−40°C to +85°C	6k	3k
−50°C to +150°C	3k	2k

FIGURE 11: Temperature to 4-20mA Transmitter



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FIGURE 12: Low Power Logarithmic Amplifier



LOW-POWER LOGARITHMIC AMPLIFIER

A logarithmic amplifier accurate over more than 4 decades is shown in Figure 12. This circuit requires less than 2mA of current when the input is at 1V (0V output). The output voltage is given by $V_{OUT} = \log(V_{REF}/R_{REF}) - \log(V_{IN}/R_{IN})$, thus the zero point may be adjusted by R_{REF} and the input scaling by R_{IN}.

Data Acquisition Subsystems
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Selection Guide
Data Acquisition Subsystems

Model	Resolution Bits	Throughput Rate kHz	No. Channels	Bus Interface	Package Options[1]	Temp Range[2]	Page	Comments
***AD1341**	**12**	**150**	**16/8**	**16**	**12**	**C, M**	**C II 7–25**	**Complete, Programmable DAS with Fast Bus Interface**
AD1332	**12**	**125**	**1**	**12**	**1**	**I, M**	**C II 7–17**	**Complete 12-Bit 125 kHz Sampling ADC, On-Chip FIFO**
AD1334	**12**	**65**	**4**	**12**	**1**	**I, M**	**C II 7–21**	**Four-Channel 12-Bit Sampling ADC, On-Chip FIFO**
AD364	12	20	16/8	12	1	C, M	C II 7–5	High Speed 16-Channel 12-Bit DAS
AD363	12	25	16/8	12	1	C, M	C II 7–5	16-Channel 12-Bit DAS
AD1362			16/8			C, M	C II 7–41	16-Channel Analog Front-End for 12-Bit ADC
AD79015	**12**	**10**	**1**	**Serial**	**2, 5**	**C**	**C II 7–49**	**Small Signal DAS with Instrumentation Amplifiers and Reference**
DAS1152	14	25	1	14	1	I	C II 7–65	14-Bit High Accuracy Sampling ADC
DAS1157	14	18	1	14	1	I	C II 7–69	Low Power 16-Bit Sampling ADC
DAS1153	15	25	1	15	1	I	C II 7–65	15-Bit High Accuracy Sampling ADC
DAS1158	15	18	1	15	1	I	C II 7–69	Low Power 15-Bit Sampling ADC
DAS1159	16	18	1	16	1	I	C II 7–69	Low Power 16-Bit Sampling ADC
***AD79024**	**20**	**0.30**	**1**	**Serial**	**2, 6**	**C**	**C II 7–57**	**Quad 20-Bit Sigma Delta ADC, Low Power**

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-In-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92.

[2]Temperature Ranges: C = Commercial, 0 to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.

Boldface type: Product recommended for new design.

*New product since the publication of the most recent Databooks.

Orientation
Data Acquisition Subsystems

Data acquisition subsystems provide many of the functional elements of a complete data acquisition system, in various combinations. By doing this, these subsystems allow complete performance to be provided and specified more easily than with systems built from individual components.

Among the functional blocks that data acquisition subsystems provide are:

- multiple channel input multiplexer
- programmable gain amplifier
- sample-hold amplifier
- microprocessor interface
- analog-to-digital converter
- converter reference

The data acquisition subsystems detailed on the following pages provide a wide span of performance capabilities. Resolutions of 12, 14, 15, 16 and 20 bits; gain ranges of 64:1 up to 512:1 and throughputs from 300 Hz to 150 kHz are available. These specifications must be compared along with input range, package size, power consumption and linearity to decide which data acquisition subsystem, if any, is best for the application.

Complete 16-Channel, 12-Bit Data Acquisition Systems

AD363/AD364

FEATURES

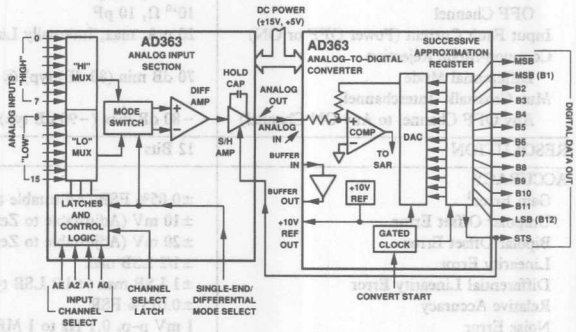
AD363

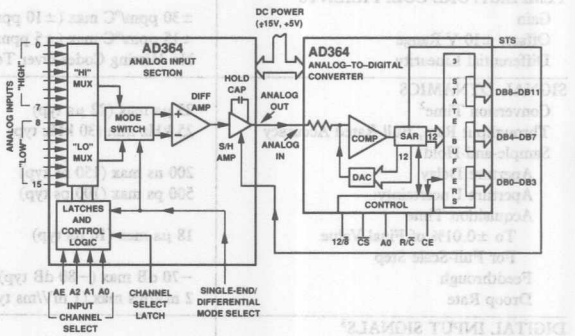
16-Channel Data Acquisition Input Stage with:
- **Digitally Controlled Channel Selection/Mode Control**
- **16 Single-Ended or 8 Differential Channels**
- **25 kHz Throughput Rate**
- **Guaranteed No Missing Codes Over Temperature**

AD364

16-Channel Data Acquisition Input Stage with:
- **Digitally Controlled Channel Selection/Mode Control**
- **16 Single-Ended or 8 Differential Channels**
- **20 kHz Throughput Rate**
- **Guaranteed No Missing Codes Over Temperature**
- **Three-State Buffered Digital Output**

FUNCTIONAL BLOCK DIAGRAMS





PRODUCT DESCRIPTIONS

The AD363 and AD364 are complete 16-channel data acquisition systems which condition and subsequently convert an analog voltage into digital form. Each system consists of two devices, an analog input stage (AIS) and an analog-to-digital converter (ADC). The AIS includes a two 8-channel multiplexers, a channel address register, a unity gain instrumentation amplifier, and a sample-hold amplifier. The multiplexers may be connected to the instrumentation amplifier in either an 8-channel differential or 16-channel single ended configuration. A unique feature of these products is an internal user controlled switch which connects the multiplexers in either single-ended or differential mode. This allows a single device to perform in either mode with hard-wire programming and permits interfacing a mixture of single-ended and differential signals by dynamically switching the input mode control.

The AD363 and AD364 differ in ADC performance. Each ADC is a complete 12-bit successive approximation converter including an internal clock and a precision reference. Active laser trimming results in maximum linearity errors of ±0.012% with conversion times of 25 μs (AD363) or 32 μs (AD364). The hybrid AD363-ADC has five user selectable input ranges (±2.5, ±5.0, ±10.0, 0 to +5, and 0 to +10 volts) and includes a high impedance buffer amplifier. The AD364-ADC is a monolithic converter with 3-state output buffer circuitry for direct interface to an 8-, 12-, or 16-bit processor bus and three user selected input ranges (±5, ±10, and 0 to +10 volts).

Both products are specified for operation over both the commercial (0°C to +70°C) and military (−55°C to +125°C) temperature ranges. The AD363 and AD364 are available with environmental screening. Please contact the factory or nearest sales office for details.

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AD363/AD364—SPECIFICATIONS (typical @ +25°C, ±15 V and +5 V unless otherwise noted)

Parameter	AD363RK	AD363RS
ANALOG INPUTS		
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)	*
Input Voltage Ranges		
Bipolar	±2.5 V, ±5.0 V, ±10.0 V	*
Unipolar	0 to +5 V, 0 to +10 V	*
Input (Bias) Current, per Channel	±50 nA max	*
Input Impedance		
ON Channel	10^{10} Ω, 100 pF	*
OFF Channel	10^{10} Ω, 10 pF	*
Input Fault Current (Power OFF or ON)	20 mA, max, Internally Limited	*
Common-Mode Rejection		
Differential Mode	70 dB min (80 dB) typ) @ 1 kHz, 20 V p–p	*
Mux Crosstalk (Interchannel,		
Any OFF Channel to Any ON Channel)	−80 dB max (−90 dB typ) @ 1 kHz, 20 V p–p	*
RESOLUTION	12 Bits	*
ACCURACY		
Gain Error[1]	±0.05% FSR (Adjustable to Zero)	*
Unipolar Offset Error	±10 mV (Adjustable to Zero)	*
Bipolar Offset Error	±20 mV (Adjustable to Zero)	*
Linearity Error	±1/2 LSB max	*
Differential Linearity Error	±1 LSB max (±1/2 LSB typ)	*
Relative Accuracy	±0.025% FSR	*
Noise Error	1 mV p–p, 0.1 Hz to 1 MHz	*
TEMPERATURE COEFFICIENTS		
Gain	±30 ppm/°C max (±10 ppm/°C typ)	±25 ppm/°C max (±15 ppm/°C typ)
Offset, ±10 V Range	±15 ppm/°C max (±5 ppm/°C typ)	±8 ppm/°C max (±5 ppm/°C typ)
Differential Linearity	No Missing Codes Over Temperature Range	*
SIGNAL DYNAMICS		
Conversion Time[2]	25 µs max (22 µs typ)	*
Throughput Rate, Full Rated Accuracy	25 kHz min (30 kHz typ)	*
Sample-and-Hold		
Aperture Delay	200 ns max (150 ns typ)	*
Aperture Uncertainty	500 ps max (100 ps typ)	*
Acquisition Time		
To ±0.01% of Final Value	18 µs max (10 µs typ)	*
For Full-Scale Step		
Feedthrough	−70 dB max (−80 dB typ) @ 1 kHz	*
Droop Rate	2 mV/ms max (1 mV/ms typ)	*
DIGITAL INPUT SIGNALS[3]		
Convert Command (to ADC Section,		
Pin 21)	Positive Pulse, 200 ns min Width. Leading Edge	
	("0" to "1") Resets Register, Trailing Edge	
	("1" to "0") Starts Conversion	*
	1 TTL Load	*
Input Channel Select (to Analog		
Input Section, Pins 28–31)	4-Bit Binary Channel Address	*
	1 LS TTL Load	*
Channel Select Latch (to Analog		
(Input Section, Pin 32)	"1" Latch Transparent	*
	"0" Latched	*
	4 LS TTL Loads	*
Sample-Hold Command (to Analog		
Input Section Pin 13 Normally	"0" Sample Mode	*
Connected to ADC "Status,"	"1" Hold Mode	*
Pin 20)	2 LS TTL Loads	*
Short Cycle (to ADC Section Pin 14)	Connect to +5 V for 12-Bits Resolution	*
	Connect to Output Bit n + 1 for n Bits	
	Resolution	*
	1 TTL Load	*
Single-Ended/Differential Mode Select		
(to Analog Input Section, Pin 1)	"0" Single Ended Mode	*
	"1" Differential Mode (+4.0 V min)	*
	3 TTL Loads	*

Parameter	AD363RK	AD363RS
DIGITAL OUTPUT SIGNALS[3]		
(All Codes Positive True)		
Parallel Date		
Unipolar Code	Binary	*
Bipolar Code	Offset Binary/Twos Complement	*
Output Drive	2 TTL Loads	*
Serial Data (NRZ Format)		*
Unipolar Code	Binary	*
Bipolar Code	Offset Binary	*
Output Drive	2 TTL Loads	*
Status (Status)	Logic "1" ("0") During Conversion	*
Output Drive	2 TTL Loads	*
Internal Clock		
Output Drive	2 TTL Loads	*
Frequency	500 kHz	*
INTERNAL REFERENCE VOLTAGE	+10.00 V, ±10 mV	*
Max External Current	±1 mA	*
Voltage Temperature Coefficient	±20 ppm/°C max	*
POWER REQUIREMENTS		
Supply Voltages/Currents	+15 V, ±5% @ +45 mA max (+38 mA typ)	*
	−15 V, ±5% @ −45 mA max (−38 mA typ)	*
	+5 V, ±5% @ +136 mA max (+113 mA typ)	*
Total Power Dissipation	2 Watts max (1.7 Watts typ)	*
TEMPERATURE RANGE		
Specification	0°C to +70°C	−55°C to +125°C
Storage	−55°C to +150°C	−55°C to +150°C
PACKAGE OPTIONS		
Analog Input Section (DH-32E)	AD363RKD	AD363RSD
AD Section (DH-32C)	AD363RKD	AD363RSD

NOTES
[1]With 50 Ω, 1% fixed resistor in place of Gain Adjust pot.
[2]Conversion time of ADC Section.
[3]One TTL Load is defined as I_{IL} = −1.6 mA max @ V_{IL} = 0.4 V, I_{IH} = 40 μA max @ V_{IH} = 2.4 V. One LS TTL Load is defined as I_{IL} = −0.36 mA max @ V_{IL} = 0.4 V, I_{IH} = 20 μA max @ V_{IH} = 2.7 V.
*Specifications same as AD363RK.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (ALL MODELS)

+V, Digital Supply . . . . . +5.5 V
+V, Analog Supply . . . . . +16 V
−V, Analog Supply . . . . . −16 V
V_{IN}, Signal . . . . . ±V, Analog Supply
V_{IN}, Digital . . . . . 0 to +V, Digital Supply
AGND to DGND . . . . . ±1 V

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ANALOG INPUT SECTION		ANALOG-TO-DIGITAL CONVERTER SECTION	
Pin Number	**Function**	**Pin Number**	**Function**
1	Single-End/Differential Mode Select "0": Single-Ended Mode "1": Differential Mode (+4.0 V min)	1	Data Bit 12 (Least Significant Bit) Out
2	Digital Ground	2	Data Bit 11 Out
3	Positive Digital Power Supply, +5 V	3	Data Bit 10 Out
4	"High" Analog Input, Channel 7	4	Data Bit 9 Out
5	"High" Analog Input, Channel 6	5	Data Bit 8 Out
6	"High" Analog Input, Channel 5	6	Data Bit 7 Out
7	"High" Analog Input, Channel 4	7	Data Bit 6 Out
8	"High" Analog Input, Channel 3	8	Data Bit 5 Out
9	"High" Analog Input, Channel 2	9	Data Bit 4 Out
10	"High" Analog Input, Channel 1	10	Data Bit 3 Out
11	"High" Analog Input, Channel 0	11	Data Bit 2 Out
12	No Connect	12	Data Bit 1 (Most Significant Bit) Out
13	Sample-Hold Command "0": Sample Mode "1": Hold Mode Normally Connected to ADC Pin 20	13	$\overline{\text{Data Bit 1}}$ ($\overline{\text{MSB}}$) Out
14	Offset Adjust	14	Short Cycle Control Connect to +5 V for 12 Bits Connect to Bit (n + 1) Out for n Bits
15	Offset Adjust	15	Digital Ground
16	Analog Output Normally Connected to ADC "Analog In"	16	Positive Digital Power Supply, +5 V
17	Analog Ground	17	$\overline{\text{Status}}$ Out "0": Conversion in Progress (Parallel Data Not Valid) "1": Conversion Complete (Parallel Data Valid)
18	"High" ("Low") Analog Input, Channel 15 (7)	18	+10 V Reference Out
19	"High" ("Low") Analog Input, Channel 14 (6)	19	Clock Out (Runs During Conversion)
20	Negative Analog Power Supply, −15 V	20	Status Out "0": Conversion Complete (Parallel Data Valid) "1": Conversion in Progress (Parallel Data Not Valid)
21	Positive Analog Power Supply, +15 V	21	Convert Start In Reset Logic ↑ Start Convert ↓
22	"High" ("Low") Analog Input, Channel 13 (5)	22	Comparator In
23	"High" ("Low") Analog Input, Channel 12 (4)	23	Bipolar Offset Open for Unipolar Inputs Connect to ADC Pin 22 for Bipolar Inputs
24	"High" ("Low") Analog Input, Channel 11 (3)	24	10 V Span R In
25	"High" ("Low") Analog Input, Channel 10 (2)	25	20 V Span R In
26	"High" ("Low") Analog Input, Channel 9 (1)	26	Analog Ground
27	"High" ("Low") Analog Input, Channel 8 (0)	27	Gain Adjust
28	Input Channel Select, Address Bit AE	28	Positive Analog Power Supply, +15 V
29	Input Channel Select, Address Bit A0	29	Buffer Out (for External Use)
30	Input Channel Select, Address Bit A1	30	Buffer In (for External Use)
31	Input Channel Select, Address Bit A2	31	Negative Analog Power Supply, −15 V
32	Input Channel Select Latch "0": Latched "1": Latch "Transparent"	32	Serial Data Out Each Bit Valid on Trailing (↓) Edge Clock Out, ADC Pin 19

SPECIFICATIONS (typical @ +25°C, ±15 V and +5 V unless otherwise noted)

Parameter	AD364RJ	AD364RK	AD364RS	AD364RT	Units
ANALOG INPUTS					
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)				
Input Voltage Range					
T_{min} to T_{max}	±10	*	*	*	V
Input (Bias) Current per Channel	±50	*	*	*	nA
Input Impedance ON Channel	10^{10}‖100	*	*	*	Ω‖pF
OFF Channel	10^{10}‖10	*	*	*	Ω‖pF
Input Fault Current	20	*	*	*	mA max
(Power ON or OFF)					(Internally
Common-Mode Rejection					Limited)
Differential Mode 1 kHz 20 V p–p	70 min (80 typ)	*	*	*	dB
Mux Crosstalk (Any OFF CHANNEL to Any ON Channel) 1 kHz					
20 V p–p	−80 max (−90 typ)	*	*	*	dB
Offset, Channel to Channel	±5	*	*	*	mV max
ACCURACY					
Gain Error[1]	0.3	*	*	*	% of FSR
Unipolar Offset Error[2]	±10	±8	*	**	mV
Bipolar Offset Error	±50	±20	*	**	mV
Linearity Error	0.024	0.012	*	**	% of FSR max
T_{min} to T_{max}	0.024	0.012	*	*	% of FSR max
Differential Linearity Error	0.024	0.012	*	**	% of FSR max
T_{min} to T_{max}	0.024	0.012	*	*	% of FSR max
Noise Error	1 mV p–p 0.1 Hz to 1 MHz	*	*	*	
TEMPERATURE COEFFICIENTS					
Gain	54	31	*	**	ppm/°C
Offset (±10 V Range)	12	7	*	**	ppm/°C
Operating Temperature Range	0°C to +70°C	*	−55°C to +125°C	***	ppm/°C
SIGNAL DYNAMICS					
Conversion Time	32 max (25 typ)	*	*	*	µs
Throughput Rate, Full Accuracy	20 min (25 typ)	*	*	*	kHz
Sample-Hold					
Aperture Delay	200 max (150 typ)	*	*	*	ns
Aperture Uncertainty	500 max (100 typ)	*	*	*	ps
Acquisition Time					
To 0.01% of Final Value					
For Full-Scale Step	18 max (10 typ)	*	*	*	µs
Feedthrough at 1 kHz	−70 max (−80 typ)	*	*	*	dB
Droop Rate	2 max (1 typ)	*	*	*	mV/ms
DIGITAL INPUT SIGNALS					
Analog Input Section					
Input Channel Select	4 Bit Binary Address	*	*	*	
	1 LS TTL Load	*	*	*	
Channel Select Latch	"1" Latch Transparent	*	*	*	
	"0" Latched	*	*	*	
	4 LS TTL Loads	*	*	*	
Single-Ended/Differential	"0" Single Ended	*	*	*	
Mode Select	"1" Differential (+4 V min)	*	*	*	
	3 TTL Loads	*	*	*	
Sample-and-Hold Command	"0" Sample Mode	*	*	*	
	"1" Hold Mode	*	*	*	
	1 TTL Load	*	*	*	
ADC Section[3] $4.5 \leq V_L \leq 5.5$					
Logic Input Threshold					
T_{min} to T_{max}					
Logic "1"	2.0	*	*	*	V min
Logic "0"	0.8	*	*	*	V max
Logic Input Current					
T_{min} to T_{max}					
Logic "1"	20	*	*	*	µA max
Logic "0"	20	*	*	*	µA max

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Parameter	AD364RJ	AD364RK	AD364RS	AD364RT	Units
DIGITAL OUTPUT SIGNALS					
Logic Outputs T_{min} to T_{max}					
Sink Current V_{OUT} = 0.4 V	1.6	*	*	*	mA min
Source Current V_{OUT} = 2.4 V	0.5	*	*	*	mA min
Output Leakage When in					
Three State	±40	*	*	*	µA max
Output Coding					
Unipolar	Positive True Binary	*	*	*	
Bipolar	Positive True Offset				
	Binary	*	*	*	
POWER REQUIREMENTS					
Supply Voltages/Currents	+15 V, ±5% @ 36 mA max	*	*	*	
	−15 V, ±5% @ 65 mA max	*	*	*	
	+5 V, ±5% @ 75 mA max	*	*	*	
PACKAGE OPTIONS					
Analog Input Section (DH-32E)	AD364RJD	AD364RKD	AD364RSD	AD364RTD	
ADC Section (D-28)	AD364RJD	AD364RKD	AD364RSD	AD364RTD	

NOTES
[1]With 50 Ω resistor from REF IN to REF OUT. Adjustable to zero.
[2]Adjustable to zero.
[3]12/8 line must be hard wired to V_{LOGIC} or digital common.

*Specifications same as AD364RJ.
**Specifications same as AD364RK
***Specifications same as AD364RS.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (ALL MODELS)

+V, Digital Supply . . . . . +5.5 V
+V, Analog Supply . . . . . +16 V
−V, Analog Supply . . . . . −16 V
V_{IN}, Signal . . . . . ±V, Analog Supply
V_{IN}, Digital . . . . . 0 to +V, Digital Supply
AGND to DGND . . . . . ±1 V

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD363RKD	0°C to +70°C	DH-32E (Analog Input Section) DH-32C (ADC Section)
AD363RSD	−55°C to +125°C	DH-32E (Analog Input Section) DH-32C (ADC Section)
AD364RJD	0°C to +70°C	DH-32E (Analog Input Section) D-28 (ADC Section)
AD364RKD	0°C to +70°C	DH-32E (Analog Input Section) D-28 (ADC Section)
AD364RSD	−55°C to +125°C	DH-32E (Analog Input Section) D-28 (ADC Section)
AD364RTD	−55°C to +125°C	DH-32E (Analog Input Section) D-28 (ADC Section)

*D = Hermetic DIP. For outline information see Package Information section.

AD364 PIN FUNCTION DESCRIPTION

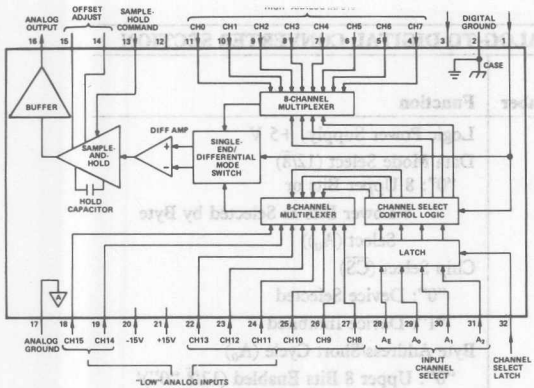
ANALOG INPUT SECTION

Pin Number	Function
1	Single-End/Differential Mode Select "0" Single-Ended Mode "1" Differential Mode
2	Digital Common
3	Positive Digital Power Supply, +5 V
4	"High" Analog Input, Channel 7
5	"High" Analog Input, Channel 6
6	"High" Analog Input, Channel 5
7	"High" Analog Input, Channel 4
8	"High" Analog Input, Channel 3
9	"High" Analog Input, Channel 2
10	"High" Analog Input, Channel 1
11	"High" Analog Input, Channel 0
12	No Connect
13	Sample-Hold Command "0": Sample Mode "1": Hold Mode Normally Connected to ADC Pin 28
14	Offset Adjust
15	Offset Adjust
16	Analog Output Normally Connected to ADC "Analog In"
17	Analog Common
18	"High" ("Low") Analog Input, Channel 15 (7)
19	"High" ("Low") Analog Input, Channel 14 (6)
20	Negative Analog Power Supply, −15 V
21	Positive Analog Power Supply, +15 V
22	"High" ("Low") Analog Input, Channel 13 (5)
23	"High" ("Low") Analog Input, Channel 12 (4)
24	"High" ("Low") Analog Input, Channel 11 (3)
25	"High" ("Low") Analog Input, Channel 10 (2)
26	"High" ("Low") Analog Input, Channel 9 (1)
27	"High" ("Low") Analog Input, Channel 8 (0)
28	Input Channel Select, Address Bit AE
29	Input Channel Select, Address Bit A0
30	Input Channel Select, Address Bit A1
31	Input Channel Select, Address Bit A2
32	Input Channel Select Latch "0": Latched "1": Latch "Transparent"

ANALOG-TO-DIGITAL CONVERTER SECTION

Pin Number	Function
1	Logic Power Supply, +5 V
2	Data Mode Select (12/$\overline{8}$) "0": 8 Upper Bits or 4 Lower Bits as Selected by Byte Select (A_0))
3	Chip Select ($\overline{CS}$) "0": Device Selected "1": Device Inhibited
4	Byte Address/Short Cycle (A_0) "0": Upper 8 Bits Enabled (12/$\overline{8}$ "0")/ 12-Bit Cycle "1": Lower 4 Bits Enabled (12/$\overline{8}$ "1")/ 8-Bit Cycle
5	Read Convert (R/$\overline{C}$) "0": Convert Start "1": Read Enable
6	Chip Enable (CE) ↓: R/$\overline{C}$ "0," $\overline{CS}$ "0" Initiates Conversion ↓: R/$\overline{C}$ "1," $\overline{CS}$ "0" Initiates Read "0": Device Disabled "1": Device Enabled
7	Analog Power Supply, +15 V (V_{CC})
8	Reference Out, +10 V
9	Analog Common (AC)
10	Reference In
11	Analog Power Supply, −15 V (V_{EE})
12	Bipolar Offset
13	10 V Span Input
14	20 V Span Input
15	Digital Common (DC)
16	Data Bit 0
17	Data Bit 1
18	Data Bit 2
19	Data Bit 3
20	Data Bit 4
21	Data Bit 5
22	Data Bit 6
23	Data Bit 7
24	Data Bit 8
25	Data Bit 9
26	Data Bit 10
27	Data Bit 11
28	Status Out

7



AIS Functional Block Diagram

DESIGN

Concept

Figures 1 and 2 show a general DAS application using the AD363 and AD364, respectively.

By dividing the data acquisition task into two sections, several important advantages are realized. Performance of each design is optimized for its specific function. Production yields are increased thus decreasing costs. Furthermore, the standard configuration packages plug into standard sockets and are easier to handle than larger packages with higher pin counts.

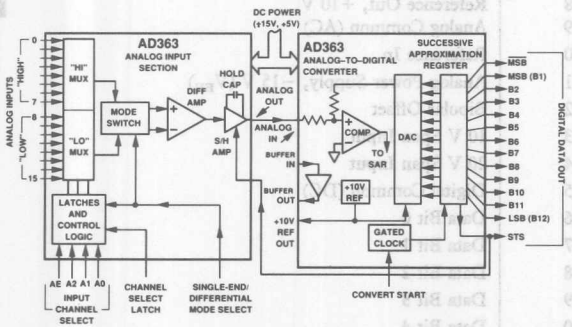


Figure 1. AD363 DAS

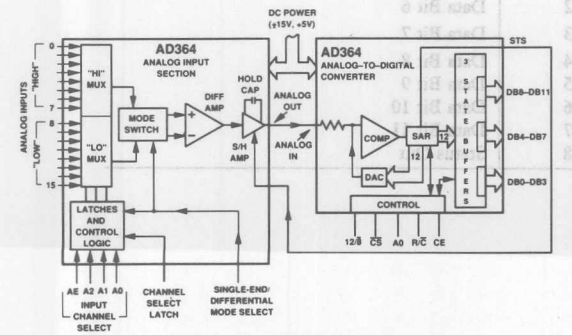


Figure 2. AD364 DAS

Figures 1 and 2 operating at the maximum conversion rate.

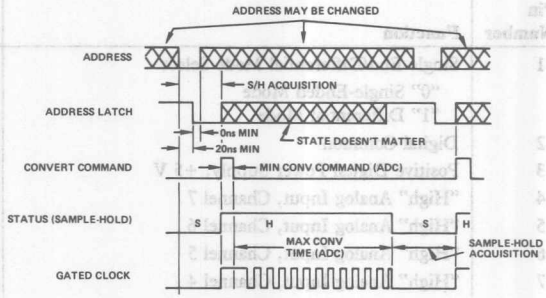


Figure 3. AD363 Timing Diagram

The normal sequence of events is as follows:

1. The appropriate Channel Select Address is latched into the address register. Time is allowed for the multiplexers to settle.
2. A Convert Start command is issued to the ADC which, in response, indicates that it is "busy" by placing a Logic "1" on its Status line.
3. The ADC Status controls the sample-and-hold. When the ADC is "busy," the sample-and-hold is the Hold mode.
4. The ADC goes into its conversion routine. Since the sample-and-hold is holding the proper analog value, the address may be updated during conversion. Thus multiplexer settling time can coincide with conversion and need not affect throughput rate.
5. The ADC indicates completion of its conversion by returning Status to Logic "0." The sample-and-hold returns to the Sample mode.
6. If the input signal has changed full scale (different channels may be widely varying data) the sample-and-hold will typically require 10 microseconds to"acquire" the next input to sufficient accuracy for 12-bit conversion.

After allowing a suitable interval for sample-and-hold to stabilize at its new value, another Convert Start command may be issued to the ADC.

AD363-ADC OPERATION

Figure 4 shows a detailed timing diagram for the AD363-ADC. Serial data changes on rising edges of the internal clock and is guaranteed to be stable on falling edges.

AD364-ADC OPERATION

There are two sets of control pins on the AD364-ADC: the general control inputs (CE, $\overline{CS}$, and R/$\overline{C}$) and the internal register controls inputs (12/$\overline{8}$ and A_O). The general control pins function similarly to those on most A/D converters, performing device timing, addressing, cycle initiation, and read enable functions. The internal register control inputs, which are not found on most A/D converters, select output data format and conversion cycle length.

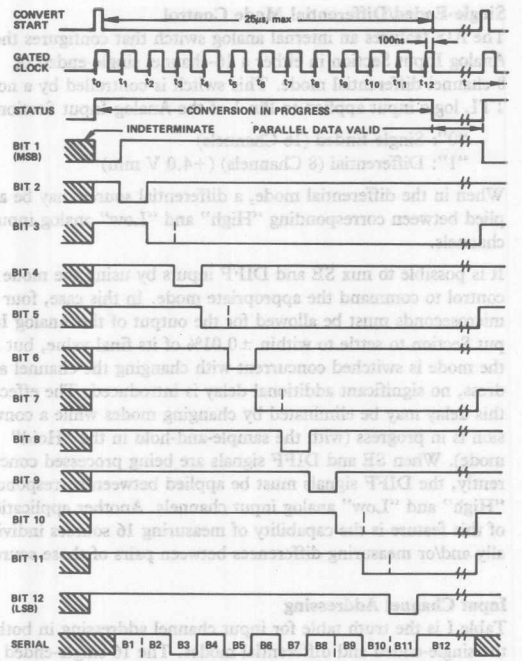


Figure 4. AD363-ADC Timing Diagram (Binary Code 110101011001)

The two major control functions, convert start and read enable, are controlled by CE, $\overline{CS}$, and R/$\overline{C}$. Although all three inputs must be in the correct state to perform the function (for convert start, CE = 1, $\overline{CS}$ = 0, R/$\overline{C}$ = 0; for read enable, CE = 1, $\overline{CS}$ = 0, R/$\overline{C}$ = 1), the sequence does not matter. For large systems, typically microprocessor controlled, standard operation for convert start would be to first set R/$\overline{C}$ = 0 (from R/$\overline{W}$ line); address the chip with $\overline{CS}$ = 0, then apply a positive start pulse to CE. A read would be done similarly but with R/$\overline{C}$ = 1.

A_O (byte select) and 12/$\overline{8}$ (data format) inputs work together to control the output data and conversion cycle. In almost all situations 12/$\overline{8}$ is hard-wired "high" (to V_{LOGIC}) or "low" (to Digital Common). If it is wired high, all 12 data lines will be enabled when the read function is called by the general control inputs. For an 8-bit bus interface, 12/$\overline{8}$ will be wired low. In this mode, only the 8 upper bits or the 4 lower bits can be enabled at once, as addressed by A_O. For these applications, the 4 LSBs (Pins 16–19) should be hard-wired to the 4 MSB (Pins 24–27). Thus, during a read, when A_O is low, the upper 8 bits are enabled and present data on Pins 20 through 27. When A_O goes high, the upper 8 data bits are disabled, the 4 LSBs then present data to Pins 24 to 27, and the 4 middle bits are overridden so that zeros are presented to Pins 20 through 23.

The A_O input performs an additional function of controlling conversion length. If A_O is held low prior to cycle initiation, a full 12-bit, 25 μs cycle will result; if A_O is held high prior to cycle initiation, a shortened 8-bit, 16 μs cycle will result. The A_O line must be set prior to cycle initiation and held in the desired position at least until STS goes high. Thus, for microprocessor interface applications, the A_O line must be properly controlled during both the convert start and read functions.

STANDARD FULL CONTROL INTERFACE

The timing for the standard full control interface is shown in Figure 5. In this operating mode, $\overline{CS}$ is used as the address input which selects the particular device, R/$\overline{C}$ selects between the read data and start conversion functions, and CE is used to time the actual functions.

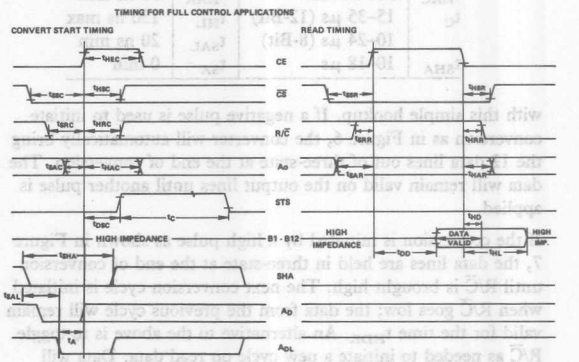


Figure 5. AD364-ADC Timing Diagram

The left side of the figure shows the conversion start control. $\overline{CS}$ and R/$\overline{C}$ are brought low (their sequence does not matter), then the start pulse is applied to CE. The timing diagram shows a time delay for $\overline{CS}$ and R/$\overline{C}$ prior to the start pulse at CE. If less time than this is allowed, the conversion will still be started, but an appropriately longer pulse will be needed at CE. However, if the hold times for $\overline{CS}$ and R/$\overline{C}$ after the rising edge of the start pulse at CE are not followed, the conversion may not be initiated.

The A_O line determines the conversion cycle length and must be selected prior to conversion initiation. If A_O is low, a 12-bit cycle results; if A_O is high, an 8-bit short cycle results. Minimum setup and hold times are shown. The status line goes high to indicate conversion in progress. The analog input signal is allowed to vary until the STS goes high. It must then be held steady until STS again goes low at the end of conversion.

The data read function operates in a similar fashion except that R/$\overline{C}$ is now held high. The data is stored in the output register and can be recalled at will until a new conversion cycle is commanded. In addition, if the converter is arranged in the 8-bit data mode, the A_O line now functions as the byte select address, with setup and hold times as shown. With A_O low, Pins 20 to 27 (DB4–11) come out of three-state and present data. With A_O high, Pins 16–19 (DB0–3) come out of three-state with data and Pins 20–23 present active trailing zeros. In the 8-bit mode, Pins 16–19 will be hard-wired directly to Pin 24–27 for direct two byte loading onto an 8-bit bus. There are two delay times for the data lines after CE is brought low: t_{HD} is the delay until the outputs are fully into the high impedance state.

STANDALONE OPERATION

For simpler control functions, the AD364-ADC can be controlled with just R/$\overline{C}$. In this case, CE is wired high, $\overline{CS}$ low, 12/$\overline{8}$ high, and A_O low. There are two ways of cycling the device

TIMING SPECIFICATIONS—FULL CONTROL MODE

t_{DSC}	400 ns max	t_{DD}	200 ns max
t_{HEC}	300 ns min	t_{HD}	25 ns min
t_{SSC}	300 ns min	t_{SSR}	150 ns min
t_{HSC}	200 ns min	t_{SRR}	0 min
t_{SRC}	250 ns min	t_{SAR}	150 ns min
t_{HRC}	200 ns min	t_{HSR}	50 ns min
t_{SAC}	0 min	t_{HRR}	0 min
t_{HAC}	300 ns min	t_{HAR}	50 ns min
t_C	15–35 μs (12-Bit)	t_{HL}	150 ns max
	10–24 μs (8-Bit)	t_{SAL}	20 ns min
t_{SHA}	10–18 μs	t_{SA}	0 min

with this simple hookup. If a negative pulse is used to initiate conversion as in Figure 6, the converter will automatically bring the 12 data lines out of three-state at the end of conversion. The data will remain valid on the output lines until another pulse is applied.

If the conversion is initiated by a high pulse as shown in Figure 7, the data lines are held in three-state at the end of conversion until R/$\overline{C}$ is brought high. The next conversion cycle is initiated when R/$\overline{C}$ goes low; the data from the previous cycle will remain valid for the time t_{HDR}. An alternative to the above is to toggle R/$\overline{C}$ as needed to initiate a new cycle on read data. Data will appear when R/$\overline{C}$ is brought high, a new cycle is initiated when R/$\overline{C}$ goes low.

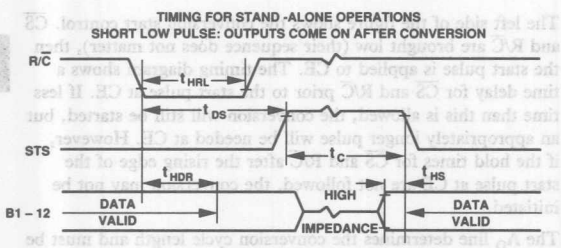


Figure 6.

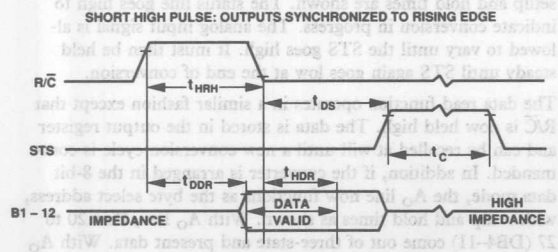


Figure 7.

TIMING SPECIFICATIONS—FULL CONTROL MODE

t_{HRL}	250 ns min	
t_{DS}	600 ns max	
t_{HDR}	25 ns max	
t_{HS}	300 ns min	1000 ns max
t_{HRH}	300 ns min	
t_{DDR}	250 ns max	

APPLICATIONS

Single-Ended/Differential Mode Control

The AIS features an internal analog switch that configures the Analog Input Section in either a 16-channel single-ended or 8-channel differential mode. This switch is controlled by a non-TTL logic input applied to Pin 1 of the Analog Input Section:

"0": Single-Ended (16 Channels)
"1": Differential (8 Channels) (+4.0 V min)

When in the differential mode, a differential source may be applied between corresponding "High" and "Low" analog input channels.

It is possible to mix SE and DIFF inputs by using the mode control to command the appropriate mode. In this case, four microseconds must be allowed for the output of the Analog Input Section to settle to within ±0.01% of its final value, but if the mode is switched concurrent with changing the channel address, no significant additional delay is introduced. The effect of this delay may be eliminated by changing modes while a conversion is in progress (with the sample-and-hold in the "Hold" mode). When SE and DIFF signals are being processed concurrently, the DIFF signals must be applied between corresponding "High" and "Low" analog input channels. Another application of this feature is the capability of measuring 16 sources individually and/or measuring differences between pairs of those sources.

Input Channel Addressing

Table I is the truth table for input channel addressing in both the single-ended and differential modes. The 16-single-ended channels may be addressed by applying the corresponding digital number to the four Input Channel Select address bits, AE, A0, A1, A2 (Pins 28–31). In the differential mode, the eight channels are addressed by applying the appropriate digital code to A0, A1, and A2; AE must be enabled with a Logic "1." Internal logic monitors the status of the SE/DIFF Mode input and addresses the multiplexers singularly or in pairs as required.

ADDRESS				ON CHANNEL (Pin Number)		
					Differential	
AE	A2	A1	A0	Single-Ended	"Hi"	"Lo"
0	0	0	0	0 (11)	None	
0	0	0	1	1 (10)	None	
0	0	1	0	2 (9)	None	
0	0	1	1	3 (8)	None	
0	1	0	0	4 (7)	None	
0	1	0	1	5 (6)	None	
0	1	1	0	6 (5)	None	
0	1	1	1	7 (4)	None	
1	0	0	0	8 (27)	0 (11)	0 (27)
1	0	0	1	9 (26)	1 (10)	1 (26)
1	0	1	0	10 (25)	2 (9)	2 (25)
1	0	1	1	11 (24)	3 (8)	3 (24)
1	1	0	0	12 (23)	4 (7)	5 (23)
1	1	0	1	13 (22)	5 (6)	5 (22)
1	1	1	0	14 (19)	6 (5)	6 (19)
1	1	1	1	15 (18)	7 (4)	7 (18)

Table I. Input Channel Addressing Truth Table

When the channel address is changed, six microseconds must be allowed for the Analog Input Section to settle to within ±0.01% of its final output (including settling times of all elements in the signal path). The effect of this delay may be eliminated by performing the address change while a conversion is in progress (with the sample-and-hold in the "hold" mode). All unused inputs must be grounded.

Input Channel Address Latch

The AIS is equipped with a latch for the Input Channel Select address bits. If the Latch Control pin (Pin 32) is at Logic "1," input channel select address information is passed through to the multiplexers. A Logic "0" "freezes" the input channel address present at the inputs at the "1"-to-"0" transition level-triggered.

This feature is useful when input channel address information is provided from an address, data or control bus that may be required to service many devices. The ability to latch an address is helpful whenever the user has no control of when address information may change.

Sample-and-Hold Mode Control

The Sample-and-Hold Mode Control input (Pin 13) is normally connected to the Status output (Pin 20) from an analog-to-digital converter. When a conversion is initiated by applying a Convert Start command to the ADC, Status goes to Logic "1," putting the sample-and-hold in to the "Hold" mode. This "freezes" the information to be digitized for the period of conversion. When the conversion is complete, Status returns to Logic "0" and the sample-and-hold returns to the "Sample" mode. Eighteen microseconds must be allowed for the sample-and-hold to acquire ("catch up" to) the analog input to within ±0.01% of the final value before a new Convert Start command is issued.

The purpose of a sample-and-hold is to "stop" fast changing input signals long enough to be converted. In this application, it also allows the user to change channels and/or SE/DIFF mode while a conversion is in progress thus eliminating the effects of multiplexer, analog switch and differential amplifier settling times. If maximum throughput rate is required for slowly changing signals, the Sample-and-Hold Mode Control may be wired to ground (Logic "0") rather than to ADC Status thus leaving the sample-and-hold in a continuous sample mode.

Analog Input Section Offset Adjust Circuit

Although the offset voltage of the AIS may be adjusted, that adjustment is normally performed at the ADC. In some special applications, however, it may be helpful to adjust the offset of the Analog Input Section. An example of such a case would be if the input signals were small (<10 mV) relative to the AIS voltage offset and if a gain stage was to be inserted between the AIS and the ADC. To adjust the offset of the AIS, the circuit shown in Figure 8 is recommended.

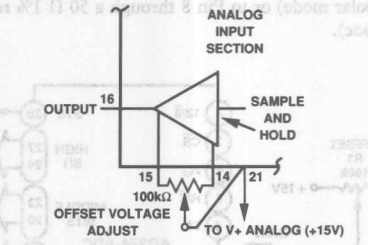


Figure 8. AIS Offset Voltage Adjustment

Under normal conditions, all calibration is performed at the ADC Section.

Gain Adjust, AD363-ADC: Gain may be adjusted by connecting a 100 Ω potentiometer between +10 V Reference Output and Gain Adjust Input (ADC Pins 18 and 27). A multi-turn, low temperature coefficient potentiometer, such as a 20-turn cermet device, is recommended. This potentiometer may be replaced with a 50 Ω, 0.1% resistor to obtain an absolute gain calibration of 0.05% without trimming.

Offset Adjust, AD363-ADC: The simplest offset adjust circuit requires a 20-turn, 20 kΩ cermet potentiometer and a 3.9 MΩ resistor as shown in Figure 9a. This arrangement has an adjustment range of ±8 LSBs, and will contribute a maximum of 2.3 ppm/°C offset drift with a carbon composition fixed resistor (TC = −1200 ppm/°C). Drift contributions from the offset adjust circuit can be reduced well below this level using metal-film resistors and the circuit of Figure 9b.

Gain Adjust, AD364-ADC: Gain may be adjusted by connecting a 100 Ω potentiometer between the Reference Output and Reference Input (ADC Pins 8 and 10). A multi-turn, low temperature coefficient potentiometer, such as a 20T cermet device, is recommended. A fixed 50 Ω, 1% resistor should be connected between Pins 8 and 10 if no gain trim is required.

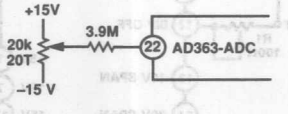


Figure 9a.

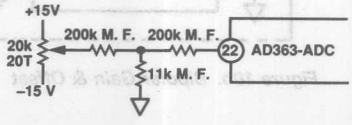


Figure 9b.

Offset Adjust, AD364-ADC: Offset adjust circuits for unipolar and bipolar operation are shown in Figures 10a and 10b. In each case the potentiometer should be a multi-turn, low temperature coefficient device, such as 20-turn cermet. Lowest offset drift in unipolar operation will be realized when the fixed resistors are low-TC (100 ppm/°C) metal-film types.

(bipolar mode).

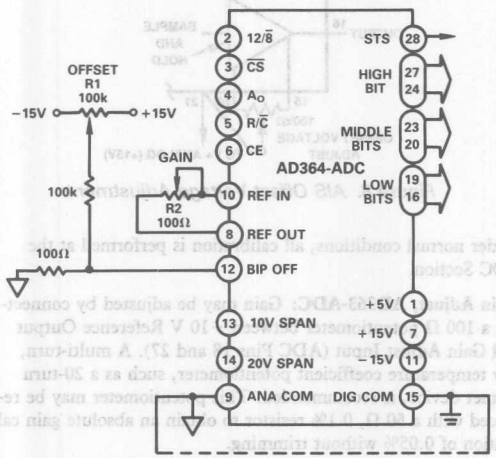


Figure 10a. Unipolar Gain & Offset

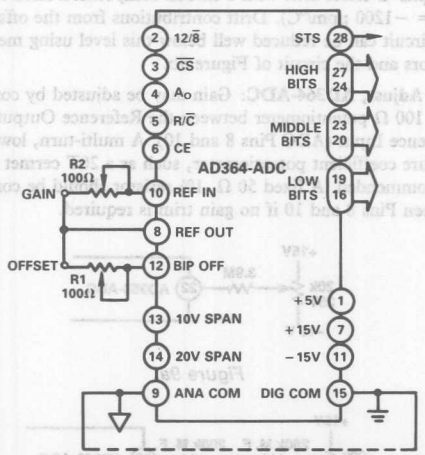


Figure 10b. Bipolar Gain & Offset

Input Scaling: Connections for the various ADC input ranges are given in Tables II and III.

Buffer: An uncommitted unity-gain buffer is available in the AD363-ADC. This buffer has a 2 μs settling time to 0.01% for a 20 V step. Its input should be grounded if the buffer is not used.

Range	Input To Pin:	Span Pin:	Pin 23 To:
0 to +5 V	24	25 to 22	22
0 to +10 V	24	—	
−2.5 V to +2.5 V	24	25 to 22	
−5 V to +5 V	24	—	
−10 V to +10 V	25	—	

Table II. AD364-ADC Pin Connections

Range	Connect Analog Input To Pin:	Connect Pin 12 To:
0 to +10 V	13	GND*
−5 V to +5 V	13	Pin 8**
−10 V to +10 V	14	Pin 8**

*Refer to Figure 10a for gain and offset adjustments.
**Refer to Figure 10b for gain and offset adjustments.

Table III. AD364-ADC Pin Connections

Other Considerations

Grounding: Analog and digital signal grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground (Pin 17) and Digital Ground (Pin 2) are not connected internally; these pins must be connected externally for the system to operate properly. Preferably, this connection is made at only one point, as close to the AIS, as possible. The case is connected internally to Digital Ground to provide good electrostatic shielding. If the grounds are not tied common on the same card with the AIS they should be connected with back-to-back general purpose diodes as shown in Figure 11. This will protect the AIS from possible damage caused by voltages in excess of ±1 volt between the ground systems which could occur if the key grounding card should be removed from the overall system. The device will operate properly with as much as ±200 mV between grounds, however this difference will be reflected directly as an input offset voltage.

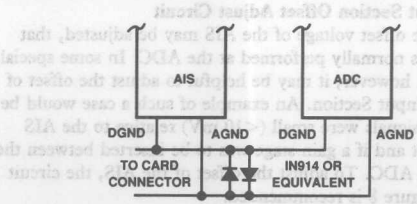


Figure 11. Ground-Fault Protection Diodes

Power Supply Bypassing: The ±15 V and +5 V power leads should be capacitively bypassed to Analog Ground and Digital Ground respectively for optimum device performance. 1 μF tantalum types are recommended; these capacitors should be located close to the system. It is not necessary to shunt these capacitors with disc capacitors to provide additional high frequency power supply decoupling since each power lead is bypassed internally with a 0.039 μF ceramic capacitor.

Complete 12-Bit Sampling A/D Converter for Digital Signal Processing

AD1332

FEATURES

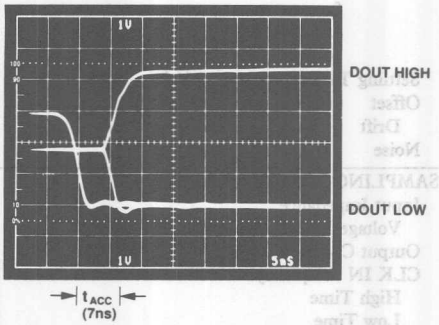
Complete A/D System for DSP Includes:
- 4th Order Antialiasing Filter
- 12-Bit Sampling A/D Converter
- 32-Word FIFO Memory
- Fully Asynchronous, High Speed Digital Interface

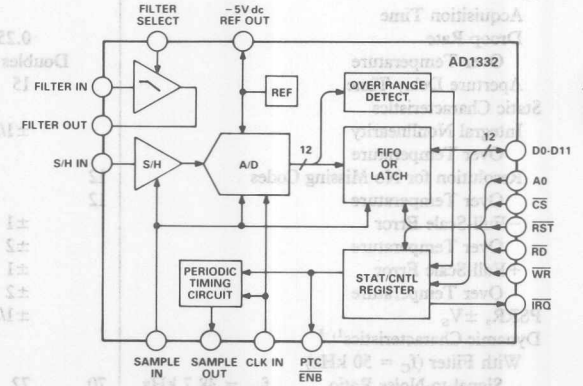
Sample Rate up to 125 kHz
Entire System Is Dynamically Specified
15 ns Data Access Time Allows "No Wait State" Interface to: ADSP-2100 (A), TMS320C25 DSP56000, NECμPD77230

APPLICATIONS

Sonar Signal Processing
Vibration Analysis
Ultrasound Imaging
PC Data Acquisition
High Speed Modems
Motion Control
Speech Processing

DATA ACCESS TIME
(Typical at +25°C)





AD1332 Block Diagram

PRODUCT DESCRIPTION

The AD1332 is a complete, 12-bit A/D converter system optimized for use in high speed digital signal processing (DSP) applications. The device consists of a fourth order antialiasing filter, a 12-bit sampling A/D, a fully asynchronous high speed digital interface and a 32-word FIFO memory. The AD1332 is manufactured using highly reliable advanced hybrid circuit assembly techniques and is packaged in a 40-pin hermetic DIP.

The antialiasing filter is an active four-pole Butterworth. Cutoff frequencies (f_C) are user-selectable (capacitor programmable), and operation is specified for f_C up to 50 kHz. The filter may be bypassed entirely if desired.

The 12-bit sampling A/D converter can convert ±5 V full-scale signals at sample rates up to 125 kHz. The rate is programmable by means of a single external clock. The entire converter system is specified and tested for signal-to-noise ratio and total harmonic distortion.

The digital interface provides a true asynchronous link between the A/D and a high speed microprocessor. Data transfer is controlled by generating an interrupt signal when data is available. Interrupts can be generated when the FIFO is full (32 words), half-full (16 words), or when a single word of data is ready (FIFO bypassed). In addition, the AD1332 can generate an interrupt signal when the A/D conversion results are overrange.

The AD1332 provides a completely specified and tested system that bridges the interface and specification gap between A/D converters and high speed DSP.

This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

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AD1332—SPECIFICATIONS (T_A = +25°C, V_S = ±15 V, V_{DD} = +5 V, unless otherwise noted)

	AD1332BD			AD1332TD			
	Min	Typ	Max	Min	Typ	Max	Units
FILTER (C1–C4 = 500 pF ±1%)							
Input Impedance	8	10		8	10		kΩ
Voltage Range	±10			±10			V
Output Voltage Range $R_L \geq 4$ k	±10			±10			V
Corner Frequency, Accuracy		±2			±2		%
Drift		±0.01			±0.01		%/°C
Gain[1] @ dc	−0.05		+0.05	−0.05		+0.05	dB
0.8 f_C	−1		+1	−1		+1	dB
f_C		−3			−3		dB
4 f_C		−48	−45		−48	−45	dB
10 f_C		−76			−76		dB
Settling Time to 0.01%, 10 V Step		100	125		100	125	µs
Offset		±2	±5		±2	±5	mV
Drift		±20	±100		±20	±100	µV/°C
Noise		75			75		µV rms
SAMPLING A/D CONVERTER[2]							
Input Impedance	4	5		4	5		kΩ
Voltage Range		−5 to +5			−5 to +5		V
Output Coding		Offset Binary			Offset Binary		
CLK IN Frequency	0.5		2.5	0.5		2.5	MHz
High Time	200			200			ns
Low Time	200			200			ns
Sampling Rate (f_S)			125			125	kHz
S/H							
Acquisition Time			2.8			2.8	µs
Droop Rate		0.25	0.5		0.25	0.5	mV/ms
Over Temperature		Doubles Every 10°C			Doubles Every 10°C		
Aperture Delay Time		15			15		ns
Static Characteristics							
Integral Nonlinearity		±1/2	±1		±1/2	±1	LSB
Over Temperature			±1			±1	LSB
Resolution for No Missing Codes	12			12			Bits
Over Temperature	12			12			Bits
−Full-Scale Error		±1	±2		±1	±2	LSB
Over Temperature		±2	±8		±2	±13	LSB
+Full-Scale Error		±1	±2		±1	±2	LSB
Over Temperature		±2	±8		±2	±13	LSB
PSRR, $\pm V_S$		±1/2			±1/2		LSB/V
Dynamic Characteristics[1, 3]							
With Filter (f_C = 50 kHz)							
Signal-to-Noise Ratio, f_{IN} = 38.7 kHz	70	72		70	72		dB
Total Harmonic Distortion, f_{IN} = 38.7 kHz		−82	−72		−82	−72	dB
Intermodulation Distortion, f_{IN1} = 32.8 kHz & f_{IN2} = 34.3 kHz		−82	−72		−82	−72	dB
Without Filter							
Signal-to-Noise Ratio, f_{IN} = 60.9 kHz	70	72		70	72		dB
Total Harmonic Distortion, f_{IN} = 60.9 kHz		−78	−68		−78	−68	dB
Intermodulation Distortion, f_{IN1} = 58.7 kHz & f_{IN2} = 60.9 kHz		−78	−68		−78	−68	dB
Reference Voltage	−5.05		−4.95	−5.05		−4.95	V
Output Current	±1	±2		±1	±2		mA
Drift		±10	±30		±10	±30	ppm/°C

	AD1332BD			AD1332TD			
	Min	Typ	Max	Min	Typ	Max	Units
DIGITAL INPUTS[1]							
$\overline{RD}$, $\overline{WR}$, $\overline{CS}$, $\overline{RST}$, A0, D0–D11, PTC $\overline{ENB}$							
Input Voltage, Logic Low			+0.8			+0.8	V
Input Voltage, Logic High	+2.0			+2.25			V
Input Current			±200			±200	µA
SAMPLE IN, CLK IN							
Input Voltage, Logic Low			+1.5			+1.5	V
Input Voltage, Logic High	+3.5			+3.5			V
Input Current			±10			±10	µA
Input Capacitance		5			5		pF
$\overline{RST}$ LOW Pulse Width	10			10			ns
DIGITAL OUTPUTS[1]							
D0–D11, SAMPLE OUT							
Output Voltage, Logic Low[5]			+0.4			+0.4	V
Output Voltage, Logic High							
D0–D11[5]	+2.4			+2.4			V
SAMPLE OUT, I_{OH} = −0.4 mA	+4.0			+4.0			V
High Impedance Leakage Current			±200			±200	µA
$\overline{IRQ}$, PTC $\overline{ENB}$							
Output Voltage, Logic Low[5]			+0.4			+0.4	V
Off-State Leakage			±10			±10	µA
Output Capacitance		5			5		pF
$\overline{IRQ}$ LOW to D0–D11 Valid[4]			0			0	ns
POWER REQUIREMENTS							
Operating Range							
$\pm V_S$	±11.4		±15.75	±11.4		±15.75	V
V_{DD}	+4.75		+5.25	+4.75		+5.25	V
$+V_S$ Supply Current		50	57		50	57	mA
$-V_S$ Supply Current		48	57		48	57	mA
$+V_{DD}$ Supply Current		6	15		6	15	mA
Consumption							
$\pm V_S$ = ±12 V		1.2	1.4		1.2	1.4	W
$\pm V_S$ = ±15 V		1.5	1.75		1.5	1.75	W
TEMPERATURE RANGE							
Operating and Specified	−40		+85	−55		+125	°C
Storage	−65		+150	−65		+150	°C

NOTES
[1]Guaranteed over operating temperature range, tested at +25°C only.
[2]f_{CLK} = 2.5 MHz, SAMPLE IN connected to SAMPLE OUT, PTC $\overline{ENB}$ = Low.
[3]THD of harmonics 2-7 of the fundamental. SNR of fundamental less harmonics 2-7.
[4]$\overline{RD}$, $\overline{CS}$, A0 = "Low;" $\overline{WR}$, $\overline{RST}$ = "High."
[5]I_{OL} = 4 mA, I_{OH} = −4 mA for AD1332BD. I_{OL} = 3.2 mA, I_{OH} = −3.2 mA for AD1332TD.
Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD1332BD	−40°C to +85°C	DH-40A
AD1332TD/883B	−55°C to +125°C	DH-40A

*D = Hermetic Ceramic DIP. For outline information see Package Information section.

SWITCHING CHARACTERISTICS

(over operating temperature and power supply voltage range, with C_{OUT} = 30 pF or 100 pF except where noted)

Parameter	Description	Conditions	Min	Max	Units
READ CYCLE					
t_{RC}	Read Cycle Time	C_{OUT} = 30 pF	25		ns
		C_{OUT} = 100 pF	35		ns
t_A	Data Access Time	C_{OUT} = 30 pF		15	ns
		C_{OUT} = 100 pF		25	ns
		C_{OUT} = 150 pF		35	ns
t_{LZ}	Output Low Z Time		2		ns
t_{HZ}	Output High Z Time	C_{OUT} = 30 pF		15	ns
		C_{OUT} = 100 pF		25	ns
t_{OH}	Output Hold Time		2		ns
t_{A0RD}	A0 Valid to $\overline{RD}$ LOW		3		ns
t_{RDA0}	$\overline{RD}$ HIGH to A0 Invalid		3		ns
t_{A0CS}	A0 Valid to $\overline{CS}$ LOW		3		ns
t_{CSA0}	$\overline{CS}$ HIGH to A0 Invalid		3		ns
WRITE CYCLE					
t_{WC}	Write Cycle Time		15		ns
t_{WP}	Write Pulse Width		5		ns
t_{SU}	Data Setup Time		2		ns
t_{IH}	Input Hold Time		4		ns
t_{A0WR}	A0 Valid to $\overline{WR}$ LOW		3		ns
t_{WRA0}	$\overline{WR}$ HIGH to A0 Invalid		3		ns
t_{A0CS}	A0 Valid to $\overline{CS}$ LOW		3		ns
t_{CSA0}	$\overline{CS}$ HIGH to A0 Invalid		3		ns

NOTE
Specifications subject to change without notice.
Specifications are guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to APWR/ASIG GND . . . . . +18 V
$-V_S$ to APWR/ASIG GND . . . . . −18 V
V_{DD} to DGND . . . . . +7 V
APWR/ASIG GND to DGND . . . . . −0.3 V to +0.3 V
Analog Input to APWR/ASIG GND
S/H IN, FILTER IN, C1vg-C4vg . . . . . $-V_S$ to $+V_S$
Digital Input to APWR GND
SAMPLE IN, CLK IN . . . . . −0.3 V to +7 V
Digital Input to DGND
D0–D11, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A0, $\overline{RST}$,
PTC $\overline{ENB}$ . . . . . −0.3 V to V_{DD} +0.3 V
Output Short Circuit Duration
FILTER OUT, REF OUT or C1wv-C4wv . . . . . Indefinite
Digital Output . . . . . 1 Output for 1 sec
Lead Temperature Range,
Soldering for 10 sec . . . . . +300°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



Four-Channel 12-Bit Sampling A/D Converter for Digital Signal Processing

AD1334

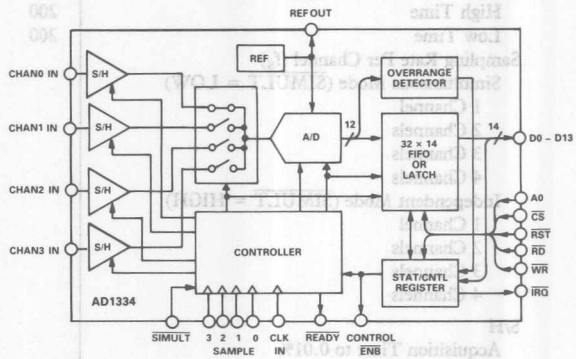
FEATURES

- Four-Channel A/D Converter for DSP Includes:
  - Simultaneous or Independent Sampling Capability
  - 12-Bit Accurate A/D Converter
  - 2-Bit Channel ID Tags Each Conversion Result
  - 32-Word FIFO Memory
  - Fully Asynchronous, High Speed Digital Interface
- Single-Channel Sample Rate Up to 67 kHz
- Four-Channel Simultaneous Sample Rate Up to 28 kHz
- Entire System Dynamically Characterized
- Minimal Effective Aperture Delay Mismatch from Channel-to-Channel & Device-to-Device
- 15 ns Data Access Time Allows "No Wait State" Interface to: ADSP-2100 (A), TMS320C25 DSP56000, NECμPD77230
- Low Power, 250 mW/Channel

APPLICATIONS

- Sonar Signal Processing
- Robotics/Machine Control
- Disk-Drive Head Positioning
- Vibration Analysis

BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1334 is a four-channel, 12-bit, sampling A/D converter system optimized for use in multichannel digital signal processing (DSP) applications. The device consists of four independent sample-and-hold amplifiers, a multiplexer, an A/D converter, a controller, a 32-word FIFO memory and a fully asynchronous high speed digital interface. The product is packaged in a 40-pin hermetic DIP.

The channel controller enables the AD1334 to appear as four independent channels of analog input by generating all of the timing necessary to ensure that the sampled channel is digitized to 12-bit accuracy. Upon receipt of a sample command, the controller will immediately place the sample-and-hold amplifier into hold mode and then prioritize and schedule the held value for A/D conversion. At the appropriate time, the sampled input is gated through the multiplexer and, after settling, is digitized by the A/D converter. The sample-and-hold amplifier is then returned to sample mode so that it can acquire the next sample.

For effective use in simultaneous sampling applications, the sample-and-hold amplifiers are designed to provide a minimum amount of aperture delay time mismatch from channel-to-channel and device-to-device.

The 12-bit A/D converter can convert ±5 V full scale signals at sample rates up to 67 kHz for single-channel operation. In the simultaneous mode, the AD1334 has a four-channel sample rate up to 28 kHz. The entire converter system is specified and tested for signal-to-noise ratio, total harmonic distortion and channel-to-channel isolation.

The digital interface provides a true asynchronous link between the A/D and a high speed microprocessor. Data transfer is controlled by generating an interrupt signal when data is available. Interrupts can be generated when the FIFO is full (32 words), half-full (16 words), or when a single word of data is ready (FIFO bypassed). The AD1334 can also generate an interrupt when the A/D conversion results are overrange.

The AD1334 provides a completely specified and tested system that bridges the interface and specification gap between A/D converters and high speed DSP.

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This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

	AD1334BD			AD1334TD			
	Min	Typ	Max	Min	Typ	Max	Units
S/H, MUX & A/D CONVERTER[1]							
Input Impedance	2	2.5		2	2.5		kΩ
Voltage Range		−5 to +5			−5 to +5		V
Output Coding		Offset Binary			Offset Binary		
CLK IN Frequency, (f_{CLK})	1.0		2.5	1.0		2.5	MHz
High Time	200			200			ns
Low Time	200			200			ns
Sampling Rate Per Channel (f_S)							
Simultaneous Mode ($\overline{SIMULT}$ = LOW)							
1 Channel			67			67	kHz
2 Channels			46			46	kHz
3 Channels			35			35	kHz
4 Channels			28			28	kHz
Independent Mode ($\overline{SIMULT}$ = HIGH)							
1 Channel			67			67	kHz
2 Channels			67			67	kHz
3 Channels			44			44	kHz
4 Channels			33			33	kHz
S/H							
Acquisition Time to 0.01%		6.5	7.5		6.5	7.5	µs
Droop Rate		0.2	1.0		0.2	1.0	mV/ms
Over Temperature		Doubles Every 10°C			Doubles Every 10°C		
−3 dB Small Signal Bandwidth		200			200		kHz
Group Delay[2] (f_{IN}<10 kHz)		785			785		ns
Aperture Delay[3]	0	10	15	0	10	15	ns
Effective Aperture Delay[4] (f_{IN}<10 kHz)	−700	−775	−850	−700	−775	−850	ns
Static Characteristics							
Integral Linearity Error		±1/2	+1		±1/2	+1	LSB
Over Temperature			±1			±1 1/2	LSB
Differential Linearity Error			±1			±1	LSB
Over Temperature			±1			±2	LSB
−Full-Scale Error		±2	±4		±2	±4	LSB
Over Temperature		±4	±8		±4	±13	LSB
+Full-Scale Error		±2	±4		±2	±4	LSB
Over Temperature		±4	±8		±4	±13	LSB
PSRR, $\pm V_S$		±1/2			±1/2		LSB/V
Dynamic Characteristics[5, 6]							
Signal-to-Noise Ratio, f_{IN} = 13.6 kHz	70	72		70	72		dB
Total Harmonic Distortion, f_{IN} = 13.6 kHz		−86	−76		−86	−76	dB
Intermodulation Distortion, f_{IN1} = 13.1 kHz & f_{IN2} = 13.6 kHz		−86	−76		−86	−76	dB
Channel-to-Channel Isolation[7], f_{IN} = 8.009 kHz							
$\overline{SIMULT}$ = LOW	70	78		70	78		dB
$\overline{SIMULT}$ = HIGH		74			74		dB
Reference Voltage	−5.05		−4.95	−5.05		−4.95	V
Output Current	±1	±2		±1	±2		mA
Drift		±10	±30		±10	±30	ppm/°C

	AD1334BD			AD1334TD			
	Min	Typ	Max	Min	Typ	Max	Units
DIGITAL INPUTS[6]							
Voltage Input, LOW			+0.8			+0.8	V
HIGH	+2.0			+2.25			V
Input Current			±250			±250	μA
Input Capacitance		5			5		pF
$\overline{RST}$ LOW Pulse Width	10			10			ns
DIGITAL OUTPUTS[6]							
D0–D13, $\overline{READY}$							
Output Voltage, Logic LOW[8]			+0.4			+0.4	V
Output Voltage, Logic HIGH[8]	+2.4			+2.4			V
3-State Leakage Current			±250			±250	μA
$\overline{IRQ}$, CONTROL $\overline{ENB}$							
Output Voltage, Logic LOW[8]			+0.4			+0.4	V
$\overline{IRQ}$ Off-State Leakage			±10			±10	μA
Output Capacitance		5			5		pF
FIFO Fall-Thru Time		400	800		400	800	ns
$\overline{IRQ}$ LOW to D0–D13 Valid[9]			0			0	ns
POWER REQUIREMENTS							
Operating Range							
$\pm V_S$	±11.4		±15.75	±11.4		±15.75	V
V_{DD}	+4.75		+5.25	+4.75		+5.25	V
Supply Current							
$+V_S$		47	60		47	60	mA
$-V_S$		39	50		39	50	mA
$+V_{DD}$		7	15		7	15	mA
Consumption							
$\pm V_S = \pm 12$ V		1.0	1.2		1.0	1.2	W
$\pm V_S = \pm 15$ V		1.25	1.5		1.25	1.5	W
TEMPERATURE RANGE							
Operating and Specified	−40		+85	−55		+125	°C
Storage	−65		+150	−65		+150	°C

NOTES

[1]Specifications are per channel in 4 Channel Simultaneous Mode (SAMPLE 0–3 connected together and $\overline{SIMULT}$ & CONTROL $\overline{ENB}$ = LOW), at f_S = 28 kHz, and with SAMPLE 0–3 having an 80% duty cycle unless noted.

[2]Group delay is the negative of the 1st derivative of phase with respect to frequency and is a measure of the analog time delay through the S/H.

[3]Aperture delay is the time delay from the SAMPLE input to S/H switch opening and is a measure of the digital time delay through the S/H.

[4]Effective aperture delay is the difference between analog and digital time delays described in (2) and (3).

[5]THD of harmonics 2–7 of the fundamental. SNR of fundamental less harmonics 2–7.

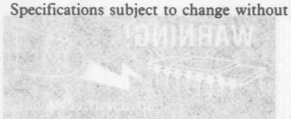
[6]Guaranteed over operating temperature and power supply voltage range.

[7]Isolation of any one channel from remaining three channels which have near maximum amplitude ac signals at their inputs.

[8]I_{OL} = 4 mA for AD1334BD, I_{OL} = 3.2 mA for AD1334TD; I_{OH} = −4 mA for AD1334BD, I_{OH} = −3.2 mA for AD1334TD.

[9]$\overline{RD}$, $\overline{CS}$, A0 = LOW; $\overline{WR}$, $\overline{RST}$ = HIGH.

Specifications subject to change without notice.



ORDERING GUIDE

Model	Temperature Range	Package Option*
AD1334BD	−40°C to +85°C	DH-40A
AD1334TD/883B	−55°C to +125°C	DH-40A

*D = Hermetic Ceramic DIP. For outline information see Package Information section.

SWITCHING CHARACTERISTICS (over operating temperature and power supply voltage range, with C_{OUT} = 30 pF or 100 pF except where noted)

Parameter	Description	Conditions	Min	Max	Units
READ CYCLE					
t_{RC}	Read Cycle Time	C_{OUT} = 30 pF	25		ns
		C_{OUT} = 100 pF	35		ns
t_A	Data Access Time	C_{OUT} = 30 pF		15	ns
		C_{OUT} = 100 pF		25	ns
t_{LZ}	Output Low Z Time		2		ns
t_{HZ}	Output High Z Time	C_{OUT} = 30 pF		15	ns
		C_{OUT} = 100 pF		25	ns
t_{OH}	Output Hold Time		2		ns
t_{A0RD}	A0 Valid to $\overline{RD}$ LOW		3		ns
t_{RDA0}	$\overline{RD}$ HIGH to A0 Invalid		3		ns
t_{A0CS}	A0 Valid to $\overline{CS}$ LOW		3		ns
t_{CSA0}	$\overline{CS}$ HIGH to A0 Invalid		3		ns
WRITE CYCLE					
t_{WC}	Write Cycle Time		15		ns
t_{WP}	Write Pulse Width		5		ns
t_{SU}	Data Setup Time		2		ns
t_{IH}	Input Hold Time		4		ns
t_{A0WR}	A0 Valid to $\overline{WR}$ LOW		3		ns
t_{WRA0}	$\overline{WR}$ HIGH to A0 Invalid		3		ns
t_{A0CS}	A0 Valid to $\overline{CS}$ LOW		3		ns
t_{CSA0}	$\overline{CS}$ HIGH to A0 Invalid		3		ns

Specifications subject to change without notice.
All specifications are guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to APWR/ASIG GND . . . . . +18 V
$-V_S$ to APWR/ASIG GND . . . . . −18 V
V_{DD} to DGND . . . . . +7 V
APWR/ASIG GND to DGND . . . . . −0.3 V to +0.3 V
Analog Input to APWR/ASIG GND . . . . . $-V_S$ to $+V_S$
Digital Input to APWR GND
SAMPLE0–SAMPLE3, CLK IN,
$\overline{SIMULT}$, CONTROL $\overline{ENB}$ . . . . . −0.3 V to +7 V
Digital Input to DGND
D0–D13, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A0, $\overline{RST}$ . . −0.3 V to V_{DD}+0.3 V
Output Short Circuit Duration
REF OUT, TP . . . . . Indefinite
Digital Output . . . . . 1 Output for 1 sec
Lead Temperature Range,
Soldering for 10 sec . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



16-Channel Data Acquisition System

AD1341

FEATURES

150,000 Channels/Second Throughput Rate
Analog Inputs
- **16 Single-Ended (SE) or 8 Differential (DE); Expandable to 32 SE or 16 DE**
- **Over Voltage Protected**
- **Power Supply Loss Protected**

Programmable Gain Amplifier (PGA)
- **Binary Gains 1 to 128**
- **Independent Gain Selection per Channel**

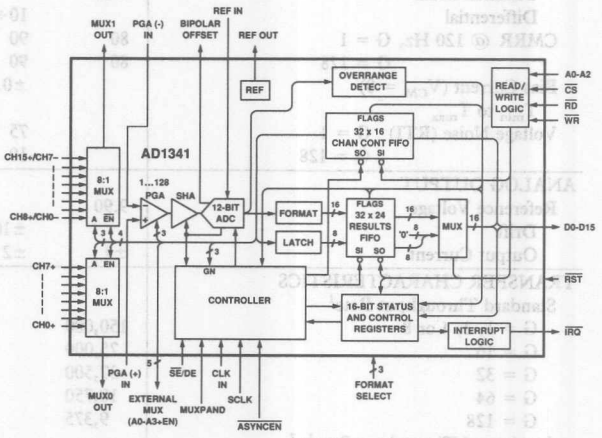
12-Bit Sampling A/D Converter
Processor Interface
- **FIFOs for Channel Control and Conversion Results**
- **Fully Asynchronous 16-Bit Parallel Bus**
- **15 ns Data Access Time**
- **Selectable 16-Bit Data Format**
- **Programmable Interrupt Structure**

Ceramic Surface Mount Package

APPLICATIONS

DSP Data Acquisition
Missile Guidance
Vibration Analysis
Process Control

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1341 is a complete 16-channel data acquisition system optimized for use in multichannel control and digital signal processing applications. The device consists of two 8-channel input multiplexers, a programmable gain amplifier (PGA), a 12-bit sampling A/D converter, two 32-word FIFOs, a controller, and registers for status and control. The device is packaged in a 100-lead ceramic quad flat package.

The input multiplexers can be configured for either 16 channels of single-ended input or 8 channels of differential input. The number of channels can be doubled with the addition of a single external 16-channel multiplexer. The inputs are protected against power loss for applications where the AD1341 is not powered from the same source as its inputs.

The programmable gain amplifier has differential inputs and 8 binary gain ranges from 1 to 128. Each channel can be programmed for a different gain. The controller timing allows the AD1341 to operate at the full 150,000 channels/second at gains from 1 to 8. Above 8, the throughput rate decreases proportionately to the increase in gain.

The 12-bit sampling A/D converter is specified and tested for both static and dynamic performance.

The AD1341 communicates asynchronously with the microprocessor over a 16-bit wide data path. Data can be formatted in either straight binary or twos complement with left, center or right justification. A 32-word FIFO is used to control channel selection and PGA gain. A second 32-word FIFO is used to store A/D conversion results.

PRODUCT HIGHLIGHTS

1. High throughput rate makes the AD1341 ideal for use in a wide range of applications in motion control, speech processing, PC data acquisition, medical instrumentation, and missile guidance.
2. Software development is simplified because timing for channel selection, PGA gain changing and settling, and A/D conversion is internal to the AD1341. Registers are available for enabling interrupt conditions and polling interrupt conditions or real-time status.
3. Software overhead is reduced by having FIFOs store channel information and conversion results.
4. Processor interface is simplified because the AD1341 operates fully asynchronously to the processor, has a maximum 15 ns data access time and is isolated by hybrid circuit construction.

7

ANALOG INPUTS (Per Channel)						
Impedance						
Single Ended		100||50			100||50	MΩ||pF
Differential		100||25			100||25	MΩ||pF
Voltage Range						
Common Mode	±10			±10		V
Differential		10÷G			10÷G	V
CMRR @ 120 Hz, G = 1	80	90		80	90	dB
G = 128	80	90		80	90	dB
Bias Current (V_{CM} = 0)		±0.1	±2		±0.1 ±2	nA
T_{min} to T_{max}			±200		±300	nA
Voltage Noise (RTI) G = 1		75			75	μV rms
G = 128		10			10	μV rms
ANALOG OUTPUT						
Reference Voltage	9.90		10.10	9.90	10.10	V
Drift		±10	±30		±10 ±30	ppm/°C
Output Current	±1	±2		±1	±2	mA
TRANSFER CHARACTERISTICS						
Standard Throughput Rate[1]						
G = 1, 2, 4 or 8	150,000			150,000		Chan/Sec
G = 16	75,000			75,000		Chan/Sec
G = 32	37,500			37,500		Chan/Sec
G = 64	18,750			18,750		Chan/Sec
G = 128	9,375			9,375		Chan/Sec
Accelerated Throughput Rate[1, 2]						
G = 1, 2, 4 or 8	150,000			150,000		Chan/Sec
G = 16	100,000			100,000		Chan/Sec
G = 32	57,690			57,690		Chan/Sec
G = 64	29,410			29,410		Chan/Sec
G = 128	14,850			14,850		Chan/Sec
STATIC CHARACTERISTICS						
PGA Gain Accuracy (Any Gain)		±1/2	±2		±1/2 ±2	%
Integral Nonlinearity		±1/2	±1		±1/2 ±1	LSB
T_{min} to T_{max}			±1		±1	LSB
Resolution for No Missing Codes	12			12		Bits
T_{min} to T_{max}	12			12		Bits
Unipolar Offset Error		±1	±2		±1 ±2	LSB
T_{min} to T_{max}			±4		±6	LSB
Bipolar Zero Error		±1	±2		±1 ±2	LSB
T_{min} to T_{max}			±4		±6	LSB
Gain Error		±1	±2		±1 ±2	LSB
T_{min} to T_{max}			±8		±12	LSB
DYNAMIC CHARACTERISTICS						
SNR						
G = 1, f_S = 150.0 kHz[3]	70	73		70	73	dB
G = 2, f_S = 150.0 kHz		72			72	dB
G = 4, f_S = 150.0 kHz		72			72	dB
G = 8, f_S = 150.0 kHz		71			71	dB
G = 16, f_S = 75.0 kHz[3]	68	71		68	71	dB
G = 32, f_S = 37.5 kHz		70			70	dB
G = 64, f_S = 18.8 kHz		69			69	dB
G = 128, f_S = 9.4 kHz		66			66	dB

Parameter	Min	Typ	Max	Min	Typ	Max	Units
THD							
G = 1, f_S = 150.0 kHz[3]		−90	−80		−90	−80	dB
G = 2, f_S = 150.0 kHz		−90			−90		dB
G = 4, f_S = 150.0 kHz		−88			−88		dB
G = 8, f_S = 150.0 kHz		−88			−88		dB
G = 16, f_S = 75.0 kHz[3]		−88	−78		−88	−78	dB
G = 32, f_S = 37.5 kHz		−88			−88		dB
G = 64, f_S = 18.8 kHz		−85			−85		dB
G = 128, f_S = 9.4 kHz		−84			−84		dB
CHANNEL-TO-CHANNEL ISOLATION		80			80		dB
DIGITAL INPUTS[4]							
Input Voltage							
Logic Low			0.8			0.8	V
Logic High	2.0			2.25			V
Input Current		±60	±200		±60	±200	μA
Input Capacitance		2			2		pF
$\overline{RST}$ Low Pulse Width	10			10			ns
CLK Input							
Frequency			3.0			3.0	MHz
Duty Cycle	45		55	45		55	%
DIGITAL OUTPUTS[4]							
Output Voltage							
Logic Low							
I_{OL} = 4.0 mA		0.2	0.4				V
I_{OL} = 3.2 mA					0.2	0.4	V
Logic High							
I_{OH} = −4.0 mA	2.4	4.5					V
I_{OH} = −3.2 mA				2.4	4.5		V
Output Capacitance		6			6		pF
High Impedance Leakage,							
D0–D15		±60	±200		±60	±200	μA
Off State Leakage, $\overline{IRQ}$		±1	±10		±1	±10	μA
POWER SUPPLY							
Operating Voltage Range							
$+V_S$	+14.25		+15.75	+13.5		+16.5	V
$-V_S$	−15.75		−14.25	−16.5		−13.5	V
V_{DD}	+4.75		+5.25	+4.5		+5.5	V
Quiescent Current							
$+V_S$		41	56		41	56	mA
$-V_S$		35	50		35	50	mA
V_{DD}		5	10		5	10	mA
POWER CONSUMPTION		1.2	1.6		1.2	1.6	W
PSRR, $\pm V_S$		±1/2			±1/2		LSB/V
TEMPERATURE RANGE							
Operating and Specified	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	°C

NOTES

[1]All channel gains are fixed at the specified value.

[2]Accelerated performance is achieved through using a pipeline architecture and constant SHA acquisition times (see page 12 of this data sheet).

[3]f_{IN} = 4.6 kHz for G = 1, 2.3 kHz for G = 16 tests. SNR excludes harmonics 2–9. THD includes harmonics 2–9. Input amplitude is −0.3 dB relative to full-scale at each gain.

[4]Guaranteed over operating temperature range, tested at +25°C only.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to APWR/ASIG GND . . . . . +18 V
$-V_S$ to APWR/ASIG GND . . . . . −18 V
V_{DD} to DGND . . . . . +7 V
APWR/ASIG GND to DGND . . . . . −0.3 V to +0.3 V
Analog Inputs to APWR/ASIG GND
  Multiplexer . . . . . $+V_S$ + 16 V, $-V_S$ − 16 V
  PGA . . . . . $-V_S$ to $+V_S$
  Reference Input . . . . . 0 V to +11 V
Digital Inputs to DGND . . −0.3 V to V_{DD} + 0.3 V or 10 mA
Output Short Circuit Duration
  Reference & Multiplexer Outputs . . . . . Indefinite
  Digital Outputs . . . . . 1 Output for 1 Second
Lead Soldering Temperature (10 seconds) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



SWITCHING CHARACTERISTICS

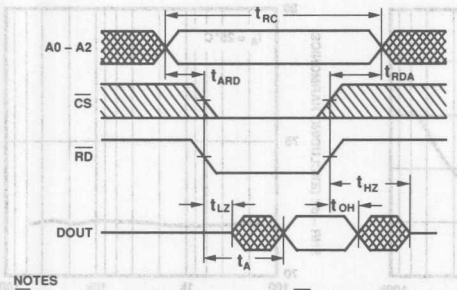
(Over operating temperature and power supply voltage range, with C_{OUT} = 30 pF or 100 pF except where noted)

Parameter	Description	Condition	Min	Typ	Max	Units
READ CYCLE						
t_{RC}	Read Cycle Time	C_{OUT} = 30 pF	25			ns
		C_{OUT} = 100 pF	35			ns
t_A	Data Access Time	C_{OUT} = 30 pF			15	ns
		C_{OUT} = 100 pF			25	ns
		C_{OUT} = 150 pF			35	ns
t_{LZ}	Output LO-Z Time		2			ns
t_{HZ}	Output HI-Z Time	C_{OUT} = 30 pF			15	ns
		C_{OUT} = 100 pF			25	ns
t_{OH}	Output Hold Time		2			ns
t_{ARD}	Address Valid to $\overline{RD}$ Low		3			ns
t_{RDA}	$\overline{RD}$ High to Address Invalid		3			ns
t_{ACS}	Address Valid to $\overline{CS}$ Low		3			ns
t_{CSA}	$\overline{CS}$ High to Address Invalid		3			ns
WRITE CYCLE						
t_{WC}	Write Cycle Time		15			ns
t_{WP}	Write Pulse Width		5			ns
t_{SU}	Input Setup Time		2			ns
t_{IH}	Input Hold Time		3			ns
t_{AWR}	Address Valid to $\overline{WR}$ Low		3			ns
t_{WRA}	$\overline{WR}$ High to Address Invalid		3			ns
t_{ACS}	Address Valid to $\overline{CS}$ Low		3			ns
t_{CSA}	$\overline{CS}$ High to Address Invalid		3			ns

ORDERING GUIDE

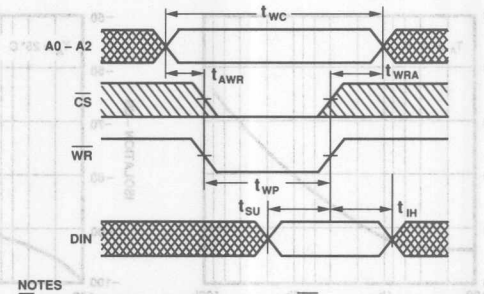
Model	Temperature Range	Package Option*
AD1341KZ	0°C to +70°C	Z-100
AD1341TZ/883B	−55°C to +125°C	Z-100

*Z = Ceramic Leaded Chip Carrier Package. For outline information see Package Information section.



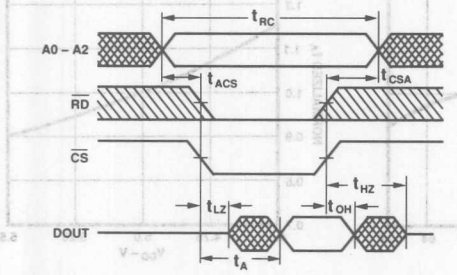
NOTES
$\overline{CS}$ IS VALID BEFORE OR COINCIDENT WITH $\overline{RD}$ HIGH - TO - LOW TRANSITION.
$\overline{CS}$ IS INVALID AFTER OR COINCIDENT WITH $\overline{RD}$ LOW - TO - HIGH TRANSITION.
$\overline{WR}$ IS NOT ACTIVE DURING READ CYCLE.

Figure 1a. Timing Waveform for Read Cycle No. 1 ($\overline{RD}$ Controlled)



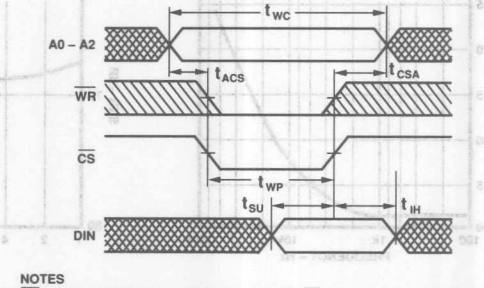
NOTES
$\overline{CS}$ IS VALID BEFORE OR COINCIDENT WITH $\overline{WR}$ HIGH - TO - LOW TRANSITION.
$\overline{CS}$ IS INVALID AFTER OR COINCIDENT WITH $\overline{WR}$ LOW - TO - HIGH TRANSITION.
$\overline{RD}$ IS NOT ACTIVE DURING WRITE CYCLE.

Figure 2a. Timing Waveform for Write Cycle No. 1 ($\overline{WR}$ Controlled)



NOTES
$\overline{RD}$ IS VALID BEFORE OR COINCIDENT WITH $\overline{CS}$ HIGH - TO - LOW TRANSITION.
$\overline{RD}$ IS INVALID AFTER OR COINCIDENT WITH $\overline{CS}$ LOW - TO - HIGH TRANSITION.
$\overline{WR}$ IS NOT ACTIVE DURING READ CYCLE.

Figure 1b. Timing Waveform for Read Cycle No. 2 ($\overline{CS}$ Controlled)



NOTES
$\overline{WR}$ IS VALID BEFORE OR COINCIDENT WITH $\overline{CS}$ HIGH - TO - LOW TRANSITION.
$\overline{WR}$ IS INVALID AFTER OR COINCIDENT WITH $\overline{CS}$ LOW - TO - HIGH TRANSITION.
$\overline{RD}$ IS NOT ACTIVE DURING WRITE CYCLE.

Figure 2b. Timing Waveform for Write Cycle No. 2 ($\overline{CS}$ Controlled)

7

AC TEST CONDITIONS

Input Pulse Levels	DGND to +3.0 V
Input Rise/Fall Times	<5 ns
Timing Reference Levels	
Inputs	1.5 V
Outputs	
LOW	0.4 V
HIGH	2.4 V
Enabled to LOW	V_T −0.1 V
Enabled to HIGH	V_T +0.1 V
Disabled from LOW	V_{OL} +0.5 V
Disabled from HIGH	V_{OH} −0.5 V

V_T = 1.5 V, the voltage to which 3-stated outputs are forced.

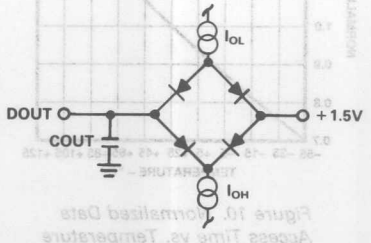


Figure 3. Output Load

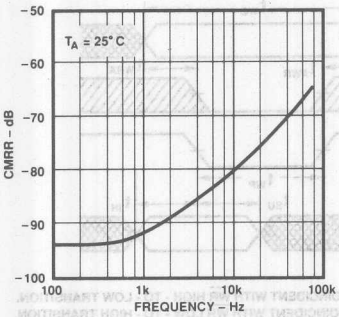


Figure 4. PGIA Common-Mode Rejection vs. Frequency, Gain = 1

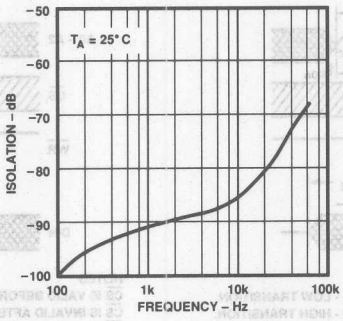


Figure 5. Multiplexer Off Isolation vs. Frequency

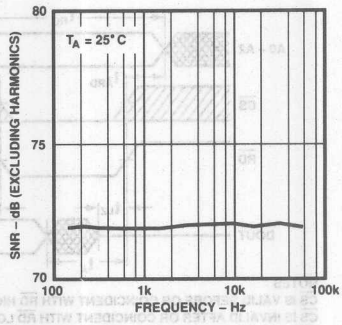


Figure 6. Signal-to-Noise Ratio vs. Frequency, Single Channel, Gain = 1

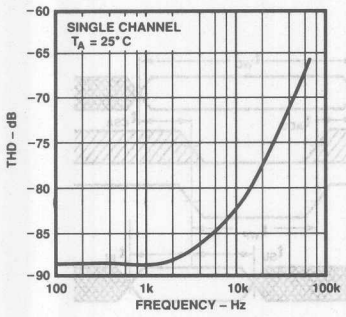


Figure 7. THD vs. Input Frequency, Single Channel, Gain = 1

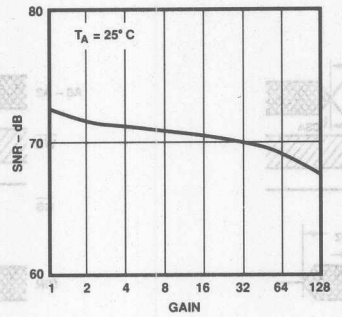


Figure 8. SNR vs. Gain, f_{IN} = 1904 Hz

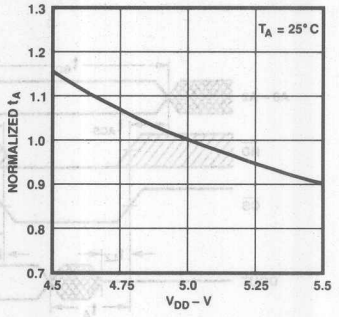


Figure 9. Normalized Data Access Time vs. V_{DD}

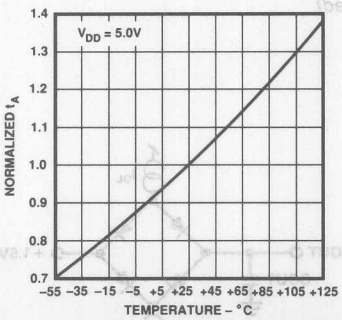


Figure 10. Normalized Data Access Time vs. Temperature

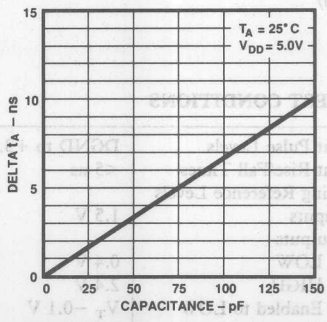


Figure 11. Change in Data Access Time vs. Loading

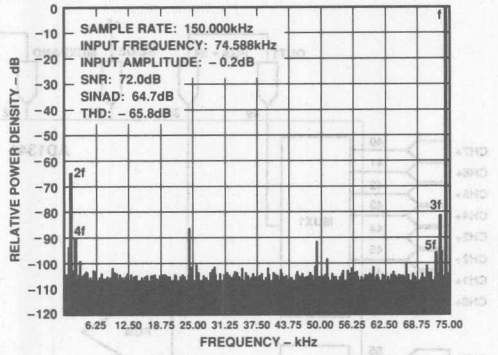


Figure 12. AD1341 Dynamic Performance (Single Channel, Gain = 1)

THEORY OF OPERATION

Functional Overview

The AD1341 is a complete data acquisition system designed with modern processor technology in mind. The heart of the AD1341 is a 12-bit Sampling Analog-to-Digital Converter with a maximum throughput of 150 kHz. The basic 10 V input range may be pin-strapped for either unipolar (0 to +10 V) or bipolar (−5 V to +5 V) operation. The ADC is preceded by a Programmable-Gain Instrumentation Amplifier possessing 8 binary-weighted gains between 1 and 128. Multiplexers provide 16 input channels which can be configured for either single-ended or 8-channel differential operation via a pin-strap option. All multiplexer inputs are fully protected against overvoltage and power-loss conditions. The multiplexer outputs and PGIA inputs are not internally connected to provide maximum flexibility and expansion capability. A +10 V reference output is also available.

The AD1341 offers a wide range of interface and control options. Programming and data readout are performed over a high speed asynchronous parallel 16-bit bus. Conversion results are stored in a 32-word FIFO which can be used to reduce I/O overhead. Six data formats are available. Sampling sequences of up to 32 channel/gain combinations are written to a command FIFO. A sampling sequence may be executed just once or may be continued indefinitely using the programmable Repeat mode. The AD1341 also includes expansion outputs which make possible a doubling of the number of input channels using a single external multiplexer. Expanded configurations retain all the operating features of a stand-alone AD1341. The interrupt structure is fully programmable. Status polling is fully supported. Finally, the AD1341 includes an independent programmable 16-bit countdown timer. Figure 13 shows a complete block diagram of the AD1341.

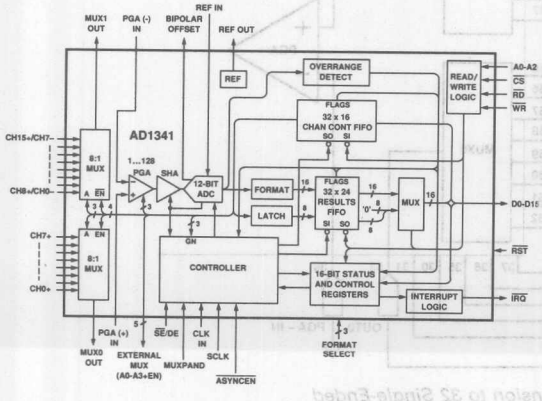


Figure 13. Functional Block Diagram

Input Configurations

The AD1341's ADC may be configured for either unipolar or bipolar inputs. Unipolar operation results when Ref Out (Pin 80) is connected to Ref In (Pin 79). BP Off (Pin 78) must be connected to Analog Signal Ground during unipolar operation. Bipolar operation requires the connection of Ref In, Ref Out, and BP Off. An external +10 V reference such as the AD2710 may be used if lower drift is required. A +10.24 V reference will provide a basic LSB size of 2 mV when the PGIA gain is set to 1.

The AD1341's multiplexer outputs and PGA inputs are not connected internally, but are instead brought out to package pins. Several pin-strapping options are possible to tailor the part to meet specific system requirements. The number of input channels may also be doubled with ease by using the AD1341's external multiplexer addressing capabilities.

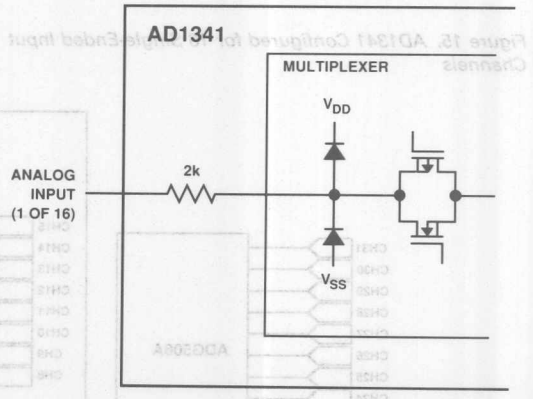


Figure 14. AD1341 Input Protection Circuitry

Single-ended or differential operation is selected using the $\overline{SE}$/DE input. When the MUXPAND input is grounded, the AD1341 can provide either 16 single-ended or 8 differential inputs. The number of inputs may be increased to 32 (single-ended) or 16 (differential) by pulling up the MUXPAND input and using an ADG506A multiplexer. Five expansion outputs enable and address the external multiplexer to give the expanded system the full functionality and programmability of a stand-alone AD1341. The four possible input schemes are shown in Figures 15 through 18, and the required pin-strapping is summarized in Table I.

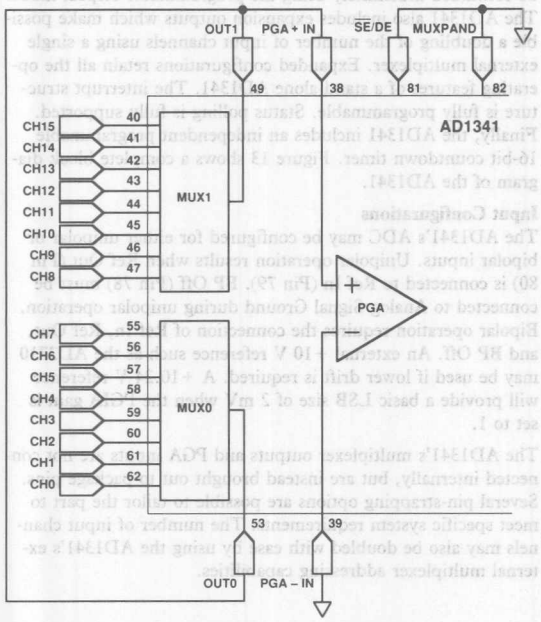


Figure 15. AD1341 Configured for 16 Single-Ended Input Channels

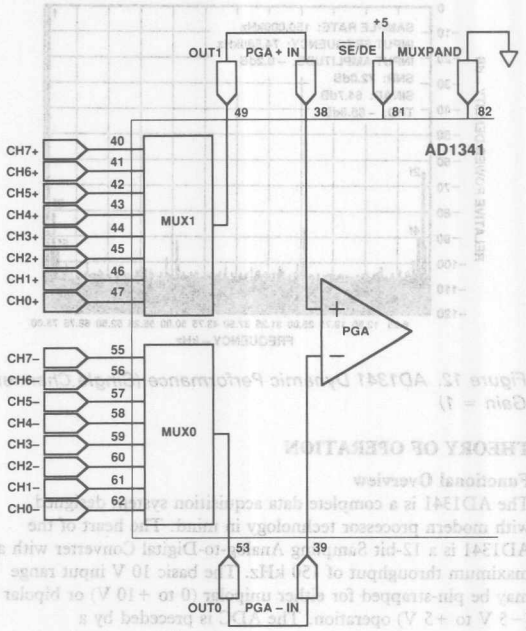


Figure 16. AD1341 Configured for 8 Differential Input Channels

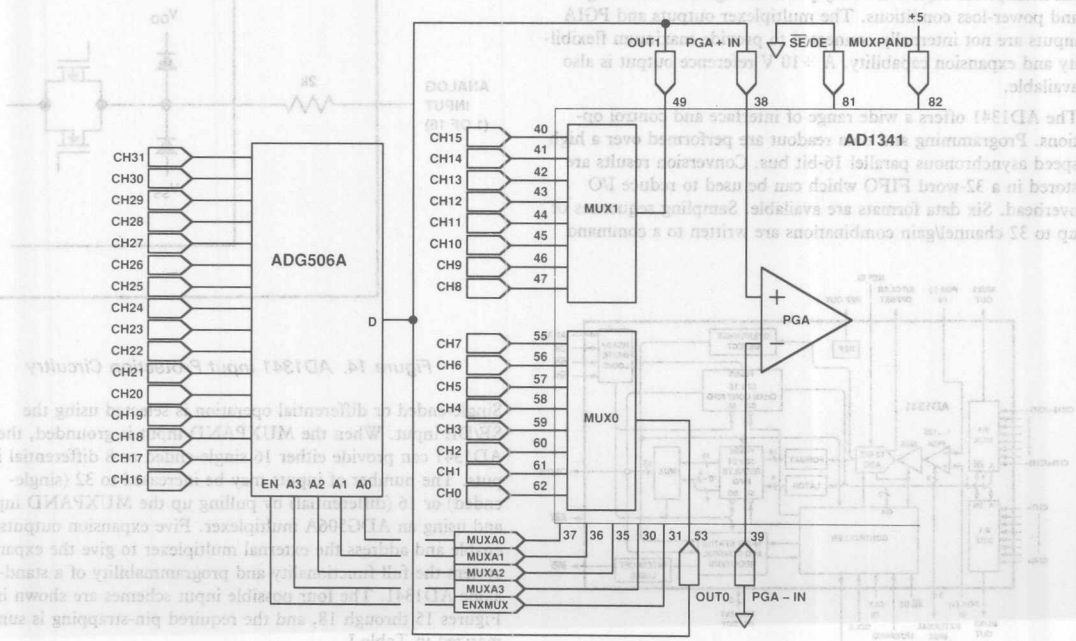


Figure 17. AD1341 with Expansion to 32 Single-Ended Input Channels

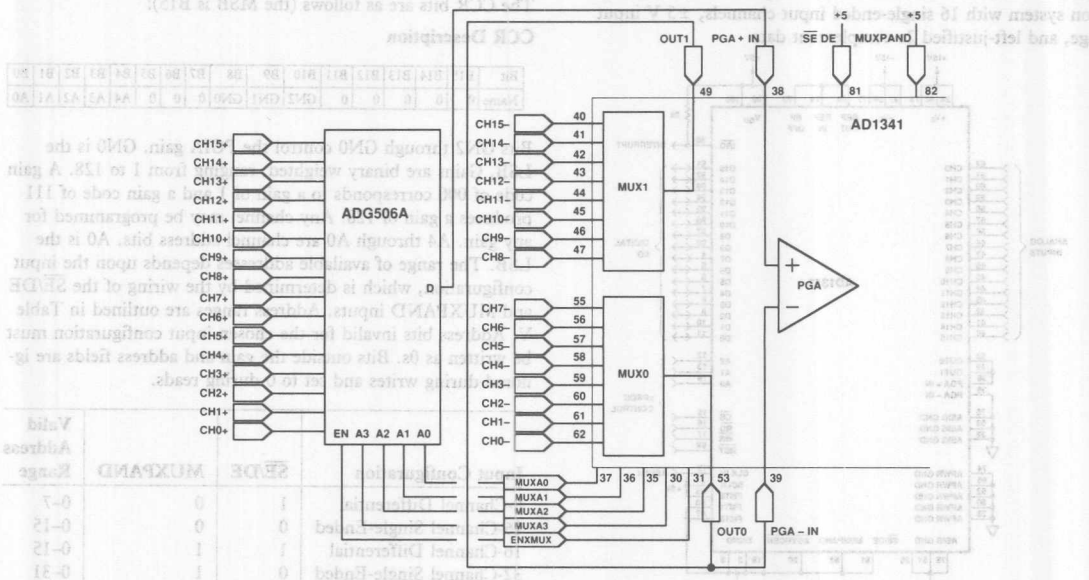


Figure 18. AD1341 with Expansion to 16 Differential Input Channels

	16-Channels Single-Ended	8-Channels Differential	32-Channels Single-Ended	16-Channels Differential
SE/DE	0	1	0	1
MUXPAND	0	0	1	1
MUXOUT1	PGA+IN	PGA+IN	PGA–IN	PGA–IN
MUXOUT0	PGA+IN	PGA–IN	PGA+IN	PGA–IN
ASIGGND	PGA–IN		PGA–IN	
D (ADG506A)			PGA+IN	PGA+IN
EN (ADG506A)			ENXMUX	ENXMUX
A0 (ADG506A)			MUXA0	MUXA0
A1 (ADG506A)			MUXA1	MUXA1
A2 (ADG506A)			MUXA2	MUXA2
A3 (ADG506A)			MUXA3	MUXA3

Table I. Connections for AD1341 Input Options

The AD1341's multiplexer inputs are protected against destructive latchup under power-loss and overvoltage conditions. Each input uses a 2 kΩ current-limiting resistor and two diodes to provide protection to at least 16 V beyond the analog supplies (Figure 14). The expanded input configurations in Figures 17 and 18 maybe similarly protected by adding 2 kΩ resistors in series with each external multiplexer input. Interactions between channels may occur under overload conditions. Unused AD1341 and ADG506A multiplexer inputs must be grounded.

Data Format Selection

Six data formats are available, offering a choice between natural binary and 2s complement coding with left, center, or right justification of the 12-bit result within the 16-bit field. The data format is determined by connections made to the three inputs FMT0, FMT1, and FMT2 (Pins 87, 86, and 85). These connections should be hardwired. Logical 0s are assigned to all unused places in the natural binary formats. The sign bit is extended as required and 0s are forced in empty least-significant places in the 2s complement formats. Tables II and III describe the data formats and their selection.

FMT2	FMT1	FMT0	Output Format
0	0	0	Natural Binary, Left Justified
0	0	1	Natural Binary, Right Justified
0	1	0	Natural Binary, Center Justified
0	1	1	Reserved
1	0	0	2s Complement, Left Justified
1	0	1	2s Complement, Right Justified
1	1	0	2s Complement, Center Justified
1	1	1	Reserved

Table II. Data Format Selection

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Nat Bin, LJ	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	0	0
Nat Bin, CJ	0	0	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0
Nat Bin, RJ	0	0	0	0	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
2s Com, LJ	$\overline{B11}$	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	0	0
2s Com, CJ	$\overline{B11}$	$\overline{B11}$	$\overline{B11}$	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0
2s Com, RJ	$\overline{B11}$	$\overline{B11}$	$\overline{B11}$	$\overline{B11}$	$\overline{B11}$	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

Table III. AD1341 Data Formats. D15 Is Data Bus MSB; B11 Is ADC MSB

range, and left-justified 2s complement data.

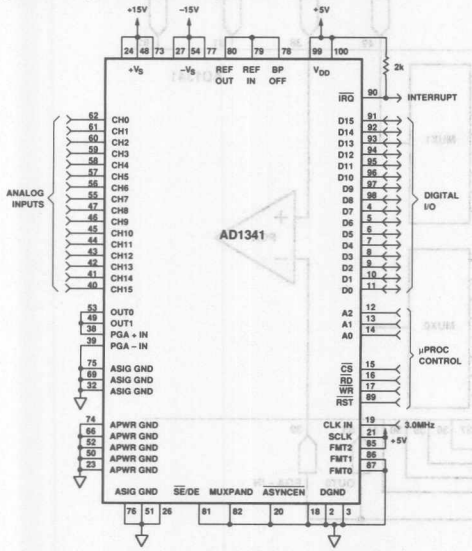


Figure 19. Typical Interface Circuit

Control Structure

The AD1341 is controlled through its digital interface. The device is completely disabled following power-up or a reset and must be programmed before conversions can be initiated.

Conversion sequences are stored in the Channel Control FIFO, from which they are subsequently executed. Each conversion instruction contains both a channel address and a channel gain. The Channel Control FIFO is 32 words deep.

Execution of programmed conversion sequences is enabled via the Mode Control Register. This register is also used to perform a programmed reset, to enable or disable interrupts, Repeat mode, and the timer, and to choose the system timing option. Selection from among a wide range of interrupt options is governed by the contents of the Interrupt Mask Register. Register contents may be read back for verification. A 32-word FIFO provides buffering for conversion results. The AD1341's register address space is defined in Table IV.

A2	A1	A0	Register Name/Function	Mnemonic	Type
0	0	0	Channel Control FIFO	CCR	R/W
0	0	1	Conversion Result FIFO	CRR	R
0	1	0	Reserved		
0	1	1	Reserved		
1	0	0	Mode Control Register	MCR	R/W
1	0	1	Timer Register	TMR	R/W
1	1	0	Interrupt Mask Register	IMR	R/W
1	1	1	Status Register	STS	R

Table IV. AD1341 Addresses

REGISTER DESCRIPTIONS

Channel Control Register (CCR)

The CCR is a 16-bit read/write register. Up to 32 CCR words may be written to the Channel Control queue for subsequent

CCR Description

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Name	0	0	0	0	0	GN2	GN1	GN0	0	0	0	A4	A3	A2	A1	A0

Bits GN2 through GN0 control the PGIA gain. GN0 is the LSB. Gains are binary weighted, ranging from 1 to 128. A gain code of 000 corresponds to a gain of 1 and a gain code of 111 produces a gain of 128. Any channel may be programmed for any gain. A4 through A0 are channel address bits. A0 is the LSB. The range of available addresses depends upon the input configuration, which is determined by the wiring of the $\overline{SE}$/DE and MUXPAND inputs. Address ranges are outlined in Table V. Address bits invalid for the chosen input configuration must be written as 0s. Bits outside the gain and address fields are ignored during writes and set to 0 during reads.

Input Configuration	$\overline{SE}$/DE	MUXPAND	Valid Address Range
8-Channel Differential	1	0	0–7
16-Channel Single-Ended	0	0	0–15
16-Channel Differential	1	1	0–15
32-Channel Single-Ended	0	1	0–31

Table V. AD1341 Address Ranges

The CCR should be read only *after* reading a conversion result from the CRR (see below). Reading the CRR causes the related CCR data to be stored in a temporary register. The contents of this register are presented on the data bus during a subsequent CCR read. If the first CCR read is not performed before the second CRR read, the gain and channel information associated with the first CRR result will be lost.

Conversion Result Register (CRR)

The CRR is a 16-bit read-only FIFO register. The results of conversions are stored in the CRR up to 32 words deep. The results can be read out sequentially without reading the CCR in between, but the channel and gain information for the previous result will be discarded. In the descriptions below R0–R11 represent the conversion result and SE represents sign-extension bits. These will be the same as R11 for 2s complement numbers and are 0 for natural (unsigned) binary numbers.

CRR Description—Left Justified

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Name	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0

CRR Description—Center Justified

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Name	SE	SE	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0

CRR Description—Right Justified

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Name	SE	SE	SE	SE	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0

Overrange and underrange results in natural binary format are coded as twelve 1s and twelve 0s, respectively, and are positioned within the 12-bit field as determined by the selected

These results will also be properly justified and sign-extended.

Mode Control Register (MCR)

The MCR is a 16-bit read/write register. It contains six active bits. The reset (default) state for all bits is 0.

MCR Description

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Name	INT	0	RST	0	CVN	0	REP	0	TIM	0	ACC	0	0	0	0	0

INT enables or disables the interrupt mask register (IMR). Interrupt generation under IMR control is enabled when INT is set to 1. New interrupts are disabled when INT is set to 0, but any interrupts pending when INT was set to 0 are not affected.

RST provides a programmed AD1341 reset. Writing a 1 to RST causes all registers and FIFOs to be reset to their default states. RST remains set until the reset sequence is complete, at which time it is cleared. A reset sequence requires one complete clock cycle and may take up to 667 ns (assuming a 3 MHz clock) depending upon the timing of the MCR write relative to the system clock.

CVN enables or disables conversions under host control. Setting CVN begins the execution of the conversion sequence stored in the CCR. Clearing CVN prevents the initiation of further conversions; any in-process conversion(s) will be completed and the conversion results written to the CRR. An in-process conversion is one for which the gain and channel instruction has been clocked out of the CCR. CVN may be set again anytime after it has been cleared; any conversions still in the CCR will resume in an orderly fashion.

REP enables the Repeat mode when set to 1. This bit may be set at any time. Setting REP disables any further writing to the CCR. Once REP has been set, the data written into the CCR queue since the last read will be repeated in a circular fashion. If Repeat mode is enabled after conversions have begun only the unexecuted conversions in the CCR queue will be repeated. Repeat mode functions with any number of instructions in the CCR queue. Clearing REP clears the CCR queue and the controller in preparation for receiving new data and starting new conversions.

TIM is used to disable or enable the 16-bit internal timer. The timer is disabled when TIM is set to 0, and enabled when TIM is set to 1. When enabled the counter counts down from the count stored in the TMR and generates an interrupt (if the timer interrupt is enabled). The preset count is then reloaded from the TMR and another countdown cycle begins on the next clock edge. Clearing TIM will halt the timer and clear its count. The contents of the TMR are not affected by clearing TIM. If the timer is enabled after having been disabled, it will begin its countdown from the previously programmed count. A Terminal Count signal is available on Pin 22.

ACC permits selection between standard and accelerated system timing (see *Conversion Timing*). Standard timing is selected when ACC is set to 0, and accelerated (optimized) timing is selected when ACC is set to 1.

Timer Register (TMR)

The TMR is a read/write register used to load and query the general purpose timer. Writing to the TMR will program a time

delay time = programmed count × basic delay unit.

The basic delay unit is one clock period, or 333.3 ns with a 3.00 MHz clock, and the maximum delay is 65535 basic delay units. T15 is the MSB. The reset (default) state for the TMR is 0. There may be an uncertainty of 1 clock period on the first countdown interval after the timer is enabled. All subsequent timer intervals will be identical and equal to the programmed delay provided timer operation is not interrupted.

TMR Description

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Name	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0

Reading the TMR will give the current programmed value. Reads are supported only when the timer is disabled. It is not possible to read the timer status during timer operation.

Interrupt Mask Register (IMR)

The IMR is a 16-bit read/write register. Setting bits in the IMR determines the conditions used to generate an interrupt to the host processor. The desired interrupt condition(s) is set by writing a 1 to the appropriate bit(s); all other IMR bits must be written as 0s. The reset (default) state for the IMR is all bits 0.

IMR Description

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Name	0	CVD	CVP	TME	0	ORG	0	CCF	CCH	CCE	0	0	0	CRF	CRH	CRE

Set IMR bits have the following effects:

CVD will cause an interrupt to be asserted every time a conversion result is shifted into the CRR.

CVP will cause an interrupt to be asserted when the conversion result obtained by executing the last command in the CCR is shifted into the CRR. The condition for a CVP interrupt is sensed at the scheduled start of the "last" conversion (see *Conversion Timing*). Writing another command to the CCR prior to the scheduled start of the "last" conversion will block the CVP interrupt.

TME will cause an interrupt to be asserted when the timer count reaches zero.

ORG will cause an interrupt to be asserted whenever overrange data are shifted into the CRR.

CCF will cause an interrupt to be asserted when the CCR queue is full. The CCR depth is 32 words.

CCH will cause an interrupt to be asserted when the CCR queue is at least half full (contains at least 16 words).

CCE will cause an interrupt to be asserted when the last channel/gain command is shifted out of the CCR and the conversion programmed therein begins. It is this conversion which leads to a CVP interrupt if no further commands are written to the CCR.

CRF will cause an interrupt to be asserted when the CRR is full. The CRR depth is 32 words.

CRH will cause an interrupt to be asserted when the CRR is at least half full.

CRE will cause an interrupt to be asserted when the CRR is empty.

Status Register (STS)

The Status Register is a 16-bit read only register which provides a continuous summary of the AD1341's internal state. The default condition for all STS bits is transparent. When an interrupt condition is enabled, the STS will latch the corresponding bit upon the assertion of the enabled interrupt; all other bits remain transparent. *The interrupt will remain asserted until the processor reads the STS contents; any latched STS bits will be reset to transparent mode once the read operation is completed.* Any pending interrupt conditions will continue the interrupt request once the STS register is read. The EVT bit is set whenever any of the unmasked interrupt conditions has generated an interrupt request.

STS Description

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Name	EVT	CVD	CVP	TME	0	ORG	0	CCF	CCH	CCE	0	0	0	CRF	CRH	CRE

STS bits correspond to IMR bits with the exception of EVT. STS bits have the following meanings:

EVT is set whenever an enabled interrupt event has occurred. This bit cannot be cleared directly by the user and remains set until the interrupt has been serviced.

CVD is set whenever a conversion is completed.

CVP is set whenever the conversion pipeline (CCR queue) is empty.

TME is set when the timer expires.

ORG is set when overrange or underrange data are shifted into the CCR.

CCF is set when the CCR queue has been filled.

CCH is set when the CCR queue is at least half full.

CCE is set when the CCR queue has been emptied.

CRF is set when the CRR FIFO is full.

CRH is set when the CRR FIFO is at least half full.

CRE is set when the CRR FIFO is empty.

Some of the remaining STS bit positions are used for diagnostic purposes. These bits (B11, B9, B5, B4, and B3) should be masked during normal operation.

FIFO Boundary Conditions

Overflow conditions occur whenever more than 32 words are written to either the CCR or the CRR. In both cases, data beyond the 32nd word are lost. The first 32 data words are not affected.

An underflow condition occurs when more than 32 words are read out of the CRR. The last valid word remains in the CRR and will be placed on the bus repeatedly in response to additional read commands. The CCR queue cannot underflow. Conversions cease after the last command in the CCR has been read and executed when Repeat mode is disabled.

Conversion Timing

The AD1341 normally overlaps some of its signal processing functions to maximize throughput. Such pipelining provides maximum throughput when multiple conversion instructions are buffered in the CCR and executed sequentially using the internal controller. Externally triggered conversions are also possible, either with or without pipelining. Finally, the internal timer may be used in conjunction with external triggering to further customize the sampling rate.

Pipelined Conversions

Normal pipelined operation is enabled by grounding the $\overline{\text{ASYNCEN}}$ input (Pin 20) and tying the SCLK input to V_{DD}. In this mode the AD1341's timing is governed by its internal controller. Channel and gain instructions for conversion N+1 are read from the CCR and executed at the start of A/D conversion N. This permits the PGIA's settling to occur during the A/D conversion. The AD1341's throughput depends on the number of channels and the gain mix because of the variation in PGIA settling time with gain. The internal sequencer always provides the proper settling time for the active channel regardless of the number of channels used or the gains selected.

There are two sequencer modes, Standard and Accelerated, selected using the ACC bit (Bit 5) in the MCR. Standard timing mode increases both the SHA acquisition time and the PGIA settling time for higher gains. Accelerated mode maintains constant SHA acquisition time independent of gain and provides maximum system throughput. Table VI details throughput performance for the two timing modes. The listed throughputs assume all channels operate at the same gain.

	Standard Mode		Accelerated Mode	
Gain	Clocks per Pipelined Conversion	Throughput, Pipelined (kHz)	Clocks per Pipelined Conversion	Throughput, Pipelined (kHz)
1–8	20	150.00	20	150.00
16	40	75.00	30	100.00
32	80	37.50	52	57.69
64	160	18.75	102	29.41
128	320	9.38	202	14.85

Table VI. AD1341 Timing and Throughput (3 MHz Clock)

When Repeat mode is enabled, the instructions in the CCR are read and executed indefinitely in a circular fashion. The per-channel sampling rate in Repeat mode for arbitrary numbers of channels and various gains can be determined with a simple calculation. This calculation uses the "Clocks per Pipelined Conversion" data from Table VI and the programmed channel and gain mix. Each channel is sampled at the calculated rate, while the exact sample time will be determined by the specific channel and gain order. The example below an assumes input expansion as shown in Figure 17.

11 channels at gains between 1 and 8	$11 \times 20 = 220$ clock periods
8 channels at gain of 16	$8 \times 30 = 240$ clock periods
5 channels at gain of 32	$5 \times 52 = 260$ clock periods
2 channels at gain of 64	$2 \times 102 = 204$ clock periods
4 channels at gain of 128	$4 \times 202 = 808$ clock periods
30 channels	1732 clock periods

$$\textit{System sample rate} = \frac{1}{1732 \times 333.33\ ns} = 1.73210\ kHz$$

Calculation of System Sample Rate (Accelerated Timing Mode, 3 MHz Clock)

It is also possible to measure the system sample rate by counting the number of clock periods between successive rising edges of the CC output. CC goes high at the start of the last conversion in a sequence and remains high until that conversion is completed. CC does not toggle when a single conversion is repeated. The duty cycle of CC depends on the number of channels in a sequence and their gains. Transitions of CC occur on rising clock edges.

Externally Triggered Conversions

Conversions may be triggered directly by the host system when $\overline{\text{ASYNCEN}}$ is tied to V_{DD}. *Externally triggered conversions may only be used with Repeat mode enabled.* Channel and gain information must first be written to the CCR. After all CCR writes are completed, REP (MCR Bit 9) should be set by the host processor. This clocks out the first CCR instruction, setting the multiplexer address and PGIA gain. A subsequent rising edge on the SCLK input places the SHA into Hold mode and triggers the A/D conversion, which is clocked to its completion using the 3 MHz clock. The first rising clock edge following the rising edge of SCLK also clocks the next channel/gain word from the CCR, permitting the pipelining of externally triggered conversions. The typical setup time for SCLK high relative to the rising edge of the clock is 10 ns.

The AD1341's acquisition timing controller is inoperative when $\overline{\text{ASYNCEN}}$ is tied high, so the host system must provide sufficient time to acquire each input before pulsing the SCLK line. Failure to do so will produce an incorrect conversion result. The minimum time required for a given gain may be found using the "Clocks per Pipelined Conversion" columns of Table VI. Externally triggered conversions have an inherent timing uncertainty of 1 clock period (333.3 ns with a 3 MHz clock) when SCLK is not synchronized with the external clock.

SCLK functions much like the Start-Convert input of a standard ADC. Unlike a conventional ADC, however, the AD1341 lacks a $\overline{\text{BUSY}}$ or STATUS output. The IMR may be programmed to cause an interrupt at the completion of each conversion, which will make the $\overline{\text{IRQ}}$ output functionally similar to a traditional $\overline{\text{BUSY}}$ or STATUS output. All AD1341 interrupt conditions function normally with externally-triggered conversions.

Timer-Controlled Conversions

The AD1341's programmable timer may be used to control externally triggered conversions, making possible extremely low sample rates with minimal host overhead. *Timer-controlled conversions may only be used with Repeat mode enabled.* TC (Pin 22) should be connected to SCLK (Pin 21), and the timer must be programmed to generate a delay at least equal to the largest required number of "Clocks per Pipelined Conversion" from Table VI.

MCR Bits 7 and 9 should be set after the CCR and TMR have been programmed. This will clock out the first CCR instruction and start the timer. The first input channel is sampled and the A/D conversion begins with first rising edge of the TC output, which indicates the end of the timer interval. This edge also clocks the next instruction from the CCR, reloads the timer delay stored in the TMR, and restarts the timer. A conversion is performed every time the timer expires until the AD1341 is reprogrammed or reset.

Single Conversions

Repeat must be disabled to perform a single conversion. The desired channel and gain must first be written to the CCR. Setting CVN (MCR Bit 11) will begin the conversion under internal timing control when $\overline{\text{ASYNCEN}}$ is low. The times required to perform the acquisition and conversion of a single sample are listed in Table VII; these times are measured from the first rising clock edge after CVN has been set. The typical setup time for CVN (trailing edge of $\overline{\text{WR}}$ to rising edge of CLK) is 10 ns.

Because acquisition and conversion begin on a clock edge rather than precisely when CVN is set, there may be an uncertainty in the instant at which the input is sampled. The variation will be up to one clock period in systems in which bus operation is not synchronous with the AD1341's 3 MHz clock, and one clock period (333 ns) should be added to the contents of Table VII to account for this. These variations can be eliminated when the host system's bus is synchronized with the 3 MHz clock provided CVN's setup time is met.

Gain	Standard Mode Conversion Time, µs	Accelerated Mode Conversion Time, µs
1–8	11.00	11.00
16	17.67	15.00
32	31.00	23.33
64	57.67	40.00
128	111.00	73.33

Table VII. AD1341 Conversion Times (3 MHz Clock, $\overline{\text{ASYNCEN}}$ Low)

With $\overline{\text{ASYNCEN}}$ high, single conversions may be triggered externally. The channel and gain instruction is clocked from the CCR when REP is set, and signal acquisition begins at that time. The rising edge of SCLK places the SHA into Hold mode, and the A/D conversion begins on the first rising clock edge following the SCLK transition. Table VIII lists the minimum permissible acquisition times between setting CVN and the rising edge of SCLK, along with the time required for the actual A/D conversion. The total conversion time is the sum of Table VIII's acquisition time and A/D time.

	Standard Mode		Accelerated Mode	
Gain	Acquisition Time, µs	A/D Time, µs	Acquisition Time, µs	A/D Time, µs
1–8	6.67	4.33	6.67	4.33
16	13.33	4.33	10.67	4.33
32	26.67	4.33	19.00	4.33
64	53.33	4.33	35.67	4.33
128	106.67	4.33	69.00	4.33

Table VIII. AD1341 Timing and Throughput (3 MHz Clock)

There is an uncertainty of one clock period in *both* the acquisition and A/D times listed in Table VIII when system operation is asynchronous. The first of these uncertainties arises from the variable relationship between the trailing edge of $\overline{\text{WR}}$ with respect to the rising edge of CLK, while the second results from the timing uncertainty between the rising edges of CLK and SCLK.

APPLICATIONS

Analog Interface

Each of the AD1341's 16 multiplexer inputs is protected against overvoltage and power-loss conditions by a series resistor and two diodes (Figure 14). Each input's time constant is typically 50 ns when the AD1341 is strapped for differential inputs and 100 ns in the single-ended configuration. The settling delays caused by these time constants have been accounted for in the AD1341's internal timing generator. Additional external series resistance will increase these time constants and could prevent the inputs from settling within the time allotted. For this reason the AD1341's inputs are best driven by low-impedance sources such as op amp outputs.

The AD1341's multiplexer outputs and PGIA inputs are brought out of the package to permit easy system expansion. Excessive capacitance at these pins should be avoided as it will also interfere with settling. All connections should be kept as short and direct as possible to minimize capacitance and noise coupling. (The AD1341's timing generator allows sufficient input settling time with the capacitance added by the expansion multiplexer as shown in Figures 17 and 18.)

A small amount of charge is dumped through each input whenever it is selected or deselected. The magnitude of this charge is typically 4 pC. Each signal source should have a low output impedance at high frequencies in order to absorb this transient. Micropower op amps may have difficulty with this type of transient because of their generally higher output impedances and lower gain-bandwidth products. The AD711, AD712, and AD713 are good choices for driving the AD1341's inputs.

Each multiplexer input requires a return path for off-state leakage currents. The driving source normally supplies this path. Unused inputs must not be left floating and should be connected to the analog ground plane.

Power Supplies and Grounds

Proper grounding and power supply bypassing techniques are necessary to obtain the AD1341's specified performance. The AD1341 has separate connections for analog signal ground, analog power ground, and digital ground. All Analog Signal and Power Ground pins must be connected to a common ground plane beneath the AD1341. This will provide the low impedance path required to minimize coupling between dynamic supply currents and low level signals being processed by the AD1341.

The AD1341's metal lid is internally connected to Analog Power Ground to provide maximum shielding against electrical interference. The lid faces the circuit board when the AD1341 is soldered in place. The board surface directly beneath the AD1341 should not contain signal or power traces to eliminate the possibility of short circuits. Using this area as a ground plane will result in the lowest possible ground impedance and will preserve signal fidelity.

The Digital Ground pins should also be connected to this ground plane if at all possible. This will provide the greatest immunity to digital switching noise. If this causes ground loops or other system-level problems then a separate ground plane or other low impedance return path must be provided. In this case the analog and digital grounds should be connected together at the AD1341 using back-to-back Schottky diodes and a good high frequency bypass capacitor. Ceramic capacitors in the range 0.01–0.1 μF are recommended. These components will prevent destructive dc potential differences between grounds and will also provide a low impedance path for transient currents.

Each power supply should be capacitively bypassed to the ground plane(s) with the capacitors located as closely as possible to the device in order to provide a low source impedance for dynamic signal and supply currents. Both ceramic and solid tantalum capacitors should be used for each supply. Appropriate values are 0.01–0.1 μF for ceramic capacitors and 1–10 μF for tantalum capacitors. Aluminum electrolytic capacitors have much higher equivalent series resistance than comparable-value tantalum devices and are not recommended.

Digital Interface

The AD1341's fast parallel bus simplifies the system designer's task by permitting zero-wait-state operation in most applications. In many cases the interface between the AD1341 and a microprocessor requires nothing more than an address decoding function. Figures 20 through 23 illustrate the AD1341's interface with several popular single-chip digital signal processors.

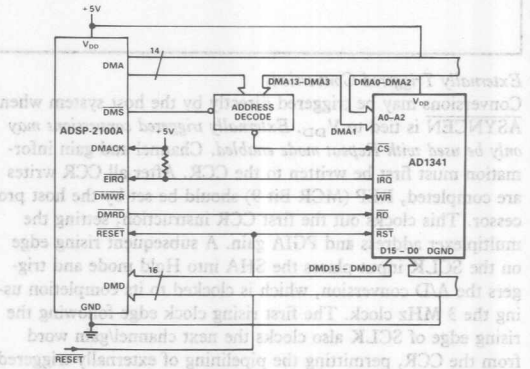


Figure 20. ADSP-2100A to AD1341 Interface

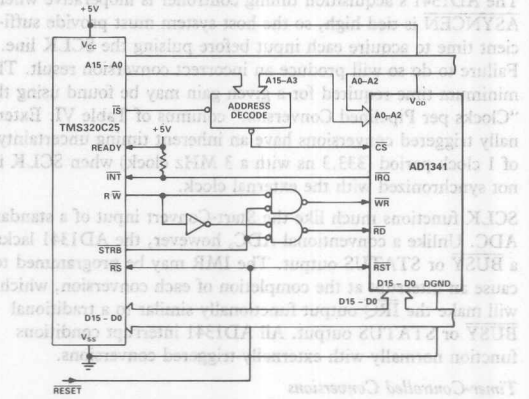


Figure 21. TMS320C25 to AD1341 Interface

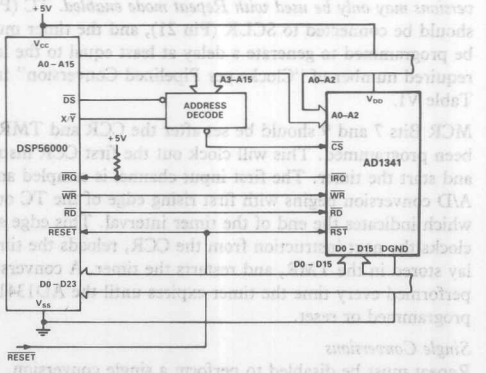


Figure 22. DSP56000 to AD1341 Interface

The AD1341's digital interface provides TTL- and CMOS-compatible levels with 10K ECL speed, exhibiting typical edge rates of 1.4 ns with 15 pF loading. Proper layout and impedance

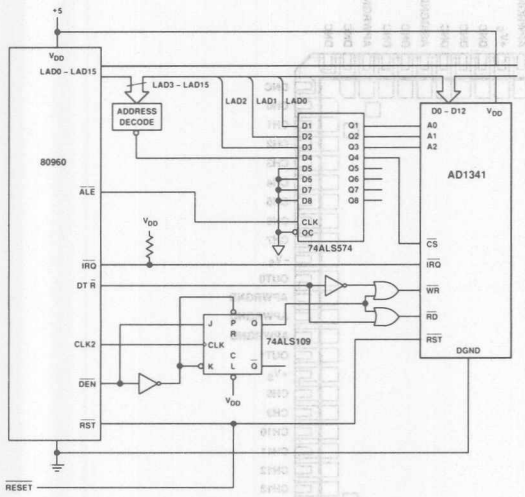


Figure 23. 80960 to AD1341 Interface

matching techniques are essential to prevent problems caused by crosstalk, reflections, and ground bounce.

Crosstalk

The fast edge rates and large voltage swings in CMOS systems will cause capacitive and inductive coupling (crosstalk) between adjacent PCB circuit traces. This will compromise signal integrity and reduce noise margins. The effect is most severe on "clocked" control lines ($\overline{RD}$, $\overline{WR}$, and $\overline{CS}$) which are close to data lines. The coupled noise may be large enough to initiate spurious I/O operations.

Crosstalk can be reduced by eliminating long parallel PCB circuit traces and by routing data lines away from clocked control lines. Grounded circuit traces may also be used to provide shielding between data and control lines, but this is less effective than physical separation.

Reflections

The gross impedance mismatches between high impedance CMOS inputs, low impedance CMOS outputs, and typical PCB circuit trace impedances can lead to voltage reflections and ringing. Reflections from impedance discontinuities become important whenever the line's round-trip delay exceeds the driving signal's rise or fall time. The critical line length, beyond which reflections begin to play a role, is only 13 cm for the AD1341, assuming an edge rate of 1.4 V/ns and a line delay of 0.055 ns/cm. The critical line length can be increased by running the signal lines over a ground plane because the added capacitance will reduce the edge rate (at the expense of increasing ground bounce).

A much better solution is to provide proper terminations for all signal lines. The AD1341's CMOS outputs do not have sufficient current drive capability to permit terminating PCB lines in their characteristic impedance. Series damping is a satisfactory alternative means to reduce reflections and ringing. A small resistor (typically 10 Ω to 75 Ω) is placed in series with the signal line as close to the signal source as possible. The goal is to match the driver's output resistance plus the series resistance to the line impedance. This will absorb any wave reflected back towards the source.

The primary disadvantage of series termination is that the line impedance and terminating resistor form a voltage divider network and the voltage along the line may lie between valid logic levels during the line's two-way propagation delay time. This means that while any number of device inputs may be connected at the end of the line, device inputs which require valid logic levels during the propagation delay time cannot be distributed along the line.

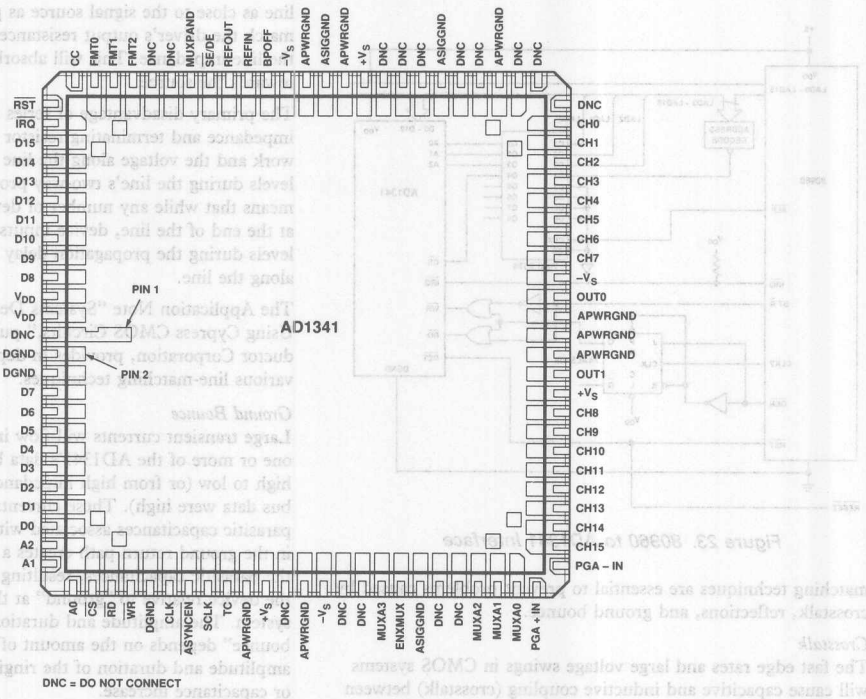
The Application Note "Systems Design Considerations When Using Cypress CMOS Circuits," published by Cypress Semiconductor Corporation, provides in-depth analysis and discussion of various line-matching techniques.

Ground Bounce

Large transient currents will flow into digital ground whenever one or more of the AD1341's data bus outputs switches from high to low (or from high impedance to low when the previous bus data were high). These currents result from the discharge of parasitic capacitances associated with the data bus. Inductance in the ground return path creates a resonant L-C circuit with the parasitic capacitances, resulting in ringing in "ground" at the device relative to "ground" at the supply or elsewhere in the system. The amplitude and duration of this ringing, or "ground bounce" depends on the amount of parasitic reactance. Both the amplitude and duration of the ringing increase as the inductance or capacitance increase.

The effect of ground bounce is to degrade the logic-low noise margin. This can result in system data errors. In particularly severe cases it can initiate spurious I/O operations in the AD1341 and cause the loss of data. The best defenses against ground bounce are to minimize the capacitive loading of the data bus and to use a ground plane to provide a low impedance return path for the inevitable transient currents. When large bus capacitance is unavoidable, it may prove beneficial to use BiCMOS bus transceivers between the AD1341 and the system data bus. This will increase both read and write cycle times, but the controlled edge speeds will reduce the peak currents, decreasing the possibility of erroneous data or I/O operations. The transceivers should be located close to the AD1341 to minimize the capacitance seen by the AD1341's data outputs.

7


AD1341
PIN 1
PIN 2
DNC = DO NOT CONNECT
CC
FMT0
FMT1
FMT2
DNC
DNC
MUXPAND
SE/DE
REFOUT
REFIN
BPOFF
–VS
APWRGND
ASIGGND
APWRGND
+VS
DNC
DNC
DNC
ASIGGND
DNC
DNC
APWRGND
DNC
DNC
RST
IRQ
D15
D14
D13
D12
D11
D10
D9
D8
VDD
VDD
DNC
DGND
DGND
D7
D6
D5
D4
D3
D2
D1
D0
A2
A1
DNC
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
–VS
OUT0
APWRGND
APWRGND
APWRGND
OUT1
+VS
CH8
CH9
CH10
CH11
CH12
CH13
CH14
CH15
PGA – IN
A0
CS
RD
WR
DGND
CLK
ASYNCEN
SCLK
TC
APWRGND
+VS
DNC
APWRGND
–VS
DNC
DNC
MUXA3
ENMUX
ASIGGND
DNC
DNC
MUXA2
MUXA1
MUXA0
PGA + IN

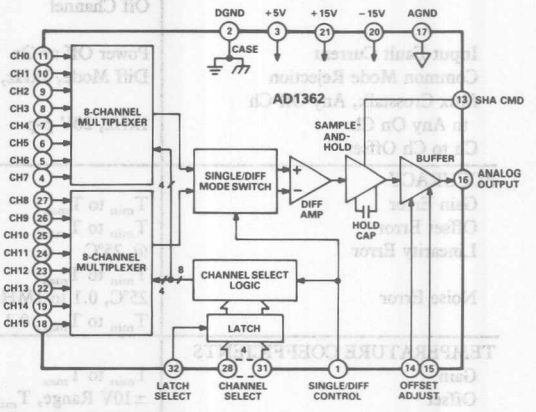
16-Channel, 12-Bit Data Acquisition System

AD1362

FEATURES

- **Pin and Functional Replacement for AD362:**
  - **Lower Power Dissipation**
  - **Lower Noise**
  - **Internal Hold Capacitor**
- **16 Single-Ended or 8 Differential Channels with Switchable Mode Control**
- **True 12-Bit Precision: Nonlinearity ≤0.005%**
- **High Speed: 10μs Acquisition Time to 0.01%**
- **Complete and Calibrated: No Additional Parts Required**
- **Versatile: Simple Interface to Popular Analog-to-Digital Converters**
- **High Differential Input Impedance ($10^{10}\Omega$) and Common Mode Rejection (80dB)**
- **Fully Protected Multiplexer Inputs**

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1362 is a complete, precision16-channel data acquisition system. The device contains two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output amplifier, a channel address latch and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD1362 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced by dynamically switching the input mode control.

The sample-and-hold mode control is designed to connect directly to the "Status" output of an analog-to-digital converter so that a convert command to the ADC will automatically put the sample-and-hold into the "Hold" mode. An internal precision hold capacitor is included with each AD1362. The AD1362 output amplifier is capable of driving the unbuffered analog input of most high speed, 12-bit successive-approximation ADCs. The interface is thereby reduced to two simple connections with no additional components required.

The AD1362KD is specified for operation over a 0 to +70°C temperature range while the AD1362SD operates to specification from −55°C to +125°C. Processing to MIL-STD-883, Class B is available for the AD1362SD. Both grades are packaged in a hermetic 32-pin ceramic dual-in-line package.

PRODUCT HIGHLIGHTS

1. The AD1362, when used with a precision analog to digital converter, forms a complete, accurate, high-speed data acquisition system.
2. The 16-input channels may be configured in single-ended, differential or a mixture of both modes. Mode switching is provided by a user controllable internal analog switch.
3. Multiplexers, differential amplifier, sample-and-hold and high-speed output buffer provide complete analog interfacing capabilities.
4. Internal channel address latches are provided to facilitate interfacing the AD1362 to data, address or control buses.
5. The AD1362 is specified over the entire military temperature range, −55°C to +125°C. Processing to MIL-STD-883, Class B is available.

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AD1362—SPECIFICATIONS (typical @ +25°C, ±15 V and +5 V unless otherwise noted)

Parameter	Test Condition	AD1362KD Min	AD1362KD Typ	AD1362KD Max	AD1362SD Min	AD1362SD Typ	AD1362SD Max	Units
ANALOG INPUTS								
Input Voltage Range	T_{min} to T_{max}	−10		+10	*		*	V
Input Bias Current	Per Channel			±50			*	nA
Input Impedance	On Channel		10			*		GΩ
			100			*		pF
	Off Channel		10			*		GΩ
			10			*		pF
Input Fault Current	Power Off or On			20			*	mA
Common Mode Rejection	Diff Mode, 1kHz, 20V p-p	70	80		*	*		dB
Mux Crosstalk, Any Off Ch to Any On Ch	1kHz, 20V p-p	−80	−90		*	*		dB
Ch to Ch Offset				±2.5			*	mV
ACCURACY								
Gain Error	T_{min} to T_{max}			±0.02			*	% FSR
Offset Error	T_{min} to T_{max}			±4			*	mV
Linearity Error	@ 25°C			±0.005			*	%
	T_{min} to T_{max}			±0.01			*	%
Noise Error	25°C, 0.1 to 1MHz			0.5			*	mV p-p
	T_{min} to T_{max}, 0.1 to 1MHz			1.0			*	mV p-p
TEMPERATURE COEFFICIENTS								
Gain	T_{min} to T_{max}			±4			±2	ppm/°C
Offset	±10V Range, T_{min} to T_{max}			±2			±1.5	ppm/°C
SAMPLE AND HOLD DYNAMICS								
Aperture Delay			150	200		*	*	ns
Aperture Uncertainty			100	500		*	*	ps
Acquisition Time	20V Step to ±0.01%		10	18		*	*	µs
Feedthrough	1kHz		−80	−70		*	*	dB
Droop Rate			1	2		*	*	mV/ms
Pedestal Voltage		−15	11	+15	*	*	*	mV
POWER SUPPLY REQUIREMENTS								
+V, Analog Voltage		+14.25		+15.75	*		*	V
−V, Analog Voltage		−14.25		−14.75	*		*	V
+V, Digital Voltage		+4.75		+5.25	*		*	V
+V, Analog Current				30			*	mA
−V, Analog Current				30			*	mA
+V, Digital Current				40			*	mA
Total Power Dissipation			0.5	1.1			*	W
TEMPERATURE RANGE								
Specification		0		+70	−55		+125	°C
Storage		−55		+85	−55		+150	°C

DIGITAL INPUT SIGNALS

Signal	Pins	TTL[1] Loads	Logic High	Logic Low
Input Channel Select	28-31	1LS	(4-Bit Binary Address)	
Channel Select Latch	32	8LS	Transparent	Latched
Single Ended/Diff Mode Select	1	3LS	Differential	Single Ended
Sample-and-Hold Command	13	2LS	Hold	Sample

NOTE

[1]One TTL Load is defined as I_{IL}=−1.6mA max @ V_{IL}=0.4V, I_{IH}=40µA max @ V_{IH}=2.4V. One LSTTL Load is defined as I_{IL}=−0.36mA @ V_{IL}=0.4V, I_{IH}=20µA max @ V_{IH}=2.7V.

*Specifications same as AD1362KD.

ABSOLUTE MAXIMUM RATINGS

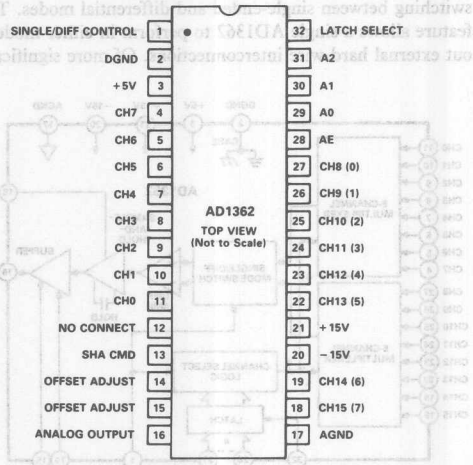
+V, Digital Supply . . . . . +5.5V
+V, Analog Supply . . . . . +17V
−V, Analog Supply . . . . . −17V
V_{IN}, Signal . . . . . ±V Analog Supply
V_{IN}, Digital . . . . . 0 to +V, Digital Supply
AGND to DGND . . . . . ±1V

ORDERING GUIDE

Model	Temperature Range	Max Gain TC	Package Option*
AD1362KD	0 to +70°C	±4ppm/°C	DH-32E
AD1362SD	−55°C to +125°C	±2ppm/°C	DH-32E
AD1362SD/883B	−55°C to +125°C	±2ppm/°C	DH-32E

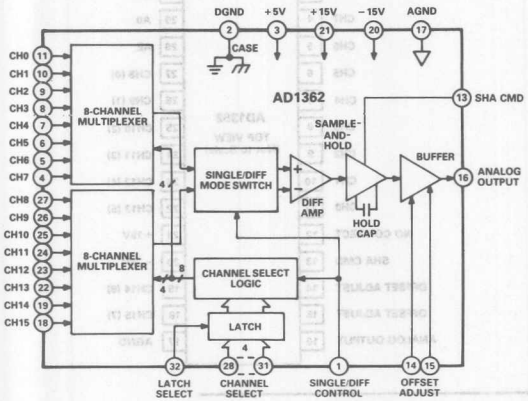
*DH-32E = Bottom Brazed Ceramic DIP. For Outline information see Package Information section.

PIN ASSIGNMENTS



Function	Number	Description
Single/Diff Control	1	Mode Select, Differential or Single Ended
DGND	2	Digital Ground
+5V	3	Digital Power Supply, +5V dc
Ch 7	4	"High" Analog Input Channel 7
Ch 6	5	"High" Analog Input Channel 6
Ch 5	6	"High" Analog Input Channel 5
Ch 4	7	"High" Analog Input Channel 4
Ch 3	8	"High" Analog Input Channel 3
Ch 2	9	"High" Analog Input Channel 2
Ch 1	10	"High" Analog Input Channel 1
Ch 0	11	"High" Analog Input Channel 0
NC	12	No Connect
SHA Cmd	13	Sample/Hold Control Input to SHA
Offset Adjust	14	Offset Adjustment Input #1
Offset Adjust	15	Offset Adjustment Input #2
Analog Output	16	Analog Output to ADC
AGND	17	Analog Ground
Ch 15	18	"High" ("Low") Analog Input Channel 15 (7)
Ch 14	19	"High" ("Low") Analog Input Channel 14 (6)
−15V	20	Negative Analog Power Supply −15V dc
+15V	21	Positive Analog Power Supply +15V dc
Ch 13	22	"High" ("Low") Analog Input Channel 15 (5)
Ch 12	23	"High" ("Low") Analog Input Channel 14 (4)
Ch 11	24	"High" ("Low") Analog Input Channel 13 (3)
Ch 10	25	"High" ("Low") Analog Input Channel 12 (2)
Ch 9	26	"High" ("Low") Analog Input Channel 11 (1)
Ch 8	27	"High" ("Low") Analog Input Channel 10 (0)
AE	28	Input Channel Address MSB
A0	29	Input Channel Address Bit 0
A1	30	Input Channel Address Bit 1
A2	31	Input Channel Address Bit 2
Latch Select	32	Channel Select Latch Control Input

channel address latches and control logic as shown in the block diagram. The multiplexers can be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD1362 is an internal analog switch controlled by a digital input that performs switching between single-ended and differential modes. This feature allows a single AD1362 to perform in either mode without external hard-wire interconnections. Of more significance is



AD1362 Block Diagram

Multiplexer channel address inputs are interfaced through a level-triggered ("transparent") input register. With a Logic "1" at the Latch Select input, the address signals feed through the register to directly select the appropriate input channel. This address information can be held in the register by placing a Logic "0" on the Latch Select input. Internal logic monitors the status of the Single-Ended/Differential Mode input and addresses the multiplexers accordingly.

A differential amplifier buffers the multiplexer outputs while providing high input impedance in both differential and single-ended modes.

The sample-and-hold is a high speed device that can also function as a gated operational amplifier. Its uncommitted differential inputs allow it to serve a second role as the output subtractor in the differential amplifier. A Logic "1" on the Sample-and-Hold Command input will cause the sample-and-hold to "freeze" the analog signal while the ADC performs the conversion. Normally the Sample-and-Hold Command is connected to the ADC Status output which is at Logic "1" during conversion and Logic "0" between conversions. For slowly changing inputs, throughput speed may be increased by grounding the Sample-and-Hold Command input instead of connecting it to the ADC status.

The output buffer is a high speed amplifier whose output impedance remains low and constant at high frequencies. Therefore, the AD1362 may drive a fast, unbuffered, precision ADC without loss of accuracy.

THEORY OF OPERATION

Concept

The AD1362 is intended to be used in conjunction with a high speed, precision analog-to-digital converter to form a complete data acquisition system (DAS). Figure 1 shows a general AD1362 with ADC DAS application.

By dividing the data acquisition task into two sections, several important advantages are realized. Performance of each design is optimized for its specific function. Production yields are increased thus decreasing costs. Furthermore, the standard configuration packages plug into standard sockets and are easier to handle than larger packages with higher pin counts.

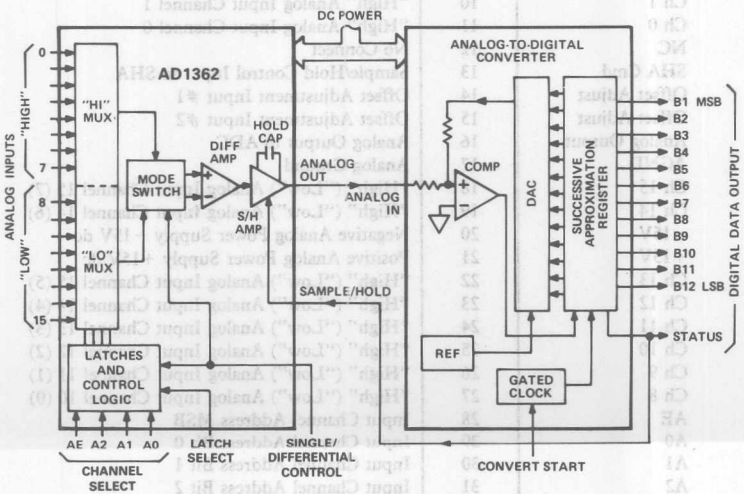


Figure 1. AD1362 with ADC as a Complete Data Acquisition System

System Timing

Figure 2 is a timing diagram for the AD1362 connected as shown in Figure 1 and operating at maximum conversion rate. The ADC is assumed to be a conventional 12-bit type such as the AD573 or AD ADC80.

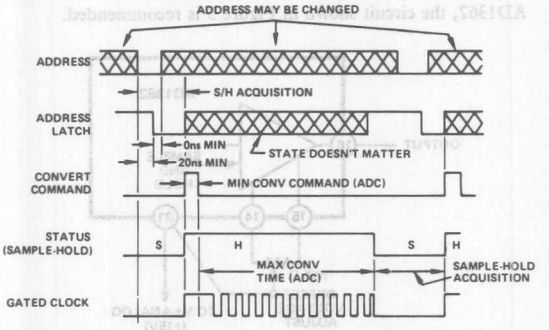


Figure 2. DAS Timing Diagram

The normal sequence of events is as follows:

1. The appropriate Channel Select Address is latched into the address register. Time is allowed for the multiplexers to settle.
2. A Convert Start command is issued to the ADC which, in response, indicates that it is "busy" by placing a Logic "1" on its Status Line.
3. The ADC Status controls the sample-and-hold. When the ADC is "busy," the sample-and-hold is in the Hold mode.
4. The ADC goes into its conversion routine. Since the sample-and-hold is holding the proper analog value, the address may be updated during conversion. Thus multiplexer settling time can coincide with conversion and need not affect throughput rate.
5. The ADC indicates completion of its conversion by returning Status to Logic "0." The sample-and-hold returns to the Sample mode.
6. If the input signal has changed full scale (different channels may have widely-varying data), the sample-and-hold will typically require 10 microseconds to "acquire" the next input to sufficient accuracy for 12-bit conversion.

After allowing a suitable interval for the sample-and-hold to stabilize at its new value, another Convert Start command may be issued to the ADC.

NOTE

Valid Output Data

Not all ADCs have all data bits available when Status indicates that the conversion is complete. Some successive approximation ADCs must have a Status delay built in or the final data bit will lag Status. This will result in two problems:

1. The sample-and-hold will return to Sample, disturbing the analog input to the ADC as it is attempting to convert the least significant bit. This may result in an error.
2. If the falling edge of Status is being used to load the data into a register, the least significant bit will not be valid when loaded.

An external delay or use of an ADC with a valid Status output is necessary to prevent this problem.

Single-Ended/Differential Mode Control

The AD1362 features an internal analog switch that configures the Analog Input Section in either a 16-channel single-ended or 8-channel differential mode. This switch is controlled by a TTL logic input applied to Pin 1:

"0": Single-Ended (16 channels)
"1": Differential (8 channels)

When in the differential mode, a differential source may be applied between corresponding "High" and "Low" analog input channels.

It is possible to mix SE and DIFF inputs by using the mode control to command the appropriate mode. In this case, four microseconds must be allowed for the output to settle to within ±0.01% of its final value, but if the mode is switched concurrent with changing the channel address, no significant additional delay is introduced. The effect of this delay may be eliminated by changing modes while a conversion is in progress (with the sample-and-hold in the "Hold" mode). When SE and DIFF signals are being processed concurrently, the DIFF signals must be applied between corresponding "High" and "Low" analog input channels. Another application of this feature is the capability of measuring 16 sources individually and/or measuring differences between pairs of those sources.

Input Channel Addressing

Table I is the truth table for input channel addressing in both the single-ended and differential modes. The 16 single-ended channels may be addressed by applying the corresponding digital number to the four Channel Select address bits, AE, A0, A1, A2 (Pins 28–31). In the differential mode, the eight channels are addressed by applying the appropriate digital code to A0, A1, and A2; AE must be enabled with a Logic "1." Internal logic monitors the status of the SE/DIFF Mode input and addresses the multiplexers singularly or in pairs as required.

When the channel address is changed, six microseconds must be allowed for the AD1362 to settle to within ±0.01% of its final output (including settling times of all elements in the signal path). The effect of this delay may be eliminated by performing the address change while a conversion is in progress (with the sample-and-hold in the "Hold" mode).

ADDRESS				ON CHANNEL		
					Differential	
AE	A2	A1	A0	Single Ended	"Hi"	"Lo"
0	0	0	0	0	None	
0	0	0	1	1	None	
0	0	1	0	2	None	
0	0	1	1	3	None	
0	1	0	0	4	None	
0	1	0	1	5	None	
0	1	1	0	6	None	
0	1	1	1	7	None	
1	0	0	0	8	0	0
1	0	0	1	9	1	1
1	0	1	0	10	2	2
1	0	1	1	11	3	3
1	1	0	0	12	4	5
1	1	0	1	13	5	5
1	1	1	0	14	6	6
1	1	1	1	15	7	7

Table I. Input Channel Addressing Truth Table

Input Channel Address Latch

The AD1362 is equipped with a latch for the input Channel Select address bits. If the Latch Select pin is at Logic "1," input channel select address information is passed through to the multiplexers. A Logic "0" "freezes" the input channel address present at the inputs at the "1"-to-"0" transition (level-triggered).

This feature is useful when input channel address information is provided from an address, data or control bus that may be required to service many devices. The ability to latch an address is helpful whenever the user has no control of when address information may change.

Sample-and-Hold Mode Control

The Sample-and-Hold Mode Control input is normally connected to the Status output from an analog to digital converter. When a conversion is initiated by applying a Convert Start command to the ADC, Status goes to Logic "1" putting the sample-and-hold into the "Hold" mode. This "freezes" the information to be digitized for the period of conversion. When the conversion is complete, Status returns to Logic "0" and the sample-and-hold returns to the "Sample" mode. Eighteen microseconds must be allowed for the sample-and-hold to acquire ("catch up" to) the analog input to within ±0.01% of the final value before a new Convert Start command is issued.

The purpose of a sample-and-hold is to "stop" fast changing input signals long enough to be converted. In this applicatain, it also allows the user to change channels and/or SE/DIFF mode while a conversion is in progress thus eliminating the effects of multiplexer, analog switch and differential amplifier settling times. If maximum throughput rate is required for slowly changing signals, the Sample-and-Hold Mode Control may be wired to ground (Logic "0") rather than to ADC Status thus leaving the sample-and-hold in a continuous Sample mode.

Analog Input Section Offset Adjust Circuit

Although the offset voltage of the AD1362 may be adjusted, that adjustment is normally performed at the ADC. In some special applications, however, it may be helpful to adjust the offset of the Data Acquisition System. An example of such a case would be if the input signals were small (<10mV) relative to AD1362 offset and gain errors. To adjust the offset of the AD1362, the circuit shown in Figure 3 is recommended.

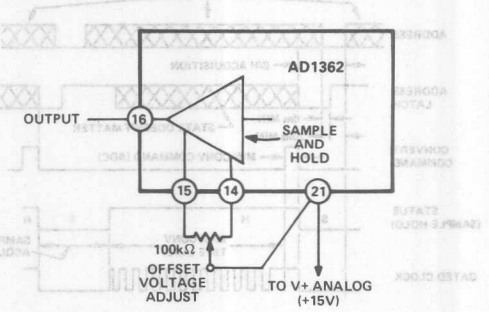


Figure 3. AD1362 Offset Voltage Adjustment

Under normal conditions, all calibration is performed at the ADC Section.

Other Considerations

Grounding: Analog and digital signal grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground and Digital Ground are not connected internally; these pins must be connected externally for the system to operate properly. Preferably, this connection is made at only one point, as close to the AD1362 as possible. The case is connected internally to Digital Ground to provide good electrostatic shielding. If the grounds are not tied common on the same card with the AD1362, the digital and analog grounds should be connected locally with back-to-back general-purpose diodes as shown in Figure 4. This will protect the AD1362 from possible damage caused by voltages in excess of ±1 volt between the ground systems which could occur if the key grounding card should be removed from the overall system. The device will operate properly with as much as ±200mV between grounds; however, this difference will be reflected directly as an input offset voltage.

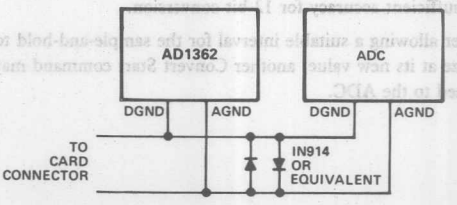


Figure 4. Ground-Fault Protection Diodes

Power Supply Bypassing: The ±15V and +5V power leads should be capacitively bypassed to Analog Ground and Digital Ground respectively for optimum device performance. One microfarad tantalum types are recommended; these capacitors should be located close to the system. It is not necessary to shunt these capacitors with disk capacitors to provide additional high frequency power supply decoupling since each power lead is bypassed internally with a 0.039μF ceramic capacitor.

Interfacing to Popular Analog to Digital Converters

The AD1362 has been designed to interface directly to most analog to digital converters; often no additional components are required and only two interconnections must be made. The direct interface requirements for the ADC are as follows:

1. The ADC Status output must be positive-true Logic ("1" during conversion).
2. Transition from "0" to "1" must occur at least 200ns before the most significant bit decision is made (successive approximation ADC) or before input integration starts (integrating type ADC).
3. Status must not return to "0" before the LSB decision is made.
4. If Status is being used to latch output data, it must not return to Logic "0" until all output data bits are valid and available.

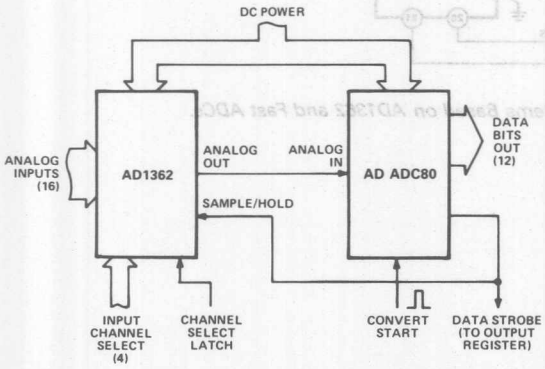
Complete system throughput performance is determined by combining the worst-case specifications of the AD1362 and the ADC. If guaranteed system performance is required, the AD363 and AD364 are recommended. The AD363 includes an AD1362 and an AD572 12-bit, 25-microsecond precision ADC. The AD364 consists of an AD1362 and an AD574 12-bit, microprocessor compatible, low cost ADC. Each is specified as a complete, two-package system.

Figure 5a shows the AD1362 driving an AD ADC80. The AD ADC80 is a 12-bit, 25-microsecond, low cost ADC that meets all of the requirements listed above. Throughput rate is typically 30kHz with no missing codes over the operating temperature range.

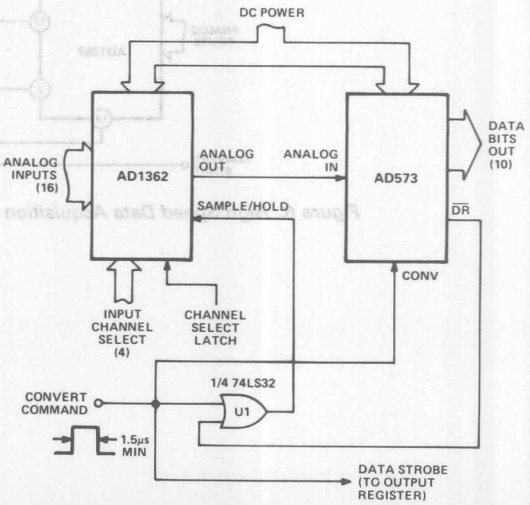
Figure 5b shows a 10-bit application based on the AD1362 and the AD573, a complete low cost 10-bit, 25-microsecond ADC. In this case, one of the above requirements is not met:

1. $\overline{DR}$ ($\overline{DATA\ READY}$), as Status, is positive-true, but . . .
2. $\overline{DR}$ does not indicate that a conversion is in progress until 1.5μs after conversion starts.

The gating provided by U1 allows the applied convert command (CC) to initiate input hold at the AD1362. CC must last for more than 1.5μs so that $\overline{DR}$ may then assume control of Hold.



a. 12-Bit DAS Using AD1362 and AD ADC80



b. 10-Bit Using AD1362 and AD573

Figure 5. Data Acquisition Systsems Based on the AD1362 and Popular ADCs

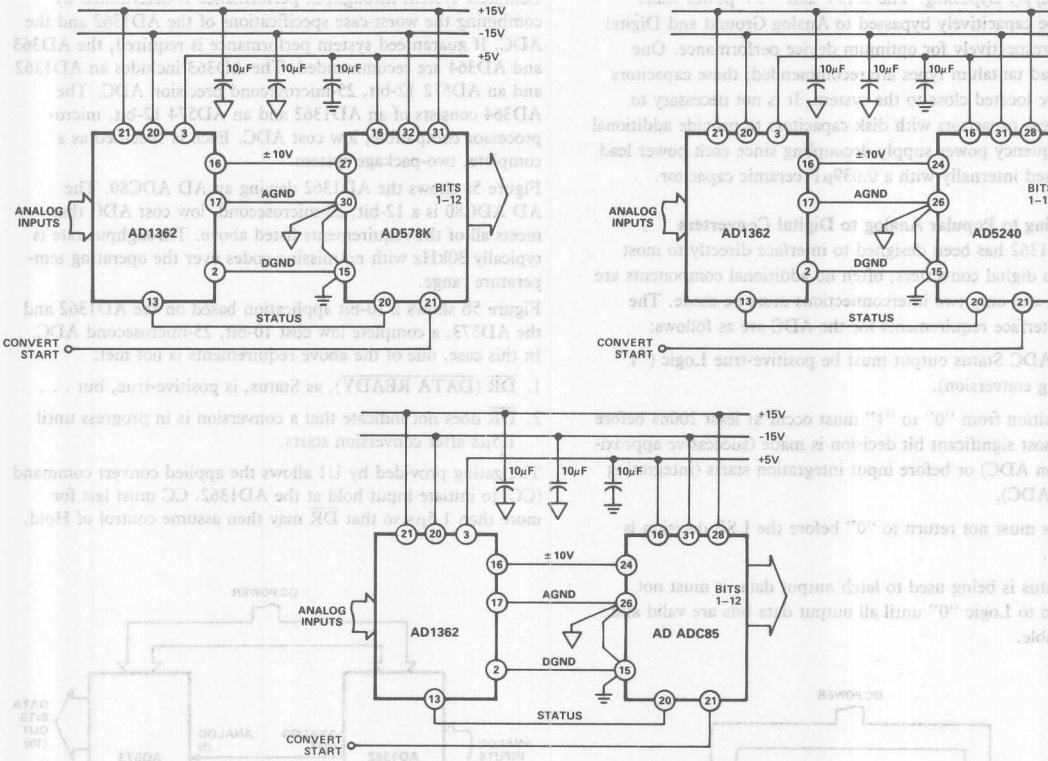


Figure 6. High Speed Data Acquisition Systems Based on AD1362 and Fast ADCs.

Data Acquisition System

AD79015

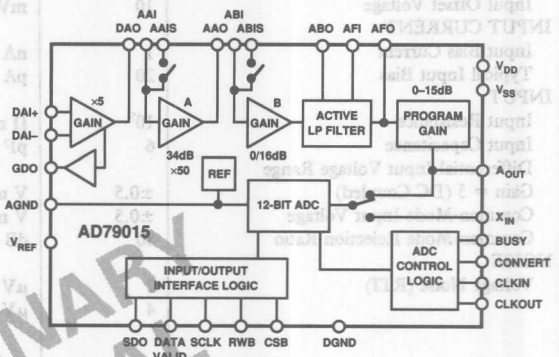
FEATURES

Functional Complete DAS
Single Package
Monolithic
High Impedance Differential Inputs
Guaranteed Low 1 nA Input Bias Current
Guaranteed 80 dB Common-Mode Rejection
External Selectable Bandpass Filter Frequencies
Software Programmable Gain Selection
12-Bit A/D Converter with On-Chip Reference
Serial Communication Interface
Data Sampling 40,000 Samples/Second
± 5 V Supplies
Low 175 mW (typ) Power Consumption
Small 28-Terminal Surface Mount Package (PLCC)

APPLICATION

Small Signal Data Acquisition
ECG Signal Data Acquisition
Patient Monitoring

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD79015 is a complete data acquisition system for very small signals (i.e., biomedical ECG) with a data sampling rate of minimum 40,000 samples/sec. It provides high accuracy, high stability, and functional completeness in a single 28-pin package.

It includes a high performance instrumentation amplifier at the front-end, bandpass filter, and an accurate 12-bit ADC with on-chip reference.

An on-chip clock circuit is provided, which may be used with a crystal for stand-alone operation. Alternatively, the clock input may be driven from an external CMOS-compatible clock source such as a microprocessor clock.

The AD79015 serial interface is compatible with many microprocessors and digital signal processors such as the ADSP-2100, TMS32020, μPD7720, and DSP-56000. It can also be used with general purpose serial to parallel converters such as shift registers.

The AD79015 is fabricated in Analog Devices' linear compatible CMOS process (LC^2MOS), an advanced, all ion-implanted process that combines fast CMOS logic and linear, bipolar circuits on a single chip, thus achieving excellent linear performance while still retaining low CMOS power levels.

PRODUCT HIGHLIGHTS

1. Single chip, complete small signal DAS. It includes a high performance differential front end amplifier, programmable gain stages, externally controlled high and low corner frequencies, and a 12-bit AD converter with on-chip reference.
2. Input amplifier has extremely low input bias current of <1 nA over full temperature range. Typical input bias current at ambient temperature is 20 pA.
3. On-chip guard driver to minimize external components.
4. Software programmable gain setting with a gain range of 0 dB to 31 dB.
5. On-chip clock oscillator to minimize external components.
6. A serial interface is provided to make it easy to use AD79015 in applications where full isolation from the mains power is required.
7. Serial interface supports multichannel applications with minimal external components.
8. LC^2MOS circuitry gives low power drain (175 mW typ) from +5 V, and −5 V supplies.

PRELIMINARY TECHNICAL DATA

7

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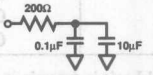
AD79015—SPECIFICATIONS (V_{DD} = +5 V ± 5%, and V_{SS} = −5 V ± 5%. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	All Grades	Units	Test Condition/Comments
INPUT AMPLIFIER			
GAIN			
Gain Range	14	dB	
	5	V/V	
Gain Error	±0.1	dB max	Over Full Temperature Range
VOLTAGE OFFSET			
Input Offset Voltage	10	mV max	
INPUT CURRENT			
Input Bias Current	1	nA max	Over Full Temperature Range
Typical Input Bias	20	pA	Typical at +25°C
INPUT			
Input Resistance	10^9	Ω min	
Input Capacitance	6	pF typ	
Differential Input Voltage Range			
Gain = 5 (DC Coupled)	±0.5	V max	
Common-Mode Input Voltage	±0.5	V max	
Common-Mode Rejection Ratio	80	dB min	
NOISE			
Voltage Noise (RTI)	2	μV p–p typ	Bandwidth 0.1 Hz–10 Hz @ +25°C
	4	μV p–p typ	Bandwidth 0.1 Hz–100 Hz @ +25°C
			Assume Gaussian Noise −V p–p = 6.6 × V rms, 0.1% Probability of Error
GUARD DRIVER			
Capacitive Load	100	pF max	
Resistive Load	2	kΩ min	
AMPLIFIER A			
Gain	34	dB	
	50	V/V	
Gain Accuracy	0.1	dB max	
	1.2	%	
Input Offset Voltage	2	mV max	
Input Bias Current	5	nA typ	
AMPLIFIER B/LOW PASS FILTER			
Gain			
Low	0	dB	
	1.0	V/V	
High	16	dB	
	6.3	V/V	
Gain Error	0.2	dB max	
	2.4	%	
Input Offset	2	mV max	
Resistors in Network	5	% max	of Absolute Value, over Full Temperature Range
PROGRAMMABLE GAIN AMPLIFIER			
Gain			
Minimum Gain	0	dB	
	1.0	V/V	
Maximum Gain	15	dB	
	5.6	V/V	
Gain Step Size	1	dB	
	12.2	%	
Gain Accuracy	0.1	dB max	
	1.0	V/V	
Input Offset Voltage	2	mV max	

PRELIMINARY TECHNICAL DATA

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Parameter	All Grades	Units	Test Condition/Comments
CONVERTER (Core Cell Is the AD7870)			
DYNAMIC PERFORMANCE			
Signal-to-Noise Ratio (SNR)	68	dB	min, V_{IN} = 1 kHz Sine, f_{SAMPLE} = 10 kHz
Total Harmonic Distortion	−80	dB	max, V_{IN} = 1 kHz Sine, f_{SAMPLE} = 10 kHz
No Missed Codes	Guaranteed		
Track/Hold Acquisition Time	2	µs	max
Conversion Time	13.25	µs	@ 4 MHz Clock Frequency
DC ACCURACY			
Resolution	12	Bits	
Relative Accuracy	±1	LSB	Typical
DNL	±1	LSB	Typical
Bipolar Zero Offset	±1	%	@ V_{IN} = 0 V
Full-Scale Error	±1	%	@ V_{IN} = −3 V or V_{IN} = +3 V, Relative to Reference
ANALOG INPUT			
Input Voltage Range	±3	V	
Input Current	±550	µA	max
REFERENCE OUTPUT			
		V min/V	
Reference Voltage @ +25°C	2.98/3.02	max	AC Decoupling Required
Reference Tempco	±40	ppm°C typ	
DIGITAL INTERFACE			
INPUTS			
Logic "1" Voltage	+2.0	V min	
Logic "0" Voltage	+0.8	V max	
Input Current	±10	µA max	V_{IN} = 0 to V_{DD}
Input Capacitance	10	pF max	
OUTPUTS			
Logic "1" Voltage	+2.4	V min	I_{SOURCE} = 200 µA
Logic "0" Voltage	+0.4	V max	I_{SINK} = 1.6 mA
Floating State Leakage	±10	µA max	
Floating State Capacitance	15	pF max	
POWER REQUIREMENTS			
V_{DD}	+5	V nominal	±5% for Specified Performance
V_{SS}	−5	V nominal	±5% for Specified Performance
I_{DD}	25	mA max	
I_{SS}	25	mA max	
Power Dissipation	175	mW typ	
TEMPERATURE RANGE (T_{MIN} to T_{MAX})	0 to +70	°C	



Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND . . . . . −0.3 V to +7 V
V_{SS} to DGND . . . . . +0.3 V to −7 V
AGND to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
Analog Input Voltage to AGND . . . . . V_{SS} to V_{DD}
Digital Input Voltage to DGND . . . . . −0.3 to V_{DD} + 0.3 V
Digital Output Voltage to DGND . . . . . −0.3 to V_{DD} + 0.3 V
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to + 150°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C . . . . . by 6 mW/°C

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

CAUTION

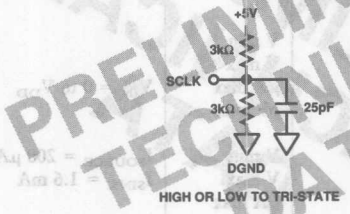
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



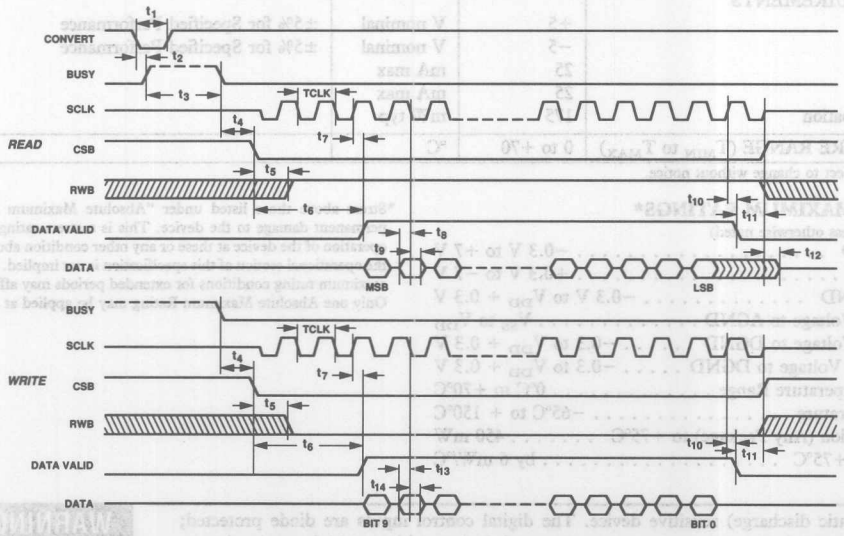
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Parameter	Limit	Units	Conditions/Comments
TIMING			
t_{CLK}	10	µs max	Clock Cycle Time 100 kHz Clock
	250	ns min	Clock Cycle Time 4 MHz Clock
t_1	t_{CLK}	ns min	ADC Start Convert Pulse Width
t_2	80	ns max	CONVERT ↓ to BUSY ↑
t_3	53* t_{CLK}	ns max	ADC Busy Period
t_4	0	ns min	BUSY ↓ to CSB ↓
t_5	2.5 t_{CLK}	ns max	CSB ↓ to RWB
t_6	2.5 t_{CLK}	ns min	CSB ↓ to DATA VALID ↑
	4.5 t_{CLK}	ns max	CSB ↓ to DATA VALID ↑
t_7	30	ns max	SCLK ↑ to DATA VALID ↑
t_8	30	ns min	Data at Output before SCLK ↓
t_9	50	ns min	Data at Output after SCLK ↓
t_{10}	30	ns max	SCLK ↑ to DATA VALID ↓
t_{11}	0	ns min	DATA VALID ↓ to CSB/RWB ↑
t_{12}	50	ns max	CSB ↑ to Data and SCLK Float (See diagram below.)
t_{13}	0	ns min	Data Setup Time before SCLK ↓
t_{14}	0.5 t_{CLK}	ns min	Data Hold Time after SCLK

*The Internal Logic is dynamic so must be continuously clocked at 100 kHz minimum.



Test Load Conditions



Timing Diagram

PRELIMINARY TECHNICAL DATA

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PIN FUNCTION DESCRIPTION

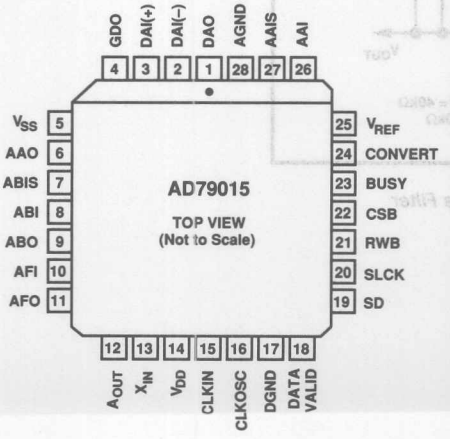
Pin	Mnemonic	Description
1	DAO	Differential Amplifier Out
2	DAI(−)	Differential Amplifier In (−)
3	DAI(+)	Differential Amplifier In (+)
4	GDO	Guard Drive Output
5	V_{SS}	Negative Supply, −5 V
6	AAO	Amplifier A Out
7	ABIS	Amplifier B In (Switched)
8	ABI	Amplifier B In
9	ABO	Amplifier B Out
10	AFI	Active Filter In (−)
11	AFO	Active Filter Out
12	A_{OUT}	Analog Out
13	X_{IN}	External ADC Input
14	V_{DD}	Positive Supply, +5 V
15	CLKIN	Clock Input Pin. An external TTL compatible clock may be applied to this pin
16	CLKOSC	Clock Oscillator Pin
17	DGND	Digital Ground
18	DATA VALID	This pin signals valid data in/out during SCLK low-high transition
19	SDO	Serial Data In/Out. This pin is in tristate when CSB is high
20	SCLK	Serial Clock Output. This pin is in tristate when CSB is high
21	RWB	Read/Write Select
22	CSB	Chip Select
23	BUSY	Converter Busy
24	CONVERT	Start Conversion
25	V_{REF}	Voltage Reference Out
26	AAI	Amplifier A In
27	AAIS	Amplifier A In (Switched)
28	AGND	Analog Ground

PRELIMINARY TECHNICAL DATA

7

PIN CONFIGURATION

PLCC



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CIRCUIT INFORMATION

SIGNAL LEVELS

For an input gain of 5, the maximum Input Signal for Full-Scale ADC Output is ±10 mV.

INTERNAL CLOCK OSCILLATOR

Figure 1 shows the AD79015 internal clock circuit. A crystal or ceramic resonator may be connected as in Figure 1 to provide a clock oscillator for the internal timing. Alternatively, the crystal/resonator may be omitted and an external CMOS-compatible clock source connected to CLKIN. The mark/space ratio of the external clock must be in the range of 45/55 and 55/45. An inverted CLKIN signal will appear at the SCLK output pin.

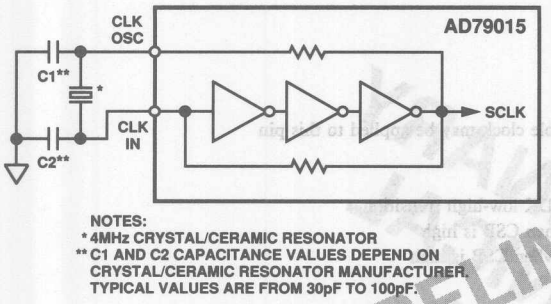


Figure 1. AD79015 Internal Clock Circuit

ACTIVE LOW-PASS FILTER

The internal active filter is implemented with a 2nd order negative feedback configuration.

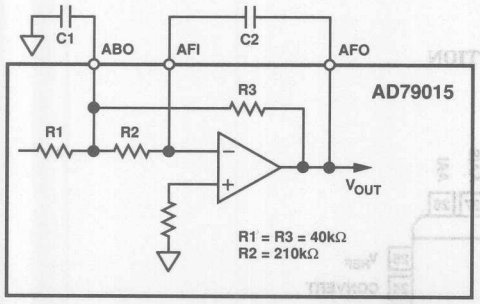


Figure 2. Low-Pass Filter

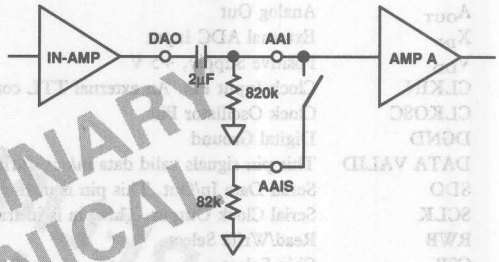
The filter cutoff frequency and filter damping factor are determined by selecting the appropriate values of C_1 and C_2. The resistor value for R1 and R3 is 40 kΩ and R2 is 210 kΩ.

$$d = \sqrt{\frac{C2}{C1}}\left[\sqrt{\frac{R2}{R3}} + \sqrt{\frac{R3}{R2}} + \sqrt{\frac{R2 \times R3}{R1}}\right] \quad gain = \frac{R3}{R1}$$

$$Bandpass\ ripple\ \frac{e_{OUT}}{e_{IN}} = -20\ log_{10}\left[\frac{d\sqrt{4-d^2}}{2}\right]$$

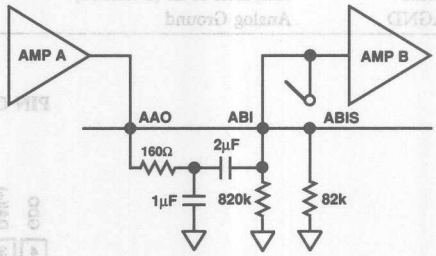
HIGH-PASS FILTER (Example Only)

This external high-pass filter can be implemented between the input gain stage and Amplifier A.



BAND PASS FILTER (Example Only)

This external band pass filter can be implemented between Amplifier A and Amplifier B.



PRELIMINARY TECHNICAL DATA

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PROGRAMMING THE AD79015

The function of the part is set by writing a ten-bit word to the control register on chip using the serial interface. The timing for the write operation is provided in the timing diagrams.

The order and function of the bits in the control register is as follows:

Bit 9	A "1" sets external input to the ADC.
Bit 8	Internal use only. Must be set to a "1."
Bit 7	Internal use only. Must be set to a "1."
Bit 3–Bit 6	A 4-bit binary code to set the gain of the programmable gain block between 0 dB and 15 dB in steps of 1 dB. "0000" is 0 dB and "1111" is 15 dB.
Bit 2	A "0" sets the gain of 3rd stage to 0 dB. A "1" sets the gain of 3rd stage to 16 dB.
Bit 1	A "1" closes the internal switches at the inputs to the 2nd and 3rd stage amplifiers.
Bit 0	Internal use only. Must be set to a "0."

Valid data available only after the first read from and write to the interface register

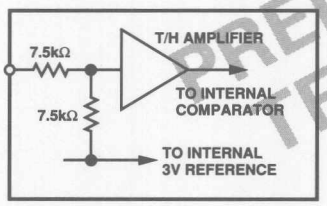


Figure 3. ADC Analog Input

ANALOG INPUT

Figure 3 shows the ADC analog input. The analog input range is 3 V into an input resistance of typically 15 kΩ. The designed code transition occurs midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS−3/2 LSBs). The output code is binary with 1 LSB = FS/4096 = 6 V/4096 = 1.46 mV. The ideal input/output transfer function is shown in Figure 4.

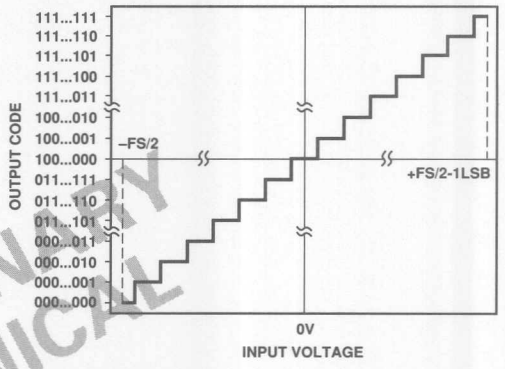


Figure 4. Bipolar Input/Output Transfer Function

PRELIMINARY TECHNICAL DATA

7

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PROGRAMMING THE AD7901/5

The function of the part is set by writing a ten-bit word to the control register on chip using the serial interface. The timing for the write operation is provided in the timing diagrams.

The order and function of the bits in the control register is as follows:

Bit 9	A "1" sets external input to the ADC.
Bit 8	Internal use only. Must be set to a "1."
Bit 7	Internal use only. Must be set to a "1."
Bit 3–Bit 6	A 4-bit binary code to set the gain of the programmable gain block between 0 dB and 15 dB in steps of 1 dB. "0000" is 0 dB and "1111" is 15 dB.
Bit 2	A "0" sets the gain of 3rd stage to 0 dB. A "1" sets the gain of 3rd stage to 15 dB.
Bit 1	A "1" closes the internal switches at the inputs to the 2nd and 3rd stage amplifiers.
Bit 0	Internal use only. Must be set to a "0."

Valid data available only after the first read from and write to the interface register

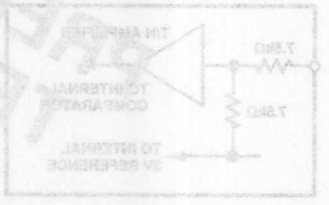


Figure 3. ADC Analog Input

ANALOG INPUT

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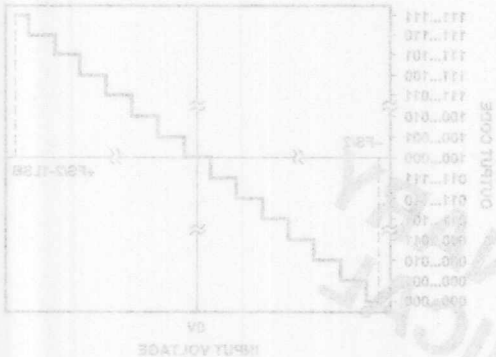


Figure 4. Bipolar Input/Output Transfer Function

PRELIMINARY TECHNICAL DATA

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20-Bit Data Acquisition System

AD79024

FEATURES

20-Bit Sigma-Delta ADC
- Dynamic Range of 105 dB (150 Hz Input)
- ±0.0015% Integral Nonlinearity (150 Hz Input)

On-Chip Low-Pass Digital Filter
- Cut-Off Programmable from 300 Hz to 18.75 Hz
- Linear Phase Response

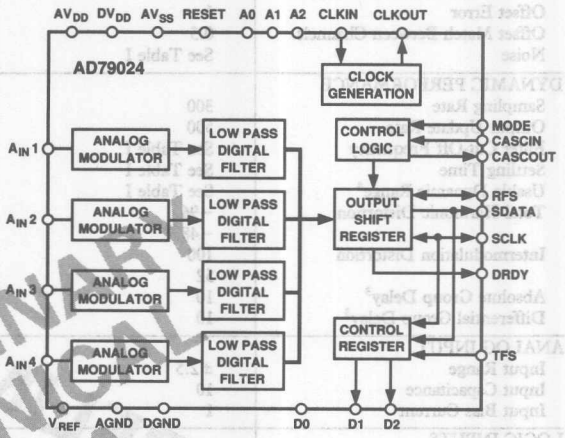
Five Line Serial I/O
Easy Interface to DSPs and Microcomputers
Software Control of Filter Cut-Off
±5 V Supply
Low Power Operation: 50 mW

APPLICATIONS

Biomedical Data Acquisition Systems
- ECG Machines
- EEG Machines

Process Control Systems
High Accuracy Measurement Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD79024 is a Signal Processing Block for Data Acquisition Systems. It is particularly suitable for biomedical applications like ECG and EEG machines. The device is capable of processing 4 channels with bandwidths of up to 300 Hz. Resolution is 20 bits, and the usable dynamic range varies from 115 dB with an input bandwidth of 18.75 Hz to 90 dB with an input bandwidth of 300 Hz.

The required system low-pass filtering is inherent in the sigma delta technique. This eliminates front-end filtering.

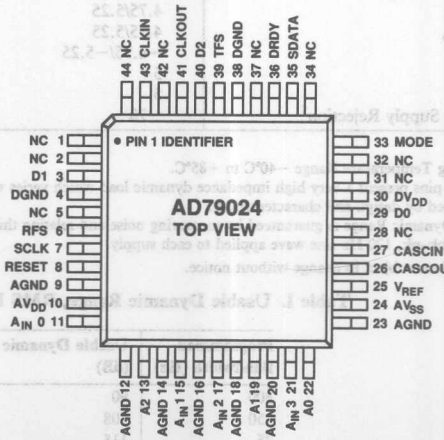
Three address pins program the device address. This allows a data acquisition system with up to 32 channels to be set up in a simple fashion. The output word from the device contains 32 bits of data. One bit is determined by the state of the D0 input and may be used with an external Pacemaker Detect Circuit to indicate that the output word is invalid because of the presence of a pacemaker pulse. There are 20 bits of data. Two bits contain the channel address, and 3 bits are the device address. Thus, each channel in a 32-channel system would have a discrete 5-bit address. The device also has a CASCOUT pin and a CASCIN pin which allow simple networking of multiple devices.

The on-chip Control Register is programmed using the SCLK, SDATA and TFS pins. Three bits of the Control Register set the Digital Filter Cut-Off Frequency for the device. Selectable frequencies are 300 Hz, 150 Hz, 75 Hz, 37.5 Hz and 18.75 Hz. A further 2 bits appear as outputs D1 and D2 and can be used for controlling calibration at the front end. The device is available in a 44-pin plastic QFP (Quad Flat Pack) package.

The AD79024 is fabricated in Analog Devices' Linear Compatible CMOS process (LC²MOS), an advanced, all ion-implanted process that combines fast CMOS logic and linear, bipolar circuits on a single chip, thus achieving excellent linear performance while still retaining low CMOS power levels.

PIN CONFIGURATION

Plastic QFP



NOTE: PIN 16–AGND IS THE PRIMARY AGND TO THE PART. SECONDARY AGND PINS ARE USED TO ISOLATE THE ANALOG INPUT PINS. NC PINS MAY BE CONNECTED TO EITHER DIGITAL SUPPLY OR LEFT UNCONNECTED.

PRELIMINARY TECHNICAL DATA

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50 Hz Sine Wave; A_{IN} Source Resistance = 750 Ω with 1 nF to AGND at each A_{IN}. I_A = I_{MIN} to I_{MAX}, unless otherwise stated.)

Parameter	Limit @ T_{MIN}, T_{MAX}	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution	20	Bits	
Integral Linearity Error	0.0015	% FSR typ	Guaranteed No Missed Codes to 20 Bits[3]
	0.003	% FSR max	
Gain Error	1	% FSR max	
Gain Match Between Channels	0.05	% FSR max	
Offset Error	1	% FSR max	
Offset Match Between Channels	0.5	% FSR max	
Noise	See Table I		
DYNAMIC PERFORMANCE			
Sampling Rate	300	kHz	
Output Update Rate	500	Hz	
Filter Cut-Off Frequency	See Table I		
Settling Time	See Table I		
Usable Dynamic Range[4]	See Table I		
Total Harmonic Distortion	−96	dB typ	
	−48	dB typ	A_{IN} = ±10 mV pk–pk
Intermodulation Distortion	100	dB typ	
	52	dB typ	A_{IN} = ±10 mV pk–pk
Absolute Group Delay[3]	10	ms max	
Differential Group Delay[3]	10	ns max	
ANALOG INPUT			
Input Range	±2.5	Volts	
Input Capacitance	10	pF typ	
Input Bias Current	1	nA typ	
LOGIC INPUTS			
V_{INH}, Input High Voltage	2.4	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	10	μA max	
C_{IN}, Input Capacitance	10	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	2.4	V min	$\|I_{OUT}\| \leq 40$ μA
V_{OL}, Output Low Voltage	0.4	V max	$\|I_{OUT}\| \leq 1.6$ mA
POWER SUPPLIES			
Reference Input	2.4/3.1	V min/V max	
AV_{DD}	4.75/5.25	V min/V max	
DV_{DD}	4.75/5.25	V min/V max	
AV_{SS}	−4.75/−5.25	V min/V max	
I_{DD}	5	mA max	
I_{SS}	5	mA max	
Power Supply Rejection[5]	−70	dB typ	

PRELIMINARY TECHNICAL DATA

NOTES
[1]Operating Temperature Range −40°C to +85°C.
[2]The A_{IN} pins present a very high impedance dynamic load which varies with clock frequency.
[3]Guaranteed by design and characterization.
[4]Usable Dynamic Range is guaranteed by measuring noise and relating this to the Full-Scale Input Range.
[5]100 mV pk–pk, 120 Hz sine wave applied to each supply.
Specifications subject to change without notice.

Table I. Usable Dynamic Range, RMS Noise and Filter Settling Time vs. Filter Bandwidth

Programmed Bandwidth (Hz)	Usable Dynamic Range (dB)	RMS Noise (μV)	Filter Settling Time to ±0.0007% FS (ms)
300	90	56	5
150	108	7	10
75	115	3	20
37.5	115	3	40
18.75	115	3	80

NOTE
Usable Dynamic Range is defined as the ratio of the rms full-scale reading (sine wave input) to the rms noise of the converter.

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Timing Characteristics[1, 2] (AV_{DD} = DV_{DD} = +5 V ± 5%; AV_{SS} = −5 V ± 5%; AGND = DGND = 0 V; f_{CLKIN} = 4 MHz; Input Levels: Logic 0 = 0 V, Logic 1 = DV_{DD}; unless otherwise stated.)

Parameter	Limit @ T_{MIN}, T_{MAX}	Units	Conditions/Comments
f_{CLKIN}[3, 4]	400	kHz min	Master Clock Frequency: Internal Gate Oscillator
	4	MHz max	
	400	kHz min	Master Clock Frequency: Externally Supplied
	4	MHz max	
t_R[5]	50	ns max	Digital Output Rise Time; Typically 20 ns
t_F[5]	50	ns max	Digital Output Fall Time; Typically 20 ns
Control Register Timing			
t_1	250	ns min	SCLK Period
t_2	77	ns min	SCLK Width
t_3	30	ns min	TFS Setup Time
t_4	20	ns min	SDATA Setup Time
t_5	10	ns min	SDATA Hold Time
t_6	20	ns min	TFS Hold Time
Master Mode Timing			
t_7	200	ns min	CASCIN Pulse Width
t_8[6]	25	ns max	CASCIN High to SCLK Valid Delay
t_9	500	ns min	SCLK Period
t_{10}	150	ns min	SCLK Width
t_{11}	25	ns max	SCLK High to RFS High Delay
t_{12}	0	ns min	RFS Hold After SCLK High
t_{13}[7]	100	ns max	SCLK High to SDATA Valid
t_{14}[8]	250	ns max	SCLK Falling Edge to Hi-Z Delay
t_{15}	25	ns max	SCLK Hi-Z to CASCOUT High Delay
t_{16}	500	ns min	CASCOUT Pulse Width
Slave Mode Timing			
t_7	200	ns min	CASCIN Pulse Width
t_{16}	500	ns min	CASCOUT Pulse Width
t_{17}	100	ns min	CASCIN High to SCLK High Setup Time
t_{18}	250	ns min	SCLK Period
t_{19}	77	ns min	SCLK Width
t_{20}	50	ns min	RFS to SCLK High Setup Time
t_{21}	10	ns min	RFS Hold Time After SCLK Low
t_{22}[7]	100	ns max	SCLK High to SDATA Valid
t_{23}[8]	250	ns max	SCLK Falling Edge to Hi-Z Delay.
t_{24}	50	ns max	SCLK Low to CASCOUT High Delay

PRELIMINARY TECHNICAL DATA

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figures 1 to 6.
[3]CLKIN Duty Cycle range is 20% to 80%.
[4]The AD79024 is production tested with f_{CLKIN} at 4 MHz. It is guaranteed by characterization to operate at 400 kHz.
[5]Specified using 10% and 90% points on waveform of interest.
[6]If DRDY is high when a rising edge occurs on CASCIN, the rising edge will not be recognized until DRDY goes low to indicate that the output register can be read.
[7]t_{13} and t_{22} are measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[8]t_{14} and t_{23} are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time quoted in the Timing Characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

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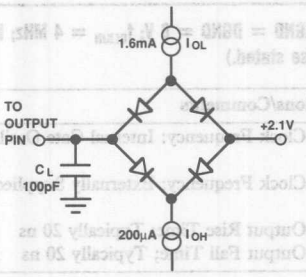


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

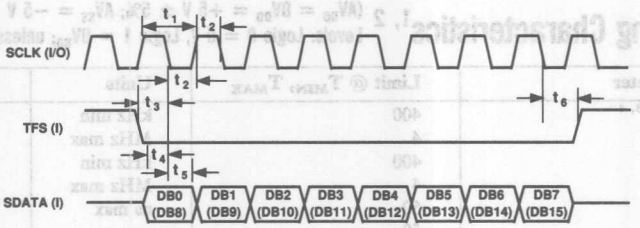
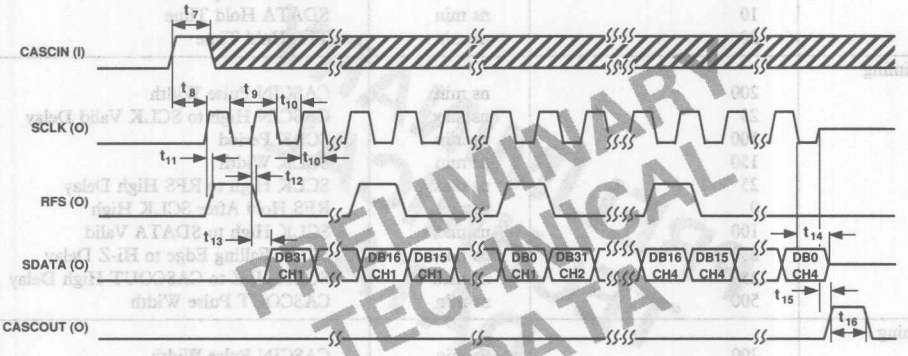


Figure 2. Control Register Timing Diagram



PRELIMINARY TECHNICAL DATA

Figure 3. Master Mode Timing Diagram

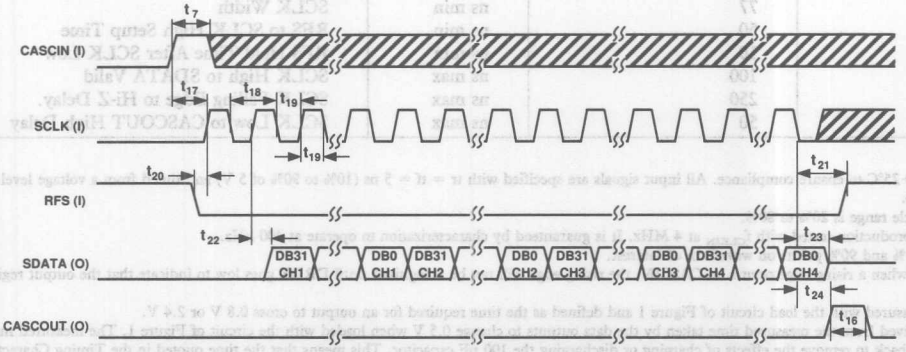


Figure 4. Slave Mode Timing Diagram

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ABSOLUTE MAXIMUM RATINGS*

AV_{DD} to AGND . . . . . −0.3 V to +7 V
AV_{SS} to AGND . . . . . +0.3 V to −7 V
AGND to DGND . . . . . −0.3 V to +0.3 V
AV_{DD} to DV_{DD} . . . . . −0.3 V to +0.3 V
Analog Inputs to AGND . . . AV_{SS} − 0.3 V to AV_{DD} + 0.3 V
V_{REF} to AGND . . . . . V_{SS} − 0.3 V to V_{DD} + 0.3 V
Digital Inputs to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
Digital Outputs to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Commercial Plastic (B Version) . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 500 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



PRELIMINARY TECHNICAL DATA

PIN DESCRIPTION

Pin	Description
AV_{DD}	Analog Positive Supply, +5 V nominal.
DV_{DD}	Digital Positive Supply, +5 V nominal.
AV_{SS}	Analog Negative Supply, −5 V nominal.
RESET	A high pulse on this pin synchronizes the sampling point on the four input channels. It can be used in a multichannel system to ensure simultaneous sampling.
A0–A2	The three address pins, A0, A1 and A2 give the device a unique address. This information is contained in the output data stream from the device.
CLKIN	Clock Input for External Clock.
CLKOUT	Clock Output which is used to generate an internal master clock by connecting a crystal between CLKOUT and CLKIN. If an external clock is used, then CLKOUT is not connected.
MODE	This digital input determines the device interface mode. If it is hardwired low then the Master Mode interface is enabled; whereas if it is high, the Slave Mode interface is enabled.
CASCIN	Positive-edge triggered digital input which is used to enable the output data stream. This input is used to cascade several devices in a multichannel system.
CASCOUT	Digital output which goes high at the end of a complete 4-channel data transfer. This can be connected to the CASCIN of the next device in a multi-channel system to ensure proper control of the data transfer.
RFS	Receive Frame Synchronization signal for the serial output data stream. This can be an input or output depending on the interface mode.
SDATA	Serial Data Input/Output pin.
SCLK	Serial Clock Input/Output. The SCLK pin is configured as an input or output, depending on the state of the Mode pin.
DRDY	Data Ready Output. DRDY is low when valid data is available in the output register. It goes high for four clock cycles when a new word is being loaded into the output register, to indicate that valid data is not available.
TFS	Transmit Frame Sync input for programming the on-chip Control Register.
D0	Digital Data Input. This is contained in the digital data stream sent from the device.
D1, D2	Digital Outputs. These two digital outputs can be programmed from the on-chip Control Register. They can be used to switch in calibration signals at the front end.
V_{REF}	Reference Input, nominally 2.5 V.
AGND	Analog Ground. Ground reference for analog circuitry.
DGND	Digital Ground. Ground return for digital circuitry.
$A_{IN}1$–$A_{IN}4$	Analog Input pins. The analog input range is ±2.5 V.

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DESCRIPTION OF OPERATION

Voltage Reference

Full scale analog input corresponds to reference voltage input.

The reference input presents exactly the same dynamic load as the analog input, but in the case of the reference input, source resistance and long settling time introduce gain errors rather than offset errors. Most precision references however have sufficiently low output impedance and wide enough bandwidth to settle to the required accuracy in the time allowed by the AD79024.

The reference should be chosen to have minimal noise in the programmed passband. Recommended references are the AD580, AD680 or the ADREF-43 from Analog Devices. These low noise references have a typical noise spectral density of 40 nV/$\sqrt{\text{Hz}}$ at 300 Hz.

Clock Generation

The device operates from a master clock which must be provided either from a crystal source or an external clock source. If a crystal is used, it must be connected across the CLKIN and CLKOUT pins. An external clock can be used by driving the CLKIN input directly with a CMOS compatible clock. In this case, CLKOUT is left unconnected. The nominal clock frequency for the device is 4.096 MHz.

Control Register Description

The 16-bit control register is programmed in two 8-bit bytes. Three control lines are used: TFS, SCLK and SDATA. SCLK can be an input or an output depending on the state of the MODE pin. When this is low, SCLK is an output (Master Mode); and when it is high, SCLK is an input (Slave Mode). When TFS goes low, data on the SDATA line is clocked into the control register on each succeeding falling edge of SCLK.

When 8 bits have been clocked in, the transfer automatically stops. Only when another negative going edge is detected on TFS will new information be written into the control register. The control register programming model is shown in Table II. Bits DB8 and DB0 allow the control register to identify whether the MS Byte or the LS Byte has been programmed. Only when DB8 is a 1 and DB0 is a 0 will the register recognize that a complete valid word has been programmed.

Control Register bit, A3, acts as an extra address bit which must always be set to 1 to enable programming of the AD79024. If it is set to 0 then the programmed word is ignored. This allows the user to bypass the AD79024 control register and use the serial stream from the DSP or microcomputer to program other serial peripheral devices.

When a valid word has been received, the device interrogates the mode bit, M0. If this is 0, then the digital filter cut-off frequencies are programmed to the appropriate value if the device address pins correspond to the A2, A1, A0 bits in the control register. If the device address pins do not correspond to the A2, A1, A0 bits, then the FC2, FC1, FC0 bits are ignored. If M0 is 1, then the digital filter cut-off frequencies are programmed to the FC2, FC1, FC0 value irrespective of the address bits. In a multichannel system this allows the user to either program all AD79024s to have the same cut-off frequency or else to give each device a separate cut-off frequency.

Control Register bits FC2, FC1, FC0 program the digital filter cut-off frequency (see Table IV).

Control Register bits D2, D1 control the digital output Pins D2 and D1. These are programmed in the same way as FC2, FC1, FC0.

PRELIMINARY TECHNICAL DATA

Table II. Control Register Programming Model

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
A3	A2	A1	A0	M0	FC2	FC1	1	FC0	D2	D1	X	X	X	X	0

Table III. M0 Truth Table

M0	Operating Mode
0	Initialization Mode 0. A2, A1, A0 determine which device is addressed and programmed with cut-off frequency and digital output.
1	Initialization Mode 1. A2, A1, A0 ignored. All devices are addressed and programmed with common cut-off frequency and digital output.

Table IV. Cut-Off Frequency Truth Table

FC2	FC1	FC0	Cut-Off Frequency (Hz)
0	0	0	300
0	0	1	150
0	1	0	75
0	1	1	37.5
1	0	0	18.75

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Reset

The AD79024 has a hardware reset which can be used to synchronize many devices. When the RESET pin goes low after being high for at least 4 CLKIN cycles, the modulator sampling points and digital filter starting points are all synchronized. This synchronizes all devices which receive the RESET pulse and gives simultaneous sampling of all channels.

Data Output Interface Modes

When the control register has been programmed, the device begins conversion. There is an initial delay of 400,000 master clock cycles to allow the digital filters to settle. These filters are $Sinc^3$ and so the filter output update rate is directly related to the programmed cut-off frequency. The ratio between these is 3.81. So, for a filter cut-off frequency of 300 Hz, the output update is 1.145 kHz. The falling edge of the DRDY output indicates that the output shift register has been updated. There are two interface modes. One is the Master Mode where the AD79024 is the master in the system and the processor to which it is communicating is the slave. The other mode is the Slave Mode where the AD79024 is the slave and the processor is the system master. In both of these modes the data output stream contains 4 × 32 bits corresponding to the four input channels. The output data format is given in Table V, and the channel address format is given in Table VI.

Master Mode Interface

In this mode, data is clocked out of the AD79024 by an internally generated serial clock and frame synchronization pulse. Two signals initiate the transfer. These are the input CASCIN* and the internally generated DRDY signal. When a rising edge is detected on CASCIN, the device checks the state of DRDY. Note, that on initial power-up or after a reset has been applied, the CASCIN input is not necessary on device 000 for the first data transfer but is required thereafter.

If DRDY is low, then the 3-state output, RFS, goes high on the next rising edge of CLKIN and stays high for two CLKIN cycles before going low again. The 3-state SCLK output is also activated on the same rising edge. As RFS goes low, DB31 is clocked out on the rising edge of SCLK. Data is transmitted in 16-bit words. For each A_{IN}, there are two 16-bit words and two RFS signals. When DB0 of $A_{IN}4$ has been clocked out, SCLK goes back into 3-state and the CASCOUT output goes high for two master clock cycles. DRDY also goes high at this point. Successive devices can be networked together by tying the CASCOUT of one device to the CASCIN on the next one.

The Master Mode interface is very suitable for loading data into a serial-to-parallel shift register or for DSPs like the ADSP-2101 which can accept a continuous stream of 16-bit words.

Slave Mode Interface

In this mode, the master processor controls the transfer of data from the signal processing block. It starts the transfer by sending a frame synchronization pulse and serial clock to the AD79024. This could be in response to an interrupt generated by the DRDY output on the AD79024. If the device has detected a rising edge on CASCIN or is device 000 on its first transfer, it starts to send out data on the next rising edge of SCLK. When all the data bits have been clocked out, the CASCOUT pin goes high for two CLKIN cycles and DRDY also goes high. If the device is still transmitting data when a new word becomes available, the old data will continue to be transmitted and the new data is lost.

The Slave Mode interface is suited to both microcomputers like the 8051 and 68HC11 and also DSPs like the TMS320C25, ADSP-2101 and 56000.

PRELIMINARY TECHNICAL DATA

7

Table V. Output Data Word Format

DB31 . . . . . DB12	DB11 DB10	DB9 DB8 DB7	DB6	DB5 . . . . . DB0
DB19 . . . . . DB0	CA1 CA0	A0 A1 A2	D0	X X
Conversion Result	Channel Address	Device Address	Pace Detect	Don't Care

Table VI. Channel Address Format

Channel	CA1	CA0
A_{IN} 1	0	0
A_{IN} 2	0	1
A_{IN} 3	1	0
A_{IN} 4	1	1

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Reset

The AD7902A has a hardware reset which can be used to synchronize many devices. When the RESET pin goes low after being high for at least 4 CLKIN cycles, the modulator sampling points and digital filter starting points are all synchronized. This synchronizes all devices which receive the RESET pulse and gives simultaneous sampling of all channels.

Data Output Interface Modes

When the control register has been programmed, the device begins conversion. There is an initial delay of 400,000 master clock cycles to allow the digital filters to settle. These filters are $Sinc^3$ and so the filter output update rate is directly related to the programmed cut-off frequency. The ratio between these is 3.81. So, for a filter cut-off frequency of 300 Hz, the output update is 1.145 kHz. The falling edge of the DRDY output indicates that the output shift register has been updated. There are two interface modes. One is the Master Mode where the AD7902A is the master in the system and the processor to which it is communicating is the slave. The other mode is the Slave Mode where the AD7902A is the slave and the processor is the system master. In both of these modes the data output stream contains 4 × 32 bits corresponding to the four input channels. The output data format is given in Table V, and the channel address format is given in Table VI.

Master Mode Interface

In this mode, data is clocked out of the AD7902A by an internally generated serial clock and framing/synchronizing pulse. Two signals initiate the transfer. These are the input CASCIN and the internally generated DRDY signal. When a rising edge is detected on CASCIN, the device checks the state of DRDY. Note, that on initial power-up or after a reset has been applied the CASCIN input is not necessary on device 000 for the first data transfer but is required thereafter.

If DRDY is low, then the 3-state output, RFS, goes high on the next rising edge of CLKIN and stays high for two CLKIN cycles before going low again. The 3-state SCLK output is also activated on the same rising edge. As RFS goes low, DB31 is clocked out on the rising edge of SCLK. Data is transmitted in 16-bit words. For each A_{DD} there are two 16-bit words and two RFS signals. When DB0 of $A_{DD}4$ has been clocked out, SCLK goes back into 3-state and the CASCOUT output goes high for two master clock cycles. DRDY also goes high at this point. Successive devices can be networked together by tying the CASCOUT of one device to the CASCIN on the next one.

The Master Mode interface is very suitable for loading data into a serial-to-parallel shift register or for DSPs like the ADSP-2101 which can accept a continuous stream of 16-bit words.

Slave Mode Interface

In this mode, the master processor controls the transfer of data from the signal processing block. It starts the transfer by sending a framing synchronization pulse and serial clock to the AD7902A. This could be in response to an interrupt generated by the DRDY output on the AD7902A. If the device has detected a rising edge on CASCIN or it is device 000 on its first transfer, it sets its second out data on the next rising edge of SCLK. When all the data bits have been clocked out, the CASCOUT pin goes high for two CLKIN cycles and DRDY also goes high. If the device is still transmitting data when a new word becomes available, the old data will continue to be transmitted and the new data is lost.

The Slave Mode interface is suited to both microcomputers like the 8051 and 68HC11 and also DSPs like the TMS320C25, ADSP-2101 and 56000.

Table V. Output Data Word Format

DB31 . . . . . DB12	DB11 DB10	DB9 DB8 DB7	DB6	DB5 . . . . . DB0
DB19 . . . . . DB0	CA1 CA0	A0 A1 A2	D0	X X
Conversion Result	Channel Address	Device Address	Free Direct	Don't Care

Table VI. Channel Address Format

Channel	CA1	CA0
$A_{DD}1$	0	0
$A_{DD}2$	0	1
$A_{DD}3$	1	0
$A_{DD}4$	1	1

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14-Bit & 15-Bit Sampling Analog-to-Digital Converters

DAS1152/DAS1153

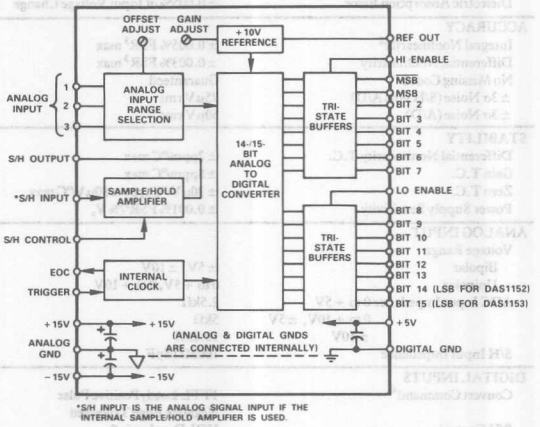
FEATURES

- Complete with High Accuracy Sample/Hold and A/D Converter
- Differential Nonlinearity: ±0.002% FSR max (DAS1153)
- Nonlinearity: DAS1152: ±0.005% FSR max
  DAS1153: ±0.003% FSR max
- Low Differential Nonlinearity T.C.: ±2ppm/°C max
- High Throughput Rate: 25kHz min (DAS1152)
- High Feedthrough Rejection: −96dB
- Byte-Selectable Tri-State Buffered Outputs
- Internal Gain & Offset Potentiometers
- Improved Second Source to A/D/A/M 824 and A/D/A/M 825 Modules

APPLICATIONS

- Process Control Data Acquisition
- Automated Test Equipment
- Seismic Data Acquisition
- Nuclear Instrumentation
- Medical Instrumentation
- Robotics

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The DAS1152/DAS1153 are 14-/15-bit sampling analog-to-digital converters having a maximum throughput rate of 25kHz/20kHz. They provide high accuracy, high stability, and functional completeness all in a 2″ × 4″ × 0.44″ metal case.

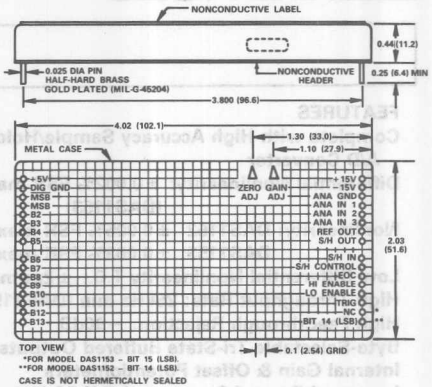
Guaranteed high accuracy system performance such as nonlinearity of ±0.005% FSR (DAS1152)/±0.003% FSR (DAS1153) and differential nonlinearity of ±0.003% FSR (DAS1152)/±0.002% FSR (DAS1153) are provided. Guaranteed stability such as differential nonlinearity T.C. of ±2ppm/°C (DAS1153) maximum, zero T.C. of ±80μV/°C maximum, gain T. C. of ±8ppm/°C maximum and power supply sensitivity of ±0.001% FSR/% V_S are also provided by the DAS1152/DAS1153.

The DAS1152/DAS1153 make extensive use of both integrated circuit and thin film components to obtain their excellent performance, small size, and low cost. The devices contain a precision sample/hold amplifier, high accuracy 14-/15-bit analog-to-digital converter, tri-state output buffers, internal gain and offset trim potentiometers, and power supply bypass capacitors (as shown in Figure 1).

Four analog input voltage ranges are selectable via user pin programming: 0 to +5V, 0 to +10V, ±5V, and ±10V. Unipolar coding is provided in true binary format with bipolar coding displayed in offset binary and two's complement. Tri-state buffers provide easy interface to bus structured applications.

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DYNAMIC PERFORMANCE		
Throughput Rate	25kHz min	20kHz min
Conversion Time	35µs max	44µs max
S/H Acquisition Time	4µs max	5µs max
S/H Aperture Delay	50ns	*
S/H Aperture Uncertainty	1ns	*
Feedthrough Rejection[1]	−96dB	*
Droop Rate	0.05µV/µs (0.1µV/µs max)	*
Dielectric Absorption Error	±0.005% of Input Voltage Change	*
ACCURACY		
Integral Nonlinearity[2]	±0.005% FSR[3] max	±0.003% FSR[3] max
Differential Nonlinearity	±0.003% FSR[3] max	±0.002% FSR[3] max
No Missing Codes	Guaranteed	*
±3σ Noise (S/H plus A/D)	75µV rms	*
±3σ Noise (A/D)	50µV rms	*
STABILITY		
Differential Nonlinearity T.C.	±2ppm/°C max	*
Gain T.C.	±8ppm/°C max	*
Zero T.C.	±30µV/°C typ, ±80µV/°C max	*
Power Supply Sensitivity	±0.001% FSR[3]/% V_s	*
ANALOG INPUT		
Voltage Range		
Bipolar	±5V, ±10V	*
Unipolar	0 to +5V, 0 to +10V	*
ADC Input Impedance 0 to +5V	2.5kΩ	*
0 to +10V, ±5V	5kΩ	*
±10V	10.0kΩ	*
S/H Input Impedance	100MΩ|5pF	*
DIGITAL INPUTS		
Convert Command[4]	1TTL Load, Positive Pulse	*
	Negative Edge Triggered	*
S/H Control	HOLD = Logic 0	*
	SAMPLE = Logic 1	*
Low Enable, High Enable	ENABLE = Logic 0	*
DIGITAL OUTPUTS		
Parallel Data Outputs		
Unipolar	Binary	*
Bipolar	Offset Binary, 2's Complement	*
Output Drive	2TTL Loads	*
Status	Logic "1" During Conversion	*
Output Drive	2TTL Loads	*
INTERNAL REFERENCE VOLTAGE	+10V, ±0.3%	*
External Load Current (Rated Performance)	2mA max	*
Temperature Stability	±5ppm/°C max	*
POWER REQUIREMENTS		
Rated Voltages	±15V (±3%), +5V (±5%)	*
Operating Voltages[5]	±12V to +17V, +4.75V to +5.25V	*
Supply Current Drain ±15V	±37mA	*
+5V	80mA	*
TEMPERATURE RANGE		
Specified	0 to +70°C	*
Operating	−25°C to +85°C	*
Storage	−25°C to +85°C	*
Relative Humidity	Meets MIL-STD-202E, Method 103B	*
Shielding	Electrostatic (RFI) 6 Sides,	*
	Electromagnetic (EMI) 5 Sides	*
SIZE	2" × 4" × 0.44" Metal Package	*



*FOR MODEL DAS1153 – BIT 15 (LSB).
**FOR MODEL DAS1152 – BIT 14 (LSB).
CASE IS NOT HERMETICALLY SEALED

NOTES
*Specifications same as DAS1152
[1]Measured in hold mode, input 20V pk-pk @ 10kHz.
[2]Worst-case summation of S/H and A/D nonlinearity errors.
[3]FSR means Full Scale Range.
[4]When connecting the Convert Command and the S/H control terminals together, the pulse width must be long enough for the S/H amplifier to acquire the input signal to the required accuracy 4µs (max, DAS1152)/5µs (max, DAS1153). If the A/D converter is only used, the Convert Command pulse width should be 100ns min (see Figure 2).
[5]If only the ADC portion is used, the operating power supply voltage can be maintained at ±12V to ±17V. But if the S/H section is required, the operating voltage must be maintained at ±15V (±3%) or the S/H input voltage must be limited to −7V to +10V for a ±12V supply voltage.
[6]Recommended Power Supply: Analog Devices Model 923.
Specifications subject to change without notice.

ASSEMBLY INSTRUCTIONS

CAUTION: This module is not an embedded assembly and is not hermetically sealed. Do not subject to a solvent or water-wash process that would allow direct contact with free liquids or vapors. Entrapment of contaminants may occur, causing performance degradation and permanent damage. Install after any clean/wash process and then only spot clean by hand.

The DAS1152/DAS1153 are functionally complete data acquisition subsystems being fully characterized as such. All the necessary data acquisition and microprocessor interface elements are provided internal to these devices. Accuracy and performance criteria are tested and specified for the entire system. Thus, design time and associated high accuracy problems are minimized because layout and component optimization have already been performed.

For operation, the only connections necessary to the DAS1152/DAS1153 are the ±15V and +5V power supplies, analog input signal, trigger pulse, and the HI-ENABLE/LO-ENABLE tri-state controls. Analog input and digital output programming are user selectable via external jumper connections.

ANALOG INPUT SECTION

The analog input can be applied to just the A/D converter or to the internal sample/hold amplifier ahead of the A/D converter. When using just the A/D converter, apply the analog input per the voltage range pin programming shown in Table I. When using the sample/hold amplifier in conjunction with A/D converter, apply the analog input to the S/H INPUT terminal and connect the S/H OUTPUT terminal to the appropriate A/D converter analog input.

Table I. Analog Input Pin Programming

Analog Voltage Input Range	Connect V_{IN} or S/H Out To	Connect Analog Common To	Connect Ref Out To
0 to +5V	ANA IN 1, ANA IN 2, ANA IN 3	Ground	NC*
0 to +10V	ANA IN 2 ANA IN 3	Ground ANA IN 1	NC*
±5V	ANA IN 1	Ground, ANA IN 3	ANA IN 2
±10V	ANA IN 3	Ground, ANA IN 1	ANA IN 2

*No Connection

Errors due to source loading are eliminated since the sample/hold amplifier is a high-impedance unity-gain amplifier. High feedthrough rejection is provided for either single-channel or multichannel applications. Feedthrough rejection can be optimized, in multichannel applications, by changing channels at the rising or falling edge of the S/H control pulse.

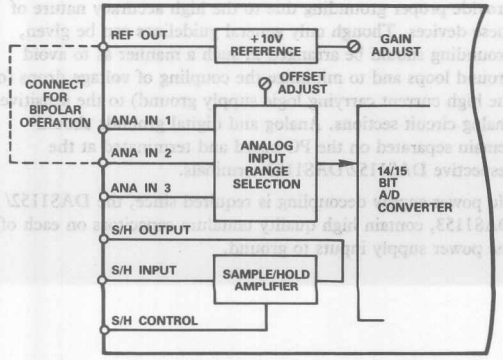


Figure 2. Analog Input Block Diagram

The timing diagram for the DAS1152/DAS1153 is illustrated in Figure 3. This figure also includes the sample/hold amplifier acquisition time.

If the sample/hold amplifier is required, the TRIGGER input and S/H CONTROL terminal can be tied together providing only one conversion control signal. When the trigger pulse goes high, it places the sample/hold amplifier in the sample mode allowing it to acquire the present input signal. The trigger pulse must remain high for a minimum of 4μs (DAS1152)/5μs (DAS1153) to insure accuracy is attained. If the sample/hold amplifier is not used, the trigger pulse needs to be only 100ns (min) in length to satisfy the A/D converter trigger requirements. At the falling edge of the trigger pulse, the sample/hold amplifier is placed in the hold mode, the A/D conversion begins, and all internal logic is reset. Once the conversion process is initiated, it cannot be retriggered until after the end of conversion.

With this negative edge of the trigger pulse the MSB is set low with the remaining digital outputs set to logic high state, and the status line is set high and remains high through the full conversion cycle. During conversion each bit, starting with the MSB, is sequentially switched low at the rising edge of the internal clock. The DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 14-/15-bit conversion taking 35μs/44μs maximum for the DAS1152/DAS1153 respectively. At this time, the STATUS line goes low signifying that the conversion is complete. For microprocessor bus applications, the digital output can now be applied to the data bus by enabling the tri-state buffers. For maximum data throughput, the digital output data should be read while the sample/hold amplifier is acquiring the new analog input signal.

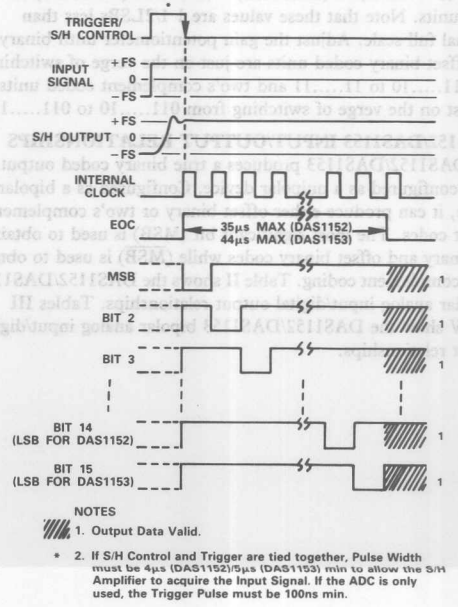


Figure 3. DAS1152/DAS1153 Timing Diagram

GAIN AND OFFSET ADJUSTMENT

The DAS1152/DAS1153 contain internal gain and offset adjustment potentiometers. Each potentiometer has ample adjustment range so that gain and offset errors can be trimmed to zero.

Since offset calibration is not affected by changes in gain calibration, it should be performed prior to gain calibration. Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable and be capable of being set to within ±1/10LSB of the desired value at any point within its range.

OFFSET CALIBRATION

For a 0 to +10V unipolar range set the input voltage precisely to +305μV for the DAS1152 and +153μV for the DAS1153. For a 0 to +5V unipolar range set the input to +153μV for the DAS1152 and +76μV for the DAS1153. Then adjust the zero potentiometer until the converter is just on the verge of switching from 000.....000 to 000.....001.

For the ±5V bipolar range set the input voltage precisely to +305μV for the DAS1152 and +153μV for the DAS1153. For a ±10V bipolar range set the input voltage precisely to +610μV for the DAS1152 and +305μV for the DAS1153. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 000.....000 to 000.....001 and the two's complement coded units are just on the verge of switching from 100.....000 to 100.....001.

GAIN CALIBRATION

Set the input voltage precisely to +9.99909V (DAS1152)/ +9.99954V (DAS1153) for the 0 to +10V units, +4.99954V (DAS1152)/+4.99977V (DAS1153) for 0 to +5V units, +9.99817V (DAS1152)/+9.99909V (DAS1153) for ±10V units, or +4.99909V (DAS1152)/+4.99954V (DAS1153) for ±5V units. Note that these values are 1 1/2LSBs less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11.....10 to 11.....11 and two's complement coded units are just on the verge of switching from 011.....10 to 011.....11.

DAS1152/DAS1153 INPUT/OUTPUT RELATIONSHIPS

The DAS1152/DAS1153 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two's complement output codes. The most significant bit (MSB) is used to obtain the binary and offset binary codes while ($\overline{\text{MSB}}$) is used to obtain two's complement coding. Table II shows the DAS1152/DAS1153 unipolar analog input/digital output relationships. Tables III and IV show the DAS1152/DAS1153 bipolar analog input/digital output relationships.

NOMINAL BIPOLAR INPUT-OUTPUT RELATIONSHIPS

Table II. Unipolar Input/Output Relationships

ANALOG INPUT			
0 to +5V Range		0 to +10V Range	
DAS1152	DAS1153	DAS1152	DAS1153
+4.99969V	+4.99984V	+9.99939V	+9.99969V
+2.50000V	+2.50000V	+5.0000V	+5.00000V
+0.62500V	+0.62500V	+1.25000V	+1.25000V
+0.0003V	+0.00015V	+0.0006V	+0.0003V
+0.0000V	+0.0000V	+0.0000V	+0.0000V

DIGITAL OUTPUT	
Binary Code	
DAS1152	DAS1153
11 111 111 111 111	111 111 111 111 111
10 000 000 000 000	100 000 000 000 000
00 100 000 000 000	001 000 000 000 000
00 000 000 000 001	000 000 000 000 001
00 000 000 000 000	000 000 000 000 000

Table III. DAS1152 Bipolar Input/Output Relationships

Analog Input		Digital Output	
±5V Range	±10V Range	Offset Binary Code	Two's Complement Code
+4.99939V	+9.99878V	11 111 111 111 111	01 111 111 111 111
+2.50000V	+5.0000V	11 000 000 000 000	01 000 000 000 000
+0.00061V	+0.00122V	10 000 000 000 001	00 000 000 000 001
+0.00000V	+0.00000V	10 000 000 000 000	00 000 000 000 000
−5.00000V	−10.00000V	00 000 000 000 000	10 000 000 000 000

Table IV. DAS1153 Bipolar Input/Output Relationships

Analog Input		Digital Output	
±5V Range	±10V Range	Offset Binary Code	Two's Complement Code
+4.99969V	+9.99939V	111 111 111 111 111	011 111 111 111 111
+2.50000V	+5.0000V	110 000 000 000 000	010 000 000 000 000
+0.0003V	+0.00061V	100 000 000 000 001	000 000 000 000 001
+0.00000V	+0.00000V	100 000 000 000 000	000 000 000 000 000
−5.00000V	−10.00000V	000 000 000 000 000	100 000 000 000 000

TRI-STATE DIGITAL OUTPUT

The ADC digital outputs are provided in parallel format to the output tri-state buffers. The output information can be applied to a data bus in either a one-byte or a two-byte format by using the HIGH BYTE ENABLE and LOW BYTE ENABLE terminals. If the tri-state feature is not required, normal digital outputs can be obtained by connecting the enable pins to ground.

POWER SUPPLY AND GROUNDING CONNECTIONS

Although the analog power ground and the digital ground are connected in the DAS1152/DAS1153, care must still be taken to provide proper grounding due to the high accuracy nature of these devices. Though only general guidelines can be given, grounding should be arranged in such a manner as to avoid ground loops and to minimize the coupling of voltage drops (on the high current carrying logic supply ground) to the sensitive analog circuit sections. Analog and digital grounds should remain separated on the PC board and terminated at the respective DAS1152/DAS1153 terminals.

No power supply decoupling is required since, the DAS1152/ DAS1153, contain high quality tantalum capacitors on each of the power supply inputs to ground.

Low Power 14-Bit, 15 Bit & 16-Bit Sampling Analog-to-Digital Converters

DAS1157/DAS1158/DAS1159

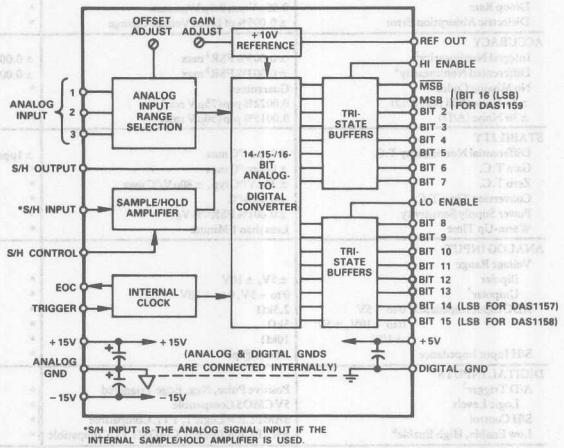
FEATURES

- Complete with High Accuracy Sample/Hold and A/D Converter
- Low Power Consumption: 650mW max, $V_S = \pm 15V$
- Rated Performance: −25°C to +85°C
- Low Nonlinearity (DAS1158 and DAS1159)
  - Differential: ±0.0015% FSR max
  - Integral: ±0.003% FSR max
  - Differential T.C.: ±1ppm/°C max
- High Throughput Rate: 18kHz min
- Byte-Selectable Tri-State Buffered Outputs
- Internal Gain & Offset Potentiometers
- Improved Second Source to A/D/A/M-834 and A/D/A/M-835 Modules

APPLICATIONS

- Seismic Data Acquisition
- Portable Field Instrumentation
- Automated Test Equipment
- Process Control Data Acquisition
- Medical Instrumentation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The DAS1157/DAS1158/DAS1159 are 14-/15-/16-bit sampling analog-to-digital converters. They are ideally suited for use in portable and remote data acquisition equipment where low power consumption (650mW maximum) and wide temperature range (−25°C to +85°C rated performance) are required.

DAS1157/DAS1158/DAS1159 provide guaranteed high accuracy and high stability system performance essential to medical, analytical and process control equipment: differential nonlinearity of ±0.0015% max and integral nonlinearity of ±0.003% max (DAS1158 and DAS1159); no missing codes guaranteed; gain T.C. of ±8ppm/°C max, zero T.C. of ±80μV/°C max and differential nonlinearity T.C. of ±1ppm/°C max.

The wide dynamic range will enhance the performance of critical measurements in gas and liquid chromatography, blood analyzers, distributed data acquisition in factory automation and power generating equipment, and in automatic test equipment.

The DAS1157/DAS1158/DAS1159 make use of Analog Devices' proprietary CMOS technology to achieve low power operation, while utilizing the latest integrated circuit and thin-film components to achieve the highest level of performance and reliability.

As shown in Figure 1, each device contains a precision sample/hold amplifier, high accuracy 14-/15-/16-bit analog-to-digital converter, precision reference, CMOS tri-state output buffers (for direct 8-bit or 16-bit bus interface), user accessible gain and offset adjust potentiometers, and power supply bypass capacitors, all in a compact low profile 2″×4″×0.375″ metal case package. No additional components are required for operation.

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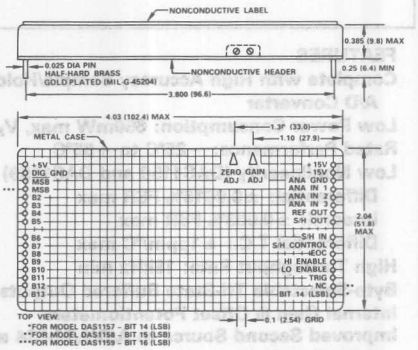
DAS1157/DAS1158/DAS1159—SPECIFICATIONS

(typical @ +25°C, V_S = ±15V, V_D = +5V unless otherwise specified)

MODEL	DAS1157	DAS1158	DAS1159
RESOLUTION	14 Bits	15 Bits	16 Bits
DYNAMIC PERFORMANCE			
Throughput Rate	18kHz min	*	*
Conversion Time	50µs max	*	*
S/H Acquisition Time	5µs max	*	*
S/H Aperture Delay	250ns	*	*
S/H Aperture Uncertainty	1ns	*	*
Feedthrough Rejection[1]	−90dB min	*	*
Droop Rate	0.05µV/µs, 0.1µV/µs max	*	*
Dielectric Absorption Error	±0.005% of Input Voltage Change	*	*
ACCURACY			
Integral Nonlinearity[2]	±0.005% FSR[3] max	±0.003% FSR[3] max	**
Differential Nonlinearity[4]	±0.003% FSR[3] max	±0.0015% FSR[3] max	**
No Missing Codes	Guaranteed	*	*
±3σ Noise (S/H plus A/D)	0.0022% p-p (75µV rms)	*	*
±3σ Noise (A/D)	0.0015% p-p (50µV rms)	*	*
STABILITY			
Differential Nonlinearity T.C.	±2ppm/°C max	±1ppm/°C max	**
Gain T.C.	±8ppm/°C max	*	*
Zero T.C.	±30µV/°C typ, ±80µV/°C max	*	*
Conversion Time T.C.	±0.05%/°C	*	*
Power Supply Sensitivity	±0.001% FSR[3]/% V_S	*	*
Warm-Up Time	Less than 1 Minute	*	*
ANALOG INPUT			
Voltage Range			
Bipolar	±5V, ±10V	*	*
Unipolar[4]	0 to +5V, 0 to +10V	*	*
ADC Input Impedance 0 to +5V	2.5kΩ	*	*
0 to +10V, ±5V	5kΩ	*	*
±10V	10kΩ	*	*
S/H Input Impedance	100MΩ‖5pF	*	*
DIGITAL INPUTS			
A/D Trigger[5]	Positive Pulse, Neg. Edge Triggered	*	*
Logic Levels	5V CMOS Compatible	*	*
S/H Control	SAMPLE = Logic 1, TTL Compatible	*	*
Low Enable, High Enable[6]	ENABLE = Logic 0, CMOS/TTL Compatible	*	*
DIGITAL OUTPUTS			
Parallel Data Outputs			
Unipolar	Binary	*	See Note 7
Bipolar	Offset Binary, 2's Complement	*	See Note 7
Output Drive	2TTL Loads	*	*
End of Conversion	Logic "1" During Conversion	*	*
Output Drive	2TTL Loads	*	*
INTERNAL REFERENCE VOLTAGE	+10V, ±0.3%	*	*
External Load Current (Rated Performance)	2mA max	*	*
POWER REQUIREMENTS			
Rated Voltages	±15V (±3%), +5V (±5%)	*	*
Operating Voltages[8,9]	±12V to ±17V, +4.75V to +5.25V	*	*
Supply Current Drain ±15V	±15mA	*	*
+5V	10mA	*	*
Total Power Consumption, V_S = ±15V	500mW typ, 650mW max	*	*
TEMPERATURE RANGE			
Rated Performance	−25°C to +85°C	*	*
Operating	−25°C to +85°C	*	*
Storage	−40°C to +100°C	*	*
Relative Humidity	Meets MIL-STD-202E, Method 103B	*	*
Shielding	Electrostatic (RFI) 6 Sides	*	*
	Electromagnetic (EMI) 5 Sides	*	*
SIZE	2" × 4" × 0.375" Metal Package	*	*

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



ASSEMBLY INSTRUCTIONS

CAUTION: This module is not an embedded assembly and is not hermetically sealed. Do not subject to a solvent or water-wash process that would allow direct contact with free liquids or vapors. Entrapment of contaminants may occur, causing performance degradation and permanent damage. Install after any clean/wash process and then only spot clean by hand.

NOTES

*Specifications same as DAS1157

**Specifications same as DAS1158

[1]Measured in hold mode, input 20V pk-pk @ 10kHz.

[2]Worst-case summation of S/H and A/D nonlinearity errors.

[3]FSR means Full Scale Range.

[4]Differential Nonlinearity in the 0 to +5V input range is specified as ±0.003% typical for the DAS1157, DAS1158 and DAS1159.

[5]When connecting the Trigger and the S/H control terminals together, the pulse width must be long enough for the S/H amplifier to acquire the input signal to the required accuracy (5µs min). If the A/D converter only is used, the Trigger pulse width should be 1µs min (see Figure 3).

[6]Low Byte Enable pin connections are Bits 8 through 15; High Byte Enable pin connections are $\overline{\text{MSB}}$, MSB or Bit 16 and Bits 2 through 7.

[7]DAS1159 unipolar coding is provided in a modified binary format (MSB complement) while bipolar coding is two's complement only. The MSB must be inverted for binary and offset binary codes.

[8]When the S/H section is required, $-V_S$ must be at least 5 volts more negative than the most negative analog input voltage (example: V_S = ±12V dc, therefore, maximum analog input is +10 and −7V).

[9]Recommended Power Supply: Analog Devices Model 923.

Specifications subject to change without notice.

OPERATION

For operation, the only connections necessary to the DAS1157/DAS1158/DAS1159 are the ±15V and +5V power supplies, analog input signal, trigger pulse, and the HI-ENABLE/LO-ENABLE tri-state controls. Analog input and digital output programming are user selectable via external jumper connections.

Input voltage ranges are selectable via user pin programming: 0 to +5V, 0 to +10V, ±5V and ±10V. Unipolar coding is provided in true binary format with bipolar coding displayed in offset binary and two's complement (DAS1157 and DAS1158). DAS1159 unipolar coding is provided in a modified binary format (MSB complement) while bipolar coding is two's complement only.

ANALOG INPUT SECTION

The analog input can be applied to just the A/D converter or to the internal sample/hold amplifier ahead of the A/D converter. When using just the A/D converter, apply the analog input per the voltage range pin programming shown in Table I. When using the sample/hold amplifier in conjunction with A/D converter, apply the analog input to the S/H INPUT terminal and connect the S/H OUTPUT terminal to the appropriate A/D converter analog input.

Analog Voltage Input Range	Connect V_{IN} or S/H Out To	Connect Analog Common To	Connect Ref Out To
0 to +5V	ANA IN 1, ANA IN 2, ANA IN 3	Ground	NC*
0 to +10V	ANA IN 2 ANA IN 3	Ground ANA IN 1	NC*
±5V	ANA IN 1	Ground, ANA IN 3	ANA IN 2
±10V	ANA IN 3	Ground, ANA IN 1	ANA IN 2

*No Connection

Table I. Analog Input Pin Programming

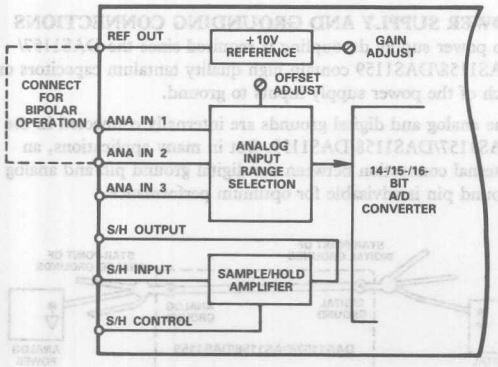


Figure 2. Analog Input Block Diagram

Errors due to source loading are eliminated since the sample/hold amplifier is a high-impedance unity-gain amplifier. High feedthrough rejection is provided for either single-channel or multichannel applications. Feedthrough rejection can be optimized, in multichannel applications, by changing channels at the rising or falling edge of the S/H control pulse.

TIMING DIAGRAM

The timing diagram for the DAS1157/DAS1158/DAS1159 is illustrated in Figure 3. This figure also includes the sample/hold amplifier acquisition time.

If the sample/hold amplifier is required, the TRIGGER input and S/H CONTROL terminal can be tied together providing only one conversion control signal. When the trigger pulse goes high, it places the sample/hold amplifier in the sample mode allowing it to acquire the present input signal. The trigger pulse must remain high for a minimum of 5μs to insure accuracy. If the sample/hold amplifier is not used, the trigger pulse needs to be 1μs (minimum) in length to satisfy the A/D converter trigger requirements. At the falling edge of the trigger pulse, the sample/hold amplifier is placed in the hold mode, all internal logic is reset and the A/D conversion begins. The conversion process can be retriggered at any time, including during conversion.

With this negative edge of the trigger pulse, the MSB is set high with the remaining digital outputs set to logic low state, and the end of conversion is set high and remains high through the full conversion cycle. During conversion each bit, starting with the MSB, is sequentially switched high at the rising edge of the internal clock. The DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 14-/15-/16-bit conversion taking 50μs maximum. At this time, the end of conversion line goes low signifying that the conversion is complete. For microprocessor bus applications, the digital output can now be applied to the data bus by enabling the tri-state buffers. For maximum data throughput, the digital output data should be read while the sample/hold amplifier is acquiring the new analog input signal.

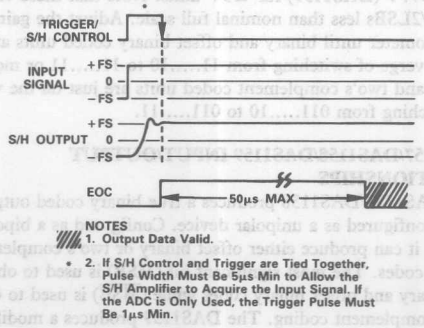


Figure 3. DAS1157/DAS1158/DAS1159 Timing Diagram

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The DAS1157/DAS1158/DAS1159 contain internal gain and offset adjustment potentiometers. Each potentiometer has ample adjustment range so that gain and offset errors can be trimmed to zero.

Offset calibration is not affected by changes in gain calibration, and should be performed prior to gain calibration. Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable and be capable of being set to within ±1/10LSB of the desired value at any point within its range.

OFFSET CALIBRATION

For a 0 to +10V unipolar range, set the input voltage precisely to +305μV for the DAS1157, +153μV for the DAS1158 and +76μV for the DAS1159. For a 0 to +5V unipolar range, set the input to +153μV for the DAS1157, +76μV for the DAS1158 and +38μV for the DAS1159. Then adjust the zero potentiometer until the converter is just on the verge of switching from 000.....000 to 000.....001 (DAS1157/DAS1158) or from 100.....000 to 100.....001 (DAS1159).

For the ±5V bipolar range, set the input voltage precisely to +305μV for the DAS1157, +153μV for the DAS1158 and +76μV for the DAS1159. For a ±10V bipolar range, set the input voltage precisely to +610μV for the DAS1157, +305μV for the DAS1158 and +153μV for the DAS1159. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 000.....000 to 000.....001 and the two's complement coded units are just on the verge of switching from 100.....000 to 100.....001.

GAIN CALIBRATION

Set the input voltage precisely to +9.99909V (DAS1157)/ +9.99954V (DAS1158)/+9.99977V (DAS1159) for the 0 to +10V units, +4.99954V (DAS1157)/+4.99977V (DAS1158)/ +4.99989V (DAS1159) for 0 to +5V units, +9.99817V (DAS1157)/+9.99909V (DAS1158)/+9.99954V (DAS1159) for ±10V units, or +4.99909V (DAS1157)/+4.99954V (DAS1158)/ +4.99977V (DAS1159) for ±5V units. Note that these values are 1 1/2LSBs less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11.....10 to 11.....11 or modified binary and two's complement coded units are just on the verge of switching from 011.....10 to 011.....11.

DAS1157/DAS1158/DAS1159 INPUT/OUTPUT RELATIONSHIPS

The DAS1157/DAS1158 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two's complement output codes. The most significant bit (MSB) is used to obtain the binary and offset binary codes while ($\overline{\text{MSB}}$) is used to obtain two's complement coding. The DAS1159 produces a modified binary coded output when configured as a unipolar device. Configured as a bipolar device it can only produce two's complement output codes. The DAS1159 uses $\overline{\text{MSB}}$ to obtain the modified binary and two's complement output codes; the DAS1159 does not have an MSB output. Table II shows the DAS1157/ DAS1158/DAS1159 unipolar analog input/digital output relationships. Table III shows the DAS1157/DAS1158/DAS1159 bipolar analog input/digital output relationships.

Unipolar Input Voltages

Analog Input		Digital Output
0 to +5V Range	0 to +10V Range	
DAS1157		Binary Code
+4.99969V	+9.99939V	11 1111 1111 1111
+0.00000V	+0.00000V	00 0000 0000 0000
DAS1158		Binary Code
+4.99985V	+9.99969V	111 1111 1111 1111
+0.00000V	+0.00000V	000 0000 0000 0000
DAS1159		Modified Binary Code
+4.99992V	+9.99985V	0111 1111 1111 1111
+0.00000V	+0.00000V	1000 0000 0000 0000

Table II. Unipolar Input-Output Relationships

Bipolar Input Voltages

Analog Input		Digital Output	
±5V Range	±10V Range	Offset Binary Code	Two's Complement Code
DAS1157			
+4.99939V	+9.99878V	11 1111 1111 1111	01 1111 1111 1111
+0.00000V	+0.00000V	10 0000 0000 0000	00 0000 0000 0000
−5.00000V	−10.00000V	00 0000 0000 0000	10 0000 0000 0000
DAS1158			
+4.99969V	+9.99939V	111 1111 1111 1111	011 1111 1111 1111
+0.00000V	+0.00000V	100 0000 0000 0000	000 0000 0000 0000
−5.00000V	−10.00000V	000 0000 0000 0000	100 0000 0000 0000
DAS1159			
+4.99985V	+9.99969V		0111 1111 1111 1111
+0.00000V	+0.00000V		0000 0000 0000 0000
−5.00000V	−10.00000V		1000 0000 0000 0000

Table III. Bipolar Input-Output Relationships

TRI-STATE DIGITAL OUTPUT

The ADC digital outputs are provided in parallel format to the output tri-state buffers. The output information can be applied to a data bus in either a one-byte or a two-byte format by using the HIGH BYTE ENABLE and LOW BYTE ENABLE terminals. If the tri-state feature is not required, normal digital outputs can be obtained by connecting the enable pins to ground.

POWER SUPPLY AND GROUNDING CONNECTIONS

No power supply decoupling is required since the DAS1157/ DAS1158/DAS1159 contain high quality tantalum capacitors on each of the power supply inputs to ground.

The analog and digital grounds are internally connected in the DAS1157/DAS1158/DAS1159. But in many applications, an external connection between the digital ground pin and analog ground pin is advisable for optimum performance.

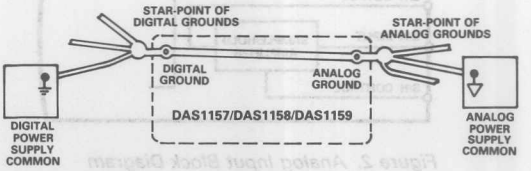
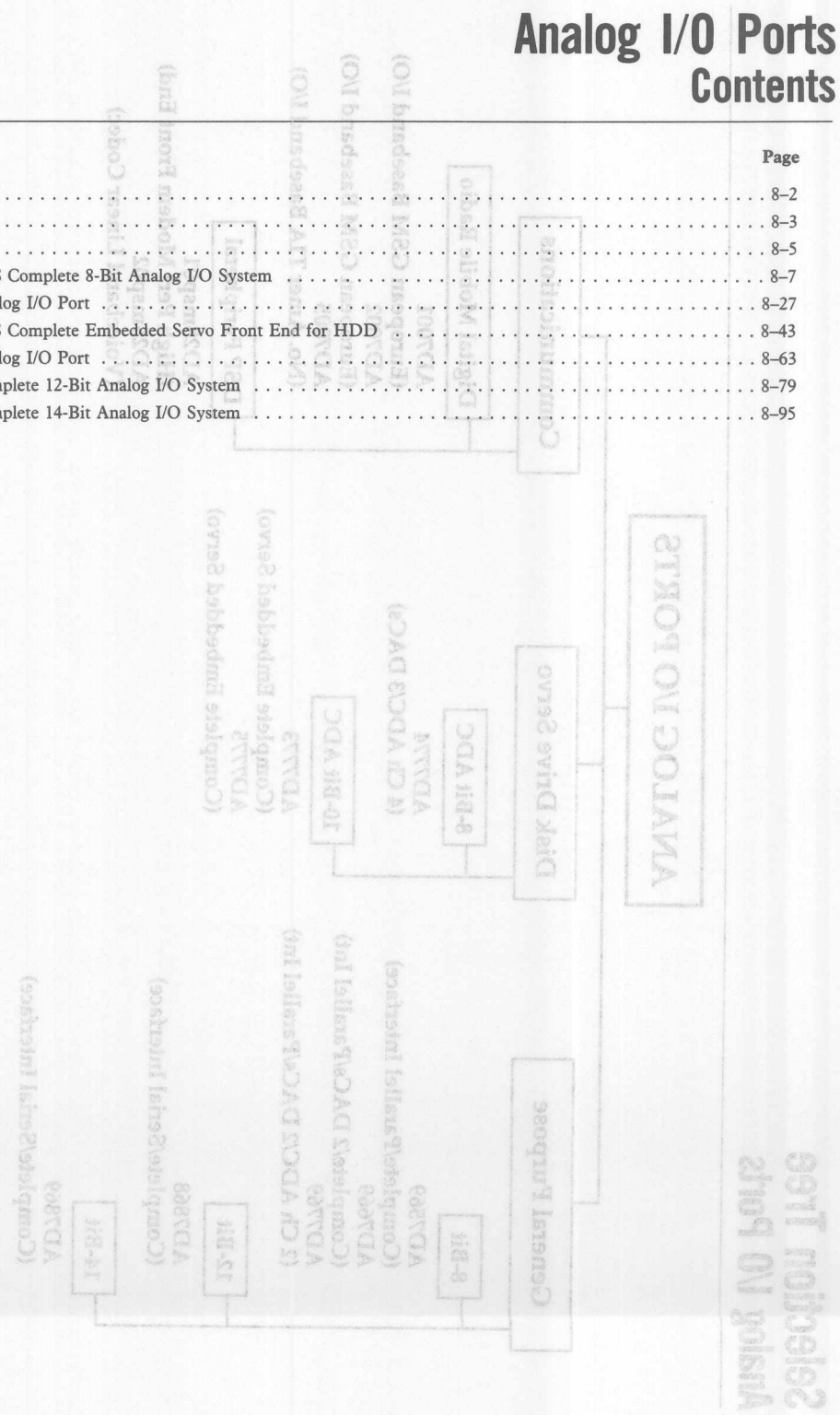


Figure 4. Typical Ground Layout for DAS1157/DAS1158/ DAS1159

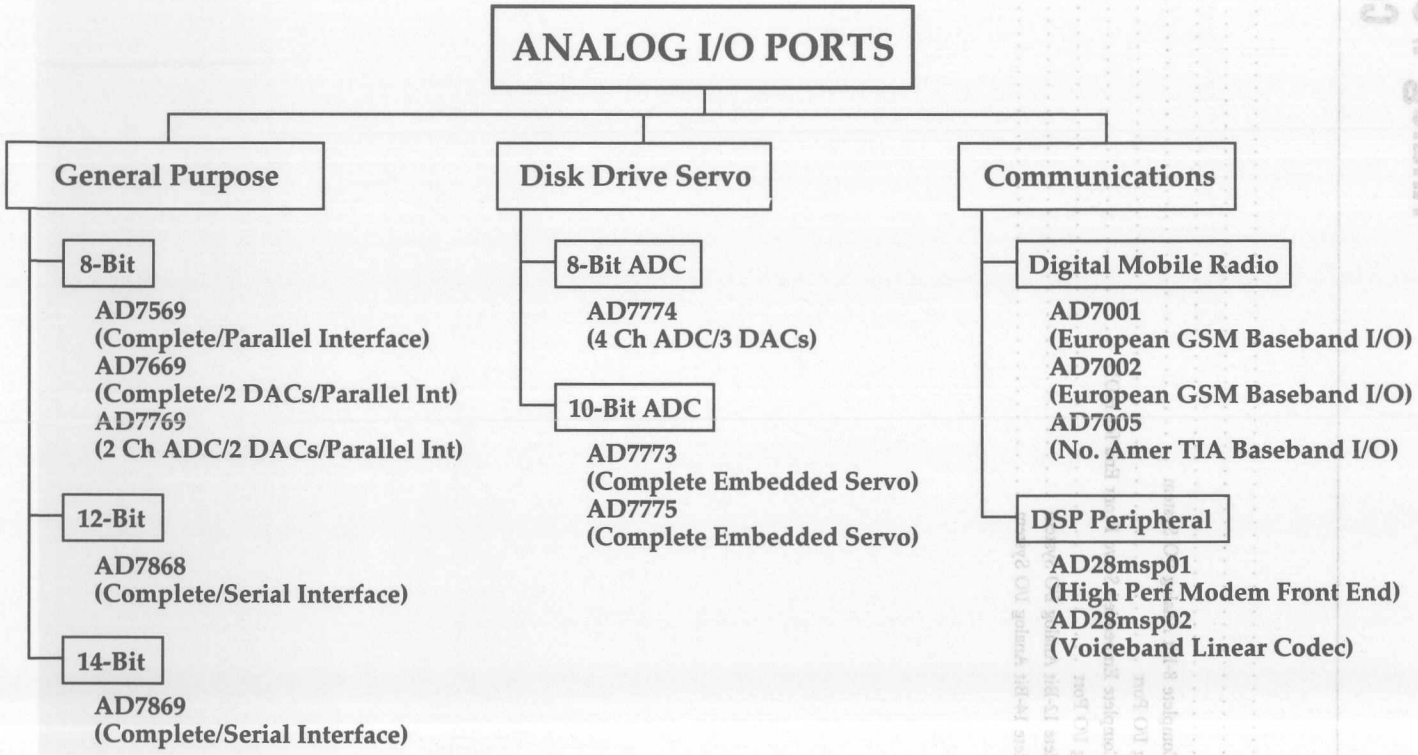
Analog I/O Ports
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Selection Tree
Analog I/O Ports



Selection Guide
Complete Analog I/O Ports

General Purpose

Model	Resolution Bits	Conv Time max μs	SHA BW kHz typ	Settling Time μs	Ref. Volt Int/Ext	Bus Interface	Package Options[1]	Temp Range[2]	Page	Comments
AD7569	8	2	500	1	Int	8, μP	2, 3, 4, 5, 6	C, I, M	C II 8–7	CMOS, Complete I/O Port with DAC, ADC, SHA, Amps and Reference
AD7669	8	2	500	1	Int	8, μP	2, 5, 6	C, I, M	C II 8–7	CMOS, Complete I/O Port with 2 DACs, ADC, SHA, Amps, and Reference
AD7769	8	3	500	2.5	Ext	8, μP	2, 5	C	C II 8–27	CMOS, Two-Channel ADC/DAC with Output Amplifiers
*AD7868	12	10	500	3	+3 V, Int	Serial, μP	2, 3, 6	I, M	C II 8–79	CMOS, Complete I/O Port with 12-Bit ADC and 12-Bit DAC
*AD7869	14	10	500	3.5	+3 V, Int	Serial, μP	2, 3, 6	C, I, M	C II 8–95	CMOS, Complete I/O Port with 14-Bit ADC and 14-Bit DAC

Disk Drive Servo

Model	ADC Resolution Bits	Conv Time max μs	DACs Resolution Bits	Settling Time μs	Ref.Volt Int/Ext	Bus Interface	Package Options[1]	Temp Range[2]	Page	Comments
*AD7774	8	3	8	4	Int/Ext	8, μP	2, 5	C	C II 8–43	CMOS, I/O Port with 4-Channel, 8-Bit ADC,
			11	8						11-Bit and Two 8-Bit DACs
*AD7773	10	3	8	3	2.1 V, Int	10, μP	6	C	C II 8–63	Complete Embedded Servo Front End for Hard
			10	4						Disk Drive with Separate Address and Data Pins
*AD7775	10	3	8	3	2.1 V, Int	10, μP	6	C	C II 8–43	Same as the AD7773 Except with Multiplexed
			10	4						Address/Data Bus

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-In-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92.
[2]Temperature Ranges: C = Commercial, 0 to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
Boldface type: Product recommended for new design.
*New product since the publication of the most recent Databooks.

Selection Guide
Complete Analog I/O Ports

Communications

Model	DAC/ADC Resolution Bits	DAC/ADC SNR + THD dB	Through-put kSPS	Ref. Volt Int/Ext	Bus Interface	Package Options[1]	Temp Range[2]	Page	Comments
*AD7001	10/8	56/44	2170	2.5 V, Int	10, 8 Serial, µP	10	C[3]	C I 4–47	GSM Baseband I/O Port
*AD7002	10/12	—/62	4333 (DAC) 541.7 (ADC)	2.5 V, Int	Serial, µP	10	C[3]	C I 4–59	GSM Baseband I/O Port with On-Board GMSK Modulator
*AD7005	10/12	—/62	97.2 (DAC) 194.4 (ADC)	2.3 V, Int	Serial, µP	10	C[3]	C I 4–75	TIA Baseband I/O Port
*AD28msp02	16/16	65/65	8	2.5 V, Int	Serial, µP	6	C	C I 4–25	Complete Voice Band Linear Codec with On-Chip Filtering
*AD28msp01	16/16	80/80	7.2/8.0/9.6	2.5 V, Int	Serial, µP	6	C	C I 4–9	Complete Analog Front End for High Performance DSP-Based Modems

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack; 11 = Single-In-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92.
[2]Temperature Ranges: C = Commercial, 0 to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
[3]Operates to −25°C.
*Boldface type: Product recommended for new design.
*New product since the publication of the most recent Databooks.

Orientation
Analog I/O Ports

Analog I/O Port products represent one of the highest levels of integration and functionality available in an IC package. These devices usually consist of the following functional blocks:

- single or multiple channel ADC
- one or more voltage output DACs with varying resolution
- sample-and-hold amplifiers
- one or more voltage references for both the DACs and ADC
- analog and/or digital filters
- associated control logic for easy μP interfacing.

This high level of integration on a chip has several distinct advantages over a multipackage solution. The ability to perform several functions on one chip lowers a systems chip count, thereby decreasing a system's real estate requirements while increasing its reliability. These devices, consisting of the various functional blocks, are fully specified, thus allowing for more predictable performance characteristics over the full operating range. The inherent cost savings due to a lower chip count as well as to lower R&D expenditures make Analog I/O Port devices an attractive solution for many data acquisition and distribution applications.

Our product portfolio for these devices can be subdivided into the following three subcategories: General Purpose, Disk Drive/Servo, and Communications. Some Analog I/O Ports are intended for specific industry applications but should not be considered to be limited to only those applications. General Purpose I/O Ports have a wide range of applications which include:

- digital signal processing
- speech recognition and synthesis
- spectrum analysis
- high speed modems
- servo control
- infinite sample and hold
- analog delay line
- peak detection.

These General Purpose I/O Ports are fully specified for dynamic parameters such as signal-to-noise ratio and harmonic distortion as well as traditional dc specifications.

Our Disk Drive/Servo category contains products which span the complete range of disk diameters and capabilities. Products such as the AD7773 and AD7775 contain all the circuitry to implement the demodulation and signal conversion in embedded servo systems. Both devices consist of a differential amplifier front end, a rectifier/integrator, a 10-bit sampling ADC and an 8- and 10-bit DAC. The AD7775 uses a multiplexed address/data bus with an ALE input latch to latch the address while the AD7773 uses a 10-bit data port with separate address pins.

The Communication I/O Port products integrate much of the functional blocks required in various communications applications onto a single chip. The AD28msp01 and the AD28msp02 are linear codecs that provide a complete front end for high performance modem and voiceband DSP applications, while the AD7001/02/05 are three products designed for the Pan-American (GSM) and American Digital Cellular Telephone systems.

DEFINITION OF SPECIFICATIONS

The specifications pertaining to these Analog I/O Port products are similar to those used in evaluating ADCs and DACs.

ANALOG DEVICES

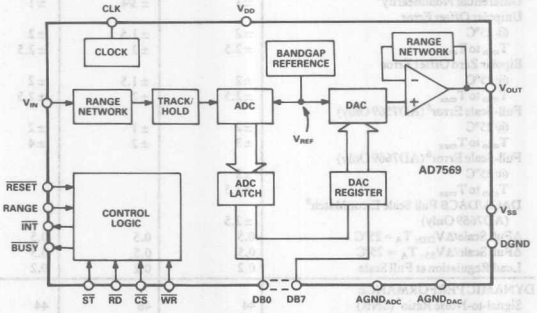
LC²MOS Complete, 8-Bit Analog I/O System

AD7569/AD7669

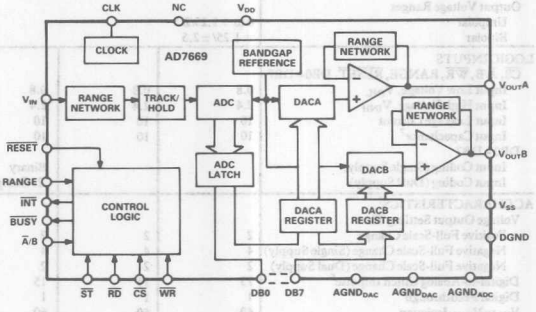
FEATURES

2μs ADC with Track/Hold
1μs DAC with Output Amplifier
AD7569, Single DAC Output
AD7669, Dual DAC Output
On-Chip Bandgap Reference
Fast Bus Interface
Single or Dual 5V Supplies

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7569/AD7669 is a complete, 8-bit, analog I/O system on a single monolithic chip. The AD7569 contains a high speed successive approximation ADC with 2μs conversion time, a track/hold with 200kHz bandwidth, a DAC and output buffer amplifier with 1μs settling time. A temperature-compensated 1.25V bandgap reference provides a precision reference voltage for the ADC and the DAC. The AD7669 is similar but contains two DACs with output buffer amplifiers.

A choice of analog input/output ranges is available. Using a supply voltage of +5V, input and output ranges of zero to 1.25V and zero to 2.5 volts may be programmed using the RANGE input pin. Using a ±5V supply, bipolar ranges of ±1.25V or ±2.5V may be programmed.

Digital interfacing is via an 8-bit I/O port and standard microprocessor control lines. Bus interface timing is extremely fast, allowing easy connection to all popular 8-bit microprocessors. A separate start convert line controls the track/hold and ADC to give precise control of the sampling period.

The AD7569/AD7669 is fabricated in Linear-Compatible CMOS (LC²MOS), an advanced, mixed technology process combining precision bipolar circuits with low power CMOS logic. The AD7569 is packaged in a 24-pin, 0.3″ wide "skinny" DIP, a 24-terminal SOIC and 28-terminal PLCC and LCCC packages. The AD7669 is available in a 28-pin, 0.6″ plastic DIP, 28-terminal SOIC, and 28-terminal PLCC package.

PRODUCT HIGHLIGHTS

1. Complete Analog I/O on a Single Chip.
   The AD7569/AD7669 provides everything necessary to interface a microprocessor to the analog world. No external components or user trims are required, and the overall accuracy of the system is tightly specified, eliminating the need to calculate error budgets from individual component specifications.
2. Dynamic Specifications for DSP Users.
   In addition to the traditional ADC and DAC specifications the AD7569/AD7669 is specified for AC parameters, including signal-to-noise ratio, distortion and input bandwidth.
3. Fast Microprocessor Interface.
   The AD7569/AD7669 has bus interface timing compatible with all modern microprocessors, with bus access and relinquish times less than 75ns and Write pulse width less than 80ns.

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AD7569/AD7669–DAC SPECIFICATIONS[1]

(V_{DD} = +5V ±5%; V_{SS}[2] = RANGE = $AGND_{DAC}$ = $AGND_{ADC}$ = DGND = 0V; R_L = 2kΩ, C_L = 100pF to $AGND_{DAC}$ unless otherwise stated. All specifications T_{min} to T_{max} unless otherwise stated.)

Parameter	AD7569 J, A Versions[3] AD7669 J Version	AD7569 K, B Versions	AD7569 S Version	AD7569 T Version	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution[4]	8	8	8	8	Bits	
Total Unadjusted Error[5]	±2	±2	±3	±3	LSB typ	
Relative Accuracy[5]	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity[5]	±1	±3/4	±1	±3/4	LSB max	Guaranteed Monotonic
Unipolar Offset Error						DAC data is all 0s; V_{SS} = 0V
@ 25°C	±2	±1.5	±2	±1.5	LSB max	Typical tempco is 10μV/°C for + 1.25V range
T_{min} to T_{max}	±2.5	±2	±2.5	±2	LSB max	
Bipolar Zero Offset Error						DAC data is all 0s; V_{SS} = −5V
@ 25°C	±2	±1.5	±2	±1.5	LSB max	Typical tempco is 20μV/°C for ±1.25V range
T_{min} to T_{max}	±2.5	±2	±2.5	±2	LSB max	
Full-Scale Error[6] (AD7569 Only)						V_{DD} = 5V
@ 25°C	±2	±1	±2	±1	LSB max	
T_{min} to T_{max}	±3	±2	±4	±3	LSB max	
Full-Scale Error[6] (AD7669 Only)						V_{DD} = 5V
@ 25°C	±3				LSB max	
T_{min} to T_{max}	±4.5				LSB max	
DACA/DACB Full Scale Error Match[6] (AD7669 Only)	±2.5				LSB max	V_{DD} = 5V
ΔFull Scale/ΔV_{DD}, T_A = 25°C	0.5	0.5	0.5	0.5	LSB max	V_{OUT} = 2.5V; ΔV_{DD} = ±5%
ΔFull Scale/ΔV_{SS}, T_A = 25°C	0.5	0.5	0.5	0.5	LSB max	V_{OUT} = −2.5V; ΔV_{SS} = ±5%
Load Regulation at Full Scale	0.2	0.2	0.2	0.2	LSB max	R_L = 2kΩ to 0/C
DYNAMIC PERFORMANCE						
Signal-to-Noise Ratio[5] (SNR)	44	46	44	46	dB min	V_{OUT} = 20kHz full-scale sine wave with $f_{SAMPLING}$ = 400kHz
Total Harmonic Distortion[5] (THD)	48	48	48	48	dB max	V_{OUT} = 20kHz full-scale sine wave with $f_{SAMPLING}$ = 400kHz
Intermodulation Distortion[5] (IMD)	55	55	55	55	dB typ	fa = 18.4kHz, fb = 14.5kHz with $f_{SAMPLING}$ = 400kHz
ANALOG OUTPUT						
Output Voltage Ranges						
Unipolar	0 to +1.25/2.5				Volts	V_{DD} = +5V, V_{SS} = 0V
Bipolar	±1.25/±2.5				Volts	V_{DD} = +5V, V_{SS} = −5V
LOGIC INPUTS						
$\overline{CS}$, A/B, $\overline{WR}$, RANGE, $\overline{RESET}$, DB0–DB7						
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Leakage Current	10	10	10	10	μA max	V_{IN} = 0 to V_{DD}
Input Capacitance[7]	10	10	10	10	pF max	
DB0–DB7						
Input Coding (Single Supply)			Binary			
Input Coding (Dual Supply)			2s Complement			
AC CHARACTERISTICS[7]						
Voltage Output Settling Time						Settling time to within ±1/2LSB of final value
Positive Full-Scale Change	2	2	2	2	μs max	Typically 1μs
Negative Full-Scale Change (Single Supply)	4	4	4	4	μs max	Typically 2μs
Negative Full-Scale Change (Dual Supply)	2	2	2	2	μs max	Typically 1μs
Digital-to-Analog Glitch Impulse[5]	15	15	15	15	nV secs typ	
Digital Feedthrough[5]	1	1	1	1	nV secs typ	
V_{IN} to V_{OUT} Isolation	60	60	60	60	dB typ	V_{IN} = ±2.5V, 50kHz Sine Wave
DAC to DAC Crosstalk[5] (AD7669 Only)	1				nV secs typ	
DACA to DACB Isolation[5] (AD7669 Only)	−70				dB max	
POWER REQUIREMENTS						
V_{DD} Range	4.75/5.25	4.75/5.25	4.75/5.25	4.75/5.25	Vmin/Vmax	For Specified Performance
V_{SS} Range (Dual Supplies)	−4.75/−5.25	−4.75/−5.25	−4.75/−5.25	−4.75/−5.25	Vmin/Vmax	Specified Performance also applies to V_{SS} = 0V for unipolar ranges.
I_{DD}						V_{OUT} = V_{IN} = 2.5V; Logic Inputs = 2.4V; CLK = 0.8V
(AD7569)	13	13	13	13	mA max	Output unloaded
(AD7669)	18				mA max	Outputs unloaded
I_{SS} (Dual Supplies)						V_{OUT} = V_{IN} = −2.5V; Logic Inputs = 2.4V; CLK = 0.8V
(AD7569)	4	4	4	4	mA max	Output unloaded
(AD7669)	6				mA max	Outputs unloaded
DAC/ADC MATCHING						
Gain Matching[6]						V_{IN} to V_{OUT} match with V_{IN} = ±2.5V, 20kHz sine wave
@25°C	1	1	1	1	% typ	
T_{min} to T_{max}	1	1	1	1	% typ	

NOTES

[1]Specifications apply to both DACs in the AD7669. V_{OUT} applies to both V_{OUT}A and V_{OUT}B of the AD7669.

[2]Except where noted, specifications apply for all output ranges including bipolar ranges with dual supply operation.

[3]Temperature ranges are as follows: J, K versions; 0 to +70°C
A, B versions; −25°C to +85°C
S, T versions; −55°C to +125°C

[4]1LSB = 4.88mV for 0 to +1.25V output range, 9.76mV for 0 to +2.5V and ±1.25V ranges and 19.5mV for ±2.5V range.

[5]See Terminology.

[6]Includes internal voltage reference error and is calculated after offset error has been adjusted out. Ideal unipolar full-scale voltage is (FS – 1LSB); ideal bipolar positive full-scale voltage is (FS/2 – 1LSB) and ideal bipolar negative full-scale voltage is −FS/2.

[7]Sample tested at 25°C to ensure compliance.

Specifications subject to change without notice.

ADC SPECIFICATIONS

(V_{DD} = +5V ±5%; V_{SS}[1] = RANGE = $AGND_{DAC}$ = $AGND_{ADC}$ = DGND = 0V; f_{CLK} = 5MHz external unless otherwise stated. All specifications T_{min} to T_{max} unless otherwise stated.) Specifications apply to Mode 1 interface.

Parameter	AD7569 J, A Versions[2] AD7669 J Version	AD7569 K, B Versions	AD7569 S Version	AD7569 T Version	Units	Conditions/Comments
DC ACCURACY						
Resolution[3]	8	8	8	8	Bits	
Total Unadjusted Error[4]	±3	±3	±4	±4	LSB typ	
Relative Accuracy[4]	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity[4]	±1	±3/4	±1	±3/4	LSB max	No Missing Codes
Unipolar Offset Error						Typical tempco is 10μV/°C for +1.25V range; V_{SS} = 0V
@25°C	±2	±1.5	±2	±1.5	LSB max	
T_{min} to T_{max}	±3	±2.5	±3	±2.5	LSB max	
Bipolar Zero Offset Error						Typical tempco is 20μV/°C for ±1.25V range; V_{SS} = −5V
@25°C	±3	±2.5	±3	±2.5	LSB max	
T_{min} to T_{max}	±3.5	±3	±4	±3.5	LSB max	
Full-Scale Error[5]						V_{DD} = 5V
@25°C	−4, +0	−4, +0	−4, +0	−4, +0	LSB max	
T_{min} to T_{max}	−5.5, +1.5	−5.5, +1.5	−7.5, +2	−7.5, +2	LSB max	
ΔFull Scale/ΔV_{DD}, T_A = 25°C	0.5	0.5	0.5	0.5	LSB max	V_{IN} = +2.5V; ΔV_{DD} = ±5%
ΔFull Scale/ΔV_{SS}, T_A = 25°C	0.5	0.5	0.5	0.5	LSB max	V_{IN} = −2.5V; ΔV_{SS} = ±5%
DYNAMIC PERFORMANCE						
Signal-to-Noise Ratio[4] (SNR)	44	46	44	45	dB min	V_{IN} = 100kHz full-scale sine wave with $f_{SAMPLING}$ = 400kHz[6]
Total Harmonic Distortion[4] (THD)	48	48	48	48	dB max	V_{IN} = 100kHz full-scale sine wave with $f_{SAMPLING}$ = 400kHz[6]
Intermodulation Distortion[4] (IMD)	60	60	60	60	dB typ	fa = 99kHz, fb = 96.7kHz with $f_{SAMPLING}$ = 400kHz
Frequency Response	0.1	0.1	0.1	0.1	dB typ	V_{IN} = ±2.5V, dc to 200kHz sine wave
Track/Hold Acquisition Time[7]	200	200	300	300	ns typ	
ANALOG INPUT						
Input Voltage Ranges						
Unipolar	0 to +1.25/+2.5				Volts	V_{DD} = +5V; V_{SS} = 0V
Bipolar	±1.25/±2.5				Volts	V_{DD} = +5V; V_{SS} = −5V
Input Current	±300	±300	±300	±300	μA max	See equivalent circuit Fig. 5
Input Capacitance	10	10	10	10	pF typ	
LOGIC INPUTS						
$\overline{CS}$, $\overline{RD}$, $\overline{ST}$, CLK, $\overline{RESET}$, RANGE						
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Capacitance[8]	10	10	10	10	pF max	
$\overline{CS}$, $\overline{RD}$, $\overline{ST}$, RANGE, $\overline{RESET}$						
Input Leakage Current	10	10	10	10	μA max	V_{IN} = 0 to V_{DD}
CLK						
Input Current						
I_{INL}	−1.6	−1.6	−1.6	−1.6	mA max	V_{IN} = 0V
I_{INH}	40	40	40	40	μA max	V_{IN} = V_{DD}
LOGIC OUTPUTS						
DB0–DB7, $\overline{INT}$, $\overline{BUSY}$						
V_{OL}, Output Low Voltage	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 200μA
DB0–DB7						
Floating State Leakage Current	10	10	10	10	μA max	
Floating State Output Capacitance[8]	10	10	10	10	pF max	
Output Coding (Single Supply)		Binary				
Output Coding (Dual Supply)		2s Complement				
CONVERSION TIME						
With External Clock	2	2	2	2	μs max	f_{CLK} = 5MHz
With Internal Clock, T_A = 25°C	1.6	1.6	1.6	1.6	μs min	Using recommended clock components shown in Figure 21. Clock frequency can be adjusted by varying R_{CLK}.
	2.6	2.6	2.6	2.6	μs max	
POWER REQUIREMENTS	As per DAC Specifications					

NOTES

[1]Except where noted, specifications apply for all ranges including bipolar ranges with dual supply operation.

[2]Temperature ranges are as follows: J, K versions; 0 to +70°C
A, B versions; −25°C to +85°C
S, T versions; −55°C to +125°C

[3]1LSB = 4.88mV for 0 to +1.25V range, 9.76mV for 0 to +2.5V and ±1.25V ranges and 19.5mV for ±2.5V range.

[4]See Terminology.

[5]Includes internal voltage reference error and is calculated after offset error has been adjusted out. Ideal unipolar last code transition occurs at (FS – 3/2LSB); Ideal bipolar last code transition occurs at (FS/2 – 3/2LSB).

[6]Exact frequencies are 101kHz and 384kHz to avoid harmonics coinciding with sampling frequency.

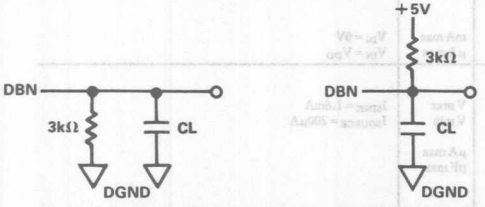
[7]Rising edge of $\overline{BUSY}$ to falling edge of $\overline{ST}$. The time given refers to the acquisition time which gives a 3dB degradation in SNR from the tested figure.

[8]Sample tested at 25°C to ensure compliance.

Specifications subject to change without notice.

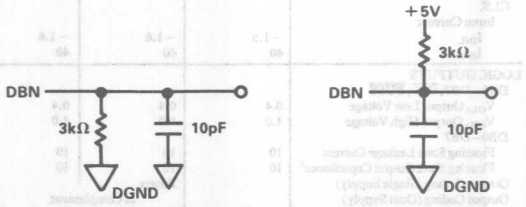
DAC Timing					
t_1	80	80	90	ns min	$\overline{WR}$ Pulse Width
t_2	0	0	0	ns min	$\overline{CS}$, A/B to $\overline{WR}$ Setup Time
t_3	0	0	0	ns min	$\overline{CS}$, A/B to $\overline{WR}$ Hold Time
t_4	60	70	80	ns min	Data Valid to $\overline{WR}$ Setup Time
t_5	10	10	10	ns min	Data Valid to $\overline{WR}$ Hold Time
ADC Timing					
t_6	50	50	50	ns min	$\overline{ST}$ Pulse Width
t_7	110	130	150	ns max	$\overline{ST}$ to $\overline{BUSY}$ Delay
t_8	20	30	30	ns max	$\overline{BUSY}$ to $\overline{INT}$ Delay
t_9	0	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Delay
t_{10}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_{11}	60	75	90	ns min	$\overline{RD}$ Pulse Width. Determined by t_{13}.
t_{12}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_{13}[2]	60	75	90	ns max	Data Access Time after $\overline{RD}$; $C_L = 20pF$
	95	120	135	ns max	Data Access Time after $\overline{RD}$; $C_L = 100pF$
t_{14}[3]	10	10	10	ns min	Bus Relinquish Time after $\overline{RD}$
	60	75	85	ns max	
t_{15}	65	75	85	ns max	$\overline{RD}$ to $\overline{INT}$ Delay
t_{16}	120	140	160	ns max	$\overline{RD}$ to $\overline{BUSY}$ Delay
t_{17}[2]	60	75	90	ns max	Data Valid Time after $\overline{BUSY}$; $C_L = 20pF$
	90	115	135	ns max	Data Valid Time after $\overline{BUSY}$; $C_L = 100pF$

NOTES
[1]Sample tested at +25°C to ensure compliance. All input control signals are specified with $t_R = t_F = 5ns$ (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]t_{13} and t_{17} are measured with the load circuits of Figure 1 and defined as the time required for an output to cross either 0.8V or 2.4V.
[3]t_{14} is defined as the time required for the data line to change 0.5V when loaded with the circuit of Figure 2.
Specifications subject to change without notice.



a. High-Z to V_{OH} *b. High-Z to V_{OL}*

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 2. Load Circuits for Bus Relinquish Time Test

ABSOLUTE MAXIMUM RATINGS

V_{DD} to $AGND_{DAC}$ or $AGND_{ADC}$ . . . . . −0.3V, +7V
V_{DD} to DGND . . . . . −0.3V, +7V
V_{DD} to V_{SS} . . . . . −0.3V, +14V
$AGND_{DAC}$ or $AGND_{ADC}$ to DGND . . −0.3V, V_{DD} +0.3V
$AGND_{DAC}$ to $AGND_{ADC}$ . . . . . ±5V
Logic Voltage to DGND . . . . . −0.3V, V_{DD} +0.3V
CLK Input Voltage to DGND . . . . −0.3V, V_{DD} +0.3V
V_{OUT} (V_{OUT}A, V_{OUT}B) to
$AGND^1_{DAC}$ . . . . . V_{SS} −0.3V, V_{DD}+0.3V
V_{IN} to $AGND_{ADC}$ . . . . . V_{SS} −0.3V, V_{DD} +0.3V

NOTE
[1]Output may be shorted to any voltage in the range V_{SS} to V_{DD} provided that the power dissipation of the package is not exceeded. Typical short circuit current for a short to AGND or V_{SS} is 50mA.

Power Dissipation (Any Package) to +75°C 450mW
Derates above 75°C by . . . . . 6mW/°C
Operating Temperature Range
Commercial (J, K) . . . . . 0 to +70°C
Industrial (A, B) . . . . . −25°C to +85°C
Extended (S, T) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 Secs) . . . . . +300°C

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



NOTE:
The term DAC (Digital-to-Analog Converter) throughout the data sheet applies equally to the dual DACs in the AD7669 as well as to the single DAC of the AD7569 unless otherwise stated. It follows that the term V_{OUT} applies to both $V_{OUT}A$ and $V_{OUT}B$ of the AD7669 also.

TERMINOLOGY

Total Unadjusted Error
Total unadjusted error is a comprehensive specification which includes internal voltage reference error, relative accuracy, gain and offset errors.

Relative Accuracy (DAC)
Relative Accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after allowing for offset and gain errors. For the bipolar output ranges the endpoints of the DAC transfer function are defined as those voltages which correspond to negative full-scale and positive full-scale codes. For the unipolar output ranges the endpoints are code 1 and code 255. Code 1 is chosen because the amplifier is now working in single supply and in cases where the true offset of the amplifier is negative it cannot be seen at code 0. If the relative accuracy was calculated between code 0 and code 255 the "negative offset" would appear as a linearity error. If the offset is negative and less than 1LSB, it will appear at code 1, and hence the true linearity of the converter is seen between code 1 and code 255.

Relative Accuracy (ADC)
Relative Accuracy is the deviation of the ADC's actual code transition points from a straight line drawn between the endpoints of the ADC transfer function. For the bipolar input ranges these points are the measured negative full-scale transition point and the measured positive full-scale transition point. For the unipolar ranges the straight line is drawn between the measured first LSB transition point and the measured full-scale transition point.

Differential Nonlinearity
Differential Nonlinearity is the difference between the measured change and an ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max ensures monotonicity (DAC) or no missed codes (ADC). A differential nonlinearity of ±3/4LSB max ensures that the minimum step size (DAC) or code width (ADC) is 1/4LSB and the maximum step size or code width is 3/4LSB.

Digital-to-Analog Glitch Impluse
Digital-to-Analog Glitch Impulse is the impulse injected into the analog output when the digital inputs change state with the DAC selected. It is normally specified as the area of the glitch in nVsecs and is measured when the digital input code is changed by 1LSB at the major carry transition.

Digital Feedthrough
Digital Feedthrough is also a measure of the impulse injected to the analog output from the digital inputs but is measured when the DAC is not selected. It is essentially feedthrough across the die and package. It is also a measure of the glitch impulse transferred to the analog output when data is read from the internal ADC. It is specified in nVsecs and is measured with $\overline{WR}$ high and a digital code change from all 0s to all 1s.

DAC-to-DAC Crosstalk (AD7669 Only)
The glitch energy transferred to the output of one DAC due to an update at the output of the second DAC. The figure given is the worst case and is expressed in nV secs. It is measured with an update voltage of full scale.

DAC-to-DAC Isolation (AD7669 Only)
DAC-to-DAC Isolation is the proportion of a digitized sine wave from the output of one DAC which appears at the output of the second DAC (loaded with all 1s). The figure given is the worst case for the second DAC output and is expressed as a ratio in dBs. It is measured with a digitized sine wave ($f_{SAMPLING}$ = 100kHz) of 20kHz at 2.5V pk-pk.

Signal-to-Noise Ratio
Signal-to-Noise Ratio (SNR) is the measured signal to noise at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals (excluding dc) up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)\ dB$$

where N is the number of bits. Thus for an ideal 8-bit converter, SNR = 50dB.

Harmonic Distortion
Harmonic Distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7569/AD7669, Total Harmonic Distortion (THD) is defined as

$$20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

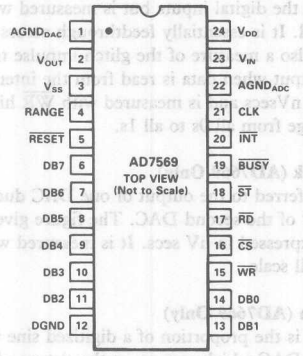
where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the individual harmonics.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mfa ± nfb, where m,n = 0, 1, 2, 3,.... . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms include (fa + fb) and (fa − fb) and the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb).

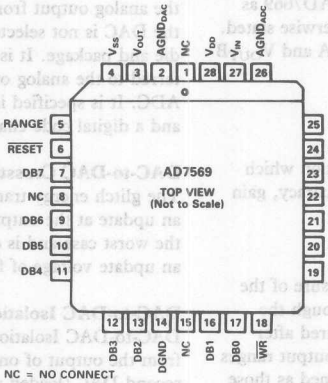
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AD7569 PIN CONFIGURATIONS

DIP, SOIC

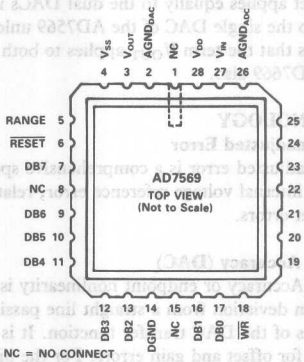


PLCC



NC = NO CONNECT

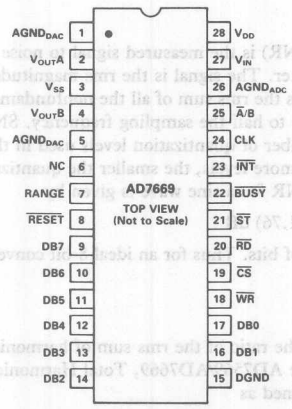
LCCC



NC = NO CONNECT

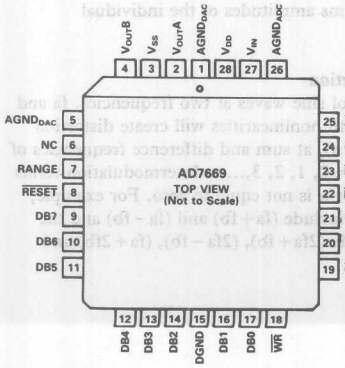
AD7669 PIN CONFIGURATIONS

DIP, SOIC



NC = NO CONNECT

PLCC



NC = NO CONNECT

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy $T_{MIN}-T_{MAX}$	Package Option[1]
AD7569JN	0°C to +70°C	±1LSB	N-24
AD7569JR	0°C to +70°C	±1LSB	R-24
AD7569AQ	−25°C to +85°C	±1LSB	Q-24
AD7569SQ[2]	−55°C to +125°C	±1LSB	Q-24
AD7569KN	0°C to +70°C	±1/2LSB	N-24
AD7569BQ	−25°C to +85°C	±1/2LSB	Q-24
AD7569TQ[2]	−55°C to +125°C	±1/2LSB	Q-24
AD7569JP	0°C to +70°C	±1LSB	P-28A
AD7569SE[2]	−55°C to +125°C	±1LSB	E-28A
AD7569KP	0°C to +70°C	±1/2LSB	P-28A
AD7569TE[2]	−55°C to +125°C	±1/2LSB	E-28A
AD7669JN	0°C to +70°C	±1LSB	N-28
AD7669JP	0°C to +70°C	±1LSB	P-28A
AD7669JR	0°C to +70°C	±1LSB	R-28

NOTES

[1]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline SOIC. For outline information see Package Information section.

[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.

PIN FUNCTION DESCRIPTION

(Applies to the AD7569 and AD7669 unless otherwise stated.)

Pin Mnemonic	Description
$AGND_{DAC}$	Analog Ground for the DAC(s). Separate ground return paths are provided for the DAC(s) and ADC to minimize crosstalk.
V_{OUT} ($V_{OUT}A$, $V_{OUT}B$)	Output Voltage. V_{OUT} is the buffered output voltage from the AD7569 DAC. $V_{OUT}A$ and $V_{OUT}B$ are the buffered DAC output voltages from the AD7669. Four different output voltage ranges can be achieved (see Table I).
V_{SS}	Negative Supply Voltage ($-5V$ for dual supply or 0V for single supply). This pin is also used with the RANGE pin to select the different input/output ranges and changes the data format from binary ($V_{SS} = 0V$) to 2s complement ($V_{SS} = -5V$) (see Table I).
RANGE	Range Selection Input. This is used with the V_{SS} input to select the different ranges as per Table I. The range selected applies to both the analog input voltage of the ADC and the output voltage from the DAC(s).
$\overline{RESET}$	Reset Input (Active Low). This is an asynchronous system reset which clears the DAC register(s) to all 0s and clears the $\overline{INT}$ line of the ADC (i.e., makes the ADC ready for new conversion). In unipolar operation this input sets the output voltage to 0V; in bipolar operation it sets the output to negative full scale.
DB7	Data Bit 7. Most Significant Bit (MSB).
DB6–DB2	Data Bit 6 to Data Bit 2.
DGND	Digital Ground.
DB1	Data Bit 1.
DB0	Data Bit 0. Least Significant Bit (LSB).
$\overline{WR}$	Write Input (Edge triggered). This is used in conjunction with $\overline{CS}$ to write data into the AD7569 DAC register. It is used in conjunction with $\overline{CS}$ and A/B to write data into the selected DAC register of the AD7669. Data is transferred on the rising edge of $\overline{WR}$.

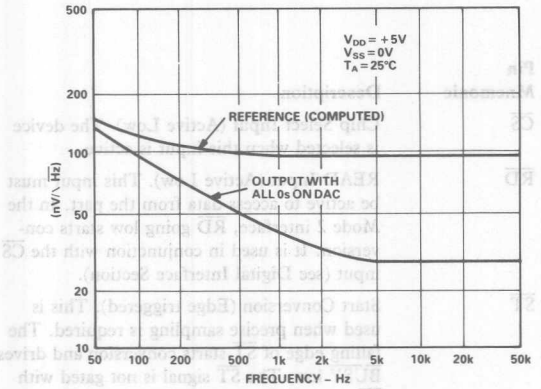
Pin Mnemonic	Description
$\overline{CS}$	Chip Select Input (Active Low). The device is selected when this input is active.
$\overline{RD}$	READ Input (Active Low). This input must be active to access data from the part. In the Mode 2 interface, $\overline{RD}$ going low starts conversion. It is used in conjunction with the $\overline{CS}$ input (see Digital Interface Section).
$\overline{ST}$	Start Conversion (Edge triggered). This is used when precise sampling is required. The falling edge of $\overline{ST}$ starts conversion and drives $\overline{BUSY}$ low. The $\overline{ST}$ signal is not gated with $\overline{CS}$.
$\overline{BUSY}$	BUSY Status Output (Active Low). When this pin is active the ADC is performing a conversion. The input signal is held prior to the falling edge of $\overline{BUSY}$ (see Digital Interface Section).
$\overline{INT}$	INTERRUPT Output (Active Low). $\overline{INT}$ going low indicates that the conversion is complete. $\overline{INT}$ goes high on the rising edge of $\overline{CS}$ or $\overline{RD}$ and is also set high by a low pulse on $\overline{RESET}$ (see Digital Interface Section).
A/B (AD7669 Only)	DAC Select Input. This input selects which DAC register data is written to under control of $\overline{CS}$ and $\overline{WR}$. With this input low data is written to the DACA register; with this input high data is written to the DACB register.
CLK	A TTL compatible clock signal may be used to determine the ADC conversion time. Internal clock operation is achieved by connecting a resistor and capacitor to ground.
$AGND_{ADC}$	Analog Ground for the ADC.
V_{IN}	Analog Input. Various input ranges can be selected (see Table I).
V_{DD}	Positive Supply Voltage ($+5V$).

Range	V_{SS}	Input/Output Voltage Range	DB0–DB7 Data Format
0	0V	0 to +1.25V	Binary
1	0V	0 to +2.5V	Binary
0	−5V	±1.25V	2s Complement
1	−5V	±2.5V	2s Complement

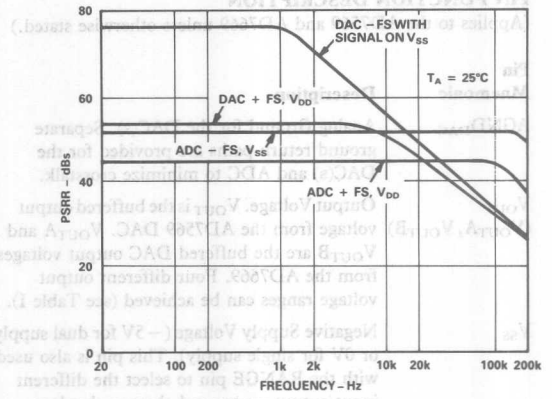
Table I. Input/Output Ranges

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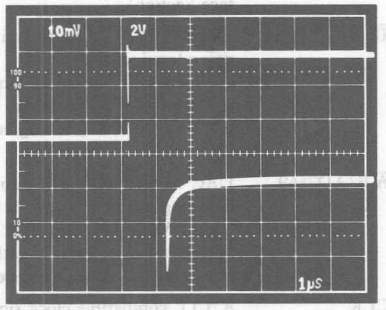
AD7569/AD7669–Typical Performance Graphs



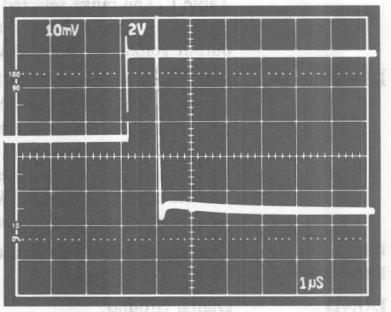
Noise Spectral Density vs. Frequency



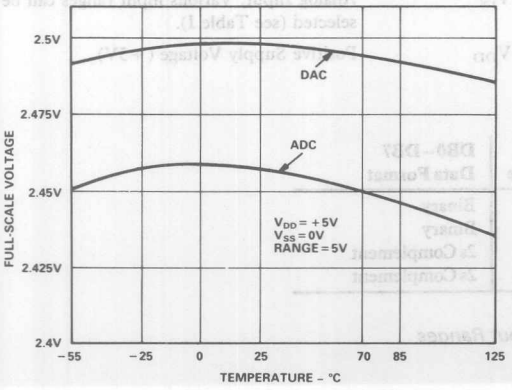
Power Supply Rejection Ratio vs. Frequency



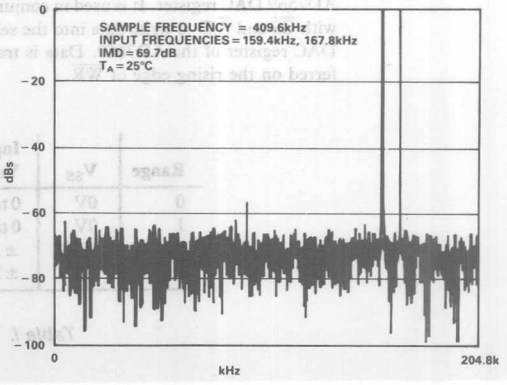
Positive-Going Settling Time (±2.5V Range)



Negative-Going Settling Time (±2.5V Range)



DAC/ADC Full-Scale Temperature Coefficient



IMD Plot for ADC

CIRCUIT DESCRIPTION

D/A SECTION

The AD7569 contains an 8-bit, voltage-mode, D/A converter which uses eight equally weighted current sources switched into an R-2R ladder network to give a direct but unbuffered 0 to +1.25V output range. The AD7669 is similar but contains two D/A converters. The current sources are fabricated using PNP transistors. These transistors allow current sources which are driven from positive voltage logic and give a zero-based output range. The output voltage from the voltage switching R-2R ladder network has the same positive polarity as the reference and therefore the D/A converter can be operated from a single power supply rail.

The PNP current sources are generated using the on-chip bandgap reference and a control amplifier. The current sources are switched to either the ladder or $AGND_{DAC}$ by high speed p-channel switches. These high-speed switches ensure a fast settling time for the output voltage of the DAC. The R-2R ladder network of the DAC consists of highly stable, thin-film resistors. A simplified circuit diagram for the D/A converter section is shown in Figure 3. An identical D/A converter is used as part of the A/D converter which is discussed later.

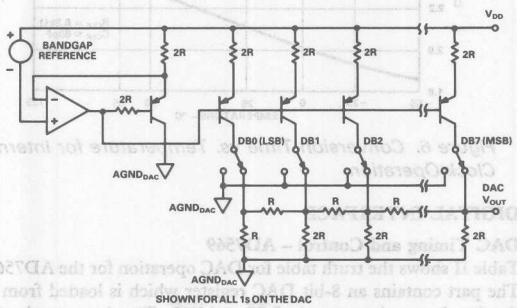


Figure 3. DAC Simplified Circuit Diagram

OP AMP SECTION

The output from the D/A converter is buffered by a high speed, noninverting op amp. This op amp is capable of developing ±2.5V across a 2kΩ and 100pF load to $AGND_{DAC}$. The amplifier can be operated from a single +5V supply to give two unipolar output ranges or from dual supplies (±5V) to allow two bipolar output ranges.

The feedback path of the amplifier contains a gain/offset network which provides four voltage ranges at the output of the op amp. The output voltage range is determined by the RANGE and V_{SS} inputs. (See Table I in the Pin Function Description section.) The four output ranges possible are: 0 to +1.25V, 0 to +2.5V, ±1.25V and ±2.5V. It should be noted that whatever range is selected for the output amplifier also applies to the input voltage range of the A/D converter.

The output amplifier settles to within 1/2LSB of its final value in typically less than 500ns. Operating the part from single or dual supplies has no effect on the positive-going settling time. However, the negative-going output settling time to voltages near 0V in single supply will be slightly longer than the settling time to negative full scale for dual supply operation. Additionally, to ensure that the output voltage can go to 0V in single supply, a transistor on the output acts as a passive pull-down with output voltages near 0V with V_{SS} = 0V. This means that the sink capability of the amplifier is reduced as the output voltage nears 0V in single supply. In dual supply operation the full sink capability of 1.25mA is maintained over the entire output voltage range.

For all other parameters the single and dual supply performances of the amplifier are essentially identical. The output noise from the amplifier with full scale on the DAC is 200μV peak-to-peak. The spot noise at 1kHz is 35nV/$\sqrt{Hz}$ with all 0s on the DAC. A noise spectral density versus frequency plot for the amplifier is shown in the typical performance graphs.

VOLTAGE REFERENCE

The AD7569/AD7669 contains an on-chip bandgap reference which provides a low noise, temperature compensated reference voltage for both the DAC and the ADC. The reference is trimmed for both absolute accuracy and temperature coefficient. The bandgap reference is generated with respect to V_{DD}. It is buffered by a separate control amplifier for both the DAC and the ADC reference. This can be seen in the DAC ladder network configuration in Figure 3.

DIGITAL SECTION

The data pins on the AD7569/AD7669 provide a connection between the external bus and both the DAC data inputs and ADC data outputs. The threshold levels of all digital inputs and outputs are compatible with either TTL or 5V CMOS levels. Internal input protection of all digital pins is achieved by on-chip distributed diodes.

The data format is straight binary when the part is used in single supply (V_{SS} = 0V). However, when a V_{SS} of −5V is applied, the data format becomes 2s complement. This data format applies to the digital inputs of the DAC and the digital outputs of the ADC.

ADC SECTION

The analog-to-digital converter on the AD7569/AD7669 uses the successive approximation technique to achieve a fast conversion time of 2μs and provide an 8-bit parallel digital output. The reference for the ADC is provided by the on-chip bandgap reference.

Conversion start is controlled by $\overline{ST}$ or by $\overline{CS}$ and $\overline{RD}$. Once a conversion has been started another conversion start should not be attempted until the conversion in progress is completed. Exercising the $\overline{RESET}$ input does not affect conversion; the $\overline{RESET}$ input resets the $\overline{INT}$ line high which is useful in interrupt-driven systems where a READ has not been performed at the end of the previous conversion. The $\overline{INT}$ line does not have to be cleared at the end of conversion. The ADC will continue to convert correctly but the function of the $\overline{INT}$ line will be affected.

Figure 4 shows the operating waveforms for a conversion cycle. The analog input voltage, V_{IN}, is held 50ns typical after the falling edge of $\overline{ST}$ or ($\overline{CS}$ & $\overline{RD}$). The MSB decision is made approximately 50ns after the second falling edge of the input CLK following a conversion start. If t_1 in Figure 4 is greater than 50ns, then the falling edge of the input CLK will be seen as the first falling clock edge. If t_1 is less than 50ns, the first falling clock edge of the conversion will not occur until one clock cycle later. The succeeding bit decisions are made approximately 50ns after a CLK edge until conversion is complete. At

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the end of conversion, the SAR contents are transferred to the output latch and the SAR is reset in readiness for a new conversion. A single conversion lasts for 8 input clock cycles.

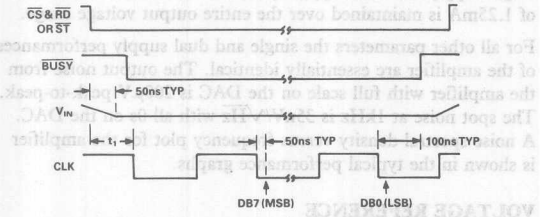
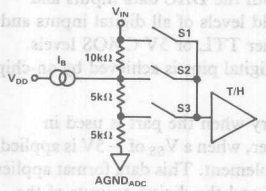


Figure 4. Operating Waveforms Using External Clock

ANALOG INPUT

The analog input of the AD7569/AD7669 feeds into an on-chip track-and-hold amplifier. To accommodate different full-scale ranges, the analog input signal is conditioned by a gain/offset network which conditions all input ranges so that the internal ADC always works with a 0 to +1.25V signal. As a result, the input current on the V_{IN} input varies with the input range selected as shown in Figure 5.



VOLTAGE RANGE	ON SWITCH	I_B
0 TO +1.25V	S1	20μA
0 TO +2.5V	S2	20μA
−1.25V TO +1.25V	S2	140μA
−2.5V TO +2.5V	S3	280μA

Figure 5. Equivalent V_{IN} Circuit

TRACK-AND-HOLD

The track-and-hold (T/H) amplifier on the analog input of the AD7569/AD7669 allows the ADC to accurately convert an input sine wave of 2.5V peak-to-peak amplitude up to a frequency of 200kHz, the Nyquist frequency of the ADC when operated at its maximum throughput rate of 400kHz. This maximum rate of conversion includes conversion time and time between conversions. Because the input bandwidth of the T/H amplifier is much larger than 200kHz, the input signal should be band-limited to avoid converting high-frequency noise components.

The operation of this T/H amplifier is essentially transparent to the user. The T/H amplifier goes from its tracking mode to its hold mode at the start of conversion. This occurs when the ADC receives a conversion start command from either $\overline{ST}$ or $\overline{CS}$ & $\overline{RD}$. At the end of conversion ($\overline{BUSY}$ going high) the T/H reverts back to tracking the input signal.

EXTERNAL CLOCK

The AD7569/AD7669 ADC can be used with its on-chip clock or with an externally applied clock. When using an external clock, the CLK input of the AD7569/AD7669 may be driven directly from 74HC, 4000B series buffers (such as 4049) or from TTL buffers. When conversion is complete, the internal clock is disabled. The external clock can continue to run between conversions without being disabled. The mark/space ratio of the external clock can vary from 70/30 to 30/70.

INTERNAL CLOCK

Clock pulses are generated by the action of an internal current source charging the external capacitor (C_{CLK}) and this external capacitor discharging through the external resistor (R_{CLK}). When a conversion is complete, this internal clock stops operating and the CLK pin goes to the DGND potential. Connections for R_{CLK} and C_{CLK} are shown in the operating diagram of Figure 21. The nominal conversion time versus temperature for the recommended R_{CLK} and C_{CLK} combination is shown in Figure 6. The internal clock provides a convenient clock source for the AD7569/AD7669. Due to process variations, the actual operating frequency for this R_{CLK}/C_{CLK} combination can vary from device to device by up to ±25%.

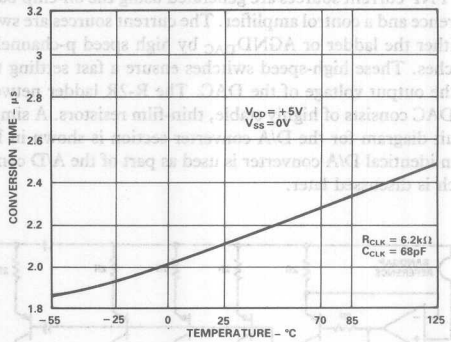


Figure 6. Conversion Time vs. Temperature for Internal Clock Operation

DIGITAL INTERFACE

DAC Timing and Control – AD7569

Table II shows the truth table for DAC operation for the AD7569. The part contains an 8-bit DAC register which is loaded from the data bus under control of $\overline{CS}$ and $\overline{WR}$. The data contained in the DAC register determines the analog output from the DAC. The $\overline{WR}$ input is an edge-triggered input and data is transferred into the DAC register on the rising edge of $\overline{WR}$. Holding $\overline{CS}$ and $\overline{WR}$ low does not make the DAC register transparent.

$\overline{CS}$	$\overline{WR}$	$\overline{RESET}$	DAC Function
H	H	H	DAC Register Unaffected
L	L	H	DAC Register Unaffected
L	↑	H	DAC Register Updated
↑	L	H	DAC Register Updated
X	X	L	DAC Register Loaded with All Zeros

L = Low State H = High State X = Don't Care

Table II. AD7569 DAC Truth Table

The contents of the DAC register are reset to all 0s by an active low pulse on the $\overline{RESET}$ line and for the unipolar output ranges the output remains at 0V after $\overline{RESET}$ returns high. For the bipolar output ranges a low pulse on $\overline{RESET}$ causes the output to go to negative full scale. In unipolar applications the $\overline{RESET}$ line can be used to ensure power-up to 0V on the AD7569 DAC output and is also useful when used as a zero override in system calibration cycles. If the $\overline{RESET}$ input is connected to the system

RESET line, then the DAC output resets to 0V when the entire system is reset. Figure 7 shows the input control logic for the AD7569 DAC and the write cycle timing diagram is shown in Figure 8.

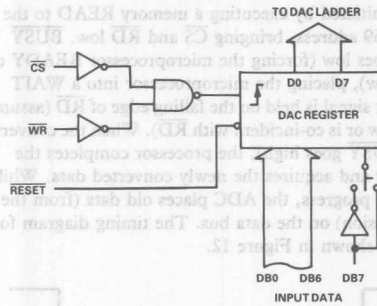


Figure 7. AD7569 DAC Input Control Logic

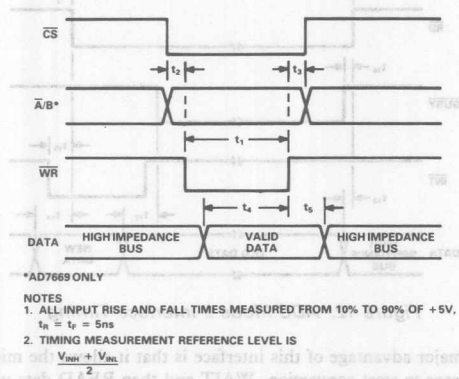


Figure 8. AD7569/AD7669 Write Cycle Timing Diagram

DAC Timing and Control – AD7669

Table III shows the truth table for the dual DAC operation of the AD7669. The part contains two 8-bit DAC registers which are loaded from the data bus under the control of CS, A/B and WR. Address line A/B selects which DAC register the data is loaded to. The data contained in the DAC registers determines the analog output from the respective DACs. The WR input is an edge-triggered input and data is transferred into the selected DAC register on the rising edge of WR. Holding CS and WR low does not make the selected DAC register transparent. The A/B input should not be changed while CS and WR are low.

CS	WR	A/B	RESET	DAC Function
H	H	X	H	DAC Registers Unaffected
L	↑	L	H	DACA Register Updated
↑	L	L	H	DACA Register Updated
L	↑	H	H	DACB Register Updated
↑	L	H	H	DACB Register Updated
X	X	X	L	DAC Registers Loaded with All Zeros

L = Low State H = High State X = Don't Care

Table III. AD7669 DAC Truth Table

The contents of the DAC registers are reset to all 0s by an active low pulse on the RESET line and for the unipolar output ranges the outputs remain at 0V after RESET returns high. For the bipolar output ranges a low pulse on RESET causes the outputs to go to negative full scale. In unipolar applications the RESET line can be used to ensure power-up to 0V on the AD7669 DAC outputs and is also useful when used as a zero override in system calibration cycles. If the RESET input is connected to the system RESET line, then the DAC outputs reset to 0V when the entire system is reset. Figure 9 shows the DAC input control logic for the AD7669, and the write cycle timing diagram is shown in Figure 8.

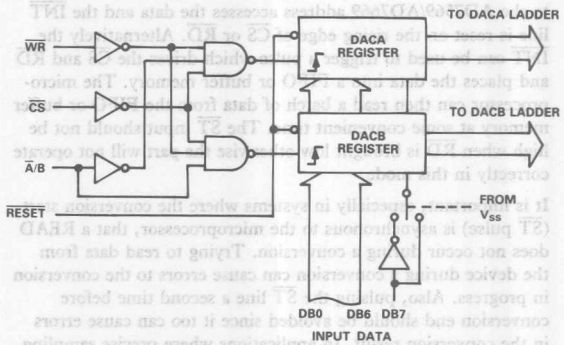


Figure 9. AD7669 DAC Control Logic

ADC Timing and Control

The ADC on the AD7569/AD7669 is capable of two basic operating modes. In the first mode the ST line is used to start conversion and drive the track-and-hold into hold mode. At the end of conversion the track-and-hold returns to its tracking mode. The second mode is achieved by hard-wiring the ST line high. In this case, CS and RD start conversion and the microprocessor is driven into a WAIT state for the duration of conversion by BUSY.

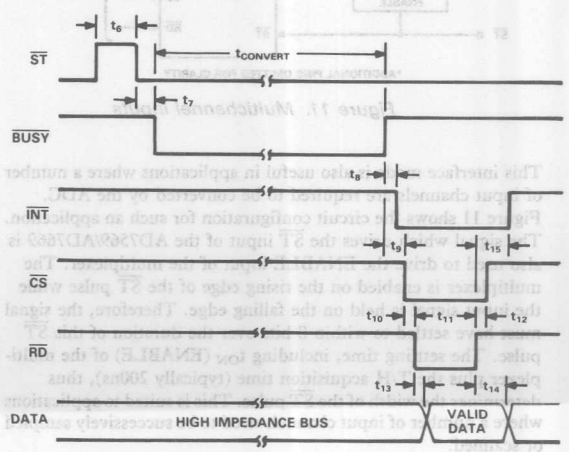


Figure 10. ADC Mode 1 Interface Timing

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The timing diagram for the first mode is shown in Figure 10. It can be used in digital signal processing and other applications where precise sampling in time is required. In these applications it is important that the signal sampling occurs at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. In these cases the $\overline{ST}$ line is driven by a timer or some precise clock source.

The falling edge of the $\overline{ST}$ pulse starts conversion and drives the AD7569/AD7669 track-and-hold amplifier into its hold mode. $\overline{BUSY}$ stays low for the duration of conversion and returns high at the end of conversion and the track-and hold amplifier reverts to its tracking mode on this rising edge of $\overline{BUSY}$. The $\overline{INT}$ line can be used to interrupt the microprocessor. A READ to the AD7569/AD7669 address accesses the data and the $\overline{INT}$ line is reset on the rising edge of $\overline{CS}$ or $\overline{RD}$. Alternatively the $\overline{INT}$ can be used to trigger a pulse which drives the $\overline{CS}$ and $\overline{RD}$ and places the data into a FIFO or buffer memory. The microprocessor can then read a batch of data from the FIFO or buffer memory at some convenient time. The $\overline{ST}$ input should not be high when $\overline{RD}$ is brought low otherwise the part will not operate correctly in this mode.

It is important, especially in systems where the conversion start ($\overline{ST}$ pulse) is asynchronous to the microprocessor, that a READ does not occur during a conversion. Trying to read data from the device during a conversion can cause errors to the conversion in progress. Also, pulsing the $\overline{ST}$ line a second time before conversion end should be avoided since it too can cause errors in the conversion result. In applications where precise sampling is not critical the $\overline{ST}$ pulse can be generated from a microprocessor $\overline{WR}$ or $\overline{RD}$ line gated with a decoded address (different to AD7569/AD7669 $\overline{CS}$ address).

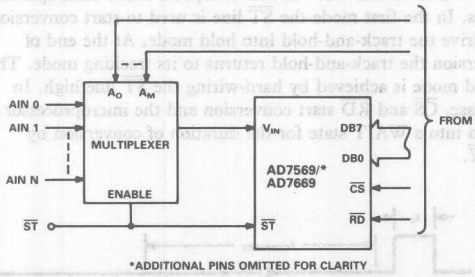


Figure 11. Multichannel Inputs

This interface mode is also useful in applications where a number of input channels are required to be converted by the ADC. Figure 11 shows the circuit configuration for such an application. The signal which drives the $\overline{ST}$ input of the AD7569/AD7669 is also used to drive the ENABLE input of the multiplexer. The multiplexer is enabled on the rising edge of the $\overline{ST}$ pulse while the input signal is held on the falling edge. Therefore, the signal must have settled to within 8 bits over the duration of this $\overline{ST}$ pulse. The settling time, including t_{ON} (ENABLE) of the multiplexer plus the T/H acquisition time (typically 200ns), thus determines the width of the $\overline{ST}$ pulse. This is suited to applications where a number of input channels need to be successively sampled or scanned.

The second interface mode is intended for use with microprocessors which can be forced into a WAIT state for at least 2µs. The $\overline{ST}$ line of the AD7569/AD7669 must be hard-wired high to achieve this mode. The microprocessor starts a conversion and is halted until the result of the conversion is read from the converter. Conversion is initiated by executing a memory READ to the AD7569/AD7669 address, bringing $\overline{CS}$ and $\overline{RD}$ low. $\overline{BUSY}$ subsequently goes low (forcing the microprocessor READY or WAIT input low), placing the microprocessor into a WAIT state. The input signal is held on the falling edge of $\overline{RD}$ (assuming $\overline{CS}$ is already low or is co-incident with $\overline{RD}$). When the conversion is complete ($\overline{BUSY}$ goes high), the processor completes the memory READ and acquires the newly converted data. While conversion is in progress, the ADC places old data (from the previous conversion) on the data bus. The timing diagram for this interface is shown in Figure 12.

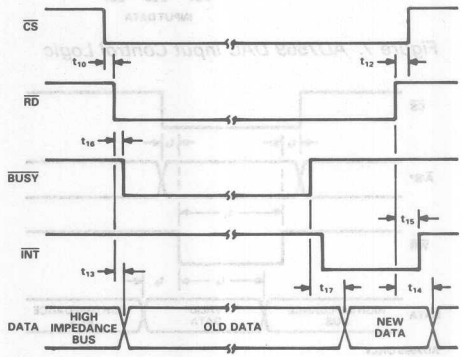


Figure 12. ADC Mode 2 Interface Timing

The major advantage of this interface is that it allows the microprocessor to start conversion, WAIT and then READ data with a single READ instruction. The user does not have to worry about servicing interrupts or ensuring that software delays are long enough to avoid reading during conversion. The fast conversion time of the ADC ensures that for many microprocessors, the processor is not placed in a WAIT state for an excessive amount of time.

DIGITAL SIGNAL PROCESSING APPLICATIONS

In Digital Signal Processing (DSP) application areas like voice recognition, echo cancellation and adaptive filtering, the dynamic characteristics (SNR, Harmonic Distortion, Intermodulation Distortion) of both the ADC and DAC are critical. The AD7569/AD7669 is specified dynamically as well as with standard dc specifications. Because the track/hold amplifier has a wide bandwidth, an anti-aliasing filter should be placed on the V_{IN} input to avoid aliasing of high-frequency noise back into the band of interest.

The dynamic performance of the ADC is evaluated by applying a sine-wave signal of very low distortion to the V_{IN} input which is sampled at a 409.6kHz sampling rate. A Fast Fourier Transform (FFT) plot or Histogram plot is then generated from which SNR, harmonic distortion and dynamic differential nonlinearity data can be obtained. For the DAC, the codes for an ideal sine wave are stored in PROM and loaded down to the DAC. The output spectrum is analyzed, using a spectrum analyzer to evaluate

consisting of pure sine waves at two frequencies is applied to the AD7569/AD7669.

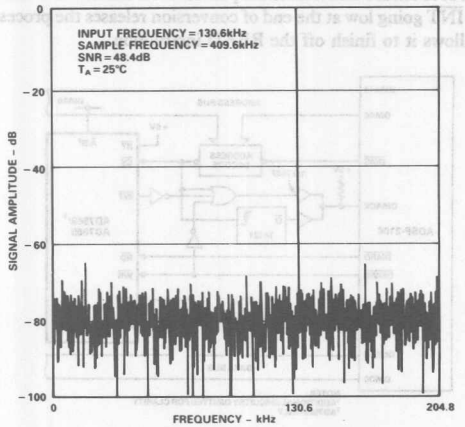


Figure 13. ADC FFT Plot

Figure 13 shows a 2048 point FFT plot of the ADC with an input signal of 130kHz. The SNR is 48.4dB. It can be seen that most of the harmonics are buried in the noise floor. It should be noted that the harmonics are taken into account when calculating the SNR. The relationship between SNR and resolution(N) is expressed by the following equation:

$$SNR = (6.02N + 1.76)dB$$

This is for an ideal part with no differential or integral linearity errors. These errors will cause a degradation in SNR. By working backwards from the above equation, it is possible to get a measure of ADC performance expressed in effective number of bits (N). This effective number of bits is plotted versus frequency in Figure 14. The effective number of bits typically falls between 7.7 and 7.8 corresponding to SNR figures of 48.1 and 48.7dB.

Figure 15 shows a spectrum analyzer plot of the output spectrum from the DAC with an ideal sine-wave table loaded to the data inputs of the DAC. In this case, the SNR is 46dB.

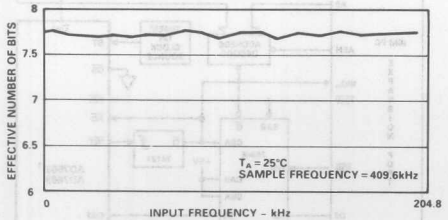


Figure 14. Effective Number of Bits vs. Frequency

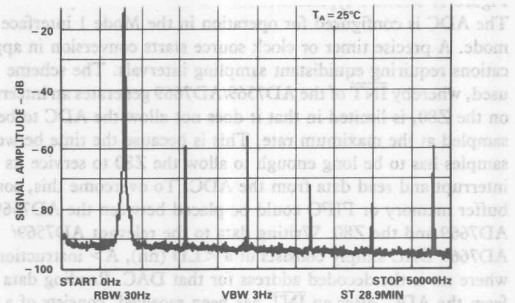


Figure 15. DAC Output Spectrum

HISTOGRAM PLOT

When a sine wave of specified frequency is applied to the V_{IN} input of the AD7569/AD7669 and several thousand samples are taken, it is possible to plot a histogram showing the frequency of occurrence of each of the 256 ADC codes. If a particular step is wider than the ideal 1LSB width, then the code associated with that step will accumulate more counts than for the code for an ideal step. Likewise, a step narrower than ideal width will have fewer counts. Missing codes are easily seen because a missing code means zero counts for a particular code. The absence of large spikes in the plot indicates small differential nonlinearity.

Figure 16 shows a histogram plot for the ADC indicating very small differential nonlinearity and no missing codes for an input frequency of 204kHz. For a sine-wave input, a perfect ADC would produce a cusp probability density function described by the equation

$$p(V) = \frac{1}{\pi (A^2 - V^2)^{1/2}}$$

where A is the peak amplitude of the sine wave and p(V) the probability of occurrence at a voltage V.

The histogram plot of Figure 16 corresponds very well with this cusp shape.

Further typical plots of the performance of the AD7569/AD7669 are shown in the Typical Performance Graphs section of the data sheet.

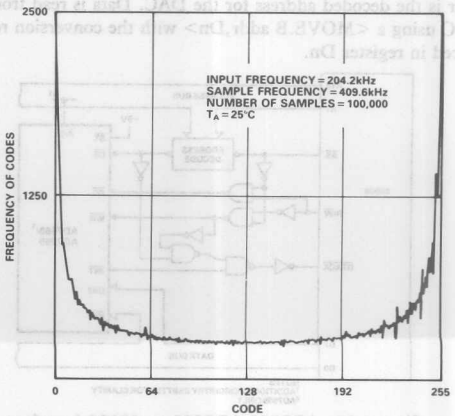


Figure 16. ADC Histogram Plot

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INTERFACING THE AD7569/AD7669

AD7569/AD7669 – Z80 INTERFACE

Figure 17 shows a typical interface to the Z80 microprocessor. The ADC is configured for operation in the Mode 1 interface mode. A precise timer or clock source starts conversion in applications requiring equidistant sampling intervals. The scheme used, whereby $\overline{INT}$ of the AD7569/AD7669 generates an interrupt on the Z80, is limited in that it does not allow the ADC to be sampled at the maximum rate. This is because the time between samples has to be long enough to allow the Z80 to service its interrupt and read data from the ADC. To overcome this, some buffer memory or FIFO could be placed between the AD7569/AD7669 and the Z80. Writing data to the relevant AD7569/AD7669 DAC simply consists of a <LD (nn), A> instruction where nn is the decoded address for that DAC. Reading data from the ADC, after an $\overline{INT}$ has been received, consists of a <LDA, (nn)> instruction.

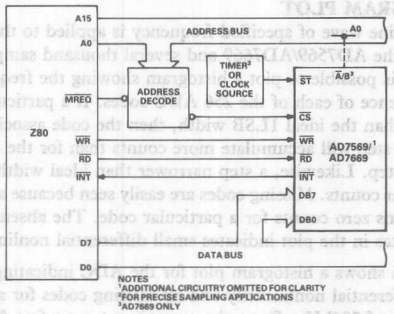


Figure 17. AD7569/AD7669 to Z80 Interface

AD7569/AD7669 – 68008 INTERFACE

A typical interface to the 68008 is shown in Figure 18. In this case the ADC is configured in the Mode 2 interface mode. This means that the one read instruction starts conversion and reads the data. The read cycle is stretched out over the entire conversion period by taking the $\overline{INT}$ line back into the $\overline{DTACK}$ input of the 68008. The additional gates are required so that the 68008 gets a $\overline{DTACK}$ when the processor is writing data to the AD7569/AD7669. In this case there are no wait states introduced into the write cycle. Writing data to the relevant AD7569/AD7669 DAC consists of a <MOVE.B Dn, addr> where Dn is the data register which contains the data to be loaded to that DAC and addr is the decoded address for the DAC. Data is read from the ADC using a <MOVE.B addr,Dn> with the conversion result placed in register Dn.

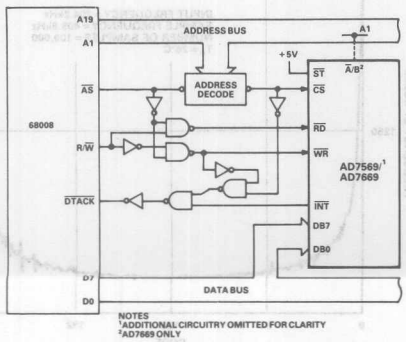


Figure 18. AD7569/AD7669 to 68008 Interface

AD7569/AD7669 – ADSP-2100 INTERFACE

Figure 19 shows a typical interface to the DSP processor, the ADSP-2100. The ADC is in the Mode 2 interface mode which means that the ADSP-2100 is halted during conversion. This is achieved using the decoded address output. This is gated with $\overline{DMWR}$ to ensure that it halts the processor for READ instructions only. $\overline{INT}$ going low at the end of conversion releases the processor and allows it to finish off the READ instruction.

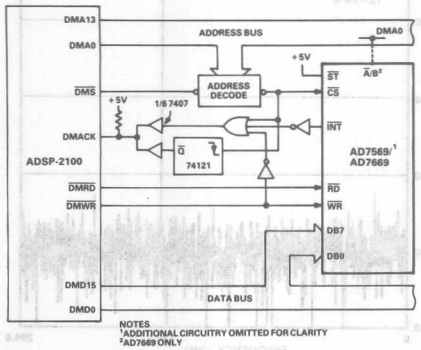


Figure 19. AD7569/AD7669 to ADSP-2100 Interface

Because the instruction cycle of the ADSP-2100 is so fast (125ns cycle) the $\overline{DMWR}$ pulse has to be stretched also for write cycles. This is achieved using the 74121 which generates a pulse which is fed back to DMACK. The duration of this pulse determines how long the ADSP-2100 write cycle is stretched. The buffers which drive the DMACK line must have open-collector outputs. Writing data to the relevant AD7569/AD7669 DAC is achieved using a single instruction, <DM (addr) = MRO> where addr is the decoded address of that DAC and MRO contains the data to be loaded to the DAC register. Data is read from the ADC using a single instruction also, <MRO = DM (addr)>where the conversion result is placed in the MRO data register.

AD7569/AD7669 – IBM PC* INTERFACE

The AD7569/AD7669 is ideal for implementing an analog input/output port for the IBM PC. Figure 20 shows an interface which realizes this function. The ADC is configured in the Mode 1 interface mode and conversions are initiated using a precise clock source for equidistant sampling intervals. At the end of

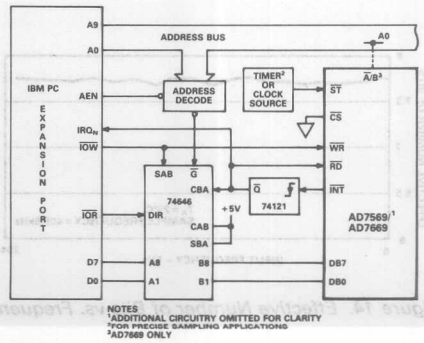


Figure 20. AD7569/AD7669 to IBM PC Interface

*IBM PC is a trademark of International Business Machines Corp.

conversion the $\overline{INT}$ line goes low, and the 74121 generates a $\overline{RD}$ pulse for the AD7569/AD7669. This $\overline{RD}$ pulse accesses data from the ADC and places the conversion result into a register on the 74646. The rising edge of this pulse generates an interrupt request to the processor. The conversion result is read from the 74646 register by performing an I/0 read to the decoded address of the 74646. Writing data to the relevant AD7569/AD7669 DAC involves an I/0 write to the 74646 which transfers the data to the data inputs of the AD7569/AD7669. Data is latched into the selected DAC register on the rising edge of $\overline{IOW}$.

APPLYING THE AD7569/AD7669 DAC

An internal gain/offset network on the AD7569/AD7669 allows several output voltage ranges. The part can produce unipolar output ranges of 0 to +1.25V or 0 to +2.5V and bipolar output ranges of −1.25V to +1.25V or −2.5V to +2.5V. Connections for these various output ranges are outlined below.

UNIPOLAR (0 to +1.25V) CONFIGURATION

The first of the configurations provides an output voltage range of 0 to +1.25V. This is achieved by tying the V_{SS} and RANGE inputs to $AGND_{DAC}$(=0V). Figure 21 shows the configuration of the AD7569 to achieve this output range. A similar configuration of the AD7669 gives the same output range. The table for output voltage versus the digital code in the DAC register is shown in Table IV.

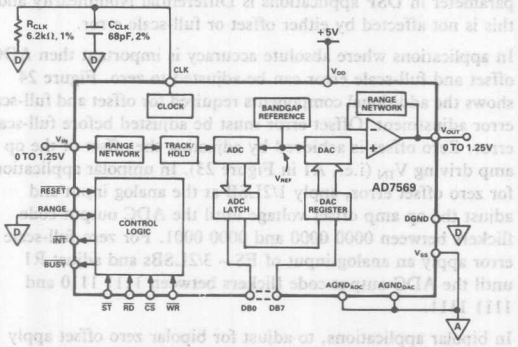


Figure 21. AD7569 Unipolar (0 to +1.25V) Operation

DAC Register Contents MSB	LSB	Analog Output, V_{OUT}
1111	1111	$+V_{REF}\left(\frac{255}{256}\right)$
1000	0001	$+V_{REF}\left(\frac{129}{256}\right)$
1000	0000	$+V_{REF}\left(\frac{128}{256}\right) = +V_{REF}/2$
0111	1111	$+V_{REF}\left(\frac{127}{256}\right)$
0000	0001	$+V_{REF}\left(\frac{1}{256}\right)$
0000	0000	0V

NOTE: 1LSB = $(V_{REF})(2^{-8}) = V_{REF}$ (1/256); V_{REF} = +1.25V Nominal

Table IV. Unipolar (0 to +1.25V) Code Table

UNIPOLAR (0 to +2.5V) CONFIGURATION

The 0 to +2.5V output voltage range is achieved by tying V_{SS} to $AGND_{DAC}$(=0V) and the RANGE input to V_{DD}. The table for output voltage versus digital code is as in Table IV, with $2.V_{REF}$ replacing V_{REF}. Note that for this range

$$1LSB = 2.V_{REF}(2^{-8}) = V_{REF}\frac{1}{128}$$

BIPOLAR (−1.25V to +1.25V) CONFIGURATION

The first of the bipolar configurations is achieved by tying the RANGE input to $AGND_{DAC}$(=0V) and V_{SS} to −5V. The V_{SS} voltage level at which the AD7569/AD7669 changes to bipolar operation is approximately −1V. When the part is configured for bipolar outputs the input coding becomes 2s complement. The table for output voltage versus the digital code in the DAC register is shown in Table V. Note that, as with the unipolar configuration, a digital input code of all 0s produces an output of 0V. It should be noted, however, that a low pulse on the $\overline{RESET}$ line for the bipolar ranges sets the ouput voltage to negative full scale.

DAC Register Contents MSB	LSB	Analog Output, V_{OUT}
0111	1111	$+V_{REF}\left(\frac{127}{128}\right)$
0000	0001	$+V_{REF}\left(\frac{1}{128}\right)$
0000	0000	0V
1111	1111	$-V_{REF}\left(\frac{1}{128}\right)$
1000	0001	$-V_{REF}\left(\frac{127}{128}\right)$
1000	0000	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

NOTE: 1LSB = $(V_{REF})(2^{-7}) = V_{REF}$ (1/128)

Table V. Bipolar (−1.25V to +1.25V) Code Table

BIPOLAR (−2.5V to +2.5V) CONFIGURATION

The −2.5V to +2.5V bipolar output range is achieved by tying the RANGE input to V_{DD} and the V_{SS} input to −5V. Once again, the input coding is 2s complement. The table for output voltage versus digital code is as in Table V with $2.V_{REF}$ replacing V_{REF}. Note that for this range

$$1LSB = 4.V_{REF}(2^{-8}) = V_{REF}\frac{1}{64}$$

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The analog input on the AD7569/AD7669 accepts the same four input ranges as the output ranges on the DAC. Whatever output range is selected for the DAC also applies to the input range of the ADC.

Although separate AGNDs exist for both the DAC and ADC to minimize crosstalk, writing data to the DAC while the ADC is performing a conversion may result in an incorrect conversion from the ADC due to an interaction of currents between the DAC and ADC. Therefore, to ensure correct operation of the ADC, the DAC register should not be updated while the ADC is converting.

UNIPOLAR OPERATION

The circuit of Figure 21 shows the AD7569 configured for both an input and output range of 0 to +1.25V (the AD7669 configuration is similar). The nominal transfer characteristic for this range is shown in Figure 22. The output code is Natural Binary with 1LSB = (1.25/256)V = 4.88mV.

As before, to achieve the unipolar 0 to +2.5V input range V_{SS} is connected to 0V and the RANGE input is tied to a logic high. The nominal transfer characteristic is as in Figure 22 but in this case ILSB = (2.5/256)V = 9.76mV.

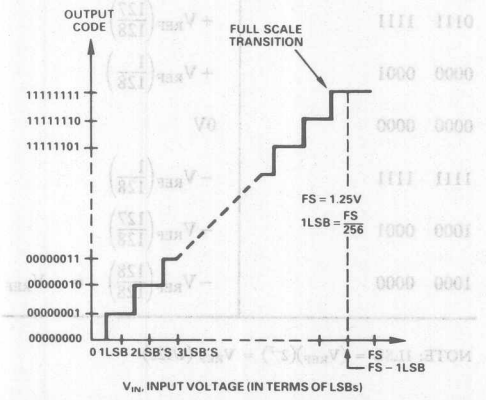


Figure 22. Nominal Transfer Characteristic for Unipolar (0 to +1.25V) Operation

BIPOLAR OPERATION

The analog input of the AD7569/AD7669 ADC is configured for bipolar inputs when V_{SS} = −5V. The output code provided by the part is 2s complement. Figure 23 shows the transfer function for bipolar (−1.25V to +1.25V) operation. The LSB size for this range is (2.5/256)V = 9.76mV.

The transfer function for the −2.5V to +2.5V range is identical to that of Figure 23 but now FS = 5V and the LSB size is (5/256)V = 19.5mV.

ADC OFFSET AND FULL-SCALE ERROR ADJUSTMENT

In most Digital Signal Processing (DSP) applications, offset and full-scale error have little or no effect on system performance. A

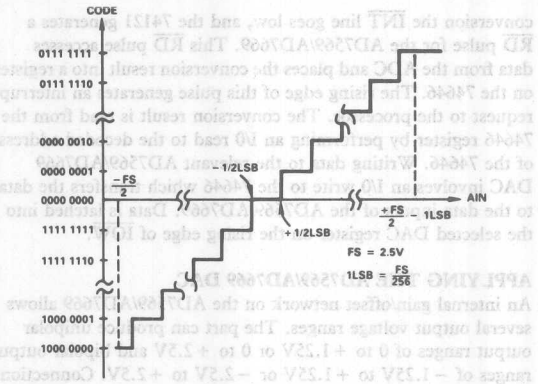


Figure 23. Nominal Transfer Characteristic for Bipolar (−1.25V to +1.25V) Operation

typical example is a digital filter, where an ac analog signal is quantized by the ADC, digitally processed and recreated using the DAC. In these type of applications the offset error can be eliminated by ac coupling the recreated signal. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. An important parameter in DSP applications is Differential Nonlinearity and this is not affected by either offset or full-scale error.

In applications where absolute accuracy is important then ADC offset and full-scale error can be adjusted to zero. Figure 24 shows the additional components required for offset and full-scale error adjustment. Offset error must be adjusted before full-scale error. Zero offset is achieved by adjusting the offset of the op amp driving V_{IN} (i.e., A1 in Figure 23). In unipolar applications, for zero offset error, apply 1/2LSB at the analog input and adjust the op amp offset voltage until the ADC output code flickers between 0000 0000 and 0000 0001. For zero full-scale error apply an analog input of FS – 3/2LSBs and adjust R1 until the ADC output code flickers between 1111 1110 and 1111 1111.

In bipolar applications, to adjust for bipolar zero offset apply −1/2LSB at the analog input and adjust the op amp offset voltage until the output code flickers between 1111 1111 and 0000 0000. For zero full-scale error apply +FS/2 – 3/2LSB at the analog input and adjust R1 until the ADC output code flickers between 01111110 and 0111 1111.

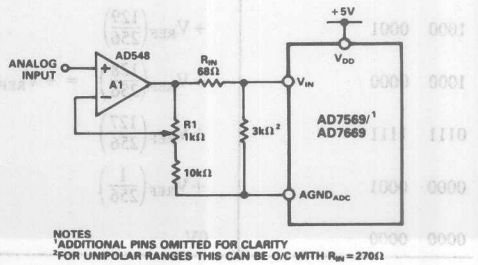


Figure 24. ADC Error Adjust Circuit

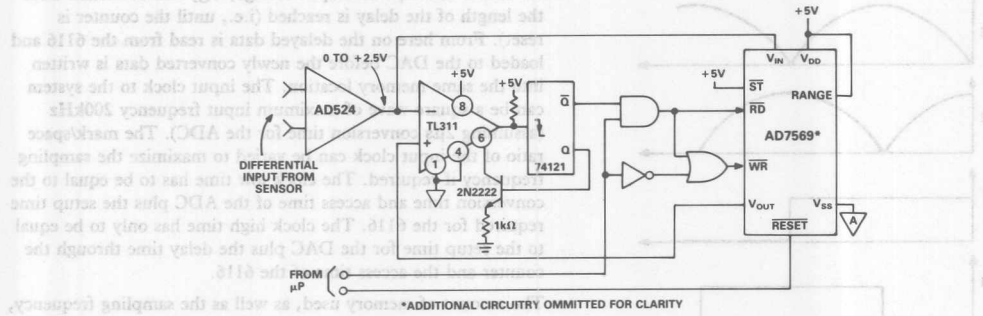


Figure 25. Peak-Reading A/D Converter

PEAK DETECTION – AD7569

The circuit of Figure 25 shows a peak-reading A/D converter which is useful in such applications as monitoring flow rates, temperature, pressure, etc. The circuit ensures that a peak will not be missed while at the same time does not require the microprocessor to frequently monitor the data. The peak value is stored in the A/D converter and can be read at any time.

The gain on the AD524 is adjusted to yield a 0 to +2.5V output. When the input signal exceeds the current stored value, the output of the TL311 goes low, triggering the $\overline{Q}$ output of the 74121. This low-going pulse starts a conversion on the AD7569 ADC and at the end of conversion latches the result into the DAC. This pulse must be at least 120ns greater than the conversion time of the ADC. The Q output is used to drive the strobe input of the TL311, resetting the TL311 output high in readiness for another conversion.

The additional gates on the $\overline{RD}$ and $\overline{WR}$ inputs are to allow the data to be read by the microprocessor while at the same time ensuring that the DAC is not updated when the microprocessor reads the data. It may be necessary to monitor the AD7569 $\overline{BUSY}$ line to ensure that a processor READ is not attempted while the AD7569 is in the middle of a conversion. The READ pulse width from the processor must be less than 1μs to ensure correct data is read from the ADC. A low-going pulse on the $\overline{RESET}$ line resets the DAC output to 0V and starts a new "peak-detection" period. This $\overline{RESET}$ pulse must also be less than 1μs.

DISK DRIVE APPLICATION – AD7669

Closed-Loop Microstepping

Microstepping is a popular technique in low density disk drives (both floppy and hard disk) which allows higher positional resolution of the disk drive head over that obtainable from a full-step driven stepper motor. Typically, a two-phase stepper motor has its phase currents driven with a sine-cosine relationship. These cosinusoidal signals are generated by two DACs driven with the appropriate data. The resolution of the DACs determines the number of microsteps into which each full step can be divided. For example, with a 1.8° full-step motor and a 4-bit DAC, a microstep size of 0.11° (1.8°/(2^n) is obtainable.

The microstepping technique improves the positioning resolution possible in any control application. However, the positional accuracy can be significantly worse than that offered by the original full-step accuracy specification due to load torque effects. To ensure that the increased resolution is useable, it is therefore necessary to use a closed-loop system where the position of the disk drive head (or motor) is monitored. The closed-loop system allows an error between the desired position and the actual position to be monitored and corrected. The correction is achieved by adjusting the ratio of the phase currents in the motor windings until the required head position is reached.

The AD7669 is ideally suited for the closed-loop microstepping technique with its on-chip dual DACs for positioning the disk drive head and on-board ADC for monitoring the position of the head. A generalized circuit for a closed-loop microstepping system is shown in Figure 26. The DAC waveforms are shown in Figure 27 along with the direction information for clockwise rotation supplied by the controller.

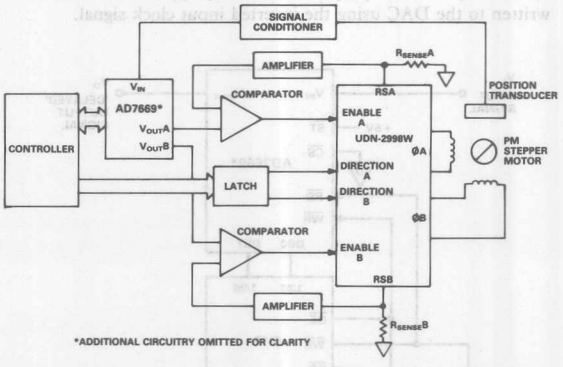


Figure 26. Typical Closed-Loop Microstepping Circuit with the AD7669

The AD7669 is used in the unipolar 0 to +2.5V configuration. This allows the circuit of Figure 26 to be completely unipolar (+5V, +12V supplies); no negative power supplies are required. The power output stage is a dual H-Bridge device such as the UDN-2998W from Sprague Electric. The phase currents in both windings are detected by means of the small value sense resistors, R_SA and R_SB, in series with the windings. The voltage developed across these resistors is amplified and compared with the respective DAC output voltage. The comparators in turn chop the phase winding current. The ADC completes the feedback path by converting information from a suitable transducer for analysis by the controller.

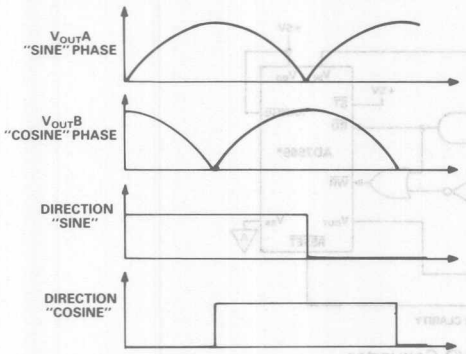


Figure 27. Typical DAC Output Voltages for Microstepping and Direction Signals for Clockwise Rotation with the UDN-2998W

ANALOG DELAY LINE – AD7569

In many applications, especially in audio systems, it is necessary to provide a delay on the input signal. The circuit of Figure 28 shows how a simple analog delay line can be implemented based on the AD7569. The input signal is sampled using the AD7569 ADC and converted data is loaded into the 6116 (2K × 8 static ram). The inverted input clock drives a counter which selects the address for the 6116. The delay is selected by choosing one of the output lines of the HCT4040 counter to reset the counter. This can be done using a simple switch in a manual system or by a multiplexer in a programmable delay application. Data is written to the DAC using the inverted input clock signal.

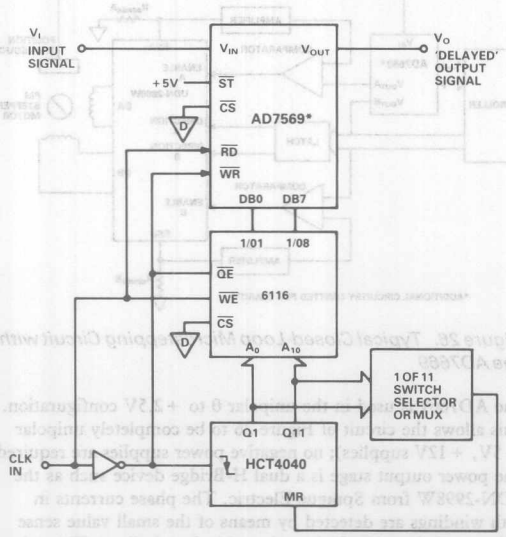


Figure 28. Analog Delay Line

On initial start-up the output voltage, V_O, will be invalid until the length of the delay is reached (i.e., until the counter is reset). From here on the delayed data is read from the 6116 and loaded to the DAC before the newly converted data is written into the same memory location. The input clock to the system can be a square wave of maximum input frequency 200kHz (assuming 2μs conversion time for the ADC). The mark/space ratio of the input clock can be varied to maximize the sampling frequency if required. The clock low time has to be equal to the conversion time and access time of the ADC plus the setup time required for the 6116. The clock high time has only to be equal to the setup time for the DAC plus the delay time through the counter and the access time of the 6116.

The amount of memory used, as well as the sampling frequency, determines the maximum possible delay. Using the HCT4040 and the 6116 with an input clock frequency of 200kHz, the maximum delay is 5ms on a maximum input frequency of 100kHz. Using 64K memory, with an 8kHz input clock frequency the maximum delay is 8 seconds on a maximum input frequency of 4kHz.

TRANSIENT RECORDER – AD7569

The scheme just outlined can also form the basis for a transient recorder. In this case transients on the input signal are converted and stored in memory. The transient can then be recalled from memory at a later time and the transient waveform can be recreated using the AD7569 DAC.

INFINITE SAMPLE-AND-HOLD – AD7569

The AD7569 is ideal for implementing a single-chip infinite sample-and-hold function. Basically, the ADC samples and converts the input signal into an 8-bit digital word. The 8 bits of data are then loaded to the DAC and the sampled value is restored to analog form. The sampled value is held until the DAC register is updated. The full-scale matching between the ADC and the DAC on the AD7569 ensures a typical error of less than 1% between the analog input voltage and the "held" output voltage. Figure 29 shows the connections required on the AD7569 to achieve this infinite sample-and-hold function.

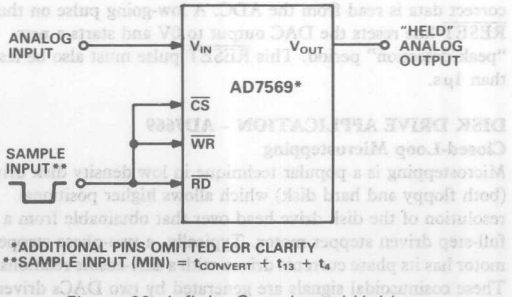


Figure 29. Infinite Sample-and-Hold

TARE FUNCTION FOR WEIGH SCALE – AD7569

The infinite sample-and-hold just outlined can also form the basis of a circuit to provide a tare function for a weigh scale system. Figure 30 shows a circuit for a weigh scale system. It incorporates a tare function using a simple circuit based on the AD7569.

The AD587 along with the 2N6285 provides a buffered +10V reference to supply the low impedance load cell transducer. The load cell output is amplified by the AD624 precision instrumentation amplifier with gain adjustment provided by R1. The output of the AD624 is applied to the noninverting input of a unity gain differential summing amplifier which uses the AD707, a high precision op amp with low drift. The AD707 feeds a 3 1/2 digit panel meter module which converts the signal for digital readout. The input signal to the panel meter is also applied to the analog input of the AD7569 for the tare function. When the tare switch (S1) is closed, a tare cycle commences and V_{IN} is sampled and held infinitely at V_{OUT} until the next tare cycle. V_{OUT} drives the inverting input of the differential amplifier and forces its output to zero. Thus, the tare function is used to give a readout of zero for any undesired weight, such as a box, when only the item placed in it is to be weighed. The tare function can also be used in calibrating the system, to cancel out offset errors due to the load cell, AD624 and differential amplifier.

The AD7569 offers many advantages in the system outlined, such as: simple, low cost circuit – no need for microprocessor, software, etc. – and low power consumption.

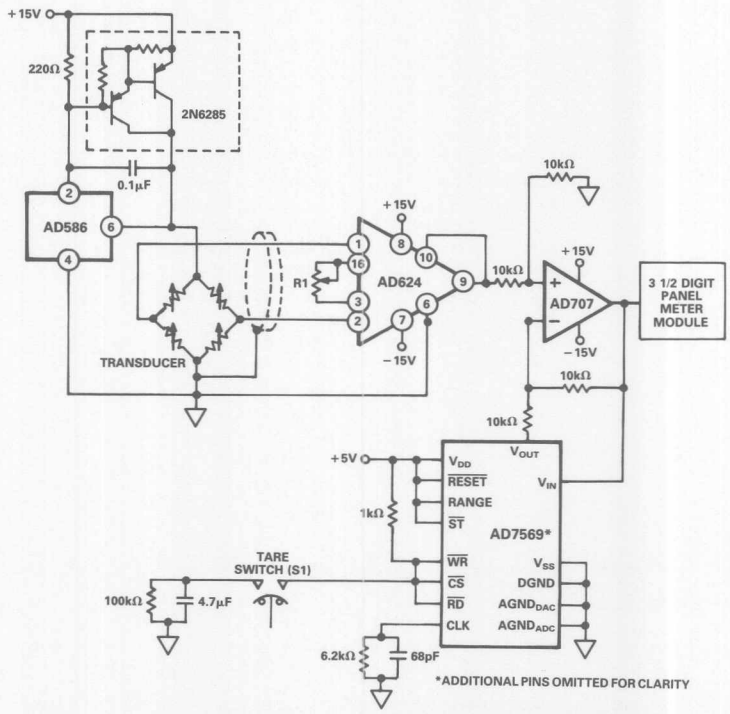
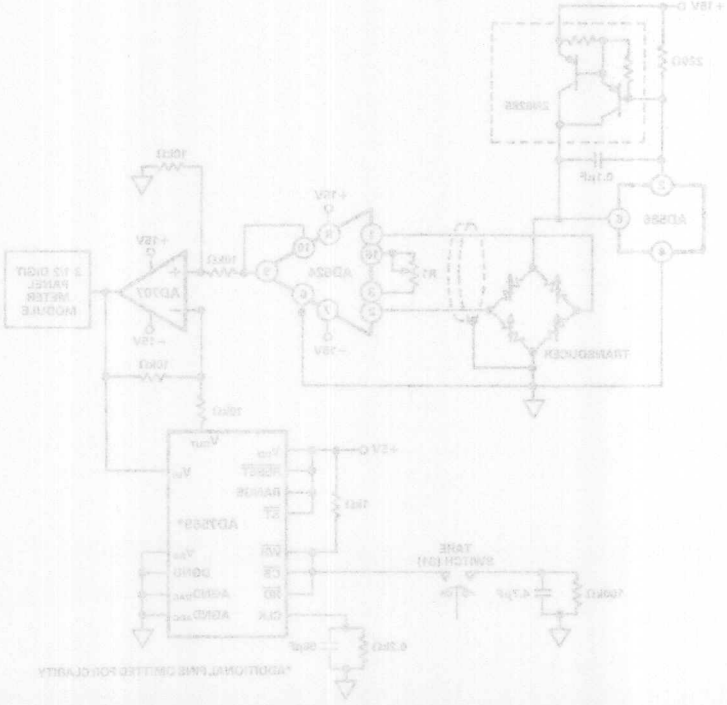


Figure 30. Weigh Scale System with Tare Function

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LC²MOS Analog I/O Port

AD7769*

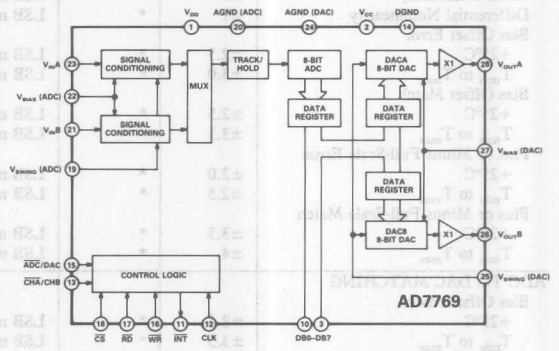
FEATURES

Two-Channel, 8-Bit 2.5 μs ADC
Two 8-Bit, 2.5 μs DACs with Output Amplifiers
Span and Offset of ADC and DAC
Independently Adjustable
Low Power

APPLICATIONS

Winchester Disk Servo Controllers
Floppy Disk Microstepping
Closed Loop Servo Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7769 is a complete, two-channel, 8-bit, analog I/O port. It has versatile input and output signal conditioning features that make it ideal for use in head-positioning servos in Winchester disk systems. It is equally suitable for floppy disk microstepping head positioning, other closed loop digital servo systems and general purpose 8-bit data acquisition.

The AD7769 contains a high speed successive approximation ADC, preceded by a two-channel multiplexer and signal conditioning circuits. The input span of the ADC and the offset of the zero point from ground can be independently set by applying ground referenced voltages. The AD7769 also contains two independent, fast settling, 8-bit DACs with output amplifiers. The output span and offset voltage of the DACs can be set independently of those of the ADC. This makes the AD7769 especially useful in disk drives, where only a positive supply rail is available and the ranges of the ADC and DACs must be referenced to some positive voltage less than the supply.

The AD7769 is easily interfaced to a standard 8-bit mpu bus via an 8-bit data port and standard microprocessor control lines.

The AD7769 is fabricated in Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 28-pin plastic DIP and 28-terminal PLCC package.

*Covered by U.S. Patent No. 4,990,916.

PRODUCT HIGHLIGHTS

1. Two-Channel, 8-Bit Analog I/O port on a Single Chip.
   The AD7769 contains a two-channel, high speed ADC with input signal conditioning and two, fast settling 8-bit DACs with output amplifiers, on a single chip.
2. Independent Control of Span and Offset.
   The input voltage span of the ADC and the midpoint of the transfer function, the output voltage swing of the two DACs and the half-scale output voltage, can be set independently by applying ground referenced control voltages.
3. Dynamic Specifications for DSP Users.
   In addition to the traditional ADC and DAC specifications, the AD7769 is specified with ac parameters including signal-to-noise ratio, distortion and signal bandwidth.
4. Fast Microprocessor Interface.
   The AD7669 has bus interface timing compatible with all modern microprocessors, with bus access and relinquish times less than 65 ns and a Write pulse width less than 90 ns.

8

AD7769—SPECIFICATIONS

ADC SPECIFICATIONS

(V_{DD} = +12 V ±10%; V_{CC} = +5 V ±5%; AGND [ADC] = AGND [DAC] = DGND = 0 V; V_{BIAS} [ADC] = +5 V; V_{SWING} [ADC] = +2.5 V; f_{CLK} = 5 MHz external. All specifications T_{min} to T_{max}[1] unless otherwise stated.)

Parameter	J Version	A Version	Units	Conditions/Comments
DC ACCURACY				
Resolution	8	*	Bits	
Relative Accuracy	±1	*	LSB max	See Terminology
Differential Nonlinearity	±1	*	LSB max	No Missing Codes. See Terminology.
Bias Offset Error				See Terminology
+25°C	±2.5	*	LSB max	
T_{min} to T_{max}	±3.0	*	LSB max	
Bias Offset Match				Channel A to Channel B
+25°C	±2.5	*	LSB max	
T_{min} to T_{max}	±3.5	*	LSB max	
Plus or Minus Full-Scale Error				See Terminology
+25°C	±2.0	*	LSB max	
T_{min} to T_{max}	±2.5	*	LSB max	
Plus or Minus Full-Scale Match				Channel A to Channel B
+25°C	±3.5	*	LSB max	
T_{min} to T_{max}	±4	*	LSB max	
ADC TO DAC MATCHING				Channel A/B to V_{OUT} A/B
Bias Offset Match				V_{BIAS} (DAC) = +5 V, V_{SWING} (DAC) = +2.5 V.
+25°C	±2.5	*	LSB max	
T_{min} to T_{max}	±3.5	*	LSB max	
Plus or Minus Full-Scale Match				
+25°C	±3.5	*	LSB max	
T_{min} to T_{max}	±4.0	*	LSB max	
DYNAMIC PERFORMANCE[2]				
Signal-to-Noise Ratio (SNR)	44	*	dB min	V_{IN} = 100 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 400 kHz
Total Harmonic Distortion (THD)	48	*	dB max	V_{IN} = 100 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 400 kHz
Intermodulation Distortion (IMD)	60	*	dB typ	f_a = 99 kHz, f_b = 96.7 kHz with $f_{SAMPLING}$ = 400 kHz
Frequency Response	0.1	*	dB typ	V_{IN} = Full-Scale, dc to 200 kHz Sine Wave
ANALOG INPUTS				
Input Voltage Ranges, $V_{IN}A$, $V_{IN}B$	V_{BIAS} − V_{SWING} or 0		V min	Whichever Is the Higher
	V_{BIAS} + V_{SWING} or 9.8		V max	Whichever Is the Lower
Input Currents, $I_{IN}A$, $I_{IN}B$	±0.4	*	mA max	
ADC REFERENCE INPUTS				
Input Voltage Levels				
V_{BIAS} (ADC)	2/6.8	*	V min/max	With Respect to AGND (ADC). For Specified Performance.
V_{SWING} (ADC)	2.0/3.0	*	V min/max	With Respect to AGND (ADC). For Specified Performance.
Input Currents				
V_{BIAS} (ADC) Input	±800	*	µA max	
V_{SWING} (ADC) Input	±1	*	µA max	
LOGIC OUTPUTS				
DB0–DB7, $\overline{INT}$				
V_{OL}, Output Low Voltage	0.4	*	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	4.0	*	V min	I_{SOURCE} = 200 µA
DB0–DB7				
Floating State Leakage Current	±10	*	µA max	
Floating State Capacitance[2]	10	*	pF max	
Output Coding	Offset Binary			
POWER REQUIREMENTS				
V_{CC} Range	4.75/5.25	*	V min/Vmax	For Specified Performance. The Part Will Function with V_{CC} = 5 V ±10% with Degraded Performance.
V_{DD} Range	10.8/13.2	*	V min/V max	For Specified Performance
I_{DD} @ +25°C	20	*	mA max	For ADC and DAC: V_{BIAS} = 5.0 V; V_{SWING} = 3.0 V; $V_{IN}A$,
$V_{UB}Am$ $V_{IN}B$ = T_{min} to T_{max}	22	*	mA max	V_{BIAS}; DAC Code = FF (Hex); DACA and DACB Load = 5 kΩ to AGND (DAC). Typically I_{DD} = 14 mA.
I_{CC} @ +25°C	5	*	mA max	Logic Inputs = 2.4 V, CLK Input = 0.8 V. Typically I_{CC} =
T_{min} to T_{max}	6	*	mA max	1.5 mA.

NOTES

[1]Temperature range as follows: J Version: 0 to +70°C; A Version: −40°C to +85°C.

[2]Sample tested at +25°C to ensure compliance.

*Specification same as J Version.

Specifications subject to change without notice.

DACA, DACB SPECIFICATIONS

(V_{DD} = +12 V ±10%; V_{CC} = +5 V ±5%; AGND [DAC] = AGND [ADC] = DGND = 0 V; V_{BIAS} [DAC] = +5 V; V_{SWING} [DAC] = +2.5 V; V_{OUT}A, V_{OUT}B load to AGND [DAC], R_L = 5 kΩ, C_L = 100 pF. All specifications T_{min} to T_{max}[1] unless otherwise stated.)

Parameter	J Version	A Version	Units	Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	*	Bits	
Relative Accuracy	±1	*	LSB max	See Terminology
Differential Nonlinearity	±1	*	LSB max	Guaranteed Monotonic. See Terminology.
Bias Offset Error				See Terminology
+25°C	±2.0	*	LSB max	
T_{min} to T_{max}	±2.5	*	LSB max	
Bias Offset Match				V_{OUT} A to V_{OUT} B
+25°C	±2.5	*	LSB max	
T_{min} to T_{max}	±3.5	*	LSB max	
Plus or Minus Full-Scale Error				See Terminology
+25°C	±1.5	*	LSB max	
T_{min} to T_{max}	±2.0	*	LSB max	
Plus or Minus Full-Scale Match				V_{OUT} A to V_{OUT} B
+25°C	±3.5	*	LSB max	
T_{min} to T_{max}	±4.0	*	LSB max	
ADC to DAC MATCHING	As Per ADC Specifications			
DYNAMIC PERFORMANCE[2]				
Signal-to-Noise Ratio (SNR)	44	*	dB min	V_{OUT} = 20 kHz Full-Scale Sine Wave With $f_{SAMPLING}$ = 400 kHz
Total Harmonic Distortion (THD)	48	*	dB max	V_{OUT} = 20 kHz Full-Scale Sine Wave With $f_{SAMPLING}$ = 400 kHz
Intermodulation Distortion (IMD)	55	*	dB typ	f_a = 18.4 kHz, f_b = 14.5 kHz with $f_{SAMPLING}$ = 400 kHz
ANALOG OUTPUTS				
Output Voltage Ranges				
V_{OUT}A, V_{OUT}B	$V_{BIAS} - V_{SWING}$ or 0.5		V min	Whichever Is the Higher
	$V_{BIAS} + V_{SWING}$ or V_{DD} −2.0		V max	Whichever Is the Lower
DC Output Impedance	0.5	*	Ω typ	
Short-Circuit Current	20	*	mA typ	
DAC REFERENCE INPUTS				
Input Voltage Levels				
V_{BIAS} (DAC)	3/6.8	*	V min/max	With Respect to AGND (DAC). For Specified Performance.
V_{SWING} (DAC)	2.0/3.0	*	V min/max	With Respect to AGND (DAC). For Specified Performance.
Input Currents				
V_{BIAS} (DAC) Input	±2	*	µA max	
V_{SWING} (DAC) Input	±1	*	µA max	
AC CHARACTERISTICS[2]				
Voltage Output Settling Time	4	*	µs max	Settling Time to Within ±1/2 LSB of Final Value. Typically 2.5 µs.
Digital-to-Analog Glitch Impulse	30	*	nV sec typ	See Terminology
Digital Feedthrough	1	*	nV sec typ	See Terminology
LOGIC INPUTS				
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, ADC/$\overline{DAC}$, CHA/$\overline{CHB}$, DB0–DB7				
Input Low Voltage, V_{INL}	0.8	*	V max	
Input High Voltage, V_{INH}	2.4	*	V min	
Input Leakage Current	±10	*	µA max	
Input Capacitance	10	*	pF max	
CLK				
Input Low Voltage	0.8	*	V max	External Clock. For Internal Clock Operation Connect
Input High Voltage	2.4	*	V min	the CLK Pin to V_{DD}.
Input Leakage Current	±10	*	µA max	
DB0–DB7				
Input Coding	Offset Binary			
POWER REQUIREMENTS	As per ADC Specifications			

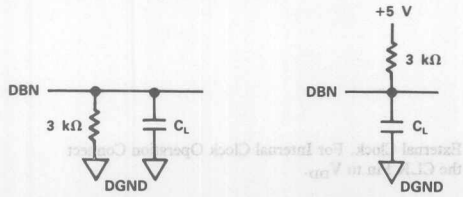
NOTES
[1]Temperature range as follows: J Version: 0 to +70°C; A Version: −40°C to +85°C.
[2]Sample tested at +25°C to ensure compliance.
*Specifications same as J Version.
Specifications subject to change without notice.

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TIMING CHARACTERISTICS[1, 2] (V_{CC} = +5 V ±5%; V_{DD} = +12 V ±10%; AGND [ADC] = AGND [DAC] = DGND = 0 V. For ADC and DAC, V_{BIAS} = +5 V, V_{SWING} = +2.5 V.)

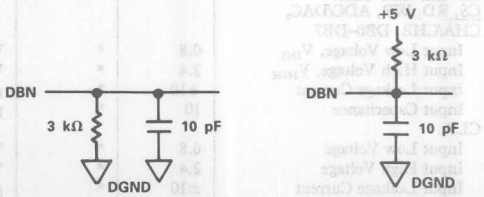
Parameter	Label	Limit at +25°C	Limit at T_{min}, T_{max}	Units	Test Conditions/Comments
ADC/DAC CONTROL TIMING					
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_1	0	0	ns min	
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_2	0	0	ns min	
$\overline{ADC}$/DAC to $\overline{WR}$ Setup Time	t_3	0	0	ns	
$\overline{ADC}$/DAC to $\overline{WR}$ Hold Time	t_4	0	0	ns min	
$\overline{CHA}$/CHB to $\overline{WR}$ Setup Time	t_5	0	0	ns min	
$\overline{CHA}$/CHB to $\overline{WR}$ Hold Time	t_6	0	0	ns min	
$\overline{WR}$ Pulse Width	t_7	80	80	ns min	
ADC CONVERSION TIMING					
Using External Clock					Load Circuit of Figure 3, C_L = 20 pF
$\overline{WR}$ to $\overline{INT}$ Low Delay	t_8	2.6	2.6	µs max	
Using Internal Clock					Load Circuit of Figure 3, C_L = 20 pF
$\overline{WR}$ to $\overline{INT}$ Low Delay	t_8	1.9/3.0	1.9/3.0	µs min/max	Typically 2.5 µs
$\overline{WR}$ to $\overline{INT}$ High Delay	t_9	85	85	ns max	Load Circuit of Figure 3, C_L = 20 pF
	t_9	120	120	ns max	Load Circuit of Figure 3, C_L = 100 pF
$\overline{WR}$ to Data Valid Delay[3]	t_{10}	t_8+70	t_8+70	ns max	Load Circuit of Figure 1, C_L = 20 pF
	t_{10}	t_8+110	t_8+110	ns max	Load Circuit of Figure 1, C_L = 100 pF
ADC READ TIMING					
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{11}	0	0	ns min	
$\overline{CS}$ to $\overline{RD}$ Hold Mode	t_{12}	0	0	ns min	
$\overline{RD}$ to Data Valid Delay[3]	t_{13}	15/65	15/65	ns min/max	Load Circuit of Figure 1, C_L = 20 pF
	t_{13}	30/100	30/100	ns min/max	Load Circuit of Figure 1, C_L = 100 pF
Bus Relinquish Time after $\overline{RD}$ High[4]	t_{14}	15/65	15/65	ns min/max	Load Circuit of Figure 2
$\overline{RD}$ to $\overline{INT}$ High Delay	t_{15}	80	80	ns max	Load Circuit of Figure 3, C_L = 20 pF
	t_{15}	110	110	ns max	Load Circuit of Figure 3, C_L = 100 pF
$\overline{RD}$ Pulse Width	t_{16}	t_{13}	t_{13}	ns min	Determined by t_{13}
DAC WRITE TIMING					
Data Valid to $\overline{WR}$ Setup Time	t_{17}	65	65	ns min	
Data Valid to $\overline{WR}$ Hold Time	t_{18}	15	20	ns min	
$\overline{WR}$ to DAC Output Settling Time	t_{19}	4	4	µs max	Load Circuit of Figure 4

NOTES
[1]See Figures 11, 12 and 13.
[2]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[3]t_{10} and t_{13} are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[4]t_{14} is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.



a. High-Z to V_{OH} b. High-Z to V_{OL}

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High-Z b. V_{OL} to High-Z

Figure 2. Load Circuits for Bus Relinquish Time Test

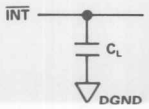


Figure 3. Load Circuit for $\overline{RD}$ and $\overline{WR}$ to $\overline{INT}$ Delay Test

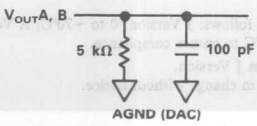


Figure 4. Load Circuit for DAC Settling Time Test

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND or DGND . . . . . −0.3 V, +15 V
V_{CC} to DGND . . . . . −0.3 V, V_{DD} +0.3 V or 7 V (Whichever is Lower)
AGND to DGND . . . . . −0.3 V, V_{DD} +0.3 V
Digital Inputs to DGND (Pins 12, 13, 15–18) . . . . . −0.3 V, V_{DD} +0.3 V
Digital Outputs to DGND (Pins 3–10, 11) . . . . . −0.3 V, V_{CC} +0.3 V
Analog Inputs to AGND . . . . . −0.3 V, V_{DD} +0.3 V
Analog Outputs to AGND . . . . . −0.3 V, V_{DD} +0.3 V
Operating Temperature Range
Commercial (J Version) . . . . . 0 to +70°C
Industrial (A Version) . . . . . −40°C to +85°C
Power Dissipation (Any Package) to +75°C . . . . . 500 mW
Derates Above +75°C by . . . . . 6 mW/°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering 10 secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



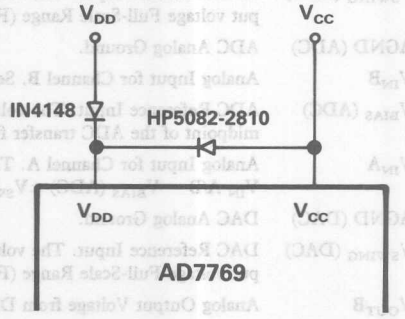
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7769JN	0°C to +70°C	N-28
AD7769JP	0°C to +70°C	P-28A
AD7769AN	−40°C to +85°C	N-28
AD7769AP	−40°C to +85°C	P-28A

*N = Plastic DIP; P = Plastic Leaded Chip Carrier. For package outline information see Package Information section.

NOTE

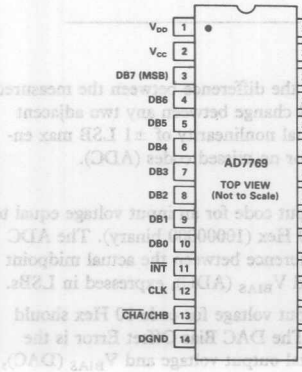
Do not allow V_{CC} to exceed V_{DD} by more than 0.3 V. In cases where this can happen the diode protection scheme shown below is recommended.



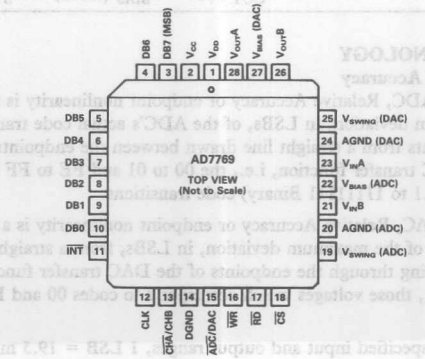
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PIN CONFIGURATION

DIP



PLCC



Pin	Mnemonic	Description
1	V_{DD}	+12 V Power Supply. This powers the analog circuitry.
2	V_{CC}	+5 V Power Supply. This powers the logic circuitry.
3–10	DB7–DB0	Input/Output Data Bus. A bidirectional data port from which ADC output data may be read and to which DAC input data may be written. DB7 is the Most Significant Bit.
11	$\overline{INT}$	Interrupt Output (active low). $\overline{INT}$ is set high on the falling edge of $\overline{RD}$ or $\overline{WR}$ to the ADC and goes low at the end of a conversion.
12	CLK	Clock input. A clock is required for the ADC. An external TTL-compatible clock may be applied to this input pin. Alternatively, tying this pin to V_{DD} enables the internal clock oscillator. With an external clock, the mark-space ratio can vary from 30/70 to 70/30.
13	$\overline{CHA}$/CHB	Channel A/Channel B Select Input. Selects Channel A or Channel B of the DAC or ADC. Used in conjunction with $\overline{WR}$, $\overline{RD}$, $\overline{CS}$ and $\overline{ADC}$/DAC for read or write operations.
14	DGND	Digital Ground.
15	$\overline{ADC}$/DAC	ADC or DAC Select Input. Selects either the ADC or the DAC for read or write operations in conjunction with $\overline{WR}$, $\overline{RD}$, $\overline{CS}$ and $\overline{CHA}$/CHB.
16	$\overline{WR}$	Write Input (edge triggered). This is used in conjunction with the $\overline{ADC}$/DAC, $\overline{CHA}$/CHB and $\overline{CS}$ control inputs to start an ADC conversion or write data to the DAC. An ADC conversion starts on the rising edge of $\overline{WR}$.
17	$\overline{RD}$	Read Input (active low). This input must be low to access data from the ADC.
18	$\overline{CS}$	Chip Select Input (active low). The device is selected when this input is low.
19	V_{SWING} (ADC)	ADC Reference Input. The voltage applied to this pin with respect to AGND (ADC) sets the input voltage Full-Scale Range (FSR) of the ADC. V_{IN} (FSR) = 2 V_{SWING} (ADC).
20	AGND (ADC)	ADC Analog Ground.
21	V_{IN}B	Analog Input for Channel B. See V_{IN}A description.
22	V_{BIAS} (ADC)	ADC Reference Input. The voltage applied to this pin with respect to AGND (ADC) sets the midpoint of the ADC transfer function.
23	V_{IN}A	Analog Input for Channel A. The input voltage range of both ADC channels is given by: V_{IN} A/B = V_{BIAS} (ADC) ±V_{SWING} (ADC).
24	AGND (DAC)	DAC Analog Ground.
25	V_{SWING} (DAC)	DAC Reference Input. The voltage applied to this pin with respect to AGND (DAC) sets the output voltage Full-Scale Range (FSR) of the DACs. V_{OUT} (FSR) = 2 V_{SWING} (DAC).
26	V_{OUT}B	Analog Output Voltage from DAC B. See V_{OUT}A description.
27	V_{BIAS} (DAC)	DAC Reference Input. The voltage applied to this pin with respect to AGND (DAC) sets the midpoint output voltage of the DACs.
28	V_{OUT}A	Analog Output Voltage from DAC A. The output voltage range of both DACs is given by: V_{OUT} A/B = V_{BIAS} (DAC) ± V_{SWING} (DAC).

TERMINOLOGY

Relative Accuracy

For an ADC, Relative Accuracy or endpoint nonlinearity is the maximum deviation, in LSBs, of the ADC's actual code transition points from a straight line drawn between the endpoints of the ADC transfer function, i.e., the 00 to 01 and FE to FF Hex (01111111 to 11111111 Binary) code transitions.

For a DAC, Relative Accuracy or endpoint nonlinearity is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function, i.e., those voltages which correspond to codes 00 and FF Hex.

For the specified input and output ranges, 1 LSB = 19.5 mV, but will vary with V_{SWING}. For both DACs and ADC, 1 LSB = 2 V_{SWING} / 256 = FSR / 256.

Differential Nonlinearity

Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max ensures monotonicity (DAC) or no missed codes (ADC).

Bias Offset Error

For an ideal ADC, the output code for an input voltage equal to V_{BIAS} (ADC), should be 80 Hex (10000000 binary). The ADC Bias Offset Error is the difference between the actual midpoint voltage for code 80 Hex and V_{BIAS} (ADC), expressed in LSBs.

For an ideal DAC, the output voltage for code 80 Hex should be equal to V_{BIAS} (DAC). The DAC Bias Offset Error is the difference between the actual output voltage and V_{BIAS} (DAC), expressed in LSBs.

Plus and Minus Full-Scale Error
The ADC and DACs in the AD7769 can be considered as devices with bipolar (plus and minus) input ranges, but referred to V_{BIAS} instead of AGND. Plus Full-Scale Error for the ADC is the difference between the actual input voltage at the FE to FF code transition and the ideal input voltage (V_{BIAS} + V_{SWING} −1.5 LSB), expressed in LSBs. Minus Full-Scale Error is similarly specified for the 01 to 00 code transition, relative to the ideal input voltage for this transition (V_{BIAS} − V_{SWING} +0.5 LSB). Plus Full-Scale Error for the DACs is the difference, expressed in LSBs, between the actual output voltage for input code FF and the ideal voltage (V_{BIAS} + V_{SWING} − 1 LSB). Minus Full-Scale Error is similarly specified for code 00, relative to the ideal output voltage (V_{BIAS} − V_{SWING}). Note that Plus and Minus Full-Scale errors for the ADC and the DAC outputs are measured after their respective Bias Offset errors have been adjusted out.

Digital-to-Analog Glitch Impulse
Digital-to-Analog Glitch Impulse is the impulse injected into the analog outputs when the digital inputs change state with either DAC selected. It is normally specified as the area of the glitch in nV secs and is measured when the digital input code is changed by 1 LSB at the major carry transition.

Digital Feedthrough
Digital Feedthrough is also a measure of the impulse injected into the analog outputs from the digital inputs but is measured when the DACs are not selected. It is essentially feedthrough across the die and package. It is important in the AD7769 since it is a measure of the glitch impulse transferred to the analog outputs when data is read from the ADC register. It is specified in nV secs and is measured with $\overline{WR}$ high and a digital code change from all 0s to all 1s.

Signal-to-Noise Ratio (SNR)
SNR is the measured Signal-to-Noise Ratio at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)\ dB$$

where N is the number of bits. Thus for an ideal 8-bit converter, SNR = 49.92 dB.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7769, Total Harmonic Distortion is defined as

$$20\ log\ \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the individual harmonics.

Intermodulation Distortion (IMD)
With inputs consisting of sine waves at two frequencies, f_a and f_b, any active device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mf_a+nf_b, where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms include (f_a+f_b) and (f_a-f_b) and the third order terms include ($2f_a+f_b$), ($2f_a-f_b$), (f_a+2f_b) and (f_a-2f_b).

8

LOGIC TRUTH TABLE

ADC CHANNEL SELECT AND START CONVERSION

$\overline{CS}$	$\overline{ADC}$/DAC	$\overline{CHA}$/CHB	$\overline{WR}$	$\overline{RD}$	DB0–DB7	$\overline{INT}$	Comments
0	0	X		Note 1	Note 1	1	$\overline{INT}$ Is Set on Falling Edge of $\overline{WR}$.
0	0	0		Note 1	Note 1	1	Select ADC Channel A and Start Conversion.
0	0	1		Note 1	Note 1	1	Select ADC Channel B and Start Conversion.
						0	$\overline{INT}$ Goes Low at End of Conversion.

READ ADC DATA

$\overline{CS}$	$\overline{ADC}$/DAC	$\overline{CHA}$/CHB	$\overline{WR}$	$\overline{RD}$	DB0–DB7	$\overline{INT}$	Comments
0	X	X	X		ADC Data	1	$\overline{INT}$ Is Set High on Falling Edge of $\overline{RD}$.
0	X	X	X	0	ADC Data	1	ADC Data on Data Bus.
0	X	X	X		High-Z	1	Data Outputs High Impedance.

WRITE TO DACA OR DACB

$\overline{CS}$	$\overline{ADC}$/DAC	$\overline{CHA}$/CHB	$\overline{WR}$	$\overline{RD}$	DB0–DB7	$\overline{INT}$	Comments
0	1	0		1	µP Data	N/C	µP Writing Data to DACA.
0	1	1		1	µP Data	N/C	µP Writing Data to DACB.
0	1	0		0	ADC Data	N/C	Data from Last ADC Conversion Will Be Written to DACA.
0	1	1		0	ADC Data	N/C	Data from Last ADC Conversion Will Be Written to DACB.
1	X	X	X	X	High-Z	N/C	No Operation.

NOTES
[1]If $\overline{RD}$ = 1, DB0–DB7 will remain high impedance. If $\overline{RD}$ = 0, DB0–DB7 will output previous ADC data. The $\overline{RD}$ input should not change during a conversion.
[2]X = Don't Care.
[3]N/C = No Change.

CIRCUIT DESCRIPTION

Analog Inputs and Outputs

The AD7769 provides the analog-to-digital and digital-to-analog conversion functions required between the microcontroller and the servo power amplifier in digital servo systems. It is intended primarily for closed loop head positioning in Winchester disk drives but may also be used for microstepping in drives with stepper motor head positioning or other servo applications. The AD7769 contains a high speed, 8-bit, sampling ADC with two input channels and two 8-bit DACs with output buffer amplifiers. A unique feature of the AD7769 is the input and output signal conditioning circuitry which allows the analog input and output voltages to be referred to a point other than analog ground. The input range and offset of the ADC, the output swing and offset of the DACs may be adjusted independently by the application of ground-referenced, positive control voltages, V_{BIAS} (ADC), V_{SWING} (ADC), V_{BIAS} (DAC) and V_{SWING} (DAC). Thus, for example, the peak-to-peak output swing of the DACs could be set to 3 V above and 3 V below a bias voltage of 5 V.

Figures 5 and 6 show the transfer functions of the ADC and DACs and their relationship to V_{BIAS} and V_{SWING}. The mid-point code of the ADC, 80 Hex (10000000 Binary), occurs at an input voltage equal to V_{BIAS}. The input FSR of the ADC is equal to 2 V_{SWING}, so that the Plus Full-Scale code transition (FE to FF Hex) occurs at a voltage equal to V_{BIAS} + V_{SWING} −1.5 LSBs and the Minus Full-Scale code transition (01 to 00 Hex) occurs at a voltage V_{BIAS} − V_{SWING} +0.5 LSBs. The transfer function of the DACs bears a similar relationship to V_{BIAS} and V_{SWING}. The DAC output voltage for code 80 Hex (10000000 binary) is equal to V_{BIAS}, whilst FF Hex (11111111 binary) gives an output voltage of V_{BIAS} + V_{SWING} −1 LSB (Plus Full-Scale) and 00 Hex gives an output voltage of V_{BIAS} − V_{SWING} (Minus Full-Scale).

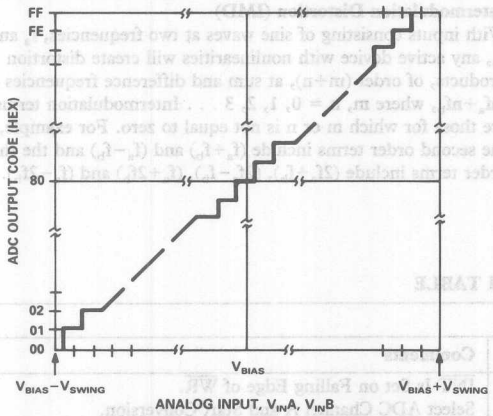


Figure 5. ADC Transfer Function

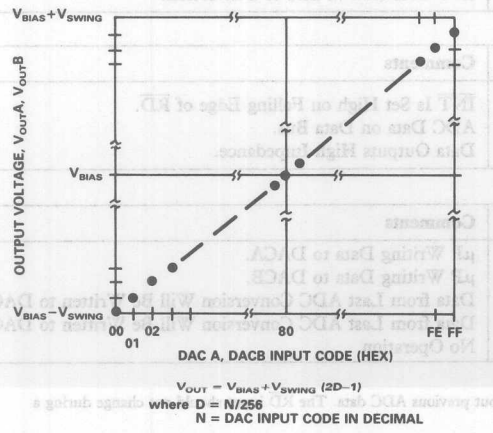


Figure 6. DAC Transfer Function

The ability to refer input and output signals to some voltage other than ground is of particular importance in disk drive applications. Typically, only +5 V digital and +12 V analog supply voltages are available, and the analog signals are often referred to a voltage around half the analog supply.

Driving the Analog Inputs and Reference Inputs

The analog inputs, $V_{IN}A$ and $V_{IN}B$, must be driven from low output impedance sources, such as from op amps. In addition, V_{BIAS} (ADC) must be driven from a similar type low impedance source (e.g., voltage reference).

Op amps are not required to drive the V_{SWING} (ADC), V_{BIAS} (DAC) and V_{SWING} (DAC) inputs as these are high impedance inputs (200 nA typical input current) that feed into on-chip buffer amplifiers. The reference voltages for these inputs can be derived using suitable resistor divider networks.

The analog reference available in the disk drive system can be used to set the bias voltage of the AD7769, and could also be attenuated to provide the reference for the input and output swing as shown in Figure 7. The same bias voltage would generally (though not necessarily) be used for the ADC and the DACs, though the input and output ranges might be different.

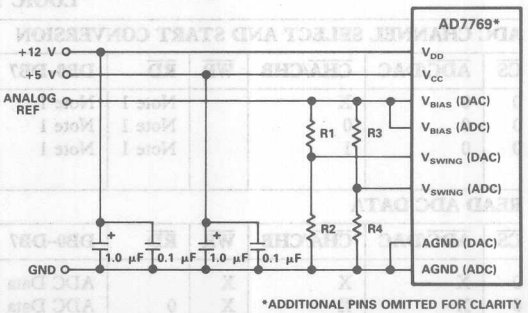


Figure 7. Typical Analog Connections to the AD7769

ADC Conversion Cycle

Figure 8 shows the operating waveforms for a conversion cycle. On the rising edge of $\overline{WR}$, the conversion cycle starts with the acquisition and tracking of the selected ADC channel, $V_{IN}A$ or $V_{IN}B$. The analog input voltage is held 50 ns (typically) after the fourth falling edge of the input CLK following a conversion start. If t_D in Figure 8 is greater than 150 ns, then the falling edge of the input CLK will be seen as the first falling clock edge. If t_D is less than 150 ns, the first falling clock edge to be recognized will not occur until one cycle later.

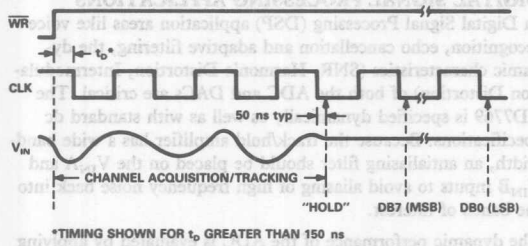


Figure 8. Operating Waveforms Using External Clock

Following the "hold" on the analog input, the MSB decision is made approximately 50 ns after the next falling edge of the input CLK. The succeeding bit decisions are made approximately 50 ns after a CLK edge until conversion is complete. At the end of conversion, the $\overline{INT}$ line goes low 100 ns (typically) after the LSB decision and the SAR contents are transferred to the output latch. The SAR is then reset in readiness for a new conversion.

Track-and-Hold

The track-and-hold (T/H) amplifier on the analog input to the ADC of the AD7769 allows the ADC to accurately convert an input sine wave of 5 V peak-to-peak amplitude up to a frequency of 200 kHz, the Nyquist frequency of the ADC when operated at its maximum throughput rate of 400 kHz. This maximum rate of conversion includes conversion time and time between conversions. Because the input bandwidth of the track-and-hold is much greater than 200 kHz, the input signal should be band limited to avoid folding unwanted signals into the band of interest.

DAC Outputs

The D/A converter outputs are buffered with on-board, high speed op amps that are capable of driving 5 kΩ and 100 pF loads to AGND (DAC). Each output amplifier settles to within 1/2 LSB of its final output value in typically less than 2.5 μs. See Figures 9 and 10 for waveforms of the typical output settling time performance.

The output noise from the amplifiers with full scale on the DACs is typically 200 μV peak-to-peak.

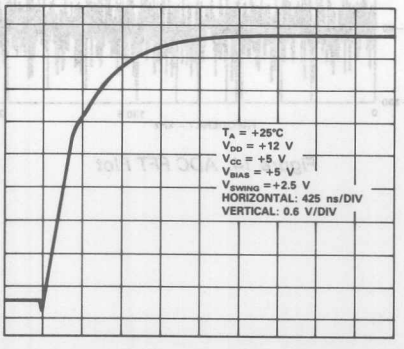


Figure 9. Positive-Going Settling Time

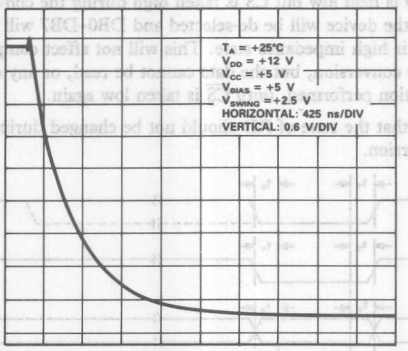


Figure 10. Negative-Going Settling Time

Internal / External Clock Operation

The AD7769 can be operated on either its own internal clock or with an externally applied clock signal . For internal clock operation the CLK input must be tied to V_{DD}. No external components are required. The internal clock typically runs at 5 MHz giving a typical conversion time of 2.5 μs. For external clock operation the CLK input must be driven with a TTL/HCMOS compatible input. The mark/space ratio of the clock signal can vary from 30/70 to 70/30. For an input frequency of 5 MHz, the conversion time is 2.5 μs.

Digital Inputs and Outputs

The AD7769 communicates over a standard, 8-bit microprocessor data bus and is controlled by standard mpu control lines, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{INT}$, plus two address lines, $\overline{ADC}$/DAC and $\overline{CHA}$/CHB, which select the DAC or ADC function and Channel A or Channel B input/output channel. The Chip Select ($\overline{CS}$) line selects the device, Write ($\overline{WR}$) is used to initiate ADC conversions or to write data to the DAC, depending on the state of $\overline{ADC}$/DAC. $\overline{INT}$ is a status flag that indicates completion of a conversion, while $\overline{RD}$ is used to read ADC output data. The 8-bit data port (DB0-DB7) is a bidirectional port into which data can be written to the two DAC registers, and from which data can be read from the ADC register. ADC output data may also be written directly into either of the DAC registers.

These logical operations are detailed in Table I and in the timing diagrams, Figures 11 to 13. Figures 12 and 13 show the fairly straightforward operations of reading ADC data and writing data to the DACs, and need little explanation. Figure 11 shows the timing for ADC channel selection and conversion start. This is more complicated as the state of the data outputs during a conversion depends on $\overline{CS}$ and $\overline{RD}$.

To initiate a conversion (or any other operation) the device must be selected by taking $\overline{CS}$ low. A conversion is started by taking $\overline{WR}$ low, then high again (conversion starts on rising edge of $\overline{WR}$). There are three possibilities for the state of the data outputs during the conversion.

1. If $\overline{RD}$ is held high, the data outputs will be high impedance throughout the conversion.
2. If $\overline{RD}$ and $\overline{CS}$ are both held low until after $\overline{INT}$ goes low, then DB0–DB7 will initially output data from the last conversion. After $\overline{INT}$ goes low the new conversion data will appear on DB0–DB7.

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sion, the device will be de-selected and DB0–DB7 will revert to their high impedance state. This will not affect completion of the conversion, but the data cannot be read, or any other operation performed, until $\overline{CS}$ is taken low again.

4. Note that the state of $\overline{RD}$ should not be changed during a conversion.

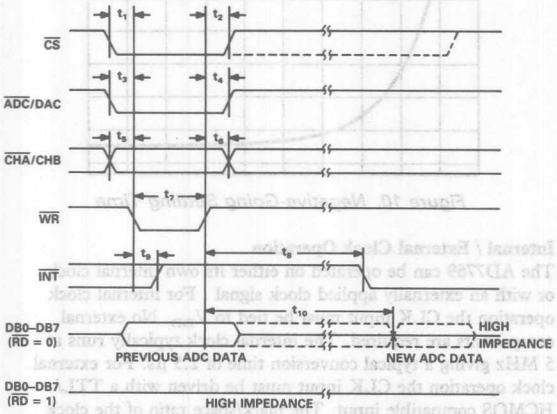


Figure 11. Timing for ADC Channel Select and Conversion Start

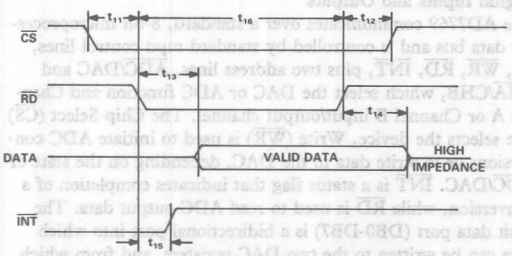
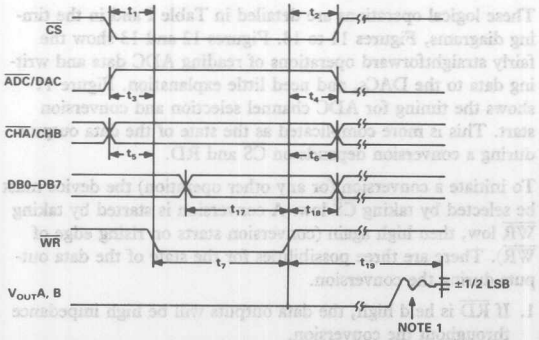


Figure 12. Timing for ADC Data Read



NOTE 1. THE TIME AXIS IS COMPRESSED FOR THIS SECTION OF THE DIAGRAM

Figure 13. Timing for DAC Channel Select and Data Write

In Digital Signal Processing (DSP) application areas like voice recognition, echo cancellation and adaptive filtering, the dynamic characteristics (SNR, Harmonic Distortion, Intermodulation Distortion) of both the ADC and DACs are critical. The AD7769 is specified dynamically as well as with standard dc specifications. Because the track/hold amplifier has a wide bandwidth, an antialiasing filter should be placed on the $V_{IN}A$ and $V_{IN}B$ inputs to avoid aliasing of high frequency noise back into the bands of interest.

The dynamic performance of the ADC is evaluated by applying a sine wave signal of very low distortion to the $V_{IN}A$ or $V_{IN}B$ input which is sampled at a 409.6 kHz sampling rate. A Fast Fourier Transform (FFT) plot or Histogram plot is then generated from which SNR, harmonic distortion and dynamic differential nonlinearity data can be obtained. For the DACs, the codes for an ideal sine wave are stored in PROM and loaded down to the DAC. The output spectrum is analyzed, using a spectrum analyzer to evaluate SNR and harmonic distortion performance. Similarly, for intermodulation distortion, an input (either to VIN or DAC code) consisting of pure sine waves at two frequencies is applied to the AD7769.

Figure 14 shows a 2048 point FFT plot of the ADC with an input signal of 130 kHz. The SNR is 49.2 dB. It can be seen that most of the harmonics are buried in the noise floor. It should be noted that the harmonics are taken into account when calculating the SNR. The relationship between SNR and resolution (N) is expressed by the following equation:

$$SNR = (6.02N + 1.76)\ dB$$

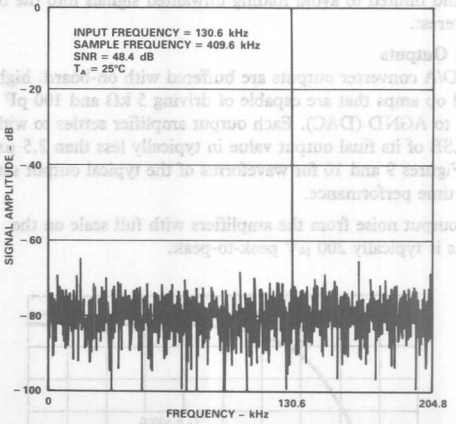


Figure 14. ADC FFT Plot

This is for an ideal part with no differential or integral linearity errors. These errors will cause a degradation in SNR. By working backwards from the above equation, it is possible to get a measure of ADC performance expressed in effective number of bits (N). The effective number of bits is plotted versus frequency in Figure 15. The effective number of bits typically falls between 7.7 and 7.9, corresponding to SNR Figures 48.1 and 49.7 dB.

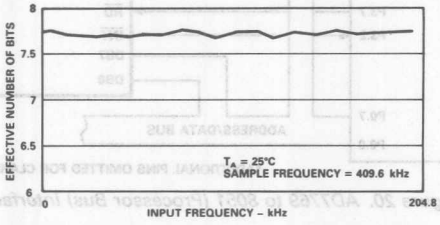


Figure 15. Effective Number of Bits vs. Frequency

Figure 16 shows a spectrum analyzer plot of the output spectrum from one of the DACs with an ideal sine wave table loaded to the data inputs of the DAC. In this case, the SNR is 47 dB.

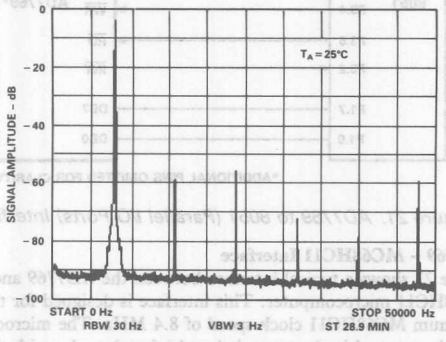


Figure 16. DAC Output Spectrum

Histogram Plot

When a sine wave of specified frequency is applied to the $V_{IN}A$ or $V_{IN}B$ input of the AD7769 and several thousand samples are taken, it is possible to plot a histogram showing the frequency of occurrence of each of the 256 ADC codes. If a particular step is wider than the ideal 1 LSB width, then the code associated with that step will accumulate more counts than for the code for an ideal step. Likewise, a step narrower than ideal width will have fewer counts. Missing codes are easily seen because a missing code means zero counts for a particular code. The absence of large spikes in the plot indicates small differential nonlinearity.

Figure 17 shows a histogram plot for the ADC indicating very small differential nonlinearity and no missing codes for an input frequency of 204 kHz. For a sine wave input, a perfect ADC would produce a probability density function described by the equation:

$$p(V) = \frac{1}{\pi (A^2 - V^2)^{1/2}}$$

where A is the peak amplitude of the sine wave and p (V) the probability of occurrence at a voltage V. The histogram plot of Figure 17 corresponds very well with this shape.

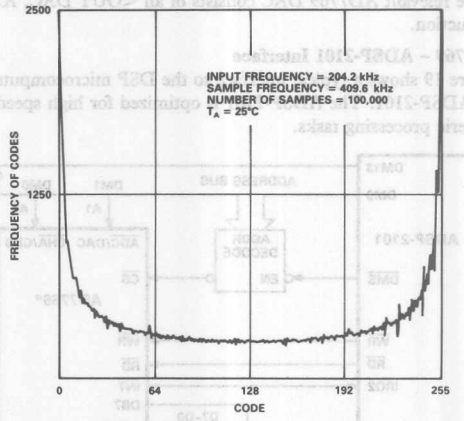


Figure 17. ADC Histogram Plot

In digital signal processing applications, where the AD7769 is used to sample AC signals, it is essential that the signal sampling occurs at exactly equal intervals. This minimizes errors due to sampling uncertainty or jitter. A precise timer or clock source, to start the conversion process, is the best method of generating equidistant sampling intervals.

MICROPROCESSOR / MICROCOMPUTER INTERFACING

The AD7769 is designed for easy interfacing to microprocessors and microcomputers as a memory mapped peripheral or an I/O device. In addition, the AD7769 high speed bus timing allows direct interfacing to many DSP processors such as the TMS320C10 and ADSP-2101.

AD7769 – TMS320C10 Interface

A typical interface to the TMS320C10 is shown in Figure 18. The AD7769 is mapped at a port address, and the interface is designed for the maximum TMS320C10 clock frequency of 20 MHz.

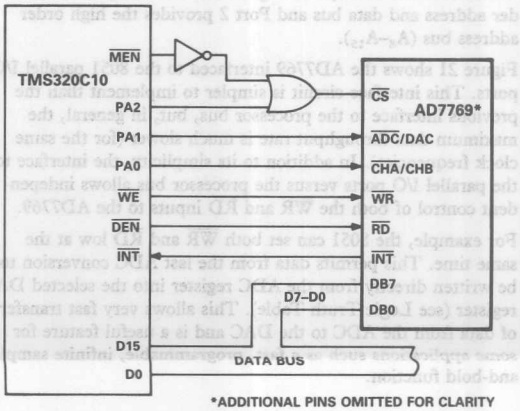


Figure 18. AD7769 to TMS320C10 Interface

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Conversion is initiated on the selected AD7769 ADC channel using a single I/O instruction, <OUT ADC, A>. The processor then polls $\overline{INT}$ until it goes low before reading the conversion result using an <IN A, ADC> instruction. Writing data to the relevant AD7769 DAC consists of an <OUT DAC, A> instruction.

AD7769 – ADSP-2101 Interface

Figure 19 shows a typical interface to the DSP microcomputer, the ADSP-2101. The ADSP-2101 is optimized for high speed numeric processing tasks.

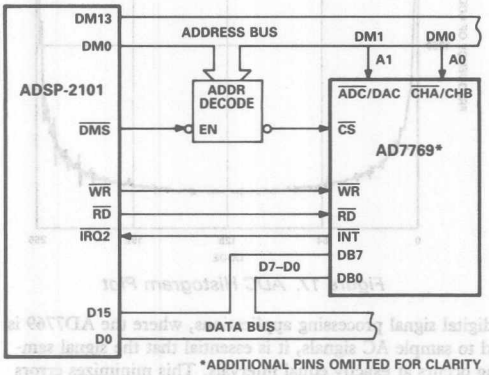


Figure 19. AD7769 to ADSP-2101 Interface

Because the instruction cycle of the ADSP-2101 is very fast (80 ns cycle), the $\overline{WR}$ and $\overline{RD}$ pulses must be stretched out to suit the AD7769. This is easily achieved as the ADSP-2101 memory interface supports slower memories and memory-mapped peripherals (i.e., AD7769) with a programmable wait state generation capability. A number of wait states, from 0 to 7, can be specified for each memory interface. One wait state is sufficient for the interface to the AD7769.

AD7769 – 8051 Interface

A choice of two interface modes are available to the 8051 microcomputer.

Figure 20 shows a typical interface to the 8051 processor bus. It is suitable for the maximum 8051 clock frequency of 12 MHz. In this interface mode, Port 0 provides the multiplexed low order address and data bus and Port 2 provides the high order address bus (A_8–A_{15}).

Figure 21 shows the AD7769 interfaced to the 8051 parallel I/O ports. This interface circuit is simpler to implement than the previous interface to the processor bus, but, in general, the maximum data throughput rate is much slower (for the same clock frequencies). In addition to its simplicity, the interface to the parallel I/O ports versus the processor bus allows independent control of both the $\overline{WR}$ and $\overline{RD}$ inputs to the AD7769.

For example, the 8051 can set both $\overline{WR}$ and $\overline{RD}$ low at the same time. This permits data from the last ADC conversion to be written directly from the ADC register into the selected DAC register (see Logic Truth Table). This allows very fast transfer of data from the ADC to the DAC and is a useful feature for some applications such as a fast, programmable, infinite sample-and-hold function.

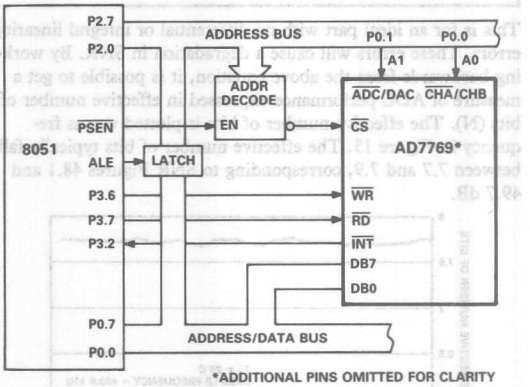


Figure 20. AD7769 to 8051 (Processor Bus) Interface

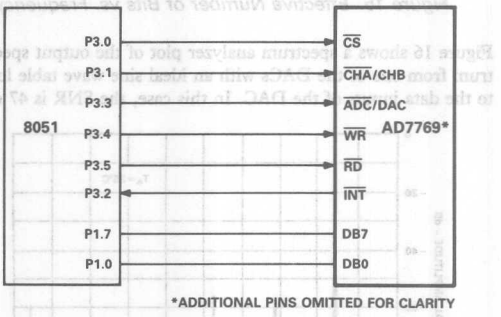


Figure 21. AD7769 to 8051 (Parallel I/O Ports) Interface

AD7769 – MC68HC11 Interface

Figure 22 shows a typical interface between the AD7769 and the MC68HC11 microcomputer. This interface is designed for the maximum MC68HC11 clock speed of 8.4 MHz. The microcomputer is operated in the expanded multiplexed mode, with the AD7769 as a memory mapped peripheral. The expansion bus is made up of Ports B and C, and control signals AS and R/$\overline{W}$.

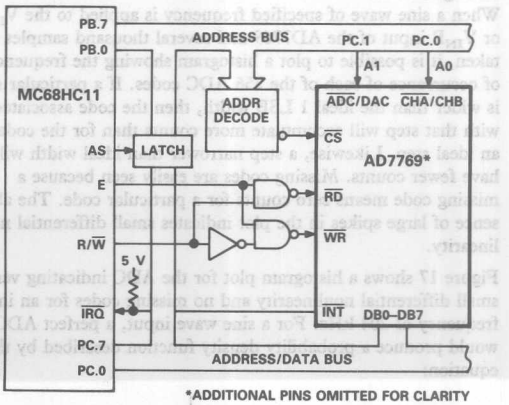


Figure 22. AD7769 to MC68HC11 Interfaced

APPLICATIONS

The AD7769 analog I/O port is used to convert servo related signals between the analog and digital domains. The input structure of the two-channel ADC makes it very easy to convert the typical output signals provided by a servo demodulator.

In a magnetic disk drive employing a dedicated servo surface, the servo demodulator produces two, positive-only, quadrature signals, generally sinusoidal or triangular, from the di-bit patterns read from the servo surface. The quadrature signals have the form of $V_{BIAS} \pm V_{SWING}$. The very fast conversion time of the AD7769 ADC allows sequential conversion of these quadrature signals without introducing significant phase delay errors. These converted signals provide the servo microcontroller with position and track crossing information from which velocity information can be derived. In optical disk drives, analogous servo signals can be derived from the quad photodiode detector to provide position and focus information for the microcontroller.

The two DACs in the AD7769 accept servo data from the microcontroller to position the head assembly. The DACs provide positive-only output signals of the form $V_{BIAS} \pm V_{SWING}$, which are ideal for driving voice coil motors. In magnetic disk drives, a single voice coil motor is used to position the head assembly and one DAC is usually sufficient to drive the motor in both the seek and track modes. In the seek mode, the DAC can be used to generate directly the desired analog velocity trajectory which the head must travel in order to achieve minimum access times. Alternatively, the DAC can generate a servo error value (computed by the microcontroller) between the actual head velocity and the desired head velocity. In the track mode, the DAC can be used to provide a position error signal to keep the head over the track or to detent the head off track, for such purposes as thermal compensation and soft error retries. The second DAC in the AD7769 may be employed in this fine positioning loop. Alternatively, the second DAC can be used to control the speed of the spindle motor via a pulse width modulator. In optical disk drives two voice coil motors are used, requiring both DACs of the AD7769—one for the focus servo loop and one for the radial positioning servo loop.

A typical servo control loop using the AD7769 is shown in Figure 23. In this dedicated servo drive, the servo demodulator converts the servo information bit patterns from the disk into the standard N and Q (normal and quadrature) servo signals. The voice coil motor current, I_L, is bidirectional and is supplied by the power transconductance amplifier. One input to this amplifier is held at V_{BIAS} (DAC), while the other input is driven from a DAC output, V_{OUT} A/B. Typical input/output waveforms for this power stage are shown in Figure 24. The transconductance, G_O, of the power stage is determined by external sense resistors.

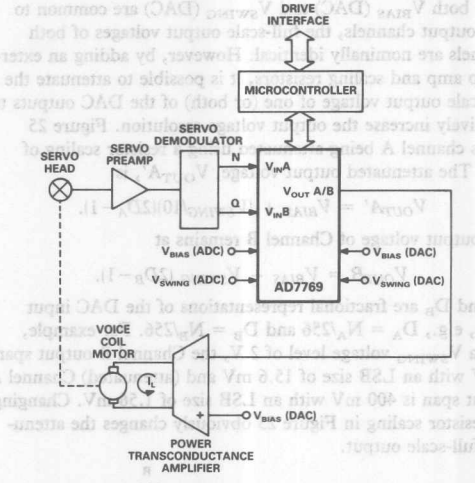


Figure 23. Typical Dedicated Servo Control Loop Using the AD7769

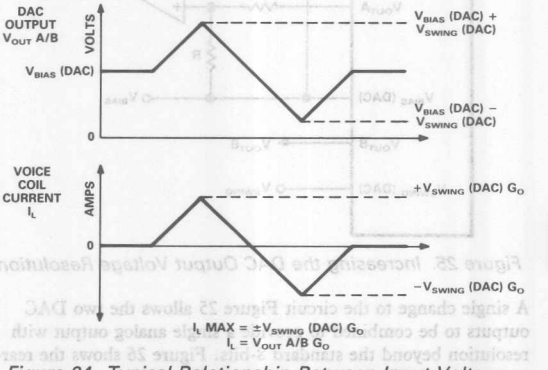


Figure 24. Typical Relationship Between Input Voltage and Output Current for Transconductance Amplifier

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Increased Resolution DAC Output

Since both V_{BIAS} (DAC) and V_{SWING} (DAC) are common to both output channels, the full-scale output voltages of both channels are nominally identical. However, by adding an external op amp and scaling resistors, it is possible to attenuate the full-scale output voltage of one (or both) of the DAC outputs to effectively increase the output voltage resolution. Figure 25 shows channel A being attenuated using a resistor scaling of 10:1. The attenuated output voltage, $V_{OUT}A'$, is

$$V_{OUT}A' = V_{BIAS} + (V_{SWING}/10)(2D_A - 1).$$

The output voltage of Channel B remains at

$$V_{OUT}B = V_{BIAS} + V_{SWING}\,(2D_B - 1).$$

D_A and D_B are fractional representations of the DAC input codes, e.g., $D_A = N_A/256$ and $D_B = N_B/256$. For example, with a V_{SWING} voltage level of 2 V, the Channel B output span is 4 V with an LSB size of 15.6 mV and (attenuated) Channel A output span is 400 mV with an LSB size of 1.56 mV. Changing the resistor scaling in Figure 25 obviously changes the attenuated full-scale output.

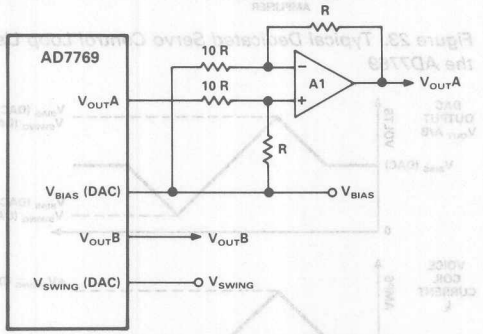


Figure 25. Increasing the DAC Output Voltage Resolution

A single change to the circuit Figure 25 allows the two DAC outputs to be combined to provide a single analog output with resolution beyond the standard 8-bits. Figure 26 shows the rearranged circuit. The composite output, V_{OUT}, is

$$V_{OUT} = V_{OUT}B + (V_{SWING}/10)(2D_A - 1)$$

or

$$V_{OUT} = V_{BIAS} + V_{SWING}\,(2D_B - 1) + (V_{SWING}/10)\,(2D_A - 1).$$

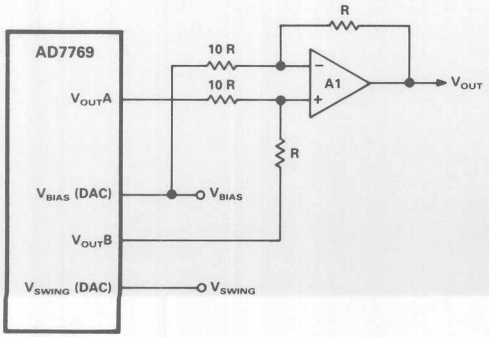


Figure 26. Combined $V_{OUT}A$, $V_{OUT}B$ Circuit

DAC A can be programmed to produce an interpolation function between the 8-bit steps of DAC B to allow, for example, very smooth velocity profile waveforms to be generated.

Servo Offset Facility

Most dedicated servo disk drives offer an offset facility whereby some small voltage is injected into the track-following loop. The purpose of the offset is to move the head to the right or left of its current on-track position to permit reading of off-track data. The circuit is shown in Figure 27. With the 10:1 resistor scaling used in the circuit the output voltage, V_{OUT}, is

$$V_{OUT} = V_{PE} + (V_{SWING}/10)\,(2D_A - 1).$$

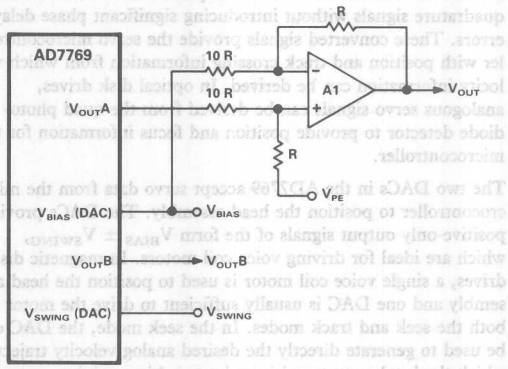


Figure 27. Servo Offset Facility

With no offset added, $V_{OUT} = V_{PE}$, where V_{PE} is the position error voltage which the servo loop normally drives to its zero level, V_{BIAS}. When an offset voltage is supplied by DAC A, the action of the servo is to move the head away from its current on-track position until the position error voltage is equal and opposite to the offset voltage. The position of the head about the track centre is thus programmable.

Programmable Full-Scale Range

The output voltage span of both DACs is determined by the V_{SWING} (DAC) voltage level. This is normally supplied from some fixed voltage source. However, it is possible to use one of the DAC channels to generate a programmable V_{SWING} voltage level. The remaining channel will thus have a full-scale range and LSB size which is software programmable. This circuit is shown in Figure 28 where $V_{OUT}B$ is used in an implicit feedback loop to generate a programmable swing voltage, V_{SWING} (DAC), for the AD7769 from an external fixed input swing voltage, V_{SWING}. Using the 5:1 resistor scaling shown in Figure 28, the expression for the AD7669 input swing voltage is

$$V_{SWING}\,(DAC) = \frac{V_{SWING}}{1 - \dfrac{(2D_B - 1)}{5}}.$$

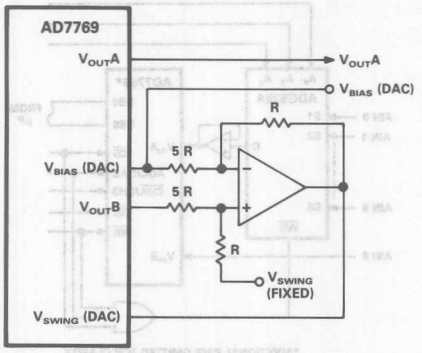


Figure 28. Generating a Software Programmable V_{SWING} (DAC)

For example, with a fixed input swing voltage of 2.5 V, the programmable span via DAC B is as follows:

$D_B = 0$: V_{SWING} (DAC) = 2.08

$D_B = 1/2$: V_{SWING} (DAC) = 2.5 V = V_{SWING}

$D_B \approx 1$: V_{SWING} (DAC) = 3.125 V

The AD7769 is specified for a V_{SWING} (DAC) voltage range from 2 V to 3 V, although in practice this range can be extended while still maintaining monotonic operation.

Closed Loop Microstepping

Microstepping is a popular technique in low density disk drives (both floppy and hard disk) which allows higher positional resolution of the disk drive head over that obtainable from a full-step driven stepper motor. Typically, a two-phase stepper motor has its phase currents driven with a sine-cosine relationship. These cosinusoidal signals are generated by two DACs driven with the appropriate data. The resolution of the DACs determines the number of microsteps into which each full step can be divided. For example, with a 1.8° full-step motor and a 4-bit DAC, a microstep size of 0.11° (1.8°/2^n) is obtainable.

The microstepping technique improves the positioning resolution possible in any control application. However, the positional accuracy can be significantly worse than that offered by the original full-step accuracy specification due to load torque effects. To ensure that the increased resolution is useable, it is therefore necessary to use a closed-loop system where the position of the disk drive head (or motor) is monitored. The closed-loop system allows an error between the desired position and the actual position to be monitored and corrected. The correction is achieved by adjusting the ratio of the phase currents in the motor windings until the required head position is reached.

The AD7769 is ideally suited for the closed-loop microstepping technique with its dual DACs for positioning the disk drive head and dual channel ADC for monitoring the position of the head. A typical circuit for a closed-loop microstepping system is shown in Figure 29. The DAC waveforms are shown in Figure 30 along with the direction information of clockwise rotation supplied by the controller.

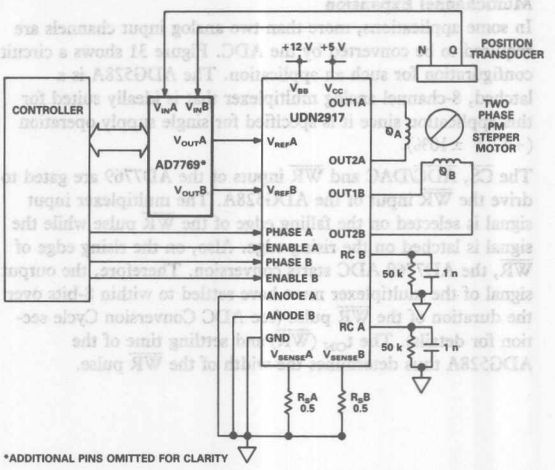


Figure 29. Typical Closed-Loop Microstepping Circuit with the AD7769

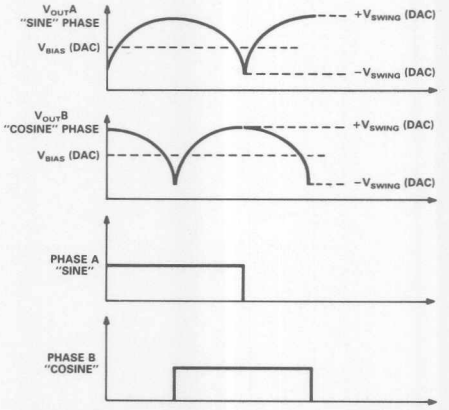


Figure 30. Typical Control Waveforms for the Microstepping Circuit of Figure 29

A typical transducer would be a moire-fringe transducer which consists of two gratings, one fixed and one moveable. The relative positions of these two gratings will modulate the amount of light from a LED which can pass through. In order to derive head direction information the stationary grating has two sets of bars, with a 90° phase relationship, and two photo-transistors. The quadrature sinusoidal output waveforms (N & Q) can be converted directly by the AD7769.

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Multichannel Expansion

In some applications, more than two analog input channels are required to be converted by the ADC. Figure 31 shows a circuit configuration for such an application. The ADG528A is a latched, 8-channel analog multiplexer that is ideally suited for this application since it is specified for single supply operation (+12 V ±10%).

The $\overline{CS}$, $\overline{ADC}$/DAC and $\overline{WR}$ inputs of the AD7769 are gated to drive the $\overline{WR}$ input of the ADG528A. The multiplexer input signal is selected on the falling edge of the $\overline{WR}$ pulse while the signal is latched on the rising edge. Also, on the rising edge of $\overline{WR}$, the AD7769 ADC starts conversion. Therefore, the output signal of the multiplexer must have settled to within 8-bits over the duration of the $\overline{WR}$ pulse (see ADC Conversion Cycle section for details). The t_{ON} ($\overline{WR}$) and settling time of the ADG528A thus determines the width of the $\overline{WR}$ pulse.

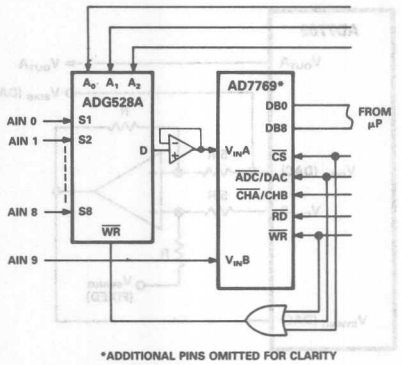


Figure 31. Multichannel Inputs

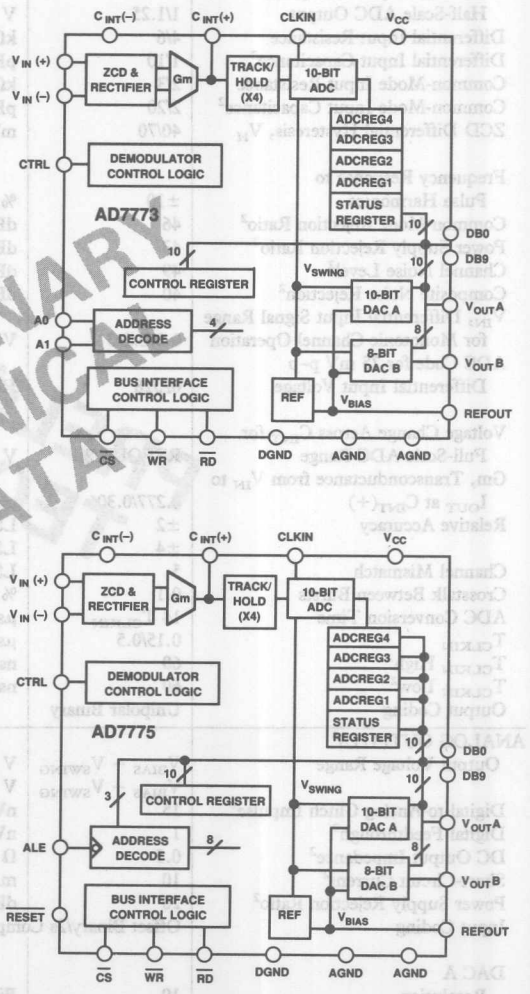
LC²MOS Complete Embedded Servo Front Ends for HDD

AD7773/AD7775*

FEATURES
10-Bit, 3 µs ADC
Two DACs with Output Amplifiers
One 10-Bit, 4 µs Settling DAC
One 8-Bit, 3 µs Settling DAC
Fully Integrated Burst Detector
Power-Down Mode
+5 V Only
Fast Interface Port
28-Pin SOIC Package

APPLICATIONS
Embedded Servo For HDD
Combined Dedicated /Embedded Servo

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD7773 and AD7775 provide all the functionality necessary to implement the servo demodulator and head positioning tasks in embedded servo systems. A power-down mode which turns all the linear circuitry OFF enhances the use of the AD7773 and AD7775 in portable systems.

The demodulator channel can capture high speed servo data from a variety of embedded servo patterns. Up to four sequential servo burst signals can be synchronously demodulated, full-wave rectified and integrated. At the end of a burst period the integrated output voltage, representing the amplitude of a captured burst, is sampled and held on one of four internal track/hold amplifiers prior to conversion. After conversion the digitized burst signals from the ADC are fed to four 10-bit wide data registers.

The AD7773 and AD7775 also contain two independent voltage-output DACs: one with 10-bit resolution and one with 8-bit resolution. The two DACs produce output signals of the form $V_{BIAS} \pm V_{SWING}$ where V_{BIAS} and V_{SWING} are internally generated on-chip. The V_{BIAS} signal is available externally on the REFOUT pin.

The devices are easily interfaced to popular DSP processors and microcontrollers. The AD7773 has a 10-bit data port with separate address pins. The AD7775 has a 10-bit multiplexed address/data bus with an ALE input to latch the address.

The AD7773 and AD7775 are fabricated in linear compatible CMOS (LC²CMOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The devices are available in 28-pin SOIC packages.

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*Protected by U.S. Patent No. 4,990,916.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

DEMODULATOR CHANNEL			All AC Test Waveforms are Sinusoidal. Minimum Signal Frequency Is 2 MHz.
ADC Resolution	10	Bits	
Differential Voltage Gain	440	LSB/V p–p min	
	520	LSB/V p–p max	
Differential Input Voltage for Half-Scale ADC Output	1/1.25	V p–p min/max	
Differential Input Resistance	4/6	kΩ min/max	Typically 5 kΩ; Measured at DC; See Terminology
Differential Input Capacitance[2]	1/10	pF min/max	
Common-Mode Input Resistance	2/3	kΩ min/max	Typically 2.5 kΩ; Measured at DC; See Terminology
Common-Mode Input Capacitance[2]	2/20	pF min/max	
ZCD Differential Hysteresis, V_H	40/70	mV p–p min/max	Typically 55 mV; See Figure 20 under Design Information
Frequency Response to Pulse Harmonics	±10	% max	See Terminology
Common-Mode Rejection Ratio[2]	46	dB min	See Terminology
Power Supply Rejection Ratio[2]	43	dB min	See Terminology
Channel Noise Level[2]	49	dB min	See Terminology
Composite Noise Rejection[2]	40	dB min	Referenced to Half-Scale; See Terminology
V_{IN}, Differential Input Signal Range for Monotonic Channel Operation	0.075/2.3	V p–p min/max	See Terminology
ADC Code for 75 mV p–p Differential Input Voltage	0A/28	Hex min/max	Equivalent to 10 LSBs and 40 LSBs, Respectively See Figure 19
Voltage Change Across C_{INT} for Full-Scale ADC Range	REFOUT/2	V	
Gm, Transconductance from V_{IN} to I_{OUT} at C_{INT}(+)	0.277/0.306	ms min/max	
Relative Accuracy	±2	LSB max	1/4 FS to 3/4 FS; See Terminology
	±4	LSB max	1/8 FS to 7/8 FS; See Terminology
Channel Mismatch	5	LSB max	Measured at Half-Scale; See Terminology
Crosstalk Between Bursts	0.1	% max	See Terminology
ADC Conversion Time	14 T_{CLKIN}	μs max	Per Captured Burst; See Terminology
T_{CLKIN}	0.15/0.5	μs min/max	Period of Input Clock CLKIN
T_{CLKIN} High[2]	60	ns min	Minimum High Time for CLKIN
T_{CLKIN} Low[2]	60	ns min	Minimum Low Time for CLKIN
Output Coding	Unipolar Binary		
ANALOG OUTPUTS[3]			Applies to Both DACs
Output Voltage Range	$V_{BIAS} - V_{SWING}$	V min	
	$V_{BIAS} + V_{SWING}$	V max	
Digital-to-Analog Glitch Impulse[2]	15	nV sec typ	See Terminology
Digital Feedthrough[2]	1	nV sec typ	See Terminology
DC Output Impedance[2]	0.5	Ω typ	
Short-Circuit Current[2]	10	mA typ	
Power Supply Rejection Ratio[2]	20	dB min	See Terminology
Input Coding	Offset Binary/2s Complement		Programmable via Location CR6 of the Control Register
DAC A			
Resolution	10	Bits	
Output Voltage Settling Time[2]	4	μs max	Settling Time to Within ±1/2 LSB of Final Value; Typically 2.0 μs
Relative Accuracy	±1	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Bias Offset Error	±8	LSB max	
Plus or Minus Full-Scale Error	±8	LSB max	Referenced to REFOUT/2

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ANALOG OUTPUTS[3] (Continued)			
DAC B			
Resolution	8	Bits	
Output Voltage Settling Time[2]	3	μs max	Settling Time to Within ±1/2 LSB of Final Value; Typically 2.0 μs
Relative Accuracy	±1	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Bias Offset Error	±4	LSB max	
Plus or Minus Full-Scale Error	±4	LSB max	Referenced to REFOUT/2.
LOGIC INPUTS			
$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, CTRL, CLKIN, $\overline{RESET}$ & ALE (AD7775), A0 & A1 (AD7773)			
Input Low Voltage, V_{INL}	0.8	V max	
Input High Voltage, V_{INL}	2.4	V min	
Input Leakage Current	10	μA max	
Input Capacitance[4]	10	pF max	
LOGIC OUTPUTS			
DB0–DB9 (AD7773)			
AD0–DB9 (AD7775)			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 200 μA
Floating State Leakage Current	10	μA max	
Floating State Capacitance[4]	10	pF max	
POWER REQUIREMENTS			
V_{CC} Range	4.75/5.25	V min/Vmax	For Specified Performance
I_{CC}, Normal Mode	20	mA max	Control Register Locations CR8 = CR9 = Logic High
I_{CC}, Power Down Mode	1	mA max	Control Register Locations CR8 = Logic High, CR9 = Logic Low All Linear Circuitry OFF
Power-Up Time to Operational Specifications[4]	500	μs max	From Standby Mode
DAC REFERENCE INPUTS			
V_{BIAS} for both DACs	REFOUT	V	Internally Connected. Available Externally on REFOUT Pin
V_{SWING} for both DACs	REFOUT/2	V	Internally Connected
REFERENCE OUTPUT[5]			
REFOUT	2.1/2.2	V min/max	
Reference Load Change	±2	mV max	For Reference Load Current Change of 0 to ± 500 μA
	±5	mV max	For Reference Load Current Change of 0 to ± 2 mA Reference Load Should Not Change During Conversion

NOTES
[1]Temperature range as follows: J Version: 0°C to +70°C.
[2]Guaranteed by design, not production tested.
[3]Output load of 10k||100 pF is referenced to REFOUT.
[4]Sample tested at 25°C to ensure compliance.
[5]For capacitive loads greater than 100 pF a series resistor is required.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

INTERFACE TIMING CHARACTERISTICS—AD7773[1, 2] (V_{CC} = +5 V ±5%; AGND = DGND = 0 V)

Parameter	Label	Limit at T_{MIN}, T_{MAX}	Units	Test Conditions/Comments
INTERFACE TIMING				
Address Setup to $\overline{WR}$ or $\overline{RD}$ Falling Edge	t_1	4	ns min	
Address Hold after $\overline{WR}$ or $\overline{RD}$ Rising Edge	t_2	0	ns min	
Address Setup to $\overline{CS}$ Falling Edge	t_3	9	ns min	
$\overline{WR}$ or $\overline{RD}$ Rising Edge to $\overline{CS}$ Rising Edge	t_4	0	ns min	
$\overline{WR}$ or $\overline{RD}$ Pulse Width	t_5	53	ns min	
$\overline{CS}$ or $\overline{RD}$ Active to Valid Data[3]	t_6	48	ns max	Timed from Whichever Occurs Last
Bus Relinquish Time after $\overline{RD}$[4]	t_7	10	ns min	
		22	ns max	
Data Valid to $\overline{WR}$ Rising Edge	t_8	55	ns min	
Data Valid after $\overline{WR}$ Rising Edge	t_9	10	ns min	
Delay Time Between Stack Reads	t_{15}	70	ns min	See Figure 12b

NOTES
[1]See Figures 1 and 2.
[2]Timing Specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[3]t_6 is measured with the load circuit of Figure 3 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[4]t_7 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 3. The measured time is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time t_7 quoted above is the true bus relinquish time of the device and, as such, is independent of the external bus loading capacitance.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

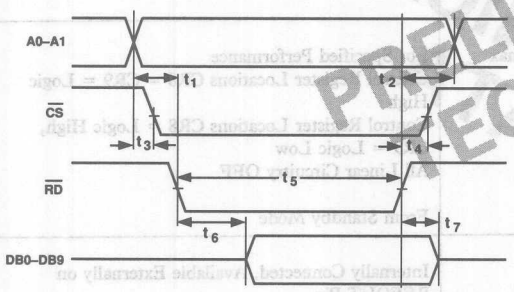


Figure 1. Read Cycle Timing for AD7773 Interface

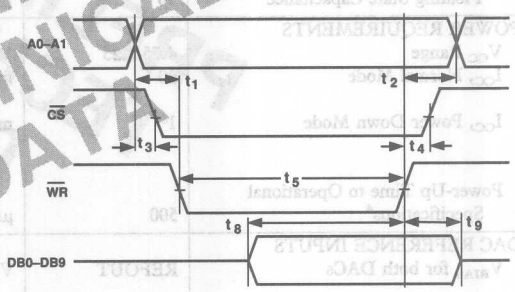
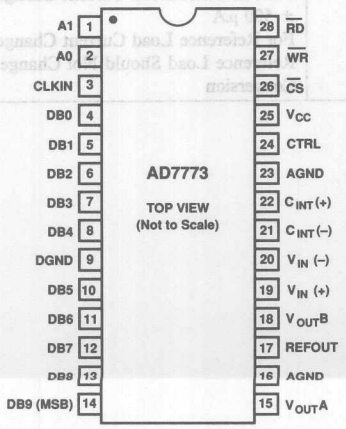
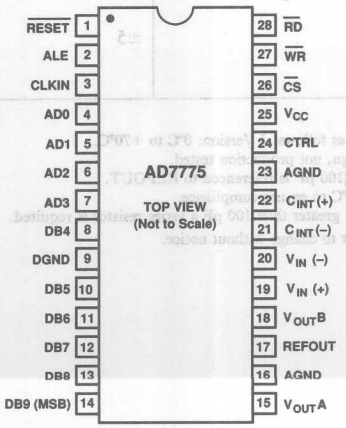


Figure 2. Write Cycle Timing for AD7773 Interface

PIN CONFIGURATIONS





This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

INTERFACE TIMING CHARACTERISTICS—AD7775[1, 2] (V_{CC} = +5 V ± 5%; AGND = DGND = 0 V)

Parameter	Label	Limit at T_{MIN} to T_{MAX}	Units	Test Conditions/Comments
INTERFACE TIMING				
ALE Pulse Width	t_1	50	ns min	
$\overline{WR}$ or $\overline{RD}$ Rising Edge to ALE Rising Edge	t_2	50	ns min	
ALE Rising Edge to $\overline{CS}$ Falling Edge	t_3	22	ns min	
$\overline{CS}$ Falling Edge to $\overline{RD}$ Falling Edge	t_4	60	ns min	
$\overline{CS}$ Falling Edge to $\overline{WR}$ Falling Edge	t_5	30	ns min	
$\overline{WR}$ or $\overline{RD}$ Rising Edge to $\overline{CS}$ Rising Edge	t_6	0	ns min	
$\overline{WR}$ or $\overline{RD}$ Pulse Width	t_7	53	ns min	
ALE Falling Edge to $\overline{WR}$ or $\overline{RD}$ Falling Edge	t_8	32	ns min	
Address Setup to ALE Falling Edge	t_9	47	ns min	
Address Hold after ALE Falling Edge	t_{10}	22	ns min	
$\overline{RD}$ Active to Valid Data[3]	t_{11}	40	ns max	Measured with t_4 = 60 ns
Bus Relinquish Time after $\overline{RD}$[4]	t_{12}	10	ns min	
		62	ns max	
Data Valid to $\overline{WR}$ Rising Edge	t_{13}	55	ns min	
Data Valid after $\overline{WR}$ Rising Edge	t_{14}	10	ns min	
Delay Time Between Stack Reads	t_{15}	70	ns min	See Figure 13b

NOTES

[1]See Figures 4 and 5.

[2]Timing specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[3]Data access time depends directly on t_4, the $\overline{CS}$ to $\overline{RD}$ setup time, e.g., $t_{11} = 100 - t_4$. Time t_{11} is measured with the load circuit of Figure 3 and is defined as the time required for an output to cross 0.8 V or 2.4 V.

[4]t_{12} is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 3. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time t_{12} quoted above is the true bus relinquish time of the device and, as such, is independent of external bus loading capacitance.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

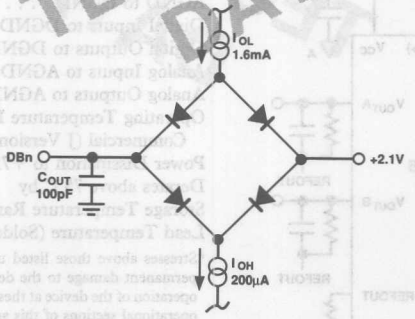


Figure 3. Load Circuit for Bus Timing Characteristics

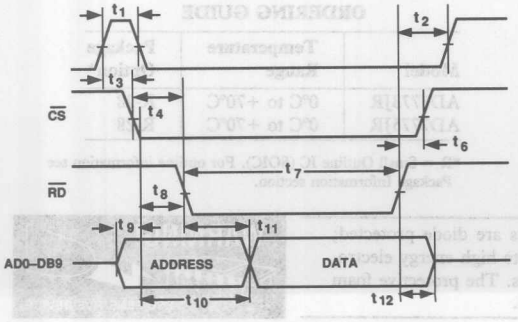


Figure 4. Read Cycle Timing for AD7775

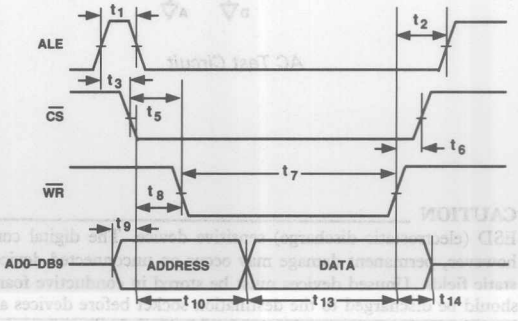


Figure 5. Write Cycle Timing for AD7775

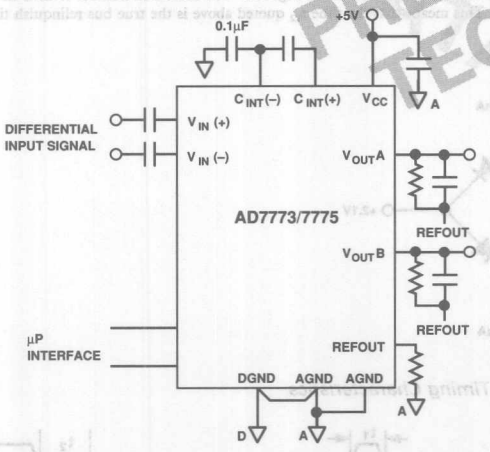
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8

DEMODULATOR TIMING CHARACTERISTICS[1] (V_{CC} = +5 V ± 5%; AGND = DGND = 0 V)

Parameter	Label	Limit at T_{MIN}, T_{MAX}	Units	Test Conditions/Comments
$\overline{RESET}$ Rising Edge to CTRL Rising Edge[2]	-	100	ns min	For AD7775 Only
$\overline{WR}$ Rising Edge to CTRL Rising Edge[2]	-	200	ns min	Applies Only after a Write Instruction to the Control Register
$\overline{RESET}$ Pulse Width[2]	-	100	ns min	For AD7775 Only
SYNCHRONOUS DETECTOR MODE[3]				
CTRL High Time	t_{C1}	N + 3.5 t_{CYC}	ns min	Minimum N for Guaranteed Performance Is 4, Maximum N Is 15. Programmable via Locations CR0–CR3 of the Control Register
CTRL Low Time[2]	t_{C2}	1.5 t_{CYC}	ns min	
Input Signal Period	t_{CYC}	200	ns min	Fundamental Input Frequency Must Lie Between
		500	ns max	2 MHz and 5 MHz
GATED DETECTOR MODE[4]				
CTRL High Time	t_{C1}	800	ns min	
CTRL Low Time[2]	t_{C2}	600 + 0.375 t_{C1}	ns min	
Input Signal Frequency	f_{IN}	5	MHz max	Corresponds to 200 ns Minimum Input Signal Period
CALIBRATION MODE[5]				
CTRL High Time	t_{C1}	800	ns min	Assumes Internal Calibration Voltage Has Settled; See Under Circuit Description for Calibration Mode
CTRL Low Time[2]	t_{C2}	300	ns min	

NOTES
[1]All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]Sample tested at +25°C to ensure compliance.
[3]See Figures 8a and 8b.
[4]See Figure 9.
[5]See Figure 10.



AC Test Circuit

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to AGND or DGND . . . . . −0.3 V, +7 V
AGND to DGND . . . . . −0.3 V, V_{CC} +0.3 V
Digital Inputs to DGND . . . . . −0.3 V, V_{CC} +0.3 V
Digital Outputs to DGND . . . . . − 0.3 V, V_{CC} + 0.3 V
Analog Inputs to AGND . . . . . −0.3 V, V_{CC} +0.3 V
Analog Outputs to AGND . . . . . −0.3 V, V_{CC} +0.3 V
Operating Temperature Range
Commercial (J Version) . . . . . 0°C to +70°C
Power Dissipation to +75°C . . . . . 500 mW
Derates above 75°C by . . . . . 6 mW/°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering 10 secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7773JR	0°C to +70°C	R-28
AD7775JR	0°C to +70°C	R-28

*R = Small Outline IC (SOIC). For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



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PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
Power Supplies		
25	V_{CC}	+5 V Power Supply.
9	DGND	Digital Ground.
16 and 23	AGND	Analog Ground.
Microprocessor Interface		
28	$\overline{RD}$	Read Input (Active Low). When active it is used in conjunction with $\overline{CS}$ to read data over the Input/Output bus. See the truth tables for Microprocessor Interfacing.
27	$\overline{WR}$	Write Input (Active Low). When active it is used in conjunction with $\overline{CS}$ to write data over the Input/Output bus.
26	$\overline{CS}$	Chip Select Input (Active Low). The device is selected when this input is low.
Microprocessor Interface—AD7773 Only		
4–8 and 10–14	DB0–DB4, DB5–DB9	Input/Output Data Bus. A 10-bit wide bidirectional data port over which data is transferred into or out of the AD7773. DB0 is the Least Significant Bit.
2	A0	Address Inputs A0 and A1 select one of four registers. See Table I for details.
1	A1	
Microprocessor Interface—AD7775 Only		
4–8 and 10–14	AD0–DB4, DB5–DB9	Multiplexed Address/Data Input/Output Bus. An ALE signal is used to demultiplex the bus. After the falling edge of ALE the address present on AD0–AD3 must be removed and $\overline{WR}$ or $\overline{RD}$ exercised to complete the instruction. The bus now transfers 10 bits of data into or out of the AD7775. AD0 is the Least Significant Bit.
2	ALE	Address Latch Enable Input used to demultiplex the address/data bus. On the falling edge of ALE address inputs AD1–AD3 are internally latched (AD0 is a don't care) and remain latched until ALE returns High. See Table II for details.
1	$\overline{RESET}$	Reset Input (Active Low). Used as a hardware reset for various functional blocks: Loads half-scale code into both DAC registers. Resets the internal ADC register stack Write Pointer to the bottom-most register. Loads Control Register with 364 (Hex). See Control Register Description. Loads Status Register with 3E0 (Hex). See Status Register Description.
Demodulator Channel		
19	$V_{IN}(+)$	Differential Inputs to the input amplifier. Analog input signals to these pins should be capac-
20	$V_{IN}(-)$	itively coupled.
22	$C_{INT}(+)$	The value of capacitor connected between these pins sets the integrator time constant. See
21	$C_{INT}(-)$	under Design Information for choosing the C_{INT} capacitor.
24	CTRL	Control Input. All signal capture operations are controlled by this input. The number of CTRL pulses applied to the device must equal the number of bursts to be captured.
3	CLKIN	Clock input. A clock is required for the ADC. An external TTL-compatible clock must be applied to this input pin. See the T_{CLKIN} specifications for CLKIN information.
Analog Outputs		Each of the two DACs has the same output voltage range given by: $V_{OUT} = V_{BIAS} \pm V_{SWING} = REFOUT \pm V_{SWING}$ With midcode in either DAC register the respective DAC output is equal to REFOUT.
15	$V_{OUT}A$	Analog Output Voltage from DAC A. 1 LSB = 2 V_{SWING}/1024 = REFOUT/1024 =2.1 mV.
18	$V_{OUT}B$	Analog Output Voltage from DAC B. 1 LSB = 2 V_{SWING}/256 = REFOUT/256 = 8.6 mV.
17	REFOUT	Voltage Reference Output. Internally this is used as the reference for the ADC and as the bias level (V_{BIAS}) for the two DACs.

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Individual bit functions are described below. Normally the demodulator channel operates as a synchronous detector to capture complete cycles of a servo burst waveform. However, if CR0 to CR3 are loaded with all 0s, the demodulator channel performs as a simple gated detector stage, gated ON/OFF by the CTRL input. See under CIRCUIT DESCRIPTION—Gated Detector Mode.

CR0 to CR3 determine the number of complete cycles to be synchronously detected within a single burst:

CR3	CR2	CR1	CR0	Cycles
0	0	0	0	Gated Detector
0	0	0	1	NA
0	0	1	0	NA
0	0	1	1	NA
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

CR4 and CR5 determine the number of bursts which are to be captured.

CR5	CR4	Number of Bursts
0	0	1
0	1	2
1	0	3
1	1	4

CR6 determines whether DAC coding is offset binary or twos complement.

CR6	Coding
0	Offset Binary
1	Twos Complement

CR7, CR8 and CR9 are decoded to provide a number of different functions. CR7 determines whether a signal will be acquired via the synchronous detector's differential inputs or direct from the $C_{INT}(+)$ pin. CR7 is ANDed with the internally generated integrate signal INT to make or break the signal path from the rectifier output to the $C_{INT}(+)$ pin. With CR7 low the rectifier output drives the external integrating capacitor on the C_{INT} pins and all input signals are acquired through the $V_{IN}(+)$ and $V_{IN}(-)$ differential input pins. With CR7 high the synchronous detector stage is bypassed and all input signals are now acquired through the single-ended $C_{INT}(+)$ pin.

CR9	CR8	CR7	Function
0	0	X*	Soft Reset
0	1	X	Power Down
1	0	0	Not Allowed
1	0	1	Calibration Mode
1	1	0	Normal Mode
1	1	1	Not Allowed

*X = don't care.

via software or hardware) the control register is loaded with 364 (Hex) as shown below.

CR0	0
CR1	0
CR2	1
CR3	0
CR4	0
CR5	1
CR6	1
CR7	0
CR8	1
CR9	1

Also on receipt of a reset command the status register is loaded with 3E0 (Hex); i.e., locations SR0–SR4 are loaded with all 0s indicating four good burst captures and conversions complete.

Power Down: In the power down mode all linear circuitry is turned off. Both DAC outputs and the REFOUT output are pulled weakly (5 kΩ) to AGND.

Calibration Mode: The purpose of this mode is to allow any channel mismatch which may exist between the four internal track/hold amplifiers to be easily measured. See under CIRCUIT DESCRIPTION—Calibration Mode section.

Normal Mode: This is the normal operating mode and allows external differential input signals to be acquired and converted. The contents of locations CR0–CR3 determine whether the demodulator channel will be in the synchronous detector mode or gated detector mode.

STATUS REGISTER DESCRIPTION

The status register (SR) is the bottom-most register of the 5-deep register stack. It is 10 bits wide and can be written to or read from. Its function is to provide status information on device operation. Location SR0 acts as a BUSY signal for the demodulator channel. SR0 is set high on the rising edge of the first CTRL pulse in a new burst capture sequence and remains high throughout the complete signal acquisition cycle and the subsequent conversion cycle. When the programmed number of conversions are complete, location SR0 is set low. The number of conversions carried out equals the number of bursts captured. This number is programmable from 1 to 4 via locations CR4 and CR5 of the control register. Up to four bursts can be captured and each of these capture operations has an individual status flag, SR1–SR4, associated with it. A logic low or "good" flag in location SR1, for instance, indicates that burst #1 was captured correctly. Alternatively, a logic high or "bad" flag in location SR1 indicates that a problem occurred while capturing burst #1; i.e., for whatever reason, less than the programmed number of cycles in burst #1 were captured. Locations SR5–SR9 of the status register are reserved and must always be read as logic highs for correct operation of the AD7773 and AD7775.

Primarily intended as a read only location, the status register has very limited write functionality. A write to the status register automatically loads all 1s into locations SR0–SR4 regardless of data present on the data bus. These flag settings represent four bad burst captures and conversions incomplete.

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As mentioned previously, locations SR5–SR9 are used for production test purposes and must be written high for correct operation of the AD7773 and AD7775. All write instructions to the status register must load the word 11111XXXXX2. Repeated write instructions to address 11_2 (AD7773) or $011X_2$ (AD7775) are all decoded to the status register.

CIRCUIT DESCRIPTION

The AD7773 and AD7775 are intended primarily for embedded servo head positioning applications in Winchester-type disk drives. The demodulator channel can capture high speed servo data from a variety of embedded servo patterns. Up to four sequential input signals can be captured, converted to digital form and stored in the four data registers ADCREG1–ADCREG4. The 10-bit DAC output can be used to control the head position via a voice coil motor (VCM). The 8-bit DAC output can be used for spindle speed control, gain control, filter control etc. There are two major modes of operation of the demodulator channel—synchronous detector mode and gated detector mode. In the synchronous detector mode the differential input signals are applied in bursts to the differential inputs $V_{IN}(+)$ and $V_{IN}(-)$. A zero crossing detector (ZCD) is used to synchronously detect full cycles of the input signal within a given burst which are then rectified and integrated. Both the number of cycles within an individual burst and also the number of bursts to be captured are programmable. In the gated detector mode the synchronous detector is bypassed and the differential input signals are simply rectified and integrated as long as CTRL remains high. Whether in the synchronous detector mode or in the gated detector mode, a third mode, a calibration or CAL mode, is possible where a reference voltage is connected to the $C_{INT}(+)$ pin to allow any mismatch which exists between the four track/hold (T/H) amplifiers to be easily measured. A simplified diagram of the demodulator channel is shown in Figure 6. With CR7 a logic Low the normal mode is selected and SW1 is closed when a valid integrate INT signal is provided by the demodulator control logic. Switches SW1 and SW3 are functional only in the normal mode. In the calibrate mode CR7 is set to a logic high and SW1 is open regardless of the INT signal. Switch SW2 is closed only in the calibrate mode. The sequence of events in each mode is explained in the following text.

Synchronous Detector Mode

The differential input circuitry is shown in Figure 7. The value of the input capacitors should be chosen so that the pole formed by the capacitor and the 2.5 kΩ equivalent input resistance is at least an order of magnitude below the lowest input signal frequency. These input resistors have a tolerance of ±40% with a typical temperature coefficient of −300 ppm/°C. The differential inputs are biased at approximately 1 V above AGND by means of a low output impedance voltage source.

PRELIMINARY TECHNICAL DATA

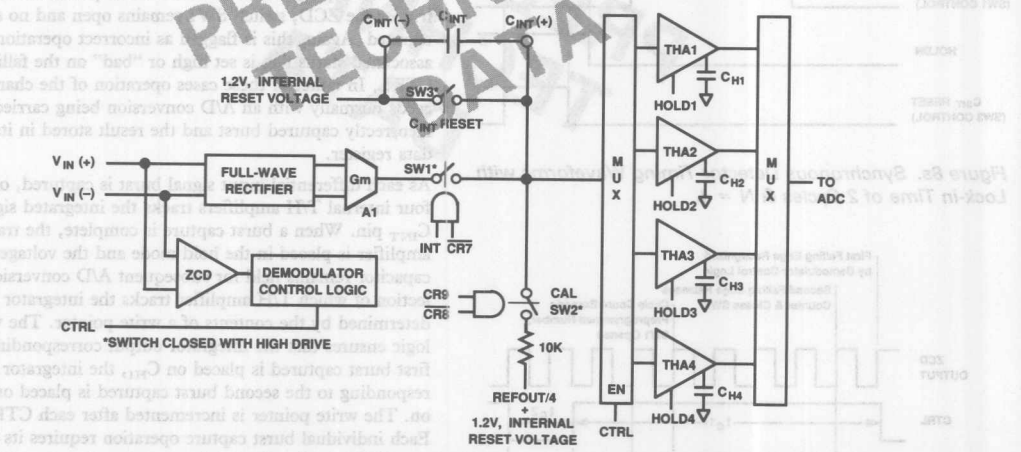


Figure 6. Simplified Block Diagram of Demodulator Channel

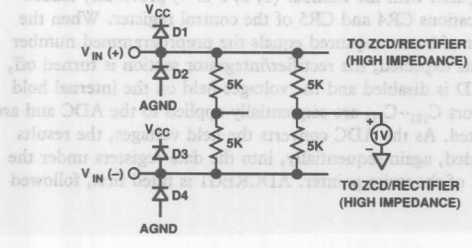


Figure 7. Simplified Input Circuitry of Demodulator Channel

From the input pins the signal passes to both a zero crossing detector (ZCD) and a full wave rectifier. The output of the rectifier drives a transconductance amplifier to convert the rectified input voltage into an output current suitable for charging the external integrating capacitor C_{INT}. Except during actual ADC conversions the ZCD is always enabled and produces a continuous pulse stream output reflecting the differential input signal transitions through 0 V. In fact, the input signal change must exceed the ZCD's input hysteresis, V_H, before its output changes. See Figure 20 in the DESIGN INFORMATION section. Since the ZCD output is usually completely asynchronous

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with the timing of the CTRL input, the main task of the demodulator control logic is to synchronize these two signals in order to integrate only full cycles of the input waveform. This is achieved by initializing the cycle counter logic on the first ZCD output falling edge recognized after CTRL goes high and releasing the counter on the following ZCD output falling edge. This produces the integrate (INT) signal to close switch SW1 to start integrating. Full cycles of the input waveform can now be counted from falling edge to falling edge of the ZCD output. The asynchronous nature of the two signals results in a random lock-in time before the integrator starts, which can vary from 1 cycle to 2 cycles of the input waveform. This is illustrated in Figures 8a and 8b. CTRL must be high for a minimum time of $(N + 3.5)\ t_{CYC}$; i.e., 7.5 cycles of the maximum burst frequency of 5 MHz when N = 4.

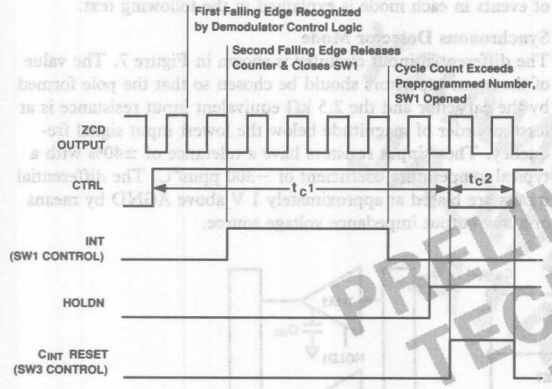


Figure 8a. Synchronous Detector Timing Waveforms with Lock-In Time of 2 Cycles & N = 4.

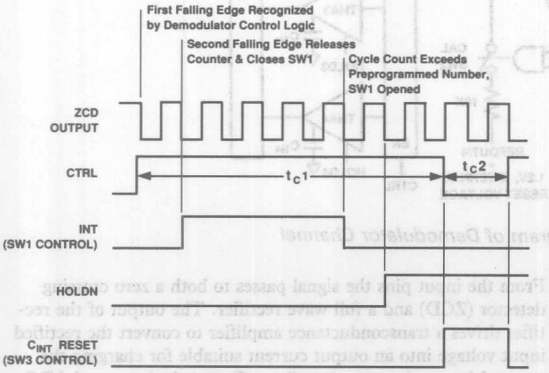


Figure 8b. Synchronous Detector Timing Waveforms with Lock-In Time of 1 Cycle & N = 4.

After the counter is released, the number of subsequent falling edges is counted and is compared with the number previously loaded into locations CR0–CR3 of the control register. When this count exceeds the preprogrammed number, the demodulator control logic brings INT Low, opening switch SW1 to halt the integrator. To ensure that the selected track/hold amplifier correctly acquires the integrated voltage on C_{INT}, a further one full cycle of the ZCD output (i.e., one full cycle of the input waveform) is counted before a hold signal, HOLD1–HOLD4, is generated.

When CTRL returns low, switch SW3 is closed to reset the voltage across the integrating capacitor to 0 V. The waveforms in Figure 8 are drawn for a correct burst capture and the status flag associated with this burst, SR1–SR4, is set "good"—a logic low—in the status register. However, there may be occasions when, for whatever reason, less than the programmed number of cycles occur in a burst, and in these circumstances the trailing edge of CTRL acts as a fail-safe hold signal for the T/H amplifier. For instance if, while capturing a burst, the signal amplitude drops below the minimum ZCD comparator threshold, then the ZCD will obviously cease providing zero-crossing pulses and invalidate the cycle counting logic. In situations like this, the trailing edge of CTRL terminates the integrator directly. If any individual burst capture is terminated by the falling edge of CTRL, then its associated status flag in the status register is set high indicating a "bad" capture. In the situation where an expected burst is so low in amplitude as not even to trigger the ZCD, switch SW1 remains open and no signal is integrated. Again, this is flagged as incorrect operation and its associated status flag is set high or "bad" on the falling edge of CTRL. In either of these cases operation of the channel proceeds normally with an A/D conversion being carried out on the incorrectly captured burst and the result stored in its respective data register.

As each differential input signal burst is captured, one of the four internal T/H amplifiers tracks the integrated signal on the C_{INT} pin. When a burst capture is complete, the tracking T/H amplifier is placed in the hold mode and the voltage on its hold capacitor remains held for subsequent A/D conversion. The selection of which T/H amplifier tracks the integrator output is determined by the contents of a write pointer. The write pointer logic ensures that the integrator output corresponding to the first burst captured is placed on C_{H1}, the integrator output corresponding to the second burst captured is placed on C_{H2} and so on. The write pointer is incremented after each CTRL pulse. Each individual burst capture operation requires its own separate CTRL; pulse, i.e., if there are four bursts to be captured, four CTRL pulses are required. The number of bursts captured is compared with the number (1, 2, 3 or 4) previously loaded into locations CR4 and CR5 of the control register. When the number of bursts captured equals the preprogrammed number of bursts expected, the rectifier/integrator section is turned off, the ZCD is disabled and the voltages held on the internal hold capacitors C_{H1}–C_{H4} are sequentially applied to the ADC and are converted. As the ADC converts the held voltages, the results are loaded, again sequentially, into the data registers under the control of the write pointer. ADCREG1 is filled first, followed

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by ADCREG2, etc. When all held voltages have been converted, the T/H amplifiers are released back into their track mode and the write pointer is left pointing at T/H amplifier #1. At this time also, the ZCD is again enabled. Note, however, that the 4-channel T/H multiplexer is enabled on the rising edge of the first CTRL pulse in a new burst capture sequence and remains enabled only for the duration of the capture sequence.

Gated Detector Mode

In this mode the synchronous detector is bypassed and the demodulator channel behaves as a simple gated detector. To select the gated detector mode, locations CR0–CR3 of the control register are loaded with all 0s, location CR7 is loaded with a logic low and locations CR8 and CR9 are loaded with logic highs. A simplified timing diagram of the channel operating as a gated detector is shown in Figure 9. When CTRL goes high at the start of a signal capture operation, switch SW1 is closed and the integrator starts integrating the rectifier's output. It will continue to do so as long as CTRL remains high, eventually saturating if CTRL is held high for too long. A minimum CTRL high pulse width of 800 ns is required in this mode. When CTRL returns low, switch SW1 is opened and the integrator is halted. As the rectifier's output is being integrated across C_{INT}, it is also being tracked by one of the four T/H amplifiers. To provide additional time for this T/H amplifier to completely acquire the integrated voltage, the falling edge of CTRL triggers a one-shot which delays the hold signal, HOLD1–HOLD4, until it times out. This delay, t_C3, has a maximum time of 600 ns. When the hold signal is generated the tracking T/H amplifier is put in the hold mode and the voltage on its hold capacitor remains held for subsequent A/D conversion. The hold signal, in turn, triggers the C_{INT} reset signal, closing SW3 and resetting the voltage across C_{INT} to 0 V. Note that both plates of the C_{INT} capacitor are at the internal reset voltage level of 1.2 V, available on $C_{INT}(-)$, in readiness for the next signal capture operation. The minimum CTRL low time, t_C2, depends on the duration of the preceding CTRL high time. The longer the integration time, the longer must be the reset time, since the reset current is fixed. The minimum CTRL low time can be determined from the expression:

$$t_C2 = 0.6\ \mu s + 0.375\ t_C1$$

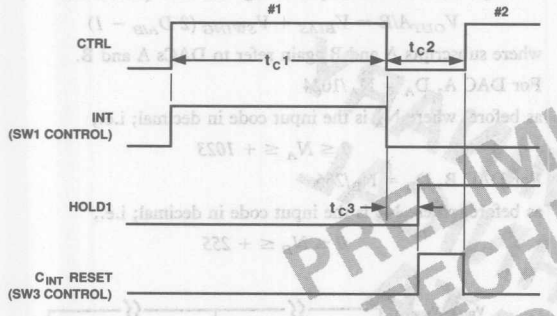


Figure 9. Channel Timing Waveforms for Gated Detector Mode

When the number of gated signals captured equals the preprogrammed number expected, the rectifier/integrator section is disabled and the held voltages are sequentially applied to the ADC and are converted. From here on, channel operation is identical to the synchronous detector mode as previously described. Note that locations SR1–SR4 of the status register now convey no meaningful information and should be ignored for gated detector operation.

Calibration Mode

The purpose of this mode is to allow any channel mismatch existing between the internal T/H amplifiers to be easily measured. The number of T/H amplifiers tested will equal the number stored in locations CR4 and CR5 of the control register. Additionally the number of CTRL pulses applied must also equal this number. The calibration (CAL) mode is selected by loading locations CR9 and CR8 of the control register with a logic high and a logic low, respectively. This condition is decoded to close switch SW2 and connect an internal dc reference, nominally REFOUT/4 above the $C_{INT}(-)$ pin, to the $C_{INT}(+)$ pin. Additionally, to avoid shorting the integrator output, switch SW1 must be opened by loading a logic high into location CR7. Unlike either the synchronous or gated detector modes, the voltage on C_{INT} is not discharged between successive CTRL pulses. In this mode the CTRL pulses simply generate the hold signals for the T/H amplifiers. The falling edge of the first CTRL pulse generates a hold signal, HOLD1, for T/H amplifier #1, the falling edge of the second CTRL pulse generates HOLD2 for T/H amplifier #2, and so on. A timing diagram of the channel in the CAL mode is shown in Figure 10.

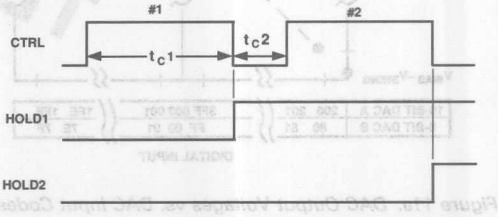


Figure 10. Channel Timing Waveforms for Calibration Mode

A minimum CTRL pulse width of 800 ns is required to allow sufficient acquisition time for the relevant T/H amplifier. Note that this pulse width assumes that the voltage on the $C_{INT}(+)$ pin has settled to the nominal REFOUT/2 level before the first CTRL pulse is applied. In order to use the minimum CTRL pulse widths the demodulator channel must be placed in the calibration mode some time prior to applying the first CTRL pulse. With C_{INT} = 180 pF, this setup time is no longer than 20 μs. Alternatively, this setup time can be avoided by making the first CTRL pulse sufficiently wide to ensure that the calibration voltage on the $C_{INT}(+)$ pin has settled. Subsequent CTRL pulses can obviously have minimum pulse widths.

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PRELIMINARY TECHNICAL DATA

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The AD7773 and AD7775 contain two independent voltage-output DACs: DAC A with 10-bit resolution and DAC B with 8-bit resolution. The two DACs produce output voltages of the form $V_{BIAS} \pm V_{SWING}$. Both V_{BIAS} and V_{SWING} reference levels are generated internally with V_{BIAS} being available externally on the REFOUT pin. V_{SWING} is nominally equal to REFOUT/2. With half-scale code in a DAC register, the DAC output voltage is equal to V_{BIAS}; With a positive full-scale code the DAC output is $V_{BIAS} + V_{SWING} - 1$ LSB; with a negative full-scale code the DAC output is $V_{BIAS} - V_{SWING}$. Dependent upon the logic level stored in location CR6 of the control register, the DAC coding (for both DACs) will be either twos complement coding (CR6 = 1) or offset binary coding (CR6 = 0). Note that on receipt of a reset command (either via software or hardware), location CR6 is loaded with a logic high and the analog outputs of both DACs go to V_{BIAS}. Figures 11a and 11b show the DAC transfer functions for twos complement and offset binary coding, respectively.

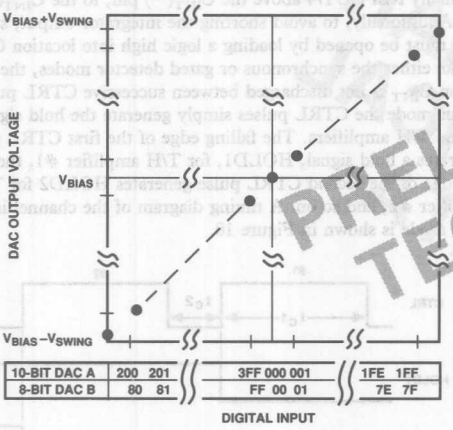


Figure 11a. DAC Output Voltages vs. DAC Input Codes in Hex—Two's Complement Coding

expressed as:

$$V_{OUT}A/B = V_{BIAS} + V_{SWING}(2\ D_{A/B})$$

where subscripts A and B refer to DACs A and B.

For DAC A, $D_A = N_A/1024$

where N_A is the decimal equivalent of the twos complement input code; i.e.,

$$-512 \le N_A \le +511$$

For DAC B, $D_B = N_B/256$

where N_B is the decimal equivalent of the twos complement input code; i.e.,

$$-128 \le N_B \le +127$$

With offset binary coding selected via location CR6 of the control register, the DAC output voltage can be expressed as:

$$V_{OUT}A/B = V_{BIAS} + V_{SWING}(2\ D_{A/B} - 1)$$

where subscripts A and B again refer to DACs A and B.

For DAC A, $D_A = N_A/1024$

as before, where N_A is the input code in decimal; i.e.,

$$0 \le N_A \le +1023$$

For DAC B, $D_B = N_B/256$

as before, where N_B is the input code in decimal; i.e.,

$$0 \le N_B \le +255$$

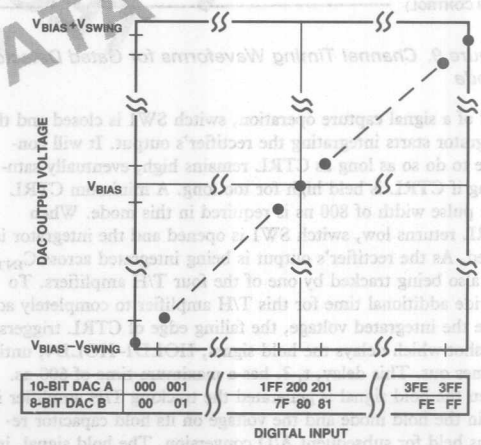


Figure 11b. DAC Output Voltages vs. DAC Input Codes in Hex—Offset Binary Coding

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MICROPROCESSOR INTERFACING

Tables I and II show the truth tables for AD7773 and AD7775 microprocessor interfacing, respectively. The multiplexed address/data bus used by the AD7775 is demultiplexed internally by means of the ALE signal. On the falling edge of ALE address inputs AD1, AD2 and AD3 are latched and remain latched until ALE returns high again. Note that address input AD0 is a "don't care" input. This decoding scheme allows 2-byte word operations to even addresses only and simplifies the interface to the 80C196, for instance, where word operations to odd addresses are not guaranteed to operate in a consistent manner. DAC data is always transferred as right-justified data, i.e., the LSB should always appear on AD0 whether loading the 10-bit DAC A or 8-bit DAC B. Similarly for the AD7773, which has a dedicated 10-bit-wide data bus, DAC data is always transferred as right-justified data, i.e., the LSB should always appear on DB0 whether loading DAC A or DAC B.

Table I. AD7773 Truth Table for Microprocessor Interfacing

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	DB0–DB9	Functions/Comments
1	X*	X	X	X	High Z	Data Port High Impedance.
0	1	0	0	0	DAC Data	Load 10-Bit DAC A Data to DAC A Register.
0	0	1	0	0	Low Z	Reserved. Do Not Use.
0	1	0	0	1	DAC Data	Load 8-Bit DAC B Data to DAC B Register.
0	0	1	0	1	Low Z	Reserved. Do Not Use.
0	1	0	1	0	CR Data	Load Control Register (CR) Data to CR. See Control Register Description.
0	0	1	1	0	Low Z	Reserved. Do Not Use.
0	1	0	1	1	SR Data	Load Status Register (SR) Data to SR. See Status Register Description.
0	0	1	1	1	Stack Data	Contents of Stack Placed on Data Bus. See Stack Reading Description.

*X = don't care.

Table II. AD7775 Truth Table for Microprocessor Interfacing

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	AD3*	AD2*	AD1*	AD0	AD0-DB9	Function/Comments
1	X**	X	X	X	X	X	High Z	Data Port High Impedance.
0	1	0	X	0	0	X	DAC Data	Load 10-Bit DAC A Data to DAC A Register.
0	0	1	0	0	0	X	Low Z	Reserved. Do Not Use.
0	1	0	X	0	1	X	DAC Data	Load 8-Bit DAC B Data to DAC B Register.
0	0	1	0	0	1	X	Low Z	Reserved. Do Not Use.
0	1	0	X	1	0	X	CR Data	Load Control Register (CR) Data to CR. See Control Register Description.
0	0	1	0	1	0	X	Low Z	Reserved. Do Not Use.
0	1	0	X	1	1	X	SR Data	Load Status Register (SR) Data to SR. See Status Register Description.
0	0	1	0	1	1	X	Stack Data	Contents of Stack Placed on Data Bus. See Stack Reading Description.
0	0	1	1	0	0	X	ADC Data	Contents of ADCREG1 Placed on Data Bus.
0	0	1	1	0	1	X	ADC Data	Contents of ADCREG2 Placed on Data Bus.
0	0	1	1	1	0	X	ADC Data	Contents of ADCREG3 Placed on Data Bus.
0	0	1	1	1	1	X	ADC Data	Contents of ADCREG4 Placed on Data Bus.

*Latched internally on the falling edge of ALE.
**X = don't care.

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Stack Reading

The register stack consists of a total of five registers: the status register and the four ADC data registers, ADCREG1–ADCREG4. The status register is the bottom-most register of the 5-deep register stack. Dependent upon the system architecture, the stack can be read in one of two ways. If the AD7773 and AD7775 are interfaced directly to a microprocessor bus then repeated read instructions to the stack address rotate the active stack locations through the data bus. One stack location is transferred per read instruction. This method of stack reading is shown in Figure 12a for the AD7773 (stack address = 11_2) and in Figure 13a for the AD7775 (stack address = $011X_2$). However, if the AD7773 or AD7775 is not directly interfaced to the microprocessor bus but comes through some peripheral controller (e.g., a proprietary gate array), then the stack can be rotated by keeping the $\overline{CS}$ input low and repeatedly pulsing the $\overline{RD}$ input. This method of stack reading is shown in Figures 12b and 13b for the AD7773 and AD7775, respectively.

For the AD7773, stack rotation is the only way in which data in the upper registers can be accessed. For the AD7775, however, the stack registers are individually addressable and the user can choose to access the data by rotating the stack, or by individually addressing the registers in any order preferred.

A read pointer ensures correct operation of the stack by setting equal the number of data registers which can be rotated and the number of bursts to be captured. The first read instruction to the register stack returns the contents of the status register. The read pointer is then incremented so that the next read operation from the stack—using the same address—returns the conversion data from ADCREG1 and so on. If n is the number of bursts to be captured (n = 1, 2, 3 or 4), then n + 1 read instructions are required to rotate the stack through all active stack registers. The stack is rotated only once with all additional read instructions repeatedly placing the contents of the status register on the data bus. Note that the stack will rotate only when the programmed number of conversions are complete; i.e., only when status register flag SR0 has returned low. When new data is loaded to the stack, for example, when a new burst sequence is captured, the read pointer is again enabled to rotate the stack registers through the data bus. Operation of the stack is summarized in Table III where all the read instructions are from stack addresses; 11_2 for the AD7773 and $011X_2$ for the AD7775.

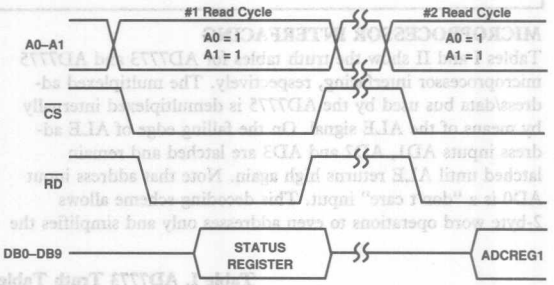


Figure 12a. AD7773 Stack Read Option 1

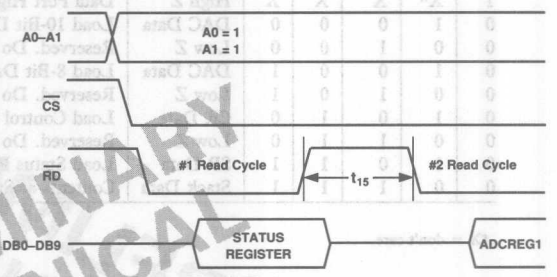


Figure 12b. AD7773 Stack Read Option 2

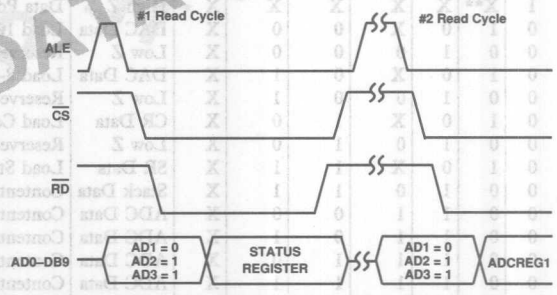


Figure 13a. AD7775 Stack Read Option 1

Table III. Stack Read Operations

Read Instruction Sequence	Data Bus
1st Read	Status Register
2nd Read	ADCREG1
3rd Read	Status Register if CR (5, 4) = (0, 0); ADCREG2 otherwise
4th Read	Status Register if CR (5, 4) = (0, 0) or (0, 1); ADCREG3 otherwise
5th Read	Status Register if CR (5, 4) = (0, 0), (0, 1) or (1, 0); ADCREG4 otherwise
6th Read	Status Register. Succeeding Read instructions always call the Status Register

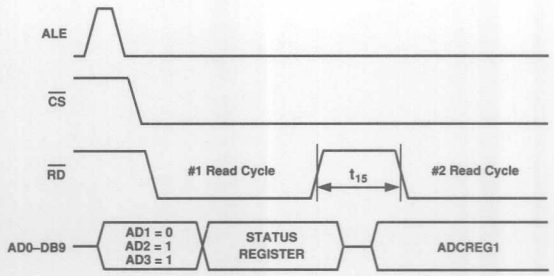


Figure 13b. AD7775 Stack Read Option 2

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Microprocessor/Microcomputer Interfacing Circuits

With its separate data and address bus architecture the AD7773 is intended to interface to DSP machines such as the ADSP-2101, ADSP-2105 and the TMS320 family. The AD7775, with its multiplexed address/data bus, is suitable for microcontrollers such as the 80C196 family.

Figure 14 shows the AD7773 interfaced to the TMS320C10 @ 20.5 MHz and the TMS320C14 @ 25 MHz. Figure 15 shows the interface with the TMS320C25 @ 40 MHz. Note that one wait state is required with this interface. The ADSP-2101-50 and the ADSP-2105-40 interface is shown in Figure 16. One wait state is required with either of these machines.

Figure 17 shows the AD7775 interface to the 80C196KB @ 12 MHz and the 80C196KC @ 16 MHz. One wait state is required with the 16 MHz machine. The 80C196 is configured to operate with a 16-bit multiplexed address/data bus.

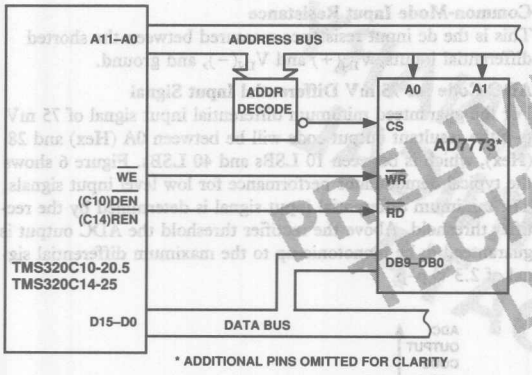


Figure 14. AD7773 to TMS320C10 & -C14 Interface

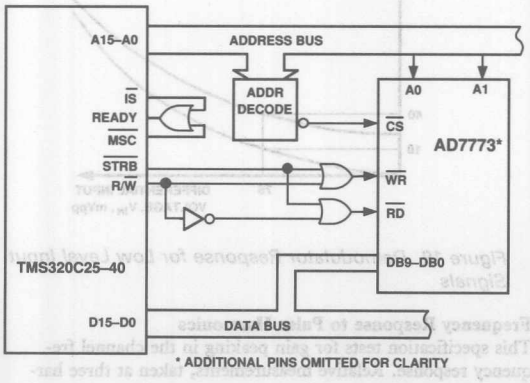


Figure 15. AD7773 to TMS320C25 Interface

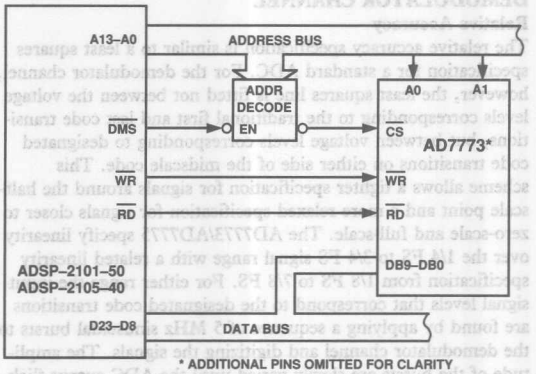


Figure 16. AD7773 to ADSP-2101 & ADSP-2105 Interface

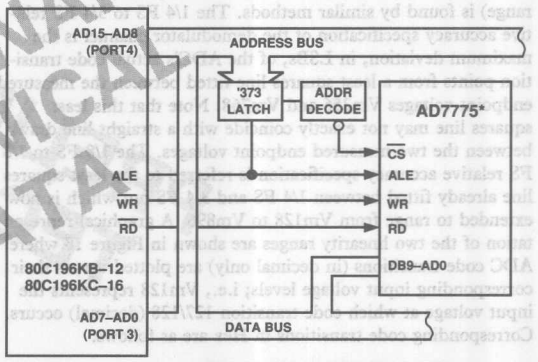


Figure 17. AD7775 to 80C196 Interface

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DEMODULATOR CHANNEL

Relative Accuracy

The relative accuracy specification is similar to a least squares specification for a standard ADC. For the demodulator channel, however, the least squares line is fitted not between the voltage levels corresponding to the traditional first and last code transitions, but between voltage levels corresponding to designated code transitions on either side of the midscale code. This scheme allows a tighter specification for signals around the half-scale point and a more relaxed specification for signals closer to zero-scale and full-scale. The AD7773/AD7775 specify linearity over the 1/4 FS to 3/4 FS signal range with a related linearity specification from 1/8 FS to 7/8 FS. For either range the input signal levels that correspond to the designated code transitions are found by applying a sequence of 5 MHz sinusoidal bursts to the demodulator channel and digitizing the signals. The amplitude of the bursts are slowly varied until the ADC output flickers around the nominated code transition. The burst amplitude which causes the transition is now designated as one endpoint for the linearity specification. The other endpoint (for the same range) is found by similar methods. The 1/4 FS to 3/4 FS relative accuracy specification of the demodulator channel is the maximum deviation, in LSBs, of the ADC's actual code transition points from a least squares line fitted between the measured endpoint voltages Vm256 and Vm768. Note that this least squares line may not exactly coincide with a straight line drawn between the two measured endpoint voltages. The 1/8 FS to 7/8 FS relative accuracy specification is referred to the least squares line already fitted between 1/4 FS and 3/4 FS but which is now extended to range from Vm128 to Vm896. A graphical representation of the two linearity ranges are shown in Figure 18 where ADC code transitions (in decimal only) are plotted versus their corresponding input voltage levels; i.e., Vm128 represents the input voltage at which code transition 127/128 (decimal) occurs. Corresponding code transitions in Hex are as follows:

Vm128: 07F/ 080 (Hex)
Vm256: 0FF/100 (Hex)
Vm768: 2FF/300 (Hex)
Vm896: 37F/380 (Hex)

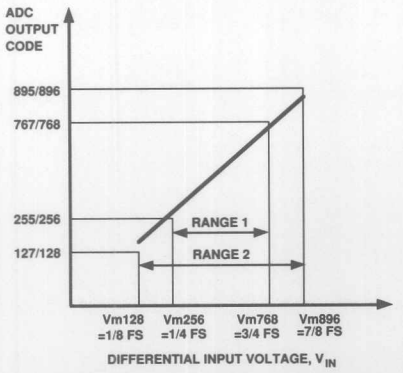


Figure 18. Guaranteed Linearity Ranges for the Demodulator Channel

The full-scale (FS) input voltage is computed from measured voltages Vm128 and Vm896, corresponding to 1/8 FS and 7/8 FS, respectively, as follows:

$$Vm896 - Vm128 = 7/8FS - 1/8\ FS$$

or

$$FS = 8/6\ (Vm896 - Vm128)$$

Using this value of FS, 1 LSB = FS/1024. Note that due to both the zero-crossing detector threshold and the rectifier threshold, the least squares line shown in Figure 18 will not pass through the origin. This means that the differential input voltages shown in Figure 18 are not referenced to the origin; i.e., the code transition 127/128 does not necessarily occur 1/8 FS above V_{IN} = 0 V.

Differential Input Resistance

This is the dc input resistance measured between $V_{IN}(+)$ and $V_{IN}(-)$.

Common-Mode Input Resistance

This is the dc input resistance measured between the shorted differential inputs, $V_{IN}(+)$ and $V_{IN}(-)$, and ground.

ADC Code for 75 mV Differential Input Signal

For the guaranteed minimum differential input signal of 75 mV p–p the resultant output code will be between 0A (Hex) and 28 (Hex), which is between 10 LSBs and 40 LSBs. Figure 6 shows the typical demodulator performance for low level input signals. The minimum differential input signal is determined by the rectifier threshold. Above the rectifier threshold the ADC output is guaranteed to be monotonic up to the maximum differential signal of 2.3 V p–p.

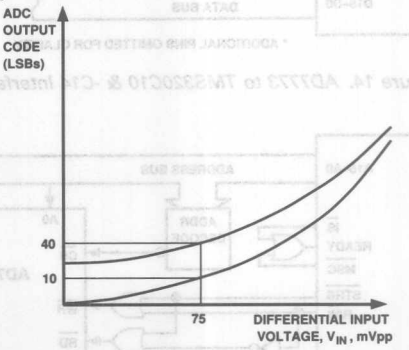


Figure 19. Demodulator Response for Low Level Input Signals

Frequency Response to Pulse Harmonics

This specification tests for gain peaking in the channel frequency response. Relative measurements, taken at three harmonically related frequencies, are compared and must be within specification. To maintain a constant integral at each frequency, the number of cycles are correspondingly increased as the signal period is decreased.

–Set up 5 MHz bursts at 0.7 V p–p and digitize. CR0–CR3 set for 4 cycles. Determine average ADC code, call it Code 1.

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–Set up 10 MHz bursts at 0.7 V p–p and digitize. CR0–CR3 set for 8 cycles. Determine average ADC code, call it Code 2.

–Set up 15 MHz bursts at 0.7 V p–p and digitize. CR0–CR3 set for 12 cycles. Determine average ADC code, call it Code 3.

–Compare (Code 1–Code 2) and (Code 1–Code 3) to the limits specified.

Due to the demodulation technique used in the AD7773 and AD7775, the frequency spectrum of the input signal can have an impact on the demodulator channel performance. To meet the specifications the following limits are placed on the harmonic content of the input signal (quoted in dB relative to a fundamental at 5 MHz and 1.25 V p–p):

2nd Harmonic:	−50 dB
3rd Harmonic:	−12 dB
4th Harmonic:	−50 dB
5th Harmonic:	−24 dB
Higher Harmonics:	−40 dB total

Common-Mode Rejection Ratio

Common-mode rejection ratio (CMRR) is a measure of the change in digital output code when both inputs are changed by equal amounts. Repeated bursts of half-scale amplitude, differential 1.25 V p–p at 5 MHz, are applied to the demodulator channel and digitized. These bursts sit on a common-mode signal of 500 mV p–p magnitude and varying in frequency from 60 Hz to 30 kHz. The standard deviation of the resultant distribution of ADC codes is checked to be less than 3.1 LSBs, a result which includes the channel noise level. When corrected for the channel noise level by rms subtraction, e.g., $\{(3.1)^2 - (1.8)^2\}^{1/2}$, the standard deviation is found to be less than 2.5 LSBs, which is equivalent to a CMRR of 46 dB. This specification holds over the allowable V_{CC} range of 4.75 V to 5.25 V.

Power Supply Rejection Ratio

For the demodulator channel, power supply rejection ratio (PSRR) is a measure of the change in digital output code due to a change in the power supply voltage. Repeated bursts of half-scale amplitude, differential 1.25 V p–p at 5 MHz, are applied to the input and digitized. An ac signal, 200 mV p–p amplitude and varying in frequency from 60 Hz to 30 kHz, is summed with the +5 V power supply V_{CC}. The standard deviation of the resultant distribution of ADC codes is checked to be less than 4 LSBs, a result which includes the channel noise level. When corrected for the channel noise level by rms subtraction, e.g., $\{(4)^2 - (1.8)^2\}^{1/2}$, the standard deviation is found to be less than 3.6 LSBs, which is equivalent to a PSRR of 43 dB. This specification holds over the allowable V_{CC} range of 4.75 V to 5.25 V.

Channel Noise Level

Channel noise level is a measure of the intrinsic noise level of the modulator channel in the absence of common-mode signals and power supply interference. Repeated bursts of half-scale amplitude, differential 1.25 V p–p at 5 MHz, are applied to the input and digitized. The standard deviation of the resultant distribution of ADC codes is checked to be less than 1.8 LSBs. This is equivalent to a channel noise level of 49 dB. Note that the duration of the burst capture sequence must be less than or equal to 1 ms.

Composite Noise Rejection

Intended as an overall channel performance indicator, the composite noise rejection figure is an rms summation of the PSRR, CMRR, the channel noise level as defined above plus an INL error of 1.15 LSBs, representing the standard deviation, under identical test conditions, of the ADC codes from device to device. It is referenced to half-scale.

Channel Mismatch

Channel mismatch is a measure of the differences which may exist between the four internal track/hold (T/H) amplifiers. To measure mismatch the AD7773/AD7775 must be put in the calibration (CAL) mode by loading control register locations CR9 and CR8 with a logic high and a logic low, respectively. Additionally, CR7 must be loaded with a logic high. These conditions disconnect the output of the integrator from the integrating capacitor C_{INT} and connect an internal dc reference (Nominally REFOUT/4 above the voltage on the $C_{INT}(-)$ pin) to the $C_{INT}(+)$ pin. The remainder of the demodulator channel operates normally: under the control of the CTRL input, the four T/H amplifiers are connected in turn to track-and-hold this reference voltage. Subsequently the held voltages are converted. Check the ADC output code for each channel to ensure results are within 5 LSBs of each other. See under CIRCUIT DESCRIPTION for Calibration Mode section.

Crosstalk Between Bursts

Between successive bursts the integrating capacitor C_{INT} is discharged to 0 V. This occurs during time t_C2 of Figures 8a, 8b and 9. Note that both plates of the C_{INT} capacitor are at the internal reset voltage level of 1.2 V, available on $C_{INT}(-)$. Any residual signal on this capacitor will be added to the integrated signal of the succeeding burst causing an apparent increase in the amplitude of that burst. The crosstalk specification defines by how much the amplitude of a burst is influenced by a preceding burst. By this definition the first burst suffers no crosstalk, the second burst suffers from the first burst, etc. To measure crosstalk a special burst sequence is applied to the demodulator input which keeps the amplitude of the burst under test constant at half-scale (differential 1.25 V p–p at 5 MHz) and alternates the amplitude of the preceding burst between 0 V and full scale. The average error due to crosstalk should be less than 1 LSB. Only two successive bursts are exercised in any one sequence.

ADC Conversion Time

Each conversion takes 14 CLKIN cycles. However, due to the asynchronous relationship between CLKIN and the burst detector operation, it is possible to get a delay of up to 2.5 CLKIN cycles before the first conversion actually starts. This means that the first conversion may not be finished for up to 14 + 2.5 CLKIN cycles after the final burst has been detected. Subsequent conversions will always take 14 CLKIN cycles.

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ANALOG OUTPUTS

Relative Accuracy

For the DACs, relative accuracy or end-point nonlinearity is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A graphical representation of the transfer curves for both twos complement and offset binary coding are shown in Figures 11a and 11b, respectively.

Differential Nonlinearity

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity.

Bias Offset Error

If the DACs are ideal, the output voltage of any DAC with midscale code loaded will be equal to V_{BIAS} (i.e., REFOUT). The DAC bias offset error is the difference between the actual output voltage and V_{BIAS}, expressed in LSBs.

Plus and Minus Full-Scale Error

The DACs in the AD7773/AD7775 can be considered to provide bipolar output voltage ranges which are referred to V_{BIAS} instead of AGND. Plus full-scale error for any DAC is the difference, expressed in LSBs, between the actual output voltage with plus full-scale code loaded into the DAC register and the ideal output voltage (V_{BIAS} + V_{SWING} − 1 LSB). Minus full-scale error is similarly defined but the DACs are now loaded with their minus full-scale codes and the ideal output voltage is now V_{BIAS} − V_{SWING}. Note that plus and minus full-scale errors for the DAC outputs are referenced to REFOUT/2 and are measured after the bias offset errors have been adjusted out.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the digital inputs change state with the DAC selected. It is normally specified as the area of the glitch in nV secs and is measured when the digital input code is changed by 1 LSB at the major carry transition. Regardless of whether offset binary or 2s complement coding is used, the major carry transition occurs at the analog output voltage change of V_{BIAS} to V_{BIAS} − 1 LSB or vice versa.

Digital Feedthrough

Digital feedthrough is also a measure of the impulse injected into the analog output from the digital inputs but is measured when the DAC is not selected. It is essentially feedthrough across the die and package. It is important in the AD7773/AD7775 since it is a measure of the glitch impulse transferred to the analog output when data is transferred over the data bus (either in or out). It is specified in nV secs and is measured with a full-scale code change on the data bus, from all 0s to all 1s and vice versa.

Power Supply Rejection Ratio

For the analog outputs, power supply rejection ratio (PSRR) is a measure of the change in the analog output of either DAC due to a change in the power supply voltage V_{CC}. For the test both DACs are loaded with their half-scale codes and an ac signal of 200 mV p–p amplitude and varying in frequency from 60 Hz to 30 kHz is summed with the +5 V power supply. The maximum output signal level on either DAC will be 22 mV. Thus, the response will be at least 20 dB below the excitation level. This specification holds over the allowable V_{CC} range of 4.75 V to 5.25 V.

DESIGN INFORMATION

Choosing the C_{INT} Capacitor

In both the synchronous detector and gated detector modes the differential input signal is rectified and integrated across the integrating capacitor C_{INT}. The correct value of integrating capacitor must be used in order to optimize the channel performance for any particular integration period. If too high a value is chosen then the integrated signal voltage developed across C_{INT} will be lower than optimum, and hence, ADC resolution will be lost due to this effective compression of the signal. Similarly too low a value for C_{INT} can lead to signal voltages being developed across C_{INT} which are beyond the dynamic range of the ADC. This effective signal expansion results in loss of ADC resolution for full-scale input signals. The ideal value of C_{INT} is found from the expression:

$$C_{INT} = I.T/V_{C_{INT}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

where I is the average rectifier output current, T is the integrate time and V_{CINT} is the integrated voltage across C_{INT}. The average rectifier output current can be expressed as:

$$I = Gm.V_{IN}\ (average)$$
$$= Gm.V_{IN}\ peak.\ (Crest\ Factor)$$
$$= Gm\ (V_{IN}\ p\text{–}p/2)\ (Crest\ Factor)$$

For sinusoidal burst signals the crest factor is equal to $2/\pi$.

In the synchronous detector mode the integrate time can be expressed as:

$$T = t_{INTEGRATE}$$
$$= N.t_{CYC}$$
$$= N/f_{IN}$$

where N is the number programmed into locations CR0–CR3 of the control register. N can range from 4 to 15. Frequency f_{IN} is the frequency of the input signal. The AD7773 and AD7775 are guaranteed to operate with N = 4 and f_{IN} = 5 MHz maximum. In the gated detector mode the integrate time is simply the period of CTRL high or t_{C1} in Figure 9.

V_{CINT} is the voltage change across C_{INT} which results in a full-scale change in the ADC output. V_{CINT} is typically equal to REFOUT/2 or 1.07 V.

As an example of calculating a value for C_{INT} consider the case of synchronous detector operation with N = 4, f_{IN} = sinusoidal 5 MHz and V_{IN} p–p = 2.3 V maximum. To ensure that no ADC resolution is lost for peak input signals, Equation 1 is solved using the maximum value of transconductance, Gm = 0.302 ms and the minimum value of V_{CINT} which is equal to REFOUT(min)/2 or 1.05 V. When these values are used in Equation 1 a value for C_{INT} equal to 170.7 pF is computed. This computed value of capacitor must include the tolerance, Δ, on the final capacitor chosen plus any stray capacitance on the C_{INT}(+) pin to ground and C_{INT}(−). That is,

$$170.7\ pF = C_{INT}\ (1 - \Delta\%/100) + C_{STRAY}$$

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If 5% tolerance capacitors are used and C_{STRAY} = 10 pF then C_{INT} = 169 pF ±5%. This is the optimum value of capacitor to use. However, if preferred values of capacitors are required, the next highest preferred value is 180 pF. This value of capacitor will result in a slight compression of the signal range. That is, a full-scale input signal, V_{IN} p–p = 2.3 V, will result in an ADC code which is less than all 1s. Exactly how much compression is caused by using a nonideal value of C_{INT} is indicated by the ratio of computed C_{INT} value to worst case C_{INT} value. Assuming C_{INT} = 180 pF ±5% and stray capacitance totalling 10 pF, the worst case C_{INT} capacitance can be found by solving

$$C_{INT} = 180\ (1 + 5/100)\ pF + 10\ pF$$
$$= 199\ pF$$

The ratio of 170.7 pF, the computed value for C_{INT}, to 199 pF gives the amount of compression, 170.7/190 = 0.85. This means that for a full-scale input signal the ADC code will never exceed 85% of its possible code range; therefore, approximately the top 150 codes will never be used.

Zero Crossing Detector

The zero crossing detector (ZCD) has a certain amount of hysteresis to prevent noise from getting through the input stage. The ZCD differential hysteresis, V_H, is typically 55 mV p–p and is specified to lie between 40 and 70 mV p–p. Only signals which exceed this level can change the ZCD's output. A 55 mV hysteresis represents approximately 5% of a typical 1.1 V differential input signal level to the demodulator channel. Figure 20 gives a graphical representation of the ZCD sensitivity and hysteresis.

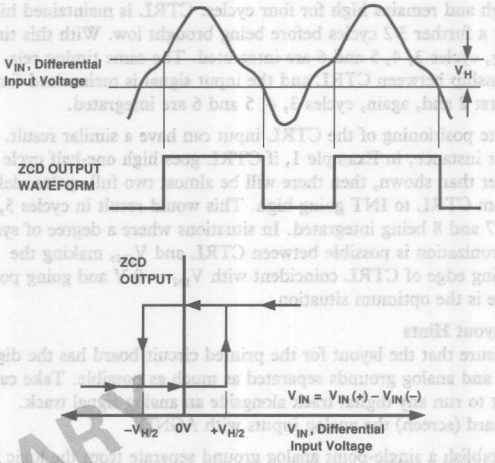


Figure 20. Zero Crossing Detector (ZCD) Sensitivity

Synchronous Detector Timing Relationships

The relative timing between an input burst signal and its respective CTRL pulse determines which of the cycles within an individual burst are integrated. Two different timing examples which result in different cycles of the input waveform being integrated are shown in Figure 21. This is drawn for a two-burst pattern with N, the programmed number of cycles to be captured, set to 4.

In Example 1, the CTRL input goes high just after the rising edge of the ZCD output which itself occurs in the middle of the second cycle of burst 1. Approximately 3/2 cycles after this, the integrate (INT) signal goes high to start the integrator and remains high for four cycles of the input waveform. The CTRL input is maintained high for a further 2 cycles of the input waveform. With this timing relationship, cycles 4, 5, 6 and 7 of burst 1 are integrated. Since CTRL is kept low for the minimum time of 3/2 cycles of the captured input waveform, the same timing relationship between CTRL and the input signal is maintained for burst 2 and, again, cycles 4, 5, 6 and 7 are integrated.

In Example 2, the CTRL input goes high just after the falling edge of the ZCD output at the start of the first cycle of burst 1.

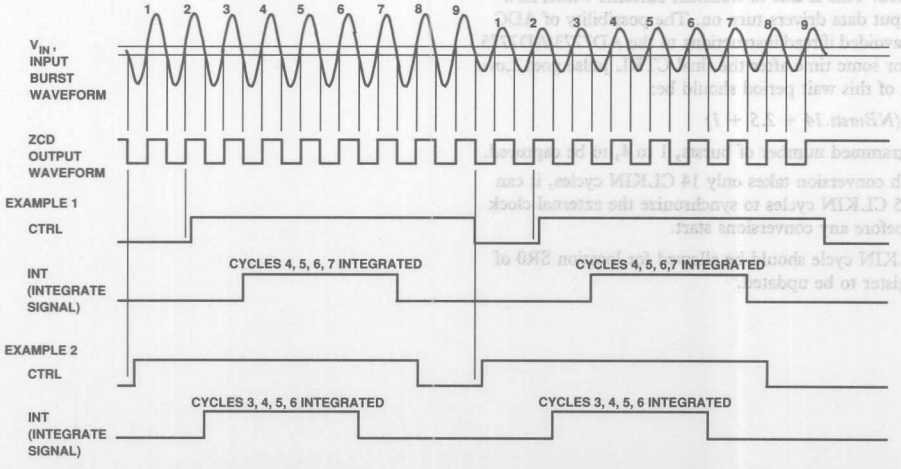


Figure 21. Two Examples of Movement of the Integration Window as a Result of Relative Timing Between CTRL and the Input Burst Signal

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Approximately 2 cycles later the integrate signal, INT, goes high and remains high for four cycles. CTRL is maintained high for a further 3/2 cycles before being brought low. With this timing, cycles 3, 4, 5 and 6 are integrated. The same timing relationship between CTRL and the input signal is maintained for burst 2 and, again, cycles 3, 4, 5 and 6 are integrated.

Late positioning of the CTRL input can have a similar result. For instance, in Example 1, if CTRL goes high one-half cycle later than shown, then there will be almost two full cycles, delay from CTRL to INT going high. This would result in cycles 5, 6, 7 and 8 being integrated. In situations where a degree of synchronization is possible between CTRL and V_{IN}, making the rising edge of CTRL coincident with V_{IN} = 0 V and going positive is the optimum situation.

Layout Hints

Ensure that the layout for the printed circuit board has the digital and analog grounds separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog inputs with AGND.

Establish a single-point analog ground separate from the logic system ground and as close as possible to the AD7773 or AD7775. Both AGND pins on the AD7773/AD7775 and all other signal grounds should be connected to this single-point analog ground. In turn, this star ground should be connected to the digital ground at one point only—preferably at the low impedance power supply itself.

Low impedance analog and digital power supply common returns are important for correct operation of the devices, so make the foil width for these tracks as wide as possible.

In order to ensure a low impedance +5 V power supply at the actual V_{CC} pin, it will be necessary to employ bypass capacitors from the pin itself to DGND. A 4.7 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor is sufficient.

ADC Corruption

Executing a read instruction to the AD7773/AD7775 while conversions are in progress can result in the conversion-in-progress being corrupted. This is due to transient currents which flow when the output data drivers turn on. The possibility of ADC corruption is avoided if read instructions to the AD7773/AD7775 are avoided for some time after the final CTRL pulse goes Low. The duration of this wait period should be:

$$T_{CLKIN}\ (NBursts.14 + 2.5 + 1)$$

N is the programmed number of bursts, 1 to 4, to be captured.

Although each conversion takes only 14 CLKIN cycles, it can take up to 2.5 CLKIN cycles to synchronize the external clock with CTRL before any conversions start.

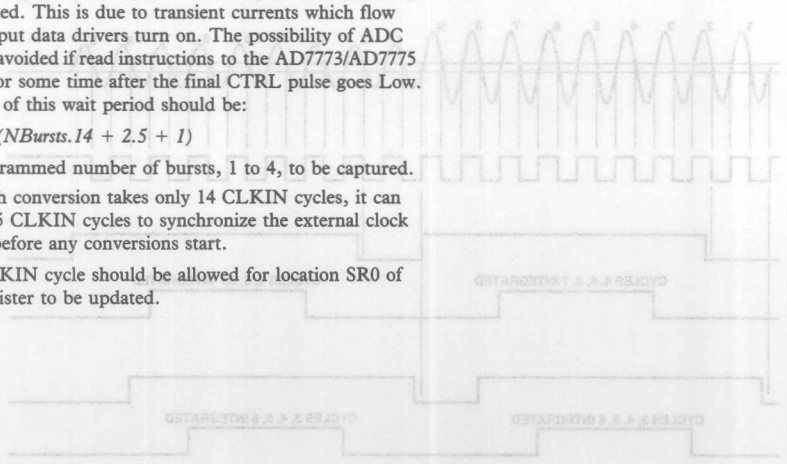
A further CLKIN cycle should be allowed for location SR0 of the status register to be updated.

Changing Modes of Operation

The AD7773 and AD7775 have two normal operating modes—synchronous detector and gated detector modes – and one calibration mode. Changing between any of these modes simply requires changing the appropriate contents of the control register as already described under the individual descriptions of these modes. However, there are a number of considerations which should be followed when changing between modes. The first is that no mode change be attempted before the burst capture and conversion sequence is complete (i.e., not until location SR0 of the Status Register returns low). This will avoid any inadvertent corruption of a conversion in progress. The second consideration involves the delay between writing to the control register and starting a new burst capture sequence. This time is defined under the Demodulator Timing Characteristics as the $\overline{WR}$ rising edge to CTRL rising edge and is specified as 200 ns minimum. It is required to ensure that the correct conditions have been set up internal to the device.

A final consideration involves allowing sufficient time for the integrating capacitor, C_{INT}, to discharge when changing from the calibration mode to one of the other operating modes. This is necessary since, in this mode, C_{INT} is not discharged by the internal discharge switch, SW3, either between successive CTRL pulses or even on completion of the burst capture sequence. A discharge time of 300 ns—equivalent to t_c2, the CTRL low time in the calibration mode—is adequate after transferring out of the calibration mode. This discharge time and the previous set up time of 200 ns must be added together to arrive at a final overall delay.

PRELIMINARY TECHNICAL DATA



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

LC²MOS Analog I/O Port

AD7774

FEATURES
Four-Channel, 8-Bit, 3.6 µs ADC
Three DACs with On-Chip Amplifiers:
One 11-Bit, 8 µs DAC
Two 8-Bit, 4 µs DACs
Simultaneous/Independent Sampling of Input Channels
Adjustable Span and Bias Voltage for Input Channels
Adjustable Bias Voltage for Output Channels
Operates from +5 V and +12 V Supplies

APPLICATIONS
HDD Dedicated Servo
HDD Hybrid Servo
Closed-Loop Servo Systems

GENERAL DESCRIPTION

The AD7774 is a complete analog I/O port comprising three DACs (two 8-bit and one 11-bit) with output amplifiers, four input channels, two track/hold amplifiers and an 8-bit ADC. It has versatile input and output signal-conditioning features which make it ideal for use in head-positioning servos in dedicated-only and combined dedicated/embedded disk systems and other closed-loop digital servo systems.

The part contains four input channels, grouped in pairs. V_{A1} and V_{A2} share a common track/hold amplifier, Track/Hold A, while V_{B1} and V_{B2} share Track/Hold B. Either single or double conversions can be performed. In single conversion mode, any one of the four input channels can be converted. In double conversion mode, either V_{A1} and V_{B1} or V_{A2} and V_{B2} are simultaneously held by Track/Hold A and Track/Hold B, and the held voltages are sequentially converted.

The center point of the transfer function (the bias voltage) can be set for all input and output channels. This makes the AD7774 especially useful in disk drives, where only a positive supply rail is available, as it allows the analog input and output voltages to be referred to a point other than analog ground. In addition, the input span (the swing around the bias voltage) can be set for the input channels. The output span for all three channels is set by the on-chip reference.

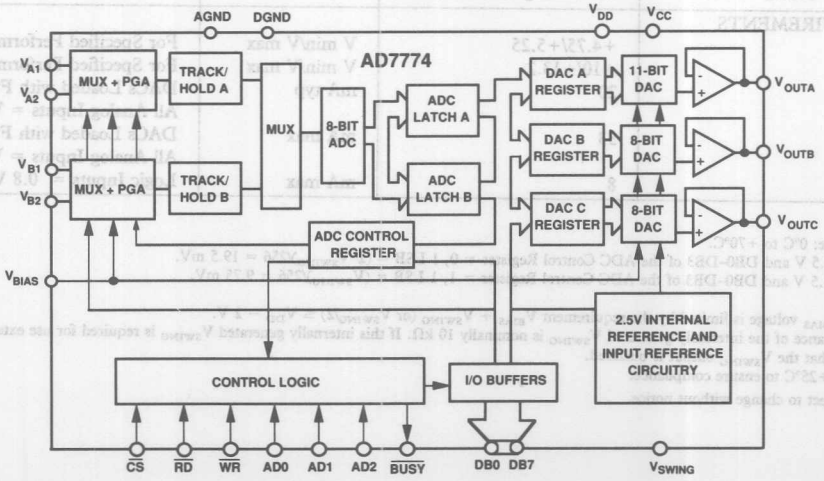
The AD7774 operates from +5 V and +12 V supplies. It is fabricated in Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 28-lead dual-in-line (DIP) package and in a 28-terminal plastic leaded chip carrier (PLCC) package.

PRODUCT HIGHLIGHTS

1. The AD7774 contains a four-channel, 3.6 µs ADC with input signal conditioning and three DACs with output amplifiers and output signal conditioning, on a single chip.
2. The midpoint of the ADC transfer function, the input voltage swing of the ADC and the midpoint output voltage of the DACs can be set by applying ground referenced control voltages.
3. The AD7774 interface timing is compatible with most modern microcontrollers and digital signal processors.

8

FUNCTIONAL BLOCK DIAGRAM



Parameter	K Version[1]	Units	Conditions/Comments
DC ACCURACY			
Resolution[2]	8	Bits	
Relative Accuracy[3]	±1	LSB max	
Differential Nonlinearity[3]	±1	LSB max	No Missing Codes
Bias Offset Error[3]	±5	LSB max	
Relative Offset Error[3]	±2	LSB max	
Full-Scale Error[3]	±5	LSB max	
ANALOG INPUTS			
Input Voltage Range			
All Inputs	$V_{BIAS} \pm V_{SWING}$	V min to V max	DB0–DB3 of ADC Control Register = 0
All Inputs	$V_{BIAS} \pm V_{SWING}/2$	V min to V max	DB0–DB3 of ADC Control Register = 1
Input Current	±1	mA max	
REFERENCE INPUTS			
Input Voltage Levels			
V_{BIAS}[4]	+3 to +6.8	V min to V max	With Respect to AGND
V_{SWING}			
Internally Generated	+2.325 to +2.675	V min to V max	2.5 V ±7%; Available on V_{SWING} Pin[5]
Internal Tempco	±50	ppm/°C typ	
Externally Applied	+2 to +3	V min to V max	With Respect to AGND for Specified Performance
Input Current			
V_{BIAS} Input	1.5	mA max	
V_{SWING} Input	±100	μA min/μA max	
LOGIC OUTPUTS			
DB0–DB7, $\overline{BUSY}$			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 200 μA
Floating State Leakage Current	±10	μA max	
Floating State Capacitance[6]	10	pF max	
Output Coding	2s Complement		
LOGIC INPUTS	See DAC Specifications		
CONVERSION TIME	See Timing Characteristics		
POWER REQUIREMENTS			
V_{CC} Range	+4.75/+5.25	V min/V max	For Specified Performance
V_{DD} Range	+10/+13.2	V min/V max	For Specified Performance
I_{DD}	20	mA typ	DACs Loaded with Full Scale; All Analog Inputs = V_{BIAS}
I_{DD}	33	mA max	DACs Loaded with Full Scale; All Analog Inputs = V_{BIAS}
I_{CC}	8	mA max	Logic Inputs = 0.8 V or 2.4 V

NOTES

[1]Temperature range: 0°C to +70°C.

[2]With V_{SWING} = 2.5 V and DB0–DB3 of the ADC Control Register = 0, 1 LSB = (2*V_{SWING})/256 = 19.5 mV.
With V_{SWING} = 2.5 V and DB0–DB3 of the ADC Control Register = 1, 1 LSB = (V_{SWING})/256 = 9.75 mV.

[3]See Terminology.

[4]The maximum V_{BIAS} voltage is limited by the requirement $V_{BIAS} + V_{SWING}$ (or $V_{SWING}/2$) ≤ V_{DD} − 2 V.

[5]The source impedance of the internally generated V_{SWING} is nominally 10 kΩ. If this internally generated V_{SWING} is required for use external to the AD7774, it is recommended that the V_{SWING} output is buffered.

[6]Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

DAC SPECIFICATIONS

(V_{DD} = +10 V to +13.2 V; V_{CC} = +5 V ± 5%; AGND = DGND = 0 V; V_{BIAS} = +5 V; R_L = 10 kΩ, C_L = 100 pF to AGND.[1] All specifications T_{min} to T_{max} unless otherwise stated.)

Parameter	K Version[2]	Units	Conditions/Comments
STATIC PERFORMANCE			
DAC A			
Resolution[3]	11	Bits	
Relative Accuracy[4]	±2	LSB max	
Differential Nonlinearity[4]	±1	LSB max	Guaranteed Monotonic
Bias Offset Error[4]	±50	mV max	
Full-Scale Error[4]	±50	mV max	
DAC B, DAC C			
Resolution[3]	8	Bits	
Relative Accuracy[4]	±1	LSB max	
Differential Nonlinearity[4]	±1	LSB max	Guaranteed Monotonic
Bias Offset Error[4]	±5	LSB max	
Full-Scale Error[4]	±5	LSB max	
ANALOG OUTPUTS			
Output Voltage Range			
All Outputs	$V_{BIAS} - V_{SWING}$ or 1.0	V min	Whichever Is the Higher
	$V_{BIAS} + V_{SWING}$ or $V_{DD} - 2.0$	V max	Whichever Is the Lower
dc Output Impedance	0.5	Ω typ	
REFERENCE INPUTS			
Input Voltage Levels			
V_{BIAS}[5]	+3 to +6.8	V min to V max	With Respect to AGND
V_{SWING}			
Internally Generated	+2.325 to +2.675	V min to V max	2.5 V ±7%; Available on the V_{SWING} Pin[6, 7]
Internal Tempco	±50	ppm/°C typ	
Input Current	As Per ADC Specifications		
AC CHARACTERISTICS[8]			
Voltage Output Settling Time			
DAC A			
Full-Scale Change	3	μs max	Settling Time to Within ±1/2 LSB of Final Value
DAC B, DAC C			
Full-Scale Change	2	μs max	Settling Time to Within ±1/2 LSB of Final Value
Digital-to-Analog Glitch Impulse[4]	15	nV sec typ	
Digital Feedthrough[4]	1	nV sec typ	
LOGIC INPUTS			
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, AD0–AD2, DB0–DB7			
Input Low Voltage, V_{INL}	0.8	V max	
Input High Voltage, V_{INH}	2.4	V min	
Input Leakage Current	10	μA max	
Input Capacitance[8]	10	pF max	
DB0–DB7			
Input Coding	2s Complement		
POWER REQUIREMENTS	See ADC Specifications		

NOTES

[1]The DACs will also operate to specification with a load of 5 kΩ and 100 pF to V_{BIAS}.

[2]Temperature range: 0°C to +70°C.

[3]1 LSB = $(2*V_{SWING})/2^N$, where N is the DAC resolution. 1 LSB = 2.44 mV for DAC A with V_{SWING} = 2.5 V; 1 LSB = 19.5 mV for DAC B, DAC C with V_{SWING} = 2.5 V.

[4]See Terminology.

[5]The maximum V_{BIAS} voltage is limited by the requirement $V_{BIAS} + V_{SWING} \leq V_{DD} - 2$ V.

[6]The source impedance of the internally generated V_{SWING} is nominally 10 kΩ. If this internally generated V_{SWING} is required for use external to the AD7774, it is recommended that the V_{SWING} output is buffered.

[7]DAC output span cannot be adjusted externally, i.e., adjusting V_{SWING} does not change the DAC output span.

[8]Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

8

TIMING CHARACTERISTICS[1] (See Figures 2, 3, 4.)
(V_{DD} = +10 V to +13.2 V, V_{CC} = +5 V ± 5%, AGND = DGND = 0 V.)

Parameter	Limit at T_{min}, T_{max}	Units	Conditions/Comments
t_1[2]	10/65	ns min/ns max	Data Access Time after $\overline{CS}$
t_2[2]	10/65	ns min/ns max	Data Access Time after $\overline{RD}$
t_3[3]	5/45	ns min/ns max	Bus Relinquish Time after $\overline{CS}$
t_4[3]	5/45	ns min/ns max	Bus Relinquish Time after $\overline{RD}$
t_5	10/75	ns min/ns max	Data Access Time after Address Valid; C_L = 50 pF
t_6	58	ns min	$\overline{WR}$ Pulse Width, t_{11} = 58 ns, t_{12} = 18 ns
	128	ns min	$\overline{WR}$ Pulse Width, t_{11} = 128 ns, t_{12} = 0 ns
t_7	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_8	0	ns min	Address Valid to $\overline{WR}$ Setup Time
t_9	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_{10}	0	ns min	Address Valid to $\overline{WR}$ Hold Time
t_{11}	58	ns min	Data Setup Time Prior to $\overline{WR}$ Rising Edge, t_6 = 58 ns, t_{12} = 18 ns
	128	ns min	Data Setup Time Prior to $\overline{WR}$ Rising Edge, t_6 = 128 ns, t_{12} = 0 ns
t_{12}	18	ns min	Data Hold Time after $\overline{WR}$ Rising Edge, $t_6 = t_{11}$ = 58 ns
	0	ns min	Data Hold Time after $\overline{WR}$ Rising Edge, $t_6 = t_{11}$ = 128 ns
t_{13}			ADC Conversion Time; Rising Edge of $\overline{WR}$ to Rising Edge of $\overline{BUSY}$
	3.6	µs max	DB4 of ADC Control Register = 1; C_L = 20 pF
	3.7	µs max	DB4 of ADC Control Register = 1; C_L = 100 pF
	6	µs max	DB4 of ADC Control Register = 0; C_L = 20 pF
	6.1	µs max	DB4 of ADC Control Register = 0; C_L = 100 pF
t_{14}	100	ns max	Rising Edge of $\overline{WR}$ to Falling Edge of $\overline{BUSY}$; C_L = 20 pF
	150	ns max	Rising Edge of $\overline{WR}$ to Falling Edge of $\overline{BUSY}$; C_L = 100 pF
t_{15}	10	ns min	Address Valid to $\overline{CS}$ or $\overline{RD}$ Setup Time
t_{SAMP}	±50	ns max	ADC Channel to Channel Sampling Skew

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]t_1 and t_2 are measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2,4 V.
[3]t_3 and t_4 are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the times, t_3 and t_4, quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitance.

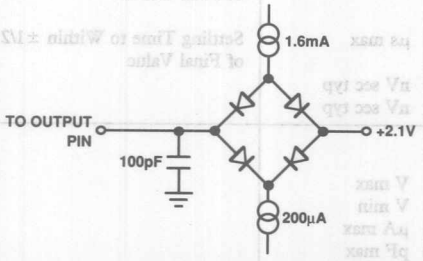


Figure 1. Load Circuits for Timing Measurements

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Package Option*
AD7774KN	0°C to +70°C	±1 LSB	N-28
AD7774KP	0°C to +70°C	±1 LSB	P-28A

*N = Plastic DIP Pacakge; P = Plastic Leaded Chip Carrier (PLCC) Package. For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS*

T_A = +25°C unless otherwise noted

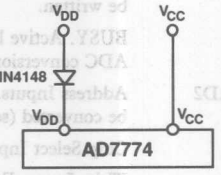
V_{DD} to AGND or DGND . . . . . −0.3 V, +15 V
V_{CC} to DGND . . . . . −0.3 V, V_{DD} + 0.3 V or +7 V (whichever is lower)
AGND to DGND . . . . . −0.3 V, V_{CC} + 0.3 V
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, AD0–AD2 to DGND . . . −0.3 V, V_{DD} + 0.3 V
DB0–DB7, $\overline{BUSY}$ to DGND . . . . . −0.3 V, V_{CC} + 0.3 V
Analog Input Voltage to AGND . . . . . −0.3 V, V_{DD} + 0.3 V
Analog Output Voltage to AGND . . . . −0.3 V, V_{DD} + 0.3 V
Operating Temperature Range
Commercial (K Version) . . . . . 0°C to +70°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 6 mW/°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

Note:
During power supply sequencing some of the absolute maximum rating specifications may be violated. The following specifications are allowed during power-up (for 5 seconds) without causing permanent damage to the device:

1) Digital Input Current, 100 mA.
2) V_{CC} to V_{DD} Current, 3A.

If the V_{CC} supply can provide more than 3A to V_{DD} during power supply sequencing or if V_{CC} can exceed V_{DD} by more than 0.3 V at any other time, the diode protection scheme shown below is recommended;



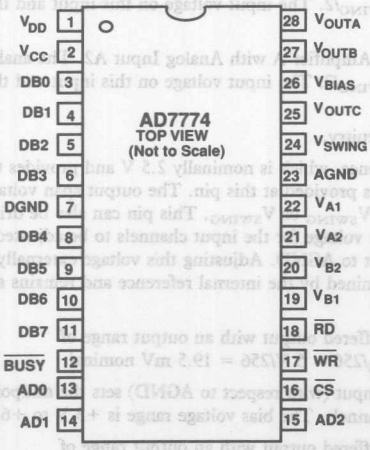
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

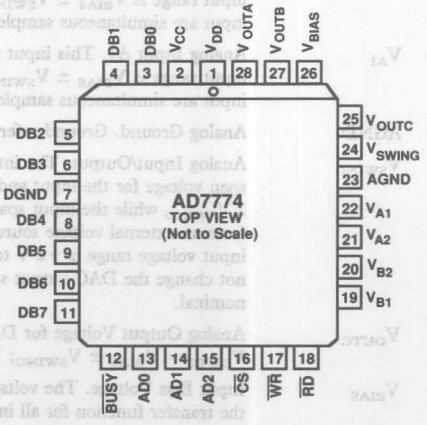


PIN CONFIGURATIONS

DIP



PLCC



8

Pin	Mnemonic	Description
1	V_{DD}	Analog Supply Voltage, +12 V nominal. This is used to power all analog circuitry on the part.
2	V_{CC}	Digital Supply Voltage, +5 V nominal. This is used to power all digital circuitry on the part.
3–6	DB0–DB3	Data Bit 0 to Data Bit 3 of the Input/Output Data Bus. This is a bidirectional data port from which ADC output data may be read and to which DAC input data and ADC Control Register data may be written.
7	DGND	Digital Ground. Ground reference for digital circuitry.
8–11	DB4–DB7	Data Bit 4 to Data Bit 7 of the Input/Output Data Bus. This is a bidirectional data port from which ADC output data may be read and to which DAC input data and ADC Control Register data may be written.
12	$\overline{BUSY}$	BUSY. Active low logic output indicating A/D converter status. The AD7774 is performing an ADC conversion if this output is low.
13–15	AD0–AD2	Address Inputs. These select the internal latches and registers and also the analog input channel to be converted (see TIMING AND CONTROL section).
16	$\overline{CS}$	Chip Select Input. The device is selected when this input is active.
17	$\overline{WR}$	Write Input. Edge-triggered logic input. It is used in conjunction with $\overline{CS}$ and AD0–AD2 to write data to the DAC registers and the ADC Control Register. Data is written to the registers on the rising edge of this $\overline{WR}$ input. The 11 bits of data for DAC A are written from the 8-bit data bus in two write operations. The rising edge of $\overline{WR}$ also starts conversion when AD0–AD2 are set to appropriate values (see ADC Control Register section).
18	$\overline{RD}$	Read Input. Active low logic input. It is used in conjunction with $\overline{CS}$ to enable the data outputs from the ADC latches.
19	V_{B1}	Analog Input B1. This input shares Track/Hold Amplifier B with Analog Input B2. The analog input range is $V_{BIAS} \pm V_{SWING}$ or $V_{BIAS} \pm V_{SWING}/2$. The input voltage on this input and the V_{A1} input are simultaneously sampled.
20	V_{B2}	Analog Input B2. This input shares Track/Hold Amplifier B with Analog Input B1. The analog input range is $V_{BIAS} \pm V_{SWING}$ or $V_{BIAS} \pm V_{SWING}/2$. The input voltage on this input and the V_{A2} input are simultaneously sampled.
21	V_{A2}	Analog Input A2. This input shares Track/Hold Amplifier A with Analog Input A1. The analog input range is $V_{BIAS} \pm V_{SWING}$ or $V_{BIAS} \pm V_{SWING}/2$. The input voltage on this input and the V_{B2} input are simultaneous sampled.
22	V_{A1}	Analog Input A1. This input shares Track/Hold Amplifier A with Analog Input A2. The analog input range is $V_{BIAS} \pm V_{SWING}$ or $V_{BIAS} \pm V_{SWING}/2$. The input voltage on this input and the V_{B1} input are simultaneous sampled.
23	AGND	Analog Ground. Ground reference for analog circuitry.
24	V_{SWING}	Analog Input/Output. The internal voltage reference, which is nominally 2.5 V and provides the span voltage for the input and output channels, is provided at this pin. The output span voltage is 2 V_{SWING} while the input span voltage can be 2 V_{SWING} or V_{SWING}. This pin can also be driven from an external voltage source to allow the span voltage for the input channels to be adjusted. The input voltage range is +2 V to +3 V with respect to AGND. Adjusting this voltage externally does not change the DAC output span which is determined by the internal reference and remains at 5 V nominal.
25	V_{OUTC}	Analog Output Voltage for DAC C. Eight-bit buffered output with an output range of $V_{OUTC} = V_{BIAS} \pm V_{SWING}$; 1 LSB = 2 $V_{SWING}/256$ = 5 V/256 = 19.5 mV nominal.
26	V_{BIAS}	Input Bias Voltage. The voltage applied to this input (with respect to AGND) sets the midpoint of the transfer function for all input and output channels. The bias voltage range is +3 V to +6.8 V.
27	V_{OUTB}	Analog Output Voltage for DAC B. Eight-bit buffered output with an output range of $V_{OUTB} = V_{BIAS} \pm V_{SWING}$; 1 LSB = 2 $V_{SWING}/256$ = 5 V/256 = 19.5 mV nominal.
28	V_{OUTA}	Analog Output Voltage for DAC A. Eleven-bit buffered output with an output range of $V_{OUTA} = V_{BIAS} \pm V_{SWING}$; 1 LSB = 2 $V_{SWING}/2048$ = 5 V/2048 = 2.44 mV nominal.

Relative Accuracy
For the AD7774 ADC, Relative Accuracy or endpoint nonlinearity is the maximum deviation, in LSBs, of the ADC's actual code transition points from a straight line drawn between the endpoints of the ADC transfer function.

For the DACs, Relative Accuracy or endpoint nonlinearity is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity
Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max ensures monotonicity (DAC) or no missed codes (ADC).

Bias Offset Error
For an ideal 8-bit ADC, the output code for an input voltage equal to V_{BIAS} should be 00 Hex. The ADC Bias Offset Error is the difference between the actual midpoint voltage for code 00 Hex and the input bias voltage, expressed in LSBs.

For an ideal DAC, the output voltage for code 000 Hex (DAC A) or code 00 Hex (DAC B, DAC C) should be equal to V_{BIAS}. The DAC Bias Offset Error is the difference between the actual output voltage and V_{BIAS}, expressed in LSBs.

Relative Offset Error
Relative Offset Error is the difference between the result of an internal bias conversion and the result of a conversion carried out with each of the analog inputs connected to V_{BIAS}.

Full-Scale Error (DAC)
The DACs in the AD7774 can be considered as having a bipolar (positive and negative) output range, but referred to the input bias voltage instead of AGND. Positive Full-Scale Error for the DACs is the difference, expressed in LSBs, between the actual output voltage for input code 3FF Hex (for DAC A) or 7F Hex (DAC B, DAC C) and the ideal voltage ($V_{BIAS} + V_{SWING} - 1$ LSB). Negative Full-Scale Error for the DAC is similarly specified for code 400 (DAC A) or code 80 (DAC B, DAC C), relative to the ideal output voltage ($V_{SWING} - V_{BIAS}$). Note that the full-scale errors for the DACs are measured after the bias offset errors have been adjusted out.

The input channels of the ADC can also be considered as having bipolar (positive and negative) input ranges, but referred to the input bias voltage instead of AGND. Positive Full-Scale Error for the ADC is the difference between the actual input voltage at the 7E to 7F code transition and the ideal input voltage ($V_{BIAS} + V_{SWING} - 1.5$ LSB), expressed in LSBs. Negative Full-Scale Error is similarly specified for the 81 to 80 code transition, relative to the ideal input voltage for this transition ($V_{BIAS} - V_{SWING} + 0.5$ LSB). Note that the full-scale errors for the ADC input channels are measured after their respective Bias Offset errors have been adjusted out.

Digital-to-Analog Glitch Impulse
Digital-to-Analog Glitch Impulse is the impulse injected into the analog output when the digital inputs change state with the DAC selected. It is normally specified as the area of the glitch in nV secs and is measured when the digital input code is changed from all 1s to all 0s.

Digital Feedthrough
Digital Feedthrough is also a measure of the impulse injected into the analog outputs from the digital inputs but is measured when the DAC is not selected. It is essentially feedthrough across the die and package. It is important in the AD7774 since it is a measure of the glitch impulse transferred to the analog output when data is read from the ADC latches. It is specified in nV secs and is measured with $\overline{WR}$ high and a digital code change from all 0s to all 1s.

TIMING AND CONTROL

The AD7774 contains two ADC data latches, an ADC control register and three DAC registers. Each of the ADC data latches contains a conversion result from the held voltage on its respective track/hold, i.e., ADC Latch A contains the result of a conversion performed on the held voltage on Track/Hold A, while ADC Latch B contains the results of a conversion done on the held voltage on Track/Hold B. The ADC control register determines whether a single or double conversion takes place and also determines the conversion sequence . In addition, it controls the analog input range for each channel.

Reading from the AD7774 accesses the contents of the ADC data latches. The $\overline{RD}$ input is a level-triggered input. Writing to the device either initiates conversion on the channel(s) determined by the ADC control register or loads data to the DAC registers. The $\overline{WR}$ input is an edge-triggered input. The following sections describe read, write and control register operations for the AD7774.

Read Operation

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	AD2	AD1	AD0	Function
1	X	X	X	X	X	No Read Operation.
X	1	X	X	X	X	No Read Operation.
0	0	X	X	X	0	The contents of ADC Latch A are output to the databus. This will contain the results of a conversion on either V_{A1} or V_{A2} (see ADC Control Register section).
0	0	X	X	X	1	The contents of ADC Latch B are output to the databus. This will contain the results of a conversion on either V_{B1} or V_{B2} (see ADC Control Register section).

Write Operation

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	AD2	AD1	AD0	Function
1	X	X	X	X	X	No Write Operation.
X	X	1	X	X	X	No Write Operation.
0	1	↓	0	0	0	DB0–DB7 are written to the upper 8 bits of the DAC A Register.
0	1	↓	0	0	1	DB5–DB7 are written to the lower 3 bits of the DAC A Register, and all 11 bits of the DAC A register are loaded to DAC A.
0	1	↓	0	1	0	DB0–DB7 are written into the DAC B Register and are loaded to DAC B.
0	1	↓	0	1	1	DB0–DB7 are written into the DAC C Register and are loaded to DAC C.
0	1	↓	1	0	0	Start conversion on either V_{A1} or V_{B1} or both (DB4 and DB5 of the ADC Control Register determine operation – see ADC Control Register section).
0	1	↓	1	0	1	Start conversion on either V_{A2} or V_{B2} or both (DB4 and DB5 of the ADC Control Register determine operation – see ADC Control Register section).
0	1	↓	1	1	0	Start conversion on either Track/Hold A bias voltage or Track/Hold B bias voltage or both (DB4 and DB5 of the ADC Control Register determine operation—see ADC Control Register section). See Bias Conversions section for explanation.
0	1	↓	1	1	1	DB0–DB5 is written to the ADC Control Register.

X = Don't Care.
A read during an ADC conversion may corrupt the data from the conversion in progress.

ADC Control Register

The ADC Control Register determines whether a single or double conversion takes place and also which track/hold output is converted when a write operation to start conversion takes place. The single/double conversion is determined by DB4 (see below). A double conversion means that both track/holds go into hold mode simultaneously, and the ADC converts both held voltages in sequence. The ADC status line, $\overline{BUSY}$, does not indicate that the conversion sequence has ended until both conversions are complete. In the single conversion mode, both track/holds again are simultaneously held but only one of these "held" voltages is converted—the other is ignored. The ADC status line, $\overline{BUSY}$, indicates that the conversion sequence has ended after one track/hold voltage has been converted. DB5 determines which track/hold voltage is converted in the single conversion mode. The ADC Control Register also determines the analog input voltage range for all four inputs (see DB0–DB3 below).

ADC Control Register Bit	Function
DB0	V_{A1} Input Voltage Range
0	Input Range is $V_{BIAS} \pm V_{SWING}$
1	Input Range is $V_{BIAS} \pm V_{SWING}/2$
DB1	V_{A2} Input Voltage Range
0	Input Range is $V_{BIAS} \pm V_{SWING}$
1	Input Range is $V_{BIAS} \pm V_{SWING}/2$
DB2	V_{B1} Input Voltage Range
0	Input Range is $V_{BIAS} \pm V_{SWING}$
1	Input Range is $V_{BIAS} \pm V_{SWING}/2$
DB3	V_{B2} Input Voltage Range
0	Input Range is $V_{BIAS} \pm V_{SWING}$
1	Input Range is $V_{BIAS} \pm V_{SWING}/2$
DB4	Single/Double Conversion
0	Double Conversion
1	Single Conversion
DB5	Conversion Sequence
0	First Conversion in the sequence is a V_A conversion[1, 2]
1	First Conversion in the sequence is a V_B conversion[1, 2]

NOTES

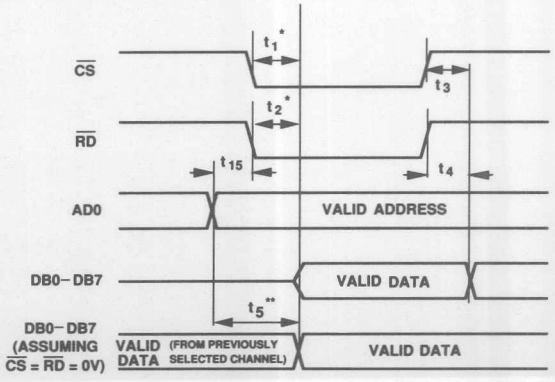
[1]A V_A conversion is a conversion on either V_{A1}, V_{A2}, or the bias voltage for Track/Hold A. Address inputs AD0, AD1 and AD2 determine which one of these signals is converted. A V_B conversion is a conversion on either V_{B1}, V_{B2}, or the bias voltage for Track/Hold B. Address inputs AD0, AD1 and AD2 determine which one of these signals is converted. (See previous page.)

[2]In the single conversion mode DB5 determines whether a V_A conversion or a V_B conversion takes place. In the double conversion mode, DB5 simply determines the order in which the two track/hold voltages are converted.

ADC Read Cycle

Figure 2 shows the timing diagram for a read operation for the AD7774. It consists of bringing both $\overline{CS}$ and $\overline{RD}$ low with data being accessed from one of the two on-chip ADC latches. Address line AD0 determines from which latch the data is accessed. With AD0 low, the contents of ADC Latch A are placed on the databus during a read operation; with AD0 high, a read operation will access the contents of ADC Latch B. ADC Latch A will contain the results of a conversion on either V_{A1} or V_{A2} or the results of a conversion on the bias voltage for Track/Hold A. ADC Latch B will contain the results of a conversion on V_{B1} or V_{B2} or the results of a conversion on the bias voltage for Track/Hold B.

Both the $\overline{CS}$ and $\overline{RD}$ inputs are level-triggered. If both are hardwired low, the data access time for a read cycle is determined from AD0.



* t_1 and t_2 are measured with t_{15} = 10ns

** t_5 is measured with $\overline{CS}$ = $\overline{RD}$ = 0V

Figure 2. AD7774 Read Cycle

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A write operation to the AD7774 consists of writing data to the DAC registers or to the ADC Control Register. A write to the AD7774 can also initiate conversion on the ADC (see ADC Conversion Sequence section). The function of the write operation is determined by address bits AD0–AD2.

The $\overline{WR}$ input is an edge-triggered input, and data is only written to the on-chip registers on the rising edge of $\overline{WR}$. Data written to the DAC registers must be left justified to load correct data. For the 11-bit DAC A, this means that the upper 8 bits are loaded with the 11-bit MSB occupying the DB7 position on the databus. The lower three bits of the 11-bit word are loaded in a separate write cycle with DB0 of the 11-bit word occupying the DB5 position on the databus. Figure 3 shows the timing diagram for a write operation to the AD7774.

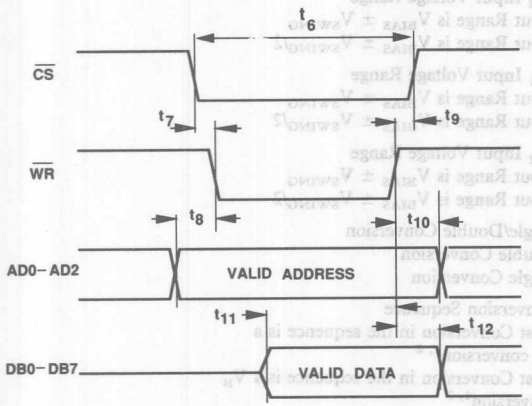


Figure 3. AD7774 Write Cycle

The AD7774 contains two track/hold amplifiers and one A/D converter. A conversion sequence can either consist of a single conversion or double conversion. In the double conversion mode, the track/holds go into hold mode simultaneously, and the held voltages are converted sequentially by the A/D converter. In the single conversion option, the track/holds again go into hold mode simultaneously, but only one voltage is converted—either the held voltage on Track/Hold A or Track/Hold B.

Figure 4 shows the timing diagram for the AD7774 conversion sequence. Conversion is initiated on the rising edge of $\overline{WR}$. Address lines AD0–AD2 determine which channel is to be converted. On the rising edge of $\overline{WR}$, the internal clock oscillator is activated, and the channel acquisition time begins. The $\overline{BUSY}$ output goes low to indicate that the conversion sequence has begun. The channel acquisition time takes approximately 1.5 μs, at which time the track/holds go into hold mode. The A/D converter then converts the held voltage on either Track/Hold A or Track/Hold B depending on the status of DB5 of the control register.

This first conversion takes a total of 3.6 μs maximum. In the single conversion mode, the conversion sequence is now complete, and the AD7774 indicates this by taking its $\overline{BUSY}$ status line high. In the double conversion mode, the conversion on the voltage held on the second track/hold starts at this time and runs for another 2.4 μs maximum. In this double conversion mode, the $\overline{BUSY}$ line does not return high until the second conversion is complete. At the end of conversion, either single or double, the internal clock oscillator is shut down.

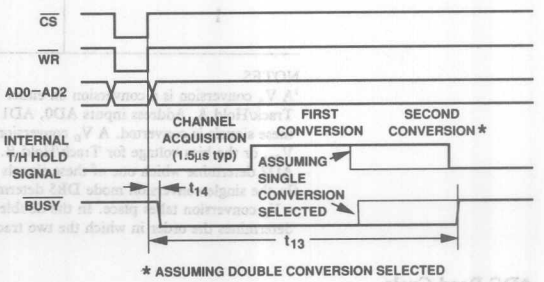


Figure 4. AD7774 Conversion Cycle

CIRCUIT DESCRIPTION

Analog Inputs and Outputs

The AD7774 provides the analog-to-digital and digital-to-analog conversion functions required between the microcontroller and the servo power amplifier in digital servo systems. It is intended primarily for closed-loop head positioning in dedicated-only and combined dedicated/embedded disk drives or other closed-loop digital servo applications. The ability to refer input and output signals to some voltage other than ground is of particular importance in disk drive applications. Typically, only +5 V digital and +12 V analog supply voltages are available, and the analog signals are often referred to a voltage around half the analog supply.

The AD7774 contains two track/hold amplifiers which feed a high speed, 8-bit, sampling ADC, each track/hold having two input channels. The part also contains three DACs with output amplifiers—one 11-bit DAC and two 8-bit DACs. A unique feature of the AD7774 is the input and output signal conditioning circuitry, which allows the analog input and output voltages to be referred to a point other than analog ground. The offset of the input channels and output channels is achieved by applying a ground-referenced, positive control voltage to the V_{BIAS} input of the AD7774. The voltage span of the input channels is set by applying a ground-referenced, positive control voltage to the V_{SWING} input of the part. The output voltage span from the DACs is set by the internal reference voltage.

Figure 5 shows the input voltage to output code relationship for the four input channels. The midpoint code of the input channels, 00 Hex (0000 0000 Binary), occurs at an input voltage equal to V_{BIAS}. Output coding from the ADC is 2s complement biased around this V_{BIAS} voltage.

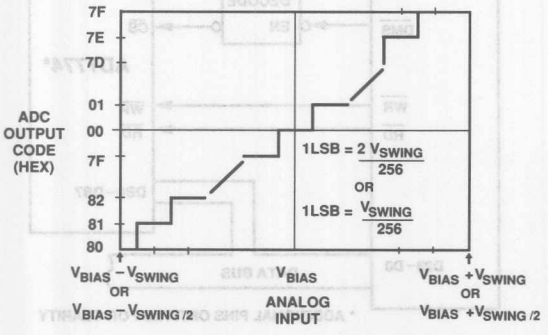


Figure 5. ADC Transfer Function

The input voltage range for the channels depends upon the status of bits DB0 to DB3 of the ADC control register. Each these bits controls the gain on one of the input channels (see ADC Control Register section). The input gain on each one of the input channels can either be a gain of 1 or a gain of 1/2. This results in an input voltage range which can be either $V_{BIAS} \pm V_{SWING}$ or $V_{BIAS} \pm V_{SWING}/2$.

For the first case, the full scale range (FSR) is 2 V_{SWING} and 1 LSB = 2 V_{SWING}/256. With the nominal V_{SWING} of +2.5 V, 1 LSB = 5 V/256 = 19.5 mV. The ideal first code transition (80 to 81 Hex) occurs at an analog input voltage equal to $V_{BIAS} - V_{SWING}$ + 0.5 LSB (negative full scale) and the ideal last code transition (7E to 7F Hex) occurs at an input voltage equal to $V_{BIAS} + V_{SWING}$ −1.5 LSBs (positive full scale).

For the second case, the full scale range (FSR) is V_{SWING} and 1 LSB = V_{SWING}/256. With the nominal V_{SWING} of +2.5 V, 1 LSB = 2.5 V/256 = 9.76 mV. The ideal first code transition (80 to 81 Hex) occurs at an analog input voltage equal to $V_{BIAS} - V_{SWING}/2$ + 0.5 LSB (negative full scale) and the ideal last code transition (7E to 7F Hex) occurs at an input voltage equal to $V_{BIAS} + V_{SWING}/2$ − 1.5 LSBs (positive full scale).

The input code to output voltage relationship for DAC A is shown in Figure 6. The DAC output voltage for an input code of 000 Hex is ideally equal to V_{BIAS}. Input coding to the DAC is 2s complement with the output voltage range biased around this V_{BIAS} voltage. The output voltage range is $V_{BIAS} \pm V_{SWING}$.

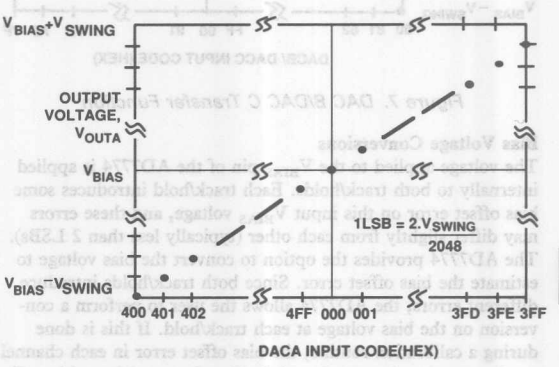


Figure 6. Transfer Function

The output range is 2 V_{SWING} where V_{SWING} is set by the internal reference voltage. The nominal DAC output swing is, therefore, 5 V and 1 LSB = 5 V/2048 = 2.44 mV. The bottom end of the transfer function occurs at an input code of 400 Hex and is ideally equal to $V_{BIAS} - V_{SWING}$. The top end of the transfer function occurs at an input code of 3FF Hex and is ideally equal to $V_{BIAS} + V_{SWING}$ −1 LSB.

The transfer function for both DAC B and DAC C is very similar to that outlined for DAC A. Once again, the output voltage range is $V_{BIAS} \pm V_{SWING}$. The V_{SWING} voltage is again set by the internal reference voltage. Therefore, the nominal output swing is 5 V and 1 LSB = 5 V/256 = 19.5 mV.

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The DAC output voltage for an input code of 00 Hex is ideally equal to V_{BIAS}. Input coding to the DACs is 2s complement with the output voltage range biased around this V_{BIAS} voltage. The bottom end of the transfer function (negative full scale) occurs at an input code of 80 Hex and is ideally equal to $V_{BIAS} - V_{SWING}$. The top end of the transfer function (positive full scale) occurs at an input code of 7F Hex and is ideally equal to $V_{BIAS} + V_{SWING} - 1$ LSB. The input code to output voltage relationship for both DAC B and DAC C is shown in Figure 7.

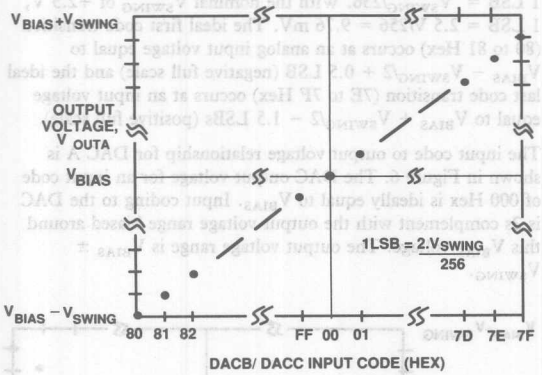


Figure 7. DAC B/DAC C Transfer Function

Bias Voltage Conversions

The voltage applied to the V_{BIAS} pin of the AD7774 is applied internally to both track/holds. Each track/hold introduces some bias offset error on this input V_{BIAS} voltage, and these errors may differ slightly from each other (typically less than 2 LSBs). The AD7774 provides the option to convert the bias voltage to estimate the bias offset error. Since both track/holds introduce different errors, the AD7774 allows the user to perform a conversion on the bias voltage at each track/hold. If this is done during a calibration routine, the bias offset error in each channel can be stored and compensated for in software. After a bias offset conversion for Track/Hold A, the results are stored in ADC Latch A and for a bias offset conversion for Track/Hold B, the results are stored in ADC Latch B.

Driving the Analog Inputs and Reference Inputs

The analog inputs, V_{A1}, V_{A2}, V_{B1} and V_{B2} require up to 1 mA of input current and as such must be driven from low output impedance sources. In addition, the V_{BIAS} and V_{SWING} inputs must also be driven from low impedance sources. The V_{SWING} pin provides the internally generated swing voltage, but this can be overdriven by an externally applied voltage. This externally applied voltage will generate the V_{SWING} voltage for the ADC but the V_{SWING} for the DACs is always generated from the internal swing voltage.

MICROPROCESSOR/MICROCOMPUTER INTERFACING

The AD7774 is designed for easy interfacing to microprocessors and microcomputers as a memory mapped peripheral or an I/O device. In addition, the AD7774 high speed bus timing allows direct interfacing to most microprocessors including the DSP processors.

AD7774–ADSP-2101/ADSP-2105 Interface

Figure 8 shows a typical interface to the DSP microcomputer, the ADSP-2101/ADSP-2105. The ADSP-2101/ADSP-2105 is optimized for high speed numeric processing tasks.

Because the instruction cycle of the ADSP-2101/ADSP-2105 is very fast, the $\overline{WR}$ and $\overline{RD}$ pulses must be stretched out to suit the AD7774. This is easily achieved as the ADSP-2101/ADSP-2105 memory interface supports slower memories and memory-mapped peripherals with a programmable wait state generation capability. A number of wait states, from 0 to 7, can be specified for each memory interface. One wait state is sufficient for the interface to the AD7774.

Conversion is initiated on the required ADC channel using a <DM(CST) = MR0> where CST is the relevant channel address. Writing data to the relevant AD7774 DAC or to the AD7774 ADC control register consists of a <DM(DAC) = MR0> instruction where DAC is the relevant DAC address or the address of the ADC control register. Two write operations are required to load the 11 bits of data to DAC A. A conversion result is read using the instruction <MR0 = DM(ADC)> where ADC is the address of the relevant ADC Latch.

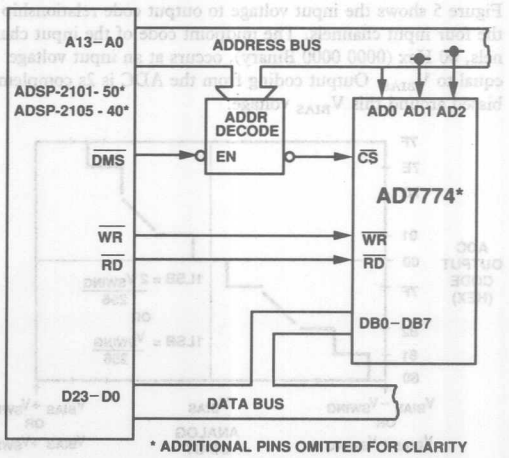


Figure 8. AD7774 to ADSP-2101/ADSP-2105 Interface

AD7774—TMS320C10/TMS320C14 Interface

A typical interface to the TMS320C10/TMS320C14 is shown in Figure 9. The AD7774 is mapped at a port address, and the interface is designed for the maximum TMS320C10 clock frequency of 20 MHz and the maximum clock frequency of 25 MHz for the TMS320C14.

Conversion is initiated on the selected AD7774 ADC channel using a single I/O instruction, <OUT CST,A> where CST is the relevant address for the selected channel. Writing data to the relevant AD7774 DAC or to the AD7774 ADC control register consists of an <OUT DAC,A> instruction where DAC is the relevant DAC address or the address of the ADC control regis-

ter. Two write operations are required to load the 11 bits of data to DAC A. A conversion result is read using the instruction <IN A,ADC> where ADC is the address of the relevant ADC Latch.

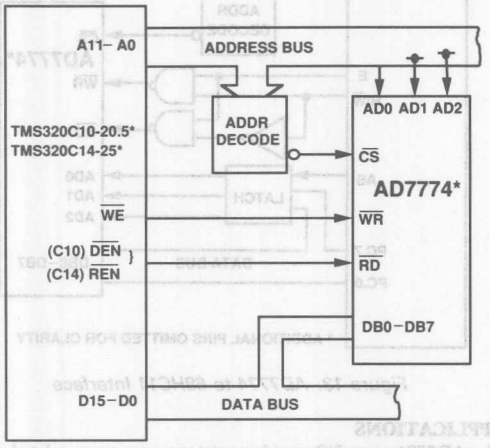


Figure 9. AD7774 to TMS320C10/TMS320C14 Interface

AD7774–TMS320C25 Interface

Figure 10 shows an interface between the TMS320C25 and the AD7774. The TMS320C25 does not have separate RD and WR signals to drive the AD7774 RD and WR inputs directly. These have to be generated from the processor STRB and R/W outputs with the addition of some logic gates.

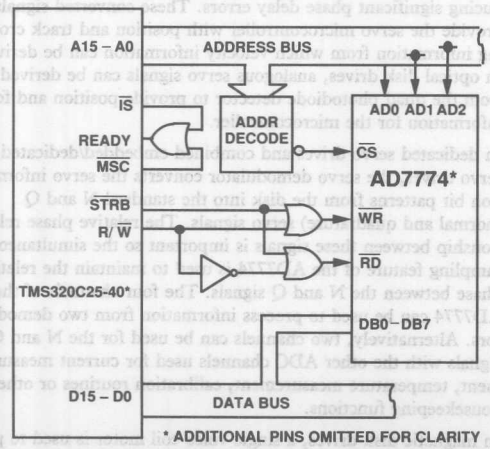


Figure 10. AD7774 to TMS320C25 Interface

Once again, because the processor cycle time is so fast a wait state has to be inserted during read and write cycles to the AD7774. This is achieved by OR-gating the IS signal with the MSC signal to drive the READY input and, thereby, generate one wait state during every read and write operation to the AD7774.

Conversion is initiated on the selected AD7774 ADC channel using a single I/O instruction, <OUT CST,A> where CST is the relevant address for the selected channel. Writing data to the relevant AD7774 DAC or to the AD7774 ADC control register consists of an <OUT DAC,A> instruction where DAC is the relevant DAC address or the address of the ADC control register. Two write operations are required to load the 11 bits of data to DAC A. A conversion result is read using the instruction < IN A,ADC > where ADC is the address of the relevant ADC Latch.

AD7774–80C196 Interface

Figure 11 shows a typical interface between the AD7774 and the 80C196 microcomputer. The microcomputer is configured in its 8-bit bus cycle mode and in the address valid strobe mode. In this mode, the high order 8 bits of the address bus appear on Port 4, while Port 3 contains the multiplexed data bus and lower order address bus.

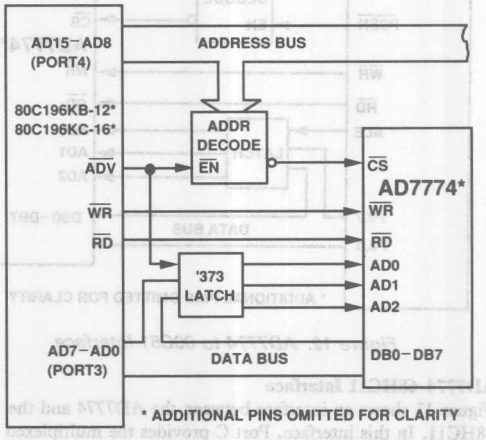


Figure 11. AD7774 to 80C196 Interface

Conversion is initiated on the selected AD7774 ADC channel using a single I/O instruction, <STB CST,D> where CST is the relevant address for the selected channel and D is a location in the 80C196 register file or is immediate data. Writing data to the relevant AD7774 DAC or to the AD7774 ADC control register consists of an <STB DAC,D> instruction where DAC is the relevant DAC address or the address of the ADC control register and D is a location in the 80C196 register file or is immediate data. Two write operations are required to load the 11 bits of data to DAC A. A conversion result is read using the instruction <LDB D,ADC> where ADC is the address of the relevant ADC latch and D is a location in the 80C196 register file.

8

AD7774–80C51 Interface

A typical interface between the AD7774 and the 80C51 is shown in Figure 12. In this interface, Port 0 provides the multiplexed low order address and data bus, and Port 2 provides the high order address bus. The ALE signal from the 80C51 is used to demultiplex the address/data bus.

Conversion is initiated on the selected AD7774 ADC channel using a single instruction, <MOV CST,A> where CST is the relevant address for the selected channel and A is the 80C51 accumulator. Writing data to the relevant AD7774 DAC or to the AD7774 ADC control register consists of an <MOV DAC,A> instruction where DAC is the relevant DAC address or the address of the ADC control register, and A is the 80C51 accumulator. Two write operations are required to load the 11 bits of data to DAC A. A conversion result is read using the instruction <MOV A,ADC> where ADC is the address of the relevant ADC Latch and A is the 80C51 accumulator.

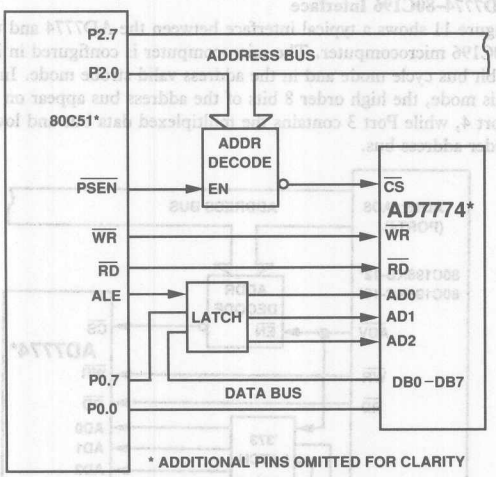


Figure 12. AD7774 to 80C51 Interface

AD7774–68HC11 Interface

Figure 13 shows an interface between the AD7774 and the 68HC11. In this interface, Port C provides the multiplexed low order address and data bus, and Port B provides the high order address bus. The AS signal from the 68HC11 is used to demultiplex the address/data bus. The 68HC11 does not have separate $\overline{RD}$ and $\overline{WR}$ signals to drive the AD7774 $\overline{RD}$ and $\overline{WR}$ inputs directly. These have to be generated from the processor E and R/$\overline{W}$ outputs with the addition of some logic gates.

Conversion is initiated on the selected AD7774 ADC channel using a single instruction, <STAA CST> where CST is the relevant address for the selected channel. Writing data to the relevant AD7774 DAC or to the AD7774 ADC control register consists of an <STAA DAC> instruction where DAC is the relevant DAC address or the address of the ADC control register, and the data is loaded to the relevant register from the 68HC11 accumulator. Two write operations are required to load the 11 bits of data to DAC A. A conversion result is read using the instruction <LDAA ADC> where ADC is the address of the relevant ADC latch, and the conversion result is loaded to the 68HC11 accumulator.

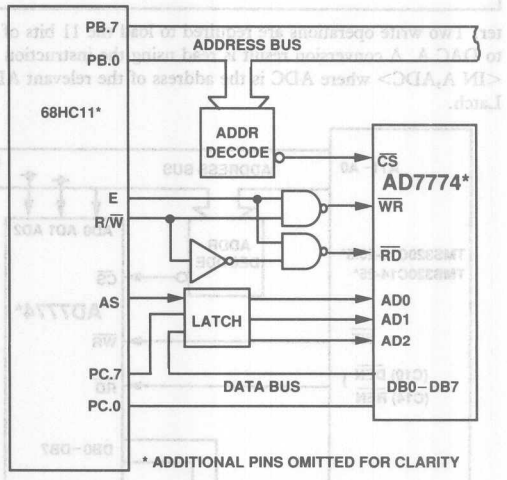


Figure 13. AD7774 to 68HC11 Interface

APPLICATIONS

The AD7774 servo I/O port is used to convert servo-related signals between the analog and digital domains. The input structure of the ADC makes it very easy to convert the typical output signals provided by a servo demodulator.

In a magnetic disk drive employing a dedicated servo surface or a combined embedded/dedicated servo surface, the servo demodulator produces two, positive-only, quadrature signals, generally sinusoidal or triangular, from the di-bit patterns read from the servo surface. The quadrature signals have the form of $V_{BIAS} \pm V_{SWING}$. The simultaneous sampling of the AD7774 input channels allows conversion of these quadrature signals without introducing significant phase delay errors. These converted signals provide the servo microcontroller with position and track crossing information from which velocity information can be derived. In optical disk drives, analogous servo signals can be derived from the quad photodiode detector to provide position and focus information for the microcontroller.

In dedicated servo drives and combined embedded/dedicated servo drives, the servo demodulator converts the servo information bit patterns from the disk into the standard N and Q (normal and quadrature) servo signals. The relative phase relationship between these signals is important so the simultaneous sampling feature of the AD7774 is used to maintain the relative phase between the N and Q signals. The four channels of the AD7774 can be used to process information from two demodulators. Alternatively, two channels can be used for the N and Q signals with the other ADC channels used for current measurement, temperature measurement, calibration routines or other housekeeping functions.

In magnetic disk drives, a single voice coil motor is used to position the head assembly and one DAC is usually sufficient to drive the motor in both the seek and track modes. In the seek mode the DAC can be used to generate directly the desired analog velocity trajectory which the head must travel in order to achieve minimum access times. Alternatively the DAC can generate a servo error value (computed by the microcontroller) between the actual head velocity and the desired head velocity. In

the track mode, the DAC can be used to provide a position error signal to keep the head over the track or to detect the head off-track, for such purposes as thermal compensation and soft-error retries. The DACs provide positive-only output signals of the form $V_{BIAS} \pm V_{SWING}$, which are ideal for driving voice coil motors. In general, up to 11 bits of resolution are required for a DAC to control the motor in both the seek and track modes. As a result, DAC A would generally be used to drive the voice coil motor. The other DAC channels can be used for programmable control of the loop filter or for AGC or programmable gain control.

A typical servo control loop using the AD7774 is shown in Figure 14. In this dedicated servo example, the servo demodulator outputs (the N and Q signals) are applied to the V_{A1} and V_{B1} inputs of the AD7774. The voice coil motor current, I_L, is bidirectional and is supplied by the power transconductance amplifier. One input to this amplifier is held at V_{BIAS} while the other input is driven from the DAC A output, V_{OUTA}. Typical input voltages for this power stage are shown in Figure 15. The transconductance, G_O, of the power stage is determined by external sense resistors.

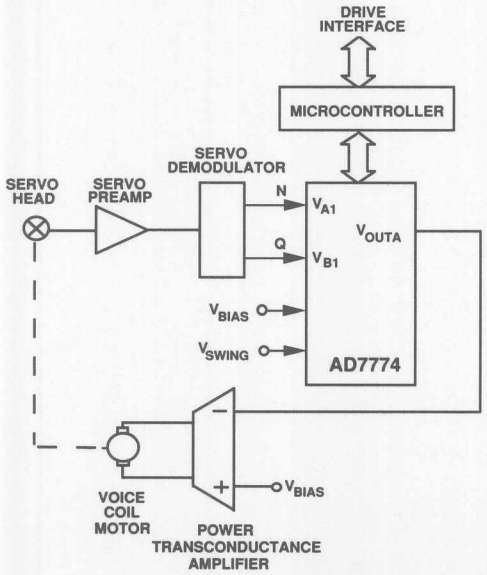


Figure 14. Typical Dedicated Servo Control Loop Using the AD7774

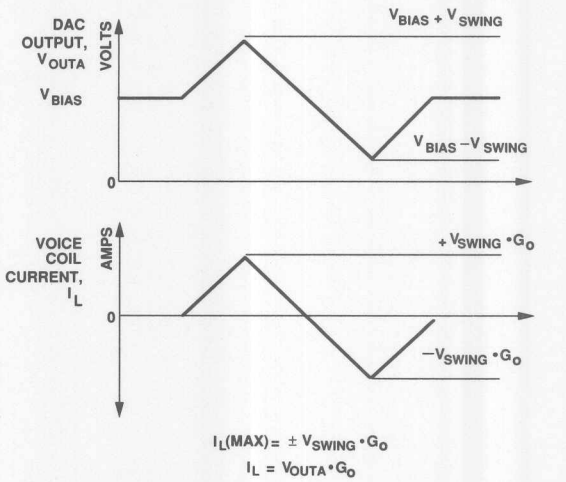


Figure 15. Typical Relationship Between Input Voltage and Output Current for Transconductance Amplifier

Multichannel Expansion

The AD7774 with its four input channels has the capability of monitoring the N and Q signals from two servo demodulators. With the addition of a multiplexer and a dual op amp, the system can be expanded so that the AD7774 handles the outputs from a number of servo demodulators. Using a differential multiplexer as shown in Figure 16, the N and Q signals for each servo demodulator can still be simultaneously sampled. The ADG527A multiplexer is ideally suited since it is specified for single supply operation (12 V ± 10%).

The $\overline{CS}$ and $\overline{WR}$ inputs to the AD7774 are gated to provide the $\overline{WR}$ input to the ADG527A. The multiplexer input is selected on the falling edge of $\overline{WR}$ while the signal is latched on the rising edge. The AD7774 starts conversion also on the rising edge of $\overline{WR}$. Therefore, the output signal of the multiplexer must have settled to within 8 bits over the duration of the $\overline{WR}$ pulse. The t_{ON} ($\overline{WR}$) and settling time of the ADG527A determine the width of the $\overline{WR}$ pulse.

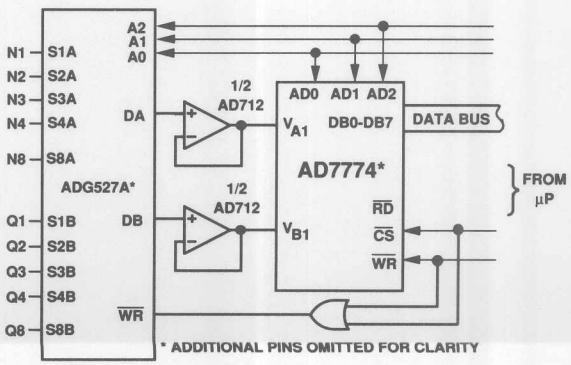
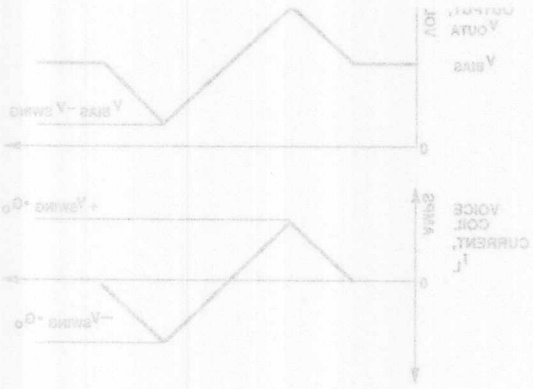
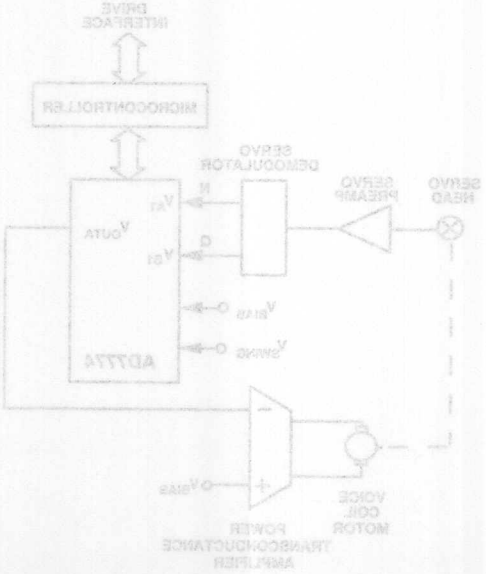
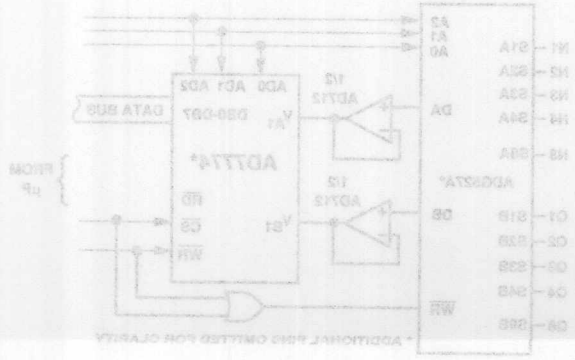


Figure 16. Multichannel System

8




MICROCONTROLLER
SERVO DEMODULATOR
SERVO PREAMP
SERVO HEAD
ADJ774
VOICE COIL MOTOR
POWER TRANSCONDUCTANCE AMPLIFIER


ADJ774*
ADG527A*

Complete, 12-Bit Analog I/O System

AD7868

FEATURES

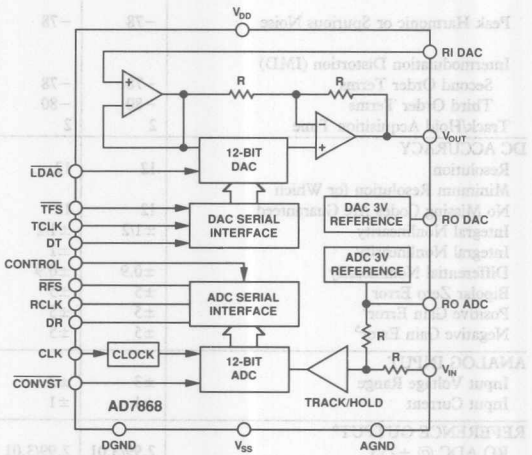
Complete 12-Bit I/O System, Comprising:
- **12-Bit ADC with Track/Hold Amplifier**
  - **83 kHz Throughput Rate**
  - **72 dB SNR**
- **12-Bit DAC with Output Amplifier**
  - **3 μs Settling Time**
  - **72 dB SNR**
- **On-Chip Voltage Reference**

Operates from ±5 V Supplies
Low Power – 130 mW typ
Small 0.3″ Wide DIP

APPLICATIONS

Digital Signal Processing
Speech Recognition and Synthesis
Spectrum Analysis
High Speed Modems
DSP Servo Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7868 is a complete 12-bit I/O system containing a DAC and an ADC. The ADC is a successive approximation type with a track-and-hold amplifier having a combined throughput rate of 83 kHz. The DAC has an output buffer amplifier with a settling time of 3 μs to 12 bits. Temperature compensated 3 V buried Zener references provide precision references for the DAC and ADC.

Interfacing to both the DAC and ADC is serial, minimizing pin count and giving a small 24-pin package size. Standard control signals allow serial interfacing to most DSP machines. Asynchronous ADC conversion control and DAC updating is made possible with the $\overline{\text{CONVST}}$ and $\overline{\text{LDAC}}$ logic inputs.

The AD7868 operates from ±5 V power supplies, the analog input/output range of the ADC/DAC is ±3 V. The part is fully specified for dynamic parameters such as signal-to-noise ratio and harmonic distortion as well as traditional dc specifications.

The part is available in a 24-pin, 0.3″ wide, plastic or hermetic dual-in-line package (DIP) and in a 28-pin, plastic SOIC package.

PRODUCT HIGHLIGHTS

1. Complete 12-Bit I/O System.
   The AD7868 contains a 12-bit ADC with a track-and-hold amplifier and a 12-bit DAC with output amplifier. Also included are separate on-chip voltage references for the DAC and the ADC.
2. Dynamic Specifications for DSP Users.
   In addition to traditional dc specifications, the AD7868 is specified for ac parameters including signal-to-noise ratio and harmonic distortion. These parameters along with important timing parameters are tested on every device.
3. Small Package.
   The AD7868 is available in a 24-pin DIP and a 28-pin SOIC package.

8

AD7868—SPECIFICATIONS

ADC SECTION (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V, f_{CLK} = 2.0 MHz external. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	T Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					
Signal-to-Noise Ratio[3, 4] (SNR) @ +25°C	70	72	70	dB min	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
T_{min} to T_{max}	70	71	70	dB min	Typically 71.5 dB for 0<V_{IN}<41.5 kHz
Total Harmonic Distortion (THD)	−78	−78	−76	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz Typically −84 dB for 0<V_{IN}<41.5 kHz
Peak Harmonic or Spurious Noise	−78	−78	−76	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz Typically −84 dB for 0<V_{IN}<41.5 kHz
Intermodulation Distortion (IMD)					
Second Order Terms	−78	−78	−76	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	−80	−80	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Track/Hold Acquisition Time	2	2	2	µs max	
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for Which					
No Missing Codes Are Guaranteed	12	12	12	Bits	
Integral Nonlinearity	±1/2	±1/2	±1/2	LSB typ	
Integral Nonlinearity		±1	±1	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	LSB max	
Bipolar Zero Error	±5	±5	±5	LSB max	
Positive Gain Error[5]	±5	±5	±5	LSB max	
Negative Gain Error[5]	±5	±5	±5	LSB max	
ANALOG INPUT					
Input Voltage Range	±3	±3	±3	Volts	
Input Current	±1	±1	±1	mA max	
REFERENCE OUTPUT[6]					
RO ADC @ +25°C	2.99/3.01	2.99/3.01	2.99/3.01	V min/V max	
RO ADC TC	±25	±25	±25	ppm/°C typ	
RO ADC TC		±40	±50	ppm/°C max	
Reference Load Sensitivity (ΔRO ADC vs. ΔI)	−1.5	−1.5	−1.5	mV max	Reference Load Current Change (0–500 µA), Reference Load Should Not Be Changed During Conversion
LOGIC INPUTS (CONVST, CLK, CONTROL)					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Current[7] (CONTROL Input Only)	±10	±10	±10	µA max	V_{IN} = V_{SS} to DGND
Input Capacitance, C_{IN}[8]	10	10	10	pF max	
LOGIC OUTPUTS					
DR, $\overline{RFS}$ Outputs					
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA, Pull-Up Resistor = 4.7 kΩ
RCLK Output					
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 2.6 mA, Pull-Up Resistor = 2 kΩ
DR, $\overline{RFS}$, RCLK Outputs					
Floating-State Leakage Current	±10	±10	±10	µA max	
Floating-State Output Capacitance[8]	15	15	15	pF max	
CONVERSION TIME					
External Clock	10	10	10	µs max	
Internal Clock	10	10	10	µs max	The Internal Clock Has a Nominal Value of 2.0 MHz
POWER REQUIREMENTS					For Both DAC and ADC
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	22	22	25	mA max	Cumulative Current from the Two V_{DD} Pins
I_{SS}	12	12	13	mA max	Cumulative Current from the Two V_{SS} Pins
Total Power Dissipation	170	170	190	mW max	Typically 130 mW

NOTES
[1]Temperature ranges are as follows: A/B Versions: −40°C to +85°C; T Version: −55°C to +125°C.
[2]V_{IN} = ±3 V.
[3]SNR calculation includes distortion and noise components.
[4]SNR degradation due to asynchronous DAC updating during conversion is 0.1 dB typ.
[5]Measured with respect to internal reference.
[6]For capacitive loads greater than 50 pF a series resistor is required (see INTERNAL REFERENCE section).
[7]Tying the CONTROL input to V_{DD} places the device in a factory test mode where normal operation is not exhibited.
[8]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

DAC SECTION (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V, RI DAC = +3 V and decoupled as shown in Figure 2, V_{OUT} Load to AGND; R_L = 2 kΩ, C_L = 100 pF. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	T Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					
Signal to Noise Ratio[3] (SNR) @ +25°C	70	72	70	dB min	V_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 83 kHz
T_{min} to T_{max}	70	71	70	dB min	Typically 71.5 dB at +25°C for 0 <V_{OUT}<20 kHz[4]
Total Harmonic Distortion (THD)	−78	−78	−76	dB max	V_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 83 kHz Typically −84 dB at +25°C for 0 <V_{OUT}<20 kHz[4]
Peak Harmonic or Spurious Noise	−78	−78	−76	dB max	V_{OUT} = 1 kHz, f_{SAMPLE} = 83 kHz Typically −84 dB at +25°C for 0 <V_{OUT}<20 kHz[4]
DC ACCURACY					
Resolution	12	12	12	Bits	
Integral Nonlinearity	±1/2	±1/2	±1/2	LSB typ	
Integral Nonlinearity	±1	±1	±1	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic
Bipolar Zero Error	±5	±5	±5	LSB max	
Positive Full-Scale Error[5]	±5	±5	±5	LSB max	
Negative Full-Scale Error[5]	±5	±5	±5	LSB max	
REFERENCE OUTPUT[6]					
RO DAC @ +25°C	2.99/3.01	2.99/3.01	2.99/3.01	V min/V max	
RO DAC TC	±25	±25	±25	ppm/°C typ	
RO DAC TC		±40	±50	ppm/°C max	
Reference Load Change (ΔRO DAC vs. ΔI)	−1.5	−1.5	− 1.5	mV max	Reference Load Current Change (0–500 μA)
REFERENCE INPUT					
RI DAC Input Range	2.85/3.15	2.85/3.15	2.85/3.15	V min/V max	3 V ± 5%
Input Current	1	1	1	μA max	
LOGIC INPUTS (LDAC, $\overline{TFS}$, TCLK, DT)					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[7]	10	10	10	pF max	
ANALOG OUTPUT					
Output Voltage Range	±3	±3	±3	V nom	
dc Output Impedance	0.3	0.3	0.3	Ω typ	
Short-Circuit Current	20	20	20	mA typ	
AC CHARACTERISTICS[7]					
Voltage Output Settling-Time					Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	3	3	3	μs max	Typically 2 μs
Negative Full-Scale Change	3	3	3	μs max	Typically 2.5 μs
Digital-to-Analog Glitch Impulse	10	10	10	nV secs typ	DAC Code Change All 1s to All 0s
Digital Feedthrough	2	2	2	nV secs typ	
V_{IN} to V_{OUT} Isolation	100	100	100	dB typ	V_{IN} = ±3 V, 41.5 kHz Sine Wave
POWER REQUIREMENTS	As per ADC Section				

NOTES
[1]Temperature ranges are as follows: A/B Versions, −40°C to +85°C; T Version, −55°C to +125°C.
[2]V_{OUT} (pk-pk) = ±3 V.
[3]SNR calculation includes distortion and noise components.
[4]Using external sample and hold.
[5]Measured with respect to RI DAC and includes bipolar offset error.
[6]For capacitive loads greater than 50 pF a series resistor is required (see INTERNAL REFERENCE section).
[7]Sample tested @ +25°C to ensure compliance.
Specifications subject to notice without notice.

ORDERING GUIDE

Model	Temperature Range	Signal-to-Noise Ratio	Relative Accuracy	Package Option[1]
AD7868AN	−40°C to +85°C	70 dB	±1/2 LSB typ	N-24
AD7868AQ	−40°C to +85°C	70 dB	±1/2 LSB typ	Q-24
AD7868TQ[2]	−55°C to +125°C	70 dB	±1 LSB max	Q-24
AD7868BN	−40°C to +85°C	72 dB	±1 LSB max	N-24
AD7868BQ	−40°C to +85°C	72 dB	±1 LSB max	Q-24
AD7868AR	−40°C to +85°C	70 dB	±1/2 LSB typ	R-28
AD7868BR	−40°C to +85°C	72 dB	±1 LSB max	R-28

NOTES
[1]N = Plastic DIP; Q = Cerdip; R = SOIC (Small Outline IC). For outline information see Package Information section.
[2]AD7868TQ wil be available to /883B processing only. Contact local sales office for military data sheet.



TIMING CHARACTERISTICS (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V)

Parameter	Limit at T_{min}, T_{max} (A, B Versions)	Limit at T_{min}, T_{max} (T Version)	Units	Conditions/Comments
ADC TIMING				
t_1	50	50	ns min	$\overline{CONVST}$ Pulse Width
t_2[3]	440	440	ns min	RCLK Cycle Time, Internal Clock
t_3	100	100	ns min	$\overline{RFS}$ to RCLK Falling Edge Setup Time
t_4	20	20	ns min	RCLK Rising Edge to $\overline{RFS}$
	100	100	ns max	
t_5[4]	155	155	ns max	RCLK to Valid Data Delay, C_L = 35 pF
t_6	4	4	ns min	Bus Relinquish Time after RCLK
	100	100	ns max	
t_{13}[5]	2 RCLK +200 to 3 RCLK + 200	2 RCLK +200 to 3 RCLK + 200	ns typ	$\overline{CONVST}$ to $\overline{RFS}$ Delay
DAC TIMING				
t_7	50	50	ns min	$\overline{TFS}$ to TCLK Falling Edge
t_8	75	100	ns min	TCLK Falling Edge to $\overline{TFS}$
t_9[6]	150	200	ns min	TCLK Cycle Time
t_{10}	30	40	ns min	Data Valid to TCLK Setup Time
t_{11}	75	100	ns min	Data Valid to TCLK Hold Time
t_{12}	40	40	ns min	$\overline{LDAC}$ Pulse Width

NOTES

[1]Timing specifications are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]Serial timing is measured with a 4.7 kΩ pull-up resistor on DR and $\overline{RFS}$ and a 2 kΩ pull-up resistor on RCLK. The capacitance on all three outputs is 35 pF.

[3]When using internal clock, RCLK mark/space ratio (measured form a voltage level of 1.6 V) range is 40/60 to 60/40. For external clock, RCLK mark/space ratio = external clock mark/space ratio.

[4]DR will drive higher capacitance loads but this will add to t_5 since it increases the external RC time constant (4.7 kΩ//C_L) and hence the time to reach 2.4 V.

[5]Time 2 RCLK to 3 RCLK depends on conversion start to ADC clock synchronization.

[6]TCLK mark/space ratio is 40/60 to 60/40.

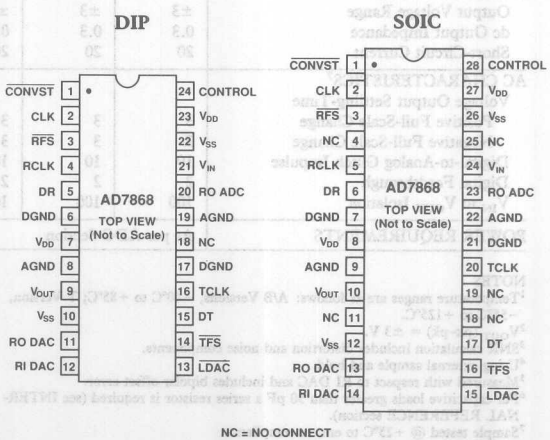
ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	−0.3 V to +7 V
V_{SS} to AGND	+0.3 V to −7 V
AGND to DGND	−0.3 V to V_{DD}+0.3 V
V_{OUT} to AGND	V_{SS} to V_{DD}
V_{IN} to AGND	V_{SS} −0.3 V to V_{DD}+0.3 V
RO ADC to AGND	−0.3 V to V_{DD}+0.3 V
RO DAC to AGND	−0.3 V to V_{DD}+0.3 V
RI DAC to AGND	−0.3 V to V_{DD}+0.3 V
Digital Inputs to DGND	−0.3 V to V_{DD}+0.3 V
Digital Outputs to DGND	−0.3 V to V_{DD}+0.3 V
Operating Temperature Range	
A, B Versions	−40°C to +85°C
T Version	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C
Power Dissipation (Any Package) to +75°C	450 mW
Derates above +75°C by	10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS



CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



PIN FUNCTION DESCRIPTION

DIP Pin Number	Mnemonic	Function
POWER SUPPLY		
7 & 23	V_{DD}	Positive Power Supply, 5 V ± 5%. Both V_{DD} pins must be tied together.
10 & 22	V_{SS}	Negative Power Supply, −5 V ± 5%. Both V_{SS} pins must be tied together.
8 & 19	AGND	Analog Ground. Both AGND pins must be tied together.
6 & 17	DGND	Digital Ground. Both DGND pins must be tied together.
ANALOG SIGNAL AND REFERENCE		
21	V_{IN}	ADC Analog Input. The ADC input range is ±3 V.
9	V_{OUT}	Analog Output Voltage from DAC. This output comes from a buffer amplifier. The range is bipolar, ±3 V with RI DAC = +3 V.
20	RO ADC	Voltage Reference Output. The internal ADC 3 V reference is provided at this pin. This output may be used as a reference for the DAC by connecting it to the RI DAC input. The external load capability of this reference is 500 μA.
11	RO DAC	DAC Voltage Reference Output. This is one of two internal voltage references. To operate the DAC with this internal reference, RO DAC should be connected to RI DAC. The external load capability of the reference is 500 μA.
12	RI DAC	DAC Voltage Reference Input. The voltage reference for the DAC must be applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7868 is 3 V.
ADC INTERFACE AND CONTROL		
2	CLK	Clock Input. An external TTL-compatible clock may be applied to this input. Alternatively, tying this pin to V_{SS} enables the internal laser-trimmed oscillator.
3	$\overline{RFS}$	Receive Frame Synchronization, Logic Output. This is an active low open-drain output which provides a framing pulse for serial data. An external 4.7 kΩ pull-up resistor is required on $\overline{RFS}$.
4	RCLK	Receive Clock, Logic Output. RCLK is the gated serial clock output which is derived from the internal or external ADC clock. If the CONTROL input is at V_{SS} the clock runs continuously. With the CONTROL input at DGND the RCLK output is gated off (three-state) after serial transmission is complete. RCLK is an open-drain output and requires an external 2 kΩ pull-up resistor.
5	DR	Receive Data, Logic Output. This is an open-drain data output used in conjunction with $\overline{RFS}$ and RCLK to transmit data from the ADC. Serial data is valid on the falling edge of RCLK when $\overline{RFS}$ is low. An external 4.7 kΩ resistor is required on the DR output.
1	$\overline{CONVST}$	Convert Start, Logic Input. A low to high transition on this input puts the track-and-hold amplifier into the hold mode and starts an ADC conversion. This input is asynchronous to the CLK input.
24	CONTROL	Control, Logic Input. With this pin at 0 V, the RCLK is noncontinuous. With this pin at −5 V, the RCLK is continuous. Note, tying this pin to V_{DD} places the part in a factory test mode where normal operation is not exhibited.
DAC INTERFACE AND CONTROL		
14	$\overline{TFS}$	Transmit Frame Synchronization, Logic Input. This is a frame or synchronization signal for the DAC with serial data expected after the falling edge of this signal.
15	DT	Transmit Data, Logic Input. This is the data input which is used in conjunction with $\overline{TFS}$ and TCLK to transfer serial data to the input latch.
16	TCLK	Transmit Clock, Logic Input. Serial data bits are latched on the falling edge of TCLK when $\overline{TFS}$ is low.
13	$\overline{LDAC}$	Load DAC, Logic Input. A new word is transferred into the DAC latch from the input latch on the falling edge of this signal.
18	NC	No Connect.

8

CONVERTER DETAILS

The AD7868 is a complete 12-bit I/O port, the only external components required for normal operation are pull-up resistors for the ADC data outputs and power supply decoupling capacitors. It is comprised of a 12-bit successive approximation ADC with a track/hold amplifier, a 12-bit DAC with a buffered output and two 3 V buried Zener references, a clock oscillator and control logic.

ADC CLOCK

The AD7868 has an internal clock oscillator which can be used for the ADC conversion procedure. The oscillator is enabled by tying the CLK input to V_{SS}. The oscillator is laser trimmed at the factory to give a conversion time of between 8.5 and 10 μs. The mark/space ratio can vary from 40/60 to 60/40. Alternatively, an external TTL compatible clock may be applied to this input. The allowable mark/space ratio of an external clock is 40/60 to 60/40. RCLK is a clock output, used for the serial interface. This output is derived directly from the ADC clock source and can be switched off at the end of conversion with the CONTROL input.

ADC CONVERSION TIMING

The conversion time for both external clock and continuous internal clock can vary from 19 to 20 rising clock edges depending on the conversion start to ADC clock synchronization. If a conversion is initiated within 30 ns prior to a rising edge of the ADC clock, the conversion time will consist of 20 rising clock edges, i.e., 9.5 μs conversion time. For noncontinuous internal clock, the conversion time is always 19 rising clock edges.

ADC TRACK-AND-HOLD AMPLIFIER

The track-and-hold amplifier on the analog input of the AD7868 allows the ADC to accurately convert an input sine wave of 6 V peak–peak amplitude to 12-bit accuracy. The input impedance is typically 9 kΩ, an equivalent circuit is shown in Figure 1. The input bandwidth of the track/hold amplifier is much greater than the Nyquist rate of the ADC, even when the ADC is operated at its maximum throughput rate. The 0.1 dB cut-off frequency occurs typically at 500 kHz. The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 2 μs.

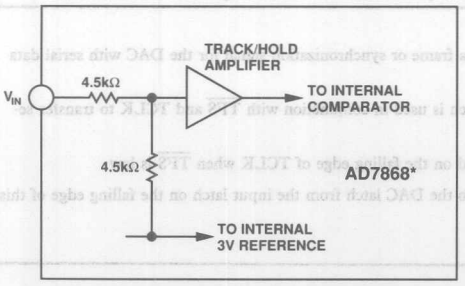


Figure 1. ADC Analog Input

The overall throughput rate is equal to the conversion time plus the track/hold amplifier acquisition time. For a 2.0 MHz input clock the throughput time is 12 μs max.

The operation of the track/hold amplifier is essentially transparent to the user. The track/hold amplifier goes from its track mode to its hold mode at the start of conversion on the rising edge of $\overline{CONVST}$.

INTERNAL REFERENCES

The AD7868 has two on-chip temperature compensated buried Zener references which are factory trimmed to 3 V ± 10 mV. One reference provides the appropriate biasing for the ADC, while the other is available as a reference for the DAC. Both reference outputs are available (labeled RO DAC and RO ADC) and are capable of providing up to 500 μA to an external load.

The DAC input reference (RI DAC) can be sourced externally or connected to any of the two on-chip references. Applications requiring good full-scale error matching between the DAC and the ADC should use the ADC reference as shown in Figure 4.

The maximum recommended capacitance on either of the reference output pins for normal operation is 50 pF. If either of the reference outputs is required to drive a capacitive load greater than 50 pF, then a 200 Ω resistor must be placed in series with the capacitive load. The addition of decoupling capacitors, 10 μF in parallel with 0.1 μF, as shown in Figure 2, improves noise performance. The improvement in noise performance can be seen from the graph in Figure 3. Note, this applies for the DAC output only; reference decoupling components do not affect ADC performance. So, a typical application will have just the DAC reference source decoupled with the other one open circuited.

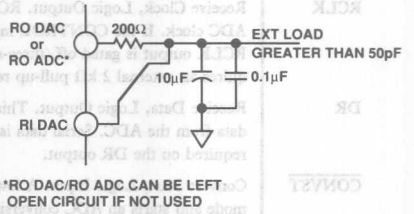


Figure 2. Reference Decoupling Circuitry

DAC OUTPUT AMPLIFIER

The output from the voltage-mode DAC is buffered by a noninverting amplifier. The buffer amplifier is capable of developing ±3 V across 2 kΩ and 100 pF load to ground and can produce 6 V peak-to-peak sine wave signals to a frequency of 20 kHz. The output is updated on the falling edge of the $\overline{LDAC}$ input. The output voltage settling time, to within 1/2 LSB of its final value, is typically less than 2 μs.

The small signal (200 mV p–p) bandwidth of the output buffer amplifier is typically 1 MHz. The output noise from the amplifier is low with a figure of 30 nV/$\sqrt{Hz}$ at a frequency of 1 kHz. The broadband noise from the amplifier exhibits a typical peak-to-peak figure of 150 μV for a 1 MHz output bandwidth. Figure 3 shows a typical plot of noise spectral density versus frequency for the output buffer amplifier and for either of the on-chip references.

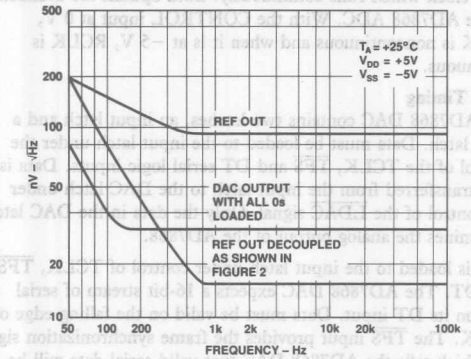


Figure 3. Noise Spectral Density vs. Frequency

INPUT/OUTPUT TRANSFER FUNCTIONS

A bipolar circuit for the AD7868 is shown in Figure 4. The analog input/output voltage range of the AD7868 is ±3 V. The designed code transitions for the ADC occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSB, 5/2 LSB . . . FS – 3/2 LSBs). The input/output code is 2s complement binary with 1 LSB = FS/4096 = 1.46 mV. The ideal transfer function is shown in Figure 5.

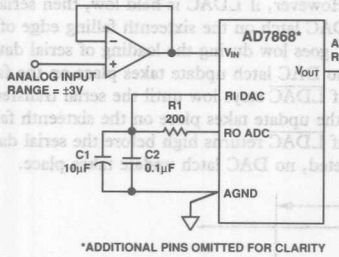


Figure 4. AD7868 Basic Bipolar Operation Using RO ADC as a Reference Input for the DAC

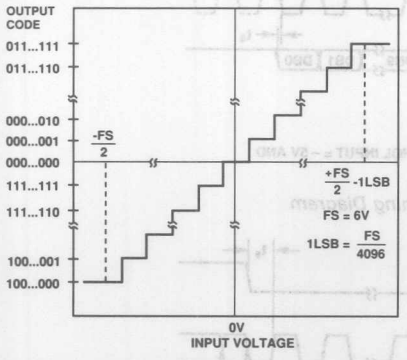


Figure 5. AD7868 Input/Output Transfer Function

OFFSET AND FULL-SCALE ADJUSTMENT

In most digital signal processing (DSP) applications, offset and full-scale errors have little or no effect on system performance. Offset error can always be eliminated in the analog domain by ac coupling. Full-scale errors do not cause problems as long as the input signal is within the full dynamic range of the ADC. For applications which require that the input signal range match the full analog input dynamic range of the ADC, offset and full-scale errors have to be adjusted to zero.

ADC ADJUSTMENT

Figure 6 has signal conditioning at the input and output of the AD7868 for trimming the end points of the transfer functions of both the ADC and the DAC. Offset error must be adjusted before full-scale error. For the ADC, this is achieved by trimming the offset of A1 while the input voltage, V1, is 1/2 LSB below ground. The trim procedure is as follows: apply a voltage of −0.73 mV (−1/2 LSB) at V1 in Figure 6 and adjust the offset voltage of A1 until the ADC output code flickers between 1111 1111 1111 (FFF HEX) and 0000 0000 0000 (000 HEX).

ADC gain error can be adjusted at either the first code transition (ADC negative full scale) or the last code transition (ADC positive full scale). The trim procedures for both cases are as follows (see Figure 6).

ADC Positive Full-Scale Adjustment

Apply a voltage of 2.9978 V (FS/2 − 3/2 LSBs) at V1. Adjust R2 until the ADC output code flickers between 0111 1111 1110 (7FE HEX) and 0111 1111 1111 (7FF HEX).

ADC Negative Full-Scale Adjustment

Apply a voltage of −2.9993 V (−FS/2 + 1/2 LSB) at V1 and adjust R2 until the ADC output code flickers between 1000 0000 0000 (800 HEX) and 1000 0000 0001 (801 HEX).

DAC ADJUSTMENT

Op amp A2 is included in Figure 6 for the DAC transfer function adjustment. Again offset must be adjusted before full scale. To adjust offset: load the DAC with 0000 0000 0000 (000 HEX) and trim the offset of A2 to 0 V. As with the ADC adjustment, gain error can be adjusted at either the first code transition (DAC negative full scale) or the last code transition (DAC positive full scale). The trim procedures for both cases are as follows:

DAC Positive Full-Scale Adjustment

Load the DAC with 0111 1111 1111 (7FF HEX) and adjust R7 until the op amp output voltage is equal to 2.9985 V, (FS/2 − 1 LSB).

DAC Negative Full-Scale Adjustment

Load the DAC with 1000 0000 0000 (800 HEX) and adjust R7 until the op amp output voltage is equal to 3.0 V (−FS/2).

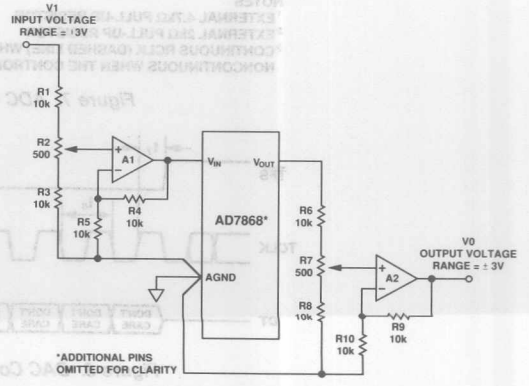


Figure 6. AD7868 with Input/Output Adjustment

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Communication with the AD7868 is managed by 6 dedicated pins. These consist of separate serial clocks, word framing or strobe pulses and data signals for both receiving and transmitting data. Conversion starts and DAC updating are controlled by two digital inputs; $\overline{\text{CONVST}}$ and $\overline{\text{LDAC}}$. These inputs can be asserted independently of the microprocessor by an external timer when precise sampling intervals are required. Alternatively, the $\overline{\text{LDAC}}$ and $\overline{\text{CONVST}}$ can be driven from a decoded address bus allowing the microprocessor control over conversion start and DAC updating as well as data communication to the AD7868.

ADC Timing

Conversion control is provided by the $\overline{\text{CONVST}}$ input. A low to high transition on $\overline{\text{CONVST}}$ input starts conversion and drives the track/hold amplifier into its hold mode. Serial data then becomes available while conversion is in progress. The corresponding timing diagram is shown in Figure 7. The word length is 16 bits; 4 leading zeros, followed by the 12-bit conversion result starting with the MSB. The data is synchronized to the serial clock output (RCLK) and is framed by the serial strobe ($\overline{\text{RFS}}$). Data is clocked out on a low to high transition of the serial clock and is valid on the falling edge of this clock while the $\overline{\text{RFS}}$ output is low. $\overline{\text{RFS}}$ goes low at the start of conversion and the first serial data bit (which is the first leading zero) is valid on the first falling edge of RCLK. All the ADC serial lines are open-drain outputs and require external pull-up resistors.

The serial clock out is derived from the ADC master clock source which may be internal or external. Normally, RCLK is required during the serial transmission only. In these cases it can be shut down (i.e., placed into high impedance) at the end of conversion to allow multiple ADCs to share a common serial bus. However, some serial systems (e.g., TMS32020) require a continuous serial clock. This can be achieved by using the CONTROL input on the AD7868 ADC. With the CONTROL input at 0 V, RCLK is noncontinuous and when it is at −5 V, RCLK is continuous.

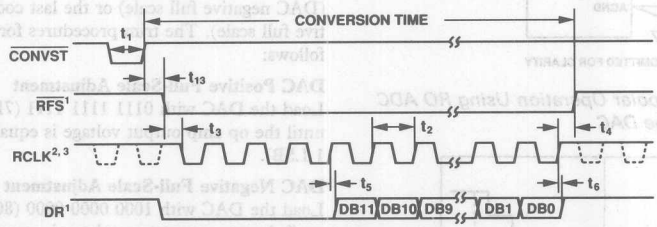
DAC Timing

The AD7868 DAC contains two latches, an input latch and a DAC latch. Data must be loaded to the input latch under the control of the TCLK, $\overline{\text{TFS}}$ and DT serial logic inputs. Data is then transferred from the input latch to the DAC latch under the control of the $\overline{\text{LDAC}}$ signal. Only the data in the DAC latch determines the analog output of the AD7868.

Data is loaded to the input latch under control of TCLK, $\overline{\text{TFS}}$ and DT. The AD7868 DAC expects a 16-bit stream of serial data on its DT input. Data must be valid on the falling edge of TCLK. The $\overline{\text{TFS}}$ input provides the frame synchronization signal which tells the AD7868 DAC that valid serial data will be available for the next 16 falling edges of TCLK. Figure 8 shows the timing diagram for the serial data format.

Although 16 bits of data are clocked into the input latch, only 12 bits are transferred into the DAC latch. Therefore, 4 bits in the stream are don't cares since their value does not affect the DAC latch data. The bit positions are 4 don't cares followed by the 12-bit DAC data starting with the MSB.

The $\overline{\text{LDAC}}$ signal controls the transfer of data to the DAC latch. Normally, data is loaded to the DAC latch on the falling edge of $\overline{\text{LDAC}}$. However, if $\overline{\text{LDAC}}$ is held low, then serial data is loaded to the DAC latch on the sixteenth falling edge of TCLK. If $\overline{\text{LDAC}}$ goes low during the loading of serial data to the input latch, no DAC latch update takes place on the falling edge of $\overline{\text{LDAC}}$. If $\overline{\text{LDAC}}$ stays low until the serial transfer is completed, then the update takes place on the sixteenth falling edge of TCLK. If $\overline{\text{LDAC}}$ returns high before the serial data transfer is completed, no DAC latch update takes place.



NOTES
[1]EXTERNAL 4.7kΩ PULL-UP RESISTOR
[2]EXTERNAL 2kΩ PULL-UP RESISTOR
[3]CONTINUOUS RCLK (DASHED LINE) WHEN THE CONTROL INPUT = −5V AND NONCONTINUOUS WHEN THE CONTROL INPUT = 0V

Figure 7. ADC Control Timing Diagram

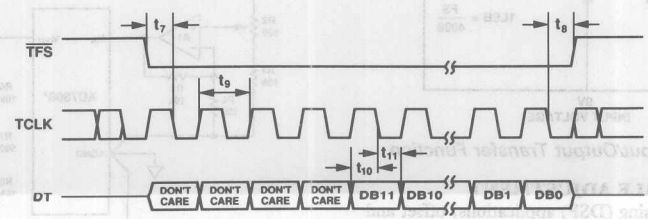


Figure 8. DAC Control Timing Diagram

The AD7868 is specified and 100% tested for dynamic performance specifications as well as traditional dc specifications such as integral and differential nonlinearity. These ac specifications are required for signal processing applications such as speech recognition, spectrum analysis, and high-speed modems. These applications require information on the converter's effect on the spectral content of the input signal. Hence, the parameters for which the AD7868 is specified include SNR, harmonic distortion and peak harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal-to-noise ratio at the output of the ADC or DAC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (fs/2) excluding dc. SNR is dependent upon the number of levels used in the quantization process; the more levels, the smaller the quantization noise. The theoretical signal-to-noise ratio for a sine wave input is given by

$$SNR = (6.02N + 1.76)\ dB \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

where N is the number of bits. Thus for an ideal 12-bit converter, SNR = 74 dB.

Effective Number of Bits

The formula given in Equation 1 relates the SNR to the number of bits. Rewriting the formula, as in Equation 2, it is possible to get a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR.

Harmonic Distortion

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7868, total harmonic distortion (THD) is defined as:

$$THD = 20\ log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through to the sixth harmonic. The THD is also derived from the FFT plot of the ADC or DAC output spectrum.

ADC Testing

The output spectrum from the ADC is evaluated by applying a sinewave signal of very low distortion to the V_{IN} input which is sampled at an 83 kHz sampling rate. A Fast Fourier Transform (FFT) plot is generated from which the SNR data can be obtained. Figure 9 shows a typical 2048 point FFT plot of the AD7868BQ ADC with an input signal of 10 kHz and a sampling frequency of 83 kHz. The SNR obtained from this graph is 73 dB. It should be noted that the harmonics are taken into account when calculating the SNR.

frequency for an AD7868BQ with a sampling frequency of 83 kHz. The effective number of bits typically falls between 11.7 and 11.85 corresponding to SNR figures of 72.2 and 73.1 dB.

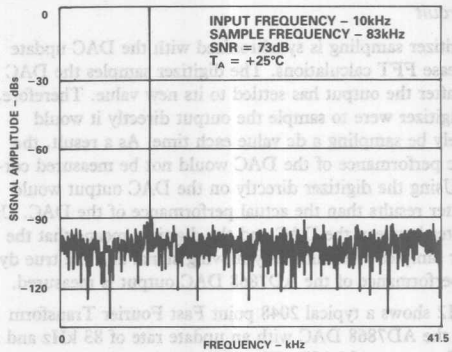


Figure 9. AD7868, ADC FFT Plot

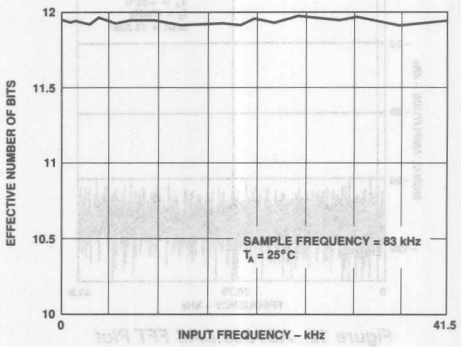


Figure 10. Effective Number of Bits vs. Frequency for the ADC

DAC Testing

A simplified diagram of the method used to test the dynamic performance specifications of the DAC is outlined in Figure 11. Data is loaded to the DAC under control of the microcontroller and associated logic. The output of the DAC is applied to a 9th order low-pass filter whose cut-off frequency corresponds to the Nyquist limit. The output of the filter is in turn applied to a 16-bit accurate digitizer. This digitizes the signal and the microcontroller generates an FFT plot from which the dynamic performance of the DAC can be evaluated.

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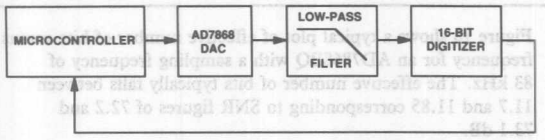


Figure 11. AD7868 DAC Dynamic Performance Test Circuit

The digitizer sampling is synchronized with the DAC update rate to ease FFT calculations. The digitizer samples the DAC output after the output has settled to its new value. Therefore, if the digitizer were to sample the output directly it would effectively be sampling a dc value each time. As a result, the dynamic performance of the DAC would not be measured correctly. Using the digitizer directly on the DAC output would give better results than the actual performance of the DAC. Using a filter between the DAC and the digitizer means that the digitizer samples a continuously moving signal and the true dynamic performance of the AD7868 DAC output is measured.

Figure 12 shows a typical 2048 point Fast Fourier Transform plot for the AD7868 DAC with an update rate of 83 kHz and an output frequency of 1 kHz. The SNR obtained from the graph is 73 dBs.

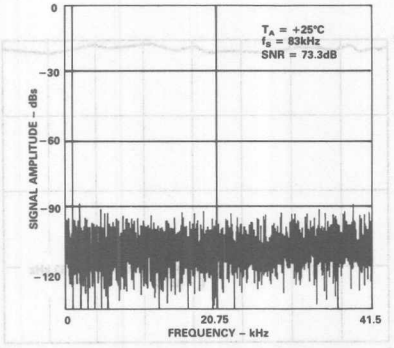


Figure 12. AD7868 DAC FFT Plot

Some applications will require improved performance versus frequency from the AD7868 DAC. In these applications, a simple sample-and-hold circuit such as that outlined in Figure 13 will extend the very good performance of the DAC to 20 kHz. Other applications will already have an inherent sample-and-hold function following the AD7868 DAC output. An example of this type of application is driving a switched-capacitor filter where the updating of the DAC is synchronized with the switched-capacitor filter. This inherent sample-and-hold function also extends the frequency range performance.

Performance versus Frequency

The typical performance plots of Figures 14 and 15 show the AD7868's DAC performance over a wide range of input frequencies at an update rate of 83 kHz. The plot of Figure 14 is without a sample-and-hold on the DAC output while the plot of Figure 15 is generated with a sample-and-hold on the output.

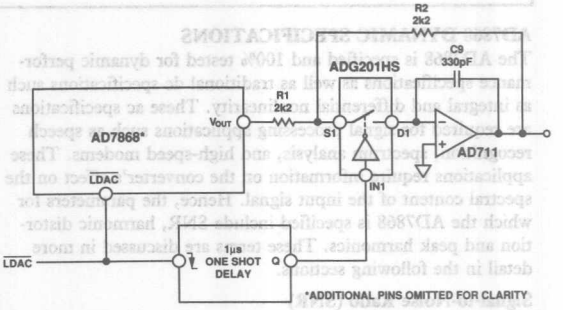


Figure 13. DAC Sample-and-Hold Circuit

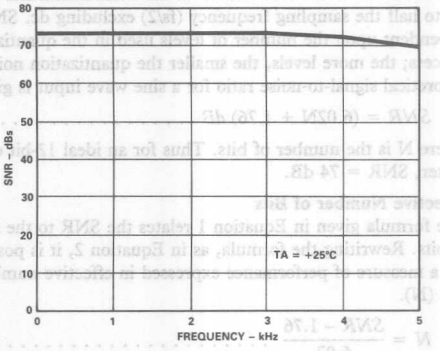


Figure 14. DAC Performance vs. Frequency (No Sample-and-Hold)

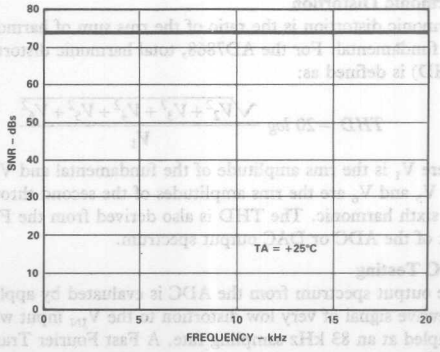


Figure 15. DAC Performance vs. Frequency (Sample-and-Hold)

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD7868 is via a serial bus that uses standard protocol compatible with DSP machines. The communication interface consists of separate transmit (DAC) and receive (ADC) sections whose operations can be either synchronous or asynchronous with respect to each other. Each section has a clock signal, a data signal and a frame or strobe pulse. Synchronous operation means that data is transmitted from the ADC and to the DAC at the same time. In this mode only one interface clock is needed and this has to be the ADC clock out, so RCLK must be connected to TCLK. For asynchronous operation, DAC and ADC data transfers are independent of each other, the ADC provides the receive clock (RCLK) while the transmit clock (TCLK) may be provided by the processor or the ADC or some other external clock source.

Another option to be considered with serial interfacing is the use of a gated clock. A gated clock means that the device that is sending the data switches on the clock when data is ready to be transmitted and three states the clock output when transmission is complete. Only 16 clock pulses are transmitted with the first data bit getting latched into the receiving device on the first falling clock edge. Ideally, there is no need for frame pulses, however, the AD7868 DAC frame input ($\overline{TFS}$) has to be driven high between data transmissions. The easiest method is to use $\overline{RFS}$ to drive $\overline{TFS}$ and use only synchronous interfacing. This avoids the use of interconnects between the processor and AD7868 frame signals. Not all processors have a gated clock facility, Figure 16 shows an example with the DSP56000.

Table I below shows the number of interconnect lines between the processor and the AD7868 for the different interfacing options. The AD7868 has the facility to use different clocks for transmitting and receiving data. This option, however, only exists on some processors and normally just one clock (ADC clock) is used for all communication with the AD7868. For simplicity, all the interface examples in this data sheet use synchronous interfacing and use the ADC clock (RCLK) as an input for the DAC clock (TCLK). For a better understanding of each of these interfaces, consult the relevant processor data sheet.

Configuration	No. of Interconnects	Signals
Synchronous	4	RCLK, DR, DT and $\overline{RFS}$ ($TCLK = RCLK$, $\overline{TFS} = \overline{RFS}$)
Asynchronous*	5 or 6	RCLK, DR, $\overline{RFS}$, DT, $\overline{TFS}$ (TCLK = RCLK or µP serial CLK)
Synchronous Gated Clock	3	RCLK, DR and DT ($TCLK = RCLK$, $\overline{TFS} = \overline{RFS}$)

*5 LINES OF INTERCONNECT WHEN TCLK = RCLK
6 LINES OF INTERCONNECT WHEN TCLK = µP SERIAL CLK

Table I. Interconnect Lines for Different Interfacing Options

AD7868 – DSP56000 Interface

Figure 16 shows a typical interface between the AD7868 and DSP56000. The interface arrangement is synchronous with a gated clock requiring only three lines of interconnect. The DSP56000 internal serial control registers have to be configured for a 16-bit data word with valid data on the first falling clock edge. Conversion starts and DAC updating are controlled by an external timer. Data transfers, which occur during ADC conversions, are between the processor receive and transmit shift registers and the AD7868's ADC and DAC. At the end of each 16-bit transfer the DSP56000 receives an internal interrupt indicating the transmit register is empty and the receive register is full.

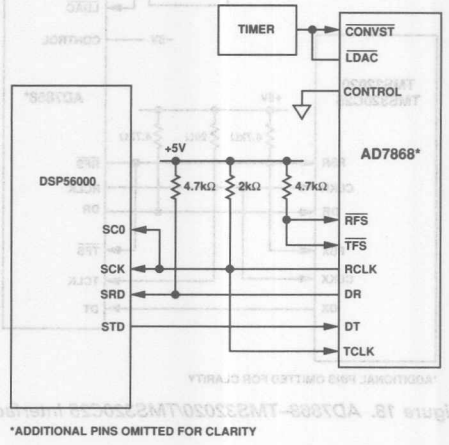


Figure 16. AD7868–DSP56000 Interface

AD7868 – ADSP-2101/ADSP-2102 Interface

An interface which is suitable for the ADSP-2101 or the ADSP-2102 is shown in Figure 17. The interface is configured for synchronous, continuous clock operation. The $\overline{LDAC}$ is tied low so the DAC gets updated on the sixteenth falling clock after $\overline{TFS}$ goes low. Alternatively $\overline{LDAC}$ may be driven from a timer as shown in Figure 16. As with the previous interface the processor receives an interrupt after reading or writing to the AD7868 and updates its own internal registers in preparation for the next data transfer.

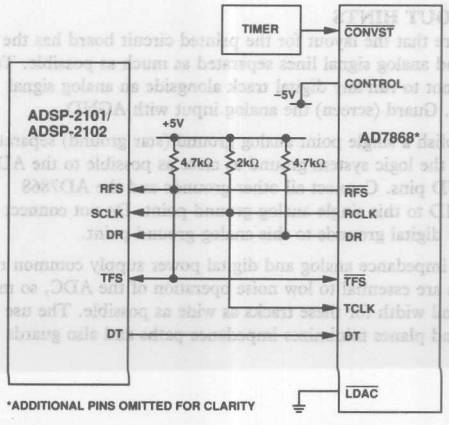


Figure 17. AD7868–ADSP-2101/ADSP-2102 Interface

AD7868 – TMS32020/TMS320C25 Interface

Figure 18 shows an interface which is suitable for the TMS32020/TMS320C25 processors. This interface is configured for synchronous, continuous clock operation. Note, the AD7868 will not interface correctly to these processors if the AD7868 is configured for a noncontinuous clock. Conversion starts and DAC updating are controlled by an external timer.

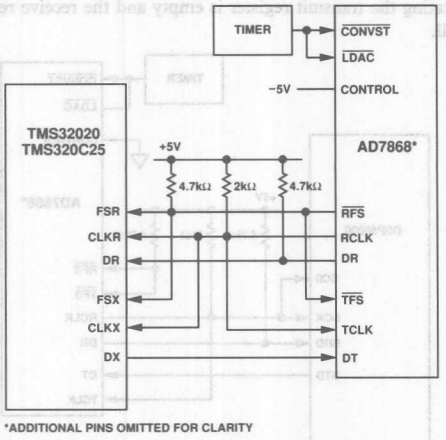


Figure 18. AD7868–TMS32020/TMS320C25 Interface

APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the circuit design itself in achieving high speed A/D performance. The AD7868's comparator is required to make bit decisions on an LSB size of 1.465 mV. To achieve this, the designer has to be conscious of noise both in the ADC itself and in the preceding analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any ADC, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground as close as possible to the AD7868 AGND pins. Connect all other grounds and the AD7868 DGND to this single analog ground point. Do not connect any other digital grounds to this analog ground point.

Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise. The circuit layout of Figures 22 and 23 have both analog and digital ground planes which are kept separated and only joined together at the AD7868 AGND pins.

NOISE

Keep the input signal leads to V_{IN} and signal return leads from AGND as short as possible to minimize input noise coupling. In applications where this is not possible, use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

INPUT/OUTPUT BOARD

Figure 19 shows an analog I/O board based on the AD7868. The corresponding printed circuit board (PCB) layout and silkscreen are shown in Figures 21 to 23.

The analog input to the AD7868 is buffered with an AD711 op amp. There is a component grid provided near the analog input on the PCB which may be used for an antialiasing filter for the ADC or a reconstruction filter for the DAC or any other conditioning circuitry. To facilitate this option, there are two wire links (labeled LK1 and LK2) required on the analog input and output tracks.

The board contains a SHA circuit which can be used on the output of the AD7868 DAC to extend the very good performance of the part over a wider frequency range. The increased performance from the SHA can be seen in Figures 14 and 15 of this data sheet. A wire link (labeled LK3) connects the board output to either the SHA output or directly to the AD7868 DAC output.

There are three $\overline{\text{LDAC}}$ link options on the board; $\overline{\text{LDAC}}$ can be driven from an external source independent of $\overline{\text{CONVST}}$, $\overline{\text{LDAC}}$ can be tied to $\overline{\text{CONVST}}$ or $\overline{\text{LDAC}}$ can be tied to GND. Choosing the latter option of tying $\overline{\text{LDAC}}$ to GND disables the SHA operation, and places the SHA permanently in the track mode.

Microprocessor connections to the board are made by a 9-way D-type connector. The pinout is shown in Figure 20. The ADC's digital outputs are buffered with 74HC4050s. These buffers provide a higher current output capability for high capacitance loads or cables. Normally, these buffers are not required as the AD7868 will be sitting on the same board as the processor.

POWER SUPPLY CONNECTIONS

The PCB requires two analog power supplies and one 5 V digital supply. Connections to the analog supply are made directly to the PCB as shown on the silkscreen in Figure 21. The connections are labeled V+ and V− and the range for both of these supplies is 12 V to 15 V. Connections to the 5 V digital supply are made through the D-type connector SKT6. The ±5 V analog supply required by the AD7868 are generated from two voltage regulators on the V+ and V− supplies.

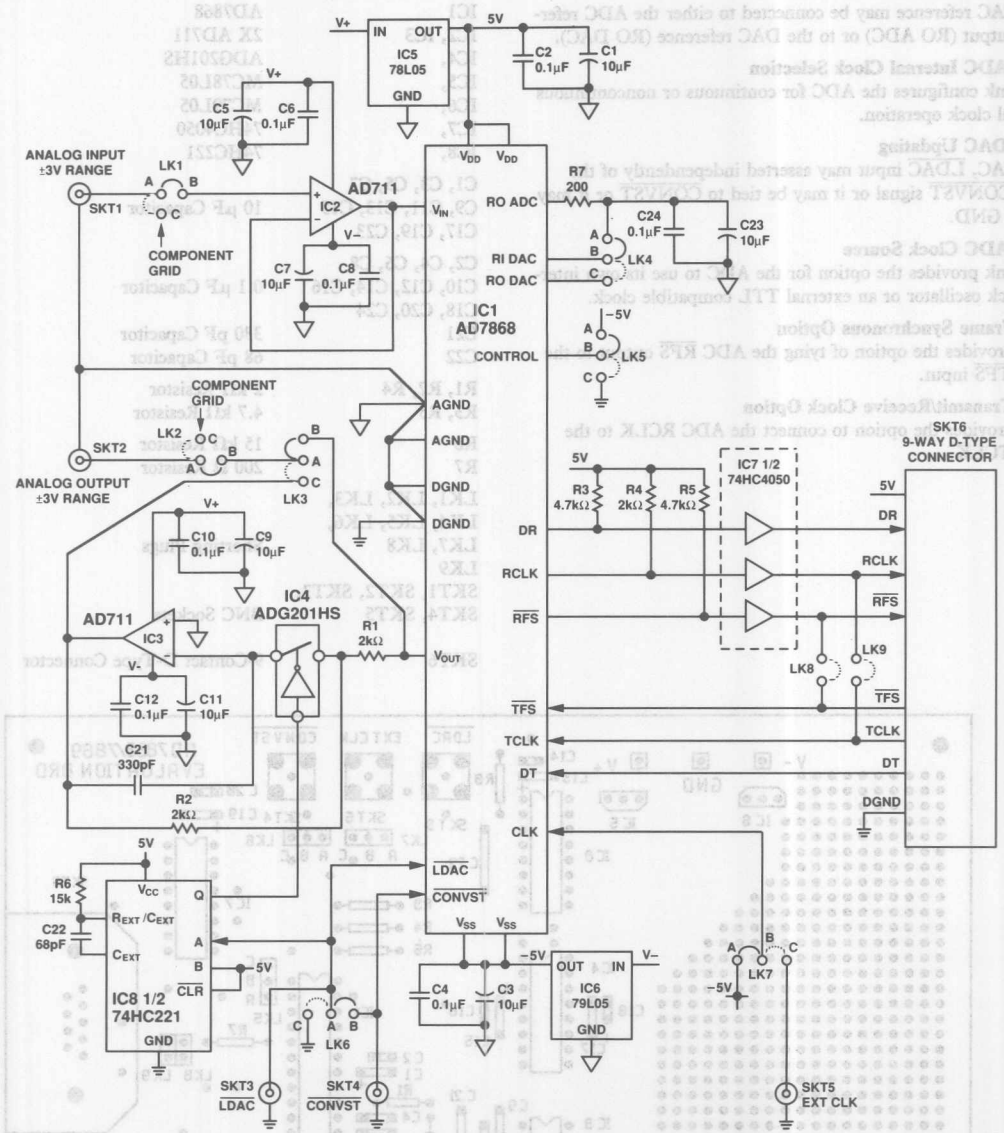


Figure 19. Input/Output Circuit Based on the AD7868

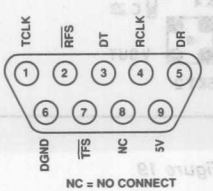


Figure 20. SKT6, D-Type Connector Pinout

WIRE LINK OPTIONS

LK1, Analog Input Link

LK1 connects the analog input to a component grid or to a buffer amplifier which drives the ADC input.

LK2, Analog Output Link

LK2 connects the analog output to the component grid or to either the SHA or DAC output (see LK3).

LK3, SHA or DAC Select

The analog output may be taken directly from the DAC or from a SHA at the output of the DAC.

LK4, DAC Reference Selection
The DAC reference may be connected to either the ADC reference output (RO ADC) or to the DAC reference (RO DAC).

LK5, ADC Internal Clock Selection
This link configures the ADC for continuous or noncontinuous internal clock operation.

LK6, DAC Updating
The DAC, $\overline{\text{LDAC}}$ input may asserted independently of the ADC $\overline{\text{CONVST}}$ signal or it may be tied to $\overline{\text{CONVST}}$ or it may tied to GND.

LK7, ADC Clock Source
This link provides the option for the ADC to use its own internal clock oscillator or an external TTL compatible clock.

LK8 Frame Synchronous Option
LK8 provides the option of tying the ADC $\overline{\text{RFS}}$ output to the DAC $\overline{\text{TFS}}$ input.

LK9 Transmit/Receive Clock Option
LK9 provides the option to connect the ADC RCLK to the DAC TCLK.

COMPONENT LIST

IC1	AD7868
IC2, IC3	2X AD711
IC4,	ADG201HS
IC5,	MC78L05
IC6,	MC79L05
IC7,	74HC4050
IC8,	74HC221
C1, C3, C5, C7 C9, C11, C13, C15 C17, C19, C23	10 µF Capacitor
C2, C4, C6, C8 C10, C12, C14, C16 C18, C20, C24	0.1 µF Capacitor
C21	330 pF Capacitor
C22	68 pF Capacitor
R1, R2, R4	2 kΩ Resistor
R3, R5	4.7 kΩ Resistor
R6	15 kΩ Resistor
R7	200 Ω Resistor
LK1, LK2, LK3, LK4, LK5, LK6, LK7, LK8 LK9	Shorting Plugs
SKT1, SKT2, SKT3, SKT4, SKT5	BNC Sockets
SKT6	9-Contact D-Type Connector

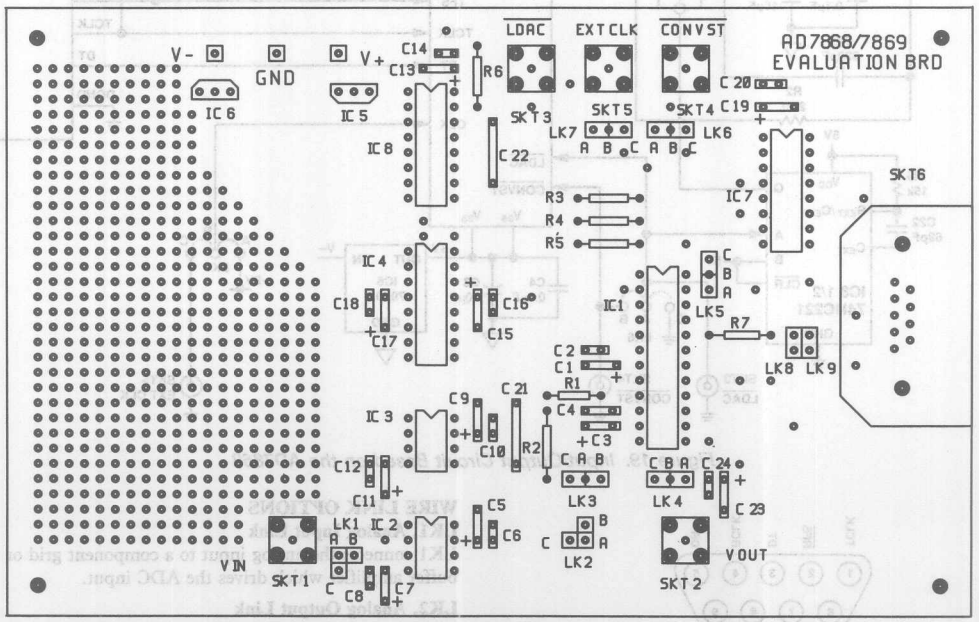


Figure 21. Silkscreen for the Circuit Diagram of Figure 19

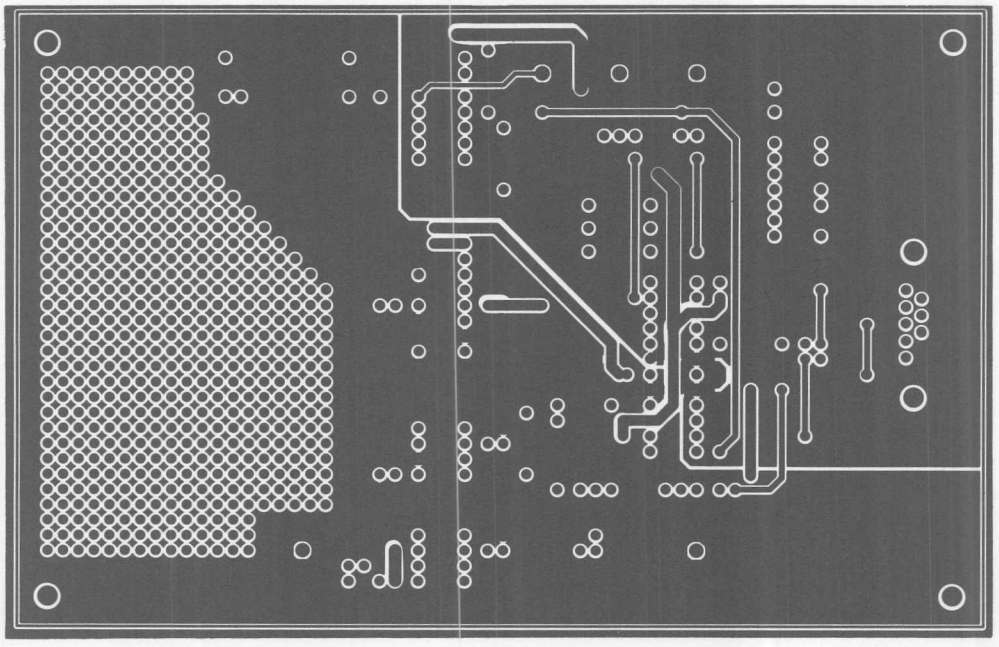


Figure 22. Component Side Layout for the Circuit Diagram of Figure 19

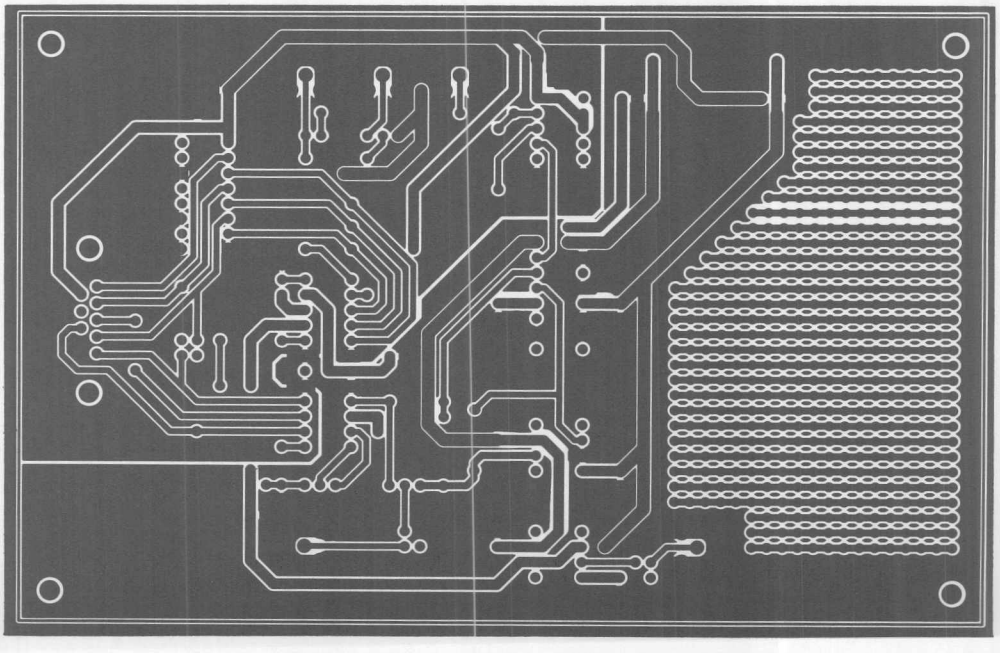
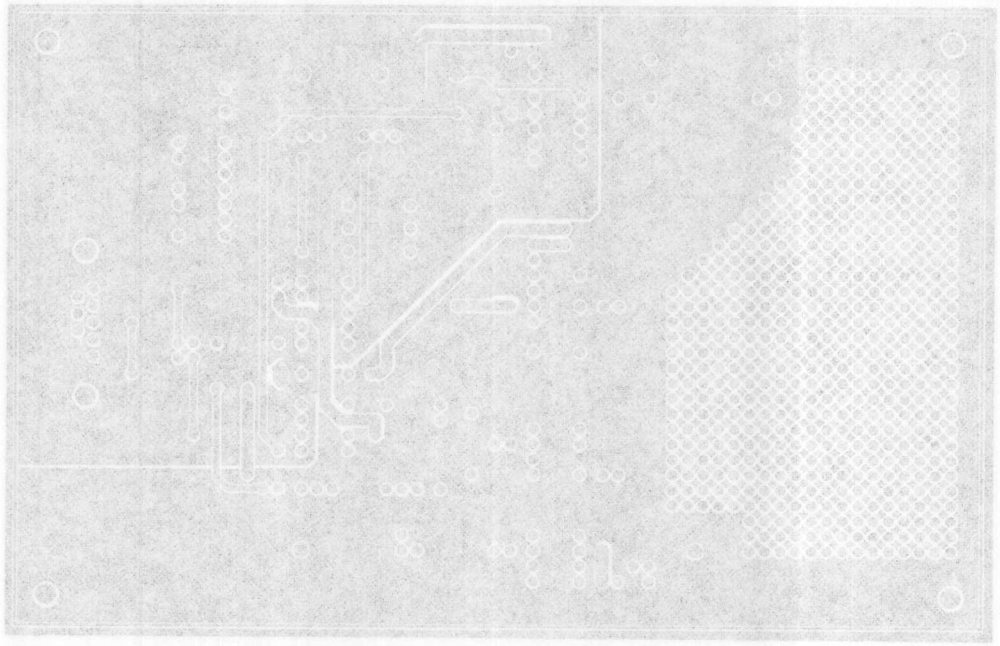
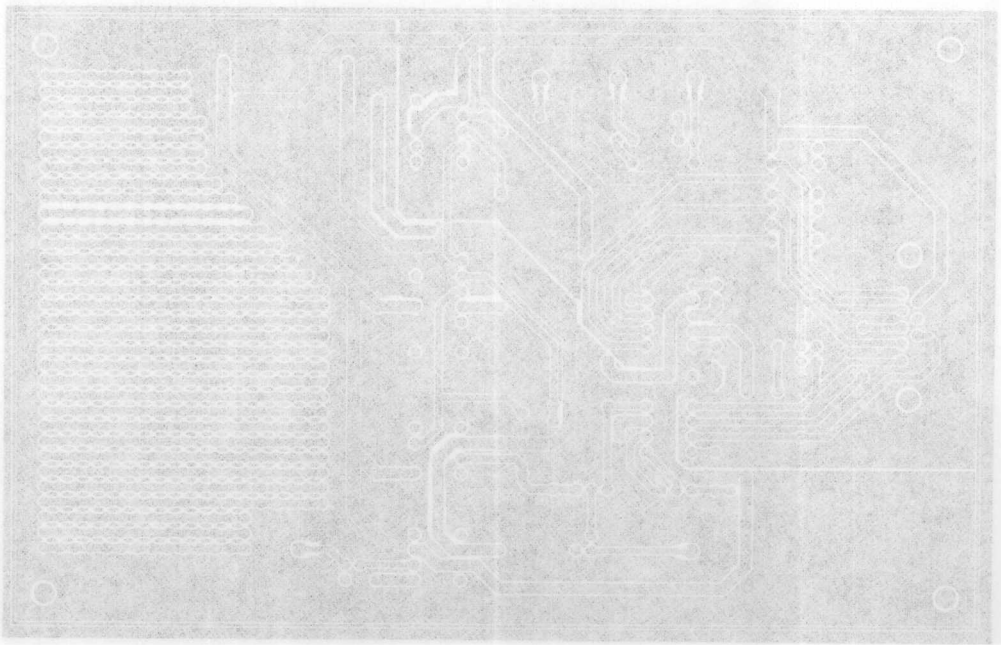


Figure 23. Solder Side Layout for the Circuit Diagram of Figure 19





ANALOG DEVICES

LC²MOS
Complete, 14-Bit Analog I/O System
AD7869

FEATURES
Complete 14-Bit I/O System, Comprising
14-Bit ADC with Track/Hold Amplifier
83 kHz Throughput Rate
14-Bit DAC with Output Amplifier
3.5 μs Settling Time
On-Chip Voltage Reference
Operates from ±5 V Supplies
Low Power – 130 mW typ
Small 0.3" Wide DIP

APPLICATIONS
Digital Signal Processing
Speech Recognition and Synthesis
Spectrum Analysis
High Speed Modems
DSP Servo Control

GENERAL DESCRIPTION

The AD7869 is a complete 14-bit I/O system containing a DAC and an ADC. The ADC is a successive approximation type with a track-and-hold amplifier having a combined throughput rate of 83 kHz. The DAC has an output buffer amplifier with a settling time of 4 μs to 14 bits. Temperature compensated 3 V buried Zener references provide precision references for the DAC and ADC.

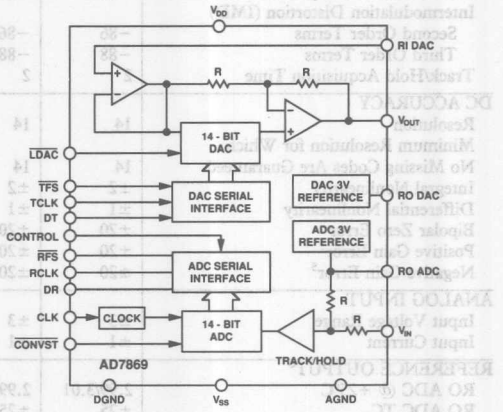
Interfacing to both the DAC and ADC is serial, minimizing pin count and giving a small 24-pin package size. Standard control signals allow serial interfacing to most DSP machines.

Asynchronous ADC conversion control and DAC updating is made possible with the $\overline{\text{CONVST}}$ and $\overline{\text{LDAC}}$ logic inputs.

The AD7869 operates form ±5 V power supplies, the analog input/output range of the ADC/DAC is ±3 V. The part is fully specified for dynamic parameters such as signal-to-noise ratio and harmonic distortion as well as traditional dc specifications.

The part is available in a 24-pin, 0.3 inch wide, plastic or hermetic dual-in-line package (DIP) and in a 28-pin, plastic SOIC package.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. Complete 14-Bit I/O System.
   The AD7869 contains a 14-bit ADC with a track-and-hold amplifier and a 14-bit DAC with output amplifier. Also included are separate on-chip voltage references for the DAC and the ADC.
2. Dynamic Specifications for DSP Users.
   In addition to traditional dc specifications, the AD7869 is specified for ac parameters including signal-to-noise ratio and harmonic distortion. These parameters along with important timing parameters are tested on every device.
3. Small Package.
   The AD7869 is available in a 24-pin DIP and a 28-pin SOIC package.

8

Parameter	J Version[1]	A Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]				
Signal-to-Noise Ratio[3, 4] (SNR) @ +25°C	78	78	dB min	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
T_{min} to T_{max}	78	77	dB min	
Total Harmonic Distortion (THD)	−86	−86	dB typ	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
Peak Harmonic or Spurious Noise	−86	−86	dB typ	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
Intermodulation Distortion (IMD)				
Second Order Terms	−86	−86	dB typ	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	−88	−88	dB typ	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Track/Hold Acquisition Time	2	2	µs max	
DC ACCURACY				
Resolution	14	14	Bits	
Minimum Resolution for Which No Missing Codes Are Guaranteed	14	14	Bits	
Integral Nonlinearity	±2	±2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	
Bipolar Zero Error	±20	±20	LSB max	
Positive Gain Error[5]	±20	±20	LSB max	
Negative Gain Error[5]	±20	±20	LSB max	
ANALOG INPUT				
Input Voltage Range	±3	±3	Volts	
Input Current	±1	±1	mA max	
REFERENCE OUTPUT[6]				
RO ADC @ +25°C	2.99/3.01	2.99/3.01	V min/ V max	
RO ADC TC	±25	±25	ppm/°C typ	
		±40	±ppm/°C max	
Reference Load Sensitivity (ΔRO ADC vs. ΔI)	−1.5	−1.5	mV max	Reference Load Current Change (0–500 µA), Reference Load Should Not Be Changed During Conversion
LOGIC INPUTS (CONVST, CLK, CONTROL)				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Current[7] (CONTROL & CLK)	±10	±10	µA max	V_{IN} = V_{SS} to DGND
Input Capacitance, C_{IN}[8]	10	10	pF max	
LOGIC OUTPUTS				
DR, $\overline{RFS}$ Outputs				
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA, Pull-Up Resistor = 4.7 kΩ
RCLK Output				
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 2.6 mA, Pull-Up Resistor = 2 kΩ
DR, $\overline{RFS}$, RCLK Outputs				
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[8]	15	15	pF max	
CONVERSION TIME				
External Clock	10	10	µs max	
Internal Clock	10	10	µs max	The Internal Clock Has a Nominal Value of 2.0 MHz
POWER REQUIREMENTS				For Both DAC and ADC
V_{DD}	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	V nom	±5% for Specified Performance
I_{DD}	22	22	mA max	Cumulative Current from the Two V_{DD} Pins
I_{SS}	12	12	mA max	Cumulative Current from the Two V_{SS} Pins
Total Power Dissipation	170	170	mW max	Typically 130 mW

NOTES

[1]Temperature ranges are as follows: J Version, 0°C to +70°C; A Version, −40°C to +85°C.

[2]V_{IN} = ±3 V.

[3]SNR calculation includes distortion and noise components.

[4]SNR degradation due to asynchronous DAC updating during conversion is 0.1 dB typ.

[5]Measured with respect to internal reference.

[6]*For capacitive loads greater than 50 pF a series resistor is* required (see Internal Reference section).

[7]Tying the CONTROL input to V_{DD} places the device in a factory test mode where normal operation is not exhibited.

[8]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

DAC SECTION (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V, RI DAC = +3 V and decoupled as shown in Figure 2, V_{OUT} Load to AGND; = 2 kΩ, C_L = 100 pF. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J Version[1]	A Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]				
Signal-to-Noise Ratio[3] (SNR) @ +25°C	78	78	dB min	V_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 83 kHz
T_{min} to T_{max}	78	77	dB min	Typically 82 dB at +25°C for 0 <V_{OUT}<20 kHz[4]
Total Harmonic Distortion (THD)	−86	−86	dB typ	V_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 83 kHz
				Typically −84 dB at +25°C for 0 <V_{OUT}<20 kHz[4]
Peak Harmonic or Spurious Noise	−86	−86	dB typ	V_{OUT} = 1 kHz, f_{SAMPLE} = 83 kHz
				Typically −84 dB at +25°C for 0 <V_{OUT}<20 kHz[4]
DC ACCURACY				
Resolution	14	14	Bits	
Integral Nonlinearity	±2	±2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
Bipolar Zero Error	±10	±10	LSB max	
Positive Full-Scale Error[5]	±10	±10	LSB max	
Negative Full-Scale Error[5]	±10	±10	LSB max	
REFERENCE OUTPUT[6]				
RO DAC @ +25°C	2.99/3.01	2.99/3.01	V min/V max	
RO DAC TC	±25	±25	ppm/°C typ	
		±40	ppm/°C max	
Reference Load Change				
(ΔRO DAC vs. ΔI)	−1.5	−1.5	mV max	Reference Load Current Change (0–500 μA)
REFERENCE INPUT				
RI DAC Input Range	2.85/3.15	2.85/3.15	V min/V max	3 V ±5%
Input Current	1	1	μA max	
LOGIC INPUTS				
(LDAC, TFS, TCLK, DT)				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V ±5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ±5%
Input Current, I_{IN}	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[7]	10	10	pF max	
ANALOG OUTPUT				
Output Voltage Range	±3	±3	V nom	
DC Output Impedance	0.3	0.3	Ω typ	
Short-Circuit Current	20	20	mA typ	
AC CHARACTERISTICS[7]				
Voltage Output Settling-Time				Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	4	4	μs max	Typically 3 μs
Negative Full-Scale Change	4	4	μs max	Typically 3.5 μs
Digital-to-Analog Glitch Impulse	10	10	nV secs typ	DAC Code Change All 1s to All Os
Digital Feedthrough	2	2	nV secs typ	
V_{IN} to V_{OUT} Isolation	100	100	dB typ	V_{IN} = ±3 V, 41.5 kHz Sine Wave
POWER REQUIREMENTS	As per ADC Section			

NOTES
[1]Temperature ranges are as follows: J Version, 0°C to +70°C; A Version, −40°C to +85°C.
[2]V_{OUT} (p–p) = ±3 V.
[3]SNR calculation includes distortion and noise components.
[4]Using external sample and hold, see Figures 13 to 15.
[5]Measured with respect to REF IN and includes bipolar offset error.
[6]For capacitive loads greater than 50 pF a series resistor is required (see Internal Reference section).
[7]Sample tested @ +25°C to ensure compliance.
Specifications subject to change without notice.

8

AD7869—TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ±5%, AGND = DGND = 0 V)

Parameter	Limit at T_{min}, T_{max} (All Versions)	Units	Conditions/Comments
ADC TIMING			
t_1	50	ns min	$\overline{CONVST}$ Pulse Width
t_2[3]	440	ns min	RCLK Cycle Time, Internal Clock
t_3	100	ns min	$\overline{RFS}$ to RCLK Falling Edge Setup Time
t_4	20	ns min	RCLK Rising Edge to $\overline{RFS}$
	100	ns max	
t_5[4]	155	ns max	RCLK to Valid Data Delay, C_L = 35 pF
t_6	4	ns min	Bus Relinquish Time after RCLK
	100	ns max	
t_{13}[5]	2 RCLK +200 to 3 RCLK + 200	ns typ	$\overline{CONVST}$ to $\overline{RFS}$ Delay
DAC TIMING			
t_7	50	ns min	$\overline{TFS}$ to TCLK Falling Edge
t_8	75	ns min	TCLK Falling Edge to $\overline{TFS}$
t_9[6]	150	ns min	TCLK Cycle Time
t_{10}	30	ns min	Data Valid to TCLK Setup Time
t_{11}	75	ns min	Data Valid to TCLK Hold Time
t_{12}	40	ns min	$\overline{LDAC}$ Pulse Width

NOTES
[1]Timing specifications are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]Serial timing is measured with a 4.7 kΩ pull-up resistor on DR and $\overline{RFS}$ and a 2 kΩ pull-up resistor on RCLK. The capacitance on all three outputs is 35 pF.
[3]When using internal clock, RCLK mark/space ratio (measured form a voltage level of 1.6 V) range is 40/60 to 60/40. For external clock, RCLK mark/space ratio = external clock mark/space ratio.
[4]DR will drive higher capacitance loads but this will add to t_s since it increases the external RC time constant (4.7 kΩ//C_L) and hence the time to reach 2.4 V.
[5]Time 2 RCLK to 3 RCLK depends on conversion start to ADC clock synchronization.
[6]TCLK mark/space ratio is 40/60 to 60/40.

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	−0.3 V to +7 V
V_{SS} to AGND	+0.3 V to −7 V
AGND to DGND	−0.3 V to V_{DD}+0.3 V
V_{OUT} to AGND	V_{SS} to V_{DD}
V_{IN} to AGND	V_{SS} −0.3 V to V_{DD}+0.3 V
RO ADC to AGND	−0.3 V to V_{DD}+0.3 V
RO DAC to AGND	−0.3 V to V_{DD}+0.3 V
RI DAC to AGND	−0.3 V to V_{DD}+0.3 V
Digital Inputs to DGND	−0.3 V to V_{DD}+0.3 V
Digital Outputs to DGND	−0.3 V to V_{DD}+0.3 V
Operating Temperature Range	
J Version	0°C to +70°C
A Version	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C
Power Dissipation (Any Package) to +75°C	1000 mW
Derates above +75°C by	10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



ORDERING GUIDE

Model	Temperature Range	Signal-to-Noise Ratio (SNR)	Relative Accuracy	Package Option*
AD7869JN	0°C to +70°C	78 dB	±2 LSB max	N-24
AD7869JR	0°C to +70°C	78 dB	±2 LSB max	R-28
AD7869AQ	−40°C to +85°C	77 dB	±2 LSB max	Q-24

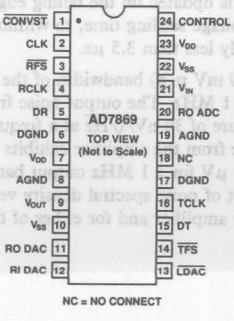
*N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

AD7869 PIN FUNCTION DESCRIPTION

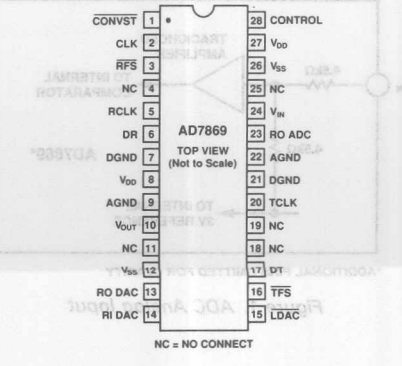
DIP Pin Number	Mnemonic	Function
POWER SUPPLY		
7 & 23	V_{DD}	Positive Power Supply, 5 V ± 5%. Both V_{DD} pins must be tied together.
10 & 22	V_{SS}	Negative Power Supply, −5 V ± 5%. Both V_{SS} pins must be tied together.
8 & 19	AGND	Analog Ground. Both AGND pins must be tied together.
6 & 17	DGND	Digital Ground. Both DGND pins must be tied together.
ANALOG SIGNAL AND REFERENCE		
21	V_{IN}	ADC Analog Input. The ADC input range is ±3 V.
9	V_{OUT}	Analog Output Voltage from DAC. This output comes from a buffer amplifier. The range is bipolar, ±3 V with RI DAC = +3 V.
20	RO ADC	Voltage Reference Output. The internal ADC 3 V reference is provided at this pin. This output may be used as a reference for the DAC by connecting it to the RI DAC input. The external load capability of this reference is 500 μA.
11	RO DAC	DAC Voltage Reference Output. This is one of two internal voltage references. To operate the DAC with this internal reference, RO DAC should be connected to RI DAC. The external load capability of the reference is 500 μA.
12	RI DAC	DAC Voltage Reference Input. The voltage reference for the DAC must be applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7869 is 3 V.
ADC INTERFACE AND CONTROL		
2	CLK	Clock Input. An external TTL-compatible clock may be applied to this input. Alternatively, tying this pin to V_{SS} enables the internal laser-trimmed oscillator.
3	$\overline{RFS}$	Receive Frame Synchronization, Logic Output. This is an active low open-drain output which provides a framing pulse for serial data. An external 4.7 kΩ pull-up resistor is required on $\overline{RFS}$.
4	RCLK	Receive Clock, Logic Output. RCLK is the gated serial clock output which is derived from the internal or external ADC clock. If the CONTROL input is at V_{SS}, the clock runs continuously. With the CONTROL input at DGND the RCLK output is gated off (three-state) after serial transmission is complete. RCLK is an open-drain output and requires an external 2 kΩ pull-up resistor.
5	DR	Receive Data, Logic Output. This is an open-drain data output used in conjunction with $\overline{RFS}$ and RCLK to transmit data from the ADC. Serial data is valid on the falling edge of RCLK when $\overline{RFS}$ is low. An external 4.7 kΩ resistor is required on the DR output.
1	$\overline{CONVST}$	Convert Start, Logic Input. A low to high transition on this input puts the track-and-hold amplifier into the hold mode and starts an ADC conversion. This input is asynchronous to the CLK input.
24	CONTROL	Control, Logic Input. With this pin at 0 V, the RCLK is noncontinuous. With this pin at −5 V, the RCLK is continuous. Note, tying this pin to V_{DD} places the part in a factory test mode where normal operation is not exhibited.
DAC INTERFACE AND CONTROL		
14	$\overline{TFS}$	Transmit Frame Synchronization, Logic Input. This is a frame or synchronization signal for the DAC with serial data expected after the falling edge of this signal.
15	DT	Transmit Data, Logic Input. This is the data input which is used in conjunction with $\overline{TFS}$ and TCLK to transfer serial data to the input latch.
16	TCLK	Transmit Clock, Logic Input. Serial data bits are latched on the falling edge of TCLK when $\overline{TFS}$ is low.
13	$\overline{LDAC}$	Load DAC, Logic Input. A new word is transferred into the DAC latch from the input latch on the falling edge of this signal.
18	NC	No Connect.

PIN CONFIGURATIONS

DIP



SOIC



8

components required for normal operation are pull-up resistors for the ADC data outputs and power supply decoupling capacitors. It is comprised of a 14-bit successive approximation ADC with a track/hold amplifier, a 14-bit DAC with a buffered output and two 3 V buried Zener references, a clock oscillator and control logic.

ADC CLOCK

The AD7869 has an internal clock oscillator which can be used for the ADC conversion procedure. The oscillator is enabled by tying the CLK input to V_{SS}. The oscillator is laser trimmed at the factory to give a maximum conversion time of 10 μs. The mark/space ratio can vary from 40/60 to 60/40. Alternatively, an external TTL compatible clock may be applied to this input. The allowable mark/space ratio of an external clock is 40/60 to 60/40.

RCLK is a clock output, used for the serial interface. This output is derived directly from the ADC clock source and can be switched off at the end of conversion with the CONTROL input.

ADC CONVERSION TIMING

The conversion time for both external clock and continuous internal clock can vary from 19 to 20 rising clock edges depending on the conversion start to ADC clock synchronization. If a conversion is initiated within 30 ns prior to a rising edge of the ADC clock, the conversion time will consist of 20 rising clock edges, i.e., 9.5 μs conversion time. For noncontinuous internal clock, the conversion time always consists of 19 rising clock edges.

ADC TRACK-AND-HOLD AMPLIFIER

The track-and-hold amplifier on the analog input of the AD7869 allows the ADC to accurately convert an input sine wave of 6 V peak–peak amplitude to 14-bit accuracy. The input impedance is typically 9 kΩ, an equivalent circuit is shown in Figure 1. The input bandwidth of the track/hold amplifier is much greater than the Nyquist rate of the ADC, even when the ADC is operated at its maximum throughput rate. The 0.1 dB cut-off frequency occurs typically at 500 kHz. The track/hold amplifier acquires an input signal to 14-bit accuracy in less than 2 μs. The overall throughput rate is equal to the conversion time plus the track/hold amplifier acquisition time. For a 2.0 MHz input clock the throughput time is 12 μs max.

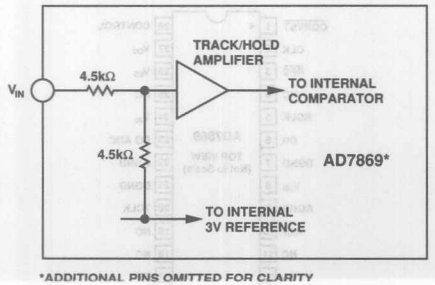


Figure 1. ADC Analog Input

mode to its hold mode at the start of conversion on the rising edge of CONVST.

INTERNAL REFERENCES

The AD7869 has two on-chip temperature compensated buried Zener references which are factory trimmed to 3 V ±10 mV. One reference provides the appropriate biasing for the ADC, while the other is available as a reference for the DAC. Both reference outputs are available (labelled RO DAC and RO ADC) and are capable of providing up to 500 μA to an external load.

The DAC input reference (RI DAC) can be sourced externally or connected to any of the two on-chip references. Applications requiring good full-scale error matching between the DAC and the ADC should use the ADC reference as shown in Figure 4.

The maximum recommended capacitance on either of the reference output pins for normal operation is 50 pF. If either of the reference outputs is required to drive a capacitive load greater than 50 pF, then a 200 Ω resistor must be placed in series with the capacitive load. The addition of decoupling capacitors, 10 μF in parallel with 0.1 μF, as shown in Figure 2 improves noise performance. The improvement in noise performance can be seen from the graph in Figure 3. Note, this applies for the DAC output only; reference decoupling components do not affect ADC performance. So, a typical application will have just the DAC reference decoupled with the other one open circuited.

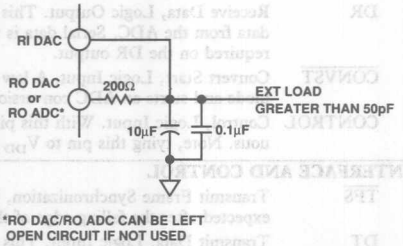


Figure 2. Reference Decoupling Components

DAC OUTPUT AMPLIFIER

The output from the voltage mode DAC is buffered by a noninverting amplifier. The buffer amplifier is capable of developing ±3 V across 2 kΩ and 100 pF load to ground and can produce 6 V peak-to-peak sine wave signals to a frequency of 20 kHz. The output is updated on the falling edge of the LDAC input. The output voltage settling time, to within 1/2 LSB of its final value, is typically less than 3.5 μs.

The small signal (200 mV p–p) bandwidth of the output buffer amplifier is typically 1 MHz. The output noise from the amplifier is low with a figure of 30 nV/$\sqrt{Hz}$ at a frequency of 1 kHz. The broadband noise from the amplifier exhibits a typical peak-to-peak figure of 150 μV for a 1 MHz output bandwidth. Figure 3 shows a typical plot of noise spectral density versus frequency for the output buffer amplifier and for either of the on-chip references.

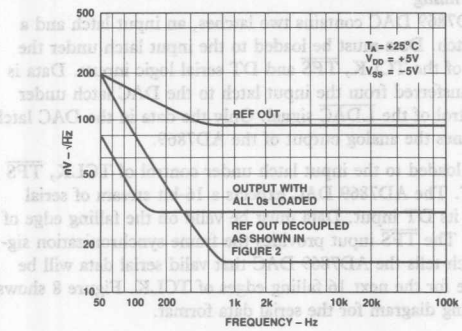


Figure 3. Noise Spectral Density vs. Frequency

INPUT/OUTPUT TRANSFER FUNCTIONS

A bipolar circuit for the AD7869 is shown in Figure 4.

The analog input/output voltage range of the AD7869 is ±3 V. The designed code transitions for the ADC occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSB, 5/2 LSB . . . FS −3/2 LSBs). The input/output code is 2s Complement Binary with 1 LSB = FS/16384 = 366 μV. The ideal transfer function is shown in Figure 5.

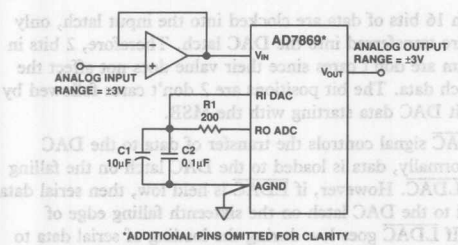


Figure 4. AD7869 Basic Bipolar Operation

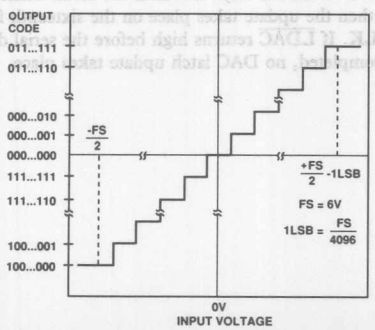


Figure 5. AD7869 Input/Output Transfer Function

OFFSET AND FULL SCALE ADJUSTMENT

In most digital signal processing (DSP) applications, offset and full-scale errors have little or no effect on system performance. Offset error can always be eliminated in the analog domain by ac coupling. Full-scale errors do not cause problems as long as the input signal is within the full dynamic range of the ADC. For applications which require that the input signal range match the full analog input dynamic range of the ADC, offset and full-scale errors have to be adjusted to zero.

ADC ADJUSTMENT

Figure 6 has signal conditioning at the input and output of the AD7869 for trimming the end points of the transfer functions of both the ADC and the DAC. Offset error must be adjusted before full-scale error. For the ADC, this is achieved by trimming the offset of A1 while the input voltage, V1, is 1/2 LSB below ground. The trim procedure is as follows: apply a voltage of −183 μV (−1/2 LSB) at V1 in Figure 6 and adjust the offset voltage of A1 until the ADC output code flickers between 11 1111 1111 1111 (3 FFF HEX) and 00 0000 0000 0000 (0000 HEX).

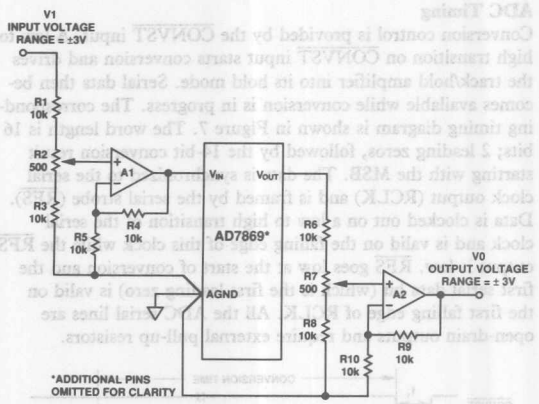


Figure 6. AD7869 with Input/Output Adjustment

ADC gain error can be adjusted at either the first code transition (ADC negative full scale) or the last code transition (ADC positive full scale). The trim procedures for both cases are as follows (see Figure 6).

ADC Positive Full-Scale Adjustment

Apply a voltage of 2.99945 V (FS/2 – 3/2 LSBs) at V1. Adjust R2 until the ADC output code flickers between 01 1111 1111 1110 (1FFE HEX) and 01 1111 1111 1111 (1FFF HEX).

ADC Negative Full-Scale Adjustment

Apply a voltage of −2.99982 V (−FS/2 + 1/2 LSB) at V1 and adjust R2 until the ADC output code flickers between 10 0000 0000 0000 (2000 HEX) and 10 0000 0000 0001 (2001 HEX).

DAC ADJUSTMENT

Op amp A2 is included in Figure 6 for the DAC transfer function adjustment. Again offset must be adjusted before full scale. To adjust offset: load the DAC with 00 0000 0000 0000 (0000 HEX) and trim the offset of A2 to 0 V. As with the ADC adjustment, gain error can be adjusted at either the first code transition (DAC negative full scale) or the last code transition (DAC positive full scale). The trim procedures for both cases are as follows:

DAC Positive Full-Scale Adjustment

Load the DAC with 01 1111 1111 1111 (1 FFF HEX) and adjust R7 until the op amp output voltage is equal to 2.99963 V, (FS/2 – 1 LSB).

DAC Negative Full-Scale Adjustment

Load the DAC with 10 0000 0000 0000 (2000 HEX) and adjust R7 until the op amp output voltage is equal to −3 V (−FS/2).

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TIMING AND CONTROL

Communication with the AD7869 is managed by 6 dedicated pins. These consist of separate serial clocks, word framing or strobe pulses and data signals for both receiving and transmitting data. Conversion starts and DAC updating are controlled by two digital inputs; $\overline{\text{CONVST}}$ and $\overline{\text{LDAC}}$. These inputs can be asserted independently of the microprocessor by an external timer when precise sampling intervals are required. Alternatively, the $\overline{\text{LDAC}}$ and $\overline{\text{CONVST}}$ can be driven from a decoded address bus allowing the microprocessor control over conversion start and DAC updating as well as data communication to the AD7869.

ADC Timing

Conversion control is provided by the $\overline{\text{CONVST}}$ input. A low to high transition on $\overline{\text{CONVST}}$ input starts conversion and drives the track/hold amplifier into its hold mode. Serial data then becomes available while conversion is in progress. The corresponding timing diagram is shown in Figure 7. The word length is 16 bits; 2 leading zeros, followed by the 14-bit conversion result starting with the MSB. The data is synchronized to the serial clock output (RCLK) and is framed by the serial strobe ($\overline{\text{RFS}}$). Data is clocked out on a low to high transition of the serial clock and is valid on the falling edge of this clock while the $\overline{\text{RFS}}$ output is low. $\overline{\text{RFS}}$ goes low at the start of conversion and the first serial data bit (which is the first leading zero) is valid on the first falling edge of RCLK. All the ADC serial lines are open-drain outputs and require external pull-up resistors.

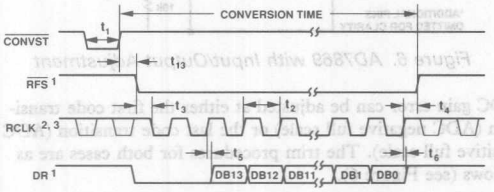


Figure 7. ADC Control Timing Diagram

The serial clock out is derived from the ADC master clock source which may be internal or external. Normally, RCLK is required during the serial transmission only. In these cases it can be shut down (i.e., placed into three-state) at the end of conversion to allow multiple ADCs to share a common serial bus. However, some serial systems (e.g., TMS32020) require a serial clock which runs continuously. Both options are available on the AD7869 ADC. With the CONTROL input at 0 V, RCLK is noncontinuous; and when it is at −5 V, RCLK is continuous.

DAC Timing

The AD7869 DAC contains two latches, an input latch and a DAC latch. Data must be loaded to the input latch under the control of the TCLK, $\overline{\text{TFS}}$ and DT serial logic inputs. Data is then transferred from the input latch to the DAC latch under the control of the $\overline{\text{LDAC}}$ signal. Only the data in the DAC latch determines the analog output of the AD7869.

Data is loaded to the input latch under control of TCLK, $\overline{\text{TFS}}$ and DT. The AD7869 DAC expects a 16-bit stream of serial data on its DT input. Data must be valid on the falling edge of TCLK. The $\overline{\text{TFS}}$ input provides the frame synchronization signal which tells the AD7869 DAC that valid serial data will be available for the next 16 falling edges of TCLK. Figure 8 shows the timing diagram for the serial data format.

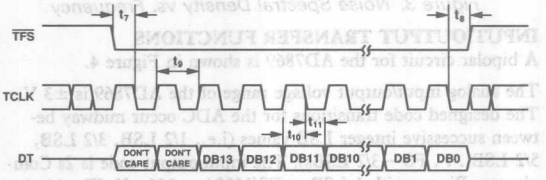


Figure 8. DAC Control Timing Diagram

Although 16 bits of data are clocked into the input latch, only 14 bits are transferred into the DAC latch. Therefore, 2 bits in the stream are don't cares since their value does not affect the DAC latch data. The bit positions are 2 don't cares followed by the 14-bit DAC data starting with the MSB.

The $\overline{\text{LDAC}}$ signal controls the transfer of data to the DAC latch. Normally, data is loaded to the DAC latch on the falling edge of $\overline{\text{LDAC}}$. However, if $\overline{\text{LDAC}}$ is held low, then serial data is loaded to the DAC latch on the sixteenth falling edge of TCLK. If $\overline{\text{LDAC}}$ goes low during the loading of serial data to the input latch, no DAC latch update takes place on the falling edge of $\overline{\text{LDAC}}$. If $\overline{\text{LDAC}}$ stays low until the serial transfer is completed, then the update takes place on the sixteenth falling edge of TCLK. If $\overline{\text{LDAC}}$ returns high before the serial data transfer is completed, no DAC latch update takes place.

AD7869 DYNAMIC SPECIFICATIONS

The AD7869 is specified and 100% tested for dynamic performance specifications as well as traditional dc specifications such as Integral and Differential Nonlinearity. These ac specifications are required for signal processing applications such as speech recognition, spectrum analysis, and high speed modems. These applications require information on the converter's effect on the spectral content of the input signal. Hence, the parameters for which the AD7869 is specified include SNR, harmonic distortion and peak harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal-to-noise ratio at the output of the ADC or DAC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency ($f_{SAMPLE}/2$) excluding dc. SNR is dependent upon the number of levels used in the quantization process; the more levels, the smaller the quantization noise. The theoretical signal-to-noise ratio for a sine wave input is given by

$$SNR = (6.02N + 1.76)\ dB \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

where N is the number of bits. Thus for an ideal 14-bit converter, SNR = 86 dB.

Effective Number of Bits

The formula given in Equation (1) relates the SNR to the number of bits. Rewriting the formula, as in Equation (2), it is possible to get a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR.

Harmonic Distortion

Harmonic Distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7869, total harmonic distortion (THD) is defined as:

$$THD = 20\ log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V1 is the rms amplitude of the fundamental and V2, V3, V4, V5 and V6 are the rms amplitudes of the second through to the sixth harmonic. The THD is also derived from the FFT plot of the ADC or DAC output spectrum.

ADC Testing

The output spectrum from the ADC is evaluated by applying a sine wave signal of very low distortion to the V_{IN} input while reading multiple conversion results. A Fast Fourier Transform (FFT) plot is generated from which the SNR data can be obtained. Figure 9 shows a typical 2048 point FFT plot of the AD7869AQ ADC with an input signal of 10 kHz and a sampling frequency of 60 kHz. The SNR obtained from this graph is 80 dB. It should be noted that the harmonics are taken into account when calculating the SNR.

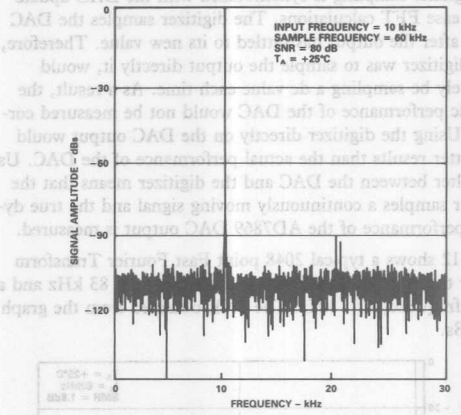


Figure 9. AD7869, ADC FFT Plot

Figure 10 shows a typical plot of effective number of bits versus frequency for an AD7869AQ with a sampling frequency of 60 kHz. The effective number of bits typically falls between 12.7 and 13.1 corresponding to SNR figures of 79 and 80.4 dB.

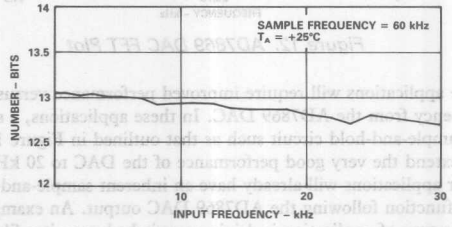


Figure 10. Effective Number of Bits vs. Frequency for the ADC

DAC Testing

A simplified diagram of the method used to test the dynamic performance specifications of the DAC is outlined in Figure 11. Data is loaded to the DAC under control of the microcontroller and associated logic. The output of the DAC is applied to a 9th order low pass filter whose cut-off frequency corresponds to the Nyquist limit. The output of the filter is in turn applied to a 16-bit accurate digitizer. This digitizes the signal and the microcontroller generates an FFT plot from which the dynamic performance of the DAC can be evaluated.

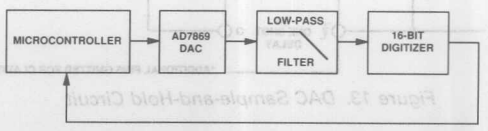


Figure 11. AD7869 DAC Dynamic Performance Test Circuit

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rate to ease FFT calculations. The digitizer samples the DAC output after the output has settled to its new value. Therefore, if the digitizer was to sample the output directly it, would effectively be sampling a dc value each time. As a result, the dynamic performance of the DAC would not be measured correctly. Using the digitizer directly on the DAC output would give better results than the actual performance of the DAC. Using a filter between the DAC and the digitizer means that the digitizer samples a continuously moving signal and the true dynamic performance of the AD7869 DAC output is measured.

Figure 12 shows a typical 2048 point Fast Fourier Transform plot for the AD7869 DAC with an update rate of 83 kHz and an output frequency of 1 kHz. The SNR obtained from the graph is 82 dBs.

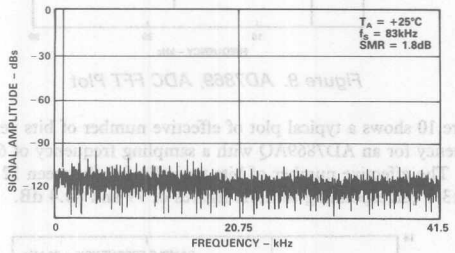


Figure 12. AD7869 DAC FFT Plot

Some applications will require improved performance versus frequency from the AD7869 DAC. In these applications, a simple sample-and-hold circuit such as that outlined in Figure 13 will extend the very good performance of the DAC to 20 kHz. Other applications will already have an inherent sample-and-hold function following the AD7869 DAC output. An example of this type of application is driving a switched capacitor filter where the updating of the DAC is synchronized with the switched capacitor filter. This inherent sample-and-hold function also extends the frequency range performance.

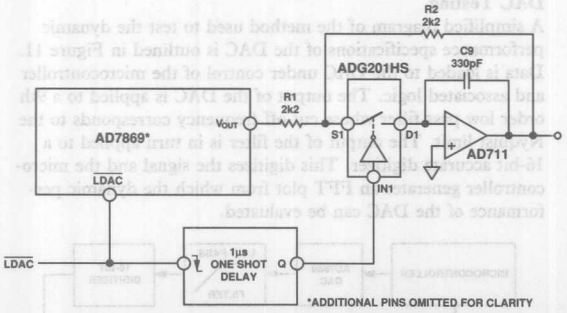


Figure 13. DAC Sample-and-Hold Circuit

The typical performance plots of Figures 14 and 15 show the AD7869 DAC performance over a wide range of input frequencies at an update rate of 83 kHz. The plot of Figure 14 is without a sample-and-hold on the DAC output while the plot of Figure 15 is generated with a sample-and-hold on the output.

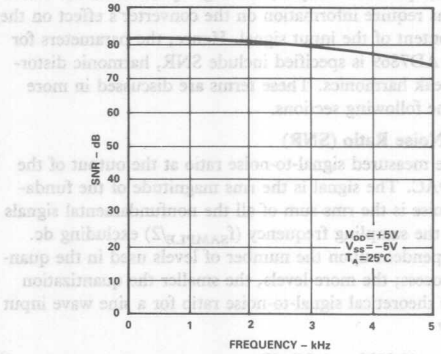


Figure 14. DAC Performance vs. Frequency (No Sample-and-Hold)

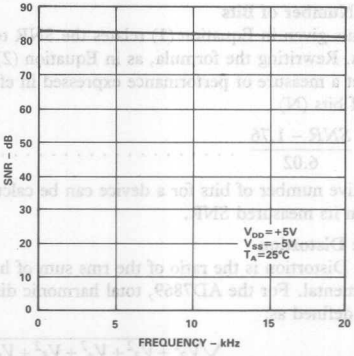


Figure 15. DAC Performance vs. Frequency (Sample-and-Hold)

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD7869 is via a serial bus that uses standard protocol compatible with DSP machines. The communication interface consists of separate transmit (DAC) and receive (ADC) sections whose operations can be either synchronous or asynchronous with respect to each other. Each section has a clock signal, a data signal and a frame or strobe pulse. Synchronous operation means that data is transmitted from the ADC and to the DAC at the same time. In this mode only one interface clock is needed, and this has to be the ADC clock out, so RCLK must be connected to TCLK. For asynchronous operation, DAC and ADC data transfers are independent of each other, the ADC provides the receive clock (RCLK) while the transmit clock (TCLK) may be provided by the processor or the ADC or some other external clock source.

Another option to be considered with serial interfacing is the use of a gated clock. A gated clock means that the device that is sending the data switches on the clock when data is ready to be transmitted and three states the clock output when transmission is complete. Only 16 clock pulses are transmitted with the first data bit getting latched into the receiving device on the first falling clock edge. Ideally, there is no need for frame pulses, however, the AD7869 DAC frame input ($\overline{TFS}$) has to be driven high between data transmissions. The easiest method is to use RFS to drive $\overline{TFS}$ and use only synchronous interfacing. This avoids the use of interconnects between the processor and AD7869 frame signals. Not all processors have a gated clock facility, Figure 16 shows an example with the DSP56000.

Table I below shows the number of interconnect lines between the processor and the AD7869 for the different interfacing options.

The AD7869 has the facility to use different clocks for transmitting and receiving data. This option, however, only exists on some processors and normally just one clock (ADC clock) is used for all communication with the AD7869. For simplicity, all the interface examples in this data sheet use synchronous interfacing and use the ADC clock (RCLK) as an input for the DAC clock (TCLK). For a better understanding of each of these interfaces, consult the relevant processor data sheet.

Configuration	Number of Interconnects	Signals
Synchronous	4	RCLK, DR, DT and $\overline{RFS}$ ($TCLK = RCLK$, $\overline{TFS} = \overline{RFS}$)
Asynchronous*	5 or 6	RCLK, DR, $\overline{RFS}$, DT, $\overline{TFS}$ ($TCLK = RCLK$ or μP serial CLK)
Synchronous Gated Clock	3	RCLK, DR and DT ($TCLK = RCLK$, $\overline{TFS} = \overline{RFS}$)

*5 LINES OF INTERCONNECT WHEN TCLK = RCLK
6 LINES OF INTERCONNECT WHEN TCLK = µP SERIAL CLK

Table I. Interconnect Lines for Different Interfacing Options

AD7869–DSP 56000 Interface

Figure 16 shows a typical interface between the AD7869 and DSP56000. The interface arrangement is synchronous with a gated clock requiring only three lines of interconnect. The DSP56000 internal serial control registers have to be configured for a 16-bit data word with valid data on the first falling clock edge. Conversion starts and DAC updating are controlled by an external timer. Data transfers, which occur during ADC conversions are between the processor receive and transmit shift registers and the AD7869's ADC and DAC. At the end of each 16-bit transfer the DSP56000 receives an internal interrupt indicating the transmit register is empty and the receive register is full.

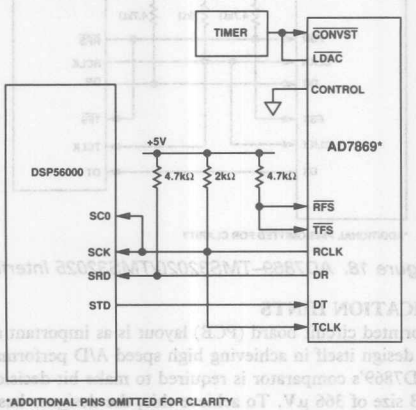


Figure 16. AD7869–DSP56000 Interface

AD7869–ADSP-2101/2102 Interface

An interface which is suitable for the ADSP-2101 or the ADSP-2102 is shown in Figure 17. The interface is configured for synchronous, continuous clock operation. The $\overline{LDAC}$ is tied low so the DAC gets updated on the sixteenth falling clock after $\overline{TFS}$ goes low. Alternatively, $\overline{LDAC}$ may be driven from a timer as shown in Figure 16. As with the previous interface the processor receives an interrupt after reading or writing to the AD7869 and updates its own internal registers in preparation for the next data transfer.

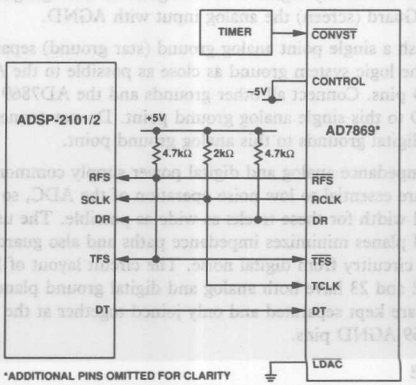


Figure 17. AD7869–ADSP-2101/ADSP-2102 Interface

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AD7869 – TMS32020 Interface

Figure 18 shows an interface which is suitable for the TMS32020/TMS320C25 processors. This interface is configured for synchronous, continuous clock operation. Note, the AD7869 will not interface correctly to these processors if the AD7869 is configured for a noncontinuous clock. Conversion starts and DAC updating are controlled by an external timer.

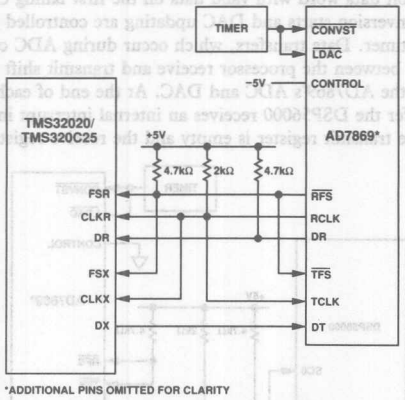


Figure 18. AD7869–TMS32020/TMS32025 Interface

APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the circuit design itself in achieving high speed A/D performance. The AD7869's comparator is required to make bit decisions on an LSB size of 366 μV. To achieve this, the designer has to be conscious of noise both in the ADC itself and in the preceding analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any ADC, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground as close as possible to the AD7869 AGND pins. Connect all other grounds and the AD7869 DGND to this single analog ground point. Do not connect any other digital grounds to this analog ground point.

Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise. The circuit layout of Figures 22 and 23 have both analog and digital ground planes which are kept separated and only joined together at the AD7869 AGND pins.

NOISE

Keep the input signal leads to V_{IN} and signal return leads from AGND as short as possible to minimize input noise coupling. In applications where this is not possible, use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

INPUT/OUTPUT BOARD

Figure 19 shows an analog I/O board based on the AD7869. The corresponding printed circuit (PC) board layout and silkscreen are shown in Figures 21 to 23.

The analog input to the AD7869 is buffered with an AD711 op amp. There is a component grid provided near the analog input on the PC board which may be used for an antialiasing filter for the ADC or a reconstruction filter for the DAC or any other conditioning circuitry. To facilitate this option, there are two wire links (labeled LK1 and LK2) required on the analog input and output tracks.

The board contains a SHA circuit which can be used on the output of the AD7869 DAC to extend the very good performance of the part over a wider frequency range. The increased performance from the SHA can be seen from Figures 14 and 15 of this data sheet. A wire link (labeled LK3) connects the board output to either the SHA output or directly to the AD7869 DAC output .

There are three $\overline{\text{LDAC}}$ link options on the board; $\overline{\text{LDAC}}$ can be driven from an external source independent of $\overline{\text{CONVST}}$, $\overline{\text{LDAC}}$ can be tied to $\overline{\text{CONVST}}$ or $\overline{\text{LDAC}}$ can be tied to GND. Choosing the latter option of tying $\overline{\text{LDAC}}$ to GND disables the SHA operation, and places the SHA permanently in the track mode.

Microprocessor connections to the board are made by a 9-way D-type connector. The pinout is shown in Figure 20. The ADC's digital outputs are buffered with 74HC4050s. These buffers provide a higher current output capability for high capacitance loads or cables. Normally, these buffers are not required as the AD7869 will be sitting on the same board as the processor.

POWER SUPPLY CONNECTIONS

The PC board requires two analog power supplies and one 5 V digital supply. Connections to the analog supply are made directly to the PC board as shown on the silkscreen in Figure 21. The connections are labeled V+ and V− and the range for both of these supplies is 12 V to 15 V. Connections to the 5 V digital supply are made through the D-type connector SKT6. The ± 5 V analog supply required by the AD7869 are generated from two voltage regulators on the V+ and V− supplies.

WIRE LINK OPTIONS

LK1, Analog Input Link

LK1 connects the analog input to a component grid or to a buffer amplifier which drives the ADC input.

LK2, Analog Output Link

LK2 connects the analog output to the component grid or to either the SHA or DAC output (see LK3).

LK3, SHA or DAC Select

The analog output may be taken directly from the DAC or from a SHA at the output of the DAC.

LK4, DAC Reference Selection

The DAC reference may be connected to either the ADC reference output (RO ADC) or to the DAC reference (RO DAC).

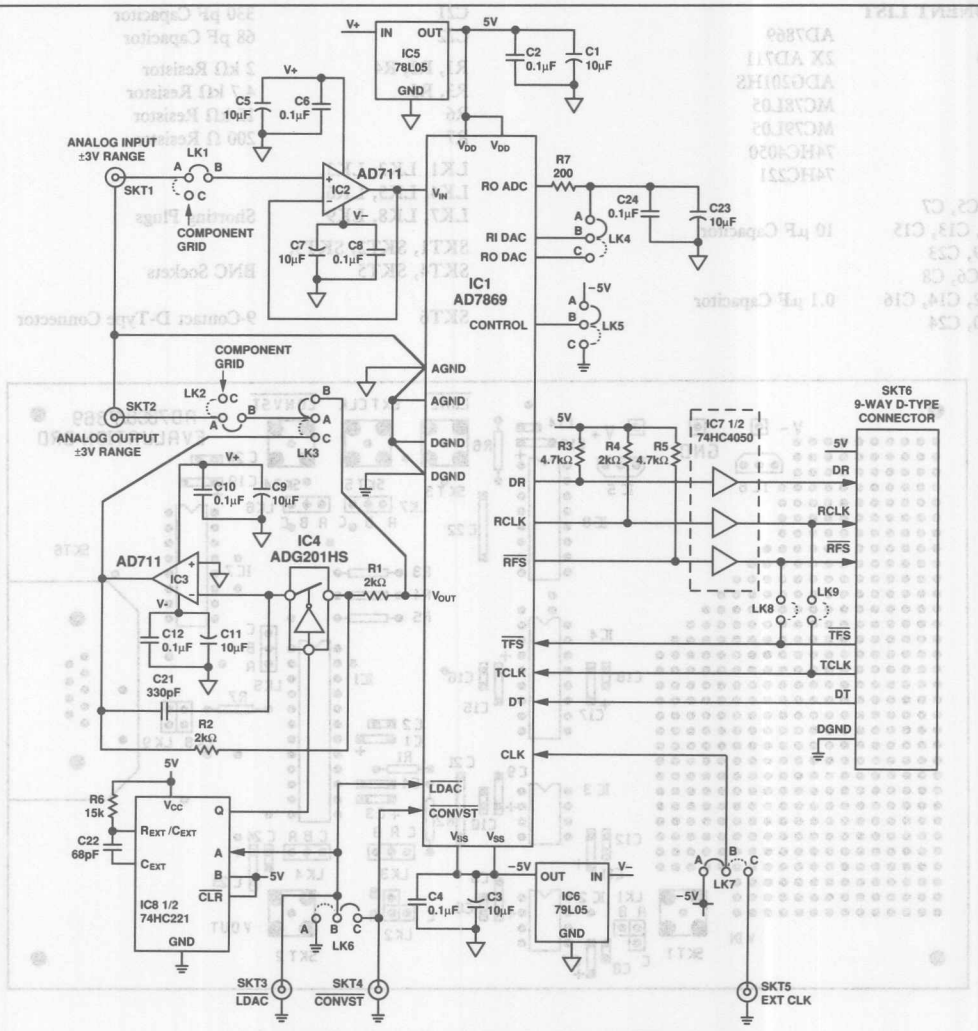


Figure 19. Input/Output Circuit Based on the AD7869

LK5, ADC Internal Clock Selection
This link configures the ADC for continuous or noncontinuous internal clock operation.

LK6, DAC Updating
The DAC, $\overline{\text{LDAC}}$ input may asserted independently of the ADC $\overline{\text{CONVST}}$ signal or it may be tied to $\overline{\text{CONVST}}$ or it may tied to GND.

LK7, ADC Clock Source
This link provides the option for the ADC to use its own internal clock oscillator or an external TTL compatible clock.

LK8 Frame Synchronous Option
LK8 provides the option of tying the ADC $\overline{\text{RFS}}$ output to the DAC $\overline{\text{TFS}}$ input.

LK9 Transmit/Receive Clock Option
LK9 provides the option to connect the ADC RCLK to the DAC TCLK.

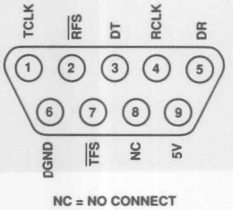


Figure 20. SKT6, D-Type Connector Pinout

COMPONENT LIST

IC1	AD7869
IC2, IC3	2X AD711
IC4,	ADG201HS
IC5,	MC78L05
IC6,	MC79L05
IC7,	74HC4050
IC8,	74HC221
C1, C3, C5, C7 C9, C11, C13, C15 C17, C19, C23	10 µF Capacitor
C2, C4, C6, C8 C10, C12, C14, C16 C18, C20, C24	0.1 µF Capacitor
C21	330 pF Capacitor
C22	68 pF Capacitor
R1, R2, R4	2 kΩ Resistor
R3, R5	4.7 kΩ Resistor
R6	15 kΩ Resistor
R7	200 Ω Resistor
LK1, LK2, LK3, LK4, LK5, LK6, LK7, LK8, LK9	Shorting Plugs
SKT1, SKT2, SKT3, SKT4, SKT5	BNC Sockets
SKT6	9-Contact D-Type Connector

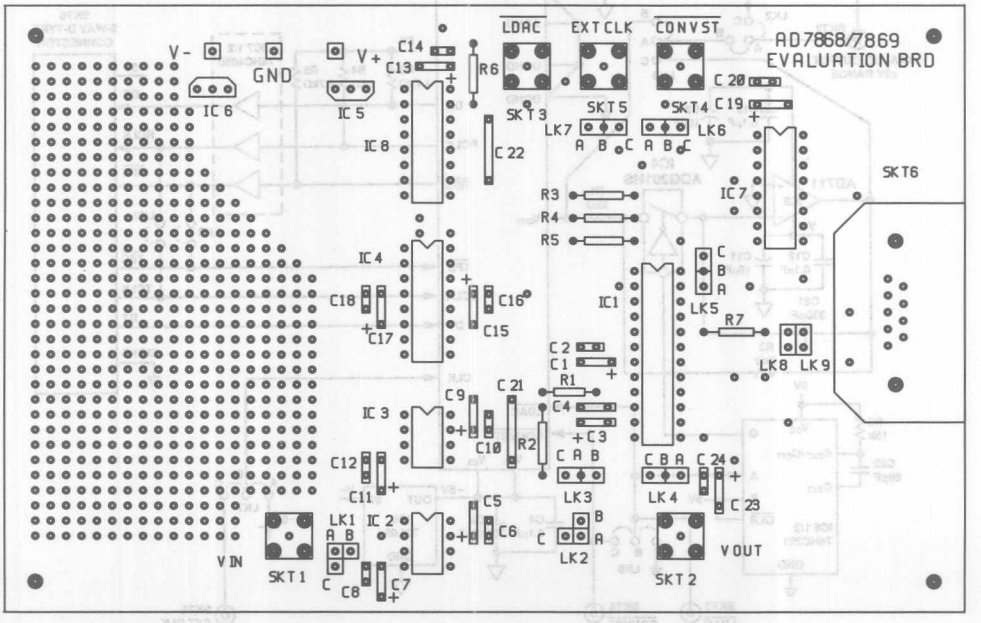


Figure 21. Silkscreen for the Circuit Diagram of Figure 19

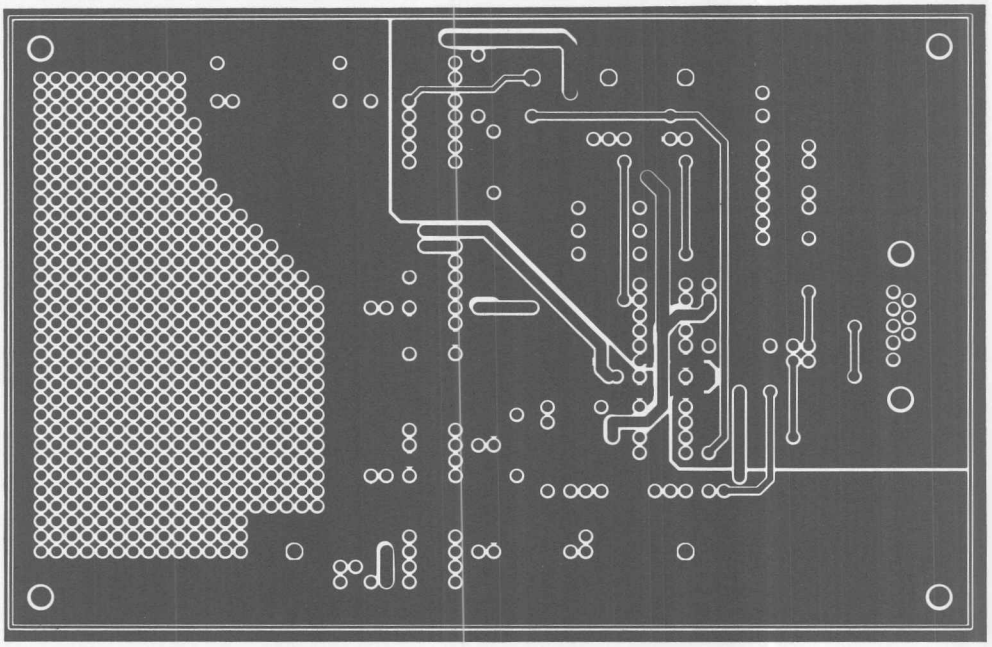


Figure 22. Component Side Layout for the Circuit Diagram of Figure 19

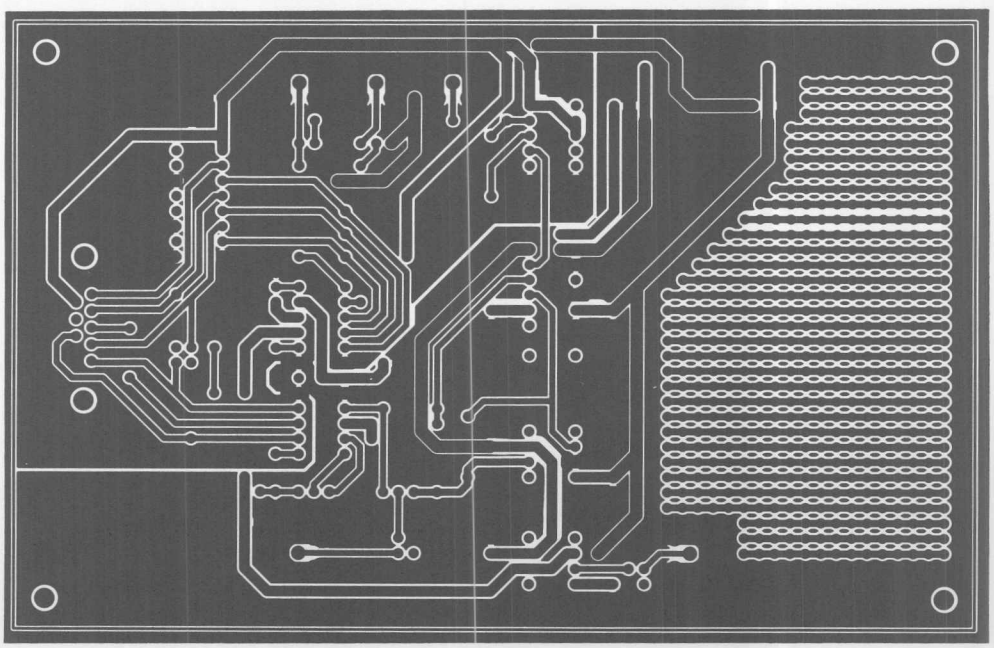
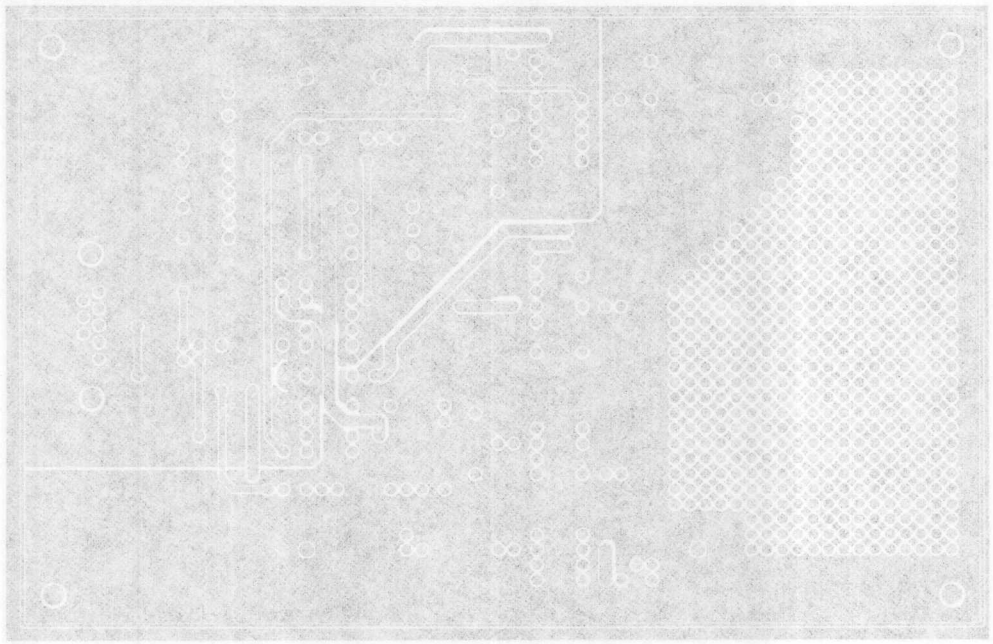
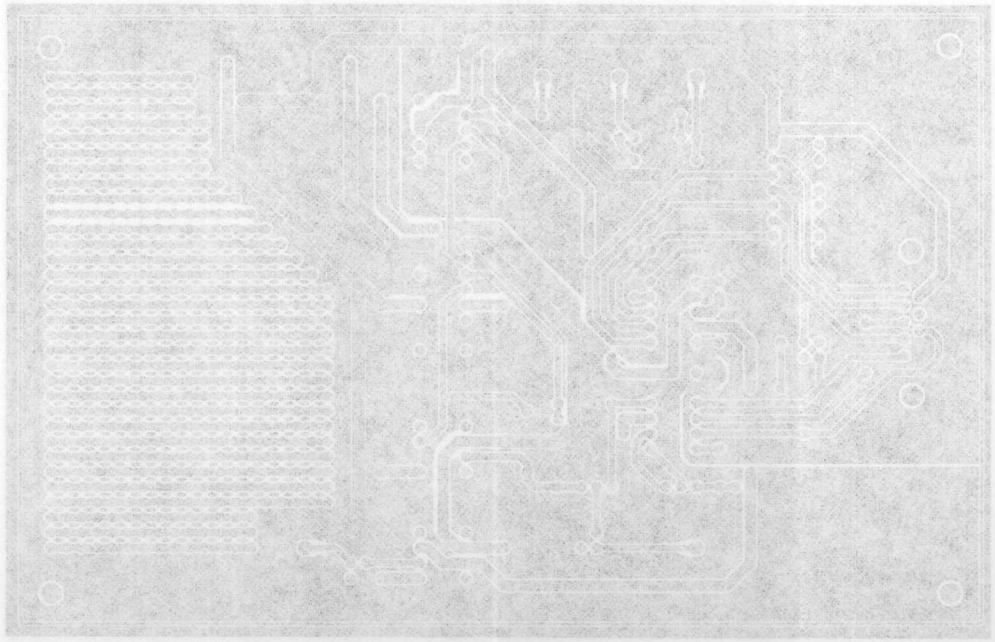


Figure 23. Solder Side Layout for the Circuit Diagram of Figure 19





Mixed-Signal Application Specific Integrated Circuits

Analog Devices offers a full spectrum of signal conditioning and conversion capabilities in mixed-signal application specific integrated circuits (ASICs). These chip-level systems can implement combined analog/digital designs with 10- to 14-bit accuracy and 12- to 20-bit resolution that formerly required board-level solutions. Combined with our general purpose DSPs from the ADSP-2100 and ADSP-21000 families, our ASICs can provide custom two-chip solutions to meet complex system requirements.

Analog Devices can incorporate most of the functions of its standard monolithic linear and converter parts in full-custom and semicustom ICs. Full-custom parts optimize performance and space requirements, while cell-based semicustom parts reduce development time and engineering expense. Development costs can be cut further by tailoring a predefined system-on-a-chip known as a Linear System Macro to your application.

Analog's experienced design engineers work with powerful computer-aided design tools to design and lay out your circuit. Design centers are currently in Massachusetts, England and Ireland.

Multiple locations for fabrication, assembly and testing ensure a ready supply of production parts. Products can be processed in our MIL-38510 certified facilities.

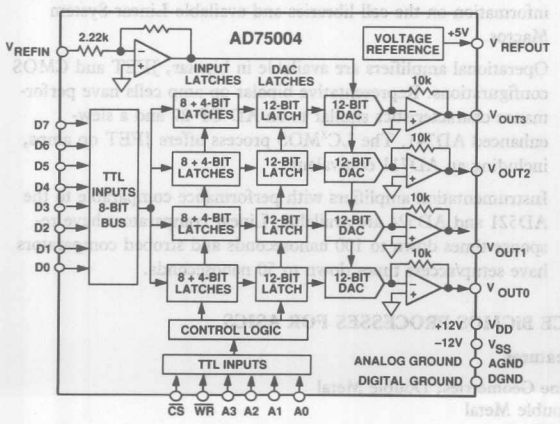
DESIGN EXAMPLES

Analog Devices has created a variety of customer-specific and function-specific ASIC parts. Described here are three Linear System Macros, a custom chipset and a semicustom chip.

AD75004 Quad DAC

This circuit contains four separate 12-bit D/A converters with amplifiers for voltage output and an on-board reference. Double-buffering latches interface with an 8-bit parallel bus and permit updating of all four channels individually or simultaneously. Outputs swing ±5 V, drive ±5 mA, and settle within 4 μs.

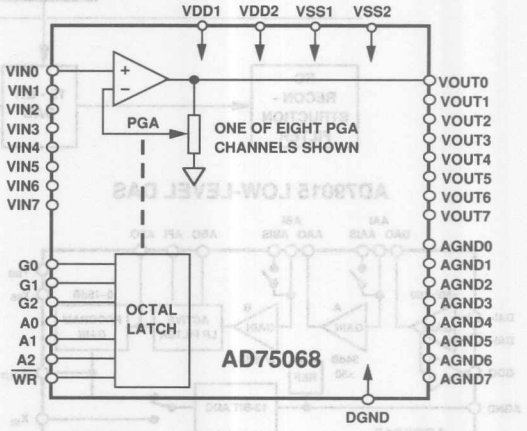
AD75004 QUAD DAC



AD75068 Octal Programmable Gain Amplifier

The AD75068 contains eight programmable gain amplifiers (PGAs). Each is complete, including switch/resistor network and gain programming latch, and requires no external components. Each channel may be independently programmed for gains from 1 to 128. A unique circuit design maintains constant 2 MHz bandwidth at all gains and offers very low phase shift; the PGAs also feature low input bias current (<4 pA).

AD75068 OCTAL PROGRAMMABLE GAIN AMPLIFIER



Derivative Circuits

The circuits outlined above can be modified to suit a specific customer's application. For example, the AD75004 quad DAC could be expanded to 6 channels, each of which may have separate reference inputs. The AD75068 could be configured to include filtering. These modifications, when based on standard library cells, can provide the fastest, most cost effective semicustom solution.

Modem Chipset

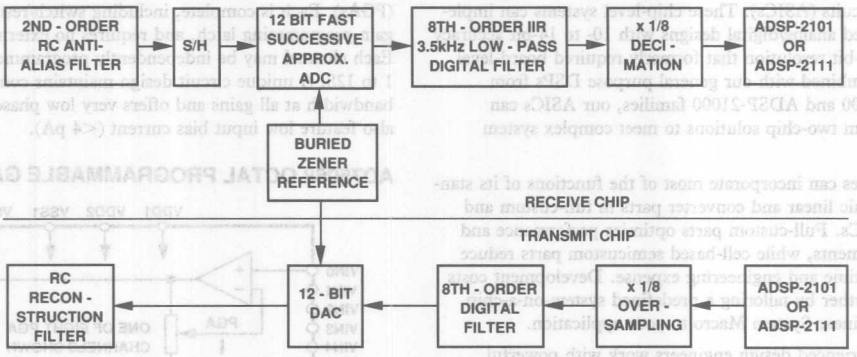
Library cells can be combined to form macro building blocks for high speed modems. This two-chip design concept filters and converts data to interface an Analog Devices digital signal processor with the analog circuitry of a 9600-baud modem. On one chip, the received signal passes through an antialiasing filter, sample-and-hold, 12-bit A/D converter, 8th-order digital filter and decimation. On the other chip, transmit data is 8 × oversampled, then goes to an 8th-order filter, a 12-bit DAC and an active reconstruction filter.

AD79015 Low Level DAS

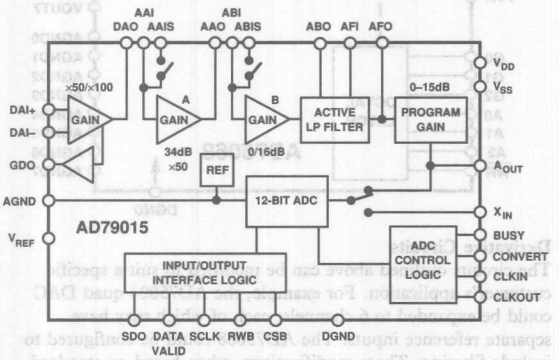
This circuit is a complete data acquisition system for low level signals (e.g., ECG and EEG) with a throughput of 10,000 samples per second. It provides high accuracy, high stability and functional completeness in a small 28-pin PLCC package. It includes a high performance instrumentation amp, low-pass and band-pass filters, and a 12-bit ADC with on-chip reference. It also includes a fast 8/12-bit serial port to interface to most microprocessor systems.

9

HIGH SPEED MODEM CHIPSET



AD79015 LOW-LEVEL DAS



HIGH PERFORMANCE PROCESSES

Analog Devices' semicustom and custom circuits are fabricated using the same high performance processes as our standard-product ICs. These mixed bipolar-CMOS processes include thin-film resistors which may be laser trimmed for precise matching and provide stable performance over a wide temperature range.

The ABCMOS, BiMOS II, and Linear Compatible CMOS (LC^2MOS) processes combine bipolar and CMOS devices on one chip. Functional density is an order of magnitude greater than previous mixed-signal processes; over 40,000 devices can be placed on a single chip. Bipolar transistors provide low noise, low offset input stages and moderate power output stages. The CMOS devices offer high input impedance, and make dense logic and analog switches for data converters, multiplexers and switched-capacitor filters. LC^2MOS also provides a JFET for very low noise amplifiers, and a low-noise buried-Zener reference. ABCMOS represents the next generation in a combined bipolar/CMOS process for mixed-signal applications.

The bipolar-CMOS processes operate on supply voltages ranging from single +5 V to split ±15V, with signal levels ranging from single-ended +3 V to ±10 V. These processes are ideally suited for applications in avionics, instrumentation, industrial automation, computers and peripherals, and telecommunications.

The following table summarizes the processes available for designing ASICs. Other processes in development will offer even higher speed, denser logic and higher integration of analog and digital functions.

CELL LIBRARIES

Cell libraries for the bipolar/CMOS processes are described below. These libraries are growing with the development of new processes, macrocells and cells. Many new catalog parts will also be available as cells. Your local sales office can give you current information on the cell libraries and available Linear System Macros.

Operational amplifiers are available in bipolar, JFET and CMOS configurations. Representative bipolar op amp cells have performance characteristics similar to an AD OP-27 and a slew-enhanced AD741. The LC^2MOS process offers JFET op amps, including an AD711 equivalent.

Instrumentation amplifiers with performance comparable to the AD521 and AD524 are available. Linear comparators have response times down to 100 nanoseconds and strobed comparators have setup/access times down to 50 nanoseconds.

ANALOG DEVICES HIGH PERFORMANCE BiCMOS PROCESSES FOR ASICS

Process	Power	Signal	Features
ABCMOS	+5 V to ±5 V	+3 V to ±3 V	Fine Geometries; Double Metal
BiMOS II	±5 V to ±12 V	±3 V to ±10 V	Double Metal
LC^2MOS	+5 V to ±15 V	+3 V to ±10 V	JFET, Zener
LC^2MOS 2	+5 V to ±5 V	+3 V to ±3 V	Fine Geometries; Poly-Poly Capacitors, JFET, Zener

Digital-to-analog converters range in resolution from 8 to 16 bits, and include cells similar to the AD667 and AD1856. Analog-to-digital converters vary from 8 to 16 bits in resolution, and include cells equivalent to the AD7871 and AD674.

Support cells include sample-and-hold amplifiers with performance comparable to the AD585, low-voltage bandgap references comparable to the AD584, and low-noise buried Zener references.

RC active filters and programmable switched-capacitor filters are available with specifications in these ranges:

Topology: all classical filter types
Frequency Range: 200 Hz to 20 kHz (switched-cap) or 100 Hz to 1 MHz (RC)
Number of Sections: up to 10th-order (switched-cap) or 4th-order (RC)
Signal/Noise and THD: >75 dB, compatible with 12-bit data acquisition.

Logic cells include gates, counters, registers, microsequencer, PLA, RAM and ROM. Interface cells include 8-bit and 16-bit parallel I/O ports as well as synchronous serial ports and UARTs.

COMPUTER-AIDED DESIGN TOOLS

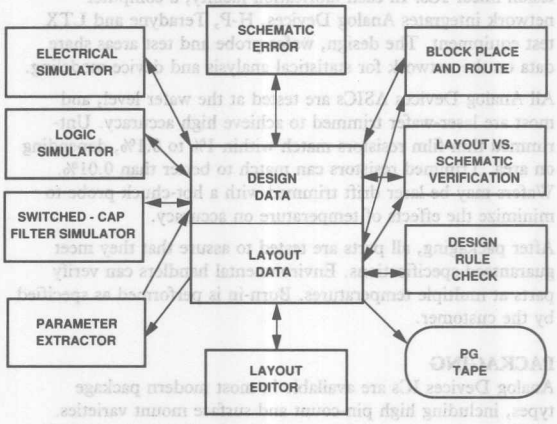
Designing a high performance mixed-signal IC is inherently more difficult than designing a gate array. The variety of analog and digital functions requires a cell-based approach. However, the use of powerful tools gives high confidence of functionality at first silicon through thorough simulation and layout verification. Complete computer-generated documentation of all schematics and analog and logic simulation waveforms permits thorough evaluation of Analog's design by your design staff before signoff for final layout and fabrication.

The overall work flow through the CAD environment follows. Key to meeting the special challenges of mixed analog/digital circuitry are the simulation and auto-layout tools, and the unification of design and layout information in a single database. Analog Devices has developed a suite of proprietary computer-aided design tools, called JANUS™, to address these issues and to implement turn-key designs.

The JANUS schematic editor offers numerous time-saving techniques and provides for specification of such data as wire widths, routing layers and routing priorities. It automatically generates a net list used by subsequent tools.

Analog uses several simulators, including electrical, logic and behavioral types. ADICE, a proprietary enhanced version of the SPICE electrical simulator, gives precision simulation of critical analog sections. It uses Newton-Raphson methods to iteratively solve nonlinear time-dependent simultaneous differential equations. It is efficient for circuits up to about 250 active devices and is used for the frequency domain or transient analysis of analog cells such as op amps, or sensitive digital cells such as dynamic RAM.

COMPUTER-AIDED DESIGN FLOW



Event-driven simulators handle larger circuits, with thousands of devices, and are typically used to simulate logic. The JANUS mixed-signal simulator combines an event-driven simulator with Newton-Raphson methods. It dynamically partitions the circuit to apply the faster event-driven techniques where possible, and the matrix methods where necessary. It also dynamically sizes the matrix and time steps to speed simulation further. The simulator can operate at the transistor level or use behavioral models, or both at the same time, allowing trade-offs between accuracy and speed.

For layout, the challenge is to increase automation while accommodating the layout sensitivity of analog circuitry. Device generators exist for the full range of active and passive devices available in the technology to automatically create a physical representation of the circuit schematic. This layout may be optimized through conventional interactive polygon-pushing.

The JANUS routing editor is driven by the connectivity of the schematics, but allows great freedom to manually control the routing of critical analog signal paths or power/ground lines while autorouting noncritical nets and spacing the layout to achieve automatic enforcement of layout rules. The JANUS routing editor uses up to three interconnect levels, and will automatically expand and compact placement as necessary to achieve 100% routing.

Finally, industry-standard layout verification tools assure conformance of the layout to both the schematic and design rules to give high confidence of functionality in first silicon. The CAD tool suite communicates via industry-standard stream formats to external databases and pattern generators.

JANUS is a trademark of Analog Devices, Inc.

TEST AND TRIM

Analog Devices has over 20 years of experience in testing complex circuits and manufactures commercial test systems for precision linear ICs. In each fabrication facility, a computer network integrates Analog Devices, H-P, Teradyne and LTX test equipment. The design, wafer probe and test areas share data on the network for statistical analysis and device modeling.

All Analog Devices ASICs are tested at the wafer level, and most are laser-wafer trimmed to achieve high accuracy. Untrimmed thin-film resistors match within 1% to 0.1%, depending on area. Trimmed resistors can match to better than 0.01%. Wafers may be laser drift trimmed with a hot-chuck probe to minimize the effects of temperature on accuracy.

After packaging, all parts are tested to assure that they meet guaranteed specifications. Environmental handlers can verify parts at multiple temperatures. Burn-in is performed as specified by the customer.

PACKAGING

Analog Devices ICs are available in most modern package types, including high pin-count and surface mount varieties. ASICs may be assembled in any of Analog Devices' standard packages, listed below. This list is constantly expanded and other packages may be used if they are suitable for high performance applications.

Available Packages

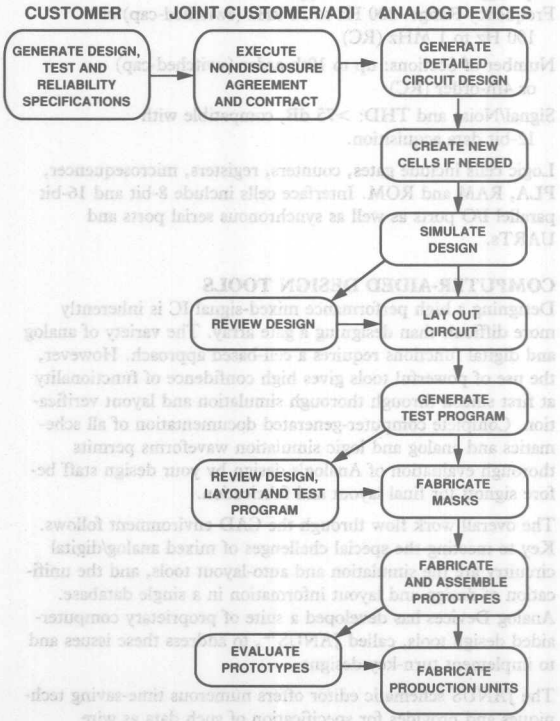
Pin Grid Array (PGA): 68 to 144 pins
Leaded Ceramic Chip Carrier (LDCC): 44 pins
Plastic Quad Flat Pack (PQFP): 44 to 132 pins
Plastic Leaded Chip Carrier (PLCC): 20 to 68 pins
Plastic Dual Inline Package (DIP): 14 to 64 pins
Side-Brazed DIP: 14 to 64 pins
Frit-Seal DIP (Cerdip): 14 to 40 pins
Small Outline (SO): 14 to 28 pins
Ceramic Quad Flat Pack (CQFP): 80 to 104 leads

PROGRAM RESPONSIBILITIES AND INTERFACES

The following figure shows the major phases in developing an ASIC and responsibilities during each phase. The overall development time depends on the complexity of the circuit and on how custom the design is.

Your Analog Devices Sales Engineer is your first interface for ASIC development. Your local sales office can provide further information on Analog Devices' custom/semicustom capabilities.

PROGRAM RESPONSIBILITIES AND INTERFACES



GENERAL DESCRIPTION

Analog Devices offers a broad line of modular ac/dc power supplies that provide both OEMs and designers a reliable, easy to use, low-cost solution to their power requirements. Models are available in PC mountable and chassis mountable designs with 5 volt to 15 volt (single, dual, triple) outputs and current ratings from 25 mA to 5 amps. Since these modular supplies are fully encapsulated, no trimming or external component selection is necessary; simply mount the unit, connect power and output leads, and you're on the air! Most Analog Devices' power supplies are available from stock in both large and small quantities with substantial discounts being applied to large quantity orders.

AC/DC POWER SUPPLY FEATURES

- Current Limit Short Circuit Protection
- PC Mounted and Chassis Mounted Versions
- Single (+5 V), Dual (±12 V, ±15 V), and Triple (±15 V/+5 V, ±15 V/+1 V to +15 V) Output Supplies
- Current Outputs:
  25 mA to 1000 mA for Dual and Triple Output Supplies
  250 mA to 5000 mA for Single Output Supplies
- Wide Input Voltage Range
- Low Output Ripple and Noise
- Excellent Line & Load Regulation Characteristics
- High Temperature Stability
- Free-Air Convection Cooling; No External Heat Sink Required

GENERAL SPECIFICATIONS

Power Requirements
- Input Voltage Range: 105 V ac to 125 V ac
- Frequency: 50 Hz to 250 Hz

Electrical Specifications
- Temperature Coefficient: 0.02%/°C
- Output Voltage Accuracy: ±2%, max
  See Specifications Table
- Breakdown Voltage: 500 V rms, min
- Isolation Resistance: 50 MΩ
- Short Circuit Protection: All ac/dc power supplies employ current limiting. They can withstand substantial overload including direct short. Prolonged operation should be avoided since excessive temperature rises will occur.

Environmental Requirements
- Operating Temperature Range: −25°C to +71°C
- Storage Temperature Range: −25°C to +85°C

SPECIFICATIONS – Typical @ +25°C and 115 V ac 60 Hz unless otherwise noted*

	Type	Model	Output Voltage Volts	Output Current mA	Line Reg. max %	Load Reg. max %	Output Voltage Error max	Ripple & Noise mV rms max	Dimensions Inches
PC Board Mounted	Dual Output	904	±15	±50	0.02	0.02	±200 mV −0 mV	0.5	3.5×2.5×0.875
		902	±15	±100	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×1.25
		902-2	±15	±100	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×0.875
		920	±15	±200	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×1.25
		925	±15	±350	0.02	0.02	±1%	0.5	3.5×2.5×1.62
		921	±12	±240	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×1.25
	Single Output	905	5	1000	0.02	0.05	±1%	1	3.5×2.5×1.25
		922	5	2000	0.02	0.05	±1%	1	3.5×2.5×1.62
		928	5	3000	0.05	0.10	±2%	5 (typ)	3.5×2.5×1.25
	Triple Output	923	±15	±100	0.02	0.02	±1%	0.5	3.5×2.5×1.25
			+5	500	0.02	0.05	±1%	0.5	
		927	±15	±150	0.02	0.02	±2%	0.5 (typ)	3.5×2.5×1.62
			+5	1000	0.02	0.10	±2%	1.0 (typ)	
Chassis Mounted	Dual Output	952	±15	±100	0.05	0.05	±2%	1	4.4×2.7×1.45
		970	±15	±200	0.05	0.05	±2%	1	4.4×2.7×1.45
		973	±15	±350	0.05	0.05	±2%	1	4.4×2.7×2.00
		975	±15	±500	0.05	0.05	±2%	1	4.4×2.7×2.00
	Single Output	955	5	1000	0.05	0.15	±2%	2	4.4×2.7×1.45
		976	5	3000	0.05	0.10	±2%	5 (typ)	4.75×2.7×1.45
		977	5	5000	0.05	0.10	±2%	5 (typ)	4.75×2.7×1.45
	Triple Output	974	±15	±150	0.02	0.02	±2%	0.5 (typ)	4.75×2.7×1.45
			+5	1000	0.02	0.10	±2%	1.0 (typ)	

*Consult Analog Devices Power Supplies Catalog for additional information.
Specifications subject to change without notice.

10

Power Supplies
Modular DC/DC Converters

GENERAL DESCRIPTION

Analog Devices' line of compact dc/dc converters offers system designers a means of supplying a reliable, easy to use, low cost solution to a variety of floating (analog and digital) power applications. These devices provide high accuracy, short circuit protected, regulated outputs with very low output noise and ripple characteristics.

Fourteen models are offered in five power levels of 1 watt, 1.8 watts, 4.5 watts, 6 watts and 12 watts. Input voltage versions include 5 volt, 12 volt, 24 volt and 28 volt with output ranges as follows: +5 volt, ±12 volts and ±15 volts at ±60 mA to 1000 mA output current capability.

Most models are high efficiency (typically over 60% at full load) and feature complete 6-sided continuous shielding for EMI/RFI protection. A π-type input filter is contained, in some models, which virtually eliminates the effects of reflected input ripple current. Most Analog Devices' dc/dc converters are available from stock in both large and small quantities with substantial discounts being applied to large quantity orders.

DC/DC POWER SUPPLY FEATURES

- Inaudible (>20 kHz) Converter Switching Frequency
- Continuous, Six-Sided EMI/RFI Shielding Except on 1 Watt and 1.8 Watt Models
- Output Short Circuit Protection (Either Output to Common)
- Automatic Restart After Short Condition Removed
- Automatic Starting with Reverse Current Injected into Outputs
- Low Output Ripple and Noise
- High Temperature Stability
- Free Air Convection Cooling
  No external heat sink or specification derating is required over the operating temperature range.

GENERAL SPECIFICATIONS FOR 1 W AND 1.8 W MODELS

Line Regulation – Full Range: ±0.3% (±1% max, 949)
Load Regulation – No Load to Full Load: ±0.4% (±0.5% max, 949)
Output Noise and Ripple: 20 mV p-p (with 15 µF tantalum capacitor across each output) 2 mV rms max, 949)
Breakdown Voltage: 300 V dc min (500 V dc min, 949)
Input Filter Type: π
Operating Temperature Range: −25°C to +71°C
Storage Temperature Range: −40°C to +125°C (+100°C, 949)
Fusing: If input fusing is desired, we recommend the use of a slow blow type fuse that is rated at 150%–200% of the dc/dc converter's full load input current.

GENERAL SPECIFICATIONS FOR 4.5 W, 6 W AND 12 W MODELS

Line Regulation – Full Range: ±0.07% max (±0.02% max, 951, 960 Series) (±0.1% max, 943)
Load Regulation – No Load to Full Load: ±0.07% max (±0.02% max, 951, 960 Series) (±0.1% max, 943)
Output Noise and Ripple: 1 mV rms max
Breakdown Voltage: 500 V dc min
Input Filter Type: π
Operating Temperature Range: −25°C to +71°C
Storage Temperature Range: −40°C to +125°C
Fusing: If input fusing is desired, we recommend the use of a slow blow type fuse that is rated at 150%–200% of the dc/dc converter's full load input current.

SPECIFICATIONS – Typical @ +25°C at nominal input voltage unless otherwise noted*

Model	Output Voltage Volts	Output Current mA	Input Voltage Volts	Input[1] Voltage Range Volts	Input Current Full Load	Output Voltage Error max	Temperature Coefficient /°C max	Efficiency Full Load min	Dimensions Inches
943	5	1000	5	4.75/5.25	1.52A	±1%	±0.02%	62%	2.0×2.0×0.38
958	5	100	5	4.5/5.5	200 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
941	±12	±150	5	4.75/5.25	1.17A	±1%	±0.01%	58%	2.0×2.0×0.38
960	±12	±40	5	4.5/5.5	384 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
962	±15	±33	5	4.5/5.5	396 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
964	±15	±33	12	10.8/13.2	165 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
965	±15	±190	5	4.65/5.5	1.7 A	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
966	±15	±190	12	11.2/13.2	710 mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
967	±15	±190	24	22.3/26.4	350 mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
949	±15	±60**	5	4.65/5.5	0.6 A	±2%	±0.03%	58%	2.0×1.0×0.375
940	±15	±150	5	4.75/5.25	1.35 A	±1%	±0.01%	62%	2.0×2.0×0.38
953	±15	±150	12	11/13	0.6 A	±0.5%	±0.01%	62%	2.0×2.0×0.38
945	±15	±150	28	23/31	250 mA	±0.5%	±0.01%	61%	2.0×2.0×0.38
951	±15	±410	5	4.65/5.5	3.7 A	±0.5%	±0.01%	62%	3.5×2.5×0.88

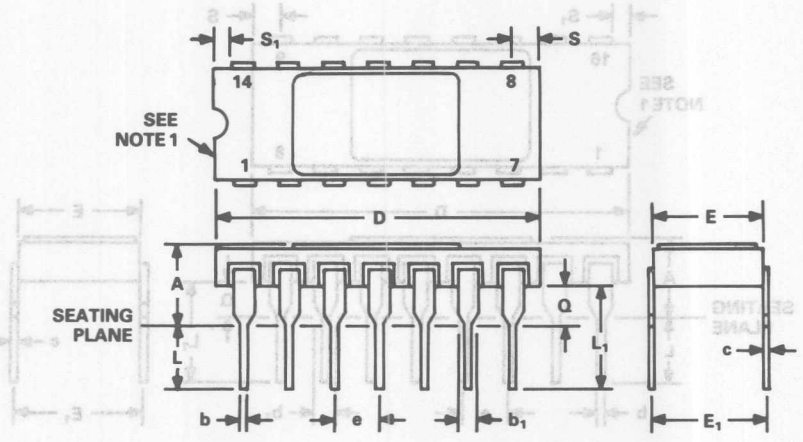
NOTES
[1]Models 940 and 941 will deliver up to 120 mA output current (and Model 943 will deliver up to 600 mA) over an input voltage range of 4.65 V dc and 5.5 V dc.
*Consult Analog Devices Power Supplies Catalog for additional information.
**Single-ended or unbalanced operation is permissible such that total output current load does not exceed a total of 120 mA.
Specifications subject to change without notice.

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ADI Letter Designator	PMI Letter Designator	Package Description	MIL-M38510 Applicable Configuration	Page
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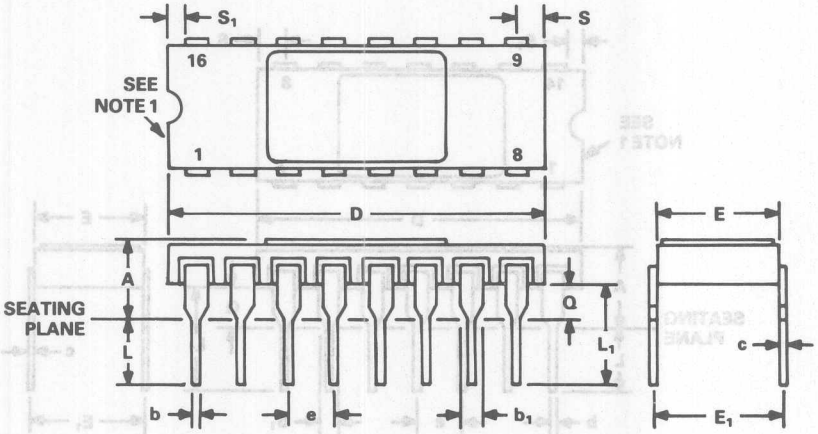
D-14
14-Lead Side Brazed Ceramic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2,6
c	0.008	0.015	0.20	0.38	6
D		0.785		19.94	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Twelve spaces.

D-16
16-Lead Side Brazed Ceramic DIP

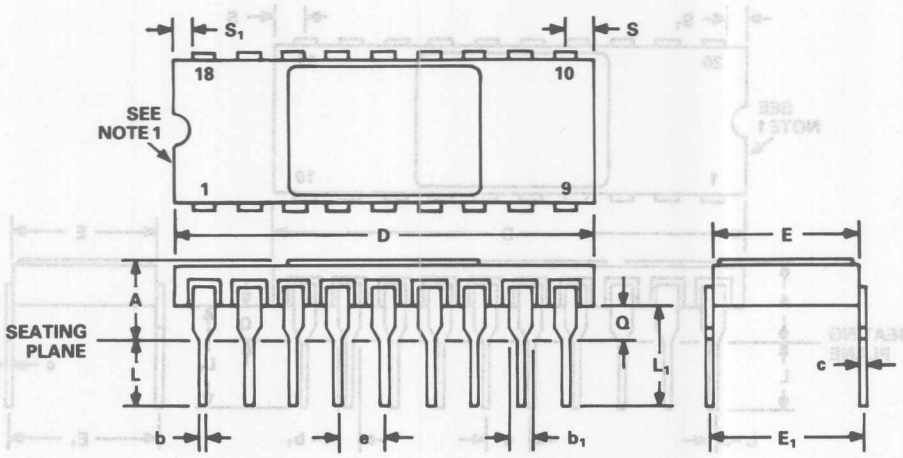


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		0.840		21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Fourteen spaces.

D-18
18-Lead Side Brazed Ceramic DIP

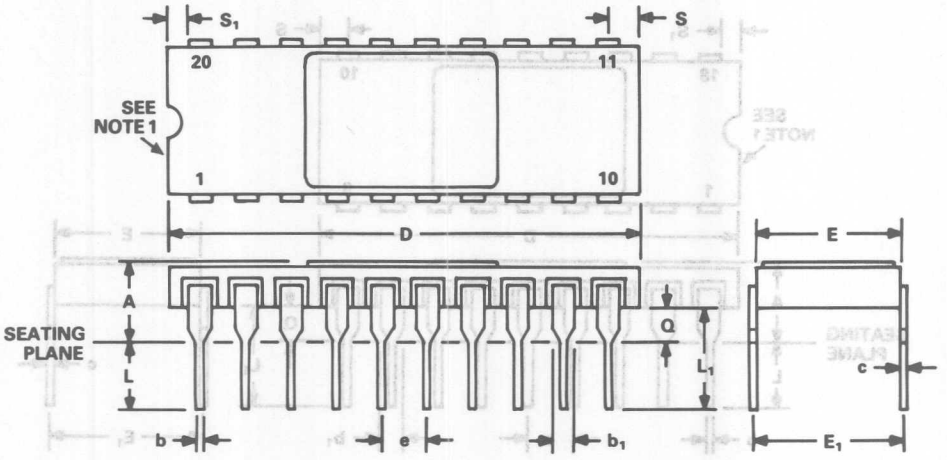


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		0.960		24.38	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Sixteen spaces.

D-20
20-Lead Side Brazed Ceramic DIP

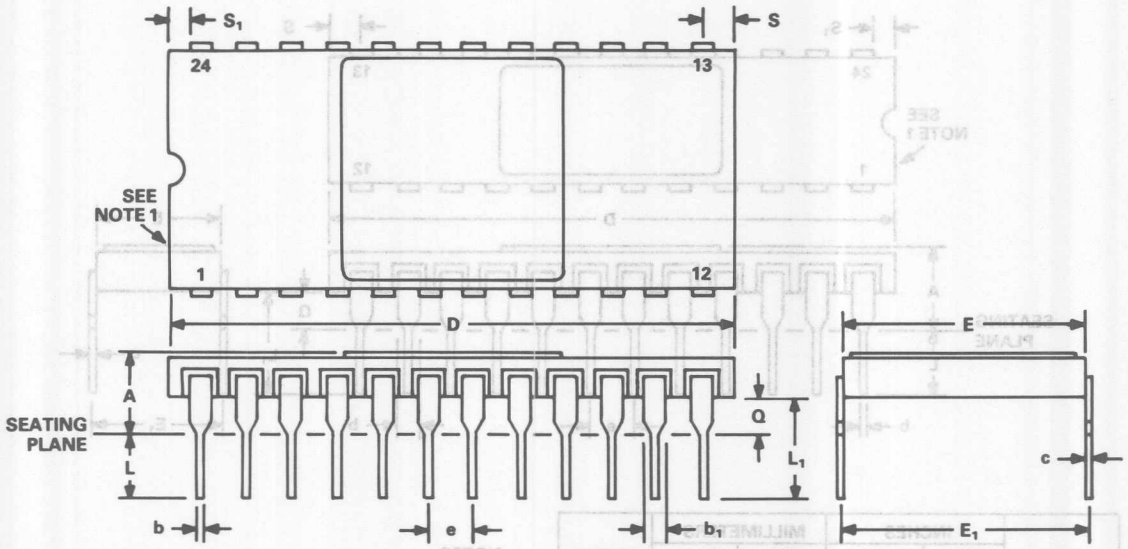


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		1.060		26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Eighteen spaces.

D-24
24-Lead Side Brazed Ceramic DIP



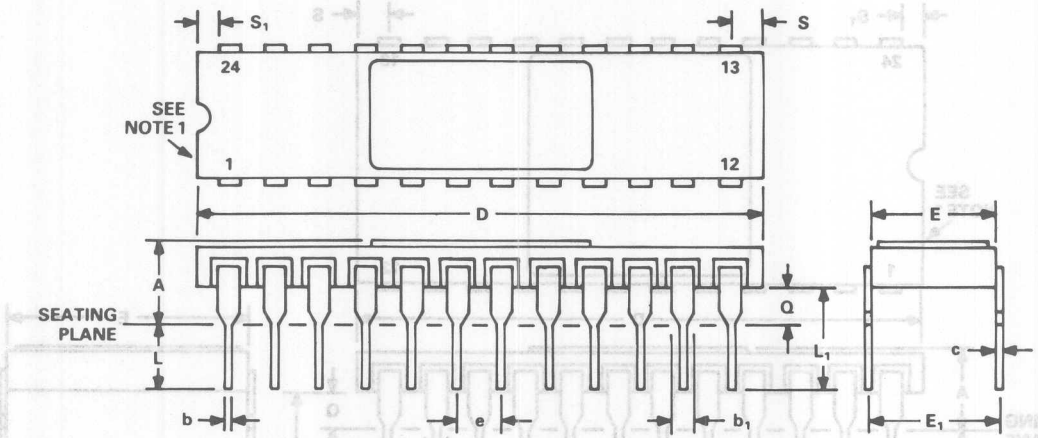
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2,6
c	0.008	0.015	0.20	0.38	6
D		1.290		32.77	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	
e	0.090	0.110	2.29	2.79	7
L	0.120	0.200	3.05	5.08	
L_1	0.150		3.81		
Q	0.015	0.075	0.38	1.91	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Twenty-two spaces.

11

D-24A

24-Lead Side Brazed Ceramic DIP (Single Width)



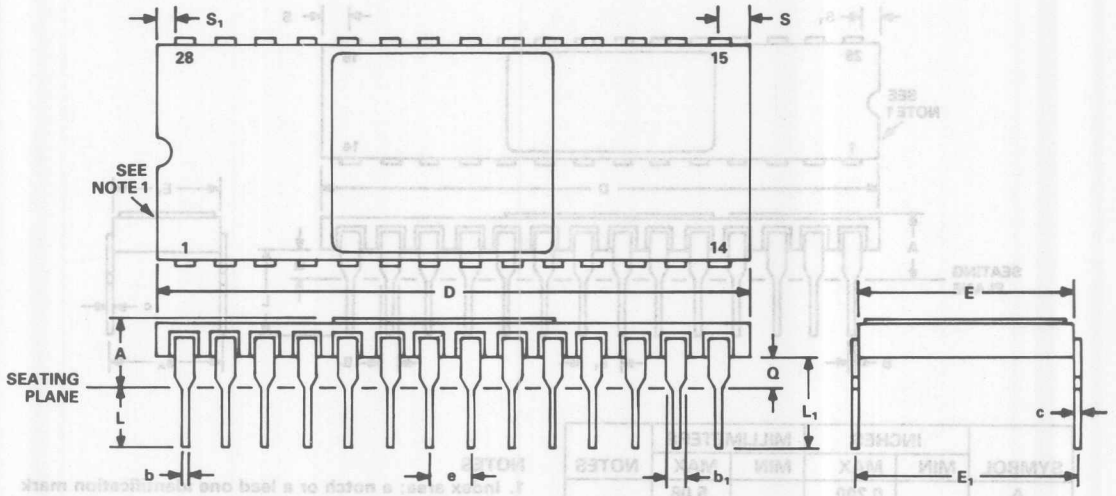
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2,6
c	0.008	0.015	0.20	0.38	6
D		1.280		32.51	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Twenty-two spaces.

D-28

28-Lead Side Brazed Ceramic DIP



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.225		5.72	
b	0.014	0.026	0.36	0.66	6
b_1	0.030	0.070	0.76	1.78	2,6
c	0.008	0.018	0.20	0.46	6
D		1.490		37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.100		2.54	5
S_1	0.005		0.13		5

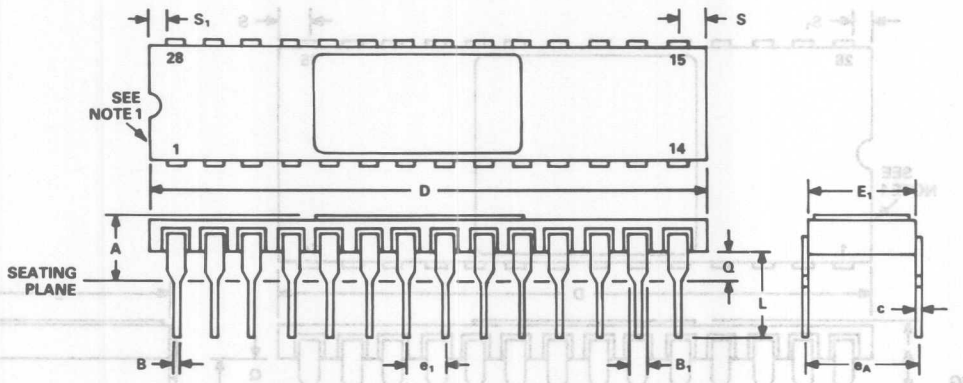
NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Twenty-six spaces.

11

D-28A

28-Lead Side Brazed Ceramic DIP (Single Width)

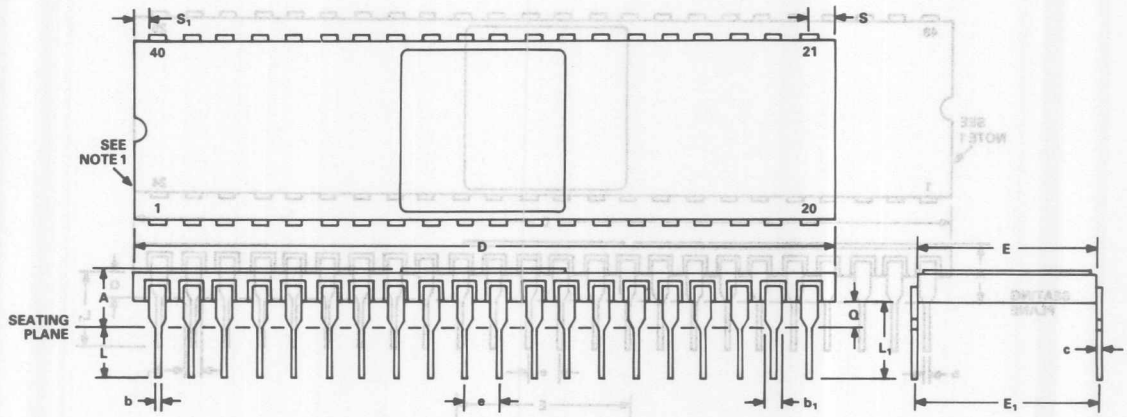


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		1.480		37.59	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003″ (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Twenty-six spaces.

D-40
40-Lead Side Brazed Ceramic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		2.096		53.24	4
E	0.590	0.620	12.95	15.75	4
E_1	0.520	0.630	13.21	16.00	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

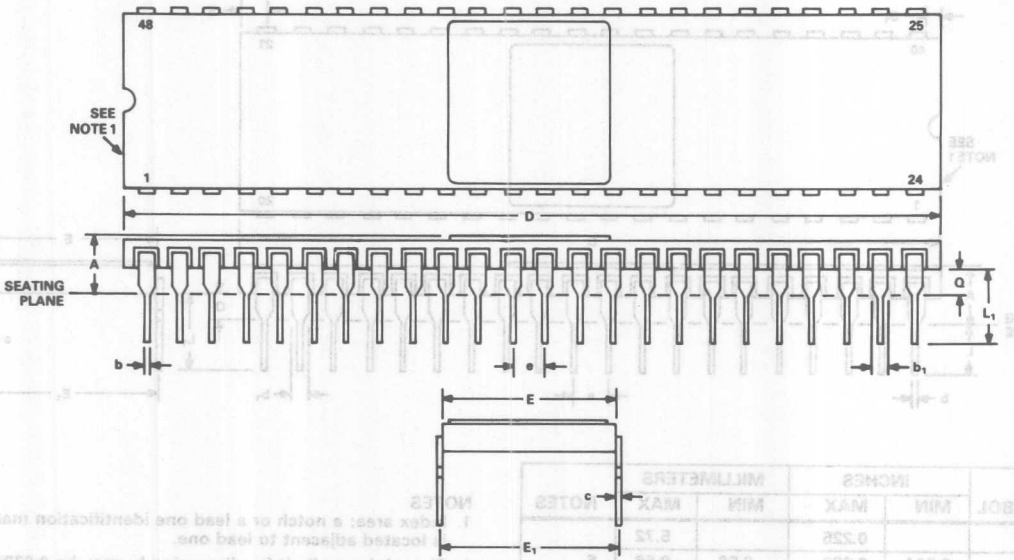
NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Thirty-eight spaces.

11

D-48

48-Lead Side Brazed Ceramic DIP



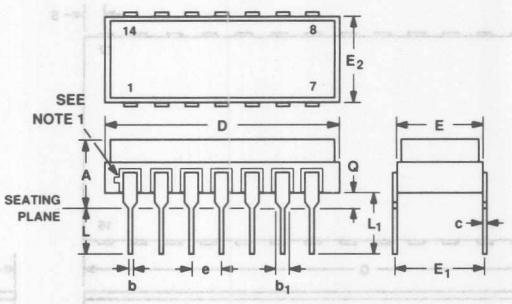
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D	2.376	2.424	60.351	61.569	4
E	0.59	0.62	12.95	15.75	4
E_1	0.52	0.63	13.21	16.00	
e	0.090	0.110	2.29	2.79	7
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Forty-six spaces.

DH-14D

14-Lead Side Brazed Ceramic DIP for Hybrid



	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.175	0.200	4.45	5.08	
b	0.016	0.020	0.41	0.51	
b_1	0.035	0.048	0.89	1.22	
c	0.009	0.012	0.23	0.30	
D	0.780	0.800	19.81	20.32	
E	0.270	0.330	6.86	8.38	
E_1	0.290	0.310	7.37	7.87	3
E_2		0.298		7.57	
e	0.095	0.105	2.41	2.67	4
L	0.145		3.68		
L_1	0.180		4.57		
Q	0.015	0.035	0.38	0.89	2

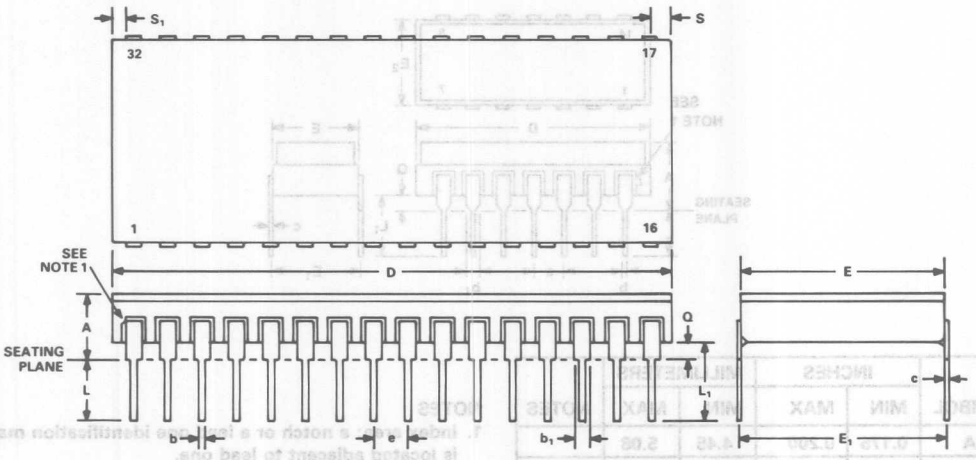
NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Dimension Q shall be measured from the seating plane to the base plane.
3. E_1 shall be measured at the centerline of the leads.
4. Twelve spaces.

11

DH-32B

32-Lead Side Brazed (Large Cavity)



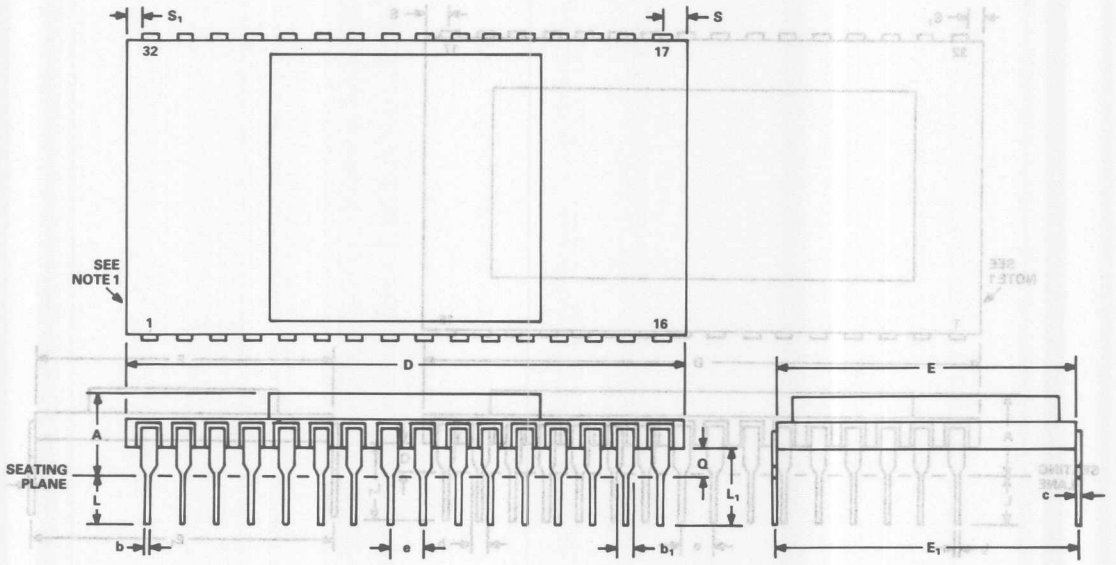
	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A		0.230		5.84	
b	0.016	0.020	0.41	0.51	
b_1	0.045	0.055	1.14	1.40	
c	0.009	0.012	0.23	0.30	
D	1.584	1.640	40.23	41.66	
E	0.580	0.605	14.73	15.37	
E_1	0.590	0.610	14.99	15.49	5
e	0.100 BSC		2.54 BSC		3, 6
L	0.120		3.05		
L_1	0.180		4.57		
Q	0.040	0.060	1.02	1.52	2
S		0.080		2.03	4
S_1	0.005		0.13		4

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Dimension Q shall be measured from the seating plane to the base plane.
3. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
4. Applies to all four corners.
5. E_1 shall be measured at the centerline of the leads.
6. Thirty spaces.

DH-32C

32-Lead Side Brazed Ceramic DIP for Hybrid (Small Cavity)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.280		7.11	
b	0.016	0.020	0.41	0.51	
b_1	0.035	0.055	0.89	1.40	
c	0.009	0.012	0.23	0.30	
D		1.620		41.15	
E	0.870	0.910	22.10	23.11	
E_1	0.890	0.930	22.61	23.62	5
e	0.100 BSC		2.54 BSC		3, 6
L	0.120		3.05		
L_1	0.180		4.57		
Q	0.040	0.060	1.02	1.52	2
S		0.098		2.49	4
S_1	0.005		0.13		4

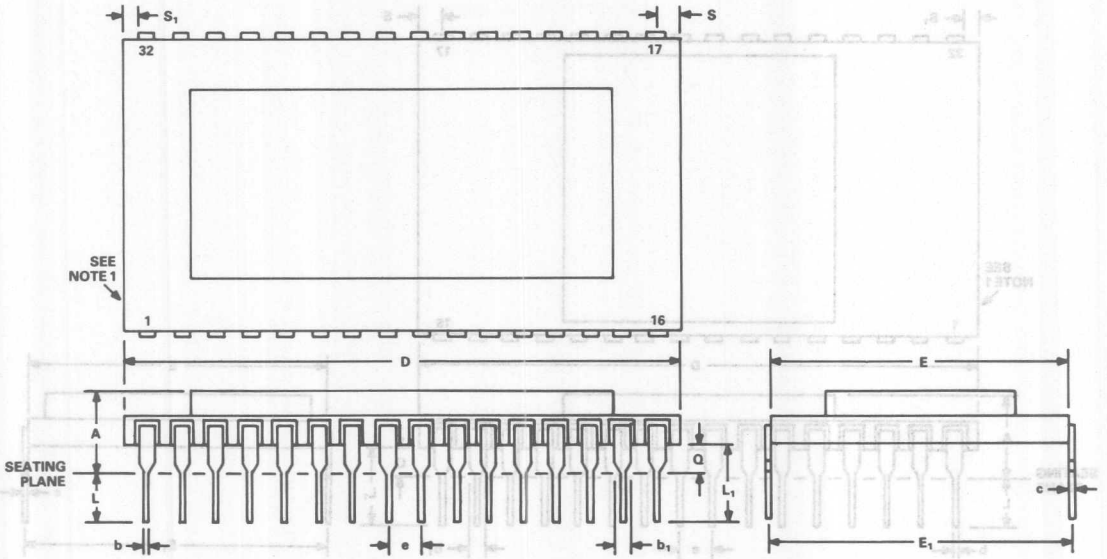
NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Dimension Q shall be measured from the seating plane to the base plane.
3. The basic pin spacing is 0.100″ (2.54 mm) between centerlines.
4. Applies to all four corners.
5. E_1 shall be measured at the centerline of the leads.
6. Thirty spaces.

11

DH-32D

32-Lead Side Brazed Ceramic DIP for Hybrid (Medium Cavity)



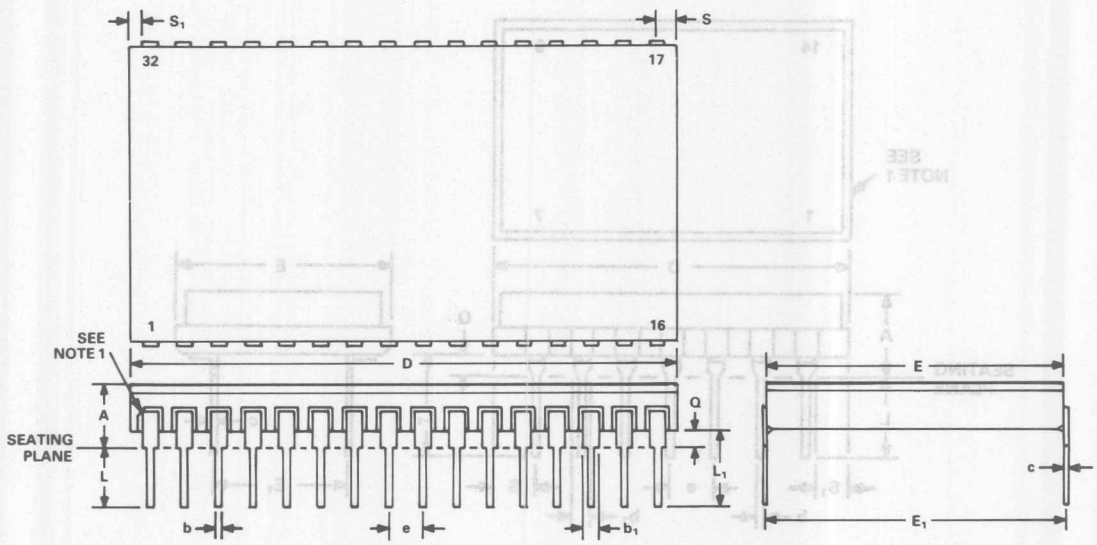
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.280		7.11	
b	0.016	0.020	0.41	0.51	
b_1	0.035	0.055	0.89	1.40	2
c	0.009	0.012	0.23	0.30	
D		1.616		41.05	
E	0.870	0.910	22.10	23.11	
E_1	0.890	0.930	22.61	23.62	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.120		3.05		
L_1	0.180		4.57		
Q	0.040	0.060	1.02	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100″ (2.54 mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Thirty spaces.

DH-32F

32-Lead Side Brazed Ceramic DIP (Large Cavity)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.230		5.84	
b	0.016	0.020	0.41	0.51	
b_1	0.045	0.055	1.14	1.40	2
c	0.009	0.012	0.23	0.30	
D	1.584	1.640	40.23	41.66	
E	0.880	0.905	22.35	22.99	
E_1	0.890	0.910	22.61	23.11	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.120		3.05		
L_1	0.180		4.57		
Q	0.040	0.060	1.02	1.52	3
S		0.080		2.09	5
S_1	0.005		0.13		5

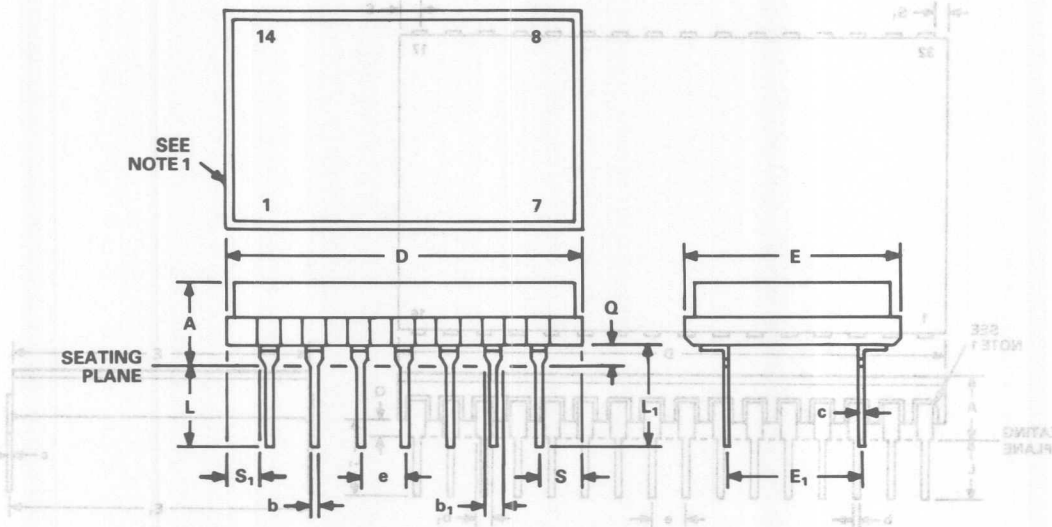
NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100″ (2.54 mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Thirty spaces.

11

DH-14A

14-Lead Bottom Brazed Ceramic Platform



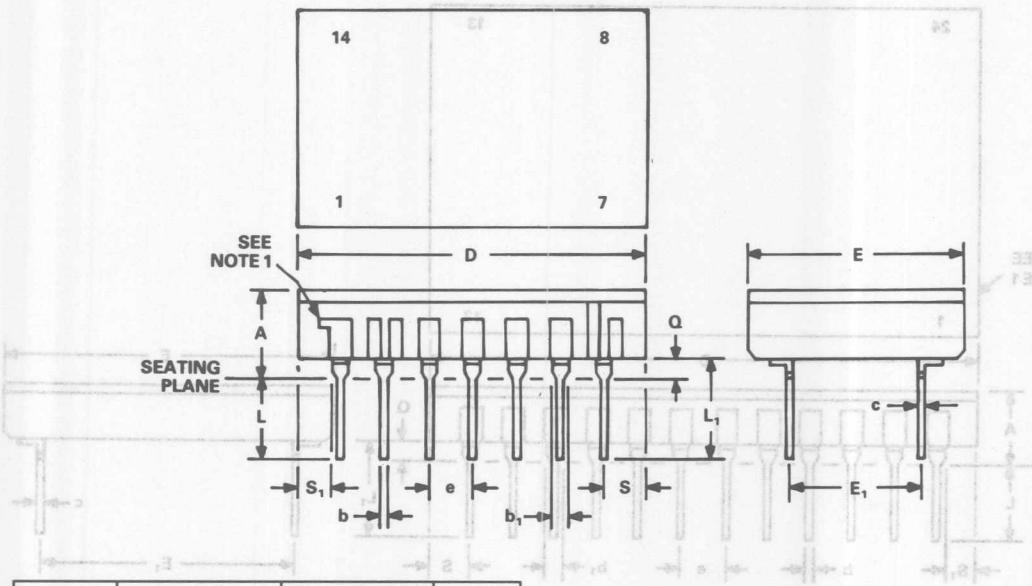
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	
c	0.008	0.015	0.20	0.38	
D		0.805		20.45	
E	0.480	0.505	12.19	12.83	
E_1	0.290	0.320	7.37	8.13	5
e	0.100 BSC		2.54 BSC		3, 6
L	0.145		3.68		
L_1	0.180		4.57		
Q	0.015	0.035	0.38	0.89	2
S		0.098		2.49	4
S_1	0.005		0.13		4

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Dimension Q shall be measured from the seating plane to the base plane.
3. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
4. Applies to all four corners.
5. E_1 shall be measured at the centerline of the leads.
6. Twelve spaces.

DH-14C

14-Lead Bottom Brazed Ceramic DIP

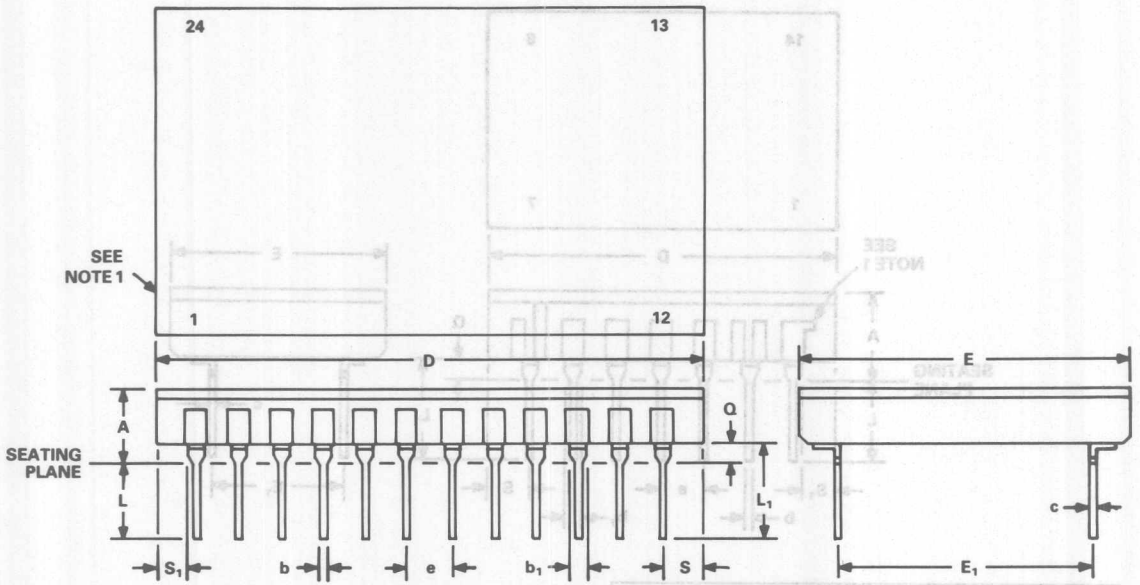


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.140	0.200	3.56	5.08	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	
D	0.770	0.810	19.56	20.57	
E	0.480	0.510	12.19	12.95	
E_1	0.295	0.305	7.49	7.75	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.145		3.68		
L_1	0.180		4.57		
Q	0.015	0.035	0.38	0.89	3
S		0.137		3.48	5
S_1	0.060		1.52		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Twelve spaces.

DH-24B
24-Lead Bottom Brazed Ceramic DIP



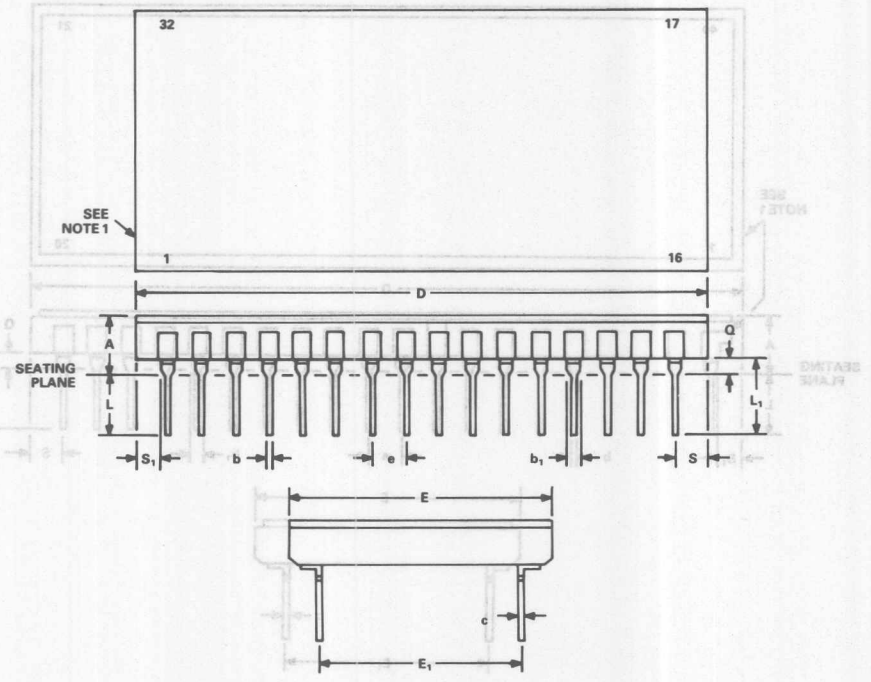
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.290		7.37	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	
D		1.320		33.53	
E	0.770	0.810	19.56	20.57	
E_1	0.580	0.620	14.73	15.75	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.145		3.68		
L_1	0.180		4.57		
Q	0.015	0.035	0.38	0.89	3
S		0.105		2.67	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100″ (2.54 mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Twenty-two spaces.

DH-32E

32-Lead Bottom Brazed Ceramic DIP



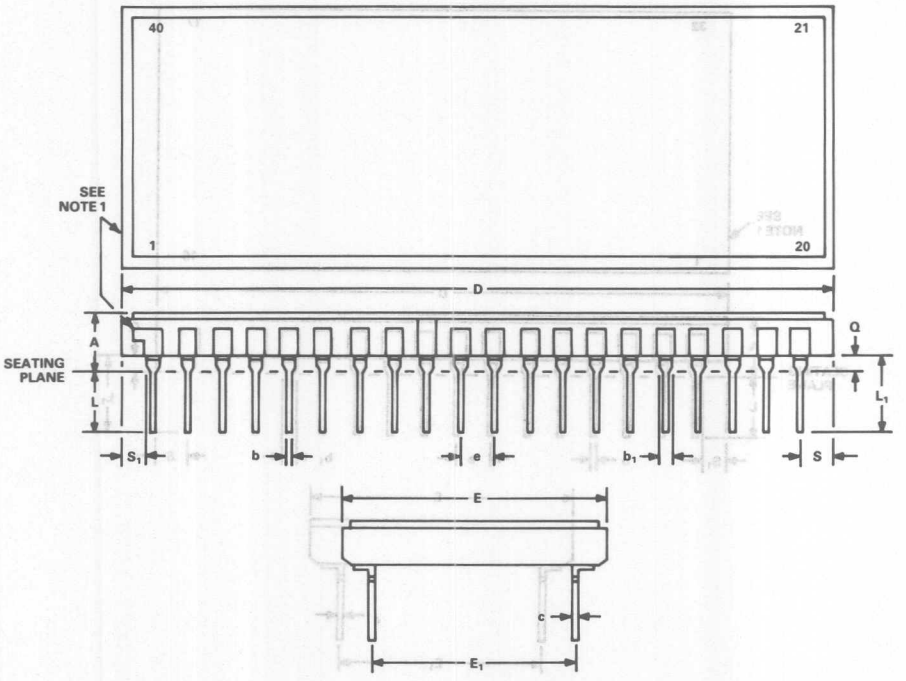
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	
D		1.750		44.45	
E	1.075	1.105	27.31	28.07	
E_1	0.890	0.910	22.61	23.11	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.145		3.68		
L_1	0.180		4.57		
Q	0.015	0.035	0.38	0.89	3
S		0.120		3.05	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100″ (2.54 mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Thirty spaces.

DH-40A

40-Lead Bottom Brazed Ceramic DIP



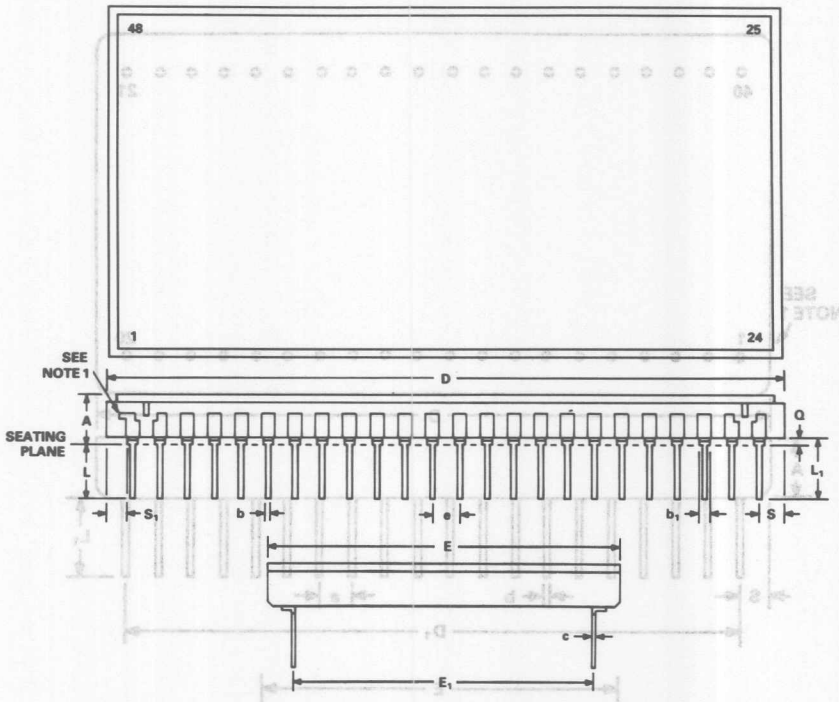
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.050	0.76	1.27	2
c	0.008	0.015	0.20	0.38	
D		2.120		53.85	
E	0.770	0.810	19.56	20.57	
E_1	0.580	0.620	14.73	15.75	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.145		3.68		
L_1	0.180		4.57		
Q	0.015	0.035	0.38	0.89	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of all the leads.
7. Thirty-eight spaces.

DH-48A

48-Lead Bottom Brazed Ceramic DIP

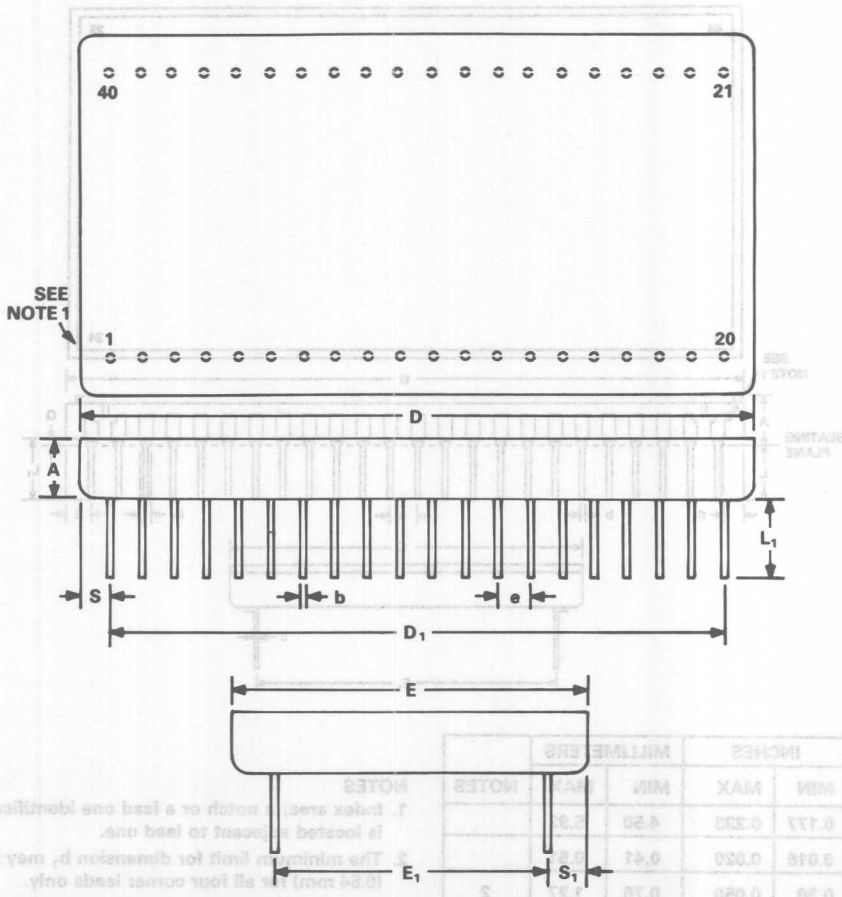


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.177	0.233	4.50	5.92	
b	0.016	0.020	0.41	0.51	
b_1	0.30	0.050	0.76	1.27	2
c	0.009	0.012	0.23	0.30	
D	2.450	2.500	62.23	63.50	
E	1.287	1.313	32.69	33.35	
E_1	0.990	1.010	25.15	25.65	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.145	0.200	3.68	5.08	
L_1	0.180		4.57		
Q	0.015	0.035	0.38	0.89	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.54 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Forty-six spaces.

M-40
40-Lead Metal Platform DIP

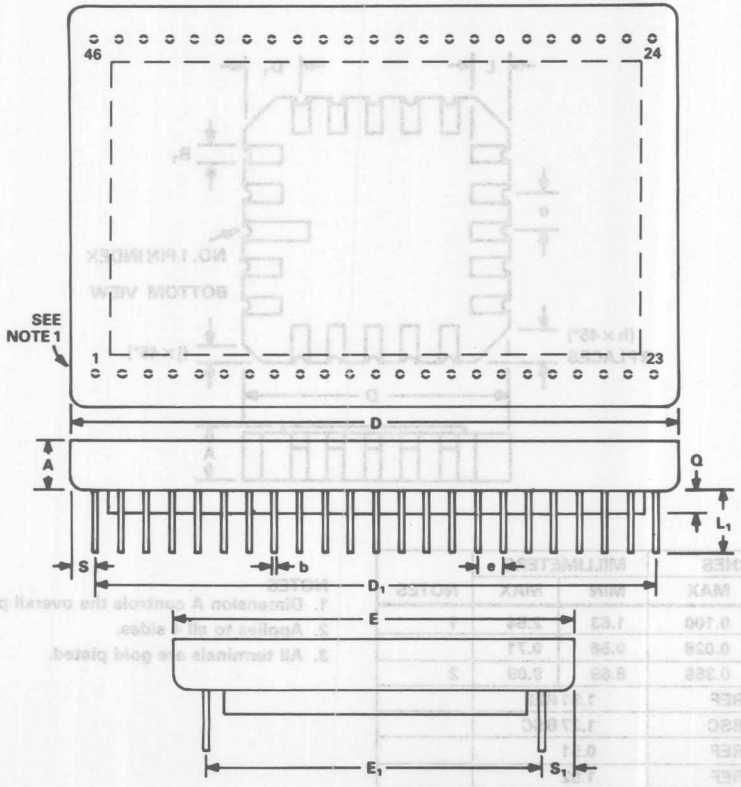


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.19		4.83	
b		0.020		0.51	
D		2.145		54.483	
D_1	1.894	1.906	48.108	48.412	
E		1.145		29.083	
E_1	0.880	0.920	22.352	23.368	3
e	0.098	0.102	2.49	2.59	4
L_1	*0.240*		*6.09*		
S	0.115	0.135	2.92	3.43	2
S_1	0.115	0.135	2.92	3.43	2

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Applies to all four corners.
3. E_1 shall be measured at the centerline of the leads.
4. Thirty-eight spaces.

M-46
46-Lead Metal Platform DIP



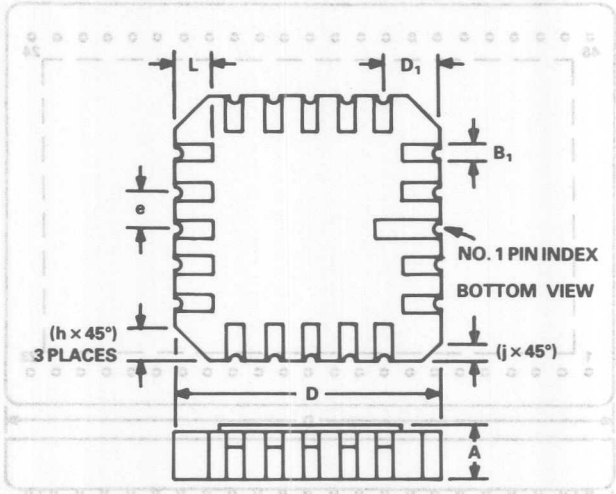
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.231		5.86	
b	0.016	0.020	0.410	0.510	
D		2.380		60.452	
D_1	2.194	2.206	55.728	56.032	
E		1.580		40.132	
E_1	1.280	1.320	32.512	33.528	3
e	0.098	0.102	2.49	2.59	4
L_1	0.210		5.334		
Q	0.055	0.065	1.397	1.651	
S	0.080	0.100	2.032	2.54	2
S_1	0.130	0.150	3.302	3.81	2

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Applies to all four corners.
3. E_1 shall be measured at the centerline of the leads.
4. Forty-four spaces.

11

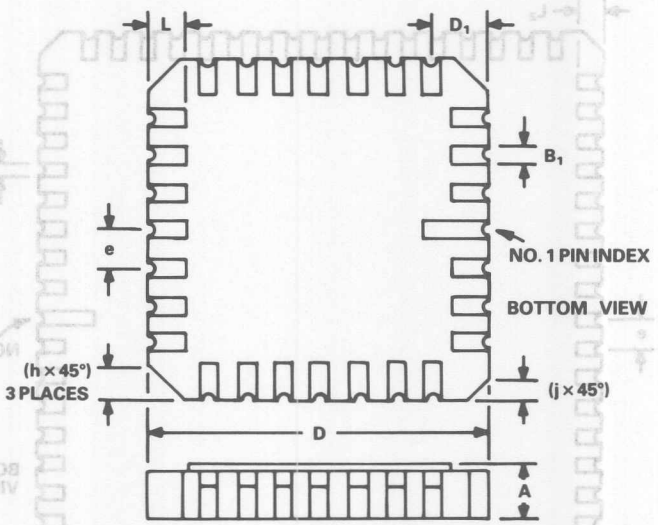
E-20A
20-Terminal Leadless Ceramic Chip Carrier



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.100	1.63	2.54	1
B_1	0.022	0.028	0.56	0.71	
D	0.342	0.358	8.69	9.09	2
D_1	0.075 REF		1.91 REF		
e	0.050 BSC		1.27 BSC		
j	0.020 REF		0.51		
h	0.040 REF		1.02		
L	0.045	0.055	1.14	1.40	

NOTES
1. Dimension A controls the overall package thickness.
2. Applies to all 4 sides.
3. All terminals are gold plated.

E-28A
28-Terminal Leadless Ceramic Chip Carrier



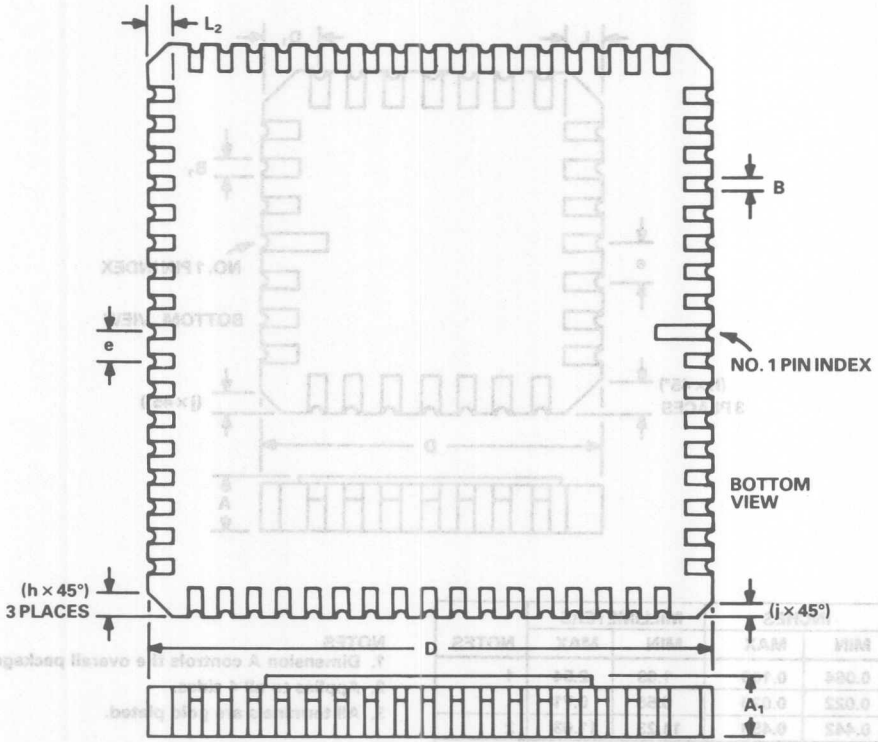
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.100	1.63	2.54	1
B_1	0.022	0.028	0.56	0.71	
D	0.442	0.458	11.23	11.63	2
D_1	0.075 REF		1.91 REF		
e	0.050 BSC		1.27 BSC		
j	0.020 REF		0.51		
h	0.040 REF		1.02		
L	0.045	0.055	1.14	1.40	

NOTES
1. Dimension A controls the overall package thickness.
2. Applies to all 4 sides.
3. All terminals are gold plated.

11

E-68A

68-Terminal Leadless Ceramic Chip Carrier



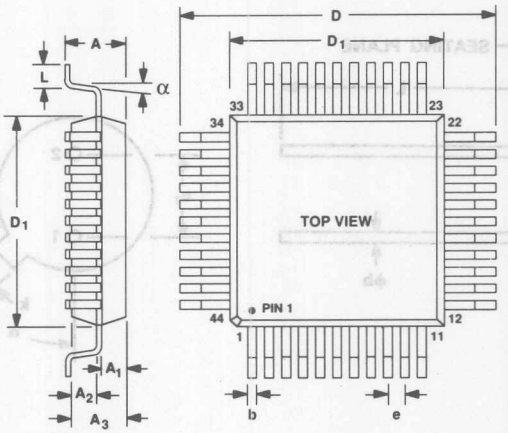
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A_1	0.065	0.103	1.65	2.62	1
B	0.020	0.030	0.51	0.76	
D	0.940	0.965	23.88	24.51	2
e	0.045	0.055	1.14	1.40	
h	0.040 TYP		1.02 TYP		
j	0.020 TYP		0.51 TYP		
L_2	0.045	0.055	1.14	1.40	

NOTES

1. Dimension controls the overall package thickness.
2. Applies to all 4 sides.
3. All terminals are gold plated.

S-44

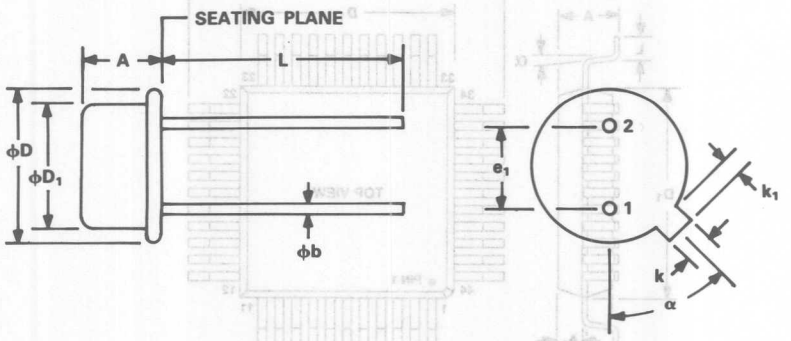
44-Lead Plastic Quad Flatpack (PQFP)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.096		2.44
b	0.012	0.016	0.30	0.41
A_3	0.077	0.083	1.96	2.11
A_1	0.032	0.040	0.81	1.02
D	0.546	0.548	13.875	13.925
A_2	0.032	0.040	0.81	1.02
D_1	0.390	0.398	9.91	10.11
e	0.029	0.033	0.74	0.84
L	0.025	0.037	0.64	0.94
α	0.8	8.0°		

11

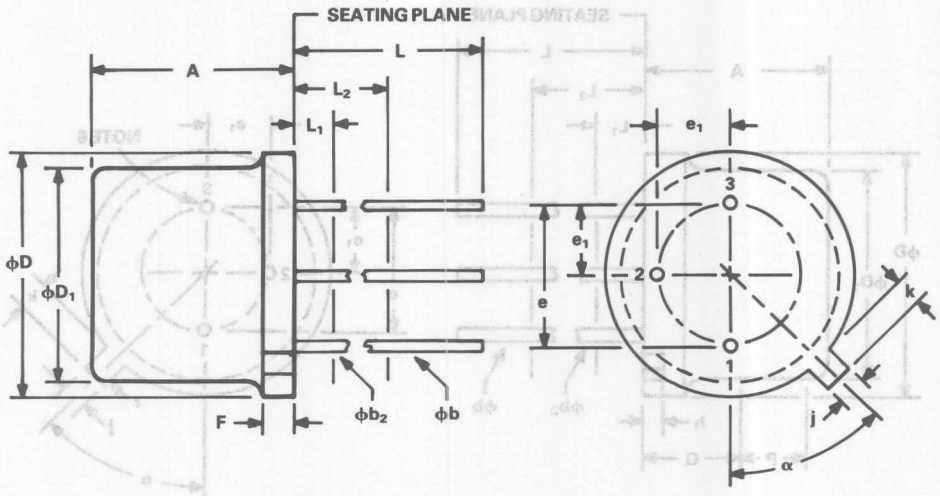
H-02A
2-Lead Metal Can



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.125	0.150	3.17	3.81	
ϕb	0.015	0.019	0.38	0.48	2
ϕD	0.209	0.230	5.31	5.84	
ϕD_1	0.178	0.195	4.52	4.95	
e_1	0.100 BSC		2.54 BSC		1
k	0.036	0.045	0.91	1.17	
k_1	0.028	0.048	0.71	1.22	
L	0.500	0.750	12.70	19.05	
α	45° BSC		45° BSC		1

NOTES
1. Leads having maximum diameter 0.019″ (0.48mm) measured in gauging plane 0.54″ (1.37mm) + 0.001″ (0.03mm) – 0.000″ (0.00mm) below the seating plane of the device are within 0.007″ (0.18mm) of their true positions relative to the maximum-width tab.
2. All leads – increase maximum limit by 0.003″ (0.08mm) when hot solder dip finish is applied.

H-03A
3-Lead Metal Can (TO-52)



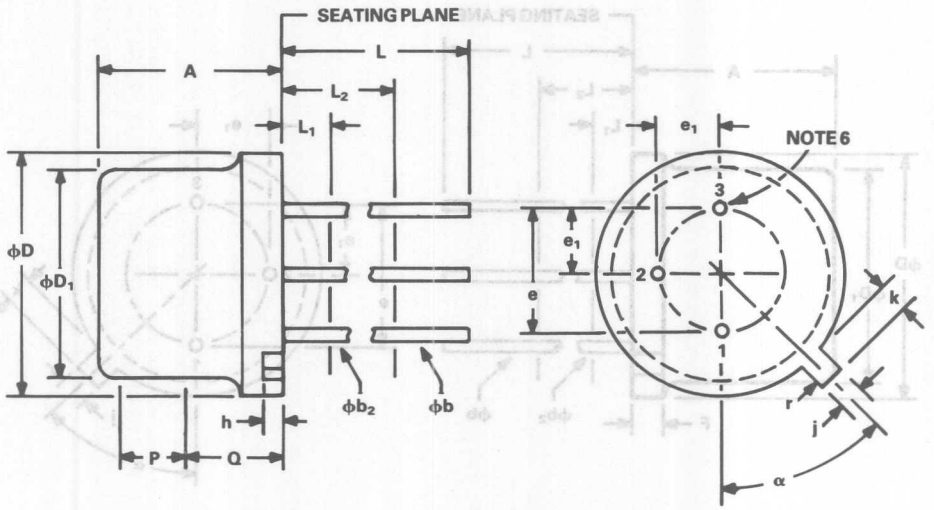
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.115	0.150	2.92	3.81	
ϕb		0.021		0.53	1,4
ϕb_2	0.016	0.019	0.41	0.48	1,4
ϕD	0.209	0.230	5.31	5.84	
ϕD_1	0.178	0.195	4.52	4.95	
e	0.100 T.P.		2.54 T.P.		2
e_1	0.050 T.P.		1.27 T.P.		2
F		0.030		0.76	
j	0.036	0.046	0.91	1.17	
k	0.028	0.048	0.71	1.22	3
L	0.500		12.70		1
L_1		0.050		1.27	1
L_2	0.250		6.35		
α	45° T.P.				

NOTES

1. (Three Leads) ϕb_2 applies between L_1 and L_2. ϕb applies between L_2 and 0.5" (12.70mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.5" (12.70mm) from seating plane.
2. Leads having maximum diameter 0.019" (0.48mm) measured in gauging plane 0.054" (1.4mm) + 0.001" (0.03mm) – 0.000" (0.00mm) below the seating plane of the device are within 0.007" (0.18mm) of their true positions relative to a maximum-width tab.
3. Measured from maximum diameter of the actual device.
4. All leads – increase maximum limit by 0.003" (0.08mm) when hot solder dip finish is applied.

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H-03B
3-Lead Metal Can (TO-5 Style)

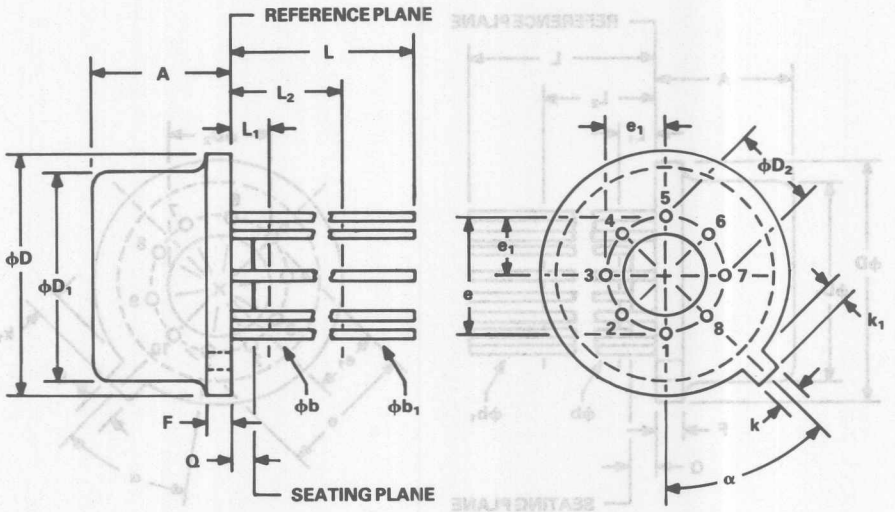


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.021	0.41	0.53	2, 7
ϕb_2	0.016	0.019	0.41	0.48	2, 7
ϕD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
e	0.200 T.P.		5.08 T.P.		4
e_1	0.100 T.P.		2.54 T.P.		
h	0.015	0.035	0.38	0.89	
j	0.028	0.034	0.71	0.86	
k	0.029	0.045	0.74	1.14	3
L	0.500		12.70		2
L_1		0.050		1.27	2
L_2	0.250		6.35		2
P	0.100		2.54		1
Q					5
r		0.007		0.18	
α	45° T.P.				

NOTES

1. This zone is controlled for automatic handling. The variation in actual diameter within the zone shall not exceed 0.010" (0.25mm).
2. (Three leads) ϕb_2 applies between L_1 and L_2. ϕb applies between L_2 and 0.500" (12.70mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70mm) from seating plane.
3. Measured from maximum diameter of the actual device.
4. Leads having maximum diameter 0.019" (0.48mm) measured in gauging plane 0.54" (1.37mm) + 0.001" (0.03mm) – 0.000" (0.00mm) below the seating plane of the device are within 0.007" (0.18mm) of their true positions relative to the maximum-width tab.
5. Details of outline in this zone optional.
6. Lead #3 connected to case.
7. All leads – increase maximum limit by 0.003" (0.08mm) when hot solder dip finish is applied.

H-08A
8-Lead Metal Can (TO-99)



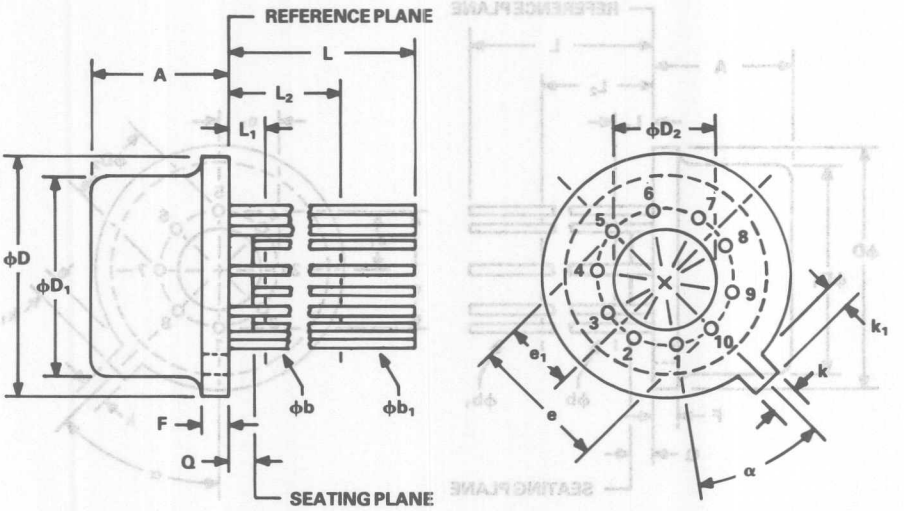
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.019	0.41	0.48	1, 4
ϕb_1	0.016	0.021	0.41	0.53	1, 4
ϕD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
ϕD_2	0.110	0.160	2.79	4.06	
e	0.200 BSC		5.08 BSC		3
e_1	0.100 BSC		2.54 BSC		3
F		0.040		1.02	
k	0.027	0.034	0.69	0.86	
k_1	0.027	0.045	0.69	1.14	
L	0.500	0.750	12.70	19.05	
L_1		0.050		1.27	
L_2	0.250		6.35		
Q	0.010	0.045	0.25	1.14	
α	45° BSC		45° BSC		3

NOTES

1. (All leads) ϕb applies between L_1 and L_2. ϕb_1 applies between L_2 and 0.500" (12.70mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019" (0.48mm) measued in gauging plane 0.054" (1.37mm) + 0.001" (0.03mm) – 0.000" (0.00mm) below the base plane of the product are within 0.007" (0.18mm) of their true position relative to the maximum width tab.
4. All leads – increase maximum limit 0.003" (0.08mm) when hot solder dip finish is applied.

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H-10A
10-Lead Metal Can (TO-100)

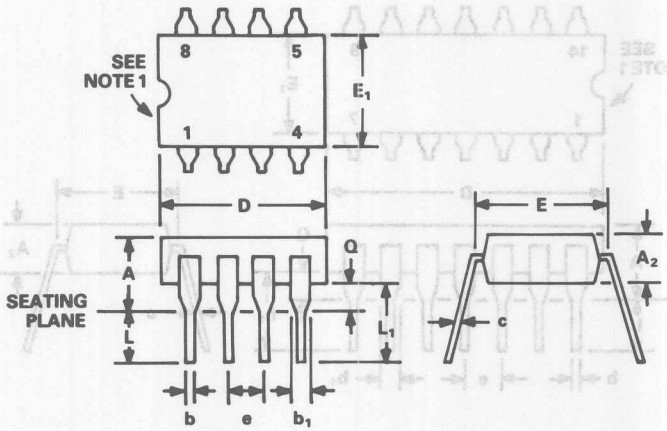


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.019	0.41	0.48	1, 4
ϕb_1	0.016	0.021	0.41	0.53	1, 4
ϕD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
ϕD_2	0.110	0.160	2.79	4.06	
e	0.230 BSC		5.84 BSC		3
e_1	0.115 BSC		2.92 BSC		3
F		0.040		1.02	
k	0.027	0.034	0.69	0.86	
k_1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L_1		0.050		1.27	1
L_2	0.250		6.35		1
Q	0.010	0.045	0.25	1.14	
α	36° BSC		36° BSC		3

NOTES

1. (Three Leads) ϕb_2 applies between L_1 and L_2. ϕb applies between L_2 and 0.5" (12.70mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.5" (12.70mm) from seating plane.
2. Leads having maximum diameter 0.019" (0.48mm) measured in gauging plane 0.054" (1.4mm) + 0.001" (0.03mm) – 0.000" (0.00mm) below the seating plane of the device are within 0.007" (0.18mm) of their true positions relative to a maximum-width tab.
3. Measured from maximum diameter of the actual device.
4. All leads – increase maximum limit by 0.003" (0.08mm) when hot solder dip finish is applied.

N-8
8-Lead Plastic DIP

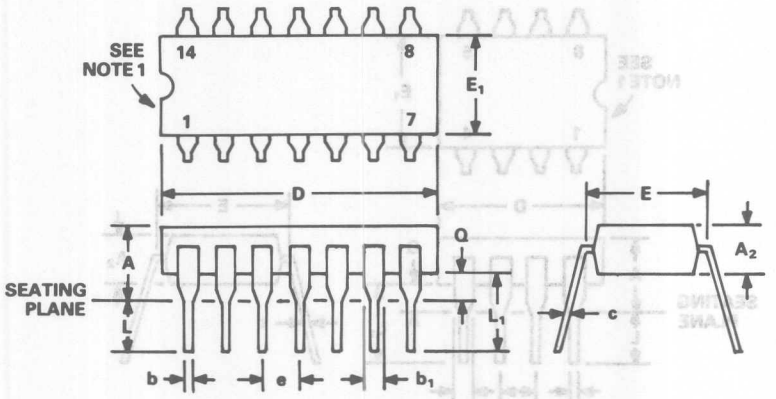


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.348	0.430	8.84	10.92	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

11

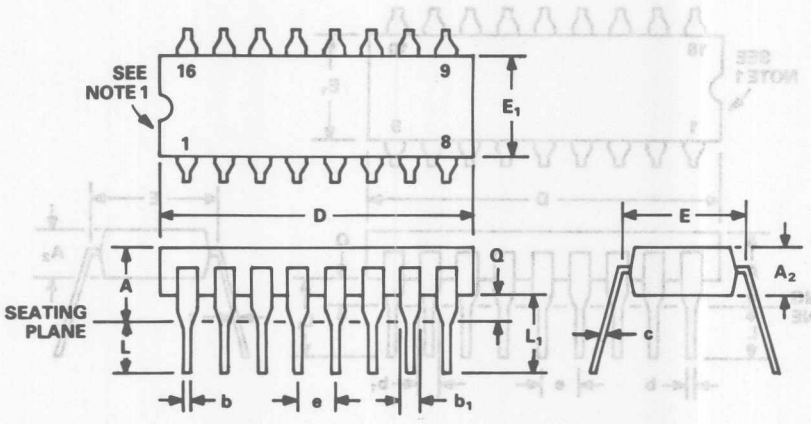
N-14
14-Lead Plastic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.725	0.795	18.42	20.19	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

N-16
16-Lead Plastic DIP



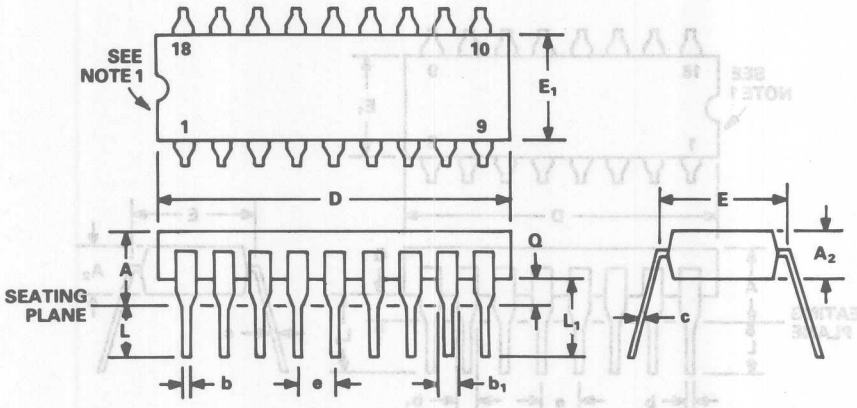
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.745	0.840	18.93	21.33	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

11

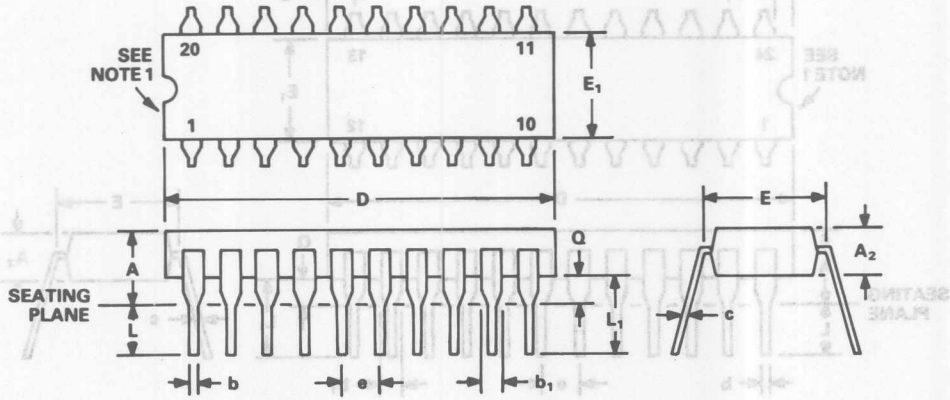
N-18
18-Lead Plastic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.845	0.925	21.47	23.49	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

N-20
20-Lead Plastic DIP



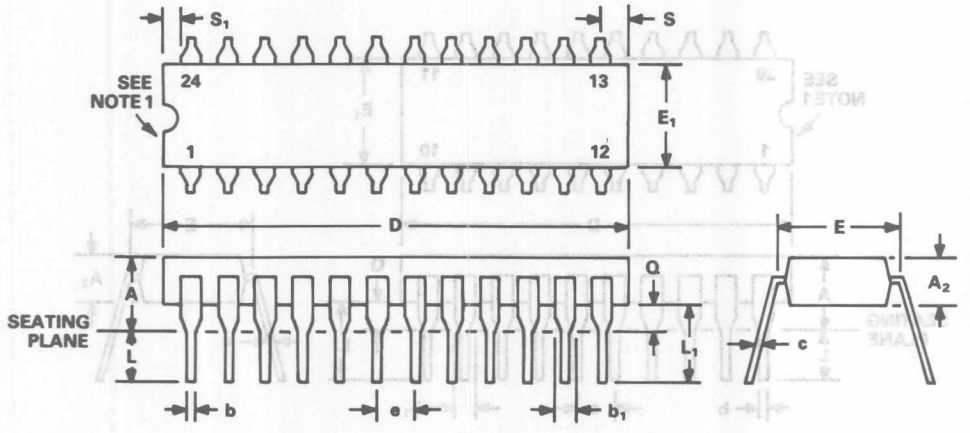
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.925	1.060	23.50	26.90	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES

1. **Index area; a notch or a lead one identification mark is located adjacent to lead one.**
2. **This dimension does not include mold flash or protrusions.**

11

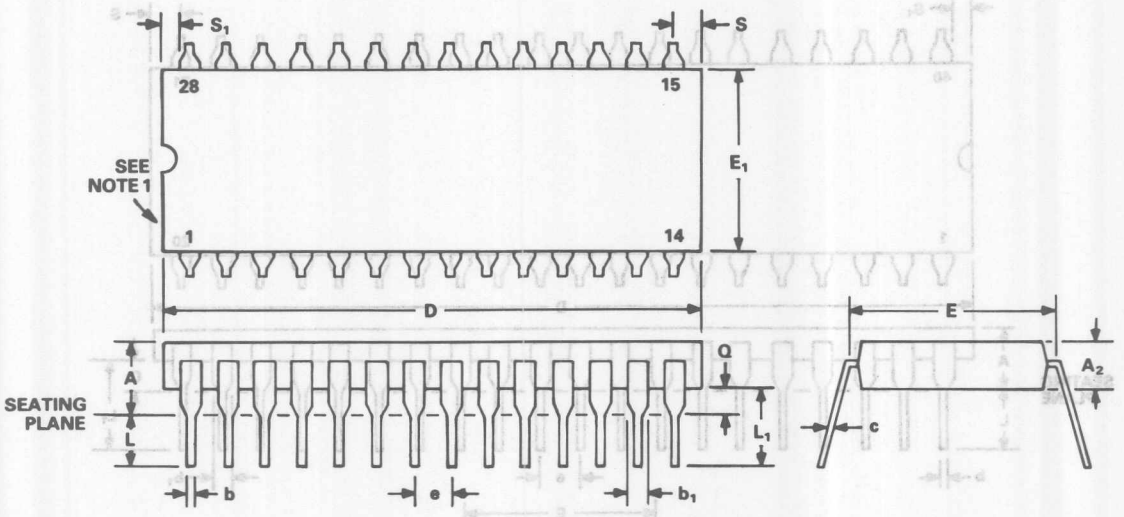
N-24
24-Lead Plastic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	1.125	1.275	28.60	32.30	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. **Index area; a notch or a lead one identification mark is located adjacent to lead one.**
2. **This dimension does not include mold flash or protrusions.**

N-28
28-Lead Plastic DIP

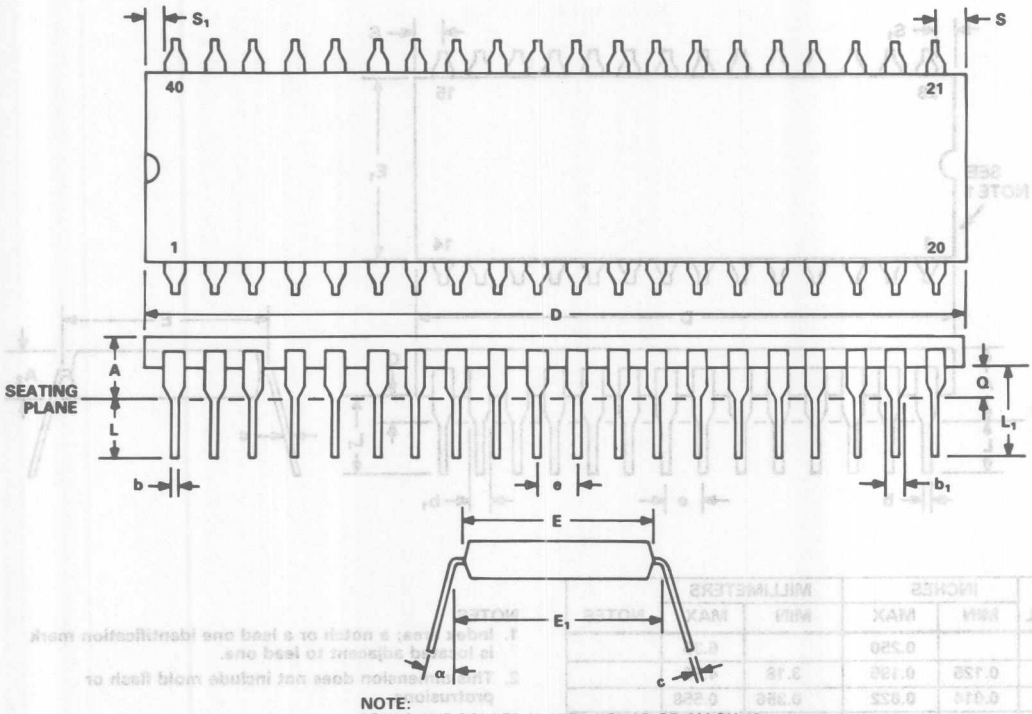


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.250		6.35	
A_2	0.125	0.195	3.18	4.95	
b	0.014	0.022	0.356	0.558	
b_1		0.070		1.77	
c	0.008	0.015	0.204	0.381	
D	1.380	1.565	35.10	39.70	2
E	0.600	0.625	15.24	15.87	
E_1	0.485	0.580	12.32	14.73	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

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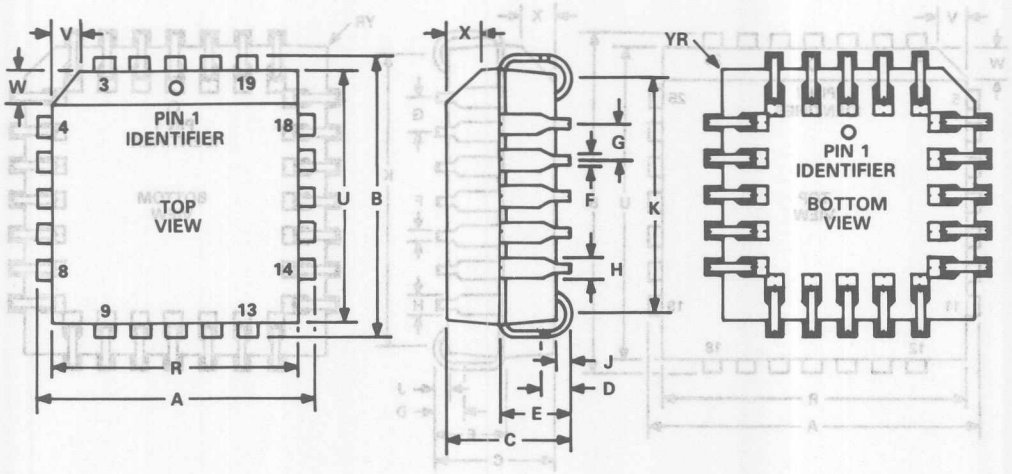
N-40A
40-Lead Plastic DIP



NOTE:
LEADS ARE SOLDER-PLATED KOVAR OR ALLOY 42

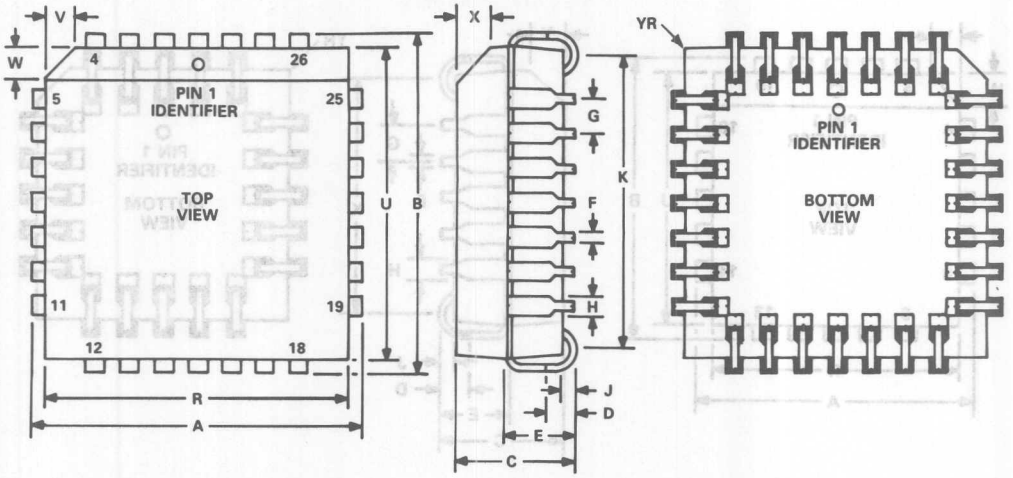
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
b	0.015	0.025	0.38	0.64
b_1	0.040	0.060	1.02	1.52
c	0.008	0.015	0.20	0.38
D	–	2.08	–	52.83
E	0.550	0.550	13.46	13.97
E_1	0.580	0.620	14.73	15.75
e	0.100 BSC		2.54 BSC	
L	0.120	0.175	3.05	4.45
L_1	0.140	–	3.56	–
Q	0.015	0.060	0.38	1.52
S	–	0.110	–	2.79
S_1	0.005	–	0.13	–
α	0°	15°	0°	15°

P-20A
20-Lead Plastic Leaded Chip Carrier (PLCC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.02
B	0.385	0.395	9.78	10.02
C	0.165	0.180	4.19	4.57
D	0.025	0.040	0.64	1.01
E	0.085	0.110	2.16	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.015	0.025	0.38	0.63
K	0.290	0.330	7.37	8.38
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50

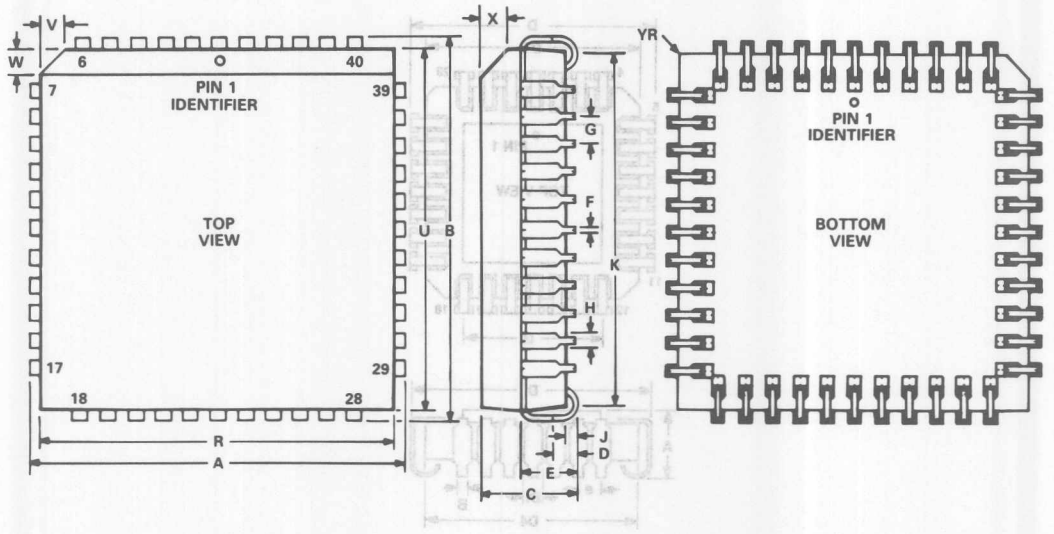
P-28A
28-Lead Plastic Leaded Chip Carrier (PLCC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.19	4.57
D	0.025	0.040	0.64	1.01
E	0.085	0.110	2.16	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.015	0.025	0.38	0.63
K	0.390	0.430	9.91	10.92
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50

P-44A

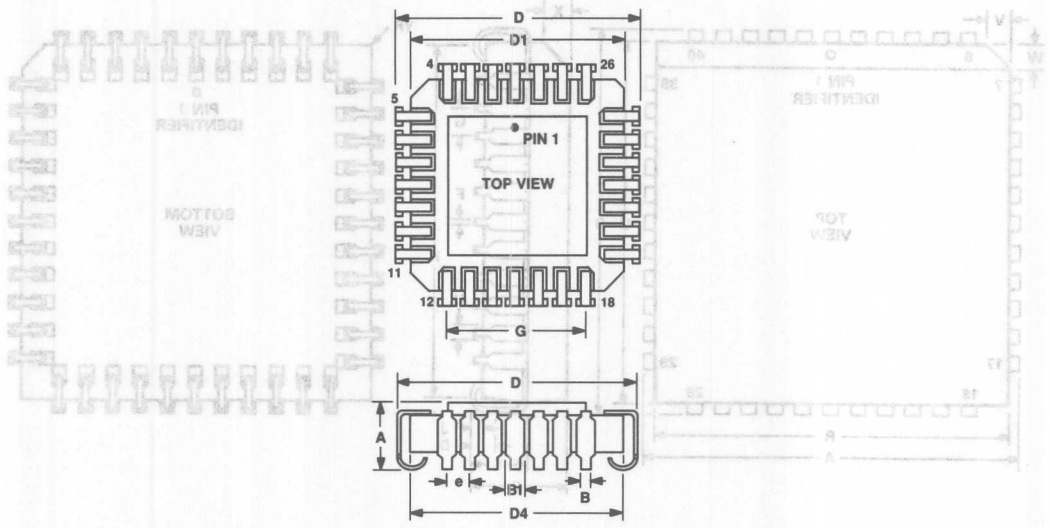
44-Lead Plastic Leaded Chip Carrier (PLCC)



	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.19	4.57
D	0.025	0.040	0.64	1.01
E	0.085	0.110	2.16	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.015	0.025	0.38	0.63
K	0.650	0.656	16.51	16.66
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50

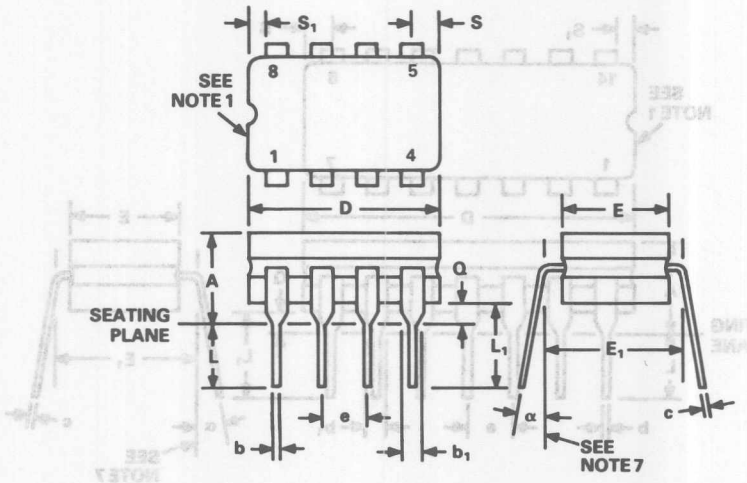
J-28

28-Lead J-Leaded Chip Carrier



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.125		3.175
B	0.013	0.021	0.330	0.534
B_1	0.017		0.432	
D	0.489	0.491	12.196	12.704
D_1	0.440	0.460	11.176	11.684
D_4	0.428	0.432	10.412	11.428
e	0.050 BSC		1.27 BSC	
G	0.280	0.310	2.366	2.874

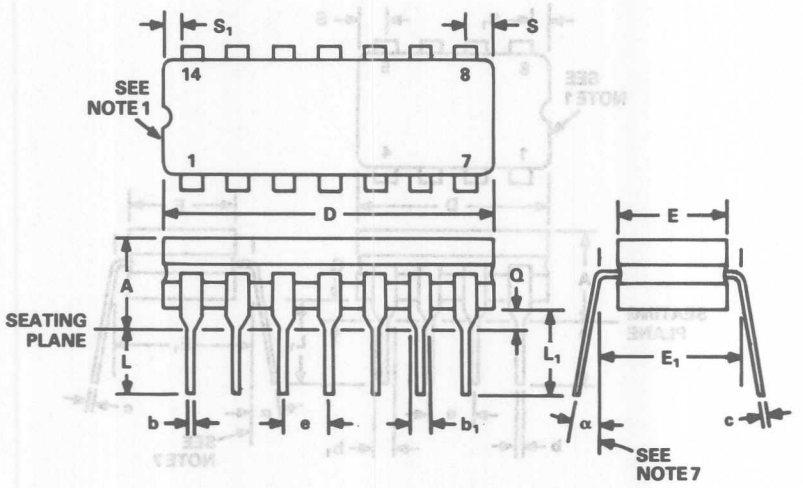
Q-8
8-Lead Cerdip



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		0.405		10.29	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.055		1.35	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Six spaces.

Q-14
14-Lead Cerdip

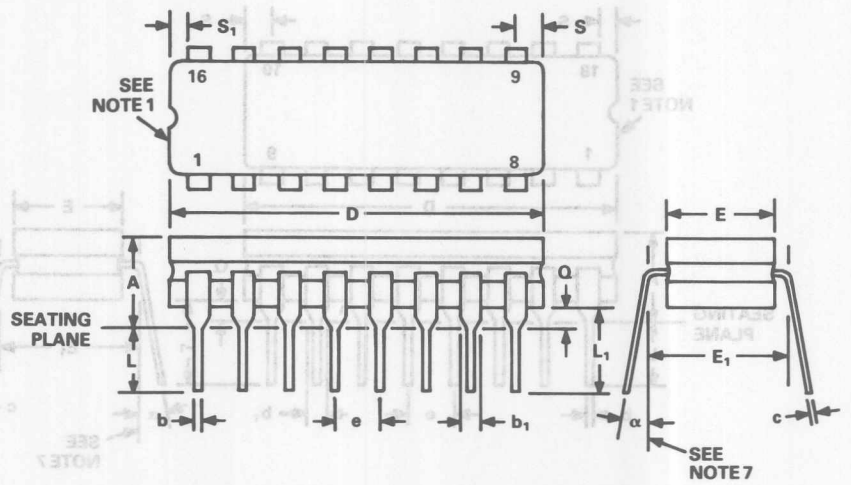


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		0.785		19.94	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Twelve spaces.

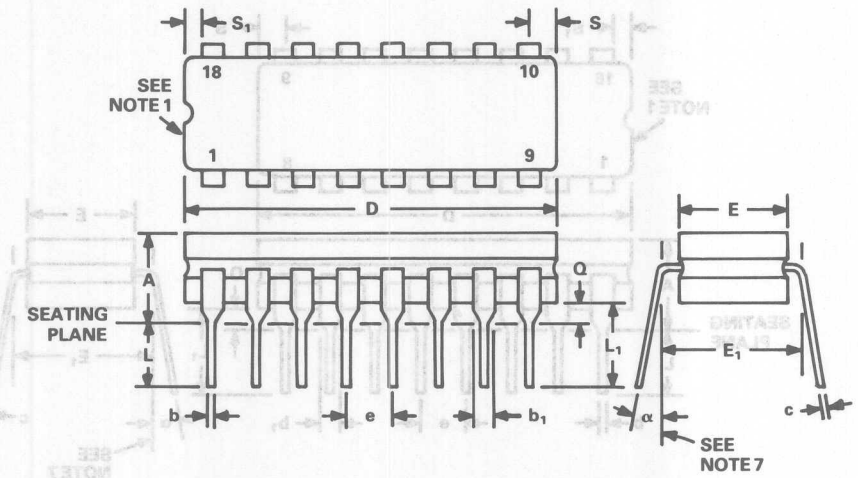
Q-16
16-Lead Cerdip



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		0.840		21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Fourteen spaces.

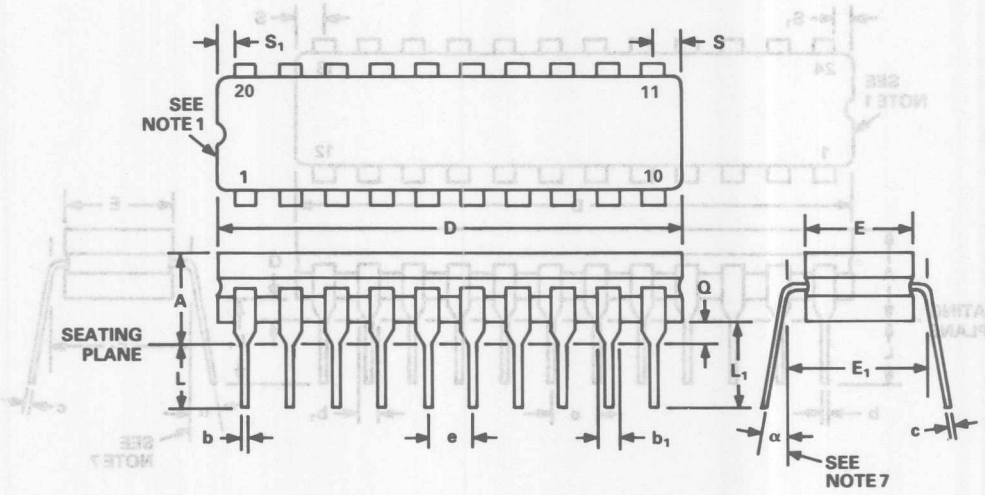
Q-18
18-Lead Cerdip



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		0.960		24.38	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Sixteen spaces.

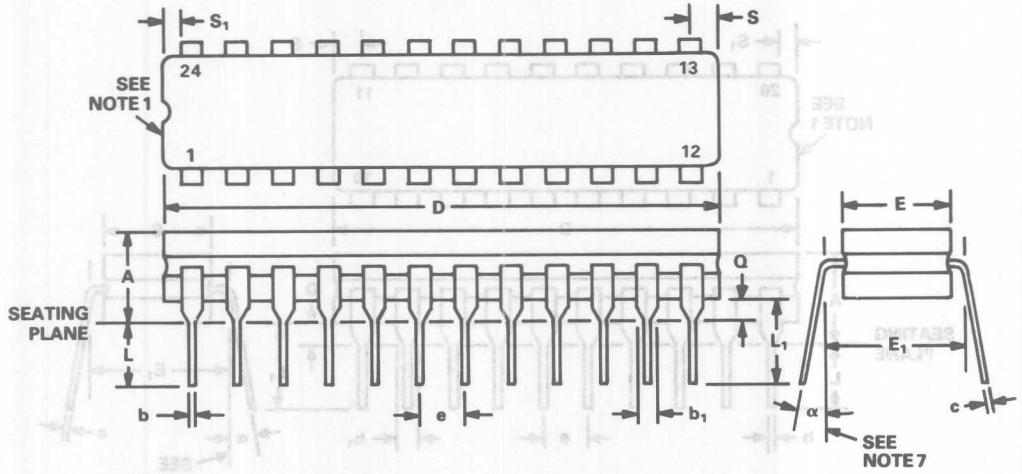
Q-20
20-Lead Cerdip



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		1.060		26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Eighteen spaces.

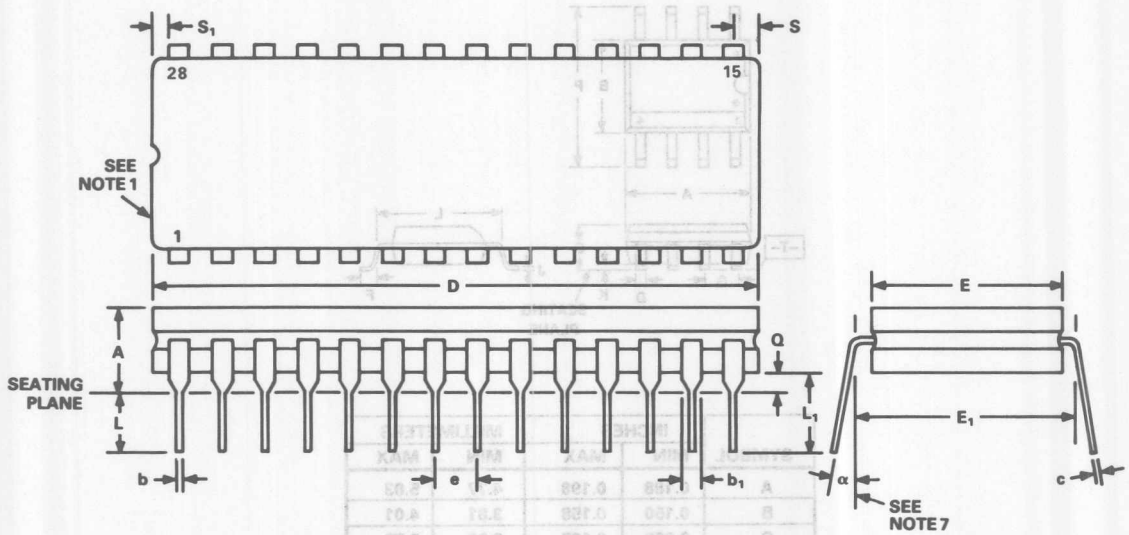
Q-24
24-Lead Cerdip



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		1.280		32.51	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Twenty-two spaces.

Q-28
28-Lead Cerdip

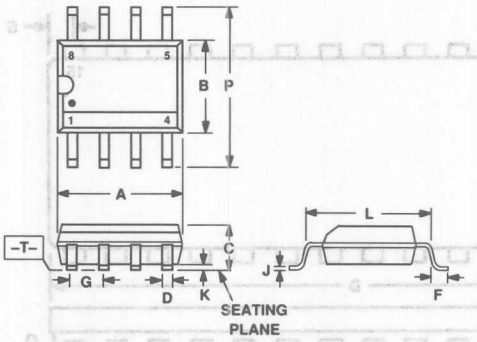


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.026	0.36	0.66	7
b_1	0.030	0.070	0.76	1.78	2, 7
c	0.008	0.018	0.20	0.46	7
D		1.490		37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015		0.38		3
S		0.100		2.54	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Twenty-six spaces.

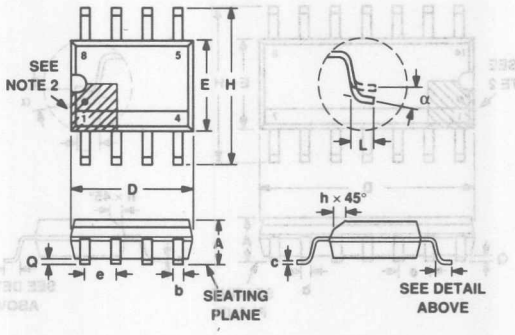
R-8
8-Lead Small Outline (SOIC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.188	0.198	4.77	5.03
B	0.150	0.158	3.81	4.01
C	0.089	0.107	2.26	2.72
D	0.014	0.022	0.36	0.56
F	0.018	0.034	0.46	0.86
G	0.050 BSC		1.27 BSC	
J	0.007	0.015	0.18	0.38
K	0.005	0.011	0.125	0.275
L	0.195	0.205	4.95	5.21
P	0.224	0.248	5.69	6.29

SO-8

8-Lead Narrow-Body SO
(S-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	
b	0.0138	0.0192	0.35	0.49	
c	0.0075	0.0098	0.19	0.25	
D	0.1890	0.1968	4.80	5.00	
E	0.1497	0.1574	3.80	4.00	
H	0.2284	0.2440	5.80	6.20	
e	0.0500 BSC		1.27 BSC		
h	0.0099	0.0196	0.25	0.50	
L	0.0160	0.0500	0.41	1.27	
Q	0.0040	0.0098	0.10	0.25	
α	0°	8°	0°	8°	

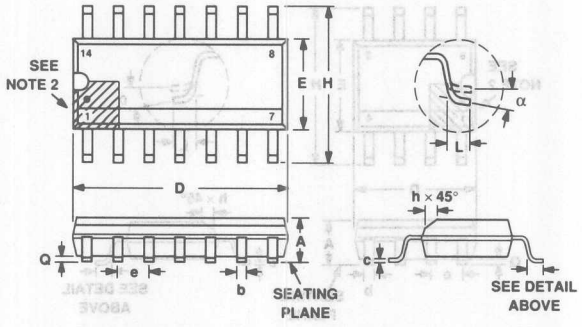
NOTES

1. **Package dimensions conform to JEDEC specification MS-012-AA (Issue A, June 1985).**
2. **Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.**

11

R-14

14-Lead Narrow-Body SO
(S-Suffix)



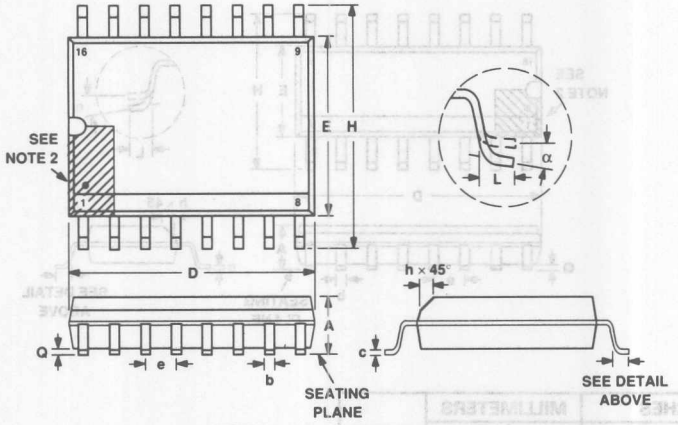
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	
b	0.0138	0.0192	0.35	0.49	
c	0.0075	0.0098	0.19	0.25	
D	0.3367	0.3444	8.55	8.75	
E	0.1497	0.1574	3.80	4.00	
H	0.2284	0.2440	5.80	6.20	
e	0.0500 BSC		1.27 BSC		
h	0.0099	0.0196	0.25	0.50	
L	0.0160	0.0500	0.41	1.27	
Q	0.0040	0.0098	0.10	0.25	
α	0°	8°	0°	8°	

NOTES

1. **Package dimensions conform to JEDEC specification MS-012-AB (Issue A, June 1985).**
2. **Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.**

R-16 (S-Suffix)

16-Lead Wide-Body SO
(SOL-16)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.3977	0.4133	10.10	10.50	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

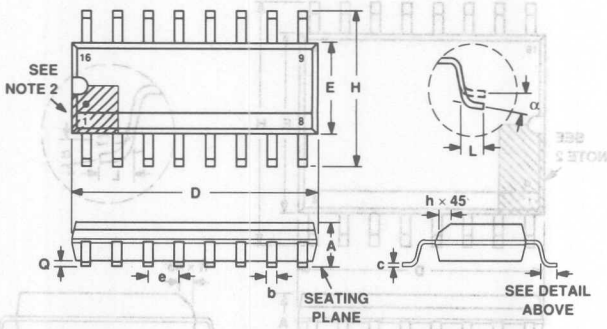
NOTES

1. **Package dimensions conform to JEDEC specification MS-013-AA (Issue A, June 1985).**
2. **Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.**

11

R-16A (S-Suffix)

16-Lead Narrow-Body SO
(SO-16)



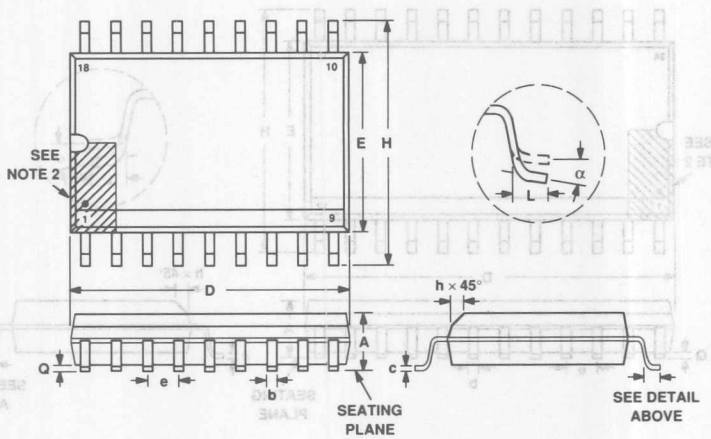
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	
b	0.0138	0.0192	0.35	0.49	
c	0.0075	0.0099	0.19	0.25	
D	0.3859	0.3937	9.80	10.00	
E	0.1497	0.1574	3.80	4.00	
H	0.2284	0.2440	5.80	6.20	
e	0.0500 BSC		1.27 BSC		
h	0.0099	0.0196	0.25	0.50	
L	0.0160	0.0500	0.41	1.27	
Q	0.0040	0.0098	0.10	0.25	
α	0°	8°	0°	8°	

NOTES

1. **Package dimensions conform to JEDEC specification MS-012-AC (Issue A, June 1985).**
2. **Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.**

R-20 (S-Suffix)

20-Lead Wide-Body SO
(SOL-20)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.4961	0.5118	12.60	13.00	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

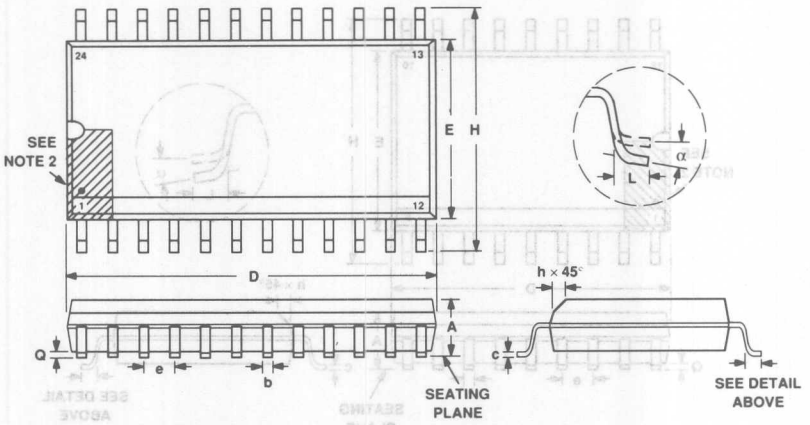
NOTES

1. **Package dimensions conform to JEDEC specification MS-013-AC (Issue A, June 1985).**
2. **Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.**

11

R-24 (S-Suffix)

24-Lead Wide-Body SO
(SOL-24)



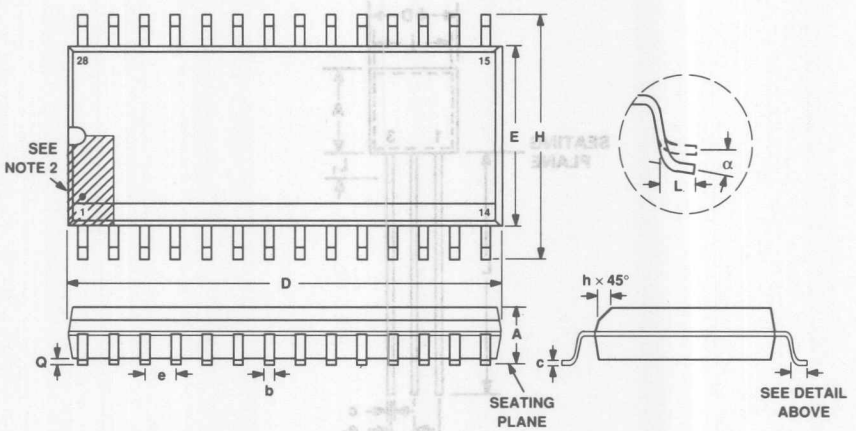
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.5985	0.6141	15.20	15.60	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

NOTES

1. **Package dimensions conform to JEDEC specification MS-013-AD (Issue A, June 1985).**
2. **Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.**

R-28 (S-Suffix)

28-Lead Wide-Body SO
(SOL-28)



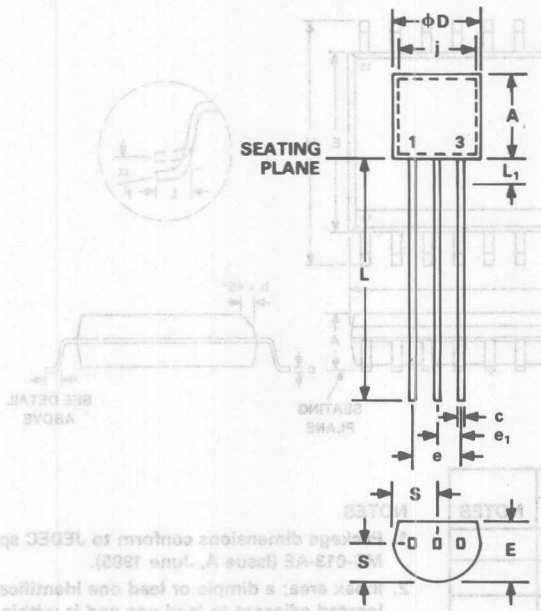
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.6969	0.7125	17.70	18.10	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

NOTES

1. **Package dimensions conform to JEDEC specification MS-013-AE (Issue A, June 1985).**
2. **Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.**

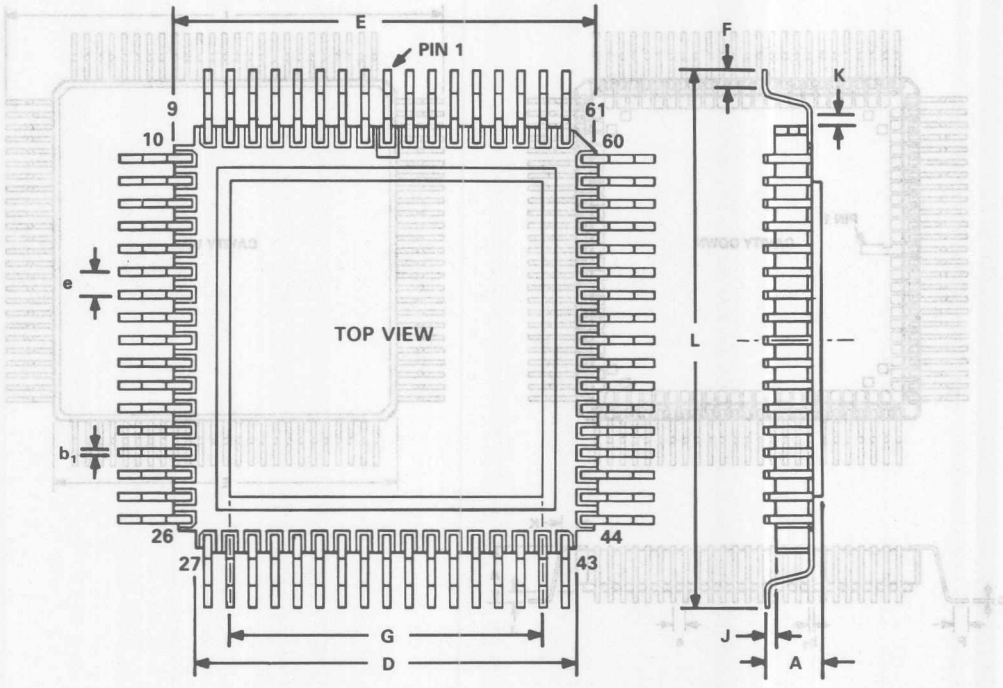
11

TO-92
3-Lead Plastic



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.170	0.210	4.58	5.33
c	0.016	0.019	0.407	0.482
ϕD	0.175	0.205	4.96	5.20
e	0.095	0.105	2.42	2.66
e_1	0.045	0.055	1.15	1.39
E	0.125	0.165	3.94	4.19
J	0.175	0.205	4.96	5.20
L	0.500		12.70	
L_1		0.050		1.27
S	0.080	0.105	2.42	2.66

Z-68
68-Lead Leaded Chip Carrier (Ceramic)

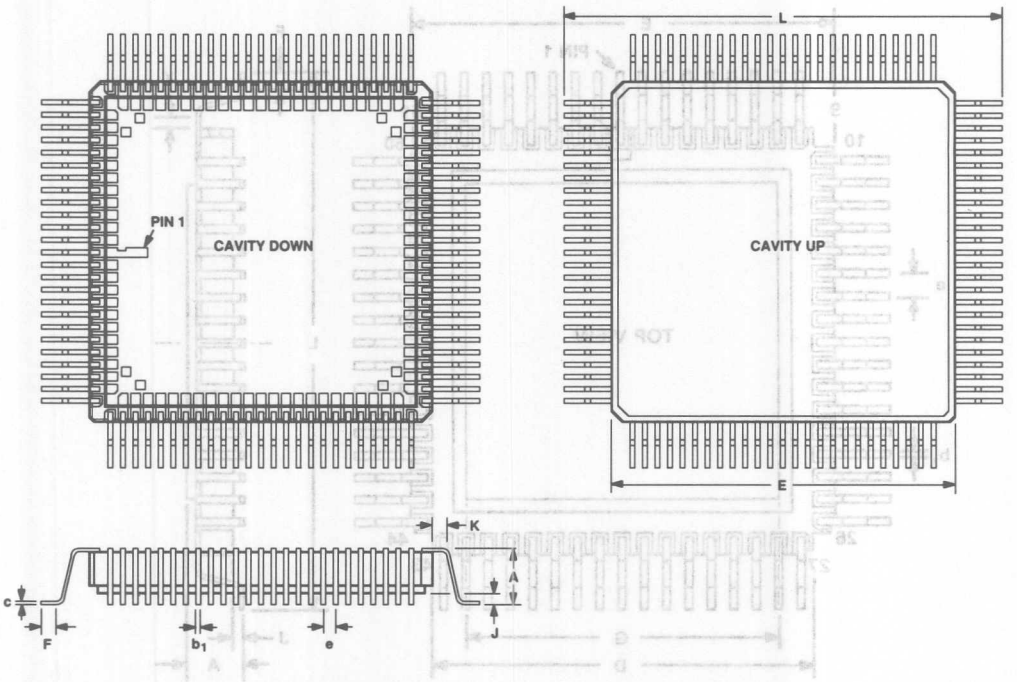


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.092	0.118	2.337	2.997
b_1	0.016	0.020	0.452	0.462
D	0.841	0.859	21.361	21.819
e	0.050 BSC		1.27 BSC	
E	0.940	0.960	23.876	24.384
F	0.040		1.016	
G	0.695	0.705	17.653	17.907
K	0.025		0.625	
L	1.200	1.220	30.476	30.984

11

Z-100

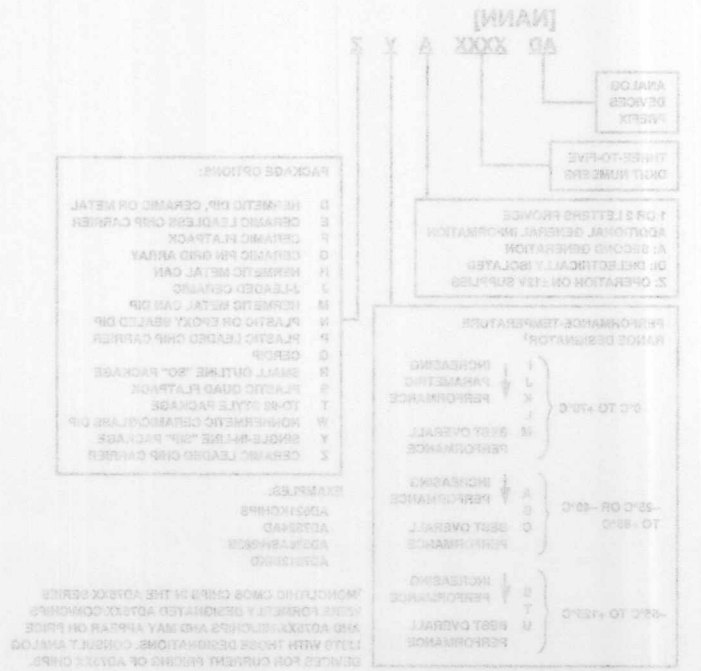
100-Lead Leaded Chip Carrier (Ceramic)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.198	0.243	5.03	6.17	
b_1	0.018	0.022	0.46	0.56	
c	0.007	0.0095	0.18	0.24	
E	1.336	1.364	33.93	34.65	
F	0.040		1.02		
e	0.050 BSC		1.27 BSC		
L	1.675	1.685	42.55	42.80	
J	0.025		0.63		
K	0.040		1.02		

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Ordering Guide

INTRODUCTION

This Ordering Guide should make it easy to order Analog Devices products, whether you're buying one IC op amp, a multioption subsystem, or 1000 each of 15 different items. It will help you:

1. Find the correct part number for the options you want.
2. Get a price quotation and place an order with us.
3. Know our warranty for components and subsystems.

For answers to further questions, call the nearest sales office (listed at the back of the book) or our main office in Norwood, Mass. U.S.A. (617-329-4700).

MODEL NUMBERING

In this reference manual many of the data sheets for products having a number of standard options contain an Ordering Guide. Use it to specify the correct part number for the exact combination of options you want. Two model numbering schemes are used by Analog Devices. The first model numbering scheme is used for designating standard Analog Devices monolithic and hybrid products. The second scheme is used by our Precision Monolithics Division (formerly PMI) as designators for its product line.

Figure 1 shows the form of model number used for our proprietary standard monolithic ICs and many of our hybrids. It consists of an "AD" (Analog Devices) prefix, a 3-to-5-digit number*, an alphabetic performance/temperature-range designator and a package designator. One or two additional letters may immediately follow the digits ("A" for second-generation redesigned ICs, "DI" for dielectrically isolated CMOS switches, e.g., AD536AJH, AD7512DIKD).

Figure 2 shows a different numbering scheme used by our Precision Monolithics Division. This numbering scheme starts with a prefix which designates the device type and model number. It is then followed by a suffix consisting of alphabetic designators (as applicable) to indicate additional functional designations or options and packaging options.

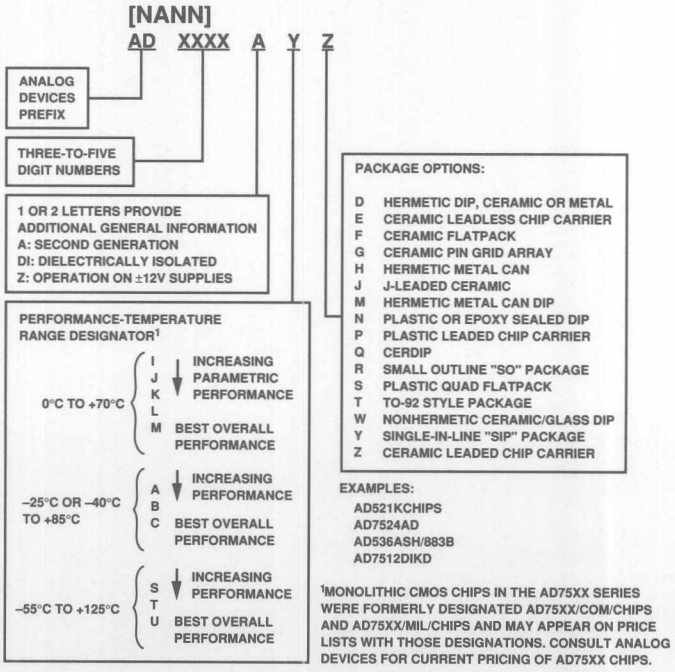


Figure 1. Model-Number Designations for Standard Analog Devices Monolithic and Hybrid IC Products. S, T and U Grades have the Added Suffix, /883B for Devices that Qualify to the Latest Revision of MIL-STD-883, Level B.

***For some models, the combination [digit][letter][two or three digits] is used instead of ADXXXX, e.g., 2S80.**

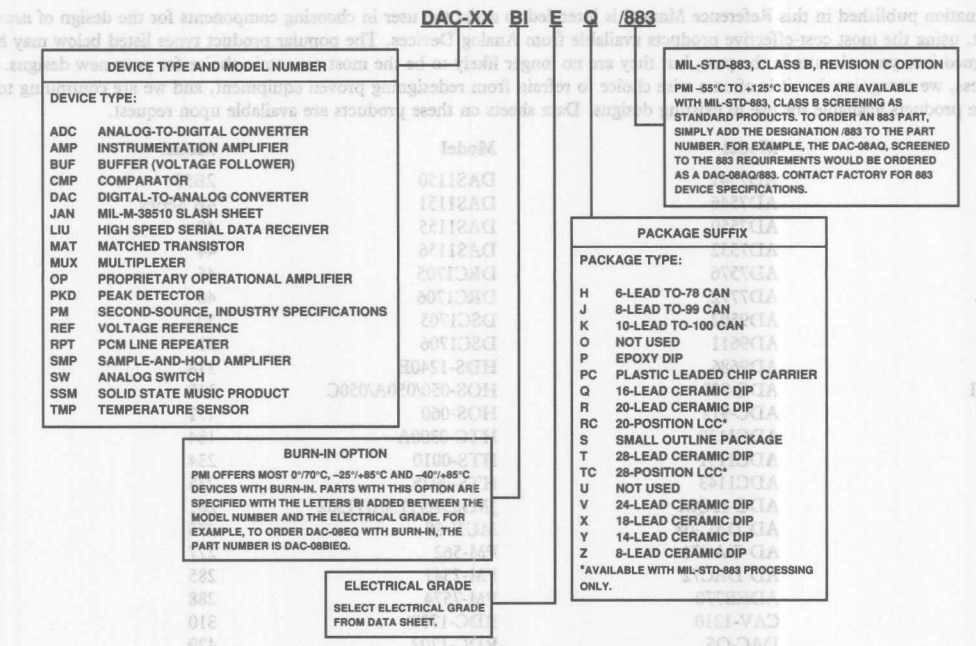


Figure 2. Precision Monolithics Division's Product Designations

ORDERING FROM ANALOG DEVICES

When placing an order, please provide specific information regarding model type, number, option designations, quantity, ship-to and bill-to address. Prices quoted are list; they do not include applicable taxes, customs, or shipping charges. All shipments are F.O.B. factory. Please specify if air shipment is required.

Place your orders with our local sales office or representative, or directly with our customer service group located in the Norwood facility. Orders and requests for quotations may be telephoned, sent via FAX or TELEX, or mailed. Orders will be acknowledged when received; billing and delivery information is included.

Payments for new accounts, where open-account credit has not yet been established, will be C.O.D. or prepaid. Analog Devices' minimum order value is two hundred fifty dollars ($250.00).

When prepaid, orders should include $2.50 additional for packaging and postage (and a 5% sales tax on the price of the goods if you are ordering for delivery to a destination in Massachusetts).

You may also order Analog Devices parts through distributors. For information on distributors, please see pages 12–12 and 12–13 at the back of this volume.

WARRANTY AND REPAIR CHARGE POLICIES

All Analog Devices, Inc., products are warranted against defects in workmanship and materials under normal use and service for one year from the date of their shipment by Analog Devices, Inc., except that components obtained from others are warranted only to the extent of the original manufacturers' warranties, if any, except for component test systems, which have a 180-day warranty, and μMAC and MACSYM systems, which have a 90-day warranty. This warranty does not extend to any products which have been subjected to misuse, neglect, accident, or improper installation or application, or which have been repaired or altered by others. Analog Devices' sole liability and the Purchaser's sole remedy under this warranty is limited to repairing or replacing defective products. (The repair or replacement of defective products does not extend the warranty period. This warranty does not apply to components which are normally consumed in operation or which have a normal life inherently shorter than one year.) Analog Devices, Inc., shall not be liable for consequential damages under any circumstances.

THE FOREGOING WARRANTY AND REMEDY ARE IN LIEU OF ALL OTHER REMEDIES AND ALL OTHER WARRANTIES, WRITTEN OR ORAL, STATUTORY, EXPRESS, OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

Product Families Not Included in the Reference Manual (But Still Available)

The information published in this Reference Manual is intended to assist the user in choosing components for the design of *new* equipment, using the most cost-effective products available from Analog Devices. The popular product types listed below may have been designed into your circuits in the past, but they are no longer likely to be the most economic choice for your new designs. Nevertheless, we recognize that it is often a wise choice to refrain from redesigning proven equipment, and we are continuing to make these products available for use in existing designs. Data sheets on these products are available upon request.

Model	Model	Model	Model
AD101	AD7541	DAS1150	2B59
AD201	AD7546	DAS1151	4B Series
AD293	AD7550	DAS1155	40
AD294	AD7552	DAS1156	44
AD301	AD7576	DRC1705	45
AD301AL	AD7772	DRC1706	46
AD367	AD9502	DSC1705	50
AD368	AD9611	DSC1706	51
AD369	AD9686	HDS-1240E	118
AD370/371	ADC-908	HOS-050/050A/050C	148
AD392	ADC-912	HOS-060	171
AD503	ADC1130	HTC-0300A	184
AD504	ADC1131	HTS-0010	234
AD506	ADC1143	HTS-0025	235
AD510	ADC-12QM	JM38510/11301/11302	261
AD515	AD DAC-08	MUX-88	275
AD518	AD DAC71	PM-562	277
AD533	AD DAC72	PM-7541	285
AD535	ADEB770	PM-7574	288
AD545	CAV-1210	RDC-1700	310
AD567	DAC-QS	RDC-1702	429
AD611	DAC-QZ	RDC-1704	433
AD651	DAC-01	RDC-1725	434
AD1147	DAC-02/03	RDC-1726	435
AD1148	DAC-05/06	RDC-1768	436
AD1403	DAC-10Z	RTM Series	440
AD2004	DAC-12M	SDC1700	442
AD2006	DAC-12QS	SDC1702	450
AD2008	DAC-12QZ	SDC1704	451
AD2009	DAC-20	SDC1725	452
AD2016	DAC71/72	SDC1726	453
AD2020	DAC-86	SDC1768	458
AD2033	DAC-88	SHA-5	460
AD2040	DAC-89	SHA-1134	603
AD3554	DAC-210	SHA-1144	751
AD3860	DAC-888	SMP-81	756
AD5200 Series	DAC1108	STM Series	903
AD5210 Series	DAC1136	SW-01/02	906
AD7110	DAC1138	SW-7510/7511 2B24	915
AD7240	DAC1146	2B34	926
AD7520	DAC-1408A	2B35	947
AD7521	DAC1420	2B50	959
AD7522	DAC1422	2B52	968
AD7523	DAC1423	2B53	972
AD7525	DAC1508A	2B56	
AD7530	DAC-8212	2B57	
AD7531	DAS1128	2B58	

Substitution Guide for Product Families No Longer Available

The products listed in the left-hand column are no longer available from Analog Devices. In many cases, comparable functions and performance may be obtained with newer models, but—as a rule—they are not directly interchangeable. The closest recommended Analog Devices equivalent, physically and electrically, is listed in the right-hand column. If no equivalent is listed, or for further information, contact your local sales office.

Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent
AD108/208/308	AD705	AD2037	None	AMP-01BX	AMP-01AX
AD108A/208A/308A	AD705	AD2038	None	AMP-01BX/883C	AMP-01AX/883C
AD111/211/311	AD790	AD5010/6020	AD9000	AMP-05BX	AMP-05AX
AD345	AD1321/1322	AD6012	AD565A	AMP-05BX/883C	AMP-05Z/883C
AD351	AD790	AD7115	AD7111	API1620/1718	Consult ADI
AD362	AD1362	AD7513	ADG201A	BDM 1615/16/17	None
AD376	AD1376	AD7516	AD7510DI	BUF-03BJ/883C	BUF-03AJ/883C
AD501	AD711	AD7519	None	CAV-0920/1020	AD9020/9060
AD502	AD711	AD7527	AD7548	CAV-1202	AD9005
AD505	AD509	AD7544	AD7548	CAV-1205	AD9005
AD508	AD517	AD7555	AD1175K	CMP-01Z	CMP-01J
AD511	AD711	AD7560	None	CMP-05BJ	CMP-05CJ
AD512	AD711	AD7570	AD7579/AD7580	CMP-05BZ	CMP-05CZ
AD513	AD711	AD7571	AD7579/AD7580	CMP-05GJ	CMP-05CJ
AD514	AD711	AD7583	AD7880+MUX	CMP-404BY	CMP-404AY
AD516	AD711	AD9011	AD9002	CMP-404BY/883C	CMP-404AY/883C
AD520	AD524	AD9521	AD640	DAC-02ACX1	DAC-02CCX1
AD523	AD549	AD9615	AD9611/AD9617	DAC-05AX1	DAC-02CCX1
AD528	AD711/744	AD9685	AD96685	DAC-05EX1	DAC-02CCX1
AD530	AD533	AD9687	AD96686	DAC-10BX	DAC-10FX
AD531	AD532	AD9688	AD9002/AD9028	DAC-10CX	DAC-10GX
AD540	AD544	AD ADC-816	AD7820/AD7821	DAC-10DF	AD568
AD559	AD557/AD558	ADC-8S	AD673	DAC-10H	DAC-10Z
AD565	AD565A	ADC-10Z	AD574A	DAC-14QM	DAC1136
AD566	AD566A	ADC-12QL	AD7578	DAC-16QM	DAC1136
AD612	AD524	ADC-12QZ	AD574A/AD674A	DAC-100AAQ7	DAC-100ACQ7
AD614	AD524	ADC-14I/17I	AD1170	DAC-100AAQ8	DAC-100ACQ8
AD689	AD586	ADC-1100	AD7550/AD7552	DAC-100ABQ7	DAC-100ACQ7
AD801	AD711	ADC1102	AD7870	DAC-100ABQ8	DAC-100ACQ8
AD810-813	None	ADC1103	AD7572A	DAC-100BBQ5/883C	DAC-100ACQ5/883C
AD814-816	None	ADC1105	AD7550/AD7552	DAC-100BCQ7	DAC-100BBQ7
AD818	None	ADC1109	AD7572A	DAC-100DDQ7	DAC-100CCQ7
AD820-822	None	ADC1111	AD574A	DAC-312BR	DAC-312ER
AD830-833	None	ADC1121	AD7880	DAC-888AX	DAC-888EX
AD835-839	None	ADC1123	AD7880	DAC-888BX	DAC-888EX
AD1145	AD7846	ADC1133	AD574A	DAC1009	AD767
AD1408	AD558	ADC-QM	AD574A/AD674A	DAC1106	AD568
AD1508	AD558	ADC-QU	AD574A/AD674A	DAC1112	DAC12QS
AD1678	AD678	AD DAC100	AD561	DAC1118	AD767
AD1679	AD679	ADG200	None	DAC1122	AD7541A
AD1779	AD779	ADG201	ADG201A	DAC1125	AD7533
AD2003	AD2021	ADLH0032G/CG	AD843	DAC1132	AD667
AD2022	None	ADLH0033G/CG	AD9620/AD9630	DAC-1408-6P	DAC-1408-8P
AD2023	None	ADM501	None	DAC-1408-7P	DAC-1408-8P
AD2024	None	ADP501	None	DAC-1408-7Q	DAC-1408-8Q
AD2025	None	ADREF01	REF-01	DAC-1408-GQ	DAC-1408-8Q
AD2027	None	ADREF02	REF-02	DAC-1508A-8Q	DAC-1408-8Q
AD2028	None	ADSHC-85	AD585	DRC1605/06	DRC1705/06; SDC1740
AD2036	None	ADSHM-5	HTC-0300A		

Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent
DRC1765/66	AD2S65/66	OP-02EZ	OP-177GZ	PM-157J	PM-175J/883C
DSC1605/06	DSC1705/06; SDC1740	OP-02J	OP-02AJ	PM-157J/883C	PM-157AJ/883C
DSC1765/66	AD2S65/66	OP-02/883C	OP-02AZ/883C	PM-208AJ	PM-108AJ/883C
DTM1716/17	AD2S65/66	OP-04DY	OP-04CY	PM-208AZ	PM-108AZ
HAS-0802	HAS1202A	OP-04GBC	OP-04NBC	PM-308AZ	PM-1008GZ
HAS-1002	HAS1202A	OP-04Y/883C	OP-04AY/883C	PM-308J	PM-1008G
HAS-1202	HAS1202A	OP-05Z	OP-05AZ	PM-4136RC	OP-11ARC/883C
HDD-1015	AD9712A	OP-05/883C	OP-05AZ/883C	PM-562AV	PM-562HV
HDD-1409	None	OP-06BJ/883C	OP-06AJ/883C	PM-562BV	PM-562HV
HDG-0805	AD9701	OP-06EZ	OP-06GZ	PM-562FV	PM-562HV
HDH-0802	AD9713A	OP-06FZ	OP-06GZ	PM-562GV	PM-562HV
HDH-1003	AD9713A	OP-08AJ	PM-1008AJ	PM-741J	OP-02AJ
HDH-1205	AD9713A	OP-08AJ/883C	PM-1008AJ/883C	RAC1763	None
HDL-3805	ADV453/ADV478	OP-08AZ/883C	PM-1008AZ/883C	RDC1602/03	RDC1702/03
HDL-3806	ADV453/ADV478	OP-08CZ/883C	PM-1008AZ/883C	RDC1711	None
HDM-1210	AD668/AD9713A	OP-08EJ	PM-1008EJ	RDC1721	AD2S46
HDS-0810E	AD9712A	OP-08EZ	PM-1008EZ	RDC1767	RDC1768
HDS-0820	AD9713A	OP-09ARC/883C	OP-11ARC/883C	RSCT1621	AD2S80A/82A
HDS-1015E	AD9712A	OP-09FY	OP-09EY	RTI-1200	RTI-711 Series
HDS-1025	AD9713A	OP-12BZ	OP-12AZ	RTI-1201	RTI-711 Series
HDS-1250	AD668/AD9713A	OP-12CZ	OP-12AZ	RTI-1202	RTI-711 Series
HOS-100AH/SH	None	OP-12GZ	OP-12FZ	RTM1630-34	RTM1680/83
HOS-200	AD9620/30	OP-14DZ	OP-14CZ	RTM1636	Consult ADI
HTC-0300	HTC-0300A	OP-14GRBC	OP-14GBC	RTM1660/63/71/72	Consult ADI
HTC-0500	HTC-0300A	OP-14J/883C	OP-14AJ/883C	RTM1679	None
IPA-1751	IPA-1764	OP-15BJ	OP-15AJ	RTM1681/86/87/89	Consult ADI
IRDC1730-33	AD2S80A/82A	OP-15BZ	OP-15AZ	RTM1690/96	Consult ADI
MAH-0801	AD9005	OP-16BJ	OP-16AJ	RTM1697	None
MAH-1001	AD9005	OP-17BZ/883C	OP-17AZ/883C	RTM1736/37	RDC1740 + CCT
MAS-0801	AD9005	OP-17CJ	OP-17AJ	SAC1763	None
MAS-1001	AD9005	OP-17FJ	OP-17EJ	SBCD1752/53/56/57	None
MAS-1202	AD9005	OP-17FZ	OP-17EZ	SCDX1623	None
MAT-01/883C	MAT-01AH/883C	OP-20CJ	OP-20BJ	SCM1677	None
MAT-02BH	MAT-02AH	OP-21GRBC	OP-21GBC	SDC1602/3/4	SDC1702/03/04/40
MAT-02BH/883C	MAT-02AH/883C	OP-215BJ	OP-215AJ	SDC1711	None
MATV-0811	AD9012/48	OP-215BJ/883C	OP-215AJ/883C	SDC1721	AD2S46
MATV-0816	AD9012/48	OP-215BZ	OP-215AZ	SDC1767	SDC1768
MATV-0820	AD9012/48	OP-215CZ/883C	OP-215BZ/883	SERDEX	µMAC-5000
MCI-1794	AD2S80A/82A	OP-21BJ	OP-21AJ	SHA-1A	AD585
MDA Family	AD9712A/13A	OP-21BZ	OP-21AZ	SHA-2A	AD781
MDH Family	AD9712A/13A	OP-21EJ	OP-21AJ	SHA-3	AD585
MDMS Family	AD9712A/13A	OP-220BJ	OP-220AJ	SHA-4	AD585
MDS Family	AD9712A/13A	OP-22AJ	OP-22AJ/883C	SHA-6	AD1154
MDSL Family	AD9712A/13A	OP-22EJ	OP-22AJ/883C	SHA1114	AD585
MOD-1005/20	AD9020/60	OP-32BZ	OP-32AZ	SMP-10BY	SMP-10AY
MUX-08AQ	MUX-08BQ	OP-32BZ/883C	OP-32AZ/883C	SMP-10BY/883C	SMP-10AY/883C
MUX-24AQ	MUX-24EQ	OP-32FZ	OP-32EZ	SPA-1695	None
MUX-24BQ	MUX-24FQ	OP-50BY	OP-50AY	SSCT1621	AD2S80A/82A
MUX-16AT	MUX-16ET	OP-50BY/883C	OP-50AY/883C	SSCT1622/23	None
MUX-16BT	MUX-16FT	OSC-1754	OSC-1758	STM1630-34	STM1680/83
OP-01HJ	OP-01J	PKD-01BY	PKD-01AY	STM1636	Consult ADI
OP-01HZ	OP-01HP	PKD-01BY/883C	PKD-01AY/883C	STM1660/63/71/72	Consult ADI
OP-02BJ	*OP-02AJ*	PM-111Y	PM-111J	STM1679	None
OP-02BJ/883C	OP-02AJ/883C	PM-11Y/883C	PM-111J/883C	STM1681/86/87/89	Consult ADI
OP-02EJ	OP-07DJ	PM-139AY	PM-139AY/883C	STM1690/96	Consult ADI
OP-02EP	OP-177GP	PM-156AZ	PM-156AZ/883C	STM1697	None

Model	Closest Recommended Equivalent
STM1736/37	SDC1740 + CCT
SW-01BQ	SW-01FQ
SW-7510AQ	SW-7510EQ
SW-7510BQ	SW-7510FQ
SW-7511AQ	SW-1577BQ
THC-Family	HTC-0300A
THS-Family	HTC-0300A
TSL1612	Consult ADI
1S10/20	1S40; AD2S80A/82A
1S14/24/44/64	1S74
1S61	1S60; AD2S80A/82A
2S20	AD2S80A/82A
5S70/5S72	AD2S75
9S70/71/72	None
9S75/76/79	None
41	AD515A
42	AD549
43	AD549
47	AD845
48	AD845
52	AD707
102	AD845
106	118
107	118
108	AD845
110	AD845
120	50
141	40
142	AD845
143	AD845
146	AD382
149	50
153	AD517
161	None
163	None
165	None
170	None
180	AD OP-07
183	184
220	234
230	235
231	233
232	235
233	None
260	AD707
272	None
273	None
276	None
274J	284J
279	286J
280	281
282J	292A
283J	292A
287	None
301	310 (Module)
302	310 (Module)

Model	Closest Recommended Equivalent
311	AD549
350	None
424	435/AD534
426	AD534
427	None
428	AD538
432	None
454	AD537
456	AD537
602J10	AD524
602J100	AD524
602K100	AD524
603	AD524
605	AD524
606	AD625
610	AD625
752	759
901	904
907	921
908	921
909	921
931	None
932	None
933	None
935	None
942	None
944	None
946	None
948	947
950	None
956	None
971	921

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MILITARY PRODUCTS DATABOOK—1990 (in two volumes) Information and data on products available with processing in accordance with MIL-STD-883.

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Volume 1: All other Analog Devices products

DATA-ACQUISITION AND CONTROL CATALOG—1990. Tutorial and Configuration Guide, with Product Reference and Index. Bus-Compatible I/O Boards for: IBM PS/2,* IBM PC/XT/AT,* STD Bus, VMEbus, MULTIBUS.† Distributed I/O Subsystems—fixed-function front ends, programmable units, and distributed control systems. Modular Signal Conditioners—analog and digitizing. Analog Signal-Conditioning Panels—isolated and nonisolated. Digital Subsystems—16- and 24/32-channel. Software—DOS drivers and applications packages.

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AD201	L
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AD203	L
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AD293	L
AD294	L
AD295	L
AD301	L
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AD365	L
AD367	D
AD368	D
AD369	D

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AD381	L
AD382	L
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AD504	L
AD506	L
AD509	L
AD510	L
AD515	L
AD515A	L
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AD518	L
AD521	L
AD522	L
AD524	L
AD526	L
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AD544	L
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AD592	L
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AD596/597	L
AD598	L
AD611	L
AD624	L
AD625	L
AD630	L
AD632	L
AD633	L
AD636	L
AD637	L
AD639	L
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•AD674B	C II 2–109
•AD675	C II 2–121
•AD676	C II 2–123
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AD693	L
AD694	L
AD704	L
AD705	L
AD706	L
AD707	L
AD708	L
AD711	L
AD712	L
AD713	L
AD734	L
AD736	L
AD737	L
AD741	L
AD743	L
AD744	L
AD746	L
•AD766	C I 2–151
AD767	C I 2–159
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•AD774B	C II 2–109
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•AD783	C II 4–65
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AD827	L
AD829	L
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AD840	L
AD841	L
AD842	L
AD843	L
AD844	L
AD845	L
AD846	L
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•AD1382	C II 2–239
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•AD1671	C II 2–259
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AD2040	D
AD2700	C II 6–75
AD2701	C II 6–75
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AD2710	C II 6–79
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AD3860	D
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AD5210 Series	D
AD5240	C II 2–809
AD5539	L
•AD7001	C I 4–47
•AD7002	C I 4–59
•AD7005	C I 4–75
•AD7008	C I 4–91
AD7110	D
AD7111	C I 2–247
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AD7224	C I 2–259
AD7225	C I 2–279
AD7226	C I 2–291
AD7228	C I 2–323
•AD7228A	C I 2–331
•AD7233	C I 2–339
AD7237	C I 2–347
AD7240	D
•AD7242	C I 2–359
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•AD7837	C I 2–681
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AD7872	C II 2–563
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•AD7875	C II 2–545
•AD7876	C II 2–545
AD7878	C II 2–595
•AD7880	C II 2–611
•AD7884	C II 2–625
•AD7885	C II 2–625
•AD7886	C II 2–637
•AD7890	C II 2–653
•AD7891	C II 2–659
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•AD7893	C II 2–669
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•AD9014	C II 2–729
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•AD9032	C II 2–765
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AD9501	L
AD9502	D
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•AD9713A	C I 2–761
•AD9720	C I 2–765
•AD9721	C I 2–765
AD9768	C I 2–769
AD9901	C I 4–115
•AD9950	C I 4–123
•AD22001	L
•AD22050	L
•AD22100	L
•AD22150	L
•AD22180	L
•AD22181	L
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•AD75089	C I 2–777
•AD75090	C I 2–777
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AD96687	L
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AD ADC80	C II 2–803
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ADC-910	C II 2–819
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•ADC-912A	C II 2–831
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ADC1140	C II 2–843
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AD DAC-08	D
AD DAC71	D
AD DAC72	D
AD DAC80	C I 2–783
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•ADDS-21XX-SW	D
•ADDS-2100A-ICE	D
ADDS-2101-ICE	D
•ADDS-2101-EZ	D
•ADDS-2111-EZ	D
ADG201A	C II 5–43
ADG201HS	C II 5–49
ADG202A	C II 5–43
ADG211A	C II 5–57
ADG212A	C II 5–57
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AD OP-27	L
AD OP-37	L
ADSP-824ROM	D
ADSP-1008A	D
ADSP-1009A	D
ADSP-1010A	D
ADSP-1010B	D
ADSP-1012A	D
ADSP-1016A	D
ADSP-1024A	D
ADSP-1080A	D
ADSP-1081A	D
ADSP-1101	D
ADSP-1110A	D
ADSP-1401	D
ADSP-1402	D
ADSP-1410	D
ADSP-2100	D
ADSP-2100A	C I 6–2
ADSP-2101	C I 6–2
ADSP-2102	C I 6–2
•ADSP-2105	C I 6–2
•ADSP-2106	C I 6–2
•ADSP-2111	C I 6–2
•ADSP-2112	C I 6–2
•ADSP-21msp50	C I 6–2
•ADSP-21msp51	C I 6–2
ADSP-3128A	D
ADSP-3201	D
ADSP-3202	D
ADSP-3210	D
ADSP-3211	D
ADSP-3212	D

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ADSP-3222	D
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ADV453	C I 2–799
ADV471	C I 2–839
•ADV473	C I 2–805
•ADV475	C I 2–827
ADV476	C I 2–817
•ADV477	C I 2–827
ADV478	C I 2–839
•ADV7120	C I 2–851
•ADV7121	C I 2–857
•ADV7122	C I 2–857
•ADV7141	C I 2–869
•ADV7146	C I 2–869
•ADV7148	C I 2–869
•ADV7150	C I 2–889
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AMP-02	P
AMP-03	P
AMP-05	P
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BUF-03	P
CAV-1210	D
CMP-01	P
CMP-02	P
CMP-04	P
CMP-05	P
CMP-08	P
CMP-404	P
DAC-QS	D
DAC-QZ	D
DAC-01	D
DAC-02/03	D
DAC-05	C I 11–4, C II 12–4
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DAC-08	C I 2–923
DAC-10	C I 2–935
DAC-10Z	D
DAC-12M	D
DAC-12QS	D
DAC-12QZ	D
•DAC-16	C I 2–943
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DAC-89	D
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DAC-312	C I 2–953
DAC-888	D
DAC1108	D
DAC1136	D
DAC1138	D
DAC1146	D
DAC-1408A	D
DAC1420	D
DAC1422	D
DAC1423	D
DAC-1508A	D
DAC-8012	C I 2–967
DAC-8043	C I 2–977
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DAC-8221	C I 2–1001
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DAC-8408	C I 2–1069
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•DAC-8413	C I 2–1083
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•DAC-8841	C I 2–1131
DAS1128	D
DAS1150	D
DAS1151	D
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DAS1156	D
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DRC1706	D
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LTS-0655	L
LTS-0680	L
LTS-2020	L
LTS-2101	L
LTS-2200	L
LTS-2302	L
LTS-2510	L
LTS-2600	L
LTS-2700	L
LTS-2800	L
MAT-01	P
MAT-02	P
MAT-03	P
MAT-04	P
MUX-08	C II 5–111
MUX-16	C II 5–123
MUX-24	C II 5–111
MUX-28	C II 5–123
MUX-88	D
OP-01	P
OP-02	P
OP-04	P
OP-05	P
OP-06	P
OP-07	P
OP-09	P
OP-10	P
OP-11	P
OP-12	P
OP-14	P
OP-15	P
OP-16	P
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OP-27	P
OP-32	P
OP-37	P
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OP-43	P
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OP-50	P
OP-61	P
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OP-207	P
OP-215	P
OP-220	P
OP-221	P
OP-227	P
OP-249	P
OP-260	P
OP-270	P
OP-271	P
•OP-282	P
OP-290	P
OP-297	P
OP-400	P
OP-420	P
OP-421	P
OP-470	P
OP-471	P
•OP-482	P
OP-490	P
•OSC1758	C I 3–117
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PM-108	P
PM-111	P
PM-119	P
PM-139	P
PM-148/248	P
PM-155	P
PM-155A	P
PM-156	P
PM-156A	P
PM-157	P
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PM-1008	P
PM-1012	P
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•PM-6012	C I 2–1141
PM-7224	C I 2–267
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PM-7628	C I 2–665
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REF-02	C II 6–91
REF-03	C II 6–99
REF-05	C II 6–107
REF-08	C II 6–113
REF-10	C II 6–121
REF-43	C II 6–127
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RPT-85	C I 4–155
RPT-86	C I 4–163
RPT-87	C I 4–163
RTM Series	D
SDC1700/RDC1700	D
SDC1702/RDC1702	D
SDC1704/RDC1704	D
SDC1725/RDC1725	D
SDC1726/RDC1726	D
SDC1740/RDC1740	C I 3–119
SDC1741/RDC1741	C I 3–119
SDC1742/RDC1742	C I 3–119
SDC1768/RDC1768	D
SHA-5	D
SHA-1134	D
SHA-1144	D
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SMP-10	C II 4–109
SMP-11	C II 4–109
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SMP-81	D
SSM-2013	P
SSM-2014	P
SSM-2015	P
SSM-2016	P
SSM-2017	P
SSM-2018	P
SSM-2024	P
SSM-2100	P
SSM-2110	P
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SSM-2122	P
SSM-2131	P
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SSM-2141	P
SSM-2142	P
SSM-2210	P
SSM-2220	P
SSM-2300	P
SSM-2402	C II 5–133
●SSM-2404	C II 5–147
SSM-2412	C II 5–133
STM Series	D
SW-01	D
SW-02	D
SW-06	C II 5–149
SW-201	C II 5–161
SW-202	C II 5–161
SW-7510	D
SW-7511	D
1B21	L
1B22	L
1B31	L
1B32	L
1B41	L
1B51	L
●1S74	C 3–127
2B20	L
2B22	L
2B23	L
2B24	L
2B30	L
2B31	L
2B34	L
2B35	L
2B50	L
2B52	L
2B53	L
2B54/2B55	L
2B56	L
2B57	L
2B58	L
2B59	L
2S50	C I 3–135
2S54	C I 3–137
2S56	C I 3–137
2S58	C I 3–137
2S80A	C I 3–55
2S81A	C I 3–71
2S82A	C I 3–71
3B Series	L
4B Series	L
5B Series	L
6B Series	L
●7B Series	L
40	L

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Model	Page*
44	L
45	L
46	L
50	L
51	L
118	L
148	L
171	L
184	L
234	L
235	L
261	L
275	L
277	L
281	L
284J	L
285	L
286J	L
288	L
289	L
290A	L
292A	L
310	L
429	L
433	L
434	L
435	L
436	L
440	L
442	L
450	D
451	D
452	D
453	D
458	D
460	D
741A/PM741	P
751	D
755	L
756	L
757	L
759	L
902/902-2	C I 9–1, C II 10–1
903	D
904	C I 9–1, C II 10–1
905	C I 9–1, C II 10–1
906	D
915	D
920	C I 9–1, C II 10–1
921	C I 9–1, C II 10–1
922	C I 9–1, C II 10–1
923	C I 9–1, C II 10–1

Model	Page*
925	C I 9–1, C II 10–1
926	D
927	C I 9–1, C II 10–1
928	C I 9–1, C II 10–1
940	C I 9–2, C II 10–2
941	C I 9–2, C II 10–2
943	C I 9–2, C II 10–2
945	C I 9–2, C II 10–2
947	D
949	C I 9–2, C II 10–2
951	C I 9–2, C II 10–2
952	C I 9–1, C II 10–1
953	C I 9–2, C II 10–2
955	C I 9–1, C II 10–1
958	C I 9–2, C II 10–2
959	D
960	C I 9–2, C II 10–2
962	C I 9–2, C II 10–2
964	C I 9–2, C II 10–2
965	C I 9–2, C II 10–2
966	C I 9–2, C II 10–2
967	C I 9–2, C II 10–2
968	D
970	C I 9–1, C II 10–1
972	D
973	C I 9–1, C II 10–1
974	C I 9–1, C II 10–1
975	C I 9–1, C II 10–1
976	C I 9–1, C II 10–1
977	C I 9–1, C II 10–1

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Model	Page*
44	L
45	L
46	L
50	L
51	L
118	L
146	L
171	L
184	L
234	L
235	L
251	L
275	L
277	L
281	L
2841	L
285	L
2861	L
288	L
289	L
290A	L
292A	L
310	L
429	L
433	L
434	L
435	L
436	L
440	L
442	L
450	D
451	D
452	D
453	D
458	D
460	D
741A/B/M741	P
751	D
755	L
756	L
757	L
759	L
902/902-2	C I 9-1, C II 10-1
903	D
904	C I 9-1, C II 10-1
905	C I 9-1, C II 10-1
906	D
915	D
920	C I 9-1, C II 10-1
921	C I 9-1, C II 10-1
922	C I 9-1, C II 10-1
923	C I 9-1, C II 10-1
925	C I 9-1, C II 10-1
926	D
927	C I 9-1, C II 10-1
928	C I 9-1, C II 10-1
940	C I 9-2, C II 10-2
941	C I 9-2, C II 10-2
943	C I 9-2, C II 10-2
945	C I 9-2, C II 10-2
947	D
949	C I 9-2, C II 10-2
951	C I 9-2, C II 10-2
952	C I 9-1, C II 10-1
953	C I 9-2, C II 10-2
955	C I 9-1, C II 10-1
958	C I 9-2, C II 10-2
959	D
960	C I 9-2, C II 10-2
962	C I 9-2, C II 10-2
964	C I 9-2, C II 10-2
965	C I 9-2, C II 10-2
966	C I 9-2, C II 10-2
967	C I 9-2, C II 10-2
968	D
970	C I 9-1, C II 10-1
972	D
973	C I 9-1, C II 10-1
974	C I 9-1, C II 10-1
975	C I 9-1, C II 10-1
976	C I 9-1, C II 10-1
977	C I 9-1, C II 10-1